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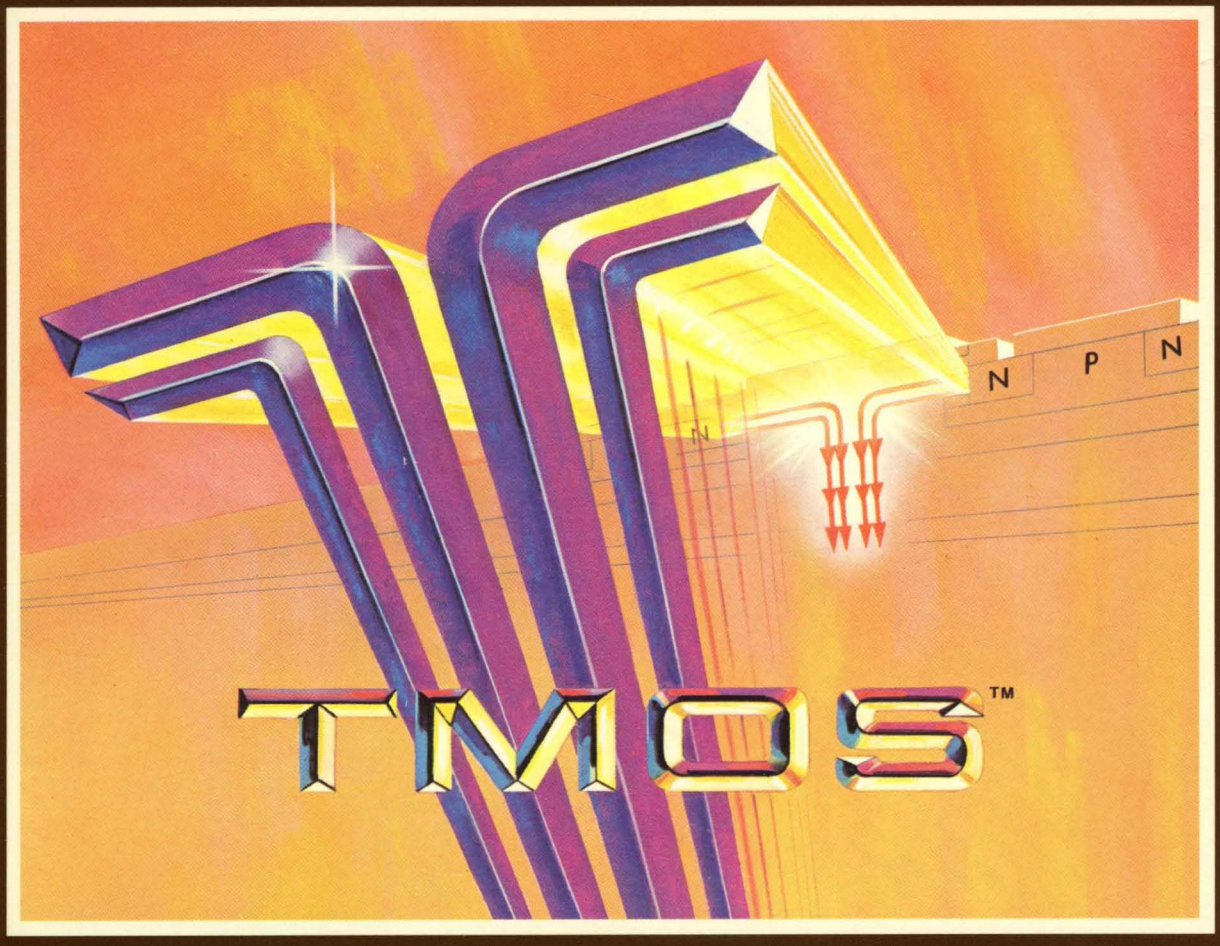
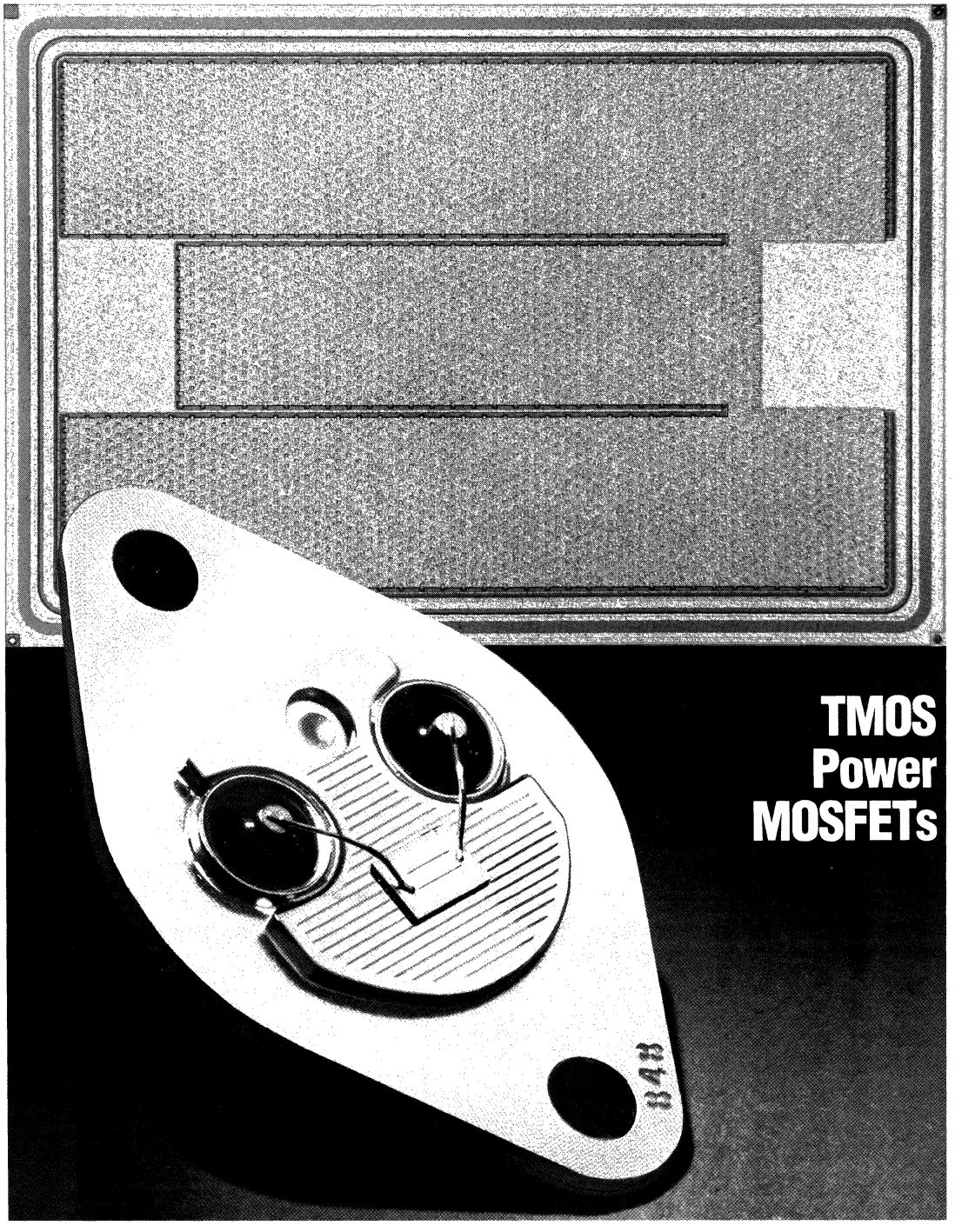
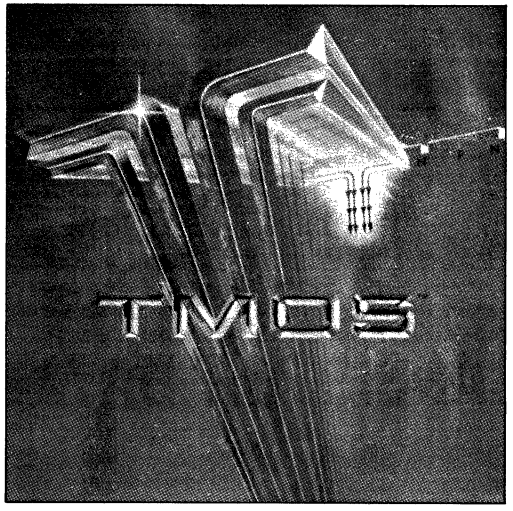


POWER MOSFET TRANSISTOR DATA


TMOS
Power
MOSFETs



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POWER MOSFET TRANSISTOR DATA

Prepared by
Technical Information Center

Preface

After several years of development, Motorola introduced its first power MOSFETs in 1980. Several technologies were evaluated and the final choice was the double diffused (DMOS) process which Motorola has acronymed TMOS. This process is highly manufacturable and is capable of producing devices with the best characteristics for product needed for power control. Most suppliers of power MOSFETs use the basic DMOS process.

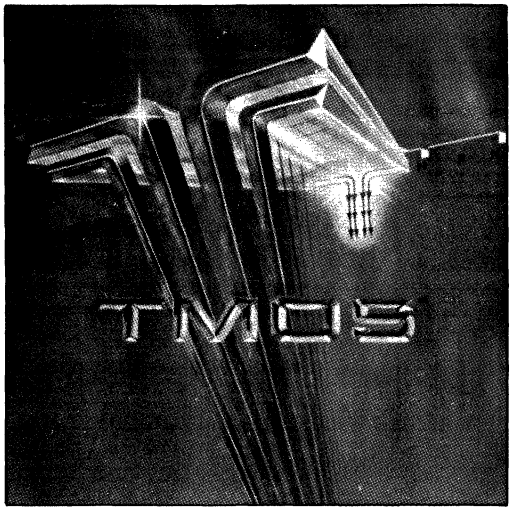
The key to success of power MOSFETs is the control of vertical current flow, which enables suppliers to reduce chip sizes comparable to bipolar transistors. This development opens a new dimension for designers of power control systems.

This manual is intended to give the users of power MOSFETs the basic information on the product, application ideas of power MOSFETs and data sheets of the broadest line of power MOSFETs with over 225 device types in eleven package configurations currently available from Motorola. Chips for hybrid circuits are also available on all the products included in this manual. The product offering is far from complete. New products will be introduced . . . doubling the product offering in the next year, offering designers an even better selection of products for their designs.

Motorola has a long history of supplying high quality power transistors in large volume to the automotive, television, industrial and computer markets. Being the leading supplier of power transistors in the world, we know how to serve our customers' needs.

First Edition

Printed in U.S.A.



Theory and Applications Chapters 1 through 13

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A

Chapter 1: Symbols, Terms and Definitions

The following are the most commonly used letter symbols, terms and definitions associated with Power MOSFETs.

Symbol	Term	Definition
C_{ds}	drain-source capacitance	The capacitance between the drain and source terminals with the gate terminal connected to the guard terminal of a three-terminal bridge.
C_{dg}	drain-gate capacitance	The same as C_{rss} — See C_{rss}.
C_{gs}	gate-source capacitance	The capacitance between the gate and source terminals with the drain terminal connected to the guard terminal of a three-terminal bridge.
C_{iss}	short-circuit input capacitance, common-source	The capacitance between the input terminals (gate and source) with the drain short-circuited to the source for alternating current. (Ref. IEEE No. 255)
C_{oss}	short-circuit output capacitance, common-source	The capacitance between the output terminals (drain and source) with the gate short-circuited to the source for alternating current. (Ref. IEEE No. 255)
C_{rss}	short-circuit reverse transfer capacitance, common-source	The capacitance between the drain and gate terminals with the source connected to the guard terminal of a three-terminal bridge.
g_{fs}	common-source small-signal transconductance	The ratio of the change in drain current due to a change in gate-to-source voltage
I_D	drain current, dc	The direct current into the drain terminal.
$I_{D(on)}$	on-state drain current	The direct current into the drain terminal with a specified forward gate-source voltage applied to bias the device to the on-state.
I_{DSS}	zero-gate-voltage drain current	The direct current into the drain terminal when the gate-source voltage is zero. This is an on-state current in a depletion-type device, an off-state in an enhancement-type device.
I_G	gate current, dc	The direct current into the gate terminal.
I_{GSS}	reverse gate current, drain short-circuited to source	The direct current into the gate terminal of a junction-gate field-effect transistor when the gate terminal is reverse biased with respect to the source terminal and the drain terminal is short-circuited to the source terminal.

Symbol	Term	Definition
I_{GSSF}	forward gate current, drain short-circuited to source	The direct current into the gate terminal of an insulated-gate field-effect transistor with a forward gate-source voltage applied and the drain terminal short-circuited to the source terminal.
I_{GSSR}	reverse gate current, drain short-circuited to source	The direct current into the gate terminal of an insulated-gate field-effect transistor with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal.
I_S	source current, dc	The direct current into the source terminal.
P_T, P_D	total nonreactive power input to all terminals	The sum of the products of the dc input currents and voltages.
$r_{DS(on)}$	static drain-source on-state resistance	The dc resistance between the drain and source terminals with a specified gate-source voltage applied to bias the device to the on state.
$R_{\theta CA}$	thermal resistance, case-to-ambient	The thermal resistance (steady-state) from the device case to the ambient.
$R_{\theta JA}$	thermal resistance, junction-to-ambient	The thermal resistance (steady-state) from the semiconductor junction(s) to the ambient.
$R_{\theta JC}$	thermal resistance, junction-to-case	The thermal resistance (steady-state) from the semiconductor junction(s) to a stated location on the case.
$R_{\theta JM}$	thermal resistance, junction-to-mounting surface	The thermal resistance (steady-state) from the semiconductor junction(s) to a stated location on the mounting surface.
T_A	ambient temperature or free-air temperature	The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.
T_C	case temperature	The temperature measured at a specified location on the case of a device.
t_c	turn-off crossover time	The time interval during which drain voltage rises from 10% of its peak off-state value and drain current falls to 10% of its peak on-state value, in both cases ignoring spikes that are not charge-carrier induced.
T_J	channel temperature	The temperature of the channel of a field-effect transistor.
T_{stg}	storage temperature	The temperature at which the device, without any power applied, may be stored.
$t_{d(off)}$	turn-off delay time	Synonym for current turn-off delay time (see Note 1)*.
$t_{d(off)i}$	current turn-off delay time	The interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain current waveform falls to 90% of its on-state amplitude, ignoring spikes that are not charge-carrier induced.
$t_{d(off)v}$	voltage turn-off delay time	The time interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain voltage waveform rises to 10% of its off-state amplitude, ignoring spikes that are not charge-carrier induced.
$t_{d(on)}$	turn-on delay time	Synonym for current turn-on delay time (see Note 1)*.

Symbol	Term	Definition
$t_{d(on)i}$	current turn-on delay time	The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the drain current waveform rises to 10% of its on-state amplitude, ignoring spikes that are not charge-carrier induced.
$t_{d(on)v}$	voltage turn-on delay time	The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the drain voltage waveform falls to 90% of its off-state amplitude, ignoring spikes that are not charge-carrier induced.
t_f	fall time	Synonym for current fall time (See Note 1)*.
t_{fi}	current fall time	The time interval during which the drain current changes from 90% to 10% of its peak off-state value, ignoring spikes that are not charge-carrier induced.
t_{fv}	voltage fall time	The time interval during which the drain voltage changes from 90% to 10% of its peak off-state value, ignoring spikes that are not charge-carrier induced.
t_{off}	turn-off time	Synonym for current turn-off time (see Note 1)*.
$t_{off(i)}$	current turn-off time	The sum of current turn-off delay time and current fall time, i.e., $t_{d(off)i} + t_{fi}$.
$t_{off(v)}$	voltage turn-off time	The sum of voltage turn-off delay time and voltage rise time, i.e., $td(off)v + t_{rv}$.
t_{on}	turn-on time	Synonym for current turn-on time (See Note 1)*.
$t_{on(i)}$	current turn-on time	The sum of current turn-on delay time and current rise time, i.e., $t_{d(on)i} + t_{ri}$.
$t_{on(v)}$	voltage turn-on time	The sum of voltage turn-on delay time and voltage fall time, i.e., $t_{d(on)v} + t_{fv}$.
t_p	pulse duration	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform. **Note:** The two reference points are usually 90% of the steady-state amplitude of the waveform existing after the leading edge, measured with respect to the steady-state amplitude existing before the leading edge. If the reference points are 50% points, the symbol t_w and term average pulse duration should be used.
t_r	rise time	Synonym for current rise time (See Note 1)*.
t_{ri}	current rise time	The time interval during which the drain current changes from 10% to 90% of its peak on-state value, ignoring spikes that are not charge-carrier induced.
t_{rv}	voltage rise time	The time interval during which the drain voltage changes from 10% to 90% of its peak off-state value, ignoring spikes that are not charge-carrier induced.
t_{ti}	current tail time	The time interval following current fall time during which the drain current changes from 10% to 2% of its peak on-state value, ignoring spikes that are not charge-carrier induced.

Symbol	Term	Definition
t_w	average pulse duration	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform, with both reference points being 50% of the steady-state amplitude of the waveform existing after the leading edge, measured with respect to the steady-state amplitude existing before the leading edge. **Note:** If the reference points are not 50% points, the symbol t_p and term pulse duration should be used.
$V_{(BR)DSR}$	drain-source breakdown voltage with (resistance between gate and source)	The breakdown voltage between the drain terminal and the source terminal when the gate terminal is (as indicated by the last subscript letter) as follows: R = returned to the source terminal through a specified resistance. S = short-circuited to the source terminal. V = returned to the source terminal through a specified voltage. X = returned to the source terminal through a specified circuit.
$V_{(BR)DSS}$	gate short-circuited to source	
$V_{(BR)DSV}$	voltage between gate and source	
$V_{(BR)DSX}$	circuit between gate and source	
$V_{(BR)GSSF}$	forward gate-source breakdown voltage	The breakdown voltage between the gate and source terminals with a forward gate-source voltage applied and the drain terminal short-circuited to the source terminal.
$V_{(BR)GSSR}$	reverse gate-source breakdown voltage	The breakdown voltage between the gate and source terminals with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal.
V_{DD}, V_{GG} V_{SS}	supply voltage, dc (drain, gate, source) voltage	The dc supply voltage applied to a circuit or connected to the reference terminal.
V_{DG} V_{DS} V_{GD} V_{GS} V_{SD} V_{SG}	drain-to-gate drain-to-source gate-to-drain gate-to-source source-to-drain source-to-gate	The dc voltage between the terminal indicated by the first subscript and the reference terminal indicated by the second subscript (stated in terms of the polarity at the terminal indicated by the first subscript).
$V_{DS(on)}$	drain-source on-state voltage	The voltage between the drain and source terminals with a specified forward gate-source voltage applied to bias the device to the on state.
$V_{GS(th)}$	gate-source threshold voltage	The forward gate-source voltage at which the magnitude of the drain current of an enhancement-type field-effect transistor has been increased to a specified low value.
$Z_{\theta JA(t)}$	transient thermal impedance, junction-to-ambient	The transient thermal impedance from the semiconductor junction(s) to the ambient.
$Z_{\theta JC(t)}$	transient thermal impedance, junction-to-case	The transient thermal impedance from the semiconductor junction(s) to a stated location on the case.

Note 1: As names of time intervals for characterizing switching transistors, the terms "fall time" and "rise time" always refer to the change that is taking place in the magnitude of the output current even though measurements may be made using voltage waveforms. In a purely resistive circuit, the (current) rise time may be considered equal and coincident to the voltage fall time and the (current) fall time may be considered equal and coincident to the voltage rise time. The delay times for current and voltage will be equal and coincident. When significant amounts of inductance are present in a circuit, these equalities and coincidences no longer exist, and use of the unmodified terms delay time, fall time, and rise time must be avoided.

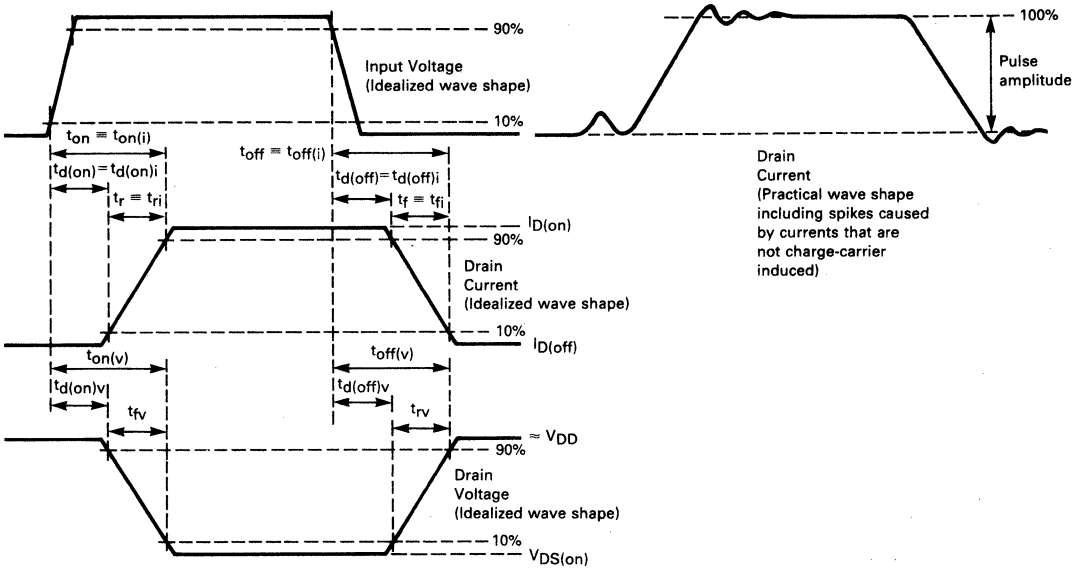
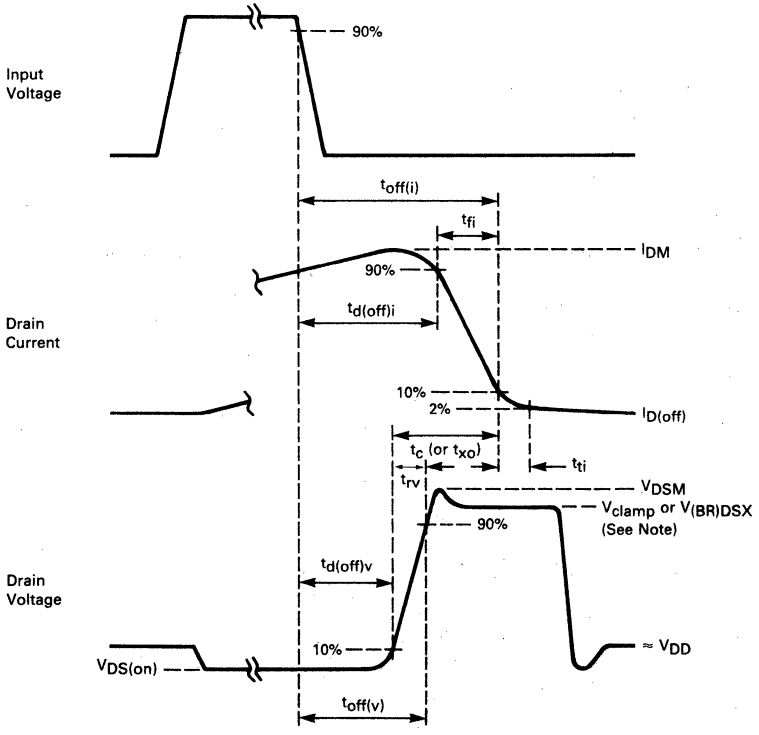


FIGURE 1-1 — WAVEFORMS FOR RESISTIVE-LOAD SWITCHING



NOTE: V_{clamp} (in a clamped inductive-load switching circuit) or $V_{(BR)DSX}$ (in an unclamped circuit) is the peak off-state voltage excluding spikes.

FIGURE 1-2 — WAVEFORMS FOR INDUCTIVE LOAD SWITCHING, TURN-OFF

Basic TMOS Structure, Operation and Physics

Structures:

Motorola's TMOS Power MOSFET family is a matrix of diffused channel, vertical, metal-oxide-semiconductor power field-effect transistors which offer an exceptionally wide range of voltages and currents with low $r_{DS(on)}$. The inherent advantages of Motorola's power MOSFETs include:

- Nearly infinite static input impedance featuring:
  - — Voltage driven input
  - — Low input power
  - — Few driver circuit components
- Very fast switching times
  - — No minority carriers
  - — Minimal turn-off delay time
  - — Large reversed biased safe operating area
  - — High gain bandwidth product
- Positive temperature coefficient of on-resistance
  - — Large forward biased safe operating area
  - — Ease in paralleling
- Almost constant transconductance
- High dv/dt immunity
- Low Cost

Motorola's TMOS power MOSFET line is the latest step in an evolutionary progression that began with the conventional small-signal MOSFET and superseded the intermediate lateral double diffused MOSFET (LDMOSFET) and the vertical V-groove MOSFET (VMOSFET).

The conventional small-signal lateral N-channel MOSFET consists of a lightly doped P-type substrate into which two highly doped N^+ regions are diffused, as shown in Figure 1-3. The N^+ regions act as source and drain which are separated by a channel whose length is determined by photolithographic constraints. This configuration resulted in long channel lengths, low current capability, low reverse blocking voltage and high $r_{DS(on)}$.

Two major changes in the small-signal MOSFET structure were responsible for the evolution of the power MOSFET. One was the use of self aligned, double diffusion techniques to achieve very short channel lengths, which allowed higher channel packing densities, resulting in higher current capability and lower $r_{DS(on)}$. The other was the incorporation of a lightly doped N^+ region between the channel and the N^+ drain allowing high reverse blocking voltages.

These changes resulted in the lateral double diffused MOSFET power transistor (LDMOS) structure shown in Figure 1-4, in which all the device terminals are still on the top surface of the die. The major disadvantage of this configuration is its inefficient use of silicon area due to the area needed for the top drain contact.

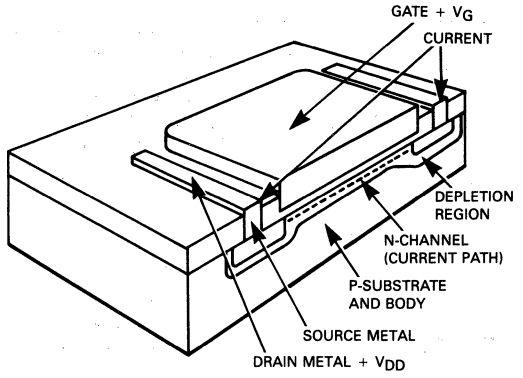


FIGURE 1-3 — CONVENTIONAL SMALL-SIGNAL MOSFET HAS LONG LATERAL CHANNEL RESULTING IN RELATIVELY HIGH DRAIN-TO-SOURCE RESISTANCE.

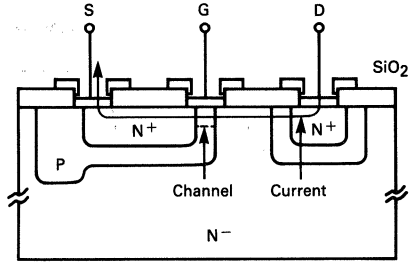


FIGURE 1-4 — LATERAL DOUBLE DIFFUSED MOSFET STRUCTURE FEATURING SHORT CHANNEL LENGTHS AND HIGH PACKING DENSITIES FOR LOWER ON RESISTANCE.

The next step in the evolutionary process was a vertical structure in which the drain contact was on the back of the die, further increasing the channel packing density. The initial concept used a V-groove MOSFET power transistor as shown in Figure 1-5. The channels in this device are defined by preferentially etching V-grooves through double diffused N^+ and P^- regions. The requirements of adequate packing density, efficient silicon usage and adequate reverse blocking voltage are all met by this configuration. However, due to its non-planar structure, process consistency and cleanliness requirements resulted in higher die costs.

The cell structure chosen for Motorola's TMOS power MOSFET's is shown in Figure 1-6. This structure is similar to that of Figure 1-4 except that the drain contact is dropped through the N^- substrate to the back of the die. The gate structure is now made with polysilicon sandwiched between two oxide layers and the source metal

applied continuously over the entire active area. This two layer electrical contact gives the optimum in packing density and maintains the processing advantages of planar LDMOS. This results in a highly manufacturable process which yields low $r_{DS(on)}$ and high voltage product.

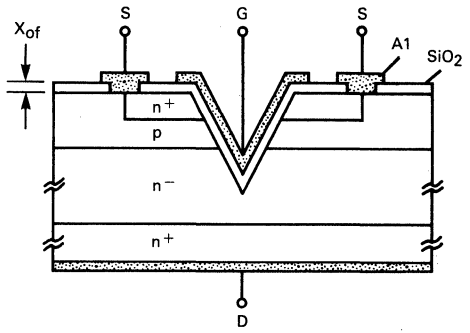


FIGURE 1-5 — V-GROOVE MOSFET STRUCTURE HAS SHORT VERTICAL CHANNELS WITH LOW DRAIN-TO-SOURCE RESISTANCE.

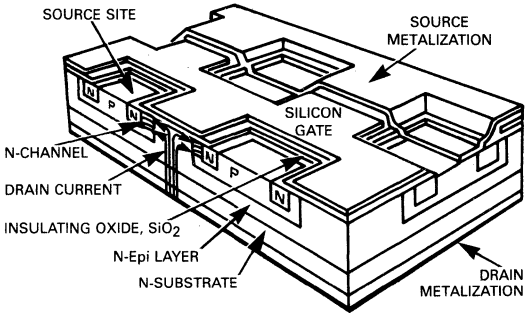


FIGURE 1-6 — TMOS POWER MOSFET STRUCTURE OFFERS VERTICAL CURRENT FLOW, LOW RESISTANCE PATHS AND PERMITS COMPACT METALIZATION ON TOP AND BOTTOM SURFACES TO REDUCE CHIP SIZE.

Operation:

Transistor action and the primary electrical parameters of Motorola's TMOS power MOSFET can be defined as follows:

Drain Current, I_D:

When a gate voltage of appropriate polarity and magnitude is applied to the gate terminal, the polysilicon gate induces an inversion layer at the surface of the diffused channel region represented by r_{CH} in Figure 1-7 (page A-8). This inversion layer or channel connects the source to the lightly doped region of the drain and current begins to flow. For small values of applied drain-to-source voltage, V_{DS}, drain current increases linearly and can be represented by Equation (1).

$$(1)\quad I_D \approx \frac{Z}{L}\,\mu Co\,[V_{GS} - V_{GS(th)}]\,V_{DS}$$

As the drain voltage is increased, the drain current saturates and becomes proportional to the square of the applied gate-to-source voltage, V_{GS}, as indicated in Equation (2).

$$(2)\quad I_D \approx \frac{Z}{2L}\,\mu Co\,[V_{GS} - V_{GS(th)}]^2$$

Where μ = Carrier Mobility
Co = Gate Oxide Capacitance per unit area
Z = Channel Width
L = Channel Length

These values are selected by the device design engineer to meet design requirements and may be used in modeling and circuit simulations. They explain the shape of the output characteristics discussed in Chapter 2.

Transconductance, g_{fs}:

The transconductance or gain of the TMOS power MOSFET is defined as the ratio of the change in drain current and an accompanying small change in applied gate-to-source voltage and is represented by Equation (3).

$$(3)\ g_{fs} = \frac{\Delta I_{D(sat)}}{\Delta V_{GS}} = \frac{Z}{L}\,\mu Co\,[V_{GS} - V_{GS(th)}]$$

The parameters are the same as above and demonstrate that drain current and transconductance are directly related and are a function of the die design. Note that transconductance is a linear function of the gate voltage, an important feature in amplifier design.

Threshold Voltage, $V_{GS(th)}$

Threshold voltage is the gate-to-source voltage required to achieve surface inversion of the diffused channel region, (r_{CH} in Figure 1-7 page A-8) and as a result, conduction in the channel.

As the gate voltage increases the more the channel is "enhanced," or the lower its resistance (r_{CH}) is made, the more current will flow. Threshold voltage is measured at a specified value of current to maintain measurement correlations. A value of 1.0 mA is common throughout the industry. This value is primarily a function of the gate oxide thickness and channel doping level which are chosen during the die design to give a high enough value to keep the device off with no bias on the gate at high temperatures. A minimum value of 1.5 volts at room temperature will guarantee the transistor remains an enhancement mode device at junction temperatures up to 150°C.

On-Resistance, $r_{DS(on)}$:

On-resistance is defined as the total resistance encountered by the drain current as it flows from the drain terminal to the source terminal. Referring to Figure 1-7, $r_{DS(on)}$ is composed primarily of four resistive components associated with:

The Inversion channel, r_{CH}; the Gate-Drain Accumulation Region, r_{ACC}; the junction FET Pinch region, r_{JFET}; and the lightly doped Drain Region, r_D, as indicated in Equation (4).

$$(4)\ r_{DS(on)} = r_{CH} + r_{ACC} + r_{JFET} + r_D$$

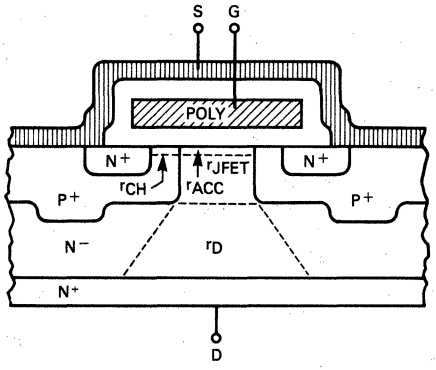


FIGURE 1-7 — TMOS DEVICE ON-RESIDENCE

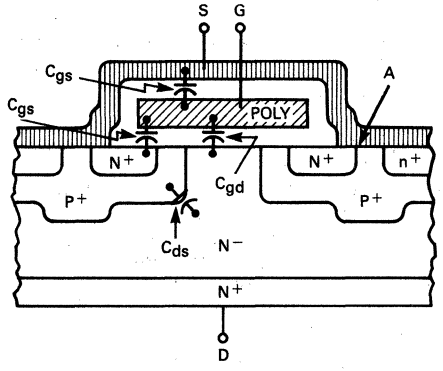


FIGURE 1-8 — TMOS DEVICE PARASITIC CAPACITANCES

Whereas the channel resistance increases with channel length, the accumulation resistance increases with poly width and the JFET pinch resistance increases with epi resistivity and all three are inversely proportional to the channel width and gate-to-source voltage. The drain resistance is proportional to the epi resistivity, poly width and inversely proportional to channel width. This says that the on-resistance of TMOS power FETs with the thick and high resistivity epi required for high voltage parts will be dominated by r_D.

Low voltage devices have thin, low resistivity epi and r_{CH} will be a large portion of the total on-resistance. This is why high voltage devices are "full on" with moderate voltages on the gate, whereas with low voltage devices the on-resistance continues to decrease as V_{GS} is increased toward the maximum rating of the device.

Note: $r_{DS(on)}$ is inversely proportional to the carrier mobility. This means that the $r_{DS(on)}$ of the P-Channel MOSFET is approximately 2.5 to 3.0 times that of a similar N-Channel MOSFET. Therefore, in order to have matched complementary on characteristics, the Z/L ratio of the P-Channel device must be 2.5–3.0 times that of the N-Channel device. This means larger die are required for P-Channel MOSFET's with the same $r_{DS(on)}$ and same breakdown voltage as an N-Channel device and thus device capacitances and costs will be correspondingly higher.

Breakdown Voltage, $V_{(BR)DSS}$:

Breakdown voltage or reverse blocking voltage of the TMOS power MOSFET is defined in the same manner as $V_{(BR)CES}$ in the bipolar transistor and occurs as an avalanche breakdown. This voltage limit is reached when the carriers within the depletion region of the reverse biased P-N junction acquire suffficient kinetic energy to cause ionization or when the critical electric field is reached. The magnitude of this voltage is determined mainly by the characteristics of the lightly doped drain region and the type of termination of the die's surface electric field.

Figure 1-9 shows a schematic representation of the cross-section in Figure 1-8 and depicts the bipolar transistor built in the epi layer. Point A shows where the emitter and base of the bipolar is shorted together. This is why $V_{(BR)DSS}$ of the power FET is equal to $V_{(BR)CES}$ of the bipolar. Also note the short brings the base in contact with the source metal allowing the use of the base-collector junction. This is the diode across the TMOS power MOSFET.

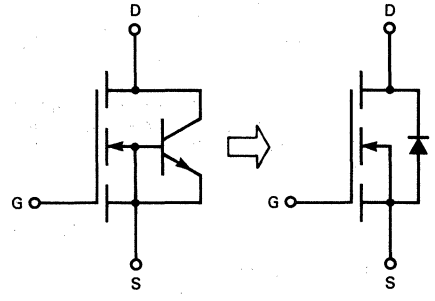


FIGURE 1-9 — SCHEMATIC DIAGRAM OF ALL THE COMPONENTS OF THE CROSS SECTION OF FIGURE 1-7.

TMOS Power MOSFET Capacitances:

Two types of intrinsic capacitances occur in the TMOS power MOSFET — those associated with the MOS structure and those associated with the P-N junction.

The two MOS capacitances associated with the MOSFET cell are:

Gate-Source Capacitance, C_{gs}

Gate-Drain Capacitance, C_{gd}

The magnitude of each is determined by the die geometry and the oxides associated with the silicon gate.

The P-N junction formed during fabrication of the power MOSFET results in the drain-to-source capacitance, C_{ds}. This capacitance is defined the same as any other planar junction capacitance and is a direct function of the channel drain area and the width of the reverse biased junction depletion region.

The dielectric insulator of C_{gs} and C_{gd} is basically a glass. Thus these are very stable capacitors and will not vary with voltage or temperature. If excessive voltage is placed on the gate, breakdown will occur through the glass, creating a resistive path and destroying MOSFET operation.

Optimizing TMOS Geometry:

The geometry and packing density of Motorola's MOSFETs vary according to the magnitude of the reverse blocking voltage.

The geometry of the source site, as well as the spacing between source sites, represents important factors in efficient power MOSFET design. Both parameters determine the channel packing density, i.e.: ratio of channel width per cell to cell area.

For low voltage devices, channel width is crucial for minimizing $r_{DS(on)}$, since the major contributing component of $r_{DS(on)}$ is r_{CH}. However, at high voltages, the major contributing component of resistance is r_D and thus minimizing $r_{DS(on)}$ is dependent on maximizing the ratio of active drain area per cell to cell area. These two conditions for minimizing $r_{DS(on)}$ cannot be met by a single geometry pattern for both low and high voltage devices.

Distinct Advantages of Power MOSFETs

Power MOSFETs offer unique characteristics and capabilities that are not available with bipolar power transistors. By taking advantage of these differences, overall systems cost savings can result without sacrificing reliability.

Speed

Power MOSFETs are majority carrier devices, therefore their switching speeds are inherently faster. Without the minority carrier stored base charge common in bipolar transistors, storage time is eliminated. The high switching speeds allow efficient switching at higher frequencies which reduces the cost, size and weight of reactive components.

MOSFET switching speeds are primarily dependent on charging and discharging the device capacitances and are essentially independent of operating temperature.

Input Characteristics

The gate of a power MOSFET is electrically isolated from the source by an oxide layer that represents a dc resistance greater than 40 megohms. The devices are fully biased-on with a gate voltage of 10 volts. This significantly simplifies the drive circuits and in many instances the gate may be driven directly from logic integrated circuits such as CMOS and TTL to control high power circuits directly.

Since the gate is isolated from the source, the drive requirements are nearly independent of the load current. This reduces the complexity of the drive circuit and results in overall system cost reduction.

Safe Operating Area

Power MOSFETs unlike bipolars, do not require derating of power handling capability as a function of applied voltage. The phenomena of second breakdown does not occur within the ratings of the device. Depending on the application, snubber circuits may be eliminated or a smaller capacitance value may be used in the snubber circuit. The safe operating boundaries are limited by the peak current ratings, breakdown voltages and the power capabilities of the devices.

On-Voltage

The minimum on-voltage of a power MOSFET is determined by the device on-resistance $r_{DS(on)}$. For low voltage devices the value of $r_{DS(on)}$ is extremely low, but with high voltage devices the value increases. $r_{DS(on)}$ has a positive temperature coefficient which aids in paralleling devices. Because of the positive temperature coefficient of $r_{DS(on)}$ and the negative temperature coefficient of transconductance, power MOSFET circuits are inherently less susceptible to thermal runaway.

Examples of Advantages Offered by MOSFETs

High Voltage Flyback Converter

An obvious way of showing the advantages of power MOSFETs over bipolars is to compare the two devices in the same system. Since the drive requirements are not the same, it is not a question of simply replacing the bipolar with the FET, but one of designing the respective drive circuits to produce an equivalent output, as described in Figures 1-10 and 1-11.

For this application, a peak output voltage of about 700 V driving a 30 kΩ load ($P_{O(pk)} \approx 16$ W) was required. With the component values and timing shown, the inductor/device current required to generate this flyback voltage would have to ramp up to about 3.0 A.

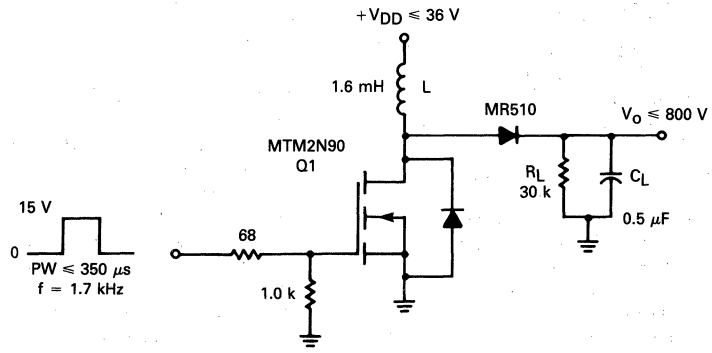


FIGURE 1-10 — TMOS OUTPUT STAGE

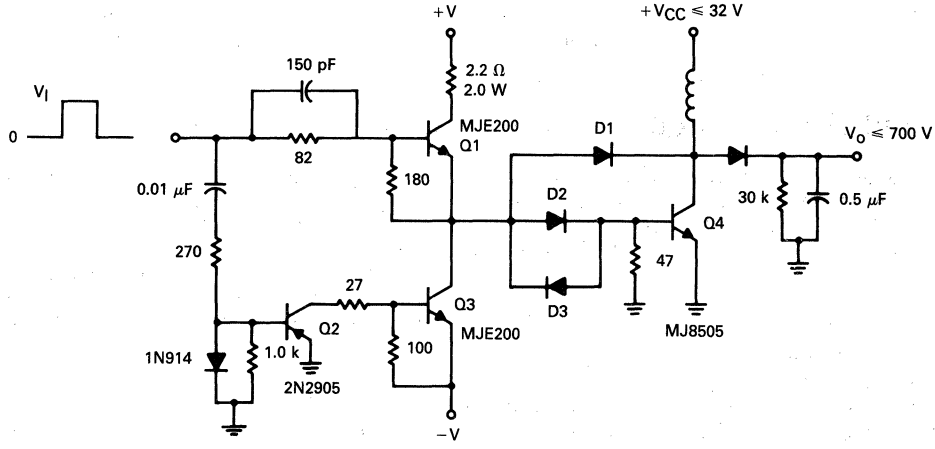


FIGURE 1-11 — BIPOLAR DRIVER AND OUTPUT STAGE

FIGURES 1-10 AND 1-11 — CIRCUIT CONFIGURATIONS FOR A TMOS AND BIPOLAR OUTPUT STAGE OF A HIGH VOLTAGE FLYBACK CONVERTER

Figure 1-10 shows the TMOS version. Because of its high input impedance, the FET, an MTM2N90, can be directly driven from the pulse width modulator. However, the PWM output should be about 15 volts in amplitude and for relatively fast FET switching be capable of sourcing and sinking 100 mA. Thus, all that is required to drive the FET is a resistor or two. The peak drain current of 3.2 A is within the MTM2N90 pulsed current rating of 7.0 A (2.0 A continuous), and the turn-off load line of 3.2 A, 700 V is well within the Switching SOA (7.0 A, 900 V) of the device. Thus, the circuit demonstrates the advantages of TMOS:

- High input impedance
- Fast Switching
- No Second breakdown

Compare this circuit with the bipolar version of Figure 1-11.

To achieve the output voltage, using a high voltage Switchmode MJ8505 power transistor, requires a rather complex drive circuit for generating the proper I_{B1} and I_{B2}. This circuit uses three additional transistors (two of which are power transistors), three Baker clamp diodes, eleven passive components and a negative power supply for generating an off-bias voltage. Also, the RBSOA capability of this device is only 3.0 A at 900 V and 4.7 A at 800 V, values below the 7.0 A, 900 V rating of the MOSFET. A detailed description of these circuits is shown in Chapter 7, TMOS applications.

20 kHz Switcher

An example of TMOS advantage over bipolar that il-

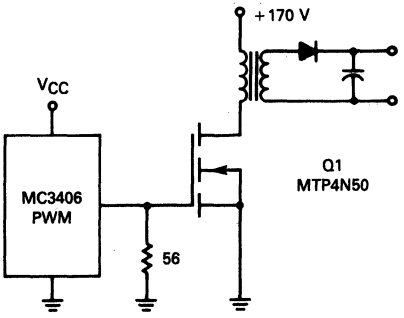


FIGURE 1-12 — TMOS VERSION

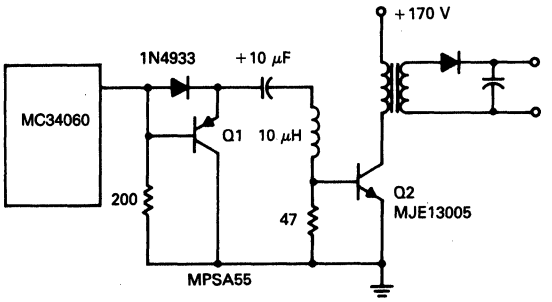


FIGURE 1-13 — BIPOLAR VERSION

FIGURES 1-12 AND 1-13 — COMPARISON OF TMOS versus BIPOLAR IN THE POWER OUTPUT STAGE OF A 20 kHz SWITCHER

lustrates its superior switching speed is shown in the power output section of Figures 1-12 and 1-13. In addition to the drive simplicity and reduced component count, the faster switching speed offers better circuit efficiency. For this 35 W switching regulator, using the same small heatsink for either device, a case temperature rise of only 18°C was measured for the MTP4N50 power MOSFET compared to a 46°C rise for the MJE13005 bipolar transistor. Although the saturation losses were greater for the TMOS, its lower switching losses predominated, resulting in a more efficient switching device. A more detailed description of this Switcher is shown in Chapter 9.

In general, at low switching frequencies, where static losses predominate, bipolars are more efficient. At higher frequencies, above 30 kHz to 100 kHz, the power MOSFETs are more efficient.

Chapter 2: Basic Characteristics of Power MOSFETs

Output Characteristics

Perhaps the most direct way to become familiar with the basic operation of a device is to study its output characteristics. In this case, a comparison of the MOSFET characteristics with those of a bipolar transistor with similar ratings is in order, since the curves of a bipolar device are almost universally familiar to power circuit design engineers.

As indicated in Figures 2-1 and 2-2, the output characteristics of the power MOSFET and the bipolar transistor can be divided similarly into two basic regions. The figures also show the numerous and often confusing terms assigned to those regions. To avoid possible confusion, this section will refer to the MOSFET regions as the "on" (or "ohmic") and "active" regions and bipolar regions as the "saturation" and "active" regions.

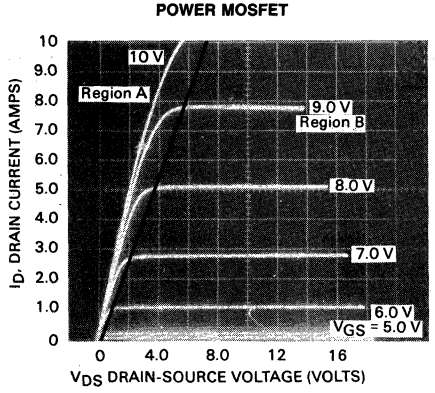


FIGURE 2-1 — I_D-V_{DS} TRANSFER CHARACTERISTICS OF MTP8N15. REGION A IS CALLED THE OHMIC, ON, CONSTANT RESISTANCE OR LINEAR REGION. REGION B IS CALLED THE ACTIVE, CONSTANT CURRENT, OR SATURATION REGION.

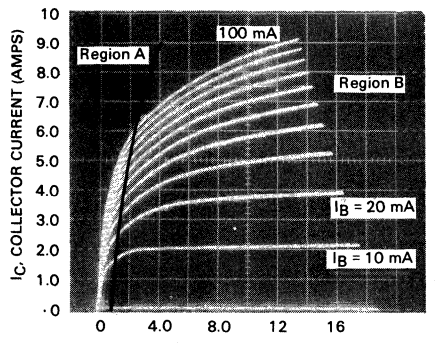


FIGURE 2-2 — I_C-V_{CE} TRANSFER CHARACTERISTICS OF MJE15030 (NPN, I_C CONTINUOUS = 8.0 A, V_{CEO} = 150 V) REGION A IS THE SATURATION REGION. REGION B IS THE LINEAR OR ACTIVE REGION.

One of the three obvious differences between Figures 2-1 and 2-2 is the family of curves for the power MOSFET is generated by changes in gate voltage and not by base current variations. A second difference is the slope of the curve in the bipolar saturation region is steeper than the slope in the ohmic region of the power MOSFET indicating that the on-resistance of the MOSFET is higher than the effective on-resistance of the bipolar.

The third major difference between the output characteristics is that in the active regions the slope of the bipolar curve is steeper than the slope of the TMOS curve, making the MOSFET a better constant current source. The limiting of I_D is due to pinch-off occurring in the MOSFET channel.

Basic MOSFET Parameters

On-Resistance

The on-resistance, or $r_{DS(on)}$, of a power MOSFET is an important figure of merit because it determines the amount of current the device can handle without excessive power dissipation. When switching the MOSFET from off to on, the drain-source resistance falls from a very high value to $r_{DS(on)}$, which is a relatively low value. To minimize $r_{DS(on)}$ the gate voltage should be large enough for a given drain current to maintain operation in the ohmic region. Data sheets usually include a graph, such as Figure 2-3, which relates this information. As Figure 2-4 indicates, increasing the gate voltage above 12 volts has a diminishing effect on lowering on-resistance (especially in high voltage devices) and increases the possibility of spurious gate-source voltage spikes exceeding the maximum gate voltage rating of 20 volts. Somewhat like driving a bipolar transistor deep into saturation, unnecessarily high gate voltages will increase turn-off time because of the excess charge stored in the input capacitance. All Motorola TMOS FETs will conduct the rated continuous drain current with a gate voltage of 10 volts.

As the drain current rises, especially above the continuous rating, the on-resistance also increases. Another important relationship, which is addressed later with the other temperature dependent parameters, is the effect that temperature has on the on-resistance. Increasing T_J and I_D both effect an increase in $r_{DS(on)}$ as shown in Figure 2-5.

Transconductance

Since the transconductance, or g_{fs}, denotes the gain of the MOSFET, much like beta represents the gain of the bipolar transistor, it is an important parameter when the device is operated in the active, or constant current, region. Defined as the ratio of the change in drain current corresponding to a change in gate voltage ($g_{fs} = dI_D/dV_{GS}$), the transconductance varies with operating conditions as seen in Figure 2-6. The value of g_{fs} is determined from the active portion of the V_{DS}-I_D transfer characteristics where a change in V_{DS} no longer significantly influences g_{fs}. Typically the transconductance rating is specified at half the rated continuous drain current and at a V_{DS} of 15 V.

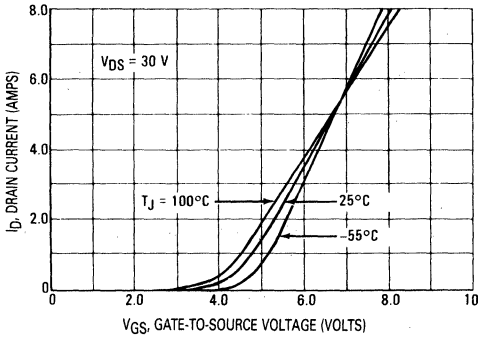


FIGURE 2-3 — TRANSFER CHARACTERISTICS OF MTP4N50

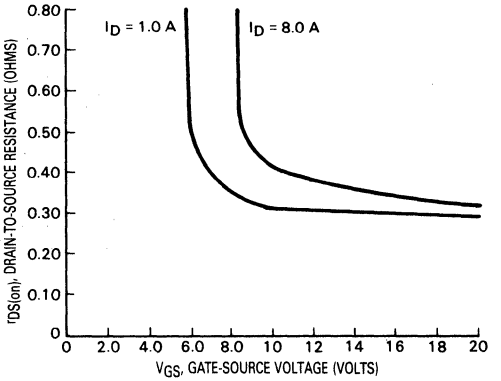


FIGURE 2-4 — VARIATION OF $r_{DS(on)}$ WITH V_{GS} AND I_D FOR MTP8N15 POWER MOSFET

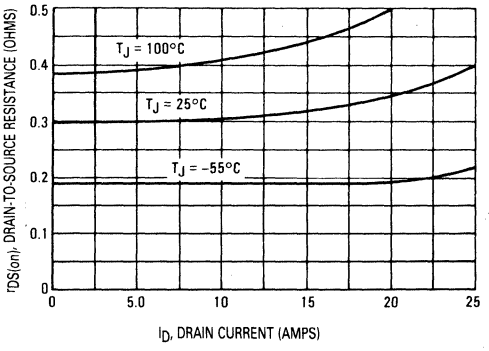


FIGURE 2-5 — VARIATION OF $r_{DS(on)}$ WITH DRAIN CURRENT AND TEMPERATURE FOR MTM15N45

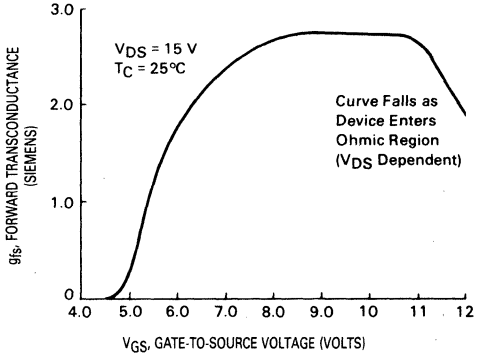


FIGURE 2-6 — SMALL-SIGNAL TRANSCONDUCTANCE versus V_{GS} OF MTP8N10

For designers interested only in switching the power MOSFET between the on and off states, the transconductance is often an unused parameter. Obviously when the device is switched fully on, the transistor will be operating in its ohmic region where the gate voltage will be high. In that region, a change in an already high gate voltage will do little to increase the drain current; therefore, g_{fs} is almost zero.

Threshold Voltage

Threshold Voltage, $V_{GS(th)}$, is the lowest gate voltage at which a specified small amount of drain current begins to flow. Motorola normally specifies $V_{GS(th)}$ at an I_D of one milliampere. Device designers can control the value of the threshold voltage and target $V_{GS(th)}$ to optimize device performance and practicality. A low threshold voltage is desired so the TMOS FET can be controlled by low voltage chips such as CMOS and TTL. A low value also speeds switching because less current needs to be transferred to charge the parasitic input capacitances. But the threshold voltage can be too low if noise can trigger the device or designers have difficulty dealing with currents from previous stages. Also, a positive-going voltage transient on the drain can be coupled to the gate by the gate-to-drain parasitic capacitance and can cause spurious turn-on of a device with a low $V_{GS(th)}$.

Using the TMOS Power MOSFET Designer's Data Sheets

Motorola Designer's Data Sheets are user oriented guides that provide information concerning all the basic TMOS parameters and characteristics needed for successful circuit design. An example of the MTM4N45 data sheet is shown on the following pages. Helpful comments and explanations have been added to clarify some of the parameter definitions and device characteristics.

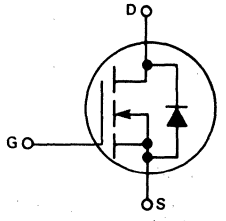
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads

TMOS™



MAXIMUM RATINGS
- Represent the extreme capabilities of the device.
- Not to be used as design condition.

V_{GS}
- All Motorola TMOS power MOSFETs feature a rated $V_{GS(max)}$ of ±20 V.
- Exceeding $V_{gs(max)}$ may result in permanent device degradation.
- Limit gate voltage spikes with a small 20 V zener diode if required.

I_D — MAXIMUM CONTINUOUS DRAIN CURRENT
I_{DM} — MAXIMUM PULSED DRAIN CURRENT MAY BE LIMITED BY
- P_D
- $r_{DS(on)}$
- Wire size and metallization
- Combination of the above

P_D — MAXIMUM POWER AT A CASE TEMPERATURE OF 25°C
- Limit P_D and T_C so that $T_C + P_D \cdot R_{\theta JC} < T_{J(max)}$

$T_{J(max)}$ — MAXIMUM JUNCTION TEMPERATURE
- Reflects a minimum acceptable device service lifetime.
- Presently specified at 150°C for all Motorola power MOSFETs.
- Operating at conditions that guarantee a junction temperature less than $T_{J(max)}$ may enhance long term operating life.

MAXIMUM RATINGS

Rating	Symbol	MTM4N45 MTP4N45	MTM4N50 MTP4N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current				Adc
Continuous	I_D	4.0		
Pulsed	I_{DM}	10		
Total Power Dissipation @ T_C = 25°C	P_D	75		Watts
Derate above 25°C		0.6		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

Designer's Data Sheets

Motorola TMOS Power FETs are characterized on "Designer's Data Sheets." These data sheets permit the design of most circuits entirely with the information provided. Key parameters are specified at elevated temperature to provide practical circuit designs.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM4N45/MTP4N45	$V_{(BR)DSS}$	450	—	Vdc
	MTM4N50/MTP4N50		500	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_C = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc

$V_{(BR)DSS}$ (BV_{DSS})
- Maximum sustaining voltage
- No "negative resistance" region in the I-V characteristic
- Positive temperature coefficient

I_{DSS}
- Specified at 25°C and 100°C
- Gate must be terminated to source

I_{GSS}
- Specified at max. rated V_{GS}

ON CHARACTERISTICS*

Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})	$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C		1.5	4.0	
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$			Vdc
(I_D = 2.0 Adc)		—	3.0	
(I_D = 4.0 Adc)		—	7.5	
(I_D = 2.0 Adc, T_J = 100°C)		—	6.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc)	$r_{DS(on)}$	—	1.5	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 2.0 A)	g_{fs}	1.5	—	mhos

$V_{GS(th)}$
- The gate voltage that must be applied to initiate conduction (Figure 2-7).
- Specified at 25°C and 100°C
- Negative temperature coefficient of about −6.7 mV/°C (Figure 2-8).

$V_{DS(on)}$, $r_{DS(on)}$
- $r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$
- Analogous to the $V_{CE(sat)}$ of a bipolar device
- Specified with a maximum V_{GS} of 10 V for Motorola TMOS power MOSFETs.
- Specified at 25°C and 100°C
- Positive temperature coefficient promotes current sharing when devices are paralleled.

g_{fs}
- The MOSFET "gain" parameter — analogous to h_{FE}
- Equal to the slope of the transfer characteristic (Figure 2-7).

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

- In current saturation region (Figure 2-7).
  $I_d = g_{fs}[V_{GS} - V_{GS(th)}]$
- Relatively constant for $V_{GS(th)} < V_{GS} < V_{DS} + V_{GS(th)}$

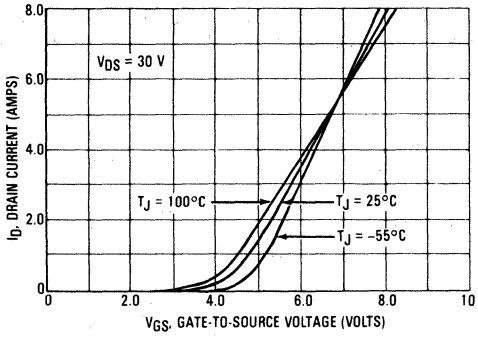


FIGURE 2-7 — TRANSFER CHARACTERISTICS

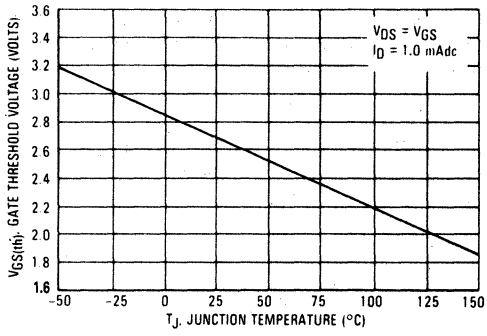


FIGURE 2-8 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

DYNAMIC CHARACTERISTICS

Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1200	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	300	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	80	pF

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the TMOS FET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interelectrode capacitances and those given on data sheets, along with their variations as a function of Drain Voltage, are shown in Figure 2-9.

In driving a MOSFET, the input capacitance, C_{iss} is an important parameter. This capacitance must be charged and discharged by the drive circuit to effect the switching function. The impedance of the drive source strongly affects the switching speed of a MOSFET. The lower the driving source impedance, the faster the switching speeds. Temperature variations have little effect on the device capacitances; therefore, switching times are affected very little by temperature variations.

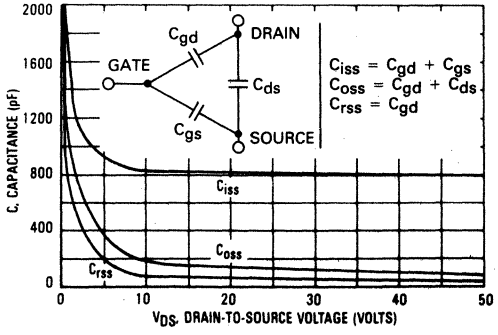


FIGURE 2-9 — TMOS INTERELECTRODE CAPACITANCES

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time (V_{DS} = 25 V, I_D = 2.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time (V_{DS} = 25 V, I_D = 2.0 A, R_{gen} 50 ohms)	t_r	—	100	ns
Turn-Off Delay Time (V_{DS} = 25 V, I_D = 2.0 A, R_{gen} = 50 ohms)	$t_{d(off)}$	—	200	ns
Fall Time (V_{DS} = 25 V, I_D = 2.0 A, R_{gen} = 50 ohms)	t_f	—	100	ns

Switching Characteristics

MOSFET switching speeds are very fast, relative to comparably sized bipolar transistors. Since they are majority carrier devices, there is no storage time associated with the turn-off time; consequently, the switching waveform components are associated with the charging and discharging of the interelectrode capacitances. Driving a MOSFET through a switching cycle involves driving these non-linear capacitances. Switching times, therefore, will strongly depend on the impedances of the driving source and drain load. Maximum limits at elevated temperature are specified.

- During $t_{d(on)}$ — The drive circuit charges C_{iss} to $V_{GS(th)}$. No drain current flows; V_{DS} remains essentially at V_{DD}.
- During t_r — C_{iss} is charged by the drive circuit to $V_{GS(on)}$. C_{oss} discharges from V_{DD} to approach $V_{DS(on)}$ and I_D increases from zero, approaching its maximum. As V_{DS} approaches $V_{DS(on)}$, the rapid rise of C_{oss} at low drain voltages delays the rise of I_D, likewise the increase of C_{iss} inhibits the rise of V_{GS} through the drive impedance.
- During $t_{d(off)}$ — C_{iss} begins to discharge through the gate circuit impedance. The transistor turns off and the drain supply charges C_{oss} through the load. The initial rise of V_{DS} is slowed by the high value of C_{oss} at low drain voltages.
- During t_f — C_{oss} diminishes rapidly as the drain voltage rises. Virtually no additional charge is required to be sourced by the drain supply; V_{DS} rises rapidly to V_{DD} (and beyond if inductance is present in the load).

Resistive Switching

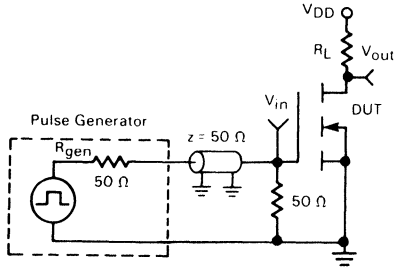


FIGURE 2-10 — SWITCHING TEST CIRCUIT

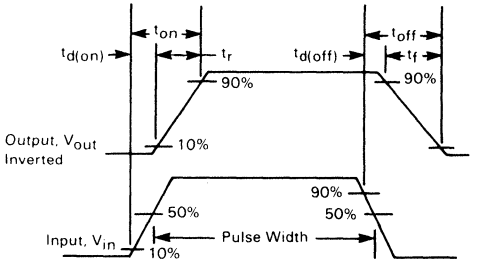


FIGURE 2-11 — SWITCHING WAVEFORMS

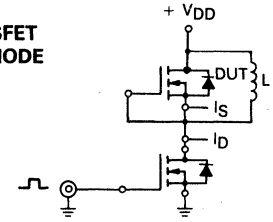
SOURCE-DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 4.0 A	V_{SD}	1.1	Vdc
Forward Turn-On Time	V_{GS} = 0	t_{on}	250	ns
Reverse Recovery Time		t_{rr}	420	ns

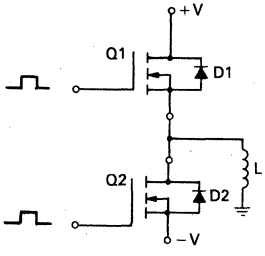
*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

- An integral feature of all power MOSFET structures.
- Reverse recovery times are comparable with those of fast recovery rectifiers.
- Rated current equal to that of the MOSFET
- May be used as a commutator in complementary totem-pole or H-bridge configurations with inductive loads, or in a "Synchronous Rectifier" mode.

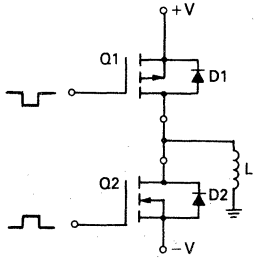
THE POWER MOSFET SOURCE-DRAIN DIODE



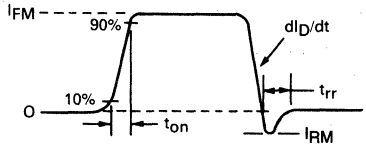
EQUIVALENT TEST CIRCUIT



TOTEM-POLE
N-CHANNEL



COMPLEMENTARY
P-CHANNEL/N-
CHANNEL



DUT WAVEFORM

DURING TURN-OFF OF Q1, D2 PROTECTS Q1; LIKEWISE
DURING TURN-OFF OF Q2, D1 PROTECTS Q2

FIGURE 2-12 — SOURCE-TO-DRAIN DIODE TEST CIRCUIT AND WAVEFORM

SAFE OPERATING AREA INFORMATION

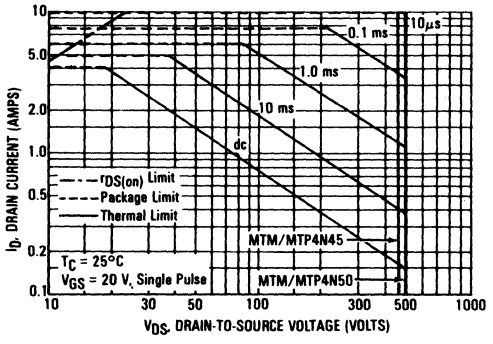


FIGURE 2-13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

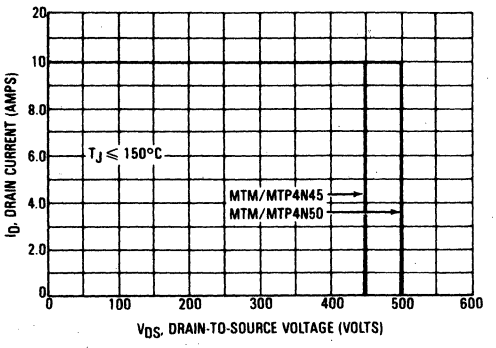


FIGURE 2-14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

THERMAL RESPONSE

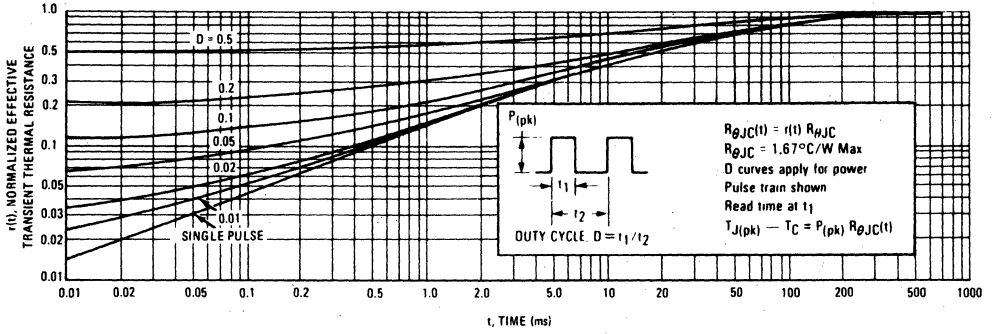


FIGURE 2-15 — MTM4N45/MTM4N50

GUARANTEED SAFE OPERATING AREA

The dc data presented in Figure 2-13 is for a single 1-second pulse, applied while maintaining the case temperature T_C at 25°C. For multiple pulses and case temperatures other than 25°C, the dc drain current at a case temperature of 25°C should be de-rated as follows:

$$I_{D(T)} = I_D\,(25°)\left[\frac{150 - T_C}{P_D \cdot R_{\theta JC} \cdot r_{(t)}}\right]$$

where P_D is the maximum power rating at 25°C, $R_{\theta JC}$ is the junction-to case thermal resistance, and $r_{(t)}$ is the normalized thermal response from Figure 2-15, corresponding to the appropriate pulse width and duty cycle.

EXAMPLE: Determine the maximum allowable drain current for an MTM4N45 at 50 volts drain voltage, with a pulse width of 10 ms and duty cycle of 50%, at a case temperature of 80°C.

From Figure 2-13, the dc drain current at V_{DS} = 50 volts is 1.5 A. For a 10 ms pulse and duty cycle of 50%, Figure 2-15 gives an $r_{(t)}$ of 0.7; then, with P_D = 75 watts at 25°C and $R_{\theta JC}$ = 1.67°C/W

$$I_D = 1.5 \times \frac{150 - 80}{75 \times 1.67 \times 0.7} = 1.5 \times 0.8 = 1.2\ A$$

The switching safe operating area in Figure 2-14 is the boundary that the load line may traverse without incurring damage to the device. The fundamental limits are the maximum rated peak drain current I_{DM}, the minimum drain to source breakdown voltage $V_{BR(DSS)}$ and the maximum rated junction temperature. The boundaries are applicable for both turn-on and turn-off of the devices for rise and fall times of less than one microsecond.

Temperature Dependent Characteristics

$r_{DS(on)}$

Junction temperature variations and their effect on the on-resistance, $r_{DS(on)}$, should be considered when designing with power MOSFETs. Since the on-resistance varies approximately linearly with temperature, power MOSFETs can be assigned temperature coefficients that describe this relationship. For example, the MTM15N45 data sheet includes Figure 2-5 which illustrates the relationship between temperature, $r_{DS(on)}$ and I_D. At I_D = 15 A, the temperature coefficient is:

$$\frac{\Delta r_{DS(on)}}{\Delta T_J} = \frac{0.44 - 0.32\ \Omega}{100 - 25°C} = 0.0016\ \Omega/°C$$

Using 0.0016 Ω/°C, an $r_{DS(on)}$ of 0.48 Ω is easily computed for an I_D of 15 A and a T_J of 125°C. The temperature coefficient will vary between product lines but the on-resistance approximately doubles between T_J of 25°C and 125°C. The fact that static losses in a bipolar transistor do not increase appreciably with increases in temperature leads to lower on-voltages, one of their greatest advantages over MOSFETs.

Switching Speeds are Constant with Temperature

High junction temperatures emphasize one of the most desirable characteristics of the MOSFET, that of low dynamic or switching losses. In the bipolar transistor, temperature increases will increase switching times, causing greater dynamic losses. On the other hand, thermal variations have little effect on the switching speeds of the power MOSFET. These speeds depend on how rapidly the parasitic input capacitances can be charged and discharged. Since the magnitudes of these capacitances are essentially temperature invariant, so are the switching speeds. Therefore, as temperature increases, the dynamic losses in a MOSFET are low and remain constant, while in the bipolar transistors the switching losses are higher and increase with junction temperature.

Threshold Voltage

The gate voltage at which the MOSFET begins to conduct, the gate-threshold voltage, is temperature dependent. The variation with T_J is linear as shown in Figure 2-16. Having a negative temperature coefficient, the threshold voltage falls about 10% for each 45°C rise in the junction temperature.

Importance of $T_{J(max)}$ and Heat Sinking

Two of the packages that commonly house the TMOS die are the TO-220AB and the TO-204 (formerly TO-3). The power ratings of these packages range from 40 to 250 watts depending on the die size and the type of material used as the heat spreader. These ratings are nearly meaningless, however, unless some heat sinking is provided. Without heat sinking the TO-204 and the TO-220 can dissipate only about 4.0 and 2.0 watts respectively, regardless of the die size.

Because long term reliability decreases with increasing junction temperature, T_J should not exceed the maximum rating of 150°C. Steady-state operation above 150°C also invites abrupt and catastrophic failure if the transistor experiences additional transient thermal stresses. Excluding the possibility of thermal transients, operating below the rated junction temperature can enhance reliability. A $T_{J(max)}$ of 150°C is normally chosen as a safe compromise between long term reliability and maximum power dissipation.

In addition to increasing the reliability, proper heat sinking can reduce static losses in the power MOSFET by decreasing the on-resistance. $r_{DS(on)}$, with its positive temperature coefficient, can vary significantly with the quality of the heat sink. Good heat sinking will decrease the junction temperature, which further decreases $r_{DS(on)}$ and the static losses.

Drain-Source Diode

Inherent in most power MOSFETs, and all TMOS transistors, is a "parasitic" drain-source diode. Figure 2-17, the illustration of cross section of the TMOS die, shows the P-N junction formed by the P-well and the N-Epi layer. Because of its extensive junction area, the current ratings of the diode are the same as the MOSFET's continuous and pulsed current ratings. For the N-Channel TMOS FET shown in Figure 2-18, this diode is forward biased when the source is at a positive potential with respect to the

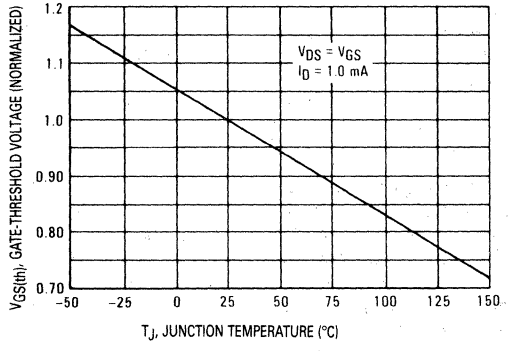


FIGURE 2-16 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

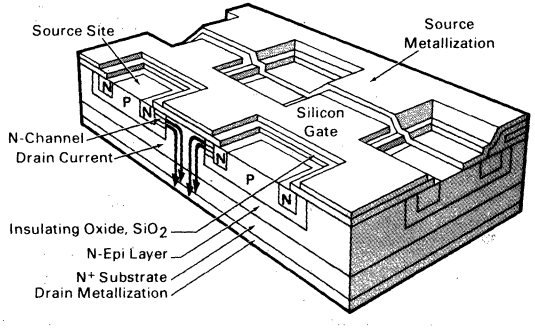


FIGURE 2-17 — CROSS SECTION OF TMOS CELL

drain. Since the diode may be an important circuit element, Motorola Designer's Data Sheets specify typical values of the forward on-voltage, forward turn-on and reverse recovery time. The forward characteristics of the drain-source diodes of several TMOS power MOSFETs are shown in Figure 2-19.

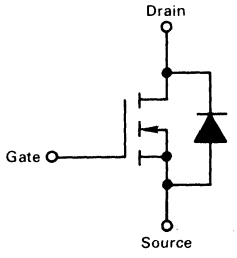


FIGURE 2-18 — COMPLETE N-CHANNEL POWER MOSFET SYMBOL INCLUDING DRAIN-SOURCE DIODE

Most rectifiers, a notable exception being the Schottky diode, exhibit a "reverse recovery" characteristic as depicted in Figure 2-20. When forward current flows in a standard diode, a carrier gradient is formed in the high resistivity side of the junction resulting in an apparent storage of charge. Upon sudden application of a reverse bias, the stored charge temporarily produces a negative current flow during the reverse recovery time, or t_{rr}, until the charge is depleted. The circuit conditions that influence t_{rr} and the stored charge are the forward current magnitude and the rate of change of current from the forward current magnitude to the reverse current peak. When tested under the same circuit conditions, the parasitic drain-source diode of a TMOS transistor has a t_{rr} similar to that of a fast recovery rectifier.

In many applications, the drain-source diode is never forward biased and does not influence circuit operation. However, in multi-transistor configurations, such as the totem pole network of Figure 2-21, the parasitic diodes play an important and useful role. Each transistor is protected from excessive flyback voltages, not by its own drain-source diode, but by the diode of the opposite transistor. As an illustration, assume that Q2 of Figure 2-21 is turned on, Q1 is off and current is flowing up from ground, through the load and into Q2. When Q2 turns off, current is diverted into the drain-source diode of Q1 which clamps the load's inductive kick to V+. By similar reasoning, one can see that D2 protects Q1 during its turn-off.

As a note of caution, it should be realized that the drain-source diode of a power MOSFET, like all diodes except the Schottky, have forward recovery times, meaning they do not instantaneously conduct when forward biased. Therefore, in a totem pole configuration, the TMOS drain-source diode may be too slow to protect the complementary transistor from excessive flyback voltage. Because of this possibility, rapid switching of such configurations may require other clamping schemes.

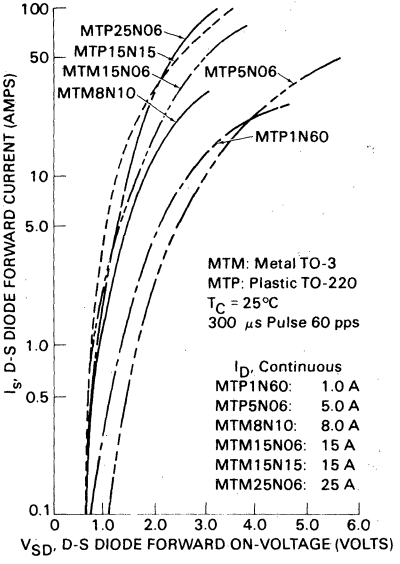


FIGURE 2-19 — FORWARD CHARACTERISTICS OF POWER MOSFETs D-S DIODES

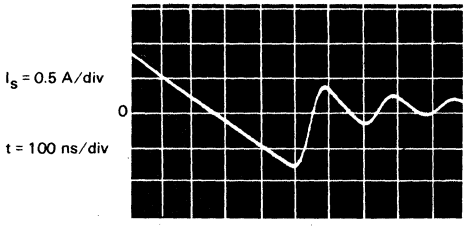


FIGURE 2-20 — REVERSE RECOVERY CHARACTERISTICS OF MTM15N15 DRAIN-SOURCE DIODE

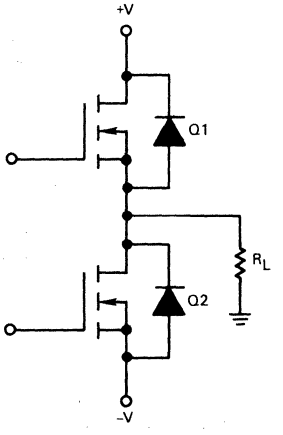


FIGURE 2-21 — TMOS TOTEM POLE NETWORK WITH INTEGRAL DRAIN-SOURCE DIODES

Chapter 3: Electrostatic Discharge and Power MOSFETs

One of the major problems plaguing electronics components today is damage by electrostatic discharge (ESD). ESD can cause degradation or complete component failure. Shown in Table 1 are the susceptibility ranges of various devices to ESD. As circuitry becomes more complex and dense, device geometries shrink, making ESD a major concern of the electronics Industry.

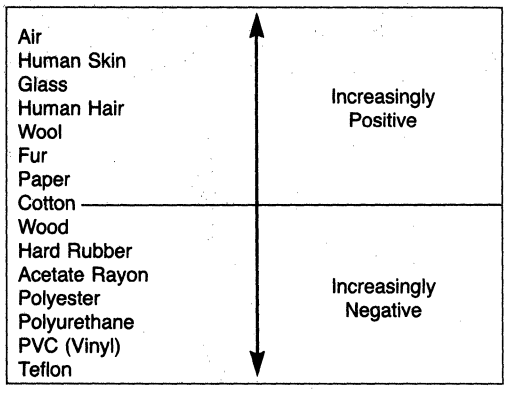
Generation of ESD

Electrostatic potential is a function of the separation of non-conductors on the list of materials known as the Triboelectric Series. (See Table 2.) Additional factors in charge generation are the intimacy of contact, rate of separation and humidity, which makes the material surfaces partially conductive. Whenever two non-conductive materials are flowing or moving with respect to each other, an electrostatic potential is generated.

TABLE 1 — Susceptibility to ESD

Device Type	Range of ESD Susceptibility (Volts)
Power MOSFET	100–200
JFET	140–10,000
CMOS	250–2,000
Schottky Diodes, TTL	300–2,500
Bipolar Transistors	380–7,000
ECL	500
SCR	680–1,000

TABLE 2 — Triboelectric Series



From Table 2, it can be seen that cotton is relatively neutral. The materials that tend to reject moisture are the most significant contributors to ESD. Table 3 gives examples of the potentials that can be generated under various conditions.

TABLE 3 — Typical Electrostatic Voltages

Means of Static Generation	Electrostatic Voltages	
	10 to 20 Percent Relative Humidity	65 to 90 Percent Relative Humidity
Walking across carpet	35,000	1,500
Walking over vinyl floor	12,000	250
Worker at bench	6,000	100
Vinyl envelopes per work instructions	7,000	600
Common poly bag picked up from bench	20,000	1,200
Work chair padded with polyurethane foam	18,000	1,500

From the Tables, it is apparent that sensitive electronic components can be easily damaged or destroyed if precautions are not taken.

ESD and Power MOSFETs

Being MOS devices, TMOS transistors can be damaged by ESD due to improper handling or installation. However, TMOS devices are not as susceptible as CMOS. Due to their large input capacitances, they are able to absorb more energy before being charged to the gate-breakdown voltage. Nevertheless, once breakdown begins, there is enough energy stored in the gate-source capacitance to cause complete perforation of the gate oxide. With a gate-to-source rating of $V_{GS} = \pm 20$ V maximum and electrostatic voltages typically being 100–25,000 volts, it becomes very clear that these devices require special handling procedures. Figure 3-1 shows curve tracer photos of a good device, and the same device degraded by ESD.

Static Protection

The basic method for protecting electronic components combines the prevention of static build up with the removal of existing charges. The mechanism of charge removal from charged objects differs between insulators and conductors. Since charge cannot flow through an insulator, it cannot be removed by contact with a conductor. If the item to be discharged is an insulator (plastic box, person's clothing, etc.), ionized air is required. If the object to be discharged is a conductor (metal tray, conductive bag, person's body, etc.), complete discharge can be accomplished by grounding it.

A complete static-safe work station should include a grounded conductive table top, floor mats, grounded operators (wrist straps), conductive containers, and an ionized air blower to remove static from non-conductors. All soldering irons should be grounded. All non-conductive items such as styrofoam coffee cups, cellophane wrappers, paper, plastic handbags, etc. should be removed from the work area. A periodic survey of the work area

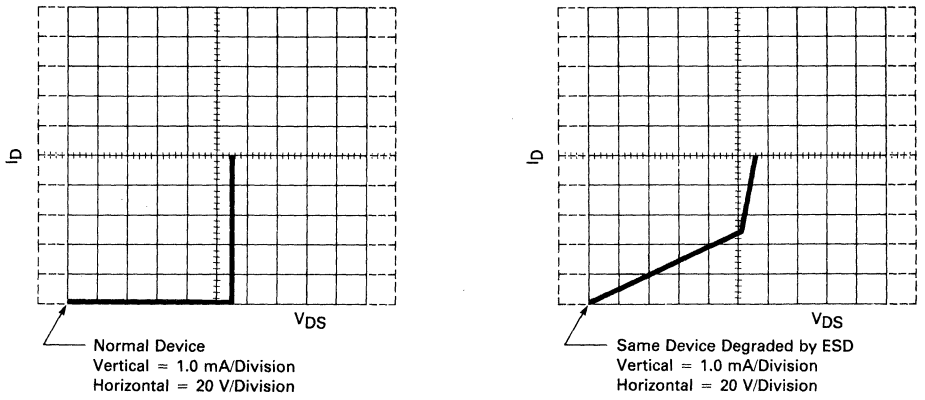
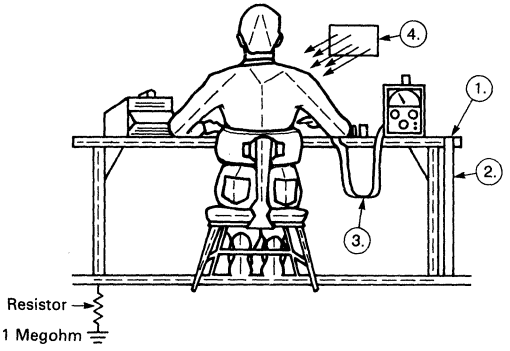


FIGURE 3-1 — CURVE TRACER DRAWINGS OF A GOOD DEVICE AND A DEVICE WITH A DEGRADED GATE. DEVICE IS A 100 VOLT, 12 AMP POWER MOSFET

with a static meter is good practice and any problems detected should be corrected immediately. Above all, education of all personnel in the proper handling of static-sensitive devices is key to preventing ESD failures. Figure 3-2 shows a typical manufacturing work station.



NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area
2. Ground strap
3. Wrist strap in contact with skin
4. Static neutralizer (Ionized air blower directed at work) Primarily for use in areas where direct grounding is impractical

FIGURE 3-2 — TYPICAL MANUFACTURING WORK STATION

By following the above procedures, and using the proper equipment, ESD sensitive devices can be handled without being damaged. The key items to remember are:

1 — Handle all static sensitive components at a static safeguarded work area.

2 — Transport all static sensitive components in static shielding containers or packages.

3 — Education of all personnel in proper handling of static sensitive components.

Test Method:

Military specifications MIL-STD-883B Method 3015.1, DOD-HDBK263, and DOD-STD-1686 classify the sensitivity of semiconductor devices to electrostatic discharge as a function of exposure to the output of a charged network (Table 4). Through measurements and general agreement, the "human-body model" was specified as a network that closely approximated the charge storage capability (100 pF) and the series resistance (1.5 k) of a typical individual (Figure 3-3). Discharge of this network directly into a device indicates that the model assumes a "hard" ground is in contact with the part. Although all pin combinations should be evaluated in both polarities (a total of six combinations for a TMOS Power MOSFET), preliminary tests usually show that gate-oxide breakdown is most likely, and that reverse-biased junctions are about an order of magnitude more sensitive than forward-biased ones. The amount of testing, and components required, can therefore be reduced to sensible levels, yet still yield statistically sound data. The damage mechanism, which can be identified through failure analysis of shorted or degraded samples, is usually oxide puncture or junction meltthrough.

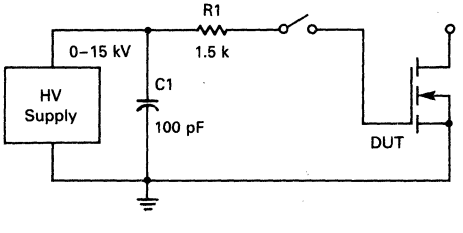


FIGURE 3-3 — THE HUMAN-BODY EQUIVALENT NETWORK

Significance of Sensitivity Data

Assuming that corrective measures cannot be immediately applied in a manufacturing area, or that products manufactured using MOSFET components are likely to

be exposed to ESD events in the field, the sensitivity of the device can be used as a general indicator of the likelihood of failure. Additionally, the extent and cost of protective measures increases as device susceptibility increases.

TABLE 4 — Sensitivity of Semiconductors to ESD from a Charged Network

Device Sensitivity (C_1 Peak Voltage)	MIL-STD-883 Class	DOD-HDBK-263 Class	Typical Preventive Measures(2)
0–1000	A (Sensitive)	Class 1	Careful Case, Keyboard Design, Wrist Straps, Ionized Air, Conductive Flooring, Conductive Clothing, etc. Field-Strength Alarm.
1000–2000	A	Class 2	
2000–4000	B (Nonsensitive)	Class 3	Antistatic Carpet Spray, Wrist Straps, Conductive Packaging Materials.
4000–15,000(1)	B	Class 3	Humidity Adjustment

Notes: 1. Data collected in many applications have shown that under special conditions voltages considerably in excess of 15 kV can be generated with certain materials in the Triboelectric Series.

2. These examples are intended only as very general guidelines. The actual accuracy of a given method is highly variable, as a large number of interdependent factors influence electrostatic field generation. Operator awareness, complemented with a high quality hand-held electrostatic field-strength meter *referenced to ground,* can be very effective in controlling profit losses due to ESD.

A Simple ESD Pulser

A simple electrostatic discharge circuit, which simulates the human body model, is shown in Figure 3-4.

The high voltage supply consists of a 20 mA constant-current luminous-tube transformer and a half-wave voltage doubler circuit. Adjustment of the high voltage is accomplished with a 1.0 Amp Variac. (An oscillator-type supply may also be constructed, using a flyback transformer.) Voltage is monitored by a microammeter, using a 600 megohm current resistor, constructed from 30-1/2 watt, 20 MΩ carbon composition resistors connected in series.

A low voltage supply powers a 555 I.C. timer to provide trigger pulses. This circuit fires a C106 SCR, discharging the 0.033 μF capacitor into an ordinary photoflash trigger coil. This provides a narrow, high-voltage pulse to fire the

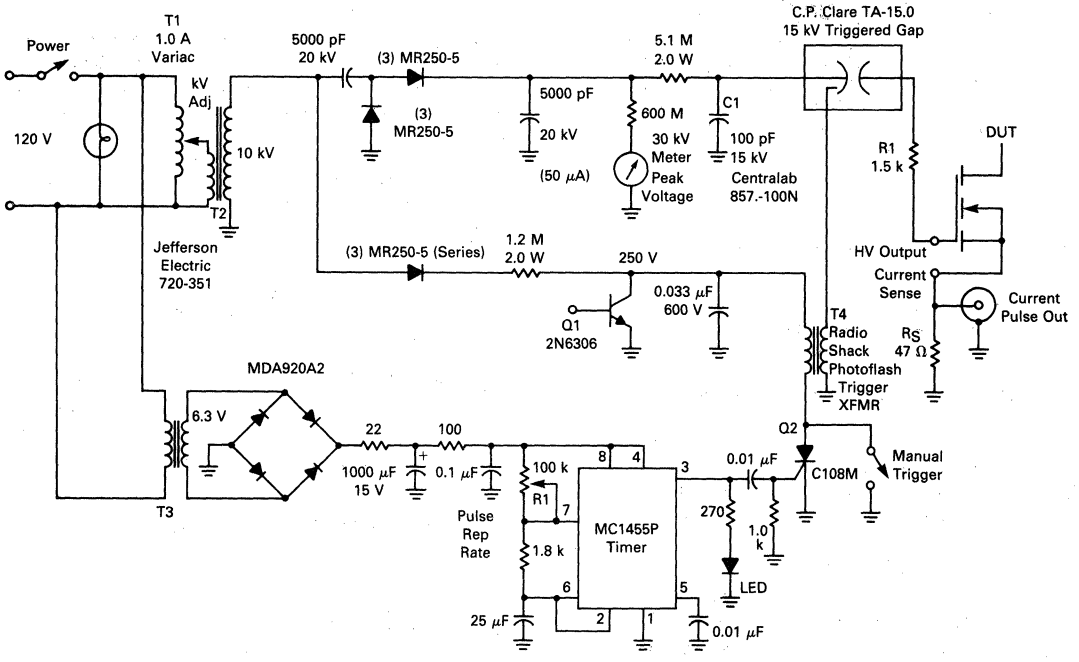


FIGURE 3-4 — ESD (ELECTRO STATIC DISCHARGE) PULSER

triggered gap. The +250 V across the 0.033 μF capacitor is derived by a separate rectifier string, and is regulated by the $V_{(BR)CEO}$ of an NPN power transistor, used as a high-voltage Zener. This voltage quickly saturates as the output control is advanced.

The high voltage supply charges a 100 pF ceramic transmitting-type capacitor, which has extremely low equivalent series inductance. This capacitor, along with the 1.5 kΩ series resistance, forms the standard human-body equivalent circuit specified by MIL-STD-883.

Discharge of the 100 pF capacitor into the DUT is accomplished by means of a triggered spark gap. This device, although somewhat expensive (≈ $100), is nearly an ideal switch, without the voltage limitations, contact bounce, and drive requirements of reed relays. The trigger pulse initiates a plasma discharge between the probe and one electrode. This plasma is swept across the gap by the electric field, initiating arc breakdown.

Warning:

Caution is advised in the construction and operation of this circuit, as the potentials and stored energies in this circuit may be ***lethal.*** Every effort should be made to shield operators from the possibility of contact. Motorola cannot be responsible for claims resulting from the use, or misuse, of this circuit.

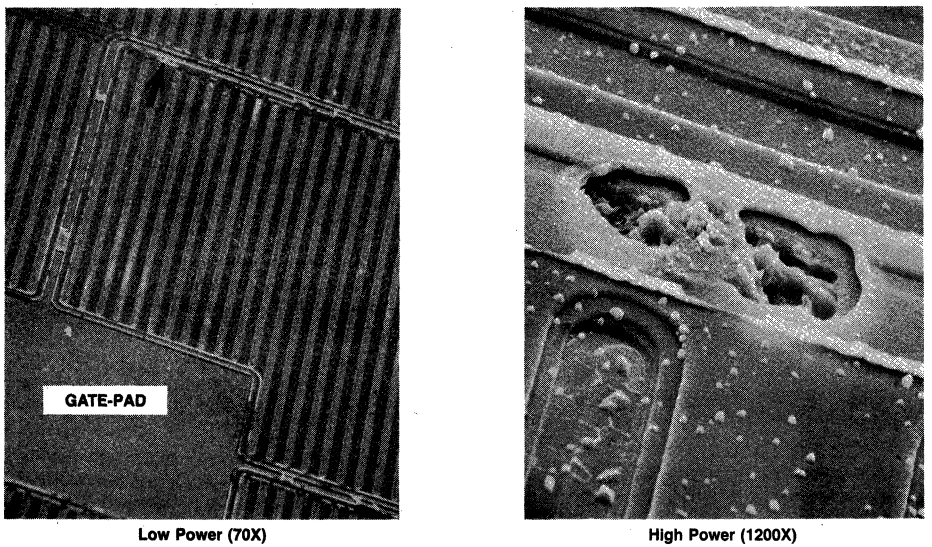
Test Results

Measurement of ESD sensitivity thresholds using the 100 pF–1.5 k circuit has produced the results shown below. An important conclusion from this data is that the ESD sensitivity decreases as the die size (and power-handling capability) increase. Also, these devices fall at or below the 2,000 volt limit defined by Mil-Std-883 as that which classifies a device as static-sensitive. Power MOSFETs, then, should be handled with proper precautions.

TABLE 5 — Test Results

Device	Ratings	Die Size ($Mils^2$)	C_{iss} (pF)	Sensitivity (Volts)
MTP5N05	5.0 A, 50 V, N-CH, Plastic	76^2	150	520
MTM15N05	15 A, 50 V, N-CH, Metal	150^2	700	880
MTM6N60	6.0 A, 600 V, N-CH, Metal	199^2	1400	1350
MTM8N60	8.0 A, 600 V, N-CH, Metal	250^2	2000	1500

The scanning electron microscope (SEM) photos of Figure 3-5 illustrate the typical damage caused to power MOSFETs by electrostatic discharge (ESD). The most prominant mechanism is puncturing of the thin gate oxide, followed by melting of the silicon.



Low Power (70X) High Power (1200X)

FIGURE 3-5 — RESULTS OF ESD TESTING A 6.0 A POWER MOSFET MTM6N60 AT 1000 V.

Chapter 4: Design Considerations in Using Power MOSFETs

Protecting the Power MOSFET

Safe Operating Areas

To provide the designer with Safe Operating Area information for the various modes of operation the TMOS transistor may encounter, two different Safe Operating Areas are defined on the TMOS data sheets: the Forward Biased Safe Operating Area, or FBSOA (often referred to as simply SOA), and the Switching SOA or SSOA. The SSOA curves of MOSFETs describe the voltage and current limitations during turn-on and turn-off and are normally used in the same manner as the RBSOA curves of bipolar transistors.

FBSOA:

An FBSOA curve defines the maximum drain voltage and currents that a device can safely handle when forward biased, or while it is on or being turned on. Of the four limits dictated by the boundaries of the FBSOA curve, the most unforgiving is the maximum drain-source voltage rating which is indicated by boundary A in Figure 4-1. If this rating is exceeded, even momentarily, the device can be damaged permanently. Thus, precautions should be taken if there may be transients in the drain supply voltage.

Maximum allowable drain current is time or pulse-width dependent and defines the second boundary of the FBSOA curve, represented by Line D. The limit is determined by the bonding wire diameter, the size of the source bonding pad, device characteristics and thermal resistance. Even though MOSFETs show rugged overcurrent capabilities, devices should not conduct more than their rated drain current for a given pulse duration. This includes transient currents such as the high in-rush current drawn by a cold incandescent lamp or the reverse recovery current required by a diode.

The third boundary, Line B is fixed by the drain-to-source on-resistance and limits the current at low drain-source voltages. Simply a manifestation of Ohm's Law, the limitation states that with a given on-resistance, current is limited by the applied voltage. The boundary does not describe a linear relationship, however, because the on-resistance increases gradually with increasing current.

The fourth limit, shown as Line C in Figure 4-1, is set by the package thermal limit. This power limited portion of the FBSOA curve is generated from the device thermal response curve, maximum allowable junction temperature and maximum $R_{\theta JC}$ rating. Operation inside this curve insures that the maximum junction temperature does not exceed the 150°C maximum rating.

Since the transient thermal resistance decreases dramatically for shorter pulse durations, the peak power handling capability increases accordingly. For example, Figure 4-2 shows that at 100 μs the normalized single pulse transient resistance of the MTM8N40 is 0.033. Multiplication by $R_{\theta JC}$ (0.033 x 0.83°C/W) results in the effective thermal impedance for a single 100 μs pulse. From the definition of thermal resistance $\left(R_{\theta JC} = \frac{T_J - T_C}{P_D}\right)$ the magnitude of the power pulse that coincides with a

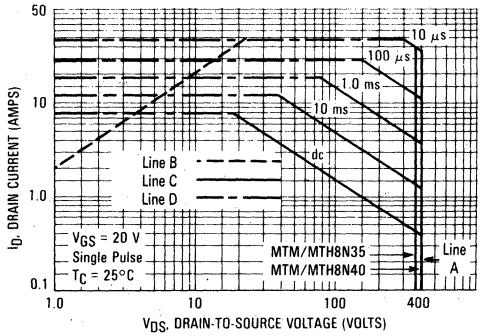


FIGURE 4-1 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA OF THE MTM8N40

T_J of 150°C and a T_C of 25°C is easily determined. In this case, $(0.033 \times 0.83°C/W = \frac{150 - 25°C}{P_D})$, P_D is 4564 W. Therefore, at a V_{DS} of 200 V, the MTM8N40 can conduct about 23 A during a 100 μs pulse without exceeding the $T_{J(max)}$ rating of 150°C.

Normally the portion of the FBSOA curves that is determined by the package thermal limit is only of interest to designers who foresee a condition of simultaneous high voltage and high current for periods greater than 10 μs. This situation can occur in linear applications or in switching applications that experience a fault condition such as a shorted load. For those applications the information contained in Figure 4-1 is incomplete since the data is based on single pulse testing at a case temperature of 25°C. For multiple pulses and case temperatures other than 25°C, the maximum allowable drain current can be computed as shown at the end of the section entitled, "Using the TMOS Designer's Data Sheets."

To a large extent, thermal limitations determine the SOA boundaries for MOSFETs used in linear applications. The maximum allowable junction temperature $T_{J(max)}$ also affects the pulsed current ratings applicable when the MOSFET is used as a switch. With respect to current ratings, MOSFETs are more like rectifiers than bipolar transistors in that their peak current ratings are not gain limited, but thermally limited. Since $r_{DS(on)}$, on-state power dissipation, switching losses, pulse width, duty cycle and junction to ambient thermal impedance all influence T_J, they also affect the maximum allowable pulsed drain current.

In switching applications the total power dissipation is comprised of switching losses and on-state losses. At low frequencies, the MOSFETs switching losses are small enough to ignore. However, as frequency increases the losses eventually become significant and force an increase in T_J. The break point between what is considered low and high frequencies depends on the gate drive impedance. With a low impedance gate-drive switching losses are small, below 40 to 50 kHz.

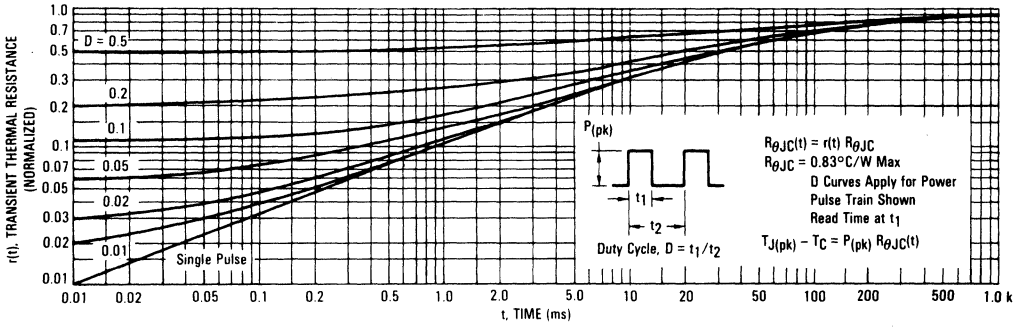


FIGURE 4-2 — THERMAL RESPONSE CURVE OF THE MTM8N40

Since the magnitude of the MOSFET capacitances and, therefore, switching speeds are nearly constant as T_J varies, power MOSFET switching losses are nearly temperature invarient. Without the additional complexity of temperature dependence, losses during the relatively high dissipation turn-on and turn-off intervals are easily modeled and estimated. These techniques are shown in Motorola Application Note AN569.

Because on-state losses are often the bulk of the total power dissipation, they greatly affect the MOSFET's maximum allowable pulsed current capability. The computation of these losses is somewhat involved due to the variation of $r_{DS(on)}$ with temperature and drain current. After computing the heating component of the drain current (RMS value), an iterative technique is used to determine the on-state power dissipation. The following example illustrates how on-state losses and junction temperature can be determined.

Assume the drain current waveform of an MTM8N40 is trapezoidal with the current rising from 8.0 A to 16 A in 25 μs. The duty cycle is 50% and the frequency is 20 kHz. Heat sinking will be provided to keep the case temperature at 80°C. From Figure 4-2, the normalized transient thermal impedance for a 25 μs pulse and 50% duty cycle is 0.5, yielding an effective thermal impedance of 0.415°C/W. [r(t) x $R_{\theta JC}$ = 0.5 x 0.83°C/W].

Before proceeding, the on-resistance and the RMS value of the I_D waveform must be determined. Since $r_{DS(on)}$ is temperature dependent, the junction temperature must be roughly estimated. A T_J of 110°C seems appropriate in this case.

The thermal coefficient of $r_{DS(on)}$, here denoted as C_T, can be obtained from Figure 4-3.

At 12 A,

$$C_T = \frac{\Delta r_{DS(on)}}{\Delta T_J} = \frac{0.97 - 0.58 \text{ ohms}}{100 - 25°C} = 0.0052 \text{ ohms/°C}$$

Assuming T_J = 110°C

$$r_{DS(on)}\Big]_{T_J = 110°C} = r_{DS(on)}\Big]_{T_J = 25°C} + (T_J - 25)\, C_T$$

= 0.58 ohms + (110°C + 25°C) 0.0052 ohms/°C

= 1.02 ohms

This value of $r_{DS(on)}$ is derived from a typical curve and does not represent a worst case value. To obtain a worst case estimate, the ratio between the maximum rated

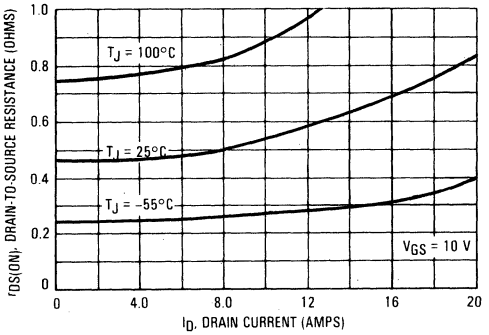


FIGURE 4-3 — ON-RESISTANCE versus DRAIN CURRENT FOR THE MTM8N40

$r_{DS(on)}$ and the typical $r_{DS(on)}$ under the same operating conditions can be used as a multiplier. In this situation, an $r_{DS(on)}$ maximum of 0.8 ohms is specified at an I_D of 4.0 A and a T_C of 25°C. At these same conditions, $r_{DS(on)}$ is typically at 0.48 ohms (Figure 4-3). Assuming the ratio between typical and worst case values remains fairly con-

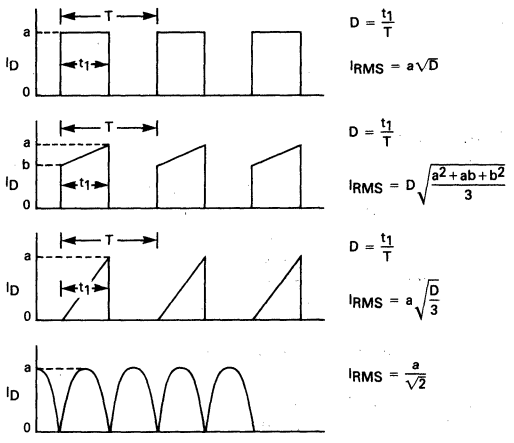


FIGURE 4-4 — RMS VALUES OF SOME COMMON CURRENT WAFEFORMS

stant, the multiplier is $1.67\left(\frac{r_{DS(on)}\ MAX}{r_{DS(on)}\ TYP} = \frac{0.8}{0.48}\right)$.

Therefore, the worst case $r_{DS(on)}$ at 12 A, 110°C is approximately 1.67 x 1.02 ohms, or 1.7 ohms.

From the trapezoid waveform in Figure 4-4:

$$I_{RMS} = D\sqrt{\frac{a^2 + ab + b^2}{3}}$$

$$= 0.5\sqrt{\frac{8^2 + 8 \cdot 16 + 16^2}{3}}$$

$$= 6.11\ A$$

and $P_D = I^2_{RMS}\ r_{DS(on)}$

$$= (6.11)^2\ 1.7$$

$$= 63\ W$$

If switching losses are significant, they should be included at this step. Proceeding with the computation of T_J,

$$T_{JC} = P_D\ R_{\theta JC}$$

$$= (63)\ (0.415) = 26°C$$

$$T_J = T_C + T_{JC}$$

$$= 80 + 26°C = 106°C$$

then the calculated T_J of 106°C replaces the original 110°C estimate and $r_{DS(on)}$, P_D and T_J are recomputed. Since the initial guess was close, 106°C is the final solution and the transistor is operating within its thermal limitations and, therefore, its current handling capabilities.

SSOA:

Switching Safe Operating Area defines the MOSFETs voltage and current limitations durinjg switching transitions. Although an SSOA curve also outlines turn-on boundaries, it is normally used as a turn-off SOA. As such, it is the MOSFET equivalent of the Reverse Biased SOA (RBSOA) of bipolars.

Like RBSOA ratings, turn-off SOA curves are generated by observing device performance as it switches a clamped inductive load. An inductive load is used because it causes the greatest turn-off stress, but it must be clamped so as not to avalanche the transistor with an uncontrolled drain-source "flyback voltage." Switching speeds, which directly determine crossover times and switching losses, also influence the turn-off SOA.

As shown in Figure 4-5, the SSOA curve of the MOSFET is bounded by its maximum pulsed drain current, I_{DM}, and the maximum drain-source voltage, V_{DSS}, as long as switching times are less than 1.0 μs. If MOSFETs are operated within their I_{DM}, V_{DSS} and $T_{J(max)}$ ratings, their SSOA curves guarantee that a secondary breakdown derating is unnecessary.

Drain-Source Overvoltage Protection

The most common cause of failure in a power MOSFET is due to an excursion across an SOA boundary. A good portion of these failures are a result of exceeding the maximum rated drain-source voltage, $V_{(BR)DSS}$. Drain voltage transients caused by switching high currents

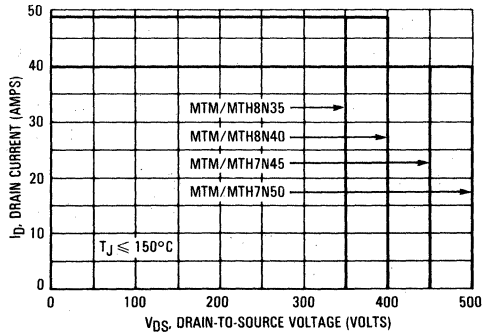


FIGURE 4-5 — MAXIMUM RATED SWITCHING SAFE OPERATING ARE OF THE MTM8N40

through load or stray inductances can force V_{DS} to exceed $V_{(BR)DSS}$ may contain enough energy to destroy the device if it begins to avalanche. Transients on the drain supply voltage can also destroy the power MOSFET.

Fortunately, if there is any danger of these destructive transients, the solutions to the problems are fairly simple. Figure 4-6 illustrates a FET switching an inductive load in a circuit which provides no protection from excessive flyback voltages. The accompanying waveform depicts the turn-off voltage transient due to the load and the parasitic lead and wiring inductance. The MTM20N10 experiences the unrecommended avalance condition for about 300 ns at its breakdown voltage of 122 volts. One of the simplest methods of protecting devices from flyback voltages is to place a clamping diode across the inductive load. Using this method, the diode will clamp most, but not all, of the voltage transient. V_{DS} will still overshoot V_{DD} by the sum of the effects of the forward recovery characteristic of the diode, the diode lead inductance and the parasitic series inductances as shown in Figure 4-7.

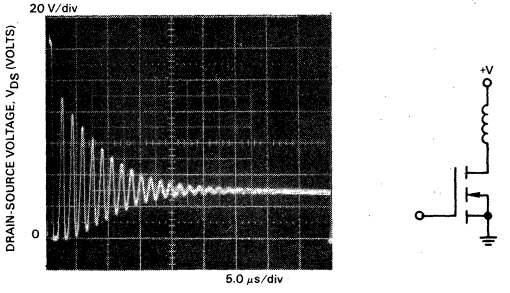


FIGURE 4-6 — V_{DS} TRANSIENT DUE TO UNCLAMPED INDUCTIVE LOAD

If the series resistance of the load is small compared to its inductance, a simple diode clamp may allow current to circulate through the load-diode loop for a significant amount of time after the MOSFET is turned off. When this lingering current is unacceptable, a resistor can be inserted in series with the diode at the expense of increasing the peak flyback voltage seen at the drain.

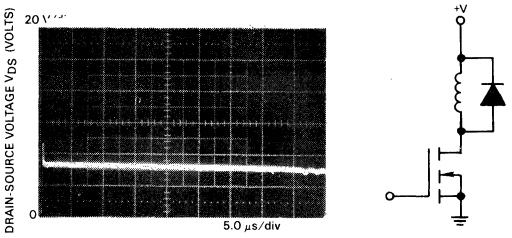


FIGURE 4-7 — V_{DS} TRANSIENT WITH CLAMPING DIODE

Protecting the drain-source from voltage transients with a zener diode, which is a wide band device, is another simple and effective solution. Except for the effects of the lead and wiring inductances and the very short forward recovery time, the zener will clip the voltage transient at its breakdown voltage. A transient with a slow dv_{DS}/dt will be clipped completely while a transient with a rapid dv/dt might momentarily exceed the zener breakdown voltage. These effects are shown in Figure 4-8. Even though it is a very simple remedy, the zener diode is one of the most effective means of transient suppression. Obviously, the power rating of the zener should be scaled so that the clipped energy is safely dissipated.

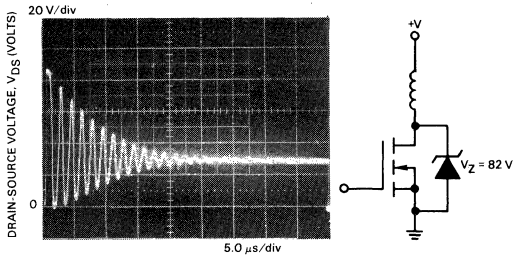


FIGURE 4-8 — V_{DS} TRANSIENT WITH ZENER CLAMP

Figure 4-9 shows an RC clamp network that suppresses flyback voltages greater than the potential across the capacitor. Sized to sustain a nearly constant voltage during the entire switch cycle, the capacitor absorbs energy only during transients and dumps that energy into the resistance during the remaining portion of the cycle. Component values may be computed by considering the power that the RC clamp network must absorb. From the power and the desired clamp voltage, the resistance can be sized. Finally, the magnitude of the capacitance may be determined by relating the RC time constant to the period of the waveform.

As an example, a similar circuit has the following characteristics:

$L = 10\ \mu H$

$i = 3.0$ A (load current just before turn-off

$f = 25$ kHz

$V_C = 60$ V (desired clamp voltage)

The power to be absorbed by the clamp network is:

$$P = 1/2\ Li^2 \times f = 1.125\ W$$

The component values can be determined:

$$\frac{V_C^2}{P} = R = 3.2K \approx 3.3K$$

Let $\tau = RC = 5.0 \div f = 200\ \mu s$

$C = 0.061\ \mu F \approx 0.05\ \mu F$

While this is a common and efficient cricuit, the switching speeds of MOSFETs may produce transients that are too rapid to be attentuated by this method. If the flyback voltage reaches its peak during the first 50 ns, the effectiveness of the circuit will be undermined due to the forward recovery characteristic of the clamp diode and any stray circuit inductance. It may be prudent in these cases to include a zener with a breakdown voltage slightly higher than the clamp voltage. When placed directly across the drain and source terminals, the lead lengths are short enough and the zener is fast enough to catch most transients. Since the zener's only purpose is to clip the initial flyback peak and not to absorb the entire energy stored in the inductor, the zener power rating can be smaller than that needed when one is used as the sole clamping element.

A fourth way to protect power MOSFETs from large drain-source voltage transients is to use an RC snubber network like that of Figure 4-10. Although it effectively reduces the peak drain voltage, the snubber network is not as efficient as a true clamping scheme. Whereas a clamping network only dissipates energy during the transient, the RC snubber also absorbs energy during portions of the switching cycle that are not overstressing the transistor. This configuration also slows turn-on due to the additional drain-source capacitance that must be discharged.

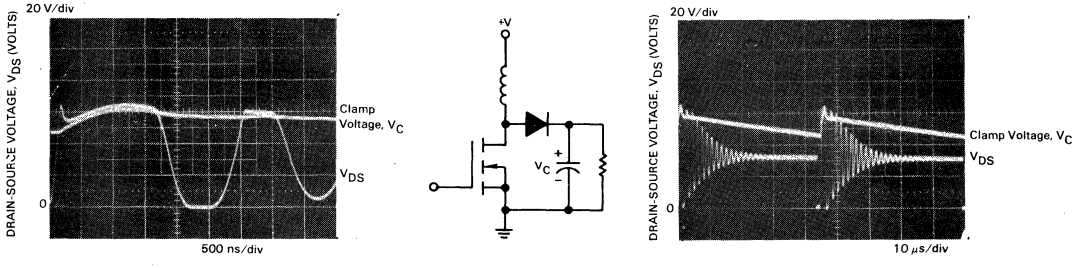


FIGURE 4-9 — V_{DS} TRANSIENT AND RC CLAMP VOLTAGE WITH RC CLAMP NETWORK

No matter which scheme is used, very rapid inductive turn-off can cause transients during the first tens of nanoseconds that may be overlooked unless a wideband oscilloscope (B.W. ≥ 200 MHz) is used to observe the V_{DS} waveform.

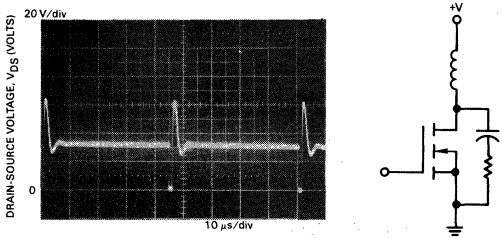


FIGURE 4-10 — V_{DS} TRANSIENT WITH RC SNUBBER

Package and Lead Inductance Considerations

The drain and source parasitic package inductance can influence the magnitude of V_{DS} during rapid switching of very large currents. In Figure 4-11, the drain and source package inductance has been combined and placed in the source because that wirebond and lead length accounts for the bulk of the inductance. The magnitude of L_S in the TO-204, (TO-3) and the TO-220 packages is around 7.0 or 8.0 nH and is large enough to produce appreciable voltage during a very rapid rate of change in drain current. The polarity of the induced voltage is such that the drain-source voltage appearing at the chip is greater than that appearing at the device terminals.

As an example, assume that an MTM35N06 is turned off in 50 ns after conducting 50 A. A di/dt of this magnitude will produce about 8.0 volts across the parasitic package inductance (v = L di/dt = 8.0 nH 50 A/50 ns). If the drain-source voltage at the terminals is 50 V, then V_{DS} at the die is 58 volts.

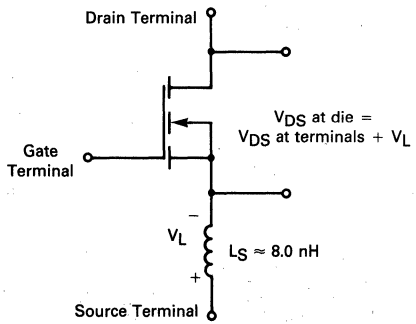


FIGURE 4-11 — VERY RAPID TURN-OFF INCREASES DRAIN-SOURCE VOLTAGE STRESS

Although all power MOSFETs experience some internally generated voltages during rapid switching, peak di/dt's are usually not extreme and the associated voltages are generally small. However, the current ratings of power MOSFETs recently have increased rapidly and, consequently, their maximum di/dt capabilities have also risen. Single die devices are now available with pulsed current ratings greater than 100 A, and the multiple die MTE100N06 has an I_{DM} of 500 A. The very large di/dt capabilities that accompany these current ratings can produce significant V_{DS} stress in addition to that observed at the drain-source terminals.

To assure that the peak V_{DS} at the chip does not exceed the maximum V_{DSS} rating of the device, the following equation can be used:

$$V_{DS(max)} = V_{(BR)DSS} - L(di/dt)$$

where $V_{DS(max)}$ is the maximum allowable voltage appearing across the drain-source terminals, $V_{(BR)DSS}$ is the maximum device rating, L is the parasitic source inductance and di/dt is the rate of change in I_D coincident with $V_{DS(max)}$.

Voltages appearing across the package source inductance also affect the magnitude of the gate-source voltage at the chip and are of such polarity that they slow both the turn-on and turn-off transitions. If large currents are being switched, the parasitic package inductance is large enough to be the factor that limits the MOSFET's switching speeds.

Except for circuits that produce very large di/dt's, the proceeding discussion of package inductance is of academic interest only. However, wiring inductance is often much larger than the package inductance and its effects are proportionately greater. Therefore, the above considerations may become very practical problems in applications in which the di/dt's are not extreme. The quality of the circuit layout dictates the degree of concern.

dv/dt Limitations in Power MOSFETs

Power MOSFET performance is eventually limited by extremely rapid rates of change in drain-source voltage. These very high dv/dt's can disturb proper circuit performance and even cause device failure in certain situations.

High dv/dt's occur during three conditions, each having its own dv/dt threshold before problems arise. The first is what is termed "static dv/dt" and occurs when the device is off. A voltage transient across the drain and source can be coupled to the gate via the gate-to-drain parasitic capacitance, C_{rss}. Depending on the magnitude of the gate-to-source impedance and the displacement current flowing into the gate node (i = C dv/dt), the gate-to-source voltage may rise above $V_{GS(th)}$, causing spurious turn-on.

Obviously, for this case the dv/dt immunity of the device depends to a large extent on the gate-to-source impedance. This underscores the importance of proper gate termination to promote good noise immunity and is one reason why operation of power MOSFETs with the gate open circuited is not recommended.

With its gate shorted to its source, each of Motorola's TMOS devices will withstand dv/dt's of at least 30 V/ns, which is in excess of values commonly seen in practical applications.

If the gate-to-source impedance is high and a voltage transient occurs between drain and source, spurious turn-on is much more likely than device failure. Typically, the

transient will be coupled to the gate and cause the MOSFET to begin its turn-on. But as V_{GS} rises, V_{DS} falls and the dv/dt is reduced. Thus, the phenomena is self-extinguishing and generally is not destructive to any circuit elements.

The second mode in which dv/dt may be of concern occurs when the MOSFET is turned off and an extremely rapidly-rising flyback voltage is generated. Since all loads appear inductive at high switching speeds, the device experiences simultaneous stresses imposed by a high drain current, a high V_{DS} and large displacement currents in the parasitic capacitances. Problems associated with this "dynamic dv/dt" (so named because the device is being switched off and is generating its own dv/dt) are evidenced by device failure.

Unless extraordinary circuit layout techniques are used — e.g., hybridized circuits that eliminate package and lead impedance — maximum attainable dv/dt's in the dynamic mode range from 10 to 45 V/ns, depending on the V_{DSS} rating of the device. Among the various product lines, maximum turn-off speeds do not differ widely and the attainable dv/dt is mainly determined by the magnitude of the voltage that the drain can be switched through. Consequently, a 1000 V MOSFET can generate a greater dynamic dv/dt than a 60 V device, regardless of die size.

All TMOS mask sets are tested and found to be immune to self generated dv/dt's during very rapid, clamped inductive turn-off. The test circuit used has an extremely tight RF layout, and the switching speeds and dv/dt's generated are assumed to be practical limits.

The third condition in which rapidly rising drain-to-source voltage may cause problems is the most stressful and probably most common. It occurs in bridge configurations wherein the drain-source diode is allowed to conduct current. Failures are usually catastrophic and are limited to a specific set of conditions. The circuit in Figure 4-12 will serve as an illustration.

Assume the inductive load is being pulse-width modulated by Q1 and Q2 and that the intrinsic drain-source diodes D1 and D2 provide the current conduction path after the MOSFETs are turned off. When Q1 is turned on, it establishes current I_1. The load current (I_2) is commutated to D2 when Q1 is turned off. If Q1 is rapidly turned on again while D2 is still conducting, dv/dt considerations are in order. Q2 may suffer damage because its diode is conducting while it experiences a rapid rise in V_{DS}.

Studies have shown that failures can occur at dv/dt's in the range of 1.0 V/ns and are common to all MOSFETs tested, regardless of the manufacturer. Since these dv/dt's are not difficult to attain with power MOSFETs, steps must be taken to ensure reliability.

Suggestions for circumventing this problem have already been introduced. One such topology is shown in Figure 4-13. Obviously, the intent of this circuit is to eliminate the problem by not allowing the intrinsic diode to conduct. However, the higher parts count, additional cost and the voltage drop due to the diode in series with the FET are all undesirable. Another solution is to limit the dv/dt with snubbers or by slowing the MOSFET turn-on.

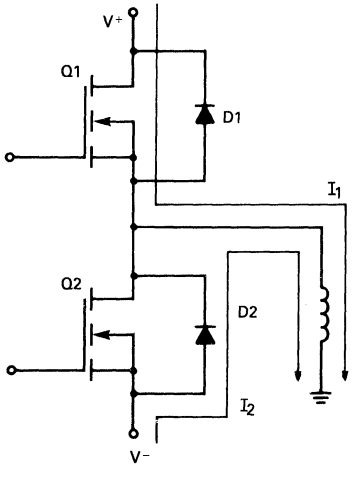


FIGURE 4-12 — TOTEM POLE CIRCUIT IN WHICH DV/DT MAY BE CONCERN

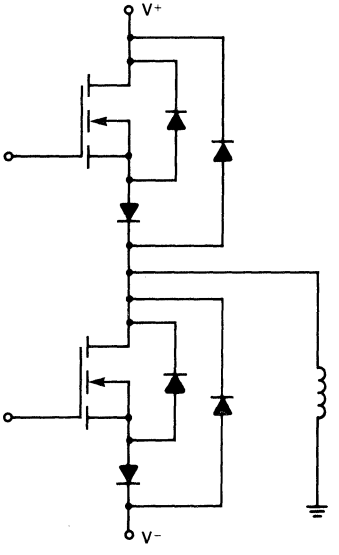


FIGURE 4-13 — CIRCUIT TO ELIMINATE CURRENT CONDUCTION IN THE MOSFET D-S DIODE

Protecting the Gate

The gate of the MOSFET, which is electrically isolated from the rest of the die by a very thin layer of SiO_2, may be damaged if the power MOSFET is handled or installed improperly. Exceeding the 20 V maximum gate-to-source voltage rating, $V_{GS(max)}$, can rupture the gate insulation and destroy the FET. TMOS FETs are not nearly as susceptible as CMOS devices to damage due to static discharge because the input capacitances of power MOSFETs are much larger and absorb more energy before being charged to the gate breakdown voltage. However, once breakdown begins, there is enough energy

stored in the gate-source capacitance to ensure the complete perforation of the gate oxide. To avoid the possibility of device failure caused by static discharge, precautions similar to those taken with small-signal MOSFET and CMOS devices apply to power MOSFETs.

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

The gate of the power MOSFET could still be in danger after the device is placed in the intended circuit. If the gate may see voltage transients which exceed $V_{GS(max)}$, the circuit designer should place a 20 V zener across the gate and source terminals to clamp any potentially destructive spikes. Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

Chapter 5: Gate Drive Requirements

Power MOSFET Gate Drive Requirements

Bipolar power transistors have been around for decades — drive circuits for these devices abound. Power MOSFETs are new arrivals. They differ from their bipolar counterparts especially in their input characteristics. These differences and their implications must be understood in order to insure that the MOSFET is operated in an optimum fashion.

Driving a power MOSFET is tantamount to driving a capacitive reactance network. Depending on the region of operation, the input "sees" either C_{iss}, the Common-Source Input capacitance, or C_{rss}, the Common-Source Reverse Transfer capacitance. C_{iss} is the sum of the gate-to-source capacitance, C_{gs}, and the gate-to-drain capacitance, C_{gd}. C_{gs}, consisting for the most part of the capacitance between the gate structure and source metal, is relatively independent of voltage; C_{rss} (C_{gd}) on the other hand, is mainly the MOS capacitance between gate and drain region and increases sharply (Figure 5-1) for drain voltages less than about 5.0 volts.

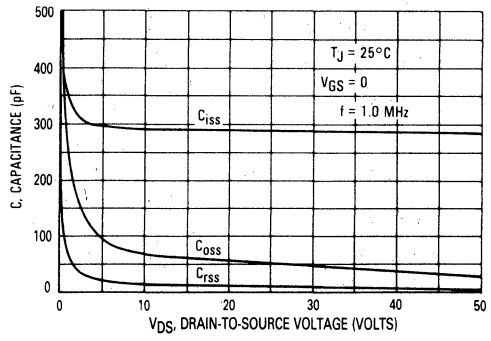


FIGURE 5-1 — CAPACITANCE VARIATION OF MTP3N40

The device capacitances, especially the reverse transfer capacitance, and the gate-drive source impedance largely determine the device switching speed. Since the MOSFET input capacitances vary significantly with the die area, a given gate-drive will switch a smaller device such as the MTP5N06 more rapidly than the larger MTM15N40. However, two considerations complicate the task of estimating switching times. First, since the magnitude of the input capacitance, C_{iss}, varies with V_{DS}, the RC time constant determined by the gate-drive impedance and C_{iss} changes during the switching cycle. Consequently, computation of the rise time of the gate voltage by using a specific gate-drive impedance and input capacitance yields only a rough estimate. The second consideration is the effect of the "Miller" capacitance, C_{rss}, which is referred to as C_{gd} in the following discussion. An example best explains why it influences switching times.

When a high voltage device is "on," V_{DS} is fairly small and V_{GS} is about 15 V. C_{gd} is charged to $V_{GS} - V_{DS(on)}$ (if the gate is considered the positive electrode). When the drain is "off" and is blocking a relatively high drain-to-source voltage, C_{gd} is charged to quite a different potential. In this case the voltage across C_{gd} is a high negative value since the potential from gate-to-source is near or below zero volts and V_{DS} is essentially the drain supply voltage.

During turn-on and turn-off, these large swings in gate-to-drain voltage tax the current sourcing and sinking capabilities of the gate-drive. In addition to charging and discharging C_{gs}, the gate-drive must also supply the displacement current required by C_{gd} ($i_{gate} = C_{gd}\, dV_{DS}/dt$). Unless the gate-drive impedance is fairly low, the V_{GS} waveform commonly plateaus during rapid changes in the drain-source voltage.

By dividing the switching transition into three distinct periods, an accurate estimate of the switching speeds can be obtained. Figure 5-2 illustrates the transfer function of an MTP3N40. To reach a given operating point, the drain current follows this transfer function as V_{GS} increases from zero to $V_{GS(on)}$.

1. In Region I in Figure 5-2 and between times t_0 and t_1 in Figure 5-3, the device is "off" and drain current is essentially zero. Input capacitance is C_{iss}; this capacitance must be charged to $V_{GS(th)}$, the boundary between Region I and II. At time t_1 the device is just beginning to turn on.

2. In Region II, which corresponds to the time between t_1 and t_2, the device is in the transition between "off" and "on." Drain current is controlled by g_{fs}, the device transconductance. Since V_{GS} increases only slightly in Region II, little additional charge enters C_{gs}. Drain voltage, however, falls from V_{DD} to slightly above $V_{DS(on)}$. This, in effect, multiplies C_{gd} by the circuit voltage gain, the familiar Miller Effect. The drive circuitry must supply the displacement current to C_{gd} during the transition through Region II.

3. In Region III and between times t_2 and t_3, the device is "on" and the drain-source impedance is mainly resistive. Drain current depends for the most part on V_{DS} and only to a lesser extent on V_{GS}. Input capacitance is, again, C_{iss} and must be charged to $V_{GS(on)}$.

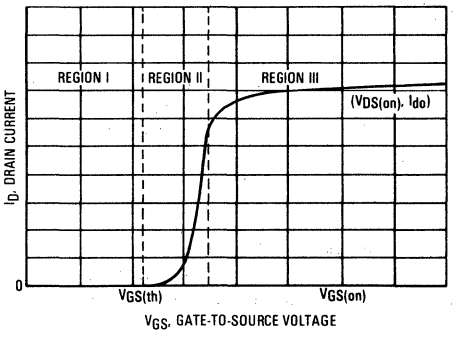


FIGURE 5-2 — TYPICAL POWER MOSFET TRANSFER FUNCTION

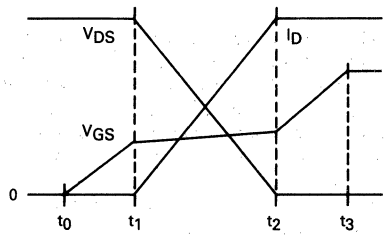


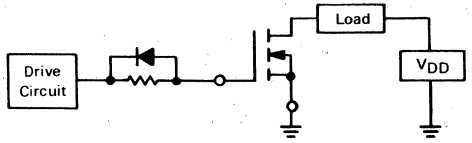
FIGURE 5-3 — IDEALIZED RESISTIVE TURN-ON WAVEFORMS

Drive circuit requirements for the three regions may be summarized as follows:

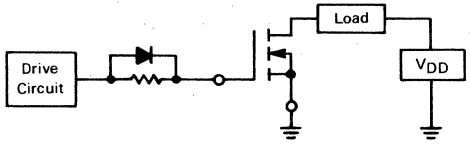
$I_G = C_{iss} \cdot V_{GS(th)}/t_1 - t_0)$ Region I
$I_G = C_{rss} \cdot (V_{DD} - V_{DS(on)})/(t_2 - t_1)$ Region II
$I_G = C_{iss} \cdot (V_{GS(on)} - V_{GS(th)})/(t_3 - t_2)$ Region III

C_{iss} and C_{rss} can be determined from the Designer's Data Sheet typical characteristic curves. For Regions I and II, assume C_{iss} and C_{rss} values at about V_{DS} = 1/2 V_{DD}. For Region III, assume a C_{iss} value corresponding to V_{DS} = $V_{DS(on)}$.

The above relations assume no gate circuit resistance. Adding resistance is an easy way to increase device switching time. If it is desired to increase turn-on time without affecting turn-off time, (for instance, to limit inrush current to a stalled motor) the configuration below may be used:



conversely, to minimize problems associated with very rapid turn-off, such as large flyback voltages, the arrangement below will increase turn-off time without affecting turn-on time:



Just as they govern the turn-on process, the parasitic capacitances and gate-drive impedance also dictate turn-off speeds. At faster switching speeds, turn-off waveforms are particularly interesting because di/dt's are not limited by load or wiring inductance.

The oscillogram of Figure 5-4 shows the turn-off waveforms of an MTP3N40. Between times t_0 and t_1, the gate-drive decreases V_{GS} from 11.5 to about 6.75 V, which is the gate-source potential needed to maintain the 3.0 A load current. Below that voltage the device begins its transition through the active region.

Note that between t_1 and t_2 the progress appears to be stalled. During this time V_{DS} is beginning to rise and the potential across C_{gd} is changing. This is an especially demanding time for the gate-drive since C_{gd} is not only acting as a Miller capacitance, but its magnitude is greatest at low drain-source voltages, as seen in Figure 5-1. As soon as V_{DS} rises above 10 V (where the magnitude of C_{gd} is smaller), the switching process accelerates. Between t_2 and t_3, the drain-source voltage rises rapidly and V_{GS} falls only slightly. Except for abberations caused by circuit parasitics, I_D falls in accordance with the transfer characteristics (Figure 5-5). For example, some of the "drain" current shown in Figure 5-4 is actually flowing into C_{gd}.

The 200 V zener across the drain-source (Figure 4-8) begins to conduct at t_3 and rapidly diverts current from the MTP3N40. Since V_{DS} is no longer changing, the Miller effect is no longer a factor and the gate-drive easily discharges C_{iss} between t_3 and t_4, completing the turn-off.

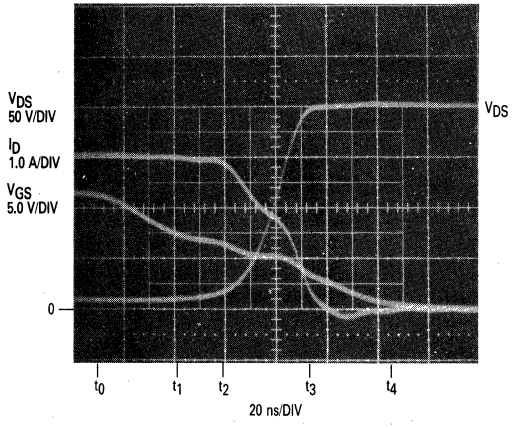


FIGURE 5-4 — CLAMPED INDUCTIVE TURN-OFF WAVEFORMS OF AN MTP3N40

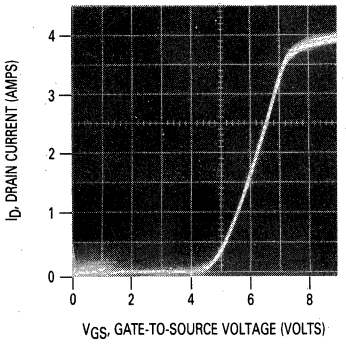


FIGURE 5-5 — TRANSFER CHARACTERISTICS OF AN MTP3N40

COMMON SOURCE SWITCHING

TTL Gate-Drives

Driving a TMOS power transistor directly from a CMOS or open-collector TTL device is possible, but this circuit simplicity is obtained at the cost of slower switching speeds due to the charging current required by the MOSFET's parasitic input capacitance and the limited source and sink capabilities of these drivers.

A TTL device with a totem pole output and no additional circuitry is generally not an acceptable gate-drive network. In this case, the output voltage available is approximately 3.5 volts, which is insufficient to ensure the MOSFET will be driven into the ohmic region. A slightly more promising situation would be to use a pull-up resistor on the TTL output to utilize the entire 5.0 V supply, but even the full 5.0 V on the gate would not guarantee the MOSFET will conduct even half of its rated continuous drain current.

The open-collector TTL device, when used with a pull-up resistor tied to a separate 10 to 15 V supply, can guarantee rapid gate turn-off and ensure sufficient gate voltage to turn the MOSFET fully on (Figure 5-6). Turn-on is not as rapid because the pull-up resistor must be sized to limit power dissipation in the lower TTL output transistor. However, when concerned about dynamic losses incurred while switching an inductive load, the gate fall time is more critical than the rise time due to the phase relationship between the drain current and drain-source voltage. Figure 5-7 shows a configuration providing fast turn-on, yet reducing power dissipation in the TTL device.

When the lower transistor in the TTL output stage is turned on, shunting the MOSFET input capacitance to ground, modeling the bipolar as a saturated device may not be appropriate. The current sinking capabilities of TTL devices in the low output state is limited by the beta of the pull-down transistor and its available base current, which varies with the product line and TTL family. Table 1 shows the current source and sink capabilities of various TTL families.

Although the TTL peak current sinking capability might be twice the continuous rating, faster turn-off can be achieved by using an outboard transistor to clamp the gate-to-ground (Figure 5-8). In this configuration, the bipolars are operating as emitter followers. As such, they

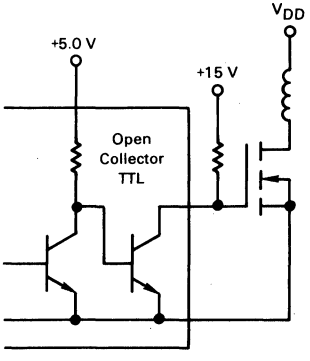


FIGURE 5-6 — DRIVING TMOS WITH OPEN COLLECTOR TTL

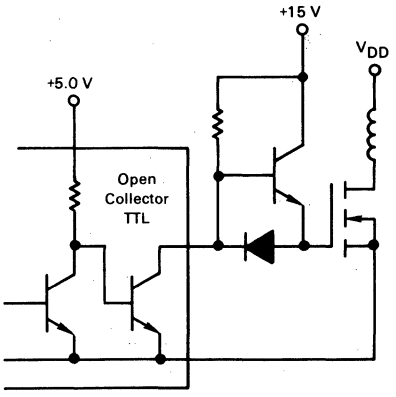


FIGURE 5-7 — OPEN COLLECTOR TTL-TMOS INTERFACE FOR FASTER TURN-ON AND REDUCED POWER DISSIPATION

are never driven into saturation and their associated storage times do not significantly affect the switching frequency limit.

CMOS Gate-Drives

Driving the power MOSFET directly from CMOS presents a different set of advantages and disadvantages. Perhaps most important, CMOS and power MOSFETs can be operated from the same 10 to 15 volt supply. A gate voltage of at least 10 volts will ensure the MOSFET is operating in its ohmic region when conducting its rated

TABLE 1 — TTL Output Current Source and Sink Capabilities

	Output Drive	
Family	**High (Source)**	**Low (Sink)**
74LS00	0.4 mA	8.0 mA
7400	0.8 mA	16 mA
9000	0.8 mA	16 mA
74H00	1.0 mA	20 mA
74S00	1.0 mA	20 mA

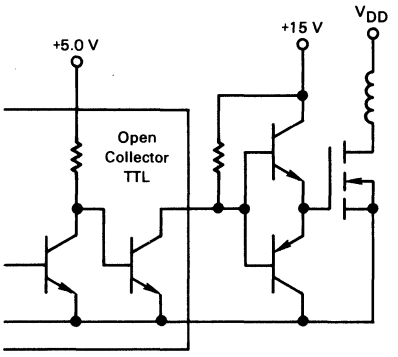


FIGURE 5-8 — OPEN COLLECTOR TTL DRIVING COMPLEMENTARY EMITTER FOLLOWER

continuous current. This benefit allows the designer to directly interface CMOS and TMOS without any additional circuitry including external pull-up resistors. Again, however, circuit simplicity results in slower MOSFET switching due to the limited current source and sink capabilities of CMOS devices. Table 2 compares the output current capabilities of standard CMOS gates to that of the CMOS buffers (MC14049, 14050). Note that while the current sinking capacity of the buffers is improved significantly over that of the standard CMOS gate, the current sourcing capacity is not. The figures in Tables 1 and 2 indicate the current at which the device can still maintain its output voltage within the proper logic level for a given logic state. As an illustration, with a V_{DS} of 15 V, a standard CMOS gate can typically source 8.8 mA in the HIGH state without its output falling below 13.5 volts.

If the switching speeds of CMOS buffers are not rapid enough, the discrete buffers suggested for use with TTL devices (Figures 5-7 and 5-8) can also be used to interface CMOS to TMOS. The only difference is the pull-up resistors are unnecessary for CMOS. Another difference in the two technologies that may affect the maximum switching frequency limit is that the TTL gates typically have faster switching times.

Other Gate-Drives

In certain situations pulse transformers are an effective means of driving the gate of a power MOSFET. They provide the isolation needed to drive bridge configurations or to control an N-Channel MOSFET driving a grounded load. One of the simplest examples of such a circuit is the first circuit in Table 3 where the rise, fall, and delay times for this and the other circuits to be discussed are tabulated.

The diode in Circuit 1 is present simply to limit the flyback voltage appearing across the drive transistor Q1. A transformer turns ratio of one-to-one was chosen to provide an appropriate voltage at the secondary given the 15 volt primary supply voltage. A potential problem with this circuit is that the duty cycle influences the magnitude of V_{GS} because the volt-seconds produced during the on and off intervals at the secondary must sum to zero. Figure 5-9 indicates that increasing the duty cycle decreases the maximum gate-source voltage. As the duty cycle increases above 33%, for the given primary voltage of 15

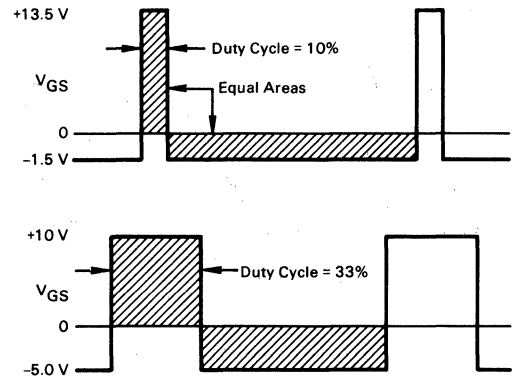


FIGURE 5-9 — VARIATION OF V_{GS} WITH DUTY CYCLE IN PULSE TRANSFORMER GATE-DRIVE

volts, the peak gate voltage falls below 10 volts and may eventually drop to a point where the device is no longer operating in the ohmic region. Increasing the primary voltage to 20 volts would increase the maximum allowable duty cycle.

The basic pulse transformer topology of Circuit 1 also has both maximum and minimum pulse width limitations in addition to those imposed by the volt-seconds requirements. The current in the primary winding may ramp-up to excessive levels due to magnetic saturation, especially in the smaller pulse transformers, if the pulse width is too wide. On the other hand, very short pulse widths may cause two different problems. First, transformer leakage inductance may limit current sourcing capability during a significant portion of the turn-on interval of a very small pulse width. Second, the pulse width must be wide enough to allow the magnetizing current (I_m) to ramp-up significantly, because the stored energy (defined by the current in the magnetizing inductance) provides turn-off drive to the MOSFET gate. To eliminate the problem of I_m varying with pulse width and to improve turn-off drive, the circuit shown in Figure 5-10 may be used.

A modification to the basic transformer gate-drive circuit described above is the addition of a zener diode in series with the clamping diode (Circuit 2). The zener allows ad-

TABLE 2 — CMOS Current Source and Sink Capabilities

			B-Series Gates (MC14001CP)		CMOS Buffers (MC14049, 14050CP)	
		V_{DD}	Min (mA)	Typ (mA)	Min (mA)	Typ (mA)
Current Source Capability	V_{OH} = 2.5 V	5.0 V	-2.1	-4.2	-1.25	-2.5
	V_{OH} = 9.5 V	10 V	-1.1	-2.25	-1.25	-2.5
	V_{OH} = 13.5 V	15 V	-3.0	-8.8	-3.75	-10
Current Sink Capability	V_{OL} = 0.4 V	5.0V	0.44	0.88	3.2	6.0
	V_{OL} = 0.5 V	10 V	1.1	2.25	8.0	16
	V_{OL} = 1.5 V	15 V	3.0	8.8	24	40

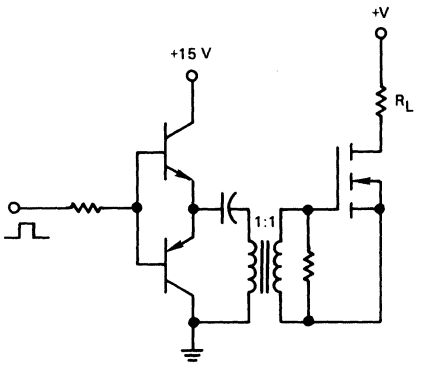


FIGURE 5-10 — CIRCUIT TO ELIMINATE THE VARYING OF I_m WITH PULSE WIDTH

ditional flyback voltage to appear across the primary terminal, when Q1 is turned off. When this additional potential is induced across the secondary, it initially provides greater reset voltage levels and, thus, more rapid gate turn-off. Naturally, inherent in this circuit are the same duty cycle, pulse width and frequency limitations that accompanied Circuit 1.

Circuit 3 is very similar to Circuit 1 except the gate resistances are scaled upward and one is shunted by a diode. The purpose of this configuration is to speed up the MOSFET turn-on while leaving the turn-off slow in comparison. While the MOSFET input capacitance can charge rapidly through the diode, it must discharge through the two relatively high impedance gate resistances. This might be done to minimize inductive flyback voltage or any other undesired phenomena occurring during very rapid turn-off.

A variation of the push-pull converter is used to drive the gate of the MOSFET in Circuit 4. When Q1 is turned on, the 10 volts across the lower of the two primary windings induces the same potential in N_2. The voltage seen at the secondary, due to the 2:1 step-down ratio (N_1 + N_2/N_3), equals the primary supply voltage. At turn-off, the potential across N_2 reverses and is clamped to the 10 V supply by D1. Now N_2 induces its voltage in N_1 and the potential appearing at the secondary reverses in polarity but the magnitude is still 10 volts. If the pulse width is long enough to generate sufficient magnetizing current, this circuit yields good current sinking capabilities.

Two opto-coupled drive circuits are shown in Circuits 5 and 6. Circuit 5 is one of the most straightforward ways of developing a low impedance gate-drive from the output of the optocoupler. This circuit, however, is plagued by long switching delays that limit the useful operating frequency. These delays are inherent in the optocoupler and their magnitudes are affected by the phototransistor's output load impedance. If this impedance is lowered, as accomplished with Circuit 6, the gate-drive turn-off delay is significantly lower. Besides the complexity of these circuits, especially Circuit 6, the gate-drive's bipolar output transistor, Q2, must remain on the entire time that the MOSFET is off. The energy dissipated in these two drivers during low duty cycle operation may be critical if efficiency is a major concern.

Circuits 7 and 8 are similar versions of a circuit that can be used as a high performance gate-drive. The base currents for the bipolar drives must be push-pulled as shown in Figure 5-11. MOSFET turn-on is initiated during a positive transition of the input pulse. Q1 is turned on, supplying the required base current for Q3, which is Baker clamped to minimize its turn-off storage time. Both circuits have excellent turn-on times because of the low impedance path provided between the supply and the gate of the MOSFET.

Turn-off occurs when the falling edge of the input pulse is differentiated by the series combination of R1 and C1, thus turning on Q2. Base current is then free to flow into Q4, clamping the gate-to-ground or a negative potential. The duration of the clamping interval may be adjusted by varying the RC network. Before the occurrence of another input pulse, the MOSFET will remain off due to the 470 Ω gate-source resistance.

Circuits 9 through 12 are examples of how TTL devices may interface with the TMOS power MOSFET. The first of the circuits, number 9, has a very simple interface between the open collector, Low Power Schottky SN74LS05 hex inverter and the MTP12N10. Turn-off speed is fair, considering the circuit simplicity, but turn-on speed is poor because of the large value of R1 needed to protect the inverter from excessive power dissipation when the TTL output is low. Putting three such buffers in parallel, Circuit 10, reduces all the associated switching times by a factor of nearly two-thirds.

Another TTL device with an open collector output is utilized in Circuit 11. Two of the six buffers in the SN7407 operate in parallel with only a pull-up resistor and the gate of the MOSFET connected to the collector of the high voltage (30 volts) output transistors. The associated switching times are quite respectable given the simplicity of the drive circuit.

Another application of the SN7407, as mentioned earlier, is to use it to drive a discrete complementary emitter-follower buffer (Circuit 12). Lowering the pull-up resistor, R1, increases the turn-on speed at the expense of increasing gate turn-off power dissipation.

Figure 5-12 shows an MTM12N10 being driven by a CMOS MC14050CL Hex Buffer. To obtain the maximum output current source and sink capability, all six buffer elements are paralleled.

While the pull-up resistor is not a necessity (as it is with open-collector TTL devices), it does balance the current source and sink capabilities of the CMOS buffer. Without that resistor, one could expect slower turn-on but the drive circuit would be more efficient because the CMOS device no longer must sink the current drawn through R1 when the CMOS outputs are low. Of course, fewer than the six paralleled inverters could be used at the cost of slower switching. Figure 5-13 shows the switching waveforms without a pull-up resistor. For the six buffer elements in parallel the peak I_G during turn-on is about 350 mA and 900 mA during turn-off.

While not as fast as other more elaborate drive circuits, the MC14050CL offers an inexpensive single power sup-

TABLE 3 — Switching Speeds of Various TMOS Gate Drives

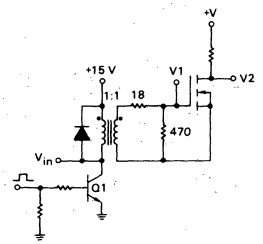
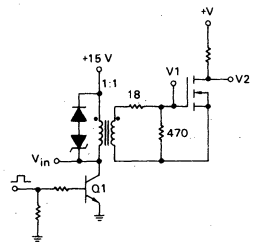
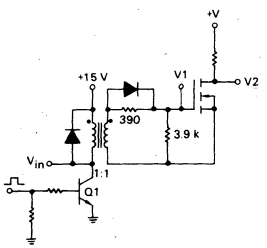
			Gate Switching Times (ns)				Drain Switching Times (ns)			
			Turn-on Delay (V_{in} vs V_1)	Turn-on Rise Time	Turn-off Delay (V_{in} vs V_1)	Turn-off Fall Time	Turn-on Delay (V_{in} vs V_2)	Turn-on Fall Time	Turn-off Delay (V_{in} vs V_2)	Turn-off Rise Time
Circuit 1 Simple Pulse Transformer			15	85	35	230	25	25	185	20
Circuit 2 Pulse Transformer w/Flyback Zener			15	90	25	190	30	25	125	35
Circuit 3 Pulse Transformer w/Speed-up Diode		With Diode D1	30	95	220	1250	60	35	640	230
		Without Diode D1	50	1500	280	1100	220	340	660	230

TABLE 3 — Switching Speeds of Various TMOS Gate Drives (continued)

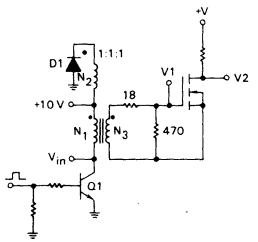
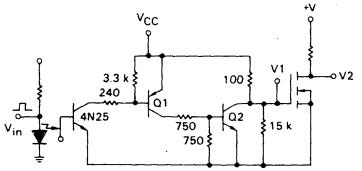
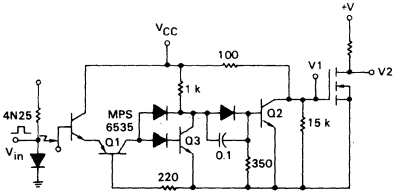
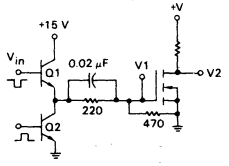
		Gate Switching Times (ns)				Drain Switching Times (ns)			
		Turn-on Delay (V_{in} vs V_1)	Turn-on Rise Time	Turn-off Delay (V_{in} vs V_1)	Turn-off Fall Time	Turn-on Delay (V_{in} vs V_2)	Turn-on Fall Time	Turn-off Delay (V_{in} vs V_2)	Turn-off Rise Time
Circuit 4 Quasi Push-Pull Transformer Drive		15	85	40	230	30	25	160	35
Circuit 5 Standard Opto-Coupling Circuit		3900	460	1600	140	4000	80	1750	20
Circuit 6 High B.W. Opto-Coupling Circuit		3700	420	450	120	3800	75	520	20
Circuit 7 High Performance Push-Pull Circuit		20	60	25	30	30	20	45	15

TABLE 3 — Switching Speeds of Various TMOS Gate Drives (continued)

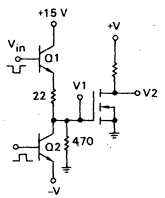
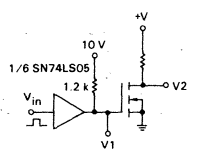
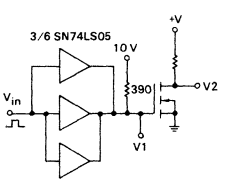
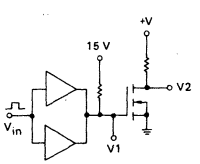
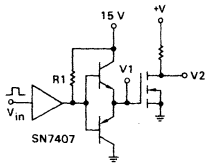
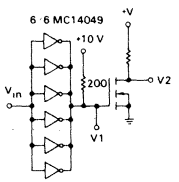
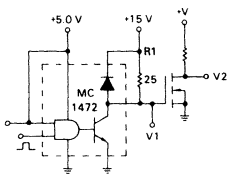
		Gate Switching Times (ns)				Drain Switching Times (ns)			
		Turn-on Delay (V_{in} vs V_1)	Turn-on Rise Time	Turn-off Delay (V_{in} vs V_1)	Turn-off Fall Time	Turn-on Delay (V_{in} vs V_2)	Turn-on Fall Time	Turn-off Delay (V_{in} vs V_2)	Turn-off Rise Time
Circuit 8 High Performance Push-Pull Circuit		20	60	45	70	40	25	85	15
Circuit 9 Low Power Schottky TTL		110	5000	60	600	480	1000	375	150
Circuit 10 Paralleled Low Power Schottky TTL		45	1800	30	210	180	310	140	50
Circuit 11 Paralleled SN7407 Buffers with Pull-Up Resistance		25	710	30	140	60	60	130	30

TABLE 3 — Switching Speeds of Various TMOS Gate Drives (continued)

			Gate Switching Times (ns)				Drain Switching Times (ns)			
			Turn-on Delay (V_{in} vs V_1)	Turn-on Rise Time	Turn-off Delay (V_{in} vs V_1)	Turn-off Fall Time	Turn-on Delay (V_{in} vs V_2)	Turn-on Fall Time	Turn-off Delay (V_{in} vs V_2)	Turn-off Rise Time
Circuit 12 SN7407 Buffer Driving a Complementary Emitter-Follower		R1 = 2.0 k	30	140	20	20	50	20	40	10
		R1 = 5.1 k	60	430	20	20	110	40	40	10
Circuit 13 Six Paralleled CMOS Inverters (MC14049UB)			30	920	20	130	100	160	90	30
Circuit 14 Dual Peripheral Driver (MC1472)			370	100	170	80	280	50	230	15
	*Transformer Specs: Ferroxcube 3019P3CB $N_1 = N_2 = N_3$ = 10 Turns #19 Trifilar Wound $L_P \approx 0.6$ mH									

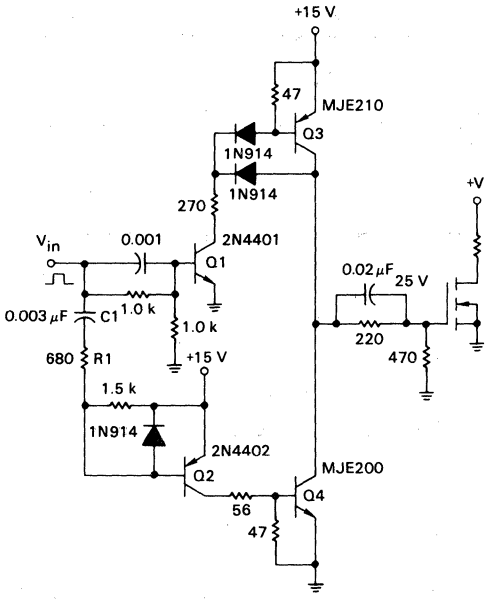


FIGURE 5-11 — PUSH-PULL BASE DRIVE FOR CIRCUITS 7 AND 8

ply device that interfaces directly to CMOS and MHTL circuitry.

Figure 5-14 shows the results of the MTM12N10 being driven by a single MC14050CL buffer element. Note the time scale has been doubled to allow V_{GS} to rise to its upper rail. The gate current scale is a factor of four smaller: peak gate currents of about 70 mA during turn-on and 240 mA during turn-off are seen.

Several ICs that were originally intended for other applications have been adopted by some circuit designers looking for fast, yet simple and efficient MOSFET gate-drive schemes. One such device is the MC1472, a dual peripheral driver, designed to interface MOS logic to high current loads such as relays, lamps and printer hammers. Because each of the two output transistors can sink 300 mA, MOSFET turn-off times are short when this device is used in a gate-drive network. Turn-on times are also short in Circuit 14 because the value of R1 is so low that it only minimally impedes the current during the charging of the MOSFET input capacitances. The advantage of this large current sourcing capability is once again offset by the significant currents that will flow whenever the MC1472 output is low to turn the MOSFET off. In fact, for the 25 ohm pull-up resistor and a V_{CC1} of 15 volts, that current approaches the combined sinking capabilities of the two output transistors in that package.

The MMH0026 Clock Driver has been designed to drive high capacitance loads. It features a peak output current of 1.5 A and transition times of about 30 ns when driving capacitance loads equivalent to the C_{iss} of a power MOSFET. Input drive voltages for the MMH0026 are compatible with Series 54/74 TTL devices, such as the MC7405 Hex Inverter (OC). Detailed information regarding transition times versus load capacitance and power dissipation can be found in the MMH0026 data sheet.

Figure 5-15 identifies the MMH0026 driving an MTM12N10. To illustrate the high peak gate currents that can be sourced by the MMH0026, no resistance was included between driver output and MOSFET gate. It is important to remember that, with gate current transitions occurring in the low nanosecond range, any lead inductance between driver and gate will add (L/R_g) delay to the gate circuit. Keep the distance between driver output and gate terminal as short as possible when fast switching times are important.

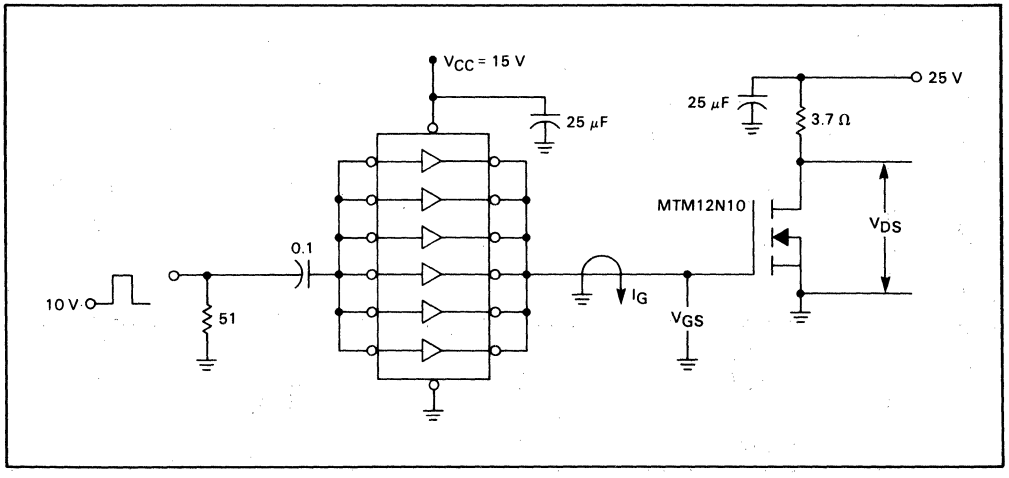


FIGURE 5-12 — MC14050CL HEX BUFFER AS A DRIVER FOR POWER MOSFET

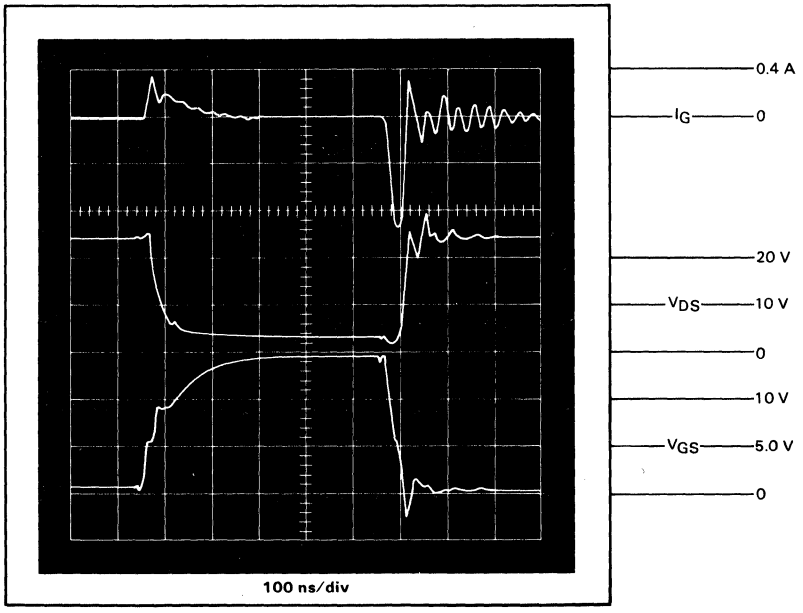


FIGURE 5-13 — POWER MOSFET SWITCHING WAVEFORMS WITH MC14050CL HEX BUFFER (6 BUFFER ELEMENTS IN PARALLEL)

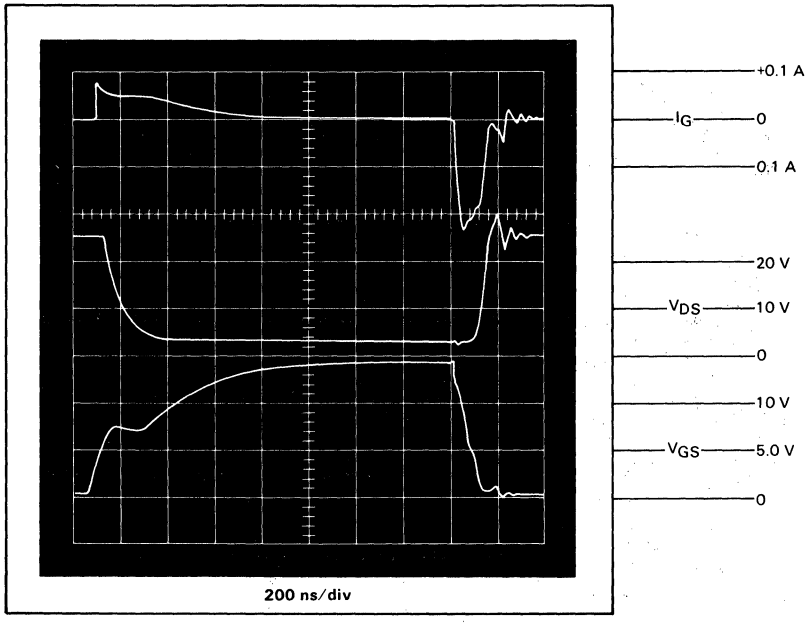


FIGURE 5-14 — POWER MOSFET SWITCHING WAVEFORMS WITH MC14050CL HEX BUFFER (SINGLE BUFFER ELEMENT)

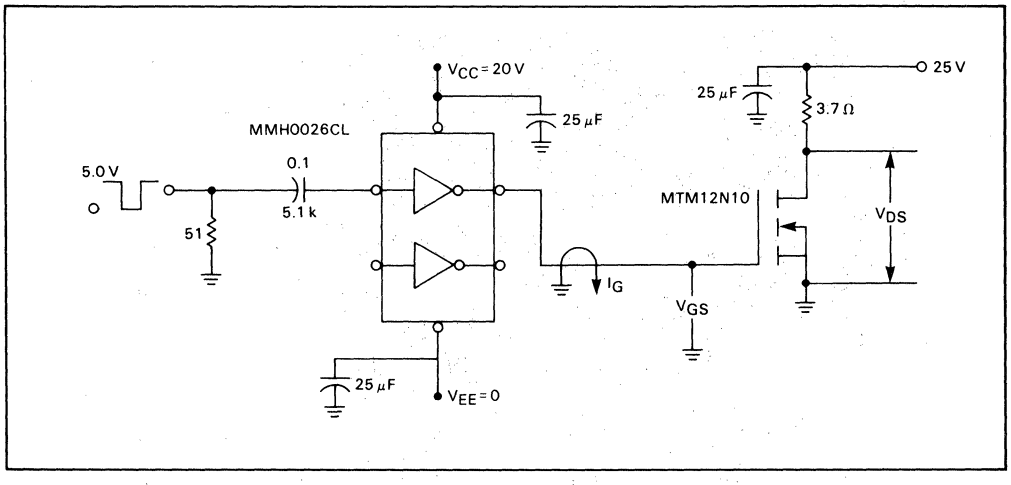


FIGURE 5-15 — MMH0026 CLOCK DRIVER AS A DRIVER FOR POWER MOSFET

Input/output waveforms of the MTM12N10 are shown in Figure 5-16. Although not shown, the maximum drain current was 5.8 A. Figure 5-16 shows that 1.2 A gate current spike that occurs during the turn-on phase, and the 1.5 A negative current pulse occurring during the turn-off phase as C_{gd} is re-charged through the 3.7 ohm load resistor by the 25 V supply. The high voltage pulse that occurs as V_{DS} rises towards 25 V can be attributed to the kick-back of the 3.7 ohm load resistor's parasitic inductance of about 90 nH. This drain voltage spike can be limited by the insertion of an appropriately sized resistor in series with the MMH0026 and the gate of the MTM12N10, to increase the R_gC_{iss} time constant, if the increase in turn-on time is acceptable.

Other examples of ICs that are used to drive the gate of a power MOSFET are the MC1555 timer, the TL494

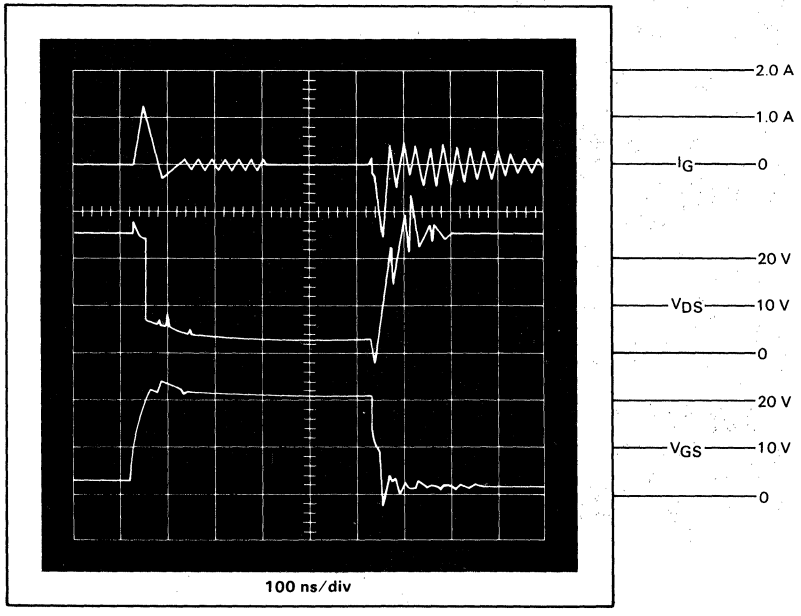


FIGURE 5-16 — POWER MOSFET SWITCHING WAVEFORMS WITH MMH0026 CLOCK DRIVER

pulse width modulation control circuit and the MC75451 peripheral driver. As power MOSFETs gain in popularity, more drivers specifically designed for MOSFETs will appear.

HIGH SIDE SWITCHING

In some situations, connecting the load to the negative bus is either convenient or necessary. In such instances the switching element must be referenced to the positive rail as shown in Figure 5-17. As with PNP and NPN bipolars, both P-channel and N-channel power MOSFETs can perform this switching function. The following discussion of high side switching centers about the P-channel in a common source configuration, and an N-channel source follower as illustrated in Figures 5-17a and 5-17b. All of the concepts presented also apply to the upper switch (or switches) in totem pole or bridge configurations. Figure 5-18 shows that Q1 is essentially operating in a source follower mode when Q2 is turned off and is effectively out of the circuit.

P-Channel Power MOSFETs

To complement some of the N-channel devices, Motorola also produces P-channel power MOSFETs. Because current carriers in the P-channel devices are holes, which have lower mobility than the electron carriers of the N-channel devices, the $r_{DS(on)}$ of P-channel MOSFETs is always greater for a given die size and drain-source breakdown voltage. This impedes the development of truly complementary devices. For instance, if equal on-resistances are desired, the unequal die dimensions will mandate differences in all die area dependent parameters such as capacitances, pulsed current ratings, thermal resistance and safe operating areas.

The application will determine which of the device parameters — whether it be the on-resistance, drain-source breakdown voltage, transconductance, etc. — need be matched closely. Table 4 compares the pertinent electrical parameters of the MTP8P10 with those of N-channel devices that may be considered as device complements. Besides showing the MTP8N10 is not always the best choice for a complement to the MTP8P10, the table also indicates the die area of a P-channel device must be approximately doubled to achieve the on-resistance of an N-channel device with the same $V_{(BR)DSS}$ rating.

P-channel power MOSFETs can simplify certain circuit configurations much in the same way that PNP bipolars can. The circuit simplicity obtained when using P-channel devices to switch a grounded load, for instance, may more than offset the price differential between the N- and P-channel devices.

In Figure 5-19 the source is connected to the positive rail and the drain is attached to the load. As such, the MOSFET is off when $V_{GS} = 0$ V and begins to turn on as V_{GS} (a negative quantity) rises in absolute magnitude above the device threshold voltage. Current would then be free to flow from the source-to-drain and into the load. Still, a logic signal, which is normally referenced to ground, must be used to control the gate. A level shifter, followed by a discrete emitter-follower buffer can supply the proper logic levels while at the same time provide rapid MOSFET switching. The NPN-PNP buffer could be omitted if slower switching is desired.

N-Channel High Side Switching

Instead of using a P-channel as the high side switch, another choice is to use a less expensive N-channel power MOSFET with the load placed in the source circuit — a source follower.

Since there is no voltage gain in a source follower, the gate voltage must equal the output voltage plus the gate-source voltage at that particular load current. Also, for efficient power transfer, the source voltage, when switched on, should approach the positive rail (limited by $r_{DS(on)}$). Thus, the gate voltage should be well above the positive rail, i.e., $V_G = V_{GS(on)} + V_S \approx V_{GS(on)} + V_{DD}$. For hard gate turn-on, V_{GS} should be greater than 10 V. Consequently, the gate voltage for a 12 V system could approach 22 V. This higher than V_{DD} supply gate voltage can be achieved by several techniques:

FIGURE 5-17 — HIGH SIDE SWITCHING

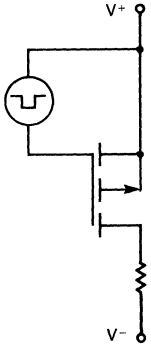


FIGURE 5-17a — P-CHANNEL IN A COMMON SOURCE CONFIGURATION

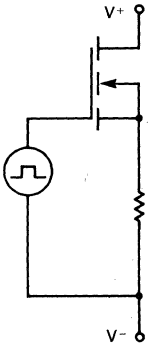


FIGURE 5-17b — N-CHANNEL AS A SOURCE FOLLOWER

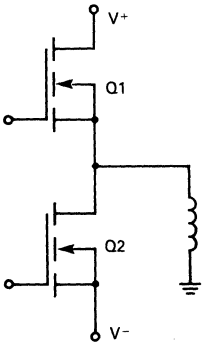


FIGURE 5-18 — TOTEM POLE NETWORK REQUIRES HIGH SIDE SWITCHING

TABLE 4 — Complements of MTP8P10

		P-Channel	N-Channel			Units
		MTP8P10	MTP8N10	MTP10N10	MTP12N10	
Drain-Source Voltage (Max)		100	100	100	100	Vdc
I_D	Continuous	8.0	8.0	10	12	Adc
	Pulsed	25	20	25	30	Adc
Max Power Dissipation		75	75	75	75	Watts
Threshold Voltage		2.0 to 4.5	2.0 to 4.5	2.0 to 4.5	2.0 to 4.5	Vdc
On-Resistance @ $I_D/2$ (Max)		0.4	0.5	0.33	0.18	ohms
Transconductance (Min)		2.0	1.5	2.5	3.0	mhos
Input Capacitance (Max)		1200	400	600	1200	pF
Output Capacitance (Max)		600	350	400	500	pF
Reverse Transfer Capacitance (Max)		180	100	80	250	pF
Fall Time (Max)		150	120	150	150	ns
Rise Time (Max)		150	60	50	100	ns
Normalized Die Area		1.0	0.45	0.66	1.0	—

1. A separate gate supply at least 10 V greater than V_{DD}.
2. Pulse Transformer
3. Optocoupler
4. Bootstrapping
5. Voltage doubler
6. Inductive (flyback)

SEPARATE SUPPLY

The most straightfoward way to accomplish high side switching with an N-channel MOSFET is to drive its gate with a separate supply (Figure 5-20). The auxiliary supply voltage must be from 10 to 20 volts greater than V_{DD} to initiate turn-on. Inherent in the circuit simplicity is the obvious disadvantage of the need of the second supply, especially since its output must be greater than what is commonly the system's high voltage bus. Another consideration is that turn-off switching speeds will be degraded due to the flyback voltage forward biasing the gate-source unless the load inductance is clamped with a freewheeling diode.

PULSE TRANSFORMERS

Pulse transformers are a very popular and practical way of driving an N-channel MOSFET serving as the upper element in a bridge network or as any other high side switch. The beauty of the transformer drive is that the gate-drive signal is easily referenced to the source of the MOSFET, as Figure 5-21 illustrates. Circuits 1 through 4, (page A-38 and A-39) will perform just as well with the load common to the source and the drain tied to the pos-

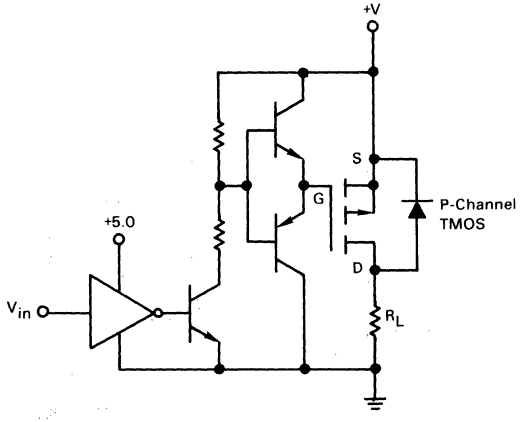


FIGURE 5-19 — LEVEL SHIFTER FOR P-CHANNEL MOSFET DRIVING A GROUNDED LOAD

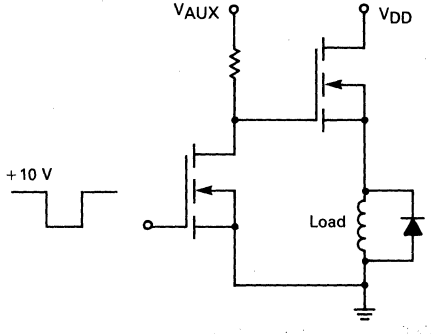


FIGURE 5-20 — HIGH SIDE SWITCHING USING AN AUXILIARY SUPPLY

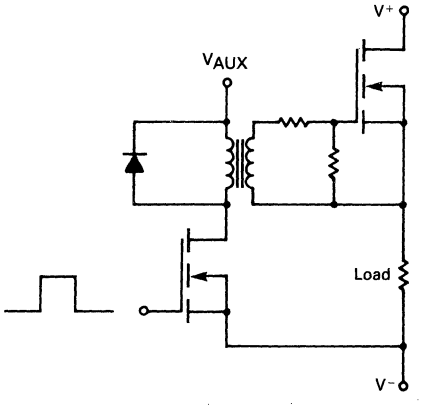


FIGURE 5-21 — PULSE TRANSFORMER DRIVER

itive rail. Other considerations for pulse transformer gate-drive design are also addressed in that section.

OPTOCOUPLERS

A third way to drive a source follower is to reference the gate-drive signal to the source of the MOSFET with the aid of an optocoupler. Figure 5-22 is an example of such a drive network. As long as the V_{CC2} supply and the emitter of the optocoupler remain referenced to the source, the load can be common to either the source or the drain. The additional supply to power the output of the optocoupler must be able to raise the gate voltage above V_{DD}. Either the supply must be isolated from the V_{DD} supply or must be generated from it with a bootstrapping technique.

BOOTSTRAPPING

The simplicity of bootstrapping makes that method the one of choice if its limitations are inconsequential in the specific application or they can somehow be circumvented. The bootstrapping circuit in Figure 5-23 generates the required gate-to-source signal. One of the main problems with this topology is that the load cannot remain in the on state for an unlimited period of time because the

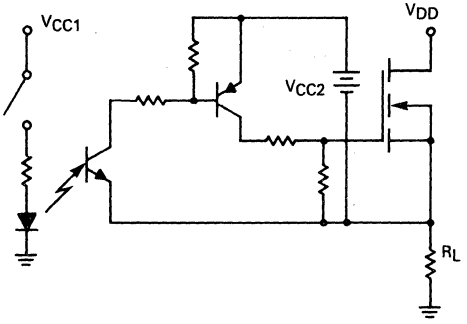


FIGURE 5-22 — DRIVING A SOURCE FOLLOWER WITH AN OPTOCOUPLER

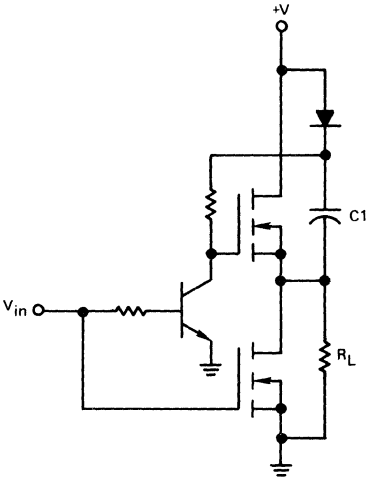


FIGURE 5-23 — BOOTSTRAPPING CIRCUIT TO DRIVE A GROUNDED LOAD WITH N-CHANNEL TMOS

finite charge stored in C1 is eventually bled off. A second problem is that this circuit cannot switch high voltages since C1 will be charged to the system supply voltage and then this potential will be impressed across the gate-to-source. Fortunately, in applications that require grounded loads, such as those in the automotive industry, the supply voltages are often compatible with this method of bootstrapping.

VOLTAGE DOUBLER

The gate voltage can be raised much higher than the source or supply voltage by using a voltage doubler, as shown in Figure 5-24. Voltage multipliers using diodes and capacitors require an oscillator input of which a simple and inexpensive method of obtaining this signal uses a CMOS astable multivibrator, designed with a quad two-input NOR gate MC14001. Gates G1 and G2 form the MV and the parallel connected gates G3 and G4 serve as a low output impedance buffer stage for driving the doubler network. When these gates are powered with the same V_{DD} supply as the power MOSFET high side switch, the output of the doubler (input to the FET gate) will approach twice V_{DD}, due to the voltage doubling effect of diodes D1–D3, capacitors C1, C2 and the input capacitance C_{iss} of the FET switch. Obviously, V_{DD} cannot exceed the maximum voltage of the CMOS (+18 V).

If greater switch output voltage is required with increasing V_{DD}, the CMOS supply can be zenered and more diode-capacitor stages cascaded to raise the gate voltage.

With the component values shown, the astable MV will oscillate at about 350 kHz. This signal and, consequently, the switch can be gated ON and OFF by applying the indicated control voltage to the second input of gates G3 and G4. However, due to the low power output of the CMOS IC, switching speeds are quite slow — tens of milliseconds — limiting this circuit to slow switching applications. Turn-off time can be substantially improved by

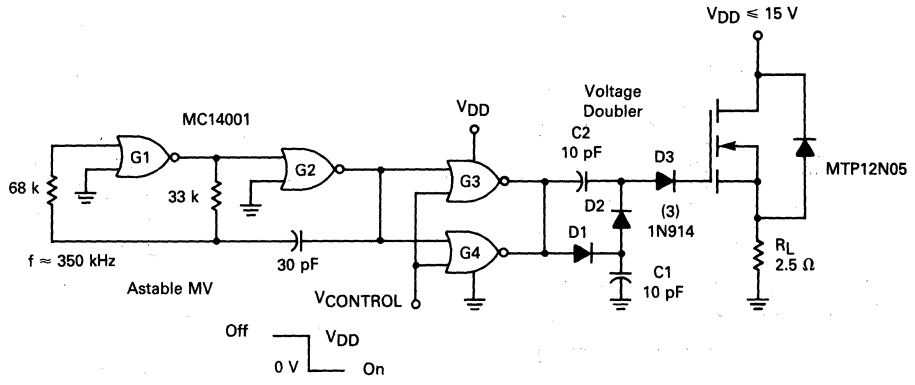


FIGURE 5-24 — N-CHANNEL SOURCE FOLLOWER WITH VOLTAGE DOUBLER DRIVE

employing an input capacitance C_{iss} discharging clamp transistor.

FLYBACK CONVERTER

Another circuit for raising the gate voltage well above the supply voltage, one that uses a flyback converter, is shown in Figure 5-25. The power switch used in this converter, an MTP3N12 power MOSFET (Q1), is easily driven by the CMOS, 100 kHz, astable multivibrator (MV). This circuit uses two of the Hex Inverter MC14572 gates (G1 and G2) as the MV with the remaining four inverters, in parallel, providing the gate-drive to the FET, about 25 mA peak to charge C_{iss}. When Q1 turns on, the drain current ramps-up to about 0.8 A and upon turn-off, the flyback voltage reaches about 60 V. This inductor stored energy is then dumped into the diode-resistor-capacitor load circuit to provide the bias for the power FET switch Q2 (MTP12N05), about 13 V gate-source (28 V gate-ground). The series connected 15 V zener diode blocks the V_{DD} supply from reaching the gate of Q2, when Q1 is off.

With this amount of gate-drive, the V_{DS} of Q2, under a 6.0 A load, measured about 0.5 V, resulting in $r_{DS(on)}$ of 0.08 Ω. This calculates to about a 97% voltage transfer (94% power transfer).

As in the previous source follower gate-drive circuit, the power switch is enabled by a zero logic level to one input of NOR Gate G1. For this circuit, however, turn-off switching speeds are much faster — about 0.15 ms — due to the relatively higher power output of the converter gate-drive.

This type of gate-drive can also be used in totem-pole (half or full-bridge) configurations, where the upper switch is also essentially a source follower. For details, see the Motor Controller Section.

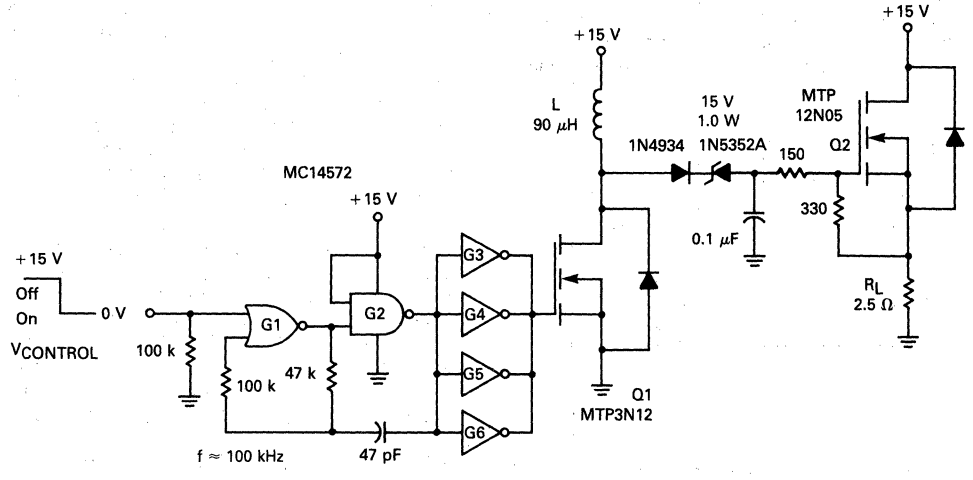


FIGURE 5-25 — N-CHANNEL SOURCE FOLLOWER WITH FLYBACK CONVERTER DRIVE

Chapter 6: Paralleling Power MOSFETs

In some applications, the most beneficial characteristic of the power MOSFET is its ability to be paralleled to increase current conduction and power switching capabilities. Current sharing among devices is important in all of the modes in which the MOSFET may conduct current. These modes are:

1 — Fully "on" during static conditions.

2 — Switching applications including transient (turn-on and turn-off) and pulsed conditions.

3 — Linear applications.

4 — Applications in which the drain-source diode will conduct current.

Since the considerations for each case are quite different, each must be investigated independently before the MOSFET can be regarded as a device that is easily paralleled. The following sections show that the MOSFET can be paralleled in each of the four modes provided certain simple recommendations are followed.

Static Current Sharing Design Considerations

Although increasing junction temperature raises the on-resistance and the conduction losses of the power MOSFET, definite benefits are attributable to the positive temperature coefficient of $r_{DS(on)}$. If a portion of the chip begins to hog current, the localized temperature will increase, causing a corresponding increase in the $r_{DS(on)}$ of that portion of the chip, and current will shift away to the cooler, less active, portions of the die. This trait accounts for the tendency of the device to share current over the entire surface of the die's active region. Because current crowding and hotspotting are eliminated under normal operating conditions, there is no need to derate power MOSFETs to guard against secondary breakdown.

The argument supporting current sharing within a device, due to the positive temperature coefficient of $r_{DS(on)}$, is easily extended to the case of paralleled devices. As within a single device with some imbalance in $r_{DS(on)}$ over the die's active area, an imbalance or mismatch of $r_{DS(on)}$ between devices will cause an initial current loading imbalance between devices. The resulting rise in junction temperature and on-resistance of the device with the lowest $r_{DS(on)}$ will decrease that device's drain current and will establish a more equal distribution of the total load current in all paralleled devices.

While this tendency is definitely observable, its influence on the degree of current sharing is often overestimated. In the power MOSFET, the current sharing mechanism is not triggered simply by high junction temperature, but by the difference in T_J between the low and high $r_{DS(on)}$ devices. Due to the generally small thermal coefficient of $r_{DS(on)}$, this difference in junction temperature sometimes must be substantial to attain a high degree of current sharing.

Since the ultimate concern is for optimum reliability, the emphasis should not be placed on obtaining large deltas in T_J to force a greater degree of current sharing. On the contrary, the effort should be focused on decreasing T_J of the hottest device. This is accomplished by close thermal coupling of the paralleled devices, provided that the total heat sinking capability is not compromised by doing so. This will tend to minimize the differences in both case and junction temperature. Before a worst case example of these concepts can be examined, some knowledge of the range of the variation of $r_{DS(on)}$ within production devices must be obtained.

Unless devices are matched for identical on-resistances, there will be at least a slight mismatch in their individual drain currents. The worst case situation is obviously the paralleling of devices with the widest possible variation in $r_{DS(on)}$. Two wafer lots of the MTP8N18 were sampled to obtain some idea of the range of variation of $r_{DS(on)}$ within the same wafer lot and between wafer lots. In addition to information on $r_{DS(on)}$, Table 1 contains data on the parameters important to dynamic current sharing which will be addressed later. From this information, one will have to design for a worst case $r_{DS(on)}$ mismatch of 30%.

TABLE 1 — Variation of $r_{DS(on)}$, g_{fs}, and $V_{GS(th)}$ in Two Wafer Lots of the MTP8N18

	$r_{DS(on)}$		g_{fs}		$V_{GS(TH)}$		Sample Size
	Min.	Max.	Min.	Max.	Min.	Max.	
Wafer Lot I	0.231	0.297	3.704	4.878	2.300	4.080	100
Wafer Lot I	0.239	0.305	3.571	4.878	3.685	3.910	50

* Maximum Rated $r_{DS(on)}$ is 0.4 ohms.

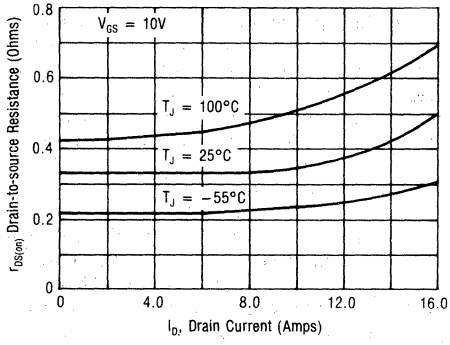
$r_{DS(on)}$ is influenced by the magnitude of the drain current and the junction temperature. I_D and T_J are, in turn, a function of the power dissipation, which is strongly dependent upon $r_{DS(on)}$. The quality of heat sinking and thermal coupling between devices also affects I_D and T_J. These interdependent relationships make an analytical attempt to determine the degree of current sharing between several devices with a given $r_{DS(on)}$ mismatch rather complicated. An example of an iterative analytical process used to accomplish this end follows. The estimated I_D mismatch is somewhat dependent on the initial assumptions.

Design requirements could include the following:

1. Maximum desired junction temperature is 125°C.
2. Sufficient heat sinking will be supplied to maintain a 90°C case temperature when T_A = 35°C during maximum power dissipation.
3. Assume worst case $r_{DS(on)}$ mismatch for the MTP8N18 is 0.230 to 0.400 ohms @ I_D = 4.0 A and T_J = 25°C.

From these conditions, the worst case variation in I_D, P_D and T_J needs to be determined. First, the thermal coefficient of $r_{DS(on)}$, C_T, must be determined from the on-resistance versus drain current curve (Figure 6-1).

In addition to assuming that C_T is invariant with temperature and drain current, it is also supposed that thermal coupling between device heat sinks is negligible. From the maximum desired junction temperature (T_J = 125°C), case temperature (T_C = 90°C), and the junction to case



$$C_T\Big|_{I_D = 8.0\ A} = \frac{\Delta r_{DS(on)}}{\Delta T} = \frac{r_{DS(on)}\Big|_{T_J = 100°C} - r_{DS(on)}\Big|_{T_J = 25°C}}{100°C\text{-}25°C}$$

$$= \frac{0.47 - 0.32\ \Omega}{75°C} = 0.002\ \Omega/°C$$

FIGURE 6-1 — ON-RESISTANCE versus DRAIN CURRENT — MTP8N18

thermal resistance ($R_{\theta JC}$ = 1.67°C/W) of the MTP8N18, the maximum power dissipation and case to ambient thermal resistance are easily calculated.

$$P_D = \frac{T_J - T_C}{R_{\theta JC}} = \frac{125\text{-}90°C}{1.67°C/W} = 20.96\ W$$

$$R_{\theta CA}\ \frac{T_C - T_A}{P_D} = \frac{90\text{-}35°C}{20.96\ W} = 2.62°C/W$$

Attention is then focused on the device with the lowest $r_{DS(on)}$ since it will be dissipating the most power. At a T_J of 125°C its $r_{DS(on)}$, drain current, and V_{DS} are:

$$r_{DS(on)}\Big|_{T_J = 125°C} = r_{DS(on)}\Big|_{T_J = 25°C} + (T_J - 25°C)\ C_T$$

$$= 0.230 + (125\text{-}25)\ .002$$

$$= 0.430\ \Omega$$

$$I_D = \sqrt{\frac{P_D}{r_{DS(on)}}} = \sqrt{\frac{20.96}{0.430}} = 6.98 \approx 7.0\ Amp$$

$$V_{DS} = I_D * r_{DS(on)} = (7) * (0.430) = 3.0\ Volts$$

To determine the operating conditions of a high resistance device operated in parallel with a low resistance device, an iterative technique must be employed. The approach is to estimate the junction temperature of the cooler device and from that, compute the $r_{DS(on)}$ at that T_J, the current and power dissipated, and the new junction temperature. The computations are then repeated until the process converges on the correct solution.

The first iteration proceeds as follows:

For T_J = 100°C:

$$r_{DS(on)}\Big|_{T_J = 100°C} = r_{DS(on)}\Big|_{T_J = 25°C} + (T_J - 25°C)\ C_T$$

$$= 0.400 + (100\text{-}25)\ 0.002 = 0.550\ \Omega$$

$$P_D = \frac{V^2}{r_{DS(on)}} = \frac{3^2}{0.550} = 16.36\ W$$

$$\Delta T_{JC} = P_D * R_{\theta JC} = 16.36 * 1.67 = 27.33°C$$

$$\Delta T_{CA} = P_D * R_{\theta CA} = 16.36 * 2.62 = 42.87°C$$

$$T_J = \Delta T_{JC} + \Delta T_{CA} + T_A = 27.33 + 42.87 + 35 = 105.2°C$$

After two more iterations, the algorithm converges. The results are tabulated for comparison with those of the low resistance device in Table 2. In addition to the case of negligible thermal coupling, the idealized situation of perfect thermal coupling of the cases is also included for direct comparison. The performance trade-off between the two examples is that little thermal coupling will achieve a greater degree of current sharing at the expense of higher junction temperature in the hottest device (119°C versus 125°C). Since $T_{J(max)}$ most directly influences reliability, close thermal coupling of devices is encouraged. The manufacturer can best do this by paralleling chips on a common heat sink.

TABLE 2 — Static Current Sharing Performance of Mismatched MTP8N18s

	Negligible Thermal Case Coupling		Perfect Thermal Case Coupling	
	$r_{DS(on)}$ Min Device	$r_{DS(on)}$ Max Device	$r_{DS(on)}$ Min Device	$r_{DS(on)}$ Max Device
$r_{DS(on)}$ @ T_J = 25°C (Ohms)	0.230	0.400	0.230	0.400
I_D (Amps)	7.00	5.38	7.14	5.24
P_D (Watts)	21.0	16.1	21.3	15.7
Steady State T_J (°C)	125	104	119	110
$r_{DS(on)}$ @ Steady State T_J (Ω)	0.430	0.558	0.419	0.570

A point essential to the above calculations is that the steady state thermal resistance was employed to compute the junction temperatures. For pulsed conditions $R_{\theta JC}$ can vary significantly, and the transient thermal resistance obtained from the thermal response curves must be used to make this calculation. During switching transitions, there is insufficient time to establish differences in junction temperature and power MOSFETs may not current share in the same manner.

Dynamic Current Sharing Design Considerations

The term "dynamic" is broadened here to include not only current during turn-on and turn-off, but also peak current during narrow pulses and small duty cycles. Under these conditions, not enough RMS current is present to cause differential heating of the junctions which triggers the tendencies of the devices to share current. Since the argument supporting current sharing under static conditions is based on differences in junction temperature due to an imbalance of power dissipation and drain currents, that reasoning does not support the concept of current sharing during dynamic conditions. However, even without the benefit of the positive temperature coefficient, power MOSFETs can current share reasonably well with simple and efficient gate-drive circuitry.

The issues of greatest concern to those interested in dynamic current sharing of paralleled MOSFETs are listed and described in order below.

1. Device parameters that influence dynamic current sharing.
2. Variation of pertinent device parameters from lot to lot.
3. Required device parameter matching to achieve safe levels of current distribution.
4. The effects of switching speed on dynamic current sharing.
5. The requirements and effects of circuit layout.
6. The possibility of self-induced oscillations.

Device Parameters That Influence Dynamic Current Sharing

The device parameters that influence the degree of dynamic current sharing are the transconductance (g_{fs}), gate-source threshold voltage [$V_{GS(th)}$], input capacitance, and the on-resistance $r_{DS(on)}$. However, the device characteristic that most accurately predicts how well paralleled MOSFETs will current share during turn-on or turn-off is the transconductance curve, i.e., the relationship between the drain current and the gate-source voltage. To obtain optimum current distribution during turn-on and turn-off, the ideal situation is to have all gate-source voltages rising (or falling) simultaneously on devices with identical transconductance curves. This combination would ensure that as the devices switch through the active region, none would be overstressed by a current imbalance. Figures 6-2a, 6-2b and 6-2c show the nearly perfect degree of current sharing obtainable solely by matching the g_{fs} curves. The current probe used induced a 20 ns delay in the current waveform in the oscillograms shown.

Since plotting the entire g_{fs} curve of each device is very time consuming, matching $V_{GS(th)}$ or g_{fs} at some drain current has been suggested as a simpler criterion for matching paralleled MOSFETs. While much of the literature suggests the importance of matching $V_{GS(th)}$, which is normally defined as the minimum gate voltage at which a small drain current (usually specified as 1.0 mA) begins to flow, this does not accurately indicate the

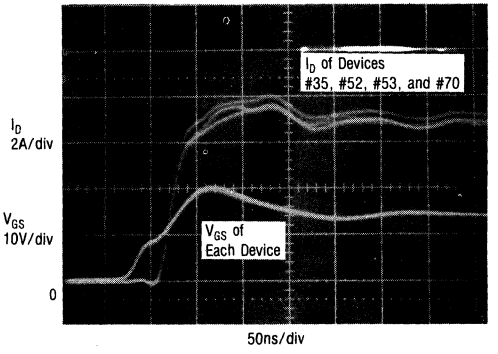


FIGURE 6-2a — PARALLELED TURN-ON

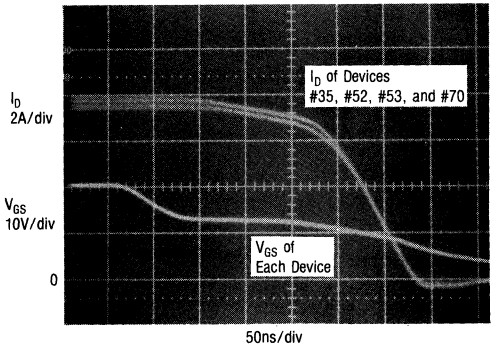


FIGURE 6-2b — PARALLELED TURN-OFF

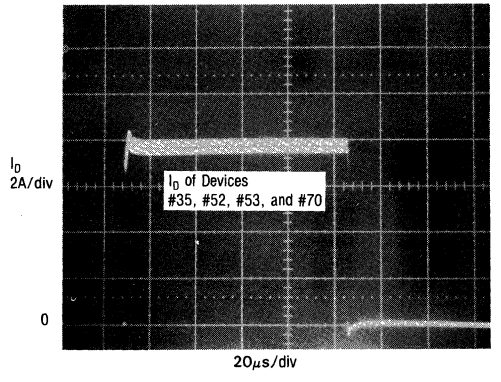


FIGURE 6-2c — COMPOSITE I_D WAVEFORM FOR TURN-ON AND TURN-OFF

FIGURE 6-2 — INDIVIDUAL I_D WAVEFORMS OF FOUR PARALLELED MTP8N18s WITH MATCHED TRANSCONDUCTANCE CURVES — RESISTIVE LOAD (DRAIN CURRENT WAVEFORMS ARE DELAYED 20 ns)

shape of the I_D versus V_{GS} curve at higher currents. Devices with 1.0 mA thresholds that vary by as much as 2.0 volts do not usually, but can, have nearly identical transconductance curves above 100 mA. Conversely, those devices out of a group of one hundred MTP8N18s found to have the widest variation of g_{fs} curves had thresholds that varied by only 4%. Therefore, for optimum current sharing, the ideal solution is to use devices with identical curves, and comparing thresholds may not be the best way to achieve this.

Another simple, yet more consistent, method is to match devices by comparing the maximum drain current they will conduct at a gate voltage higher than $V_{GS(th)}$. For example, all four devices shown in Figure 6-2 conduct an I_D of 4.0 A at a V_{GS} of 6.0 volts and were found to have nearly identical g_{fs} curves (Figure 6-3). Though similar to matching thresholds, this method matches points on the g_{fs} curve that are more germane to the intended application of the devices.

Variation of Pertinent Device Parameters from Lot to Lot

Before any definitive statement may be made concerning the degree or type of matching required for safe dynamic current sharing, the variation of pertinent device parameters from lot to lot must be known. Two wafer lots of the MTP8N18s, with sample sizes of 100 and 50 units respectively, were characterized for this pupose. The maximum and minimum values of threshold voltage, transconductance, and on-resistance are shown in Table 1. Figure 6-4 illustrates the widest variation in g_{fs} curves within Wafer Lot I and is similar to the results obtained from Wafer Lot II.

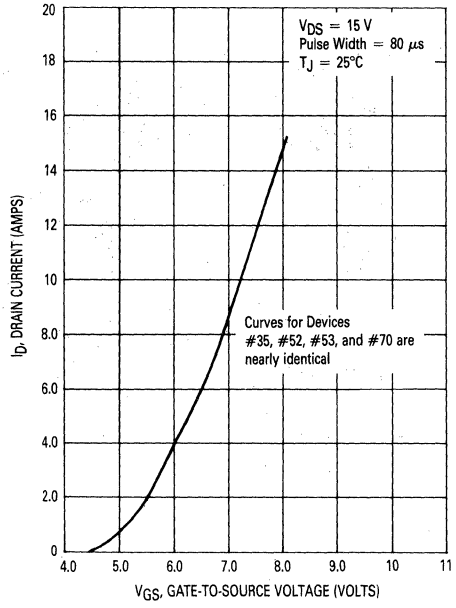


FIGURE 6-3 — TRANSCONDUCTANCE CURVES OF MATCHED MTP8N18s

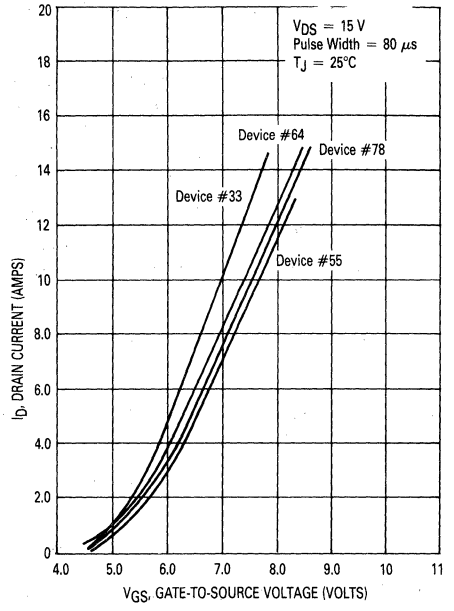


FIGURE 6-4 — WIDEST VARIATION IN TRANSCONDUCTANCE CURVES FOUND IN WAFER LOT I

Obviously, the possibility of larger than expected variations in these pertinent parameters diminishes as the number of sampled wafer lots increases. To get an adequate sampling of available devices, the user could characterize devices with different date codes or obtain units from several distributors.

Required Matching for Safe Levels of Current Distribution

After characterization and determining the degree of variation possible, the effects of matching or mismatching the critical device characteristics can be observed. The circuit used for this study is shown in Figure 6-5. Some of the possible modifications of the circuit include adding resistors in series with the gate to slow the turn-on and turn-off, and a second MOSFET may be included to clamp the gate bus to ground to observe the effects of very rapid turn-off.

In this discussion of resistive switching, Figure 6-2 will serve as a standard for comparisons since matching transconductance curves has achieved such good performance. Extreme care was taken to provide as pure a resistive load as possible. The 1.6 ohm load was constructed from 39, 62-ohm carbon composition resistors connected in parallel between two copper plates. Though the drain wiring and load inductances were very small, during rapid turn-on, the L/R time constant of the circuit may be the factor that limits the current rise times and not the switching speed of the MOSFETs.

One of the worst case situations is to parallel devices with greatly mismatched g_{fs} curves. Representing the

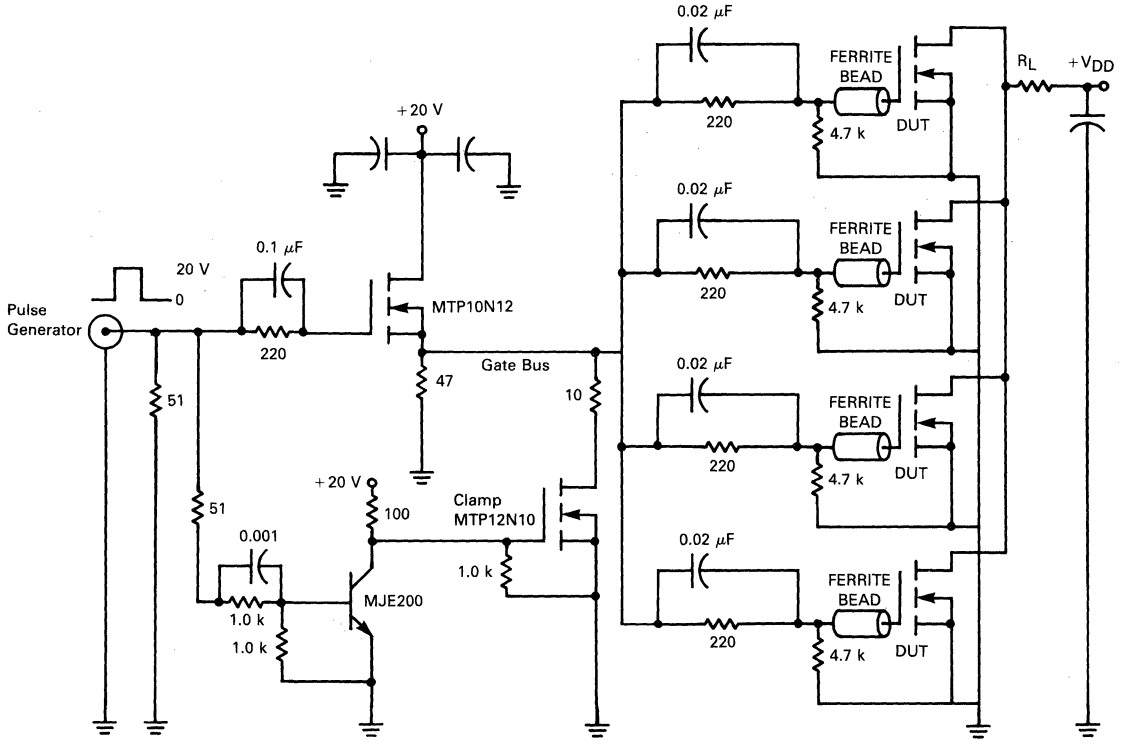


FIGURE 6-5 — DYNAMIC CURRENT SHARING TEST CIRCUIT

widest variation in the g_{fs} curves in Wafer Lot I, Figure 6-4 shows the curve of a device that will begin to turn on with a rising V_{GS} slightly sooner than the other three devices. It may be expected that device #33 will turn on first and possibly fail due to current overload. However, since the variation in the I_D versus V_{GS} curves of these mismatched devices is small, the failure will not occur. As shown in Figure 6-6, parallel operation of these mismatched devices in the given circuit poses no significant reliability hazard.

Matching the 1.0 mA thresholds does not guarantee the nearly perfect results of matching the g_{fs} curves, as shown in Figure 6-7. Although their thresholds were matched to within 2%, these devices exhibited a fairly wide variation in g_{fs} curves (Figure 6-8) which resulted in device #45 beginning its turn-off slightly sooner than the

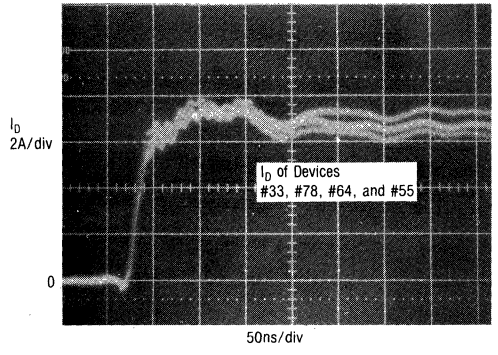


FIGURE 6-6a — PARALLELED TURN-ON

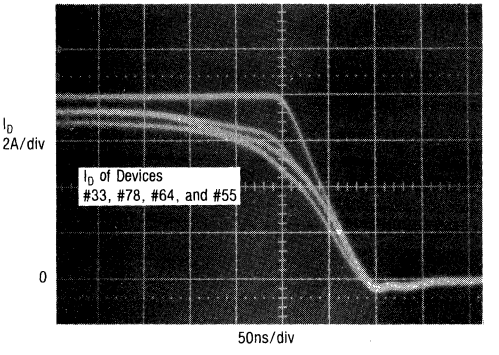


FIGURE 6-6b — PARALLELED TURN-OFF

FIGURE 6-6 — INDIVIDUAL I_D WAVEFORMS OF FOUR PARALLELED MTP8N18s WITH MISMATCHED TRANSCONDUCTANCE CURVES — RESISTIVE LOAD

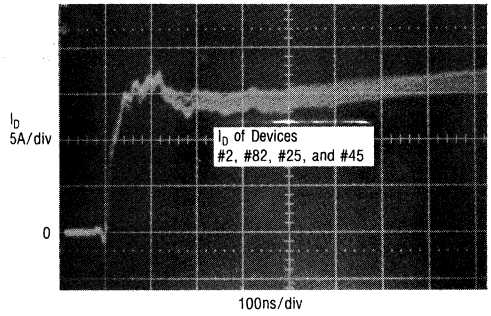


FIGURE 6-7a — PARALLELED TURN-ON

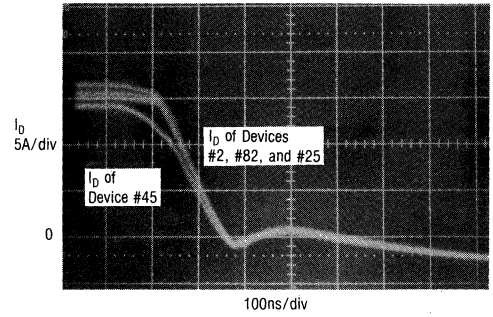


FIGURE 6-7b — PARALLELED TURN-OFF

FIGURE 6-7 — INDIVIDUAL I_D WAVEFORM OF FOUR PARALLELED MTP8N18s WITH MATCHED THRESHOLD VOLTAGES — RESISTIVE LOAD

Waveform/Curve Relations

Note: The order of the device numbers shown in all the current waveforms is important. The first number indicates the upper current waveform in each group with succeeding curves corresponding to the following device numbers. The order of waveforms is identified to enable the reader to correlate the devices' performance in the current waveforms to the devices' g_{fs} curves provided.

rest. The waveform photos again indicate that the performance of this group is also quite adequate. For comparison, the devices in Figures 6-9 and 6-10 have fairly similar g_{fs} curves even though their 1.0 mA threshold voltages vary by as much as 33%. Turn-on times for this group are almost simultaneous while the turn-off is just short of ideal.

Because the MTP8N18s of the two wafer lots were so close in characteristics, the worst conceivable mismatch that might occur could not be found. In order to study the effects of such a wide disparity between parameters, an MTP12N10 was paired with three closely matched

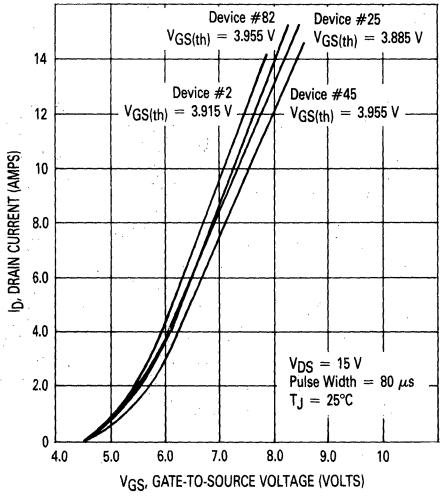


FIGURE 6-8 — TRANSCONDUCTANCE CURVES OF MTP8N18s WITH MATCHED THRESHOLD VOLTAGES

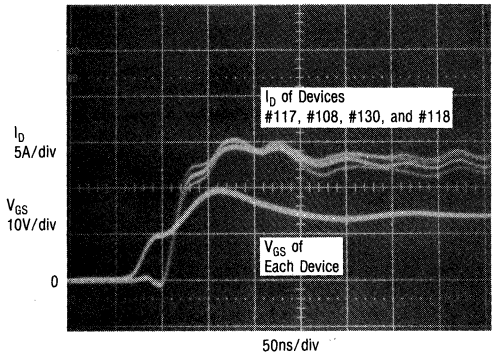


FIGURE 6-9b — PARALLELED TURN-OFF

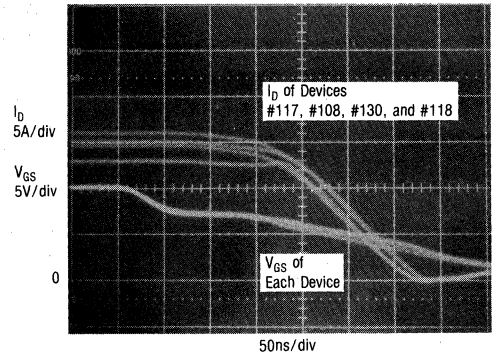


FIGURE 6-9a — PARALLELED TURN-ON

FIGURE 6-9 — INDIVIDUAL I_D WAVEFORMS OF FOUR MTP8N18s WITH MATCHED TRANSCONDUCTANCE CURVES AND MISMATCHED THRESHOLD VOLTAGES

TABLE 3 — Parameter Comparison of One MTP12N10 and Three MTP8N18s

Device Number	Device Type	$r_{DS(on)}$ I_D = 4.0 A (Ohm)	$V_{GS(th)}$ I_D = 1.0 mA (Volts)	g_{fs} I_D = 4.0 A V_{GS} = 15 V (Volts)	C_{rss} (pF)	C_{iss} (pF)	C_{oss} (pF)
#122	MTP12N10	0.145	3.600	4.300	90	685	395
#52	MTP8N18	0.238	3.955	4.762	45	700	220
#53	MTP8N18	0.256	3.900	4.444	45	700	245
#70	MTP8N18	0.255	3.930	4.444	45	700	235

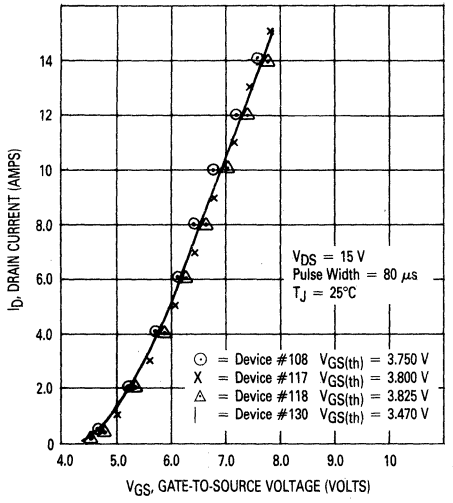


FIGURE 6-10 — TRANSCONDUCTANCE CURVES OF MTP8N18s WITH THRESHOLD VOLTAGE $V_{GS(th)}$ MISMATCH

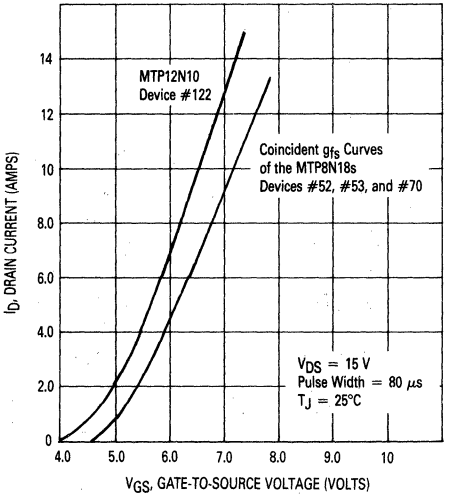


FIGURE 6-11 — TRANSCONDUCTANCE CURVES OF AN MTP12N10 AND THREE MTP8N18s

MTP8N18s. The MTP12N10 is a 12 A, 100 V device with the same die dimensions as the MTP8N18. Table 3 and Figure 6-11 compare the different device characteristics. The result of paralleling these four devices is shown in Figure 6-12.

The MTP12N10 is the last device to begin turn-on even though its transconductance curve rises earlier than those of the MTP8N18s. This is due to the larger C_{rss} (reverse transfer or gate-drain capacitance) which is effectively multiplied in value by the device gain due to the Miller effect. Although not completely simultaneous, the turn-off is smooth. By the time the MTP8N18s have completely switched off, the MTP12N10 has moved well into the active or constant current region. At that time, the total load

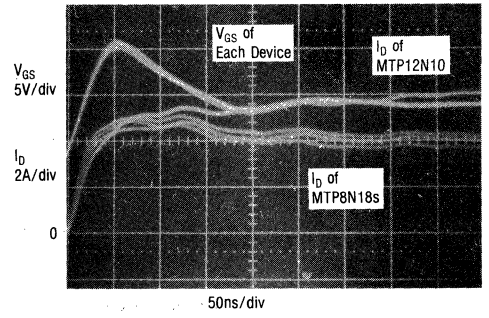


FIGURE 6-12a — PARALLELED TURN-ON

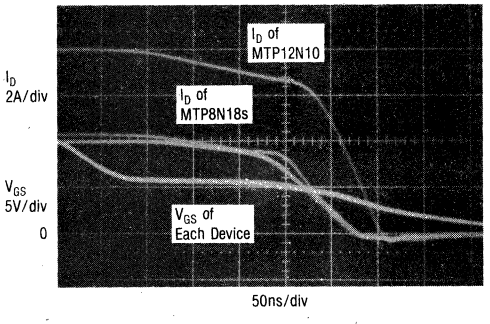


FIGURE 6-12b — PARALLELED TURN-OFF

FIGURE 6-12 — INDIVIDUAL I_D WAVEFORMS OF AN MTP12N10 PARALLELED WITH THREE MTP8N18s — RESISTIVE LOAD

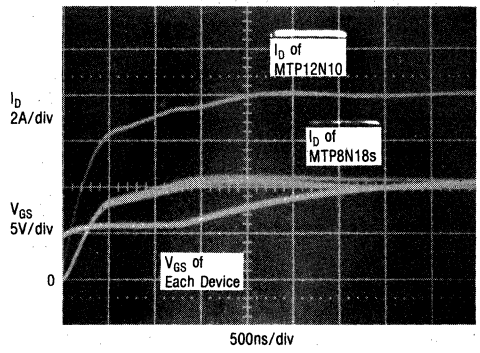


FIGURE 6-13a — PARALLELED TURN-ON

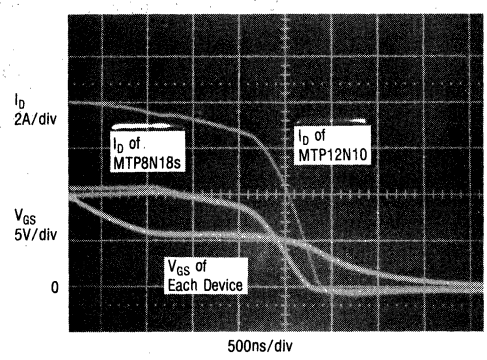


FIGURE 6-13b — PARALLELED TURN-OFF

FIGURE 6-13 — INDIVIDUAL I_D WAVEFORMS OF AN MTP12N10 PARALLELED WITH THREE MTP8N18s — RESISTIVE LOAD — SLOW SWITCHING

current has been substantially reduced and the slightly unsynchronized turn-off poses no threat to the MTP12N10 at these switching speeds.

It is apparent that for this specific application, i.e., resistive switching at moderate switching speed, device matching improves paralleled performance but is not necessary for safe operation. This recommendation will be extended to include both fast and slow switching speeds for both resistive and inductive loads provided certain circuit layout criteria are met.

Effects of Switching Speed on Dynamic Current Sharing

The gate-drive circuit used to switch the MTP12N10 and the three MTP8N18s was altered to either increase or decrease the switching speed. The four 0.02 μF speed-up capacitors were removed to determine the quality of current sharing as the gate-source voltages rise or fall at speeds that are fairly slow for power MOSFETs. The MTP12N10 is the first to turn on and the last to turn off (Figure 6-13) due to the differences in the devices' g_{fs} curves. During slow switching, the I_D versus V_{GS} curves can be used to accurately predict the I_D curves. For instance, the MTP12N10 begins to turn on when the composite gate-source voltage waveform reaches 4.0 volts, but the MTP8N18s hesitate until V_{GS} reaches 4.5 volts. Since the I_D waveforms are easily related via the g_{fs} curves to the rising or falling gate voltages and the variation in the g_{fs} curves over a product line are fairly small, slow switching of unmatched TMOS power MOSFETs can be a safe undertaking.

To judge the effects of rapid turn-off, a second MOSFET was added to clamp the gate-to-ground. This method achieves the 20 ns current fall times depicted in Figure 6-14. During such rapid switching, the V_{GS} and g_{fs} curves can no longer be used to accurately predict device performance due to package and lead parasitics such as the package source inductance. Once again however, these mismatched devices performed well as they were switched very rapidly through the active region. Although not quite as predictable, rapid resistive switching also appears safe.

A comparison of Figures 6-12, 6-13, and 6-14 indicates that faster switching tends to improve dynamic current sharing. This is in part a consequence of switching the devices through the active region at a much faster rate and correspondingly decreasing any difference in switching speeds. The parasitic source inductance also plays an important role as discussed below.

Dynamic Current Sharing With Inductive Loads

The investigation of the effects of current sharing with inductive loads was conducted using a fast recovery diode (40 A, 400 V) placed in parallel with a 135 μH inductor as a load. The diode was included not so much to protect the MOSFET against flyback voltages, but to test the paralleled transistors' ability to conduct the large peak reverse recovery current required by the diode. The standard of performance is again set by devices with matched g_{fs} curves and shown in Figure 6-15.

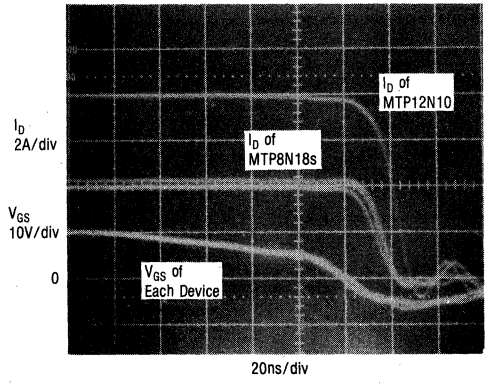


FIGURE 6-14 — INDIVIDUAL I_D WAVEFORMS OF AN MTP12N10 PARALLELED WITH THREE MTP8N18s — RESISTIVE LOAD — RAPID TURN-OFF

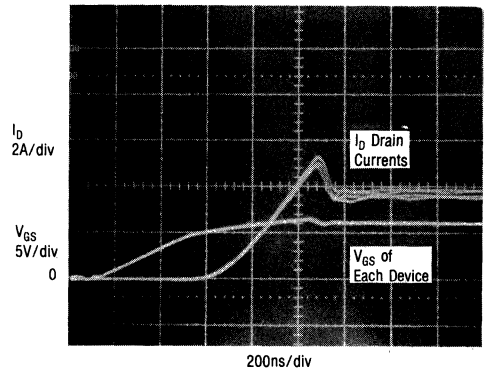


FIGURE 6-15a — PARALLELED TURN-ON

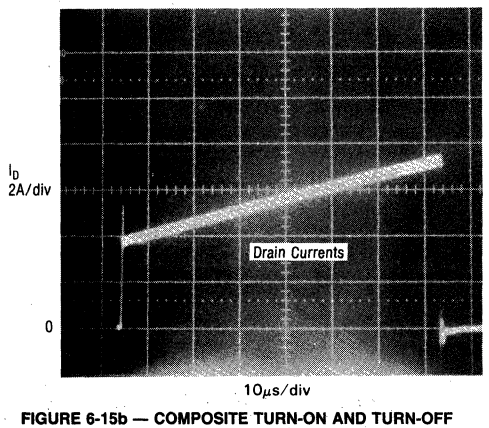


FIGURE 6-15b — COMPOSITE TURN-ON AND TURN-OFF WAVEFORM

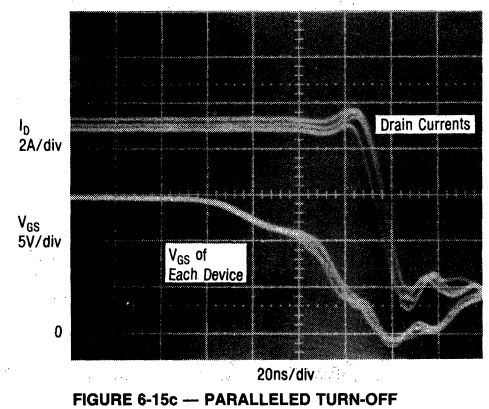


FIGURE 6-15c — PARALLELED TURN-OFF

FIGURE 6-15 — INDIVIDUAL I_D WAVEFORMS OF MATCHED MTP8N18s SWITCHING AN INDUCTIVE LOAD — DEVICES #35, #52, #53, and #70

To obtain a larger sample size for the worst case inductive testing, 250 additional MTP8N18s of unknown wafer origin were characterized for their widest variation in g_{fs} curves. The mismatched transconductance curves are shown in Figure 6-16. Figure 6-17 depicts both rapid and slow inductive turn-on and turn-off. This group of figures represents the greatest current imbalance seen in any set of mismatched MTP8N18s under any load conditions. While there are obvious current mismatches, they require only a small amount of derating to guardband against possible harmful situations. The keys to success are: 1) that pertinent device characteristics do not vary widely; and, 2) strict attention is given to the symmetry of the circuit layout.

Circuit Layout — A Critical Concern

Even with identically matched devices, dynamic current sharing between MOSFETs will be poor if an asymmetrical circuit layout is used. Obviously, if the gate-drives are different, unequal rates of gate-source voltage rise and fall can cause unsynchronized switching and even device failure in extreme cases. As the switching speeds of these devices are increased, the designer's perception as to what may constitute an important parasitic circuit element must change. When approaching the maximum switching speeds of power MOSFETs, even small variations in lead length may influence their paralleled switching performance. Unequal source wiring inductances are especially deleterious.

Figures 6-18a and 6-18b illustrate the effects of an imbalance in source wiring inductance. The devices and circuit layout are both closely matched except that an additional source lead inductance of 50 nH (1.5 inches of #22 wire formed into a 1-1/2 turn loop) was added to one device. As can be seen in the photographs, any source lead or wiring inductance will degenerate both the turn-on and turn-off speeds. Fortunately, perhaps the most important consideration for successful operation of paralleled MOSFETs is completely within easy control of the circuit designer. The circuit should be free from parasitics and as symmetrical as possible, especially for higher switching speeds.

Another obvious consideration is that the output impedance of the gate-drive circuits must be matched. Mismatched gate-drives will cause unsynchronized charging or discharging of the input capacitances, forcing the devices to begin switching at different times and rates.

The Benefit of Parasitic Source Inductance

Provided that the circuit layout is symmetrical, especially with respect to the source wiring inductance, faster switching can actually benefit the degree of current sharing between paralleled MOSFETs. During switching transitions of less than 100 ns, the source package inductance (approximately 7.0 nH) plays an important part in determining the shape of the rising and falling drain current waveform. The following example assumes the wiring inductance is negligible and relates only the effect of the source package inductance. The intent of this illustration is to show the significance of the package inductance and by extension relate the importance of the usually much larger wiring inductance.

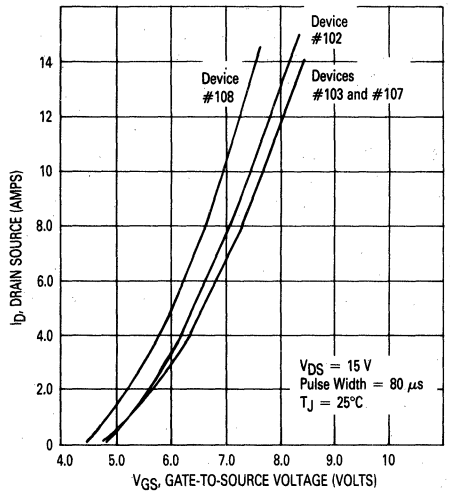


FIGURE 6-16 — WIDEST VARIATION IN TRANSCONDUCTANCE CURVES OF 250 ADDITIONAL MTP8N18s

Assuming a very rapid turn-off accompanied by a di/dt of 8.0 A/50 ns, the voltage appearing across the parasitic lead inductance is approximately 1.1 volts (v = L di/dt = 7.0 nH x 8.0 A/50 ns). This inductive drop must be added to the voltage appearing across the gate-source terminals to reveal the potential impressed at the chip. A difference in gate voltage of this size makes a significant difference in the magnitude of the drain current as the device switches through the active region. Therefore, equal source inductances will tend to equalize the rate of the rise and fall of the individual drain currents during rapid switching of paralleled MOSFETs. In effect, source ballasting is achieved during rapid switching.

Protecting the Circuit From Self-Induced Oscillations

Two of the most highly esteemed characteristics of the power MOSFET can combine to cause a problem in paralleled devices. Their high input impedance and very high frequency response may cause parasitic oscillations at frequencies greater than 100 MHz. This problem occurs when all gates are driven directly from a common node as in the circuit in Figure 6-19. Without individual gate

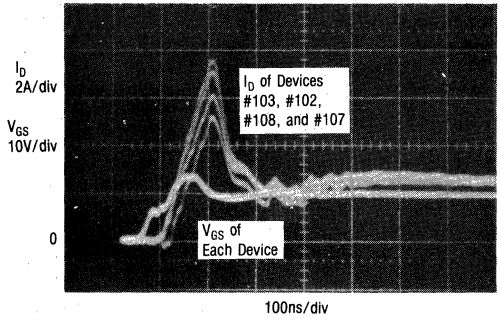


FIGURE 6-17a — RAPID TURN-ON SUPPLYING REVERSE RECOVERY CURRENT OF FREEWHEELING DIODE

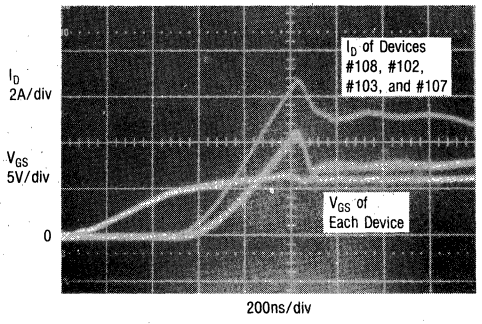


FIGURE 6-17b — SLOW TURN-ON SUPPLYING REVERSE RECOVERY CURRENT OF FREEWHEELING DIODE

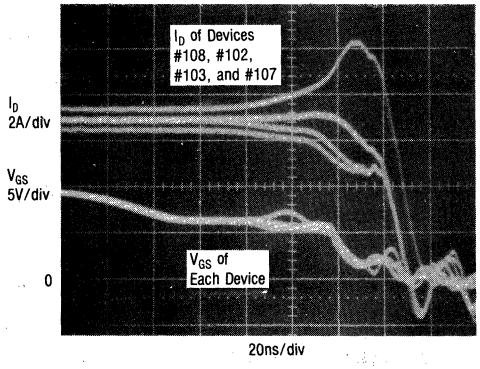


FIGURE 6-17c — RAPID INDUCTIVE TURN-OFF

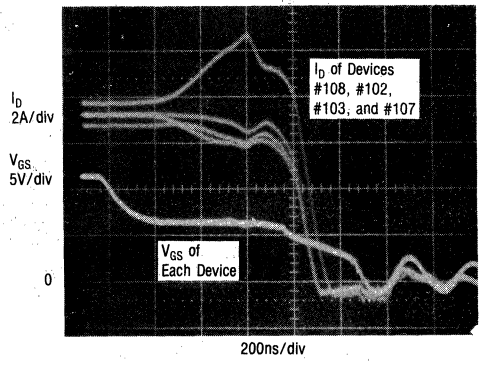


FIGURE 6-17d — SLOW INDUCTIVE TURN-OFF

FIGURE 6-17 — INDIVIDUAL I_D WAVEFORMS OF MISMATCHED MTP8N18s SWITCHING AN INDUCTIVE LOAD

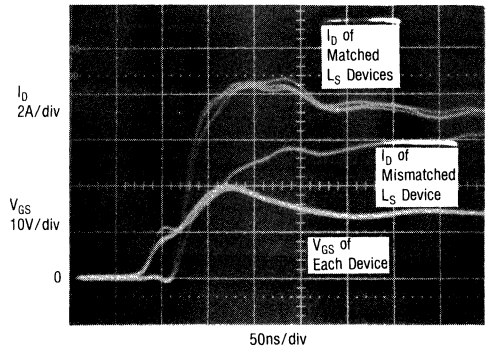


FIGURE 6-18a — TURN-ON

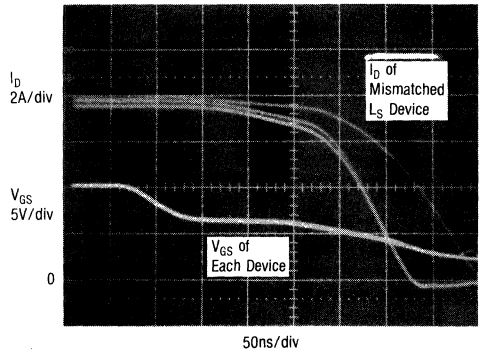


FIGURE 6-18b — TURN-OFF

FIGURE 6-18 — EFFECTS OF IMBALANCED SOURCE INDUCTANCES ON PARALLELED PERFORMANCE

resistances a high-Q network (Figure 6-20) is established that may cause the device to oscillate when operating in or switching through the active region. The device transconductance, gate-to-drain parasitic capacitance, and drain and gate parasitic inductances have all been shown to influence the stability of the circuit.

Although potentially serious, this problem is easily averted. By decoupling the gates of each device with lossy elements such as resistors or ferrite beads, the Q of the circuit can be sufficiently degraded to the point that oscillations are no longer possible (note dotted resistors shown in Figure 19). For the maximum switching speeds, the value of gate decoupling resistors should be kept as low as safely allowable. A value in the range of 10 to 20 ohms is generally sufficient.

A Practical Application — An Inductive Load

To show the feasibility of paralleling power MOSFETs in an application that imposes stresses typical of an inductive load, four MTP8N20's were paralleled in the circuit shown in Figure 6-21. At a 50% duty cycle and a V_{DD} of 44 V, the MOSFETs delivered about 450 W to the RC load. To minimize the power that the drain-source zener clamp must dissipate, MOSFET turn-off speed was limited by the placement of an 82 Ω resistor in series with each gate.

Again, the performance of interest is that of mismatched devices. In this case, fifty units from a newly designed mask set were tested for the widest variation in on-resistance (0.255 Ω to 0.230 Ω). The three highest $r_{DS(on)}$ devices were grouped with the lowest $r_{DS(on)}$ unit. Since a low $r_{DS(on)}$ usually indicates a high g_{fs}, the transconductance curves of these devices were also mismatched.

The degree of current sharing among these four units was well within safe operating limits. As expected, the lowest $r_{DS(on)}$ device carried the greatest on-state current. For clarity, only the on-state currents of the lowest and highest $r_{DS(on)}$ units are shown in Figure 6-22. The currents of the other two devices were nearly identical to device #8. As Figure 6-23 shows, the drain current of the lowest $r_{DS(on)}$ device, #11, peaked slightly due to its different g_{fs} curve.

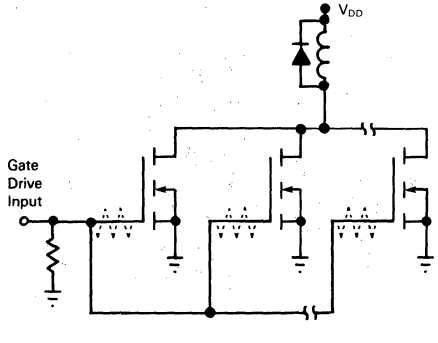


FIGURE 6-19 — METHOD FOR DRIVING PARALLELED MOSFETs USING GATE DECOUPLING RESISTORS

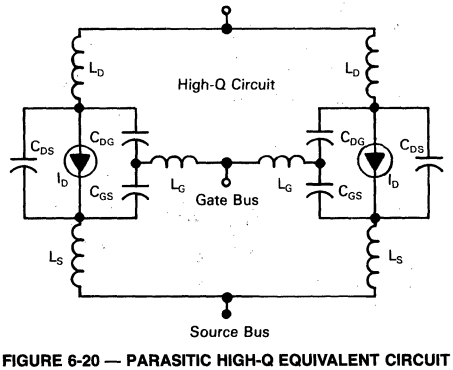


FIGURE 6-20 — PARASITIC HIGH-Q EQUIVALENT CIRCUIT OF PARALLELED MOSFETs WITHOUT GATE DECOUPLING RESISTORS

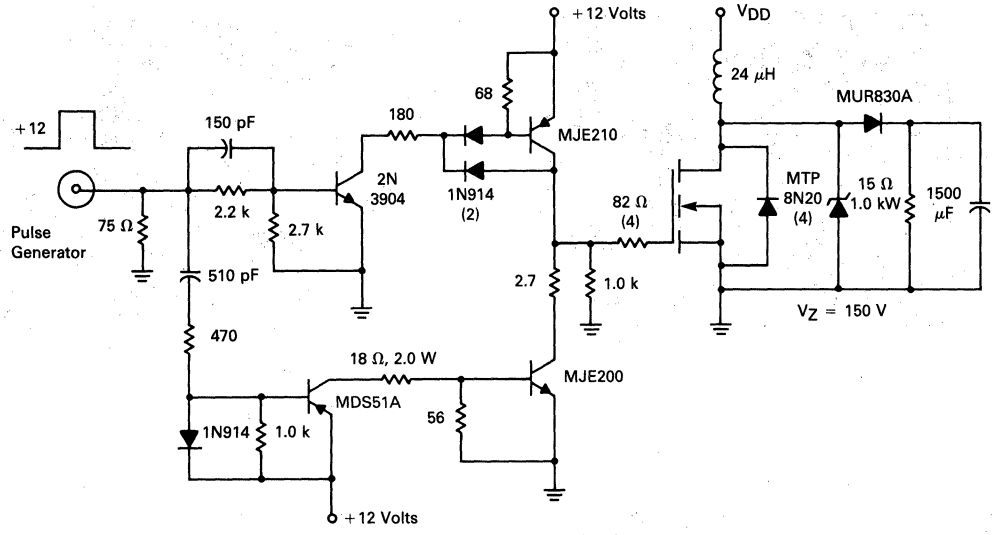


FIGURE 6-21 — CURRENT SHARING TEST CIRCUIT WITH AN INDUCTIVE LOAD

Each device was mounted on a separate heat sink, and the case temperatures were monitored to detect any thermal imbalances. Because of its low $r_{DS(on)}$, theory predicts that the case temperature of device #11 will be higher than the others. However, since the operating frequency was fairly high (40 kHz), the difference in switching losses may have also influenced the temperature comparison. Whether it was due to a variation in $r_{DS(on)}$ or g_{fs} curves, the temperature difference was very small (54.3°C for device #11 and 52.3°C for device #8) and did not significantly affect device performance, i.e., the degree of current sharing.

The following is a summary of recommendations and findings concerning static and dynamic current, sharing in paralleled power MOSFETs.

1. For static current sharing, the current mismatches are determined by the $r_{DS(on)}$ mismatch. A small degree of guardbanding or $r_{DS(on)}$ matching will ensure safe operation.
2. For dynamic current sharing, the turn-on and turn-off waveforms are largely determined by the transconductance curves. If matching is deemed necessary in a particular application, selecting devices by comparing g_{fs} curves is the most accurate approach. A simple, yet adequate, substitute is to match a single point on the g_{fs} curves at which the devices conduct significant drain currents.
3. Increasing the switching speeds in symmetrical circuits tends to equalize the rate of current rise and

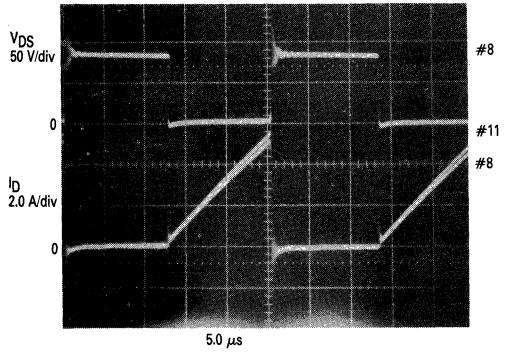


FIGURE 6-22 — I_D WAVEFORMS OF LOW AND HIGH $r_{DS(on)}$ DEVICES — INDUCTIVE LOAD

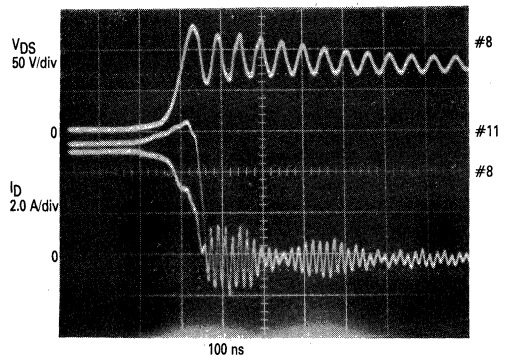


FIGURE 6-23 — I_D TURN-OFF WAVEFORMS OF LOW AND HIGH $r_{DS(on)}$ DEVICES — INDUCTIVE LOAD

fall in paralleled devices due to the ballasting effect of the parasitic source inductance.

4. The circuit layout should be as symmetrical as possible with respect to the gate-drive and the source, gate, and drain parasitic inductances.
5. In all applications, the gates should be decoupled with small resistors or ferrite beads to eliminate parasitic oscillations.

Paralleling Power MOSFETs in Linear Applications

Often lauded for their efficient high frequency switching capability, power MOSFETs are ideally suited for a myriad of switching applications. However, some of their other less renowned characteristics also make them attractive to designers of linear systems. Often the reason cited for their use is the inherent ruggedness of the MOSFET as evidenced by the lack of a second breakdown derating. Another characteristic that is appealing is the high input impedance that results in simplified gate-drive circuitry. Also, the transconductance is nearly linear over a wide operating range and its variation among devices in a given product line is small.

Although these benefits are significant, a method of predicting and stabilizing the operating point is necessary before linear operation can be successful. In the following sections a product line is characterized for the parameters pertinent to Q-point variation in the linear mode. The effects of a source resistor on the operating point and the small-signal transconductance are then discussed for single device operation. Finally, these concepts are extended to include the case of paralleled devices with special attention paid to the degree of current sharing.

Device Characteristics Important for Operating Point Stability

When developing a system that operates in the linear mode, it is often either desirable or imperative to accurately fix the system quiescent operating point (Q-point). The most pertinent graphs describing the operation of TMOS Power MOSFETs in the linear mode are those showing the output characteristics (Figure 6-24) and the transfer characteristics, or transconductance curves (Figure 6-25). However, since these are typical curves, they relate no information concerning how the operating point may vary within a given product line. For example, on the transfer characteristics curve a desired quiescent drain current of 4.0 amps may correspond to a gate-source voltage of 5.75 volts in a typical device. This gate voltage applied to an atypical device of the same product line may result in a drain current that ranges from 2.5 to 4.5 A.

Matching device parameters is often proposed as a means of ensuring some minimum variation in the Q-point. This approach, especially using the threshold voltage, is not the optimum solution. The gate-threshold voltage is defined as the minimum gate-source voltage at which the MOSFET conducts some small drain current, usually specified as 1.0 mA. On the scale that the transfer characteristics are usually drawn, this 1.0 mA drain current is very small and the exact threshold voltage is indiscernable. It is not difficult to find two devices with nearly identical transfer characteristics that have thresholds that vary by nearly 2.0 volts. Conversely, devices with matched thresholds can have significantly different transfer curves, usually due to a g_{fs} mismatch. Attempting to match devices by comparing transconductance or on-resistance also gives little assurance that the transfer curves will be similar.

If component screening is desired, the most direct method is to actually compare each I_D versus V_{GS} curve. Since this is often impractical, one of two other courses may be taken. The criteria for matching could be the drain current at the gate voltage that is typical of the desired quiescent current. Referring back to the previous example, one may select devices on the basis of I_D at a V_{GS} of 5.75 volts. The other solution, which completely eliminates any device screening, involves the use of source resistors and is detailed in the next section.

Junction temperature is another important variable that influences the quiescent operation point. Figure 6-25 shows that the g_{fs} curve of the MOSFET can be divided into two regions. Below a V_{GS} of 6.1 volts, an increase in T_J increases I_D. This is due to the negative temperature coefficient of $V_{GS(th)}$ dominating the positive coefficient of $r_{DS(on)}$. As T_J rises, the threshold voltage falls and I_D increases despite an increase in $r_{DS(on)}$.

At gate-to-source voltages greater than 6.1 volts, the temperature dependence of $r_{DS(on)}$ governs the change

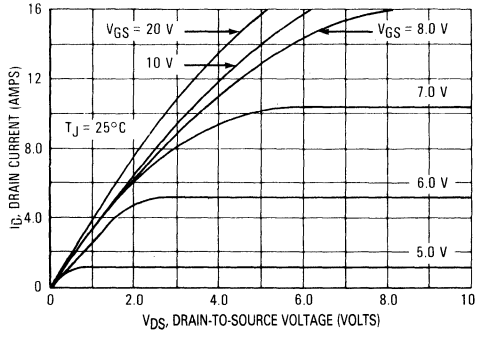


FIGURE 6-24 — TYPICAL OUTPUT CHARACTERISTICS OF AN MTP8N20

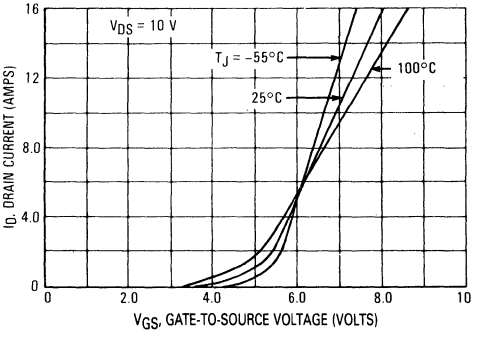


FIGURE 6-25 — TYPICAL TRANSCONDUCTANCE CURVES OF AN MTP8N20

in I_D. Even though $V_{GS(th)}$ is falling as T_J rises, the effect of the increase in $r_{DS(on)}$ begins to dominate, causing I_D to decrease. The temperature dependence of I_D necessitates the consideration of the effect that T_J has on the Q-point, especially at low drain currents where the percentage change in I_D is high.

Using a Source Resistor to Stabilize the Q-Point

Operating point stability can be improved without preselecting devices by using a source resistor. The placement of such a resistor provides degenerative feedback to the gate by decreasing V_{GS} by an amount proportional to the drain current (Figure 6-26). Equations for the small-signal transconductance and voltage gain with and without the source resistor are derived in Table 4.

Determining the effect of a source resistor on the operating point of a power MOSFET is a simple geometric exercise. The first step is to obtain, usually with a curve tracer, the transconductance curve of the device in question. With no source resistance (R_S = 0 Ω), a vertical line through the g_{fs} curve will indicate the drain current at a given V_{GS}. For instance, the device depicted in Figure 6-27 will conduct 0.375 A at a V_{GS} of 4.7 volts.

If a source resistor is included, the abscissa represents the gate-to-ground voltage (V_{GG}). The relationship between V_{GG} and I_D is determined by an R_S load line through a given V_{GG} with a slope of $-1/R_S$. Figure 6-27 shows that for an R_S of 2.0 Ω and a V_{GG} of 5.45 V, the Q-point is fixed so that I_D is still 0.375 A. The effects of varying the gate-to-ground voltage can be determined by constructing parallel lines through the gate voltages of interest. Changing the slope of the line graphically models changes in R_S.

To use the technique of employing a source resistor to improve Q-point stability, the worst case variation in the g_{fs} curves needs to be determined for the product line in question. For this study, 350 MTP8N18's from the same wafer lot were checked for the greatest difference in transconductance curves. The results are shown in Figure 6-28. With these curves, actually sizing R_S and determining the gate voltage for a desired operating point (with a defined allowable variation) is a very simple geometric exercise.

Assume that the desired conditions are as follows:

I_D quiescent = 0.4 A

Allowable I_{DQ} variation from 0.4 A is 0.05 A

T_J = 100°C

An R_S load line drawn through points A and B and extending down to the gate voltage axis determines both the required magnitude of R_S and the quiescent gate voltage. The figure could also be used to show the effects of swinging the gate voltage above and below the quiescent V_{GG}. The dashed curves in Figure 6-28 represent the transfer characteristics at a junction temperature of 25°C. Obviously, the curves vary enough to influence the

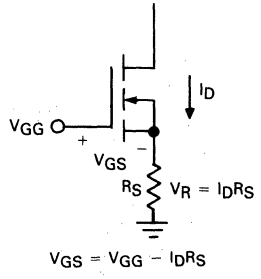
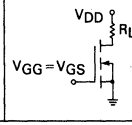
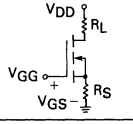


FIGURE 6-26 — SOURCE RESISTOR SUPPLIES NEGATIVE FEEDBACK TO THE GATE

TABLE 4 — Equations for the Small-Signal Transconductance and Voltage Gain With and Without a Source Resistor

	With No Source Resistor	With A Source Resistor
Small Signal Transconductance	$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$	$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$ $g_{fs}(\Delta V_{GG} - \Delta I_D R_S) = \Delta I_D$ $g_{fs}\Delta V_{GG} = \Delta I_D(1 + R_S g_{fs})$ $g'_{fs} = \frac{\Delta I_D}{\Delta V_{GG}} = \frac{g_{fs}}{1 + R_S g_{fs}}$
Small Signal Voltage Gain	$A_v = \frac{-\Delta V_{DS}}{\Delta V_{GS}}$ $= \frac{-\Delta I_D R_L}{\Delta I_D / g_{fs}}$ $\therefore A_v = -g_{fs} R_L$	$A'_v = -g'_{fs} R_L$ $= \frac{-R_L g_{fs}}{1 + g_{fs} R_S}$ $\therefore A'_v = \frac{-R_L}{1/g_{fs} + R_S}$
Circuits		

Primed numbers indicate the effective values for the MOSFET and source resistor combination.

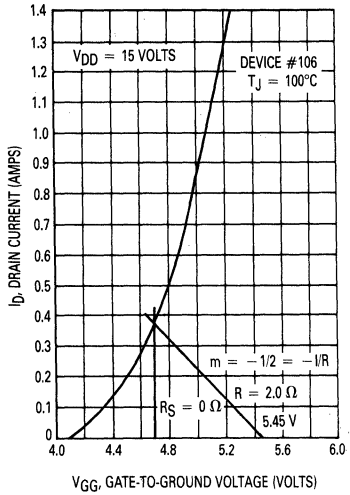


FIGURE 6-27 — GRAPHICAL METHOD OF PREDICTING THE EFFECT OF A SOURCE RESISTOR ON THE QUIESCENT OPERATING POINT

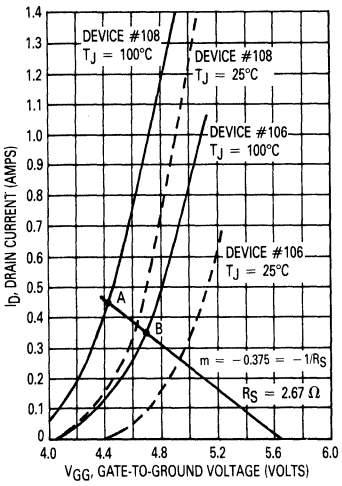


FIGURE 6-28 — USING A SOURCE RESISTOR TO STABILIZE THE QUIESCENT OPERATING POINT

selection of R_S if the device experiences large swings in T_J.

Paralleling MOSFETs in the Linear Mode

In many applications using MOSFETs in the linear mode, the quest is to obtain large swings in the load voltage and utilize as much of the maximum drain-to-source voltage rating as possible. With a large quiescent drain voltage, I_{DQ} must be fairly small to keep the MOSFET power dissipation within manageable levels.

Unfortunately, paralleling in the linear mode at a low I_{DQ} and a high V_{DSQ} is not as straightforward as paralleling in switching applications, for instance. Since this is the most difficult and most common case of paralleling in the linear mode, it is the one that is addressed here.

One problem is that at low currents the potential I_D mismatches, as a percent of the total load current are much greater. As an illustration, one device may conduct 0.3 A at a V_{GS} of 5.0 V, whereas a second device may conduct 1.25 A at the same V_{GS}. If these two devices are operated in parallel in the linear mode, the second would dissipate far more power than the first. Unlike MOSFETs that are paralleled in switching applications, the difference in junction temperature forces an even greater disparity in the amount of current each device conducts.

As explained earlier, at low drain currents the temperature dependence of the drain current is dominated by the negative temperature coefficient of $V_{GS(th)}$ rather than the positive coefficient of $r_{DS(on)}$. Consequently, the device that is dissipating the most power will heat up, carry more current and dissipate even more power.

Although the situation appears to be hopeless — very wide variations in g_{fs} curves causing even greater differences in power dissipation — the use of source resistors can minimize the differences and dramatically improve the chance of success.

Using a source resistor to stabilize the operating point of devices with widely differing g_{fs} curves is also applicable to improving current sharing among MOSFETs operated in the linear mode. If the Q-points are closely matched, then the paralleled devices will, by definition, carry nearly the same drain currents and incur approximately the same power dissipation.

In this study, the devices with widest variation in g_{fs} curves were paralleled in the circuit shown in Figure 6-29. Individual source resistances of 3.3 Ω were chosen as a good compromise between a stable Q-point and the lower system gain are poorer efficiency attributable to an increase in R_S. Table 5 establishes the equations for g_{fs} and small signal voltage gain of paralleled MOSFETs with and without source resistors.

Figure 6-30 shows the results of pairing the devices with the widest mismatch in g_{fs} curves. Note how the drain currents can be predicted by relating the g_{fs} curves (Figure 6-31) to the instantaneous gate voltage. Case temperatures were also monitored, but the difference was not as great as expected. While the device that carried the most current ran hotter, it did so by only a couple of degrees (83 versus 85°C). A difference of 5 to 10°C was expected but did not materialize, most likely due to slight variations in the heat sinks. The MOSFETs were mounted on separate heat sinks, again to simulate a worst case

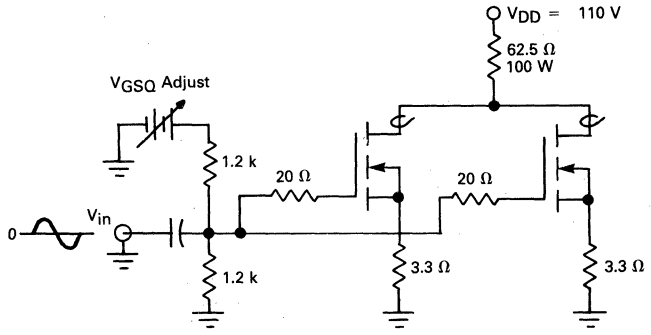


FIGURE 6-29 — CIRCUIT TO TEST CURRENT SHARING IN PARALLELED MOSFETs OPERATING IN THE LINEAR MODE

TABLE 5 — Equations for the Small Signal Transconductance and Voltage Gain of Two Paralleled MOSFETs With and Without Individual Source Resistances.

	With No Source Resistors	With Individual Source Resistors, R_S
Small Signal Transconductance	$\Delta I_{D1} = \frac{g_{fs1}}{\Delta V_{GS}}, \Delta I_{D2} = \frac{g_{fs2}}{\Delta V_{GS}}$ $\Delta I_{D1} + \Delta I_{D2} = \frac{g_{fs1} + g_{fs2}}{\Delta V_{GS}}$ $g_{fs1} + g_{fs2} = \frac{\Delta I_{D1} + \Delta I_{D2}}{\Delta V_{GS}}$ $\therefore g_{fsT} = g_{fs1} + g_{fs2}$	$g_{fs1}(\Delta V_{GS1}) = \Delta I_{D1}, g_{fs2}(\Delta V_{GS2}) = \Delta I_{D2}$ $g_{fs1}(\Delta V_{GG} - \Delta I_{D1} R_S) + g_{fs2}(\Delta V_{GG} - \Delta I_{D2} R_S) = \Delta I_{D1} + \Delta I_{D2}$ $g_{fs1}(\Delta V_{GG}) + g_{fs2}(\Delta V_{GG}) = \Delta I_{D1}(1 + g_{fs1} R_S) + \Delta I_{D2}(1.0 + g_{fs2} R_S)$ $(g_{fs1} + g_{fs2})(\Delta V_{GG}) = (\Delta I_{D1} + \Delta I_{D2})(1.0 + \overline{g}_{fs} R_S)$, where $\overline{g}_{fs} = \frac{g_{fs1} + g_{fs2}}{2}$ $\therefore g'_{fsT} = \frac{\Delta I_T}{\Delta V_{GG}} = \frac{g_{fs1} + g_{fs2}}{1.0 + \overline{g}_{fs} R_S}$
Small Signal Voltage Gain	$A_v = \frac{-\Delta V_{DS}}{\Delta V_{GS}} = \frac{-\Delta I_{DT} R_L}{\Delta I_{DT}/g_{fsT}}$ $\therefore A_{vT} = -g_{fsT} R_L$	$A'_{vT} = -g'_{fsT} R_L = \frac{-R_L(g_{fs1} + g_{fs2})}{1.0 + \overline{g}_{fs} R_S}$

Primed variables indicate the effective value for the MOSFET and source resistor combination.
Subscript "T" indicates the total value for all MOSFETs in parallel.

condition. Close thermal coupling by placing units on the same heat sink is recommended to minimize variations in T_C and T_J and therefore decrease any thermally induced differences in g_{fs} curves.

The benefits of device matching are shown in Figure 6-32. The nearly identical drain currents were obtained by matching devices by comparing the drain currents they would conduct at a V_{GS} of 4.7 volts and a junction temperature of 25°C. The slight mismatch at higher drain currents is mainly due to a small difference in g_{fs} curves at a T_J of 100°C. The case temperatures of these two devices were essentially identical. The 20 Ω gate resistors in Figure 6-29 serve an important function. The high input impedance and high frequency capabilities of the MOSFET present the possibility of self-induced oscillations in paralleled devices. Inserting small resistances in series with each gate defuses the problem by degrading the Q of the LC network formed by the gate-and-drain inductances and the MOSFETs gate-to-drain capacitance. The magnitude of R_S necessary to allow trouble-free operation depends on the value of each of the circuit parasitics. The circuit in Figure 6-29 oscillated with series gate resistances of 10 Ω, but stabilized with 20 Ω. Increasing R_S results in a more stable circuit at the expense of lower bandwidth.

In conclusion, the same method used to stabilize the operating quiescent point of small signal MOSFETs can

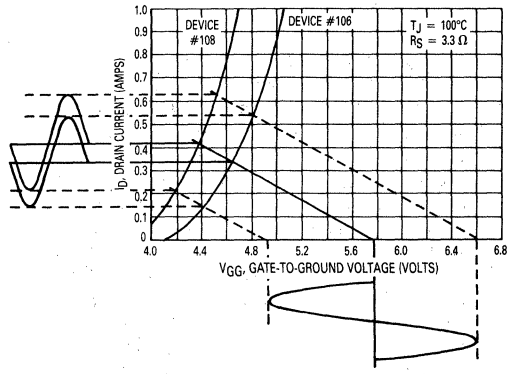


FIGURE 6-31 — TRANSFER CHARACTERISTICS AND R_S LOADLINE OF MISMATCHED MTP8N18s

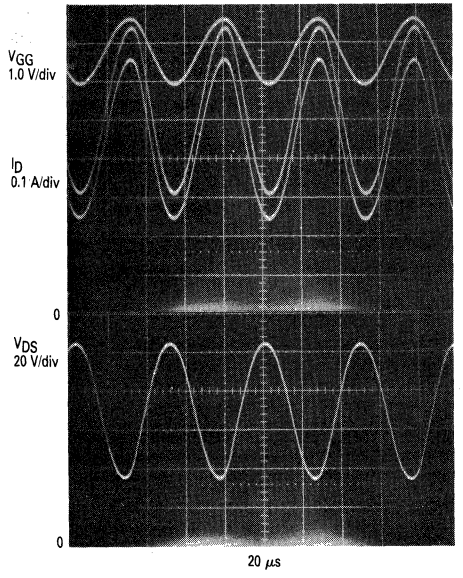


FIGURE 6-30 — V_{GG}, I_D AND V_{DS} WAVEFORMS OF MISMATCHED MTP8N20s PARALLED IN THE LINEAR MODE R_S = 3.3 Ω

rents is mainly due to a small difference in g_{fs} curves at a T_J of 100°C. The case temperatures of these two devices were essentially identical. The 20 Ω gate resistors in Figure 6-29 serve an important function. The high input impedance and high frequency capabilities of the MOSFET present the possibility of self-induced oscillations in paralleled devices. Inserting small resistances in series with each gate defuses the problem by degrading the Q of the LC network formed by the gate-and-drain inductances and the MOSFETs gate-to-drain capacitance. The magnitude of R_S necessary to allow trouble-free operation depends on the value of each of the circuit parasitics. The circuit in Figure 6-29 oscillated with series gate resistances of 10 Ω, but stabilized with 20 Ω. Increasing R_S results in a more stable circuit at the expense of lower bandwidth.

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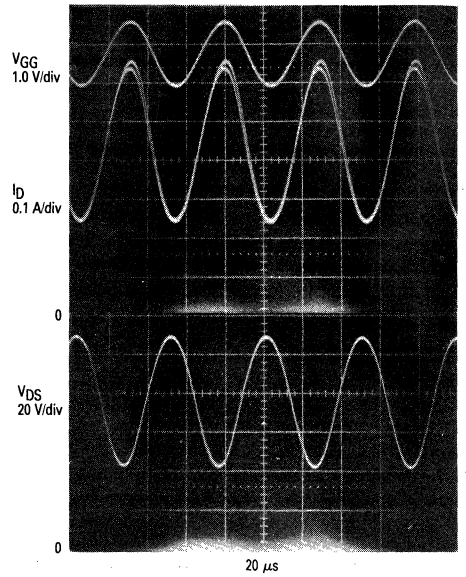


FIGURE 6-32 — V_{GG}, I_D AND V_{DS} WAVEFORMS OF MATCHED MTP8N20s PARALLELED IN THE LINEAR MODE R_S = 3.3 Ω

be easily extended to linear applications of power MOSFETs. After sampling a product line to obtain the widest expected variation in g_{fs} curves, a simple graphical technique can be used to accurately predict the Q-point associated with a given source resistor and gate-to-ground voltage.

Since small variations in Q-point limit possible variations in drain current, successful paralleling is also achievable with this same method. The only additional consideration is the need to limit potential self-induced oscillations with individual gate suppression reistors.

Drain-to-Source Diodes

The previous text on paralleling power MOSFETs has shown the effects of parameter matching (or unmatching) on the degree of current sharing when the FETs are operating in either switching or linear applications. However, it has not described the effects on the paralleled drain-source diodes when these diodes are used as clamp or free-wheeling diodes in practical applications. These diodes can be used in multi-MOSFET switching applications (see Chapter 11 on characterizing D-S Diodes) when the diode switching speeds are commensurate with the application. In a half bridge, as an example, the diode of one FET protects the drain-source of the second FET and, conversely, the diode of the second FET protects the first FET. Whatever the circuit configuration, the equivalent circuit reduces to that of a clamped inductive load, whereby the drain-source diode is effectively across the load inductance (Figure 6-33).

When power MOSFETs are paralleled in switching applications, the question arises as to how well their intrinsic diodes share the clamped current. To determine this, three MOSFETs were paralleled in the circuit shown in Figure 6-34. The test circuit (a complete schematic is shown in Figure 11-19 of Chapter 11) was duty cycle controlled to produce a continuous load current; thus, the commutated diode current indicated both the reverse recovery time t_{rr} and turn-on time t_{on}. The individual and total diode currents, as well as the driver drain current, were monitored.

To obtain some indication of a worst case condition, a modest sample (20 pieces) of MTM20N15s were characterized for parameters that affect their paralleled performance. The forward on-voltage of the diodes at 10 A ranged from 1.05 to 1.20 volts, and t_{rr} varied from 0.25 to 0.32 μs. Devices with the widest mismatch in parameters were grouped and tested in the circuit shown in Figure 6-34.

Testing indicated that current mismatches were small, even in devices with the greatest difference in D-S diode on-voltage. Figure 6-35 shows the current waveforms of three paralleled diodes and the expected mild mismatch. Also shown is a representation of I_{TOTAL}, which is somewhat distorted due to the saturation of the current transformer that was used.

Current waveforms of devices with the widest variation in t_{rr} are shown in Figure 6-36. Again, even though the diodes are mismatched, the synchronized turn-on and turn-off transitions illustrate the high degree of current sharing that occurs as the load current is commutated between the freewheeling diodes and the drive transistor.

Applications of Paralleling MOSFETs

Paralleling Power MOSFETs in a Very Fast, High Voltage High Current Switch

There are many applications requiring an extremely fast high voltage, high current semiconductor switch, especially for device characterization, where the switch must

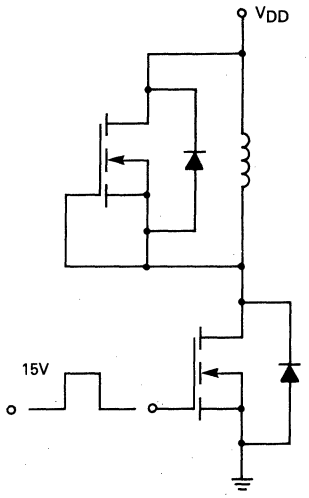


FIGURE 6-33 — INTRINSIC D-S DIODE CLAMPING AN INDUCTIVE LOAD

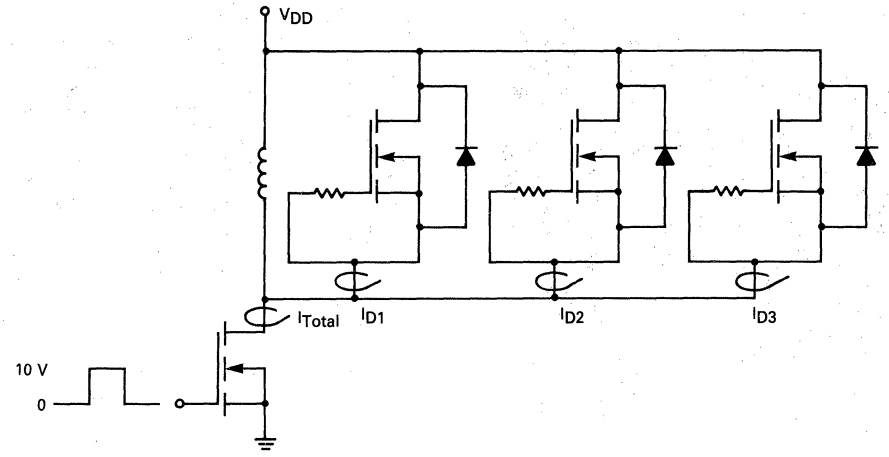


FIGURE 6-34 — TEST CIRCUIT TO OBSERVE CURRENT SHARING OF PARALLELED D-S DIODES

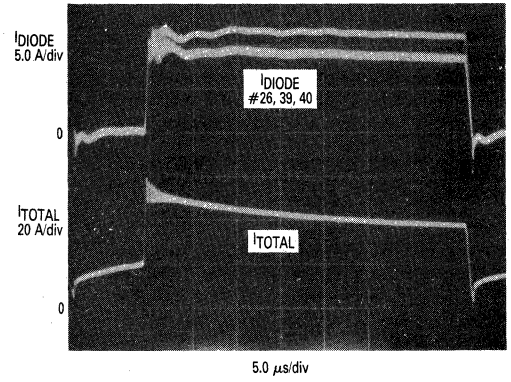


FIGURE 6-35 — DRAIN-SOURCE DIODE ON CHARACTERISTICS OF THREE MTM20N15s WITH MISMATCHED D-S DIODE ON-VOLTAGES

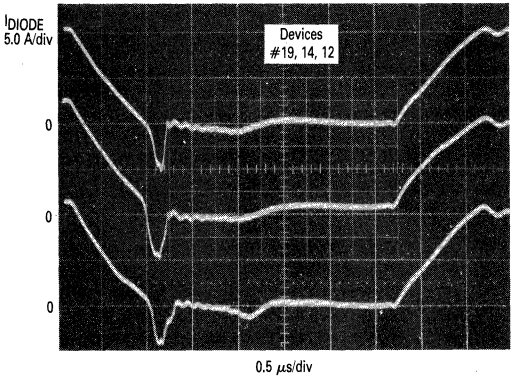


FIGURE 6-36 — PARALLELED DIODE TURN-ON AND TURN-OFF OF MTM15N20s WITH MISMATCHED t_{rr}

be much faster than the device under test (DUT). Power MOSFETs serve this function extremely well, but they are presently limited in current capability. However, they can be readily paralleled to increase the current, without using current sharing ballast resistors, due to the inherent positive temperature coefficient of the drain-source ON-resistance $r_{DS(on)}$. For example, if the transconductance g_{fs} of the FETs are unmatched, the FET with the highest g_{fs} would tend to take initially the largest drain current, but due to the greater dissipation ($I_D^2 r_{DS(on)}$) and resulting temperature rise, $r_{DS(on)}$ would increase, thus, self-limiting the current. This process tends to equalize the drain currents of the respective devices.

A circuit for generating this fast pulse is shown in Figure 6-38. It uses 15 N-Channel power MOSFETs in parallel as the output power switch to achieve the system capability of 150 A of peak, pulsed current. The FETs used were unmatched TO-220 MTP5N40(2.7 V < $V_{GS(th)}$ < 3.9 V) with 400 V blocking capability BV_{dss}, 5.0 A continuous drain current rating (10 A pulsed) and specified $r_{DS(on)}$ of 1.0 Ω max. The TO-220 devices lend themselves to efficient circuit layout and packaging (Figure 6-37).

The particular application for which this circuit was designed required the DUT to be referenced to ground (drain circuit); consequently, the switch is powered with a negative, high voltage supply ($-V_{ss}$) tied to the FETs sources. Thus, the ground referenced pulse generator output must be level translated to this negative supply. For fast switching, this translator must have the current drive capability for quickly charging the power MOSFETs input capacitances C_{iss} and reverse transfer capacitance C_{rss}. To accomplish this, two P-Channel MTP2P45's are configured as a parallel connected, series switch. These FETs are turned on by the negative going input pulse derived from a 50 V, 10 ns rise time pulse generator. A

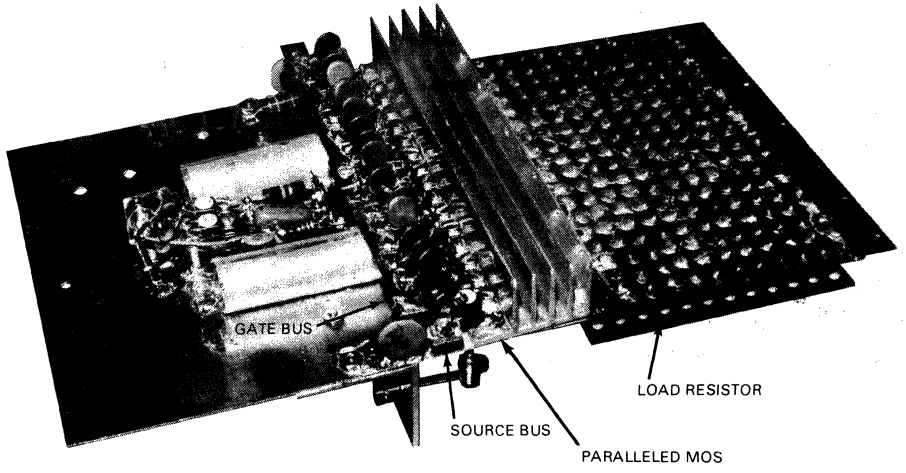


FIGURE 6-37 — BREADBOARD LAYOUT OF THE SWITCH ILLUSTRATING TIGHT PACKAGING CONCEPTS

20 V zener diode is used to protect the gate-source and still allows adequate gate-drive for rapid switching of the drain circuit. Connected to the drain is a current limiting resistor R2 (with speed-up capacitor C2) feeding the 15 respective gate circuits (only circuits 1 and 15 are shown); each circuit consists of a direct-coupled resistor, speed-up capacitor and protection zener diodes. The zener diodes come into operation when high V_{SS} (−160 V) is used. When V_{SS} is reduced to as low as 40 V, the gate-drive voltage dividers still provide adequate drive. For low duty cycles (< 1.0%), the resistors can be relatively low wattage. The circuit can be operated within the blocking

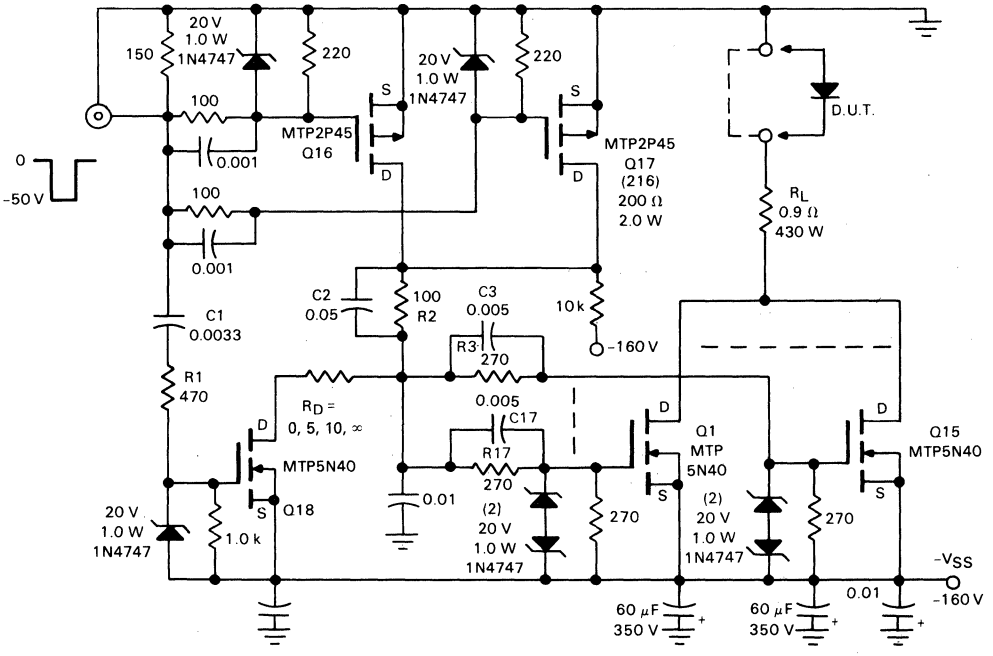


FIGURE 6-38 — PARALLELED POWER MOSFETs 150 A SWITCH

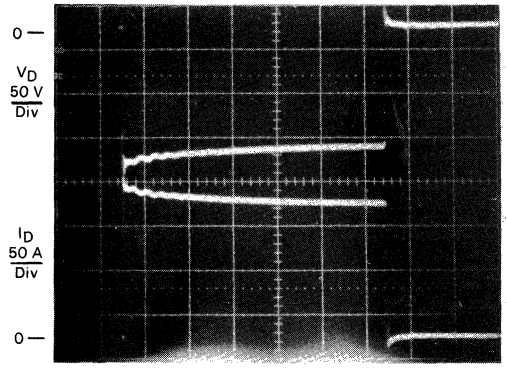


FIGURE 6-38 — SWITCHED VOLTAGE AND CURRENT

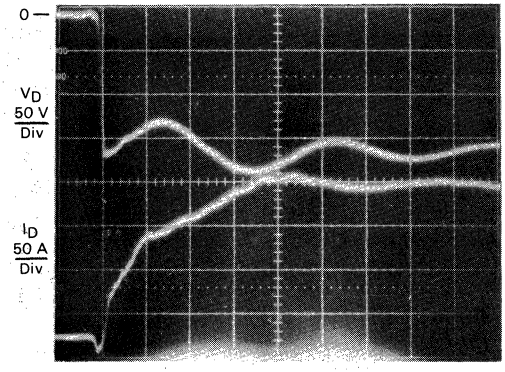


FIGURE 6-39 — TURN-ON DRAIN VOLTAGE AND CURRENT

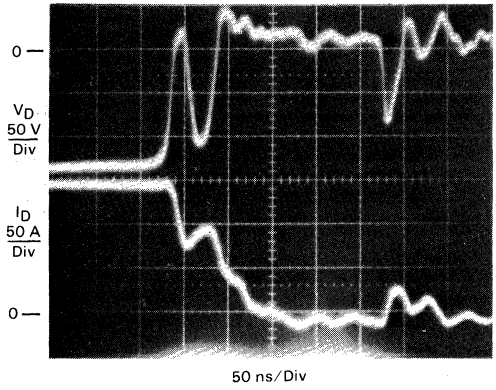


FIGURE 6-40 — TURN-OFF WITH CLAMP, R_D = 0

voltage capability of the FETs (to 400 V), but the passive circuit elements should be scaled up accordingly.

To improve the turn-off switching times of the power switch, the FET capacitance must be quickly discharged. This is accomplished by the N-channel FET clamp Q18 which, when turned on, supplies the reverse gate voltage to the power switch through the voltage storing effect of C3 across R3. FET Q18 is turned on coincident with the trailing edge of the input pulse by means of the differentiating network C1-R1, the derived positive-going pulse supplying the gate-drive and duration for the clamp action.

The complete pulse-width voltage and current waveforms are shown in Figure 6-38 with the time expanded turn-on and turn-off waveforms shown in Figures 6-39 and 6-40.

For these test conditions (V_{SS} = −160 V, R1 ≈ 0.93 Ω), approximately 150 A at 140 V (21 kW peak) was switched in extremely fast times; the voltage turn-on time was less than 10 ns and the current rise time being circuit inductance limited to about 250 ns.

Without the turn-off clamp circuit of Q18 the drain voltage (and resistive load drain current) turn-off time was about 1.0 μs (Figure 6-41a) due to the time required to discharge the FET's capacitances.

With the clamp, this time can be substantially reduced (0.2 μs) as shown in the photos of Figures 6-41b and 6-41c, the capacitance discharge limiting resistance R_D being 10 Ω and 5.0 Ω respectively. As this resistor value is decreased, the FET will turn-off faster, but consequently be subjected to greater switching perturbations (Figure 6-40, R_D = 0). Thus, the turn-off characteristics can be somewhat tailored to the requirements.

Care should be exercised in the layout of the fifteen parallel FET's, especially with the gate-source drive circuitry. The fifteen FET's are mounted side-by-side with the gates and sources tied to their two respective, parallel run busses (Figure 6-37). Device lead lengths should be made as short as possible and the source buss should be RF by-passed at several points along its length to minimize reactive effects.

Obtaining high power resistive loads with low inductance is a problem. For a pulsed current of 150 A and a low resistance of about 0.93 Ω, the peak power would be about 21 kW. Obviously, the duty cycle has to be very low

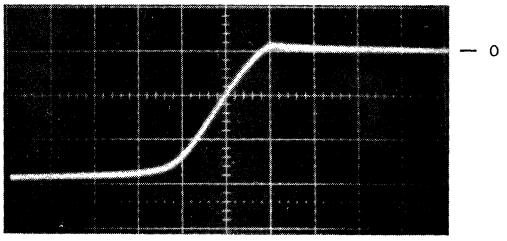


FIGURE 6-41a — TURN-OFF DRAIN VOLTAGE $R_D = \infty$

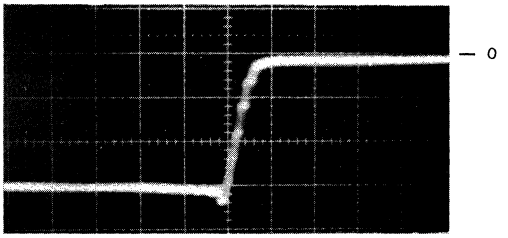
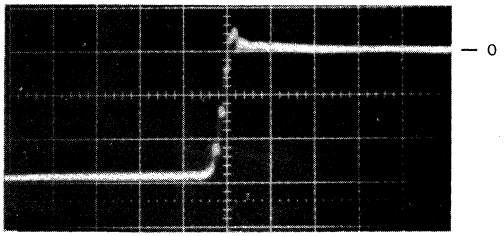


FIGURE 6-41b — TURN-OFF DRAIN VOLTAGE $R_D = 10\ \Omega$



Vert. = 500 V/Div
Horiz. = 500 ns/Div

FIGURE 6-41c — TURN-OFF DRAIN VOLTAGE $R_D = 5.0\ \Omega$

for this application to avoid overheating the load resistor. This resistor was fashioned with 216,200 Ω, 2.0 W, metal oxide resistors sandwiched in parallel. This resulted in a load resistor of approximately 430 W capability. Therefore, duty cycles of less than 1.0% should be used to ensure operation within the load rating while still offering good oscilloscope viewing.

Fast, Complementary Power MOSFET Switch

Many present day semiconductors require test circuits that can supply large pulsed currents and fast voltage transitions.

In today's real world circuits, rectifiers are vital components in motor controls and in switching power supplies as the operating frequency and power level increases. Rectifier characteristics and selection can be critical for these applications.

Due to its fast switching speed, the complementary power FET switch, shown in Figure 6-42, is useful in measuring forward (t_{fr}) and reverse (t_{rr}) recovery times of fast recovery rectifiers, as well as for general uses requiring a complementary power signal.

The internal collector-emitter diode in power Darlington transistors and the drain-source diode in power FETs can be of great interest to the circuit designer. Rectifier operation is dependent on several conditions, two of which are the turn-off rate (di/dt) of forward current and the rate of rise (dv/dt) of the reapplied blocking voltage.

In some switching power supplies, a designed-in dead time is required between the switching transistors to avoid simultaneous conduction. The duration of the dead time and the dv/dt of the reapplied blocking voltage can be critical, especially for some power MOSFETs. This complementary switch, with dv/dt adjustment and control of the dead time, can help determine the capability of power FETs in circuits when the above conditions are important.

Circuit Configuration and Operation

Two CMOS Quad 2 input NOR gates (MC14001) are used for pulse generation and signal delay. Gates A1 and A2 are configured as an astable multivibrator (MV), clocking the respective delay and pulse width monostable MV's. The turn-on pulse is frequency (R1) and width adjustable (R4) whose output feeds, in order, cascaded bipolar transistors Q5, Q6, power FET Q7 and the N-Channel output switch Q8.

Pulse delay (R2) and width control (R3) for the P-Channel switch (Q4) are obtained with Gates B1, B2, B3 and B4 which drives two cascaded bipolar transistors Q1, Q2 and power FET Q3.

Transistor Q9 drives power FET Q10 as an optional clamp to turn-off Q8 rapidly by discharging gate capacitance through a low impedance path. Duration of the clamp interval is dictated by the RC differentiating circuit in the base of Q9.

The complementary output FETs Q4 and Q8 consist of four P-Channel (MTP8P10's) in parallel and four N-Channel (MTP20N10's) in parallel. A limiting resistor R_D is shown in the drain of Q8 but may be in the drain of Q4 or in both drains. The external load may be a test rectifier

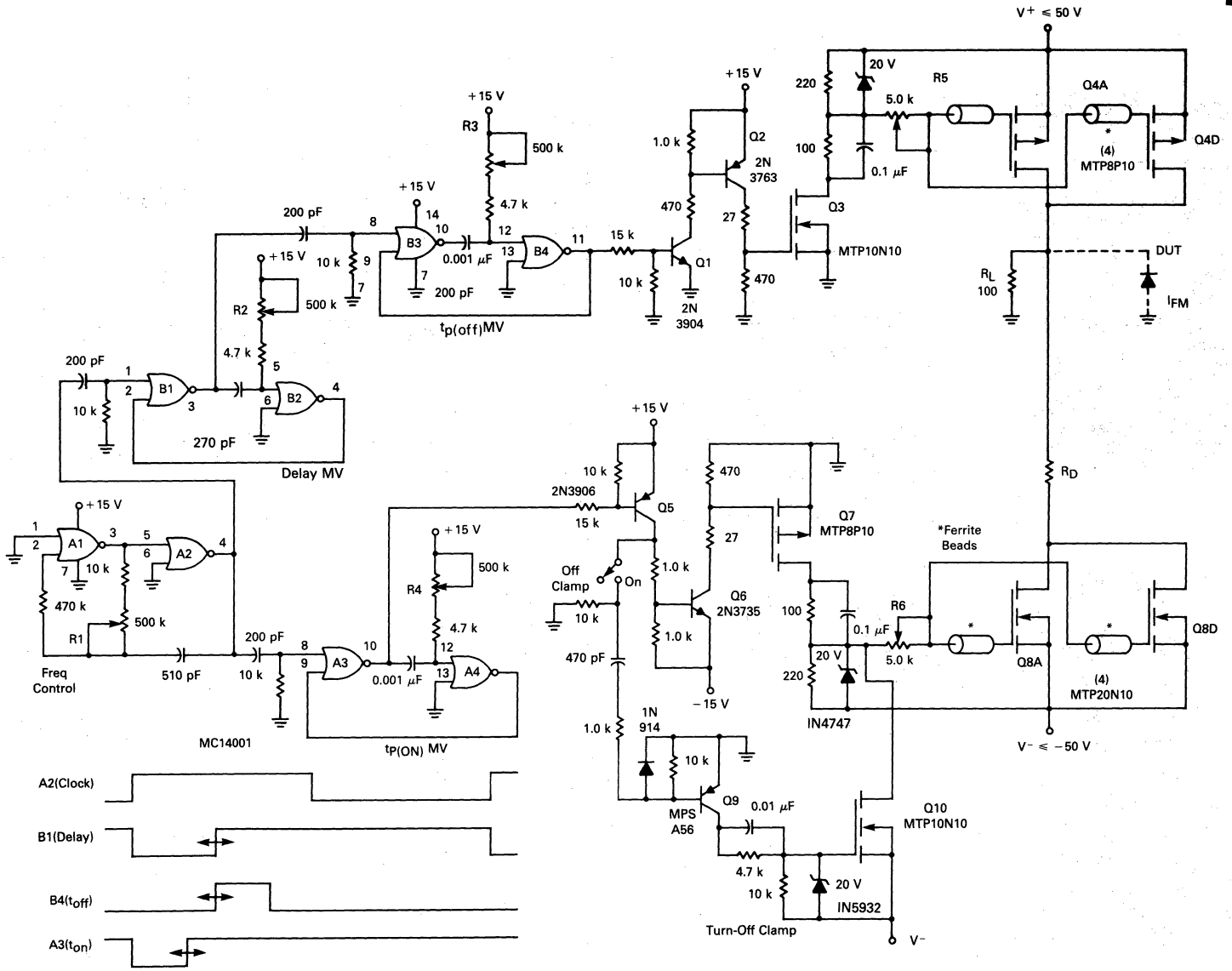


FIGURE 6-42 — FAST, COMPLEMENTARY POWER FET SWITCH

or any other load requiring the unique drive characteristics of this tester: fast, adjustable, complementary waveforms. The negative output switch Q8 (N-Channel) is capable of switching at least 100 A, whereas the positive switch Q4 (P-Channel) is limited to about 50 A due to the differences in the respective on-resistances. Additional devices can be paralleled for either switch for higher currents, if so required. Also, power FETs with higher V_{DSS} ratings may be used.

Output Waveforms

The negative and positive switched output waveforms are shown in Figures 6-43a and 6-43b, with the positive voltage delayed about 2.0 μs, in Figure 6-43a. The external load resistor R_L is about 2.0 ohms, with the switched voltages of about $\pm$ 42 volts.

In Figure 6-43a, the switched negative and positive voltages have very fast leading edges (about 10 ns) and slow trailing edges (about 3.0 μs and 1.0 μs, respectively). Figure 6-43b shows the same switched voltages but with the clamp transistor (Q10) switched on. This discharges Q8 gates through a low impedance path and speeds up the trailing edge of the negative voltage to about 25 ns instead of 3.0 μs.

In Figure 6-45, a MR821 fast recovery rectifier is shown as the load, with I_{FM} = 40 A, di/dt = 300 A/μs, and the dv/dt of the applied blocking voltage about 2500 V/μs.

Adjustment of dv/dt is accomplished with R5 for the positive switched voltage and with R6 for the negative voltage.

Figure 6-44 shows the transition time of about 35 ns between the negative and positive voltages, with both the clamp on and with Q4 diverting current from Q8.

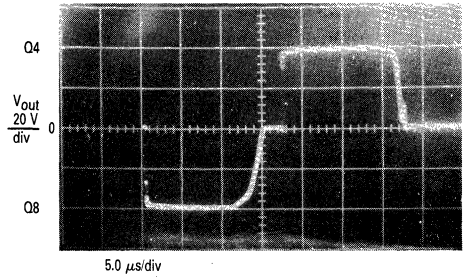


FIGURE 6-43a — FAST LEADING EDGE

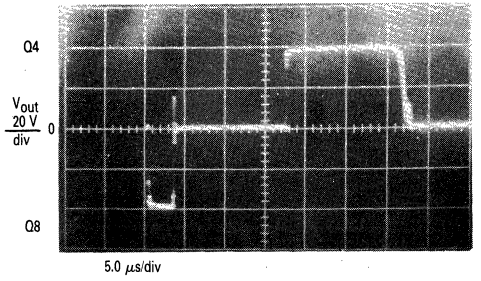


FIGURE 6-43b — FAST TRAILING EDGE, NEG. VOLTAGE, TURN-OFF CLAMP Q10 "ON"

FIGURE 6-43 — NEGATIVE AND POSITIVE SWITCHED OUTPUT VOLTAGE WITH R_L = 2.0 Ω, V^- AND $V^+ \approx$ 42 V, DRAIN Q8

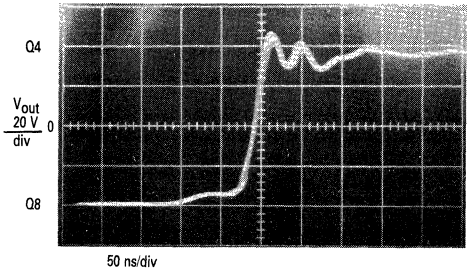


FIGURE 6-44 — NEGATIVE AND POSITIVE TRANSITION, DRAIN Q8, TURN-OFF CLAMP Q10 "ON"

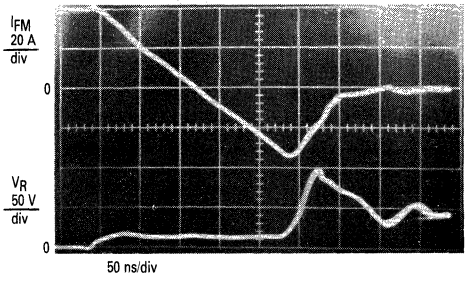


FIGURE 6-45 — REVERSE RECOVERY (t_{rr}) OF MR821 FAST RECOVERY RECTIFIER

Chapter 7: TMOS Applications

100 kHz Switcher

Power FETs have proven themselves to be performance competitive and cost effective in flyback regulators operating at 100 kHz to 200 kHz.

The circuit described here proves the point. It is a 60 W 100 kHz FET switcher with four output voltages ± 5.0 V and ± 12 V. It operates from 120 Vac, has an efficiency of 75% and the total parts cost is approximately $35.

Components unique to this high frequency design include the following:

- Motorola's MTP5N40 power FET. This 5.0 A, 400 V device has only one ohm of on-resistance and is driven directly from a linear IC. It not only switches in less than 50 ns but has enough RBSOA to eliminate the need for snubbers.
- Pulse Engineering's PE63133 power transformer. This is a continuous mode flyback transformer which is ideally suited to high frequency operation. Zener clamps are not required because the clamp winding is interleaved with primary halves. Regulation of the auxillary outputs is within ± 10% under varying conditions of line and load.
- Motorola's MC34060 Switchmode control IC, 4N27 optocoupler, and MC1723 linear regulator. These devices are used in a practical demonstration of a low-cost, three-chip control system. The MC1723 is the error amplifier, the MC34060 is a fixed frequency PWM, and the 4N27 couples the feedback signal from the MC1723 to the MC34060.
- Motorola's MBR1035 (TO-220) Schottky rectifier was used to rectify the +5.0 V output at half the cost of a comparable DO-4. Similar cost savings result from using the TO-220 fast recovery rectifiers, i.e., the MUR805 in the ± 12 V outputs.
- Mepco/Electra's 3428 series of output capacitors. These high frequency electrolytics feature low ESR and high RMS current ratings. Only 50 to 70 mV (PP) of ripple occurs at the outputs. Power loss is less than 0.5 W.

Circuit Design

The goal of most low-power flyback designs is for reduced parts count (or size) and reduced cost. The 60 W 100 kHz switcher shown schematically in Figure 7-1, met these requirements. At 100 kHz, the transformer size and cost are reduced by about 30% compared with a 20 kHz design. Also, at 100 kHz, a FET can be driven directly from logic circuits (100 to 200 mA) and still switch very efficiently. This eliminates the need for drive interface circuits. The output caps used are about 50% smaller and they cost less as well. Finally, a relatively new three-chip control system is used. It replaces an expensive and performance limited drive transformer with a lower-cost optocoupler.

The FET is the control element for the flyback transformer and is directly driven from the MC34060 linear IC. A rather standard off line starter circuit is used to initially power the control circuit and this is also lower in cost than the filament transformer supply which is often used to power a single-chip system. The design procedure followed here was:

1. Design and test the power stage.
2. Add and stabilize the control loop.
3. Change from dc to ac power.

The FET waveforms obtained with the design are shown in Figure 7-2. The exceptional switching speed of the FET can be varified here (less than 50 ns) and ringing on the current waveform is due to the layout which includes a current-sense loop and noise pickup on the scope probe.

The input capacitor does not reduce in size like the outputs because it is needed for energy storage which still occurs at 60 Hz. Noise filters used here include a toroid from PE and the economical 41GS series of tan-

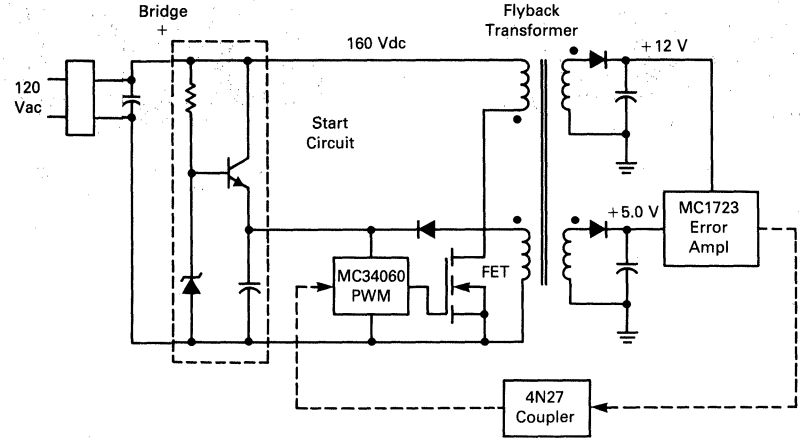


FIGURE 7-1 — REGULATOR BLOCK DIAGRAM

talum capacitor from M/E. The 12 V output rectifiers were Motorola's MUR805 ultrafast recovery button rectifiers which are housed in a TO-220 package. They were ideally suited to this relatively high current (10–15 A peak) application because the correct amount of heat sinking was easily attained by simply bolting a fin to the tab.

The relatively new MBR1035 TO-220 Schottky rectifier is the best choice for rectifying the 5.0 V output. It is about half the cost of the equivalent DO-4 version, a 1N6095.

The overall efficiency of this regulator (including the control circuits) is 75%. As usual, most of the losses are associated with the power handling components as noted in Table 1.

TABLE 1 — Efficiency Data

1. Input Power				
V_{In}	I_{In}	P_{PRMS}	P_A	P_F
160 Vdc	0.6 A	96	96	100%
120 Vac	1.4 A	170	95*	56%
*Note using Clark-Hess wattmeter.				
2. Output Power				
Winding	5.0	−5.0	+12.0	−12.0
Load (ohms)	1.0	10.0	8.0	8.0
Voltage	5.1	5.1	13.2	13.3
Power	2.5	2.6	21.5	22.0
3. Efficiency				
Eff. = P_O/P_{in} = 72 W/95 W = 75%				
4. Estimated Losses				
FET	4.0 W	Fast Recovery (both)		8.0 W
Schottky	4.0 W	Misc.		5.0 W
Transformer	2.0 W			

The control loop contains three chips as noted earlier. The functional diagram of this arrangement is shown in Figure 7-3. The first chip is an MC1723 linear regulator. It is used here to provide a 5.0 V reference and an error amplifier. It is powered from the +12 V output winding and receives feedback or control signal from the +5.0 V output. The MC1723 drives the second chip, a 4N27 optocoupler. The coupler maintains isolation between the primary and secondary windings and couples the dc control signal to the input of the third chip, a MC34060. The MC34060 performs a fixed frequency pulse width modulator (PWM) function and is used to directly drive the FET power switch which is connected to the primary or energy storage winding.

The key regulating blocks are the 0 to 3.0 V sawtooth oscillator and the feedback comparator. As the feedback signal is raised from 0 to 3.0 V, it gradually narrows the on time of output pulse coming from the comparator. During start up, the feedback is missing and resistor divider network controls the second or dead-time comparator to ensure that on time cannot exceed 45%. This, and the soft start capacitor, prevents transformer saturation problems during start-up. Pull down of the gate voltage is accomplished as shown in Figure 7-3 with the addition of a low cost TO-92 PNP transistor (Q3). In this design, the MC34060 is started off line with the addition of a 200 V transistor (Q2) and 12 V zener as shown in Figure 7-4. It ultimately (at normal line voltage) runs off the 12 V auxiliary winding which back biases this transistor. Because it and the FET gate draw so little current from the line, about 20 mA, undervoltage inhibiting common to bipolar designs was not required here and this current becomes functional and runs safely when the input reaches 40 Vac.

The performance of this 100 kHz switcher is similar to most others. It is relatively easy to keep output ripple, both

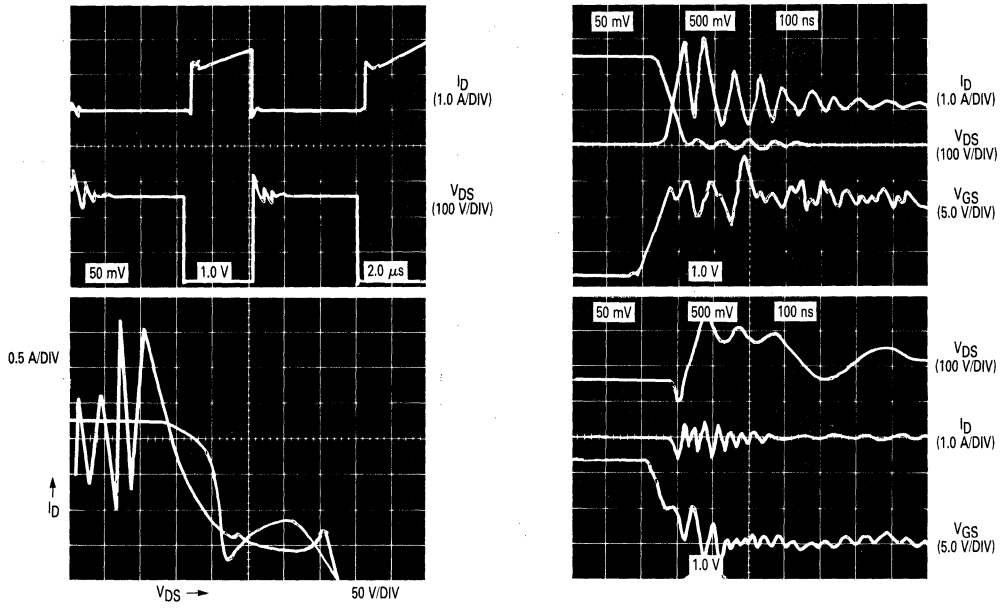


FIGURE 7-2 — FET WAVEFORMS — 120 Vac, FULL LOAD

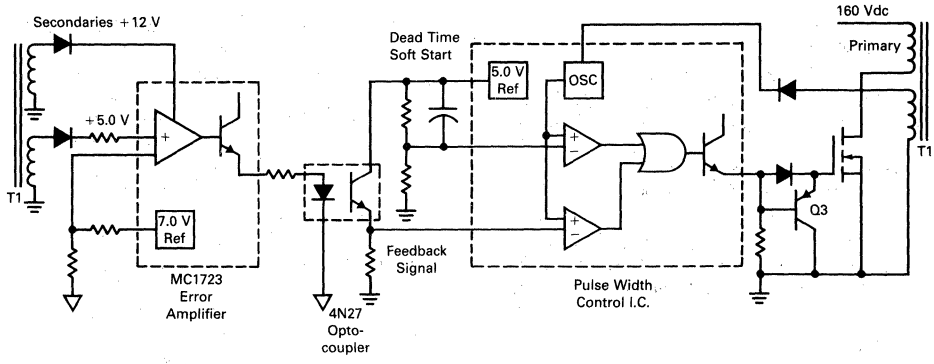


FIGURE 7-3 — THREE CHIP CONTROL SYSTEM

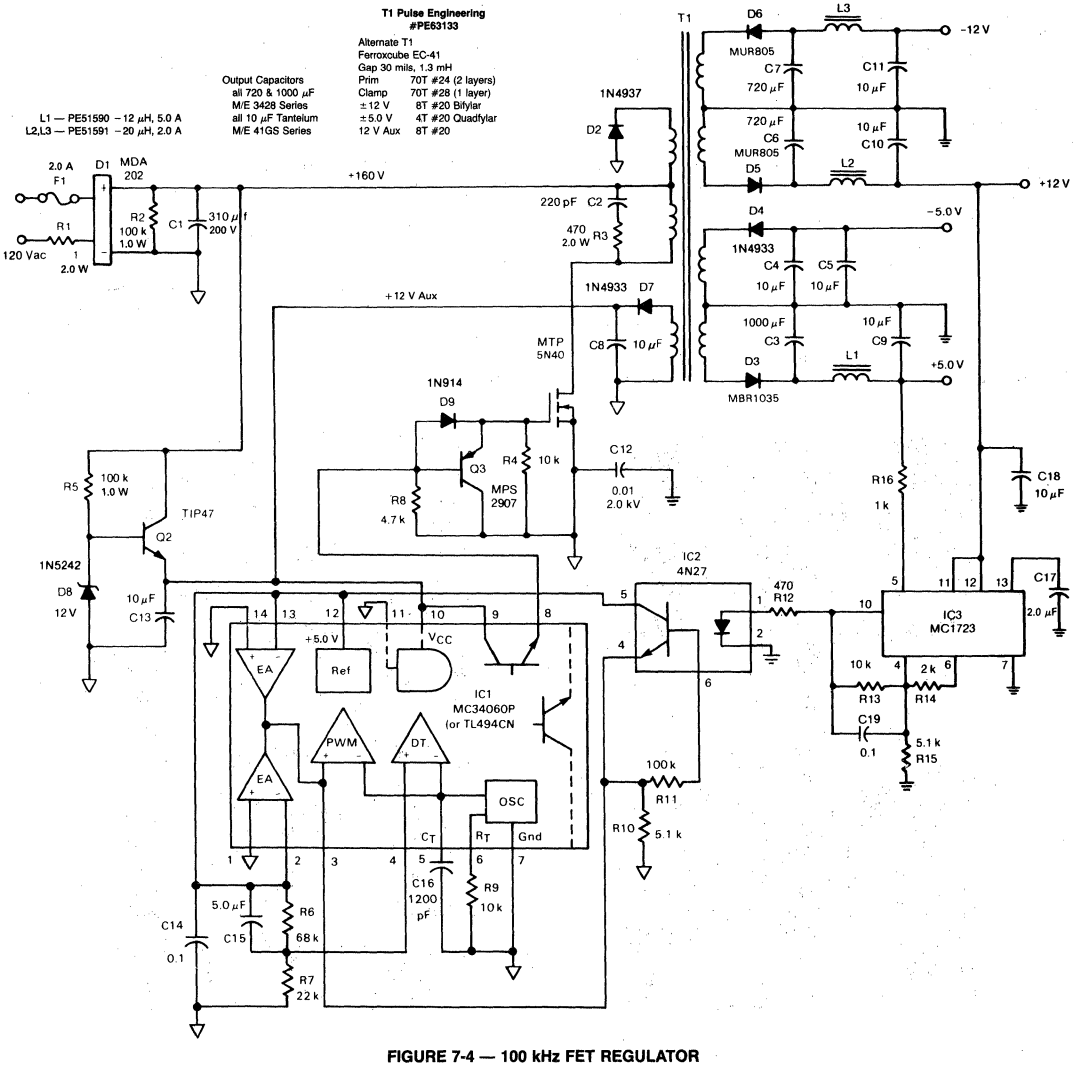


FIGURE 7-4 — 100 kHz FET REGULATOR

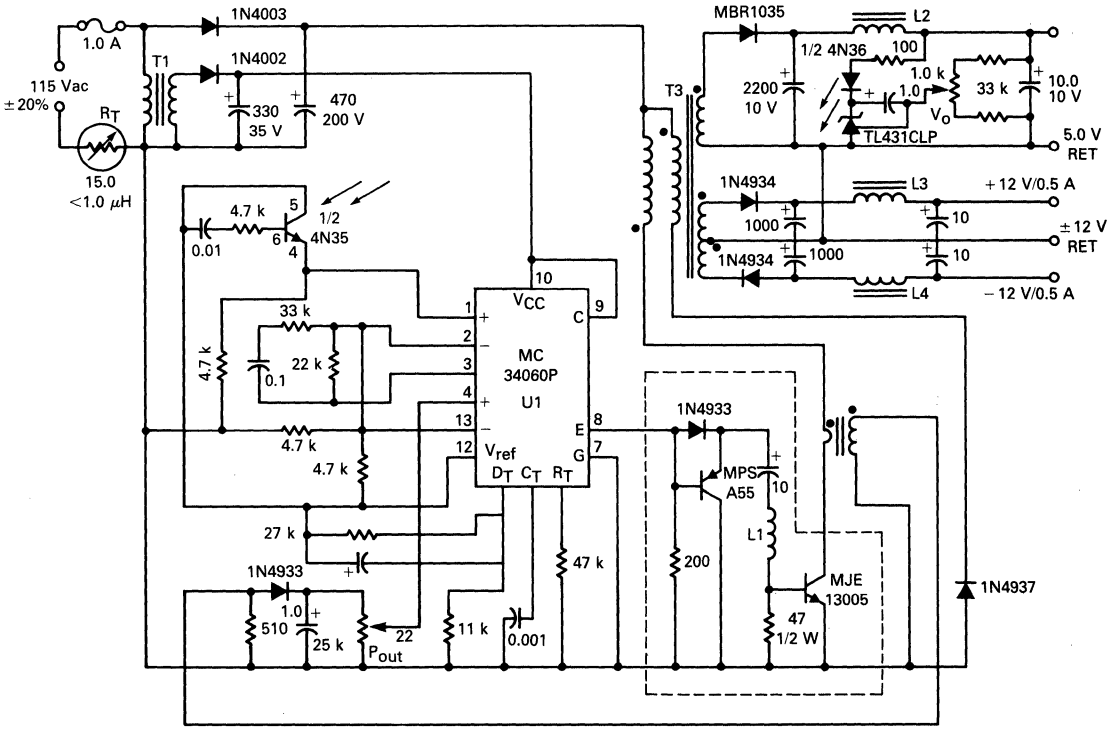


FIGURE 7-5 — 20 kHz SWITCHING POWER SUPPLY USING A BIPOLAR SWITCH

Unless otherwise noted:
All resistors are 1/2 W
All capacitors rated 25 V

Transformer Data

T1: Internal power supply transformer for switching regulator
TRAID F90X Primary — Black-red and black green. Secondary — Blue and green

T2: Collector current sense transformer Coilcraft D1870
Core: Ferroxcube 768T183-3C8
Windings: Primary — 1 turn, #26 Awg. lead from primary of T3 looped through center of T2, note dots.
Secondary — 100 turns, #28 Awg.

T3: High frequency output transformer
Core: Coilcraft 11-464-16, 0.025 gap in each leg.
Bobbin: Coilcraft 37-573
Windings: Primary — 2 windings 75 turns each, #26 Awg, bifilar wound. One winding is connected to the MJE13005 and the second is connected to the 1N4937, note dots.
Secondary — 5.0 V, 6 turns, #16 Awg.
12 V, 14 turns, #22 Awg, bifilar wound.

L1: Base drive inductor
Core: None
Bobbin: Ferroxcube 1408F1D
Winding: 39 turns, #28 Awg., 10.5 μH

L2: 5.0 Volt output filter inductor
Coilcraft Z7156, 15 μH at 5.0 A

L3,L4: 12 V output filter inductors
Coilcraft Z7257, 25 μH at 1.0 A

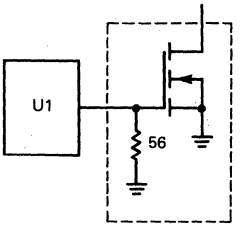


FIGURE 7-6 — POWER MOSFET VERSION

60 Hz and 100 kHz, below 100 mV on all outputs. (See Table 2.) Line regulation here was excellent, less than 0.1%, but load reg (2.0%) could have been better. Normally tight layouts and higher loop gain can get this down to 0.1 to 0.5% as well. Efficiency (75%) and cross regulation (±10%) are also similar to other multiple output switcher designs.

TABLE 2 — Output Data

1. Ripple Voltages (120 Vac, Full Load)				
Winding	+5.0	−5.0	+12	−12
100 k Ripple (PP)	60 mV	300 mV	70 mV	50 mV
60 Hz Ripple (PP)	20 mV	50 mV	70 mV	60 mV
Noise Spikes (PP)	2.0 V	2.0 V	2.0 V	2.0 V
2. +5.0 V Regulation				
Line	100 Vac	100 Vac	130 Vac	130 Vac
Load	Full	Half*	Full	Half
Voltage	5.10	5.21	5.10	5.21

*Note: +5.0 V Load increased to 2.0 ohms and −12 V load removed.
Load Reg. = $\Delta V_O/V_O$ = 0.11/5.1 = 2.2%.
Line Reg. $\Delta V_O/V_O$ = 0.005/5.1 = 1.0%.

20 kHz Switcher

A less novel 20 kHz flyback switcher provides a good illustration of the interchangeability of FETs and bipolar transistors. The 35 watt supply shown in Figure 7-5 was originally designed around the MJE13005 bipolar output transistor. With the bipolar, crossover time and case temperature rise were measured with V_{in} at 160 Vdc and outputs fully loaded.

A view of the crossover waveforms is shown in Figure 7-7. At the full load case temperature of 71°C, the MJE13005 is turning on in a crossover time of slightly under one microsecond, (46°C case temperature rise), providing a good relative measure of its efficiency as a switching element.

When an MTP4N50 FET is substituted for the bipolar transistor, the drive circuit is greatly simplified as illustrated in Figure 7-7. Now the MC34060 control circuit is capable of directly driving the FET, eliminating the complex base drive circuitry required for the bipolar. The end result is that the FET can be substituted for the bipolar by removing five components and changing one resistor value. Thus, the FET substitution results in a reduced components count.

Performance wise, the FET is the better choice, with a considerably improved crossover time, Figure 7-8, and a case temperature rise of only 18°C.

Automotive DC-DC Converter

In the previous example, FET drive circuitry was maximally simplified. The penalty for this simplification is that turn-on gate-source voltage, applied across a relatively low gate-source resistor, draws approximately as much drive power as a bipolar would. This example illustrates how the FET's low drive power requirements can be used advantageously. The circuit, shown in Figure 7-9, is a 25 watt DC-DC converter that is designed for automotive use. It uses the same control IC as the previous example. The significant difference is the addition of Q1, D3, & D6 to the drive loop. This arrangement provides a low impedance loop for fast turn-off, while drawing a negligible amount of current from the IC after the FET is turned-on.

The FET and this circuit work well together. Efficiency was measured at 78% with V_{in} at 13.6 volts, load regulation at 0.4%/Amp., and line regulation at 0.01%/volt. In general, the comparatively low $r_{DS(on)}$ of FETs with 100 V (or less) ratings makes the FET a particularly good choice for this type of application.

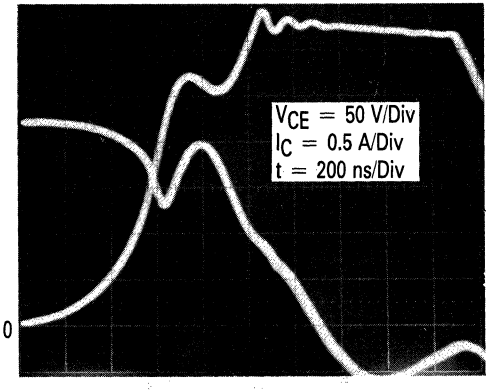


FIGURE 7-7 — BIPOLAR CROSSOVER TIME

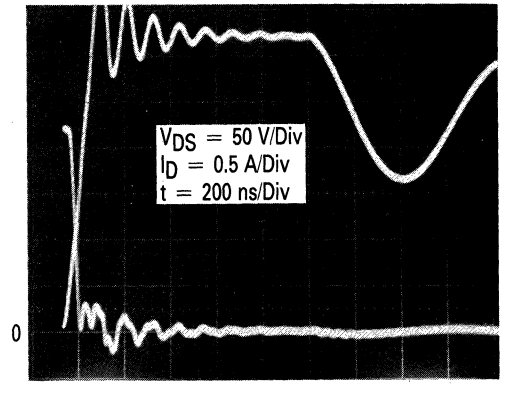
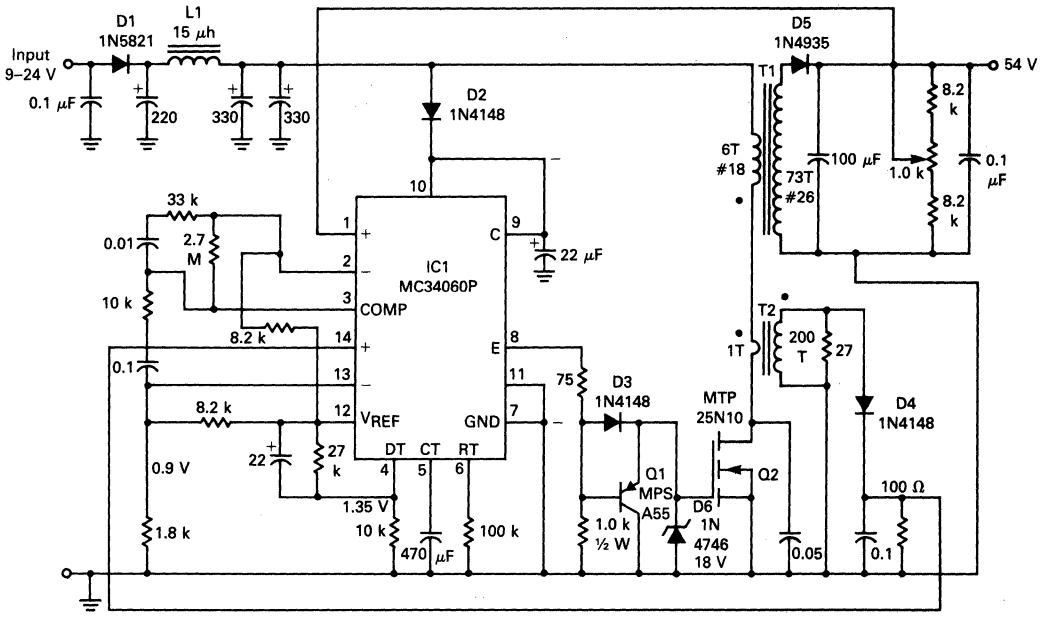


FIGURE 7-8 — FET CROSSOVER TIME



T1: CORE = FERROXCUBE 3019-L00-3C8
BOBBIN = FERROXCUBE 3019F-1D
GAP = 0.015″

T2: COILCRAFT D1871 CURRENT SENSE XFMR.

T3: CORE = COILCRAFT 11-464-41 EE-19
BOBBIN = COILCRAFT 37-612-001
GAP = 0.0075″

L1: COILCRAFT Z7156, 15 μH

L2: COILCRAFT Z7157, 25 μH

FIGURE 7-9 — AUTOMOTIVE DC-DC CONVERTER

MOSFET HV Flyback Converter

The advantages of power MOSFETs over bipolars — high input impedance (low drive power), fast switching, freedom from second breakdown — have been cited many times and can clearly be shown when the two technologies are used in the same application. Such is the case when a HV flyback converter, initially designed with a bipolar, was redesigned for the power MOSFET.

The first design used a Switchmode high-voltage bipolar MJ8505 output transistor in a PWM flyback converter, Figure 7-10c. This transistor has breakdown voltage ratings $V_{CEO(sus)}$ and V_{CEV} of 800 V and 1400 V, respectively, and a continuous collector current of 10 A. But, most important, it has a reverse bias safe operating area (RBSOA) curve, shown in Figure 7-11a, which allows a peak flyback voltage of about 700 V, generated by a peak collector current in the 3.0 to 4.0 A range.

To achieve this RBSOA capability an off-bias voltage, $V_{BE(off)}$, of about −5.0 V is required. Also, since there

is a trade-off of β with high-voltage transistors (β_{min} = 7.5 at I_C = 1.5 A), a low forced beta β_F of about 2.5 (I_{B1} ≈ 1.5 A) was chosen to ensure device saturation. To produce clean, monotonic, relatively fast clamped inductive turn-off waveforms, the Baker Clamp network of diodes (D2–D4) is suggested. Consequently, a power amplifier consisting of an I_{B1} forward base current circuit (transistors Q1 and Q2) and an off-bias circuit (transistors Q3 and Q4) is required to interface the low level PWM with the MJ8505. The PWM (U1), for this example, need only provide a +5.0 V pulse to the power Amp with about 20 mA sourcing and sinking capability.

If, however, the output device is a comparably rated power MOSFET, MTM2N90 the drive circuitry can be greatly simplified, with the resulting savings in cost and improved reliability. Moreover, the faster switching

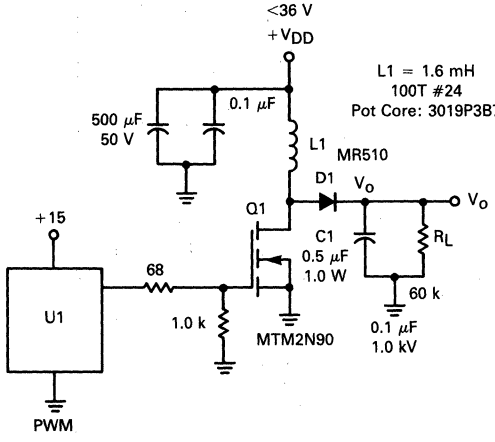


FIGURE 7-10a — SINGLE MOSFET OUTPUT

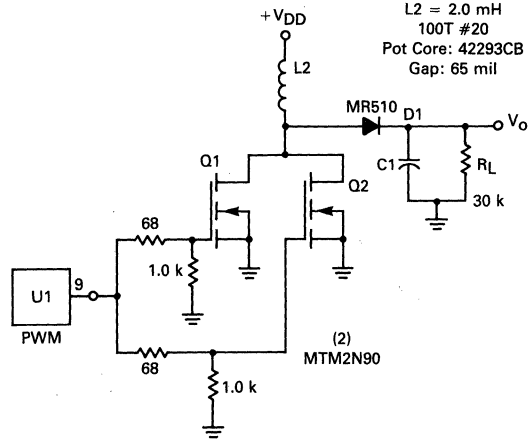


FIGURE 7-10b — TWO PARALLEL MOSFET OUTPUT

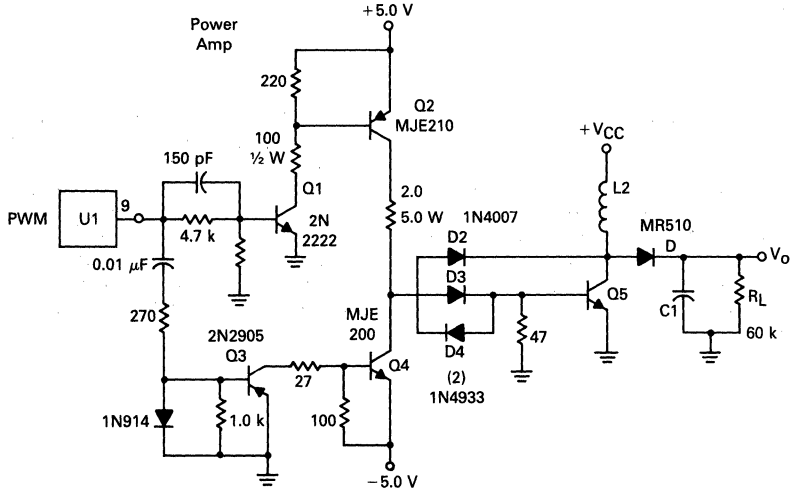


FIGURE 7-10c — DRIVER WITH BIPOLAR OUTPUT

FIGURE 7-10 — HIGH VOLTAGE FLYBACK CONVERTER WITH POWER MOSFET & BIPOLAR OUTPUTS

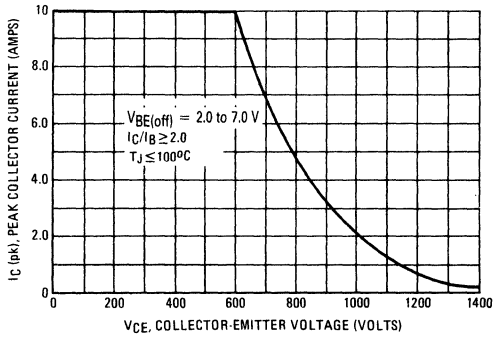


FIGURE 7-11a — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

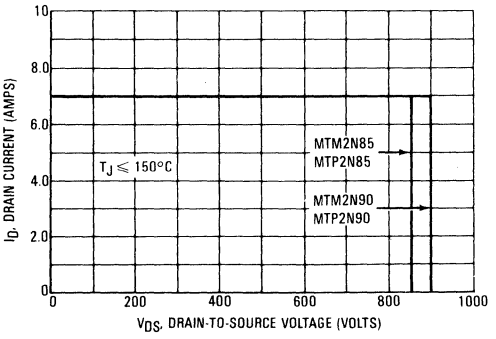


FIGURE 7-11b — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

MOSFET improves system efficiency and as subsequently described, greater RBSOA or turn-off switching SOA is achieved (see Figure 7-11 for comparison of the MTM2N90 with the MJ8505).

The PWM can be any of the 15 V powered I.C.'s with source and sink capability in the 100 mA range. This current level is amendable to driving power MOSFETs at a relatively fast switching speed, the current sourcing, charging up the FET input capacitance C_{iss} and the sinking, discharging the capacitance for fast turn-off switching. Also, the near 15 V PWM output ensures that the FET is well turned on.

This is exactly what was done for the second version of the high voltage Switchmode power supply; the PWM directly drives the FET gate. Using a single N-channel, high-voltage TMOS MTM2N90 transistor ($V_{BR(DSS)}$ = 900 V, I_D = 2.0 A), a high-voltage output of 750 V peak, capable of driving a 60 k load was achieved. With the illustrated load inductor L1 and switching frequency, the peak drain current was about 2.5 A (limited by the magnetic saturation of the inductor) and the flyback voltage was about 750 V.

Atlhough this current exceeds the continuous 2.0 A drain current rating of the device, it is well within the 7.0 A pulsed current rating. But, of even greater interest, since the FET has no second breakdown limitations — as do bipolars — it can sustain simultaneous high switching voltages and currents. Thus, the 750 V, 2.5 A load line is well within the SOA rating.

To produce even higher output power levels, two parallel connected power MOSFETs can be driven, as illustrated in Figure 7-10b. Using a larger inductor L2, the circuit was capable of easily producing an 800 V output into a 30 k load. The total peak drain current was 3.5 A with each driver sharing current inversely proportional to its $r_{DS(on)}$: i.e., matched on-resistance of 5.0 Ω produced about equal values of I_D of 1.75 A, unmatched 5.0 and 8.0 Ω, about 2.1 A and 1.4 A respectively. Reducing the load resistance even further, resulted in greater power output, with the individual device drain current being well within spec limits, as shown in Table 3:

TABLE 3

R_L	V_{DD}	V_O	Total $I_{D(pk)}$	P_O
30 k	28 V	800 V	3.6 A	21.3 W
25 k	31 V	800 V	3.8 A	25.6 W
21 k	34 V	800 V	4.2 A	30.5 W

And finally, to make a direct comparison between the two devices, the loads and the stored energy inductor should be the same. Since the bipolar originally was tested with the larger inductor and a 30 k load to produce as great as a 700 V output from a peak collector current of 3.2 A, the single TMOS was also tested to these conditions. Not only did the power MOSFET reach this energy level, it also reached 800 V at 3.6 A. To achieve the required inductor stored energy and power output for this application, the switching frequency was about 1.7 kHz. Even at this low frequency, the relatively high static losses [$V_{DS(on)} = r_{DS(on)}\ I_D$ = 8.0 Ω (max) (3.2 A) ≈ 25 V] contributed little to the total device loss.

Admittedly, power MOSFETs are still more expensive than a comparably die sized bipolar, but, as progression along the learning curve is achieved, the FET will become more cost competitive. Nevertheless, it has been shown that the single power FET circuit is much simpler and cost effective to drive in this example than the bipolar and offers the second breakdown free rectangular SOA curve that allows full $V_{BR(DSS)}$, I_D switching capabilities.

SWITCHMODE Power Supply (SMPS) Configurations

The implementation of switching power supplies by the non-specialist is becoming increasingly easy due to the availability of power devices and control ICs especially developed for this purpose by the semiconductor manufacturer.

This section is meant to help in the preliminary selection of the devices required for the implementation of the listed switching power supplies.

Flyback Switching Power Supplies: 50 W to 250 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: $\delta_{max} = -0.4$
- Maximum MOSFET working current:

$$I_W = \frac{2.0\ P_{out}}{\eta \cdot \delta_{max} \cdot \sqrt{in}(min) \cdot \sqrt{2.0}} = \frac{5.5\ P_{out}}{V_{in}}$$

- Maximum FET working voltage: $V_{DSW} = 2.0 \cdot V_{in(max)} \cdot \sqrt{2.0}$
- Minimum FET drain-source voltage: $V_{DS} \geq 1.2 \cdot V_{DSW}$
- Working frequency: f = 20 to 200 kHz

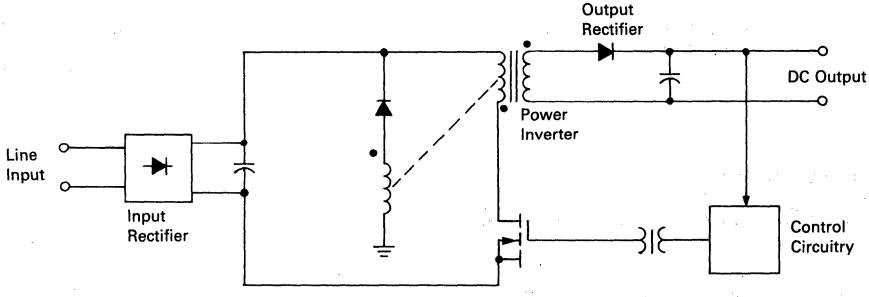


FIGURE 7-12 — BASIC FLYBACK CONFIGURATION

TABLE 4 — Flyback Semiconductor Selection Chart

Output Power	50 W		100 W		175 W		250 W
Input Line Voltage, V_{in}	120 V	220 V or 240 V	120 V	220 V or 240 V	120 V	220 V or 240 V	120 V
MOSFET Requirements							
Max Working Current, I_W	2.25 A	1.2 A	4.0 A	2.5 A	8.0 A	4.4 A	11.4 A
Max Working Voltage, V_{DSW}	380 V	750 V	380 V	750 V	380 V	750 V	380 V
Power MOSFETs Recommended							
Metal (TO-204AA) (TO-3)	MTM4N45	MTM2N90	MTM4N45	MTM2N90	MTM7N45	MTM4N90	MTM15N45
Plastic (TO-220AB)	MTP4N45	MTP2N90	MTP4N45	MTP2N90	—	—	—
Plastic (TO-218AC)	—	—	—	—	MTH7N45	—	—
Input Rectifiers							
Max Working Current, I_{DC}	0.4 A	0.25 A	0.4 A	0.5 A	2.35 A	1.25 A	4.6 A
Recommended Types	MDA104A	MDA106A	MDA206	MDA210	MDA970	MDA210	MDA3506
Output Rectifiers							
Recommended types for							
Output Voltage of: 5.0 V	MBR3035PT		MBR3035PT		MBR12035CT		MBR20035CT
10 V	MUR3010PT		MUR3010PT		MUR10010CT		MUR10010CT
20 V	MUR1615CT		MUR1615CT		MUR3015PT		MUR10015CT
50 V	MUR1615CT		MUR1615CT		MUR1615CT		MUR3015PT
100 V	MUR440, MUR840A		MUR840A		MUR840A		MUR840A
Recommended Control Circuits	SG1525A, SG1526, TL494; Inverter Control Circuit MC3423, MC3424; Overvoltage Detector Error Amplifier: SINGLE TL431; DUAL-MC3438, LM358; QUAD — MC3403, LM324, LM2902						

Push-Pull Switching Power Supplies: 100 W to 500 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: δ_{max} = 0.8
- Maximum MOSFET working current:

$$I_W = \frac{P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2.0}} = \frac{1.4\ P_{out}}{V_{in}}$$

- Maximum FET working voltage: $V_{DSW} = 2.0 \cdot V_{in(max)} \cdot \sqrt{2.0}$
- Minimum FET drain-source voltage: $V_{DS} \geq 1.2 \cdot V_{DSW}$
- Working frequency: f = 20 to 200 kHz

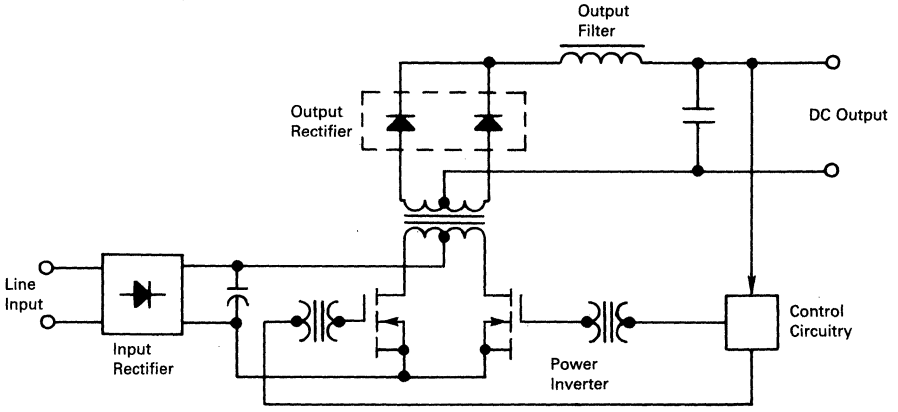


FIGURE 7-13 — BASIC PUSH-PULL CONFIGURATION

TABLE 5 — Push-Pull Semiconductor Selection Chart

Output Power	100 W		250 W		500 W	
Input Line Voltage, V_{in}	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements Max Working Current, I_W Max Working Voltage, V_{DSW}	 1.2 A 380 V	 0.6 A 750 V	 2.9 A 380 V	 1.6 A 750 V	 5.7 A 380 V	 3.1 A 750 V
Power MOSFETs Recommended Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM2N45 MTP2N45 —	 MTM2N90 MTP2N90 —	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N94 —	 MTM7N45 — MTH7N45	 MTM4N90 — —
Input Rectifiers Max Working Current, I_{DC} Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.35 A MDA970-5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltages of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	See Table 4					

Half-Bridge Switching Power Supplies: 100 W to 500 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: δ_{max} = 0.8
- Maximum MOSFET working current:

$$I_W = \frac{2.0\ P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2.0}} = \frac{2.8\ P_{out}}{V_{in}}$$

- Maximum FET working voltage: $V_{DSW} = V_{in(max)} \cdot \sqrt{2.0}$
- Minimum FET drain-source voltage: $V_{DS} \geq 1.2 \cdot V_{DSW}$
- Working frequency: f = 20 to 200 kHz

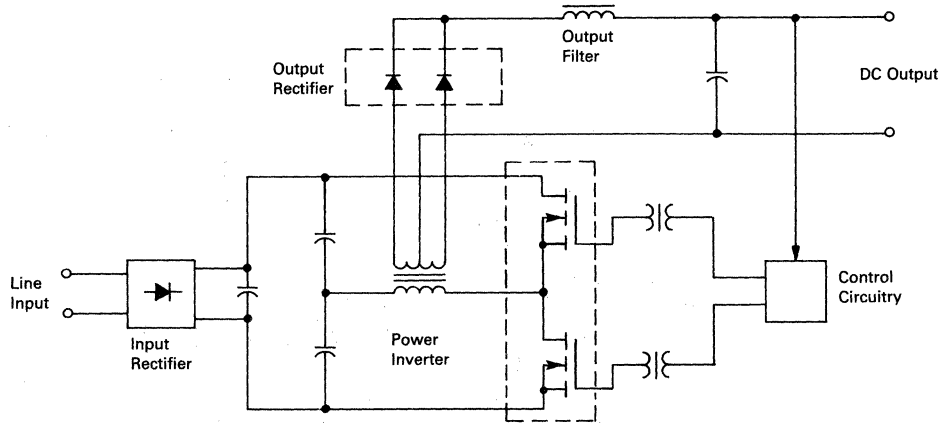


FIGURE 7-14 — BASIC HALF-BRIDGE CONFIGURATION

TABLE 6 — Half-Bridge Semiconductor Selection Chart

Output Power	100 W		350 W		500 W	
Input Voltage, V_{in}	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements Max Working Current, I_W Max Working Voltage, V_{DSW}	 2.3 A 190 V	 1.25 A 380 V	 5.7 A 190 V	 3.1 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM3N35 MTP3N35 —	 MTM2N45 MTP2N45 —	 MTM8N35 — MTH8N35	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 — MTH7N45
Input Rectifiers Max Working Current, I_{DC} Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.3 A MDA970-5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	See Table 4					

Full-Bridge Switching Power Supplies: 500 W to 1000 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: δ_{max} = 0.8
- Maximum MOSFET working current:

$$I_w = \frac{P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2.0}} = \frac{1.4\ P_{out}}{V_{in}}$$

- Maximum MOSFET working voltage: $V_{DSW} = V_{in(max)} \cdot \sqrt{2.0}$
- Minimum FET drain-source voltage: $V_{DS} \geq 1.2 \cdot V_{DSW}$
- Working frequency: f = 20 to 200 kHz

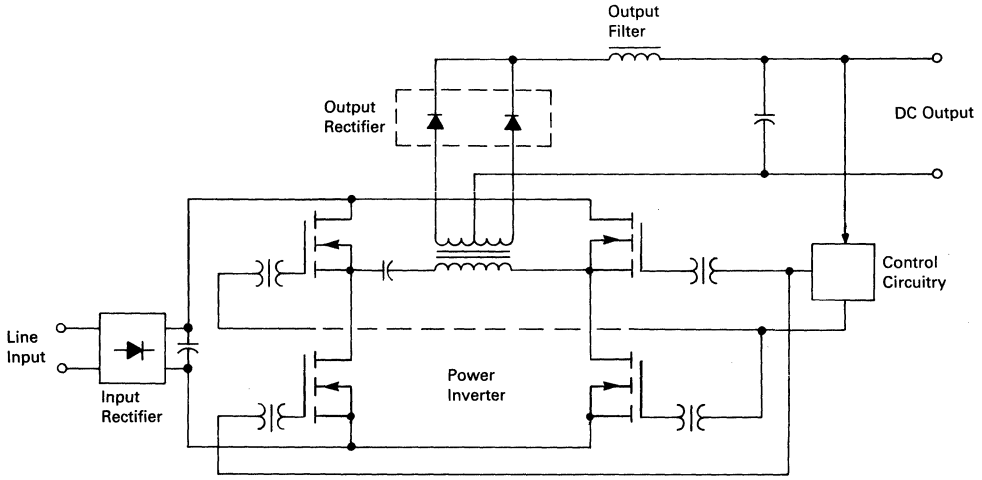


FIGURE 7-14 — BASIC FULL-BRIDGE CONFIGURATION

TABLE 7 — Full Bridge Semiconductor Selection Chart

Output Power	500 W		750 W		1000 W	
Input Voltage, V_{in}	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements Max Working Current, I_w Max Working Voltage, V_{DSW}	 5.7 A 190 V	 3.1 A 380 V	 8.6 A 190 V	 4.7 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM7N20 MTP7N20 —	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 MTP4N45 MTH7N45	 MTM12N20 MTP12N20 MTH15N20	 MTM7N45 — MTH7N45
Input Rectifiers Max Working Current, I_{DC} Recommended Types	 4.6 A MDA3506	 2.5 A MDA3510	 7.0 A	 3.8 A	 9.25 A	 5.0 A
Output Rectifiers: Recommended types for output voltages of: 5.0 V 10 V 20 V 50 V 100 V	 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR804PT		 MBR30035CT MUR10010CT* MUR10015CT MUR3015PT* MUR3040PT*		 MBR30035CT* MUR10010CT* MUR10015CT* MUR10015CT MUR3040PT	
Recommended Control Circuits	See Table 4					

*More than one device per leg, matched.

Motor Controls

Power MOSFETs are interesting devices for motor drive applications. The advantages and disadvantages are similar to those discussed for switching power supplies. With motor drives, however, there is more of a distinction. Whereas FETs are not yet a match for bipolar Darlingtons in off-line multiple horsepower drives, they are an excellent choice for fractional horsepower drives and drives that are operated off busses less than 100 V.

Three examples are illustrated. They include a stepping motor drive, a high efficiency H bridge, and a one-transistor PM motor speed control.

Using Power MOSFETs in Stepping Motor Control

Stepping motors are used extensively in electromechanical positioning systems. Applications range from printers to tape drivers, floppy disk drives, numerically controlled machinery and other digitally controlled positioning systems. The task of the stepping motor controller is to drive the rotation generating sequential current flows in the field winding of the motor on command from an external device.

The use of TMOS Power MOSFETs and CMOS logic simplifies the drive circuitry while allowing considerable flexibility of control. This section describes several types of stepping motor control circuits including an 88.0% efficient switching drive. Stepping motor logic sequencing, power requirements and dynamics are briefly examined.

DRIVE TECHNIQUES

Stepping Motor Characteristics

A basic understanding of stepping motors is desirable. A permanent magnet stepping motor consists of a series of permanent magnets distributed radially on a rotor shaft surrounded by electromagnets attached to the stationary housing. Energizing the electromagnets with the proper polarities generates a magnetic field pattern to which the motor magnets try to align producing torque. A simplified representation of a stepping motor is shown in Figure 7-16. Initially, Poles A and B are both energized with north up, drawing the rotor's south pole to the up position. Reversing the polarity of Pole A draws the rotor 90° clockwise to its final position; this is known as a full step. If pole A had been turned off instead of reversed, the rotor would have rotated only 45° clockwise to line up with the field created by Pole B; this is known as a half step. Stepping motors obtain small angle step increments by using large numbers of poles. Stator pole reversal can be accomplished by reversing the current flow direction in the winding or by using alternate halves of a center-tapped winding.

An external block diagram of a center-tapped stepping motor plus control switches, inductive clamp diodes, resistive current limiting and power supply is shown in Figure 7-17. Pole A, for instance, can be energized to one polarity by turning Switch 1 on and Switch 2 off; the opposite polarity is generated by turning Switch 1 off and Switch 2 on.

It follows that the proper magnetic polarity sequence for stepping can be generated by controlling Switches 1–4. Clamp diodes prevent the voltage across the inductive winding from flying up and destroying the switches as they are turned off. The required switching sequences for full and half step operation are shown in Figure 7-18. Reversing the sequences of Figure 7-18 will reverse the direction of motor rotation.

Rapid stepping requires high di/dt in the motor windings. Since di/dt is a function of supply voltage, a high supply voltage is desirable. The average winding current is limited by the motor manufacturer's specification. As an example, Superior Electric's SLO-SYN model M093-FC07 has a current rating of 3.5 amps/winding with 1.23 Ω/winding resistance and 7.94 mH/winding inductance. The recommended power supply is 24 volts; currents are limited to the maximum rating by a 6.5 Ω, 100 W resistor/winding. This yields a dc current of about 3.0 A and an L/R time constant of 1.0 ms. Higher supply voltages and

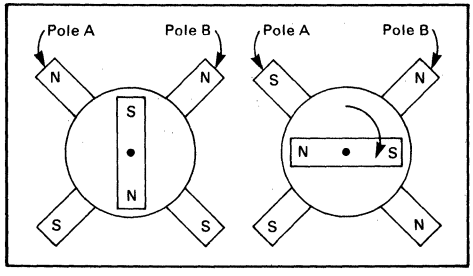


FIGURE 7-16 — SIMPLIFIED STEPPING MOTOR

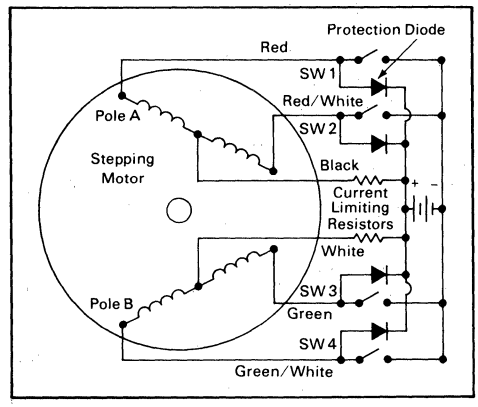


FIGURE 7-17 — SIMPLIFIED STEPPING MOTOR AND CONTROL BLOCK DIAGRAM*

*Colors are for Superior Electric SLO-SYN dc Stepping Motors

the resulting larger current limiting resistor will decrease L/R and increase the obtainable stepping rate.

Depending on rotor inertia, torque requirements and winding currents, a stepping motor may exhibit oscillatory behavior including vibration, lost steps and/or stalling near self-resonant stepping frequencies. Oscillatory behavior may be lessened or eliminated by adjusting winding currents, by adjusting interial and/or torque loading or by the use of mechanical dampers.

A Full Step Center-Tapped Drive

Figure 7-19 illustrates a full step center-tapped stepping motor controller using one CMOS 4-bit presettable shift register to drive four N-Channel TMOS Power FETs. Examining the full-step sequence of Figure 7-18, shows that the sequences for the various gate signals are the same except for a phase shift. Therefore, the desired control sequence of two on-time periods followed by two off-time periods may be preset into the 4-bit shift register (MC14194) of Figure 7-19. The required phasings are obtained by tapping the appropriate shift register outputs.

Clockwise stepping is obtained by right shifting the MC14194; left shifting yields counterclockwise stepping. Control signals S0 and S1 plus a clock line control stepping. On power-up, the MC14194 requires a preset obtained by setting S0, S1 = 1,1 and supplying a leading edge clock; this puts the logic in a known state. The remainder of the control functions are illustrated in the control table of Figure 7-19; stepping occurs in a leading edge clock. Diodes 1–4 prevent the inductive turn-off spike from avalanching the TMOS Power FETs. Resistor R3 creates a back voltage which halts winding current rapidly on turn-off. R3 is selected to limit the voltage spike to the TMOS S-D voltage rating. TMOS power FETs switch extremely fast, and the turn-on delay of the diodes may not be short enough to prevent S-D avalanche. A small capacitor (0.01 to 0.1 μF) placed across the motor winding will usually lower dv/dt sufficiently to prevent S-D avalanche. Resistors R1 and R2 limit motor winding currents.

A Full or Half Step Center-Tapped Drive

Figure 7-20 illustrates a full or half step controller. As in the full step sequence, the gate control signals for the half step sequence are identical except for a phase shift. Similarly, the desired pattern of three on-time periods followed by five off-time periods can be preset on a leading edge clock into an eight-bit shift register formed by two MC14194's. The full step sequence can be generated by setting the half step line high and performing a preset. Right shifting and left shifting control the motor shaft's direction of rotation as before. A full step will be executed for every two rising clock pulses independent of stepping sequence. Diodes D1–D4 and resistor R3 form the overvoltage protection for the TMOS Power FETs. R1 and R2 limit motor winding currents.

Push-Pull Drive

Figure 7-21 illustrates a complementary push-pull drive for a non-center tapped stepping motor driven from a 24 volt motor supply and a 15 volt logic supply. One of two winding drive sections plus the complete control logic is shown in Figure 7-21. The total drive consists of four N-Channel and four P-Channel TMOS Power FETs arranged in two push-pull drives per winding (the M093-FC07 center tap leads were floated, inductance/full winding = 31.76 μH, resistance/full winding = 2.46 Ω and rated current = 2.0 amps/winding).

Phasing signals are obtained with the shift register technique described earlier. The circuit of Figure 7-21 will provide a full or half step sequence as clocked into the two CMOS shift registers during a preset (a full step only controller can be implemented with one 4-bit CMOS shift register). Gate signals for the N-Channel FETs are taken directly from the CMOS registers. Gate signals for the P-Channel FETs are translated and referenced to the motor power rail through Q9–Q10.

Sufficient capacitance across the sources of the bridge FETs must be used to limit P-Channel gate-source voltage transients to below the pass frequency of the collector resistor and the P-Channel gate capacitance. During switching transients, it is possible that both FETs in a given complementary pair could briefly be on at once. This condition could short power to ground through the complementary pair. To avoid exceeding peak drain current rating, the gate-drive on the P-Channel FET is restricted to 10 V.

TMOS Power FETs are constructed with internal source-to-drain diodes. The circuit of Figure 7-21 uses these diodes to shunt turn-off transient currents from the ground plane to the power rail; thus, a given FET is protected from winding turn-off energy by the source-drain diode of its complement. The source-drain diode, how-

Full-Step Sequence

STEP	SW1	SW2	SW3	SW4
1	OFF	ON	OFF	ON
2	OFF	ON	ON	OFF
3	ON	OFF	ON	OFF
4	ON	OFF	OFF	ON
1	OFF	ON	OFF	ON

Half-Step Sequence

STEP	SW1	SW2	SW3	SW4
1	OFF	ON	OFF	ON
2	OFF	ON	OFF	OFF
3	OFF	ON	ON	OFF
4	OFF	OFF	ON	OFF
5	ON	OFF	ON	OFF
6	ON	OFF	OFF	OFF
7	ON	OFF	OFF	ON
8	OFF	OFF	OFF	ON
1	OFF	ON	OFF	ON

FIGURE 7-18 — STEPPING SEQUENCES**

**Clockwise Rotation as Viewed from the Nameplate End of the Motor

ever, requires about 300 ns of turn-on time. A 0.1 μF capacitor is placed across each winding so that the windings dv/dt is low enough to allow for diode turn-on without avalanching the FETs. Winding currents are limited by the 9.0 ohm 5.0 watt resistors.

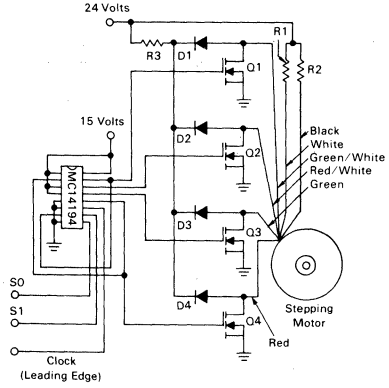
Switched Current Limiting

The circuit of Figure 7-21 uses resistive current limiting. With 2.0 amps flowing in each winding, 4.0 amps will be drawn off of the 24 volt supply yielding 96 watts of draw with only 25% of that power being delivered to the motor. Some form of switched current limiting is clearly desirable. Figure 7-22 illustrates a simple switching scheme.

Starting with zero current flow, let the desired current flow be left to right through the motor winding. Let the referenced voltage V_{ref} be 0.2 volts. Assuming $R_H >> R_{ref}$, the positive comparator inputs will be approximately 0.2 volts. With no current flow, the sense resistors will have no voltage across them and the comparators will have high outputs; this enables the C1 and C2 inputs to drive the P-Channel Power FETs. The proper C1, C2 input for left to right current flow is 1,0. This turns the upper left P-Channel and the lower right N-Channel on placing the full power supply across the motor winding. Current I1 increases with di/dt = V/L. When I1 increases to 2.0 amps, the voltage across the lower right 0.1 sensing resistor will be 0.2 volts, and the lower right comparator will go low after a short filter delay shutting off the upper left P-Channel FET. The current through the motor winding begins to decay around the I2 current path.

When the comparator went low, it shifted its positive input reference down by about 70 mV. I2 decays until the voltage across the 0.1 sense resistor falls below the hysteresis determined level; at that point, the comparator will go high turning on the upper left P-Channel FET and recharging the winding current along the I1 current path. The winding current within the C1, C2 control envelope increases to the reference level and oscillates around that level at a value set by RH, R_{ref} and the logic supply voltage. The frequency of oscillation is set by V/L, the hysteresis value and the current path resistances.

The circuit of Figure 7-22 places a negative voltage on



Control Signals

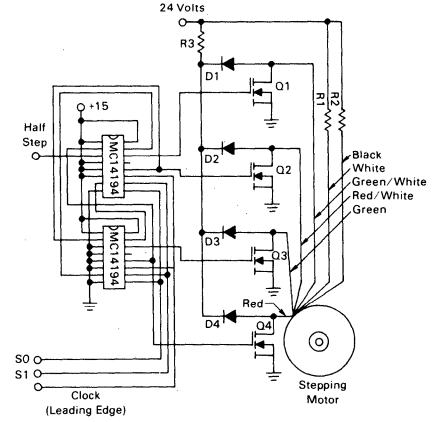
S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

Logic Levels are Standard
15 V, CMOS
MC14194 is a Standard 16 Pin DIP.

Parts:

1. Example Motor is M093-FC07 Manufactured By Superior Electric
2. Diodes, D1-D4, 1N4002
3. R3, 10 Ω 10 W
4. R1, R2, 6.5 Ω 100 W
5. Integrated Circuit, MC14194 (CMOS)
6. Q1-Q4, MTM12N08 or MTP12N08

FIGURE 7-19 — CENTER-TAPPED STEPPING MOTOR DRIVE



Control Signals

S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

PARTS:

1. Example Motor is Superior Electric's Model M093-FC07
2. Diodes, D1-D4, 1N4002 or Equivalent
3. R3, 10 Ω 10 W
4. R1, R2, 6.5 Ω 100 W
5. Integrated Circuits, MC14194 (2 Required)
6. Q1-Q4, MTM12N08 or MTP12N08

FIGURE 7-20 — HALF- OR FULL-STEP DRIVE FOR CENTER-TAPPED STEPPING MOTORS

the negative input terminal of the comparators during the I2 current path. This is not detrimental to the comparator provided that the terminal current doesn't exceed a few milliamps.

The complete logic circuit plus one of two required winding drive sections for a push-pull stepping motor with switched current limiting is shown in Figure 7-23. Figure 7-24 is the corresponding parts list for the complete circuit. The circuit of Figure 7-23 is limited to 8.0 amps continuous with a motor power supply voltage of about 70 volts by the specified P-Channel TMOS Power FETs. Thus, the controller can handle up to 560 watts delivered to each winding. Changes in RH, R_{ref} and the sensing resistor may be desirable for motors other than the example motor. For low inductance motors driven from high voltage supplies with low levels of hysteresis, faster components in the switched feedback loop may be required.

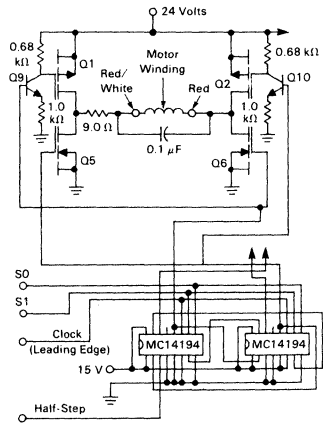
Utilizing Synchronous Rectification

The circuit of Figure 7-23 required 26.4 watts to maintain 2.0 amps/winding with 78.8% of the drawn power delivered to the M093-FC07. Calculations indicated that greater than 50.0% of the control circuit power consumption was due to the S-D diode drop during the I2 current loop (Figure 7-22). This drop could be lowered by operating the lower N-Channel Power FETs as synchronous rectifiers. The additional logic required for synchronous rectification amounts to three CMOS integrated circuits. A complete logic circuit plus one of the two required winding drive sections is shown in Figure 7-25. Essentially, the lower N-Channel is turned on when the upper complementary P-Channel is turned off by the comparator or when the N-Channel control signal is high. The circuit of Figure 7-25 yielded 88.4% efficiency at 2.0 amps/winding.

Further Possibilities

Shaping of the applied current waveform is often desirable. If a large stepping torque followed by a low holding torque is desired, the required current waveform can be applied to the positive comparator input. Within the comparator hysteresis and the circuit's current response speed, the current in the motor will follow the comparator reference. The di/dt circuit response is limited by approximately $V_{motor\ supply}/L_{motor}$, provided that the series resistance drops only a few percent of the supply voltage. If current is allowed to decay without applying a reverse supply voltage, current decay time will be set by the L_{motor}/R_{decay} loop time constant.

In summary, the switching circuit of Figure 7-23 yields 79.0% efficiency at 2.0 amps/winding with faster current response than the 25.0% efficient resistive current limited circuit of Figure 7-20. Adding three CMOS integrated circuits to the circuit of Figure 7-23 yields the 88.0% efficient circuit of Figure 7-25. The use of TMOS Power FETs and CMOS logic in the designs of Figures 7-23 and 7-25 allowed high efficiency and considerable control flexibility to be achieved without excessive parts count or undue complexity.



S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

Parts:

1. 2 × MC14194 (CMOS)
2. Q1–Q4, 4 × MTP8P08 or MTM8P08 (TMOS Power FETs)
3. Q5–Q8, 4 × MTP12N08 or MTM12N08 (TMOS Power FETs)
4. Q9–Q12, 4 × MPS8099 (NPN Small Signal)
5. 2 × 9 Ohm 50 Watt Resistors
6. 4 × 0.68 kΩ 1/4 W Resistors
7. 4 × 1.0 kΩ 1/4 W Resistors

Example Motor: Superior Electric SLO-SYN Model M093-F007

FIGURE 7-21 — HALF- OR FULL-STEP RESISTIVE CURRENT LIMITED DRIVE FOR STEPPING MOTORS WITHOUT CENTER-TAP

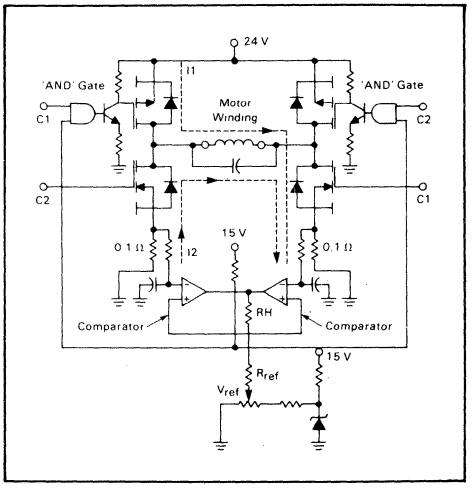
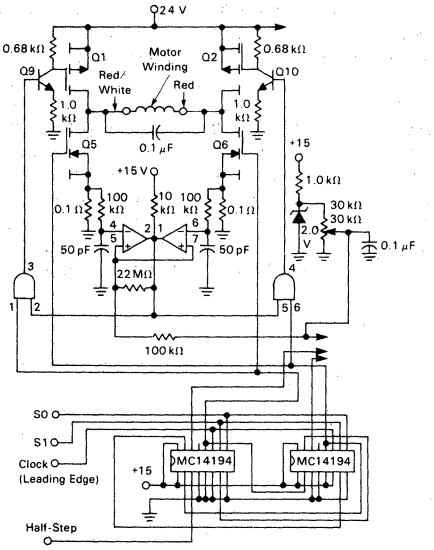


FIGURE 7-22 — COMPARATOR SWITCHED CURRENT LIMITING



S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

FIGURE 7-23 — HALF- OR FULL-STEP SWITCHED CURRENT DRIVE FOR STEPPING MOTORS WITHOUT CENTER-TAP

Integrated Circuits
1. 2 × MC14194B, CMOS 4-Bit Shift Register
2. 1 × MC14081B, CMOS Quad "AND" Gate
3. 1 × MLM399P, Quad Comparator

TMOS Power FETs
1. Q1–Q4, 4 × MTP8P08 or MTM8P08, P-Channel Power FET
2. Q5–Q8, 4 × MTP12N08 or MTM12N08, N-Channel Power FET

Transistors
1. Q9–Q12, 4 × MPS8099, NPN Small Signal Transistors

Resistors
1. 4 × 0.1 Ω 2.0 W
2. 4 × 680 Ω 1/4 W
3. 5 × 1.0 kΩ 1/4 W
4. 2 × 10 kΩ 1/4 W
5. 1 × 30 kΩ 1/4 W
6. 1 × 30 kΩ Adjustable, 1/4 W
7. 6 × 100 kΩ 1/4 W
8. 2 × 22 MΩ 1/8 W

Zener Diode
1. 1 × MZ4679, 2 V Reference

Capacitors
1. 3 × 0.1 μF 100 V
2. 4 × 50 pF 50 V

FIGURE 7-24 — PARTS LIST FOR CIRCUIT OF FIGURE 8

H. Bridge Performance Comparisons

Power MOSFETs are excellent candidates for low voltage H Bridges. In this example, MOSFETs are compared with two other popular alternatives, bipolar discretes and bipolar Darlingtons. Circuits were designed for all three types of output power devices. Each circuit design is optimized for the output device used.

GENERAL "H" SWITCH DESIGN CONSIDERATIONS:

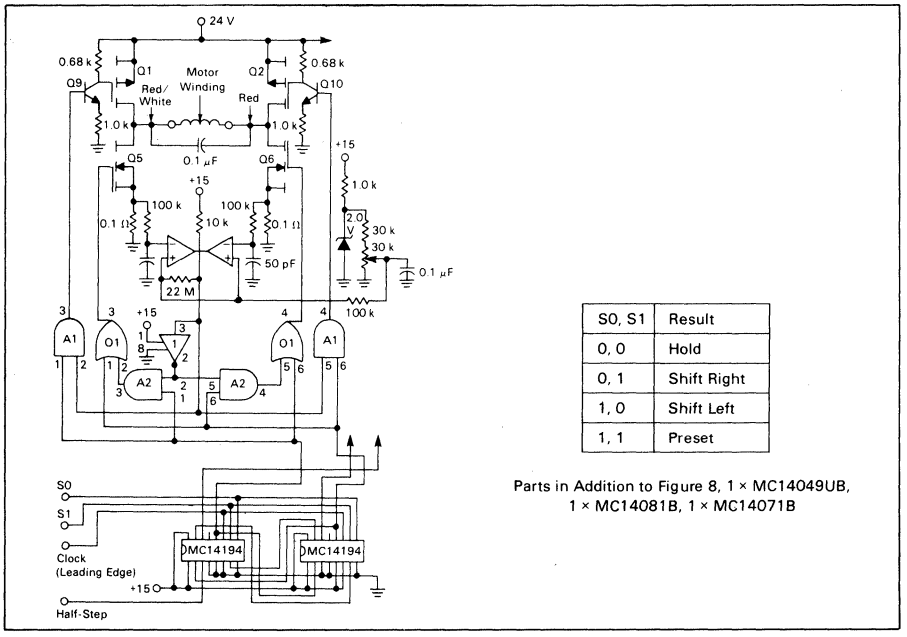
- P.M. DC Motor, 2.0 A run, 15 A stall/start.
- 12 V protected bus, 32 V max peak, 14 V nominal.
- "H" switch input, 2.0 mA max sink requirement.
- Discrete driver stages (for comparison of designs).
- Maximum ambient temperature of 100°C, maximum junction temperature = 150°C.
- Off the shelf type output power devices using maximum data sheet limits to calculate drive requirements and forward "on" voltage levels. The power output devices were chosen such that die sizes for the three types are approximately equal.

Discrete Bipolar "H" Switch

TIP35 and TIP36 power transistors were selected for their low cost and high current capacity. The high current-gain specification for these units results in base drive requirement of 1.5 amperes to switch a 15-ampere load current. It may be that base drive can be reduced by 30 percent if the units are screened for high-current h_{fe}, but for this design comparison, only "off-the-shelf" standard devices with the regular data-sheet specifications are under consideration.

The bipolar "H" switch design requires medium size driver transistors and large-wattage voltage-dropping resistors in the base-drive circuit. A buffer stage is also required. The control lines are shown tied to a SPDT center off switch. In an actual circuit, this switch would be a logic array or a microcontroller output network. A protective counter-EMF voltage clamp is provided by the back-to-back Zener rectifiers. The Darlington and TMOS units have built-in clamp diodes and for many applications would not require the zeners. Capacitor and resistor snubbing networks may be required with all three types output devices.

As indicated in the performance table, the bipolar design is not very practical because of the large base drive requirement. Of the three power devices, it is the least efficient by a wide margin. In most situations, FETs or Darlingtons are a better choice.



S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

Parts in Addition to Figure 8, 1 × MC14049UB, 1 × MC14081B, 1 × MC14071B

FIGURE 7-25 — HALF- OR FULL-STEP SWITCHED CURRENT DRIVE WITH SYNCHRONOUS RECTIFICATION

$V_{CE(sat)}$ = 1.8 V @ 15 A, I_B = 1.5 A
$V_{CE(sat)}$ = 0.4 V @ 2.0 A, I_B = 1.5 A
Base Drive P_D = 14 V x 1.5 A
= 21 W
MTR P_D = 10.4 V x 15 A
= 156 W
MTR P_D = 13.2 V x 2.0 A
= 26.4 W

$$EFF = \frac{156}{75 + 156}, 75 = SW\ P_D + Base\ Drive\ P_D$$
= 67.5% at stall condition

$$EFF = \frac{26.4}{22.6 + 26.4}$$
= 53.8% at nominal run condition

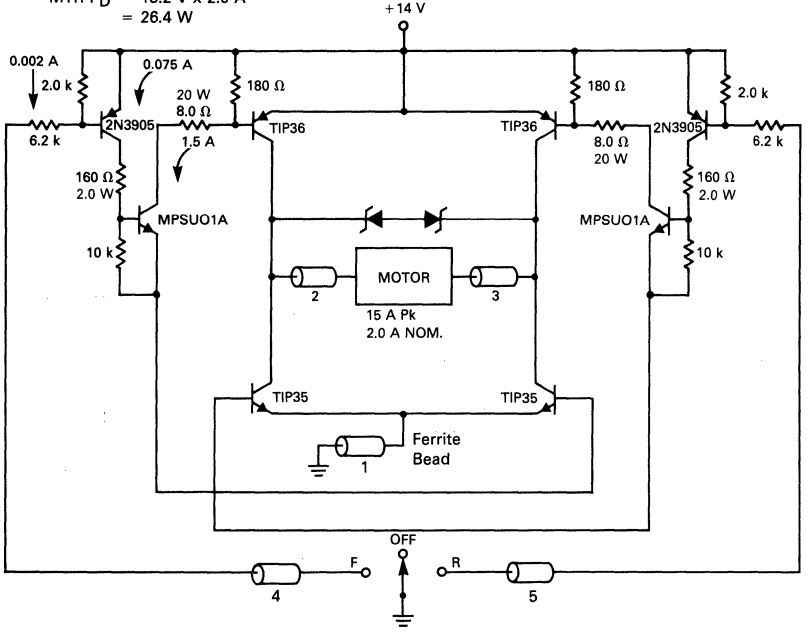


FIGURE 7-26 — "H" SWITCH BIPOLAR CONTROL CIRCUIT

Discrete Darlington "H" Switch

Motorola MJ4030 and MJ4033 power TO-204 (TO-3) Darlingtons were chosen for the Darlington version of the H bridge. As the chart shows, the drive-power requirements are substantially reduced from the bipolar power design. The tradeoff is that the forward "on" voltage is raised to such a high level that this particular motor will no longer be within its terminal voltage specification during stall or start-up. Also, the Darlington's dissipation will require a larger heat sink than the bipolar design. The Darlington does provide internal clamp diodes.

The Darlington "H" switch design works best in high-voltage, low-current load control circuits where the Darlington's high saturation power loss is not significant.

Power TMOS "H" Switch

An MTP25N05 Power FET was chosen for this design. Since the die size falls somewhat shy of the bipolar and Darlington device die sizes, an adjustment was made in the conduction loss calculation. Actual $V_{DS(on)}$ measurements were scaled according to the area ratio in order to arrive at the numbers presented here. As the comparison chart reveals, the TMOS design is clearly superior to the bipolar and Darlington designs. Its only technical drawback is the 34 volt bias supply requirement. This supply only has to source approximately 200 microamperes for this dc control, and can be derived from a single voltage pump-up circuit using TMOS gates and voltage doubling networks.

Test Measurement Calculations

The following equations were used to determine the circuit performance values for this example.

1. MOTOR POWER CONSUMPTION — The applied voltage across the motor load-terminals multiplied times the normal motor current.

   $P_{D(MTR)} = 1.0 \times (V_{BATT} - 2.0 \times V_{F(on)})$

   I = 2.0 AMPS RUN MODE I = 15 AMPS STALL MODE

   $V_{F(on)} = V_{CE(sat)}$ or V_{DS} per data sheet

2. OUTPUT DEVICE POWER DISSIPATION

   $P_{D(sw)} = (I \times V_{F(on)}) \times 2.0$

3. "H" SWITCH CONTROL EFFICIENCY

   $$EFF = \frac{\text{Power Out}}{\text{Power In}}$$

   Power Out = $P_{D(MTR)}$

   Power In = $P_{D(sw)} + P_{D(MTR)}$

$V_{CE(sat)}$ = 3.0 V @ 15 A, I_B = 0.08 A
$V_{CE(sat)}$ = 1.1 V @ 2.0 A, I_B = 0.08 A
Base Drive P_D = 1.12 W
MTR P_D = 8.0 V x 15 A
= 120 W
MTR P_D = 11.8 V x 2.0 A
= 23.6 W

$$EFF = \frac{120}{91.1 + 120} = 57\% \text{ stall mode}$$

$$EFF = \frac{23.6}{5.3 + 23.6} = 81\% \text{ run mode}$$

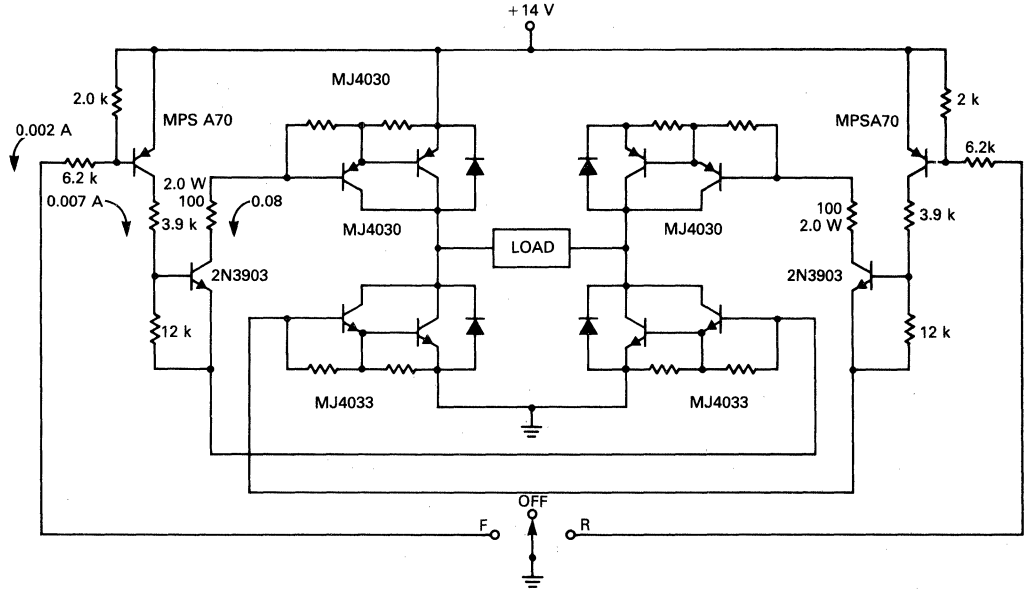


FIGURE 7-27 — "H" SWITCH DARLINGTON CIRCUIT

$V_{DS(on)}$ = 0.9 V @ 15 A, V_{GS} = 20 V
$V_{DS(on)}$ = 0.12 V @ 2.0 A, V_{GS} = 20 V
BIAS CIRCUIT P_D = 0.01 W MAX
MTR P_D = 12.2, 2.0 V × 15 A
= 183 W
MTR P_D = 13.76 V × 2.0 A
= 27.5 W

$$EFF = \frac{183}{27 + 183}$$
= 87% STALL MODE

$$EFF = \frac{27.5}{0.48 + 27.5}$$
= 98% RUN MODE

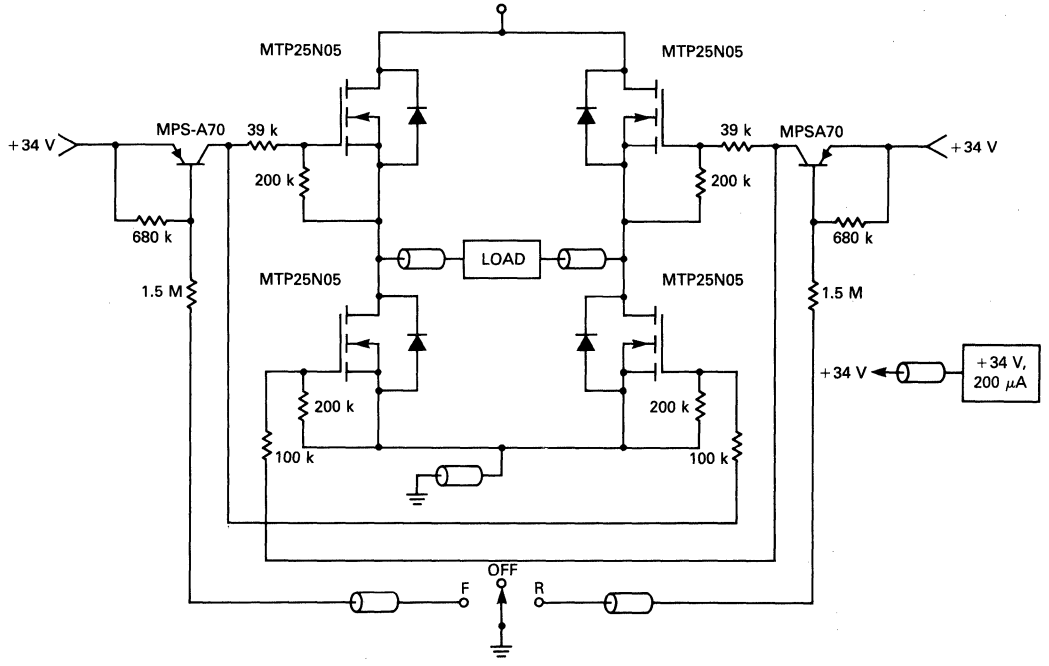


FIGURE 7-28 — "H" SWITCH POWER TMOS CIRCUITS

"H" SWITCH DESIGN COMPARISON CHART FOR AUTOMOTIVE MOTOR LOAD

	Die Size Area (Sq. Mils)	Max Forward Voltage (Off State)	Max Cont. Current	Forward Voltage Drop @ 2.0 Amp	Forward Voltage Drop @ 15 Amp	Driver Circuit Power Consumption	Switch Power Consumption @ 2.0 Amp	Switch Power Consumption @ 15 Amp	"H" Switch Total Efficiency @ 2.0 Amp	"H" Switch Total Efficiency @ 15 Amp	Motor Voltage @ 2.0 Amps with "H" Switch	Motor Voltage @ 15 Amps with "H" Switch	Comments
Bipolar	192	40 V	25 A	0.4 V	1.8 V	21 W	1.6 W	54 W	54%	68%	13.2 V	10.4 V	High base current required
Darlington	200	60 V	16 A	1.1 V	3.0 V	1.1 W	4.2 W	90 W	81%	57%	11.8 V	8.0 V.	Large forward voltage drop
TMOS	176	40 V	20 A	0.12 V	0.9 V	0.01 W	0.48 W	27 W	98%	87%	13.8 V	12.2 V	34 V 200 μA Bias supply required

NOTES:
1) Bipolar devices are TIP35 and TIP36 TO-218 plastic NPN and PNP
2) Darlington devices are MJ4030 and MJ4033 TO-204 (TO-3) metal NPN and PNP.
3) TMOS devices are MTP25N05.
4) Figures shown above are the worst case data sheet condition for the parameter calculated.

MOSFETs Improve Motor-Drive Efficiency

By using power MOSFETs in Figure 7-29b's circuit, fractional-horsepower motors can be driven bidirectionally with only a small percentage of the base-drive power that bipolars require. Moreover, by sensing the motor's back EMF and delaying drive-voltage reversal, the circuit reduces the peak currents encountered during motor reversal. This feature allows the use of lower current MOSFETs than an instantaneous-reversal method would dictate.

A basic H switch, Figure 7-29a reverses the motor's supply voltage for bidirectional control. In Figure 7-29b's circuit, two pairs of N-channel MOSFETs serve as the CW (clockwise) and CCW (counterclockwise) switches. A flyback-type dc/dc inverter, composed of a CMOS hex inverter and a small signal MOSFET, drives the FET switches. The 3-inverter oscillator operates at 240 kHz; the three remaining inverter's average output tracks the power-supply input, ensuring adequate gate-bias voltage even for input-supply voltages as low as 6.0 V.

The Darlington transistors sense the motor's counter EMF (via the 20 V snubber zeners that become forward biased when the motor's back EMF appears) and shunt the drive-reversal signal to ground until the back EMF decays. The transistors will hold the gate-drive line low until the counter EMF drops below the base-to-emitter threshold voltage. This action causes the circuit to wait until the motor nearly stops rotating before applying reverse voltage. If faster response times are needed, the Darlingtons can be eliminated while connecting the 1.0 MΩ base resistors to ground — this change, however, would necessitate higher current MOSFETs because of the large peak-reversal currents that would ensue.

Figure 7-30 shows the dramatic difference in the peak currents that occur with and without the back-EMF-sensing feature. With the sensing circuit disabled (a), the currents exceed 50 A; the resulting MOSFET dissipation is approximately 140 W. Enabling the circuit (b) reduces the currents to approximately 30 A and the MOSFETs' dissipation to about 14 W. A 16 V zener diode limits the

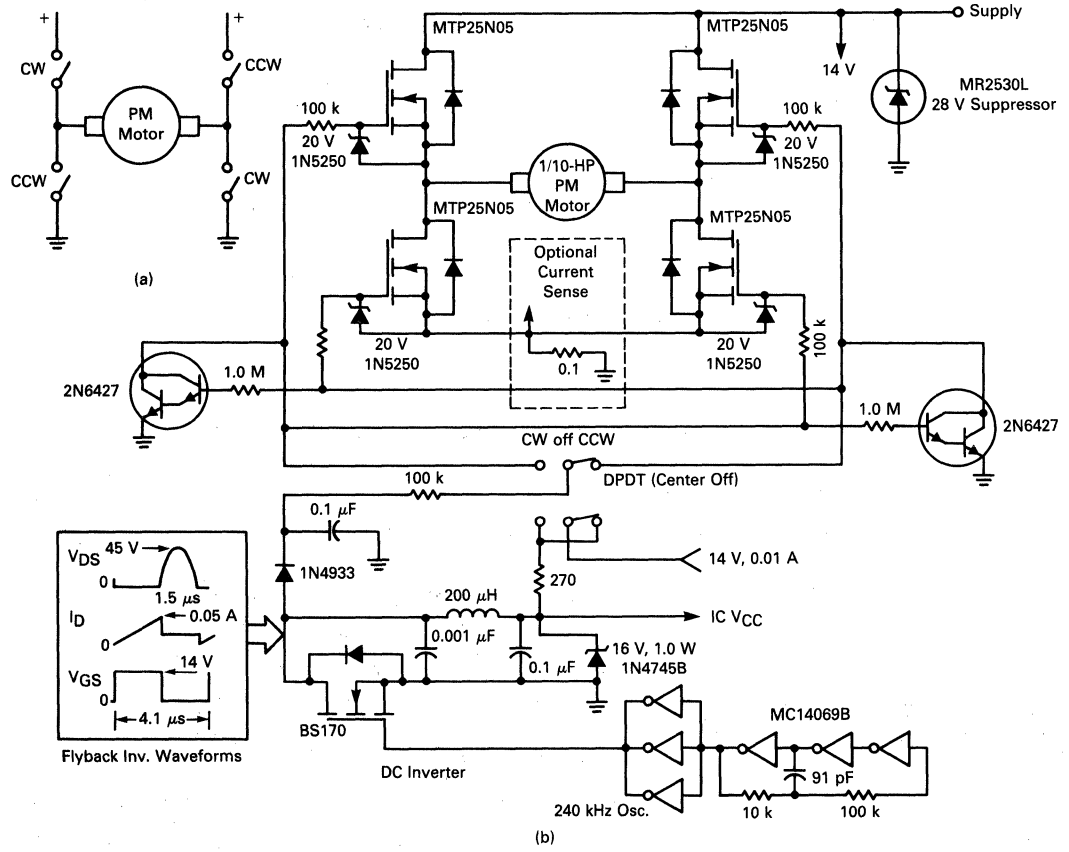


FIGURE 7-29 — DRIVE FRACTIONAL-HORSEPOWER MOTORS EFFICIENTLY WITH THIS POWER-MOSFET H-BRIDGE CIRCUIT. IT DISSIPATES MUCH LESS POWER THAN A BIPOLAR-TRANSISTOR DRIVER — MOREOVER, IT ALLOWS THE USE OF LOW-CURRENT MOSFETs BY DELAYING REVERSAL VOLTAGE UNTIL THE MOTOR COASTS TO A STOP.

input voltage to the flyback inverter in case the supply rises higher than 16 V; the transient suppressor protects the MOSFETs from supply spikes greater than 28 V.

In this design, the MOSFETs require heat sinking to keep their junction temperatures less than 150°C in worst-case conditions (that could occur, for example, with a 16 V supply, 100°C ambient temperature and a stalled motor). As an option, a current-sensing circuit can be added to gate-off the power FETs after detecting a stall condition.

PWM MOTOR Speed Control

FETs can be used to considerable advantage for simplifying permanent-magnet motor speed control. The circuit shown in Figure 7-31 provides efficient pulse-width modulated control with a minimum number of components. The key feature is direct drive of the power FET from a CMOS control IC. The result is a control system with minimized parts count.

The control system is based upon the MC14528B dual monostable multivibrator. One-half of the monostable is connected in an astable mode, producing a pulse oscillator. The remaining half is then used as a one-shot, with its adjustable pulse-width determining the duty cycle and, therefore, motor speed.

In addition to its simplicity, the circuit of Figure 7-31 is notable for its low standby power drain. The combination CMOS control and TMOS power gives a very low quiescent current drain that is desirable in battery operated applications.

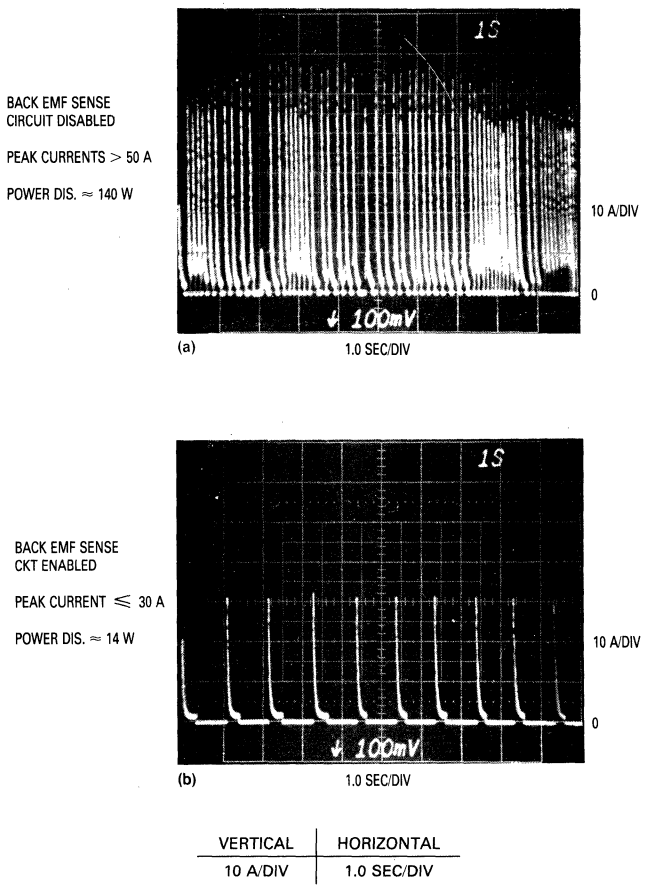


FIGURE 7-30 — COMPARISON OF "H" SWITCH PEAK CURRENTS DURING MAXIMUM FORWARD TO REVERSE SWITCHING WITH MANUAL TOGGLE SWITCH

Other Applications of Power MOSFETs

HORIZONTAL DEFLECTION CIRCUITS

Power MOSFETs can be a good alternative to bipolars in high resolution CRT sweep circuits. The most obvious advantage is simplicity. However, MOSFET horizontal outputs also offer significant benefits in terms of increased reliability and faster switching times.

Drive simplification with the MOSFET is even more significant than in the preceeding switching power supply examples. In most cases, a base-drive transformer is eliminated, as well as di/dt wave shaping networks.

The reliability issue is a little more complex, and relates to differences in SOA characteristics. It is normal design practice to exceed bipolar collector-emitter breakdown ratings during the retrace pulse transition. This is permissible if the base-emitter voltage is held negative during the retrace period. If, however, a positive noise pulse occurs during the retrace period, the bipolar base-emitter junction can become forward biased when collector-emitter voltage is greater than $V_{CEO(sus)}$. The bipolar's safe operating area is then violated, creating a substantial risk of failure. MOSFETs, on the other hand, will handle this type of stress quite readily, since their FBSOA capability extends beyond peak retrace voltage. Therefore, increased reliability with the MOSFET horizontal output is directly related to the probability of noise occurring in the drive circuitry.

Speed is also an important issue. At a 30 kHz scan rate, 1.0 μs of bipolar storage-time delay represents 3% of the horizontal line period, or a loss of 30 lines of data in a field of 1024 lines. In addition, bipolar storage time is not a fixed constant, but changes from device to device and with temperature. A horizontal phase locked loop can be added to compensate for the storage-time delays in the horizontal output stage. The active video data time may also be cut back, accordingly, to allow for internal horizontal timing delay.

Based upon these considerations, effective use of the bipolar transistor at high scan frequencies requires a complex base drive circuit, custom selection of the bipolar device for minimum storage-time variation, and an accurate phase locked loop to compensate for saturation time delays. Power MOSFETs, on the other hand, can be driven from a CMOS IC, do not require critical parameter screening, exhibit minimal turn-off delay, and do not require a phase locked loop for correcting device-induced timing errors.

Design Example

The power MOSFET, until recently, could not handle much current at voltages above 500 V. Recent technology developments have pushed this limit up to the 1000 V range with increased current ratings. Therefore, a power MOSFET can now be selected for computer CRT display systems with power supply requirements ranging from 12 V to 75 V.

The standard horizontal raster scan system is used in this design. That is, the horizontal yoke and flyback transformer are both switched by one output device. It should be pointed out that the power MOSFET has been switched up to 120 kHz scan rates, but due to other device constraints, the CRT anode high voltage network's performance is very marginal at this high frequency rate. Even a scan frequency of 30 kHz is pushing the limits of the high-voltage rectifier and associated components.

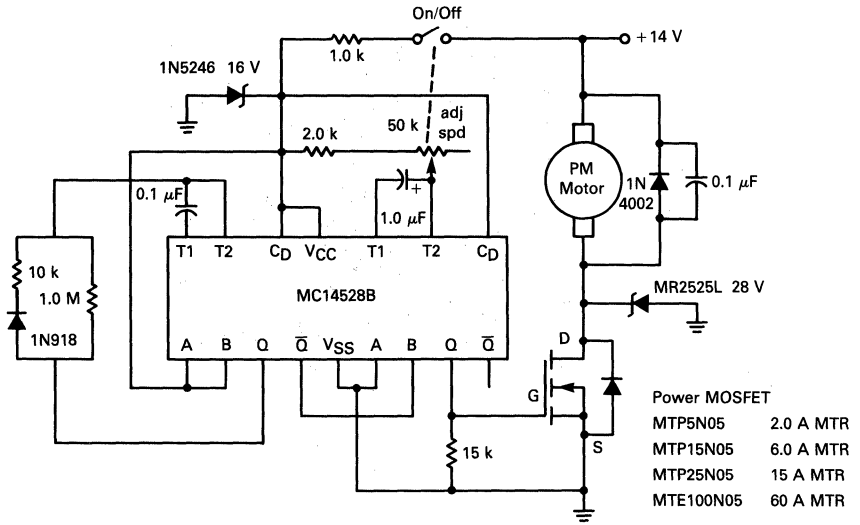


FIGURE 7-31 — POWER MOSFET MOTOR SPEED CONTROL CIRCUIT

The design concept is shown in the block diagram of Figure 7-32. The horizontal drive signal can be supplied by a free running synchronous clocked oscillator or by external computer logic. The safest method is to use a free running synchronous oscillator to insure the horizontal frequency is held within safe limits. There are several horizontal processor linear integrated circuits containing a phase detector, oscillator and predriver available. A partial list includes SGS TDA1180 and Motorola MC1391. None of these devices are presently designed to drive a MOSFET power unit directly; so some type of an interface or buffer circuit is required. Three power MOSFET drive circuits are shown in Figure 7-33. These circuits perform adequately in the horizontal system described here.

Circuit Description

The design presented in Figure 7-34 eliminates the driver transformer, driver transistor, and associated passive components that would normally be found in a bipolar design. A MLM311 comparator is used to invert and level-shift the incoming positive going synchronous pulse. The comparator output is ac coupled to the MC1391 horizontal processor which consists of a phase comparator and voltage controlled oscillator with adjustable duty cycle. The phase comparator of the MC1391 is connected to the incoming conditioned horizontal synchronous pulse and the output of the MC1391's internal oscillator. An error voltage is applied to the oscillator timing control voltage to lock in the external synchronous pulse and the oscillator. The duty cycle of the MC1391 oscillator output is set to provide a 63% "ON" time to the power MOSFET gate.

Essentially, the prime requirement for driving the power MOSFET for this horizontal scan output design is to insure sufficient gate on-voltage and low enough impedance for a fast turn-off transition. Since the power MOSFET has a high gate input impedance, the gate voltage requirement is easily met, with little wasted power. The off transition requires that the power MOSFET's internal 1000 pF gate capacitance be discharged very quickly. This is accomplished by using a single hex inverter IC, with all the gates wired in parallel. As mentioned before, other devices can be used to drive the MOSFET. The CMOS inverter was chosen to show that CMOS technology is sufficient to drive the MOSFET.

The system described above provides excellent performance. The gate-drive voltage of the power MOSFET was purposely pulsed during the peak retrace drain voltage pulse to simulate destructive transients due to anomalies such as arcing.

It was found that a controlled drain-to-source current occurred, with no catastrophic failures, as long as the total power dissipation was held within the limits of the power FET's safe operating area ratings. Figure 7-34 shows the waveforms associated with the retrace pulse test. Since the MOSFET is a high input impedance device, it is important to insure the gate of the power MOSFET is at a low impedance during the retrace period. The gate should not be driven negative, to minimize the possibility of voltage spikes causing gate avalanche. The gate cannot withstand an avalanche condition of any measurable current intensity and survive. Since the power MOSFET device selected for this design exhibits at least a 2.0 volt threshold, a negative gate-drive is not important.

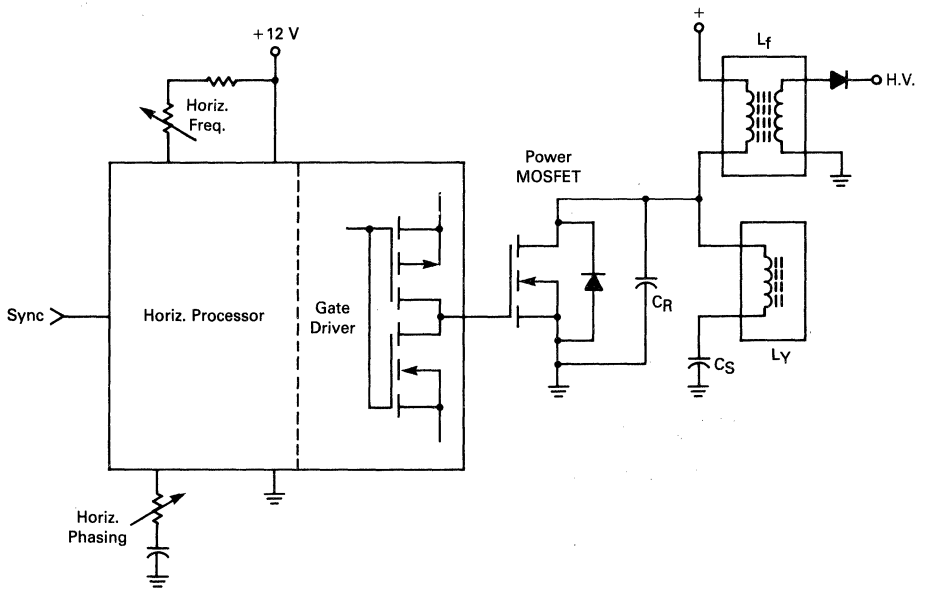


FIGURE 7-32 — POWER MOSFET HORIZONTAL OUTPUT SYSTEM

Figure 7-35 shows a comparison of the key horizontal output circuit waveform patterns between a bipolar and MOSFET design. Note the large reduction in the horizontal output drive power and lack of storage time in the MOSFET design.

FAST HIGH-CURRENT MOSFET DRIVER

A totem-pole MOSFET driver circuit shines when high-current, fast-transition pulses must be generated from low-voltage sources. Its MOSFETs sidestep a number of problems that their bipolar counterparts present in the same circuit.

High-speed transistors and high-current transistors intended for PWM applications have created a need for high-current, fast-drive circuits. Transistors that demand 20 to 35 A of reverse base current for rapid turn-off and can be driven by as little as 5.0 V of off-voltage are a common requirement. Bipolar devices switch in nanoseconds but are limited to 5.0 to 10 A when driven from low-voltage collector supplies. With higher current capability, such transistors require power transistors as drivers and, when driven by a low-voltage source, sacrifice switching speed.

Yet a third possible solution — paralleling fast, low-current transistors — presents two problems: current sharing and physical layout.

The MOSFET driver circuit in Figure 7-36 uses two N-channel devices with positive and negative polarities. Fast transitions are possible, even when a low-voltage source is used. The circuit returns to 0 V between pulses, an important feature when driving high-power Darlington transistors with base-bias resistors and speed-up diodes. In this case, excessive heating would otherwise occur during the off-time interval.

Small size, simple configuration, and minimum component count join with ease of operation to make this driver circuit very useful for applications in variable-frequency switched-mode power supplies, and inverters.

In operation, a single-polarity, negative-going pulse from a pulse generator is applied to the input. The pulse, whose width can vary anywhere from 5.0 μs to 3.0 ms, turns on PNP predriver transistors Q2 for the positive-polarity output.

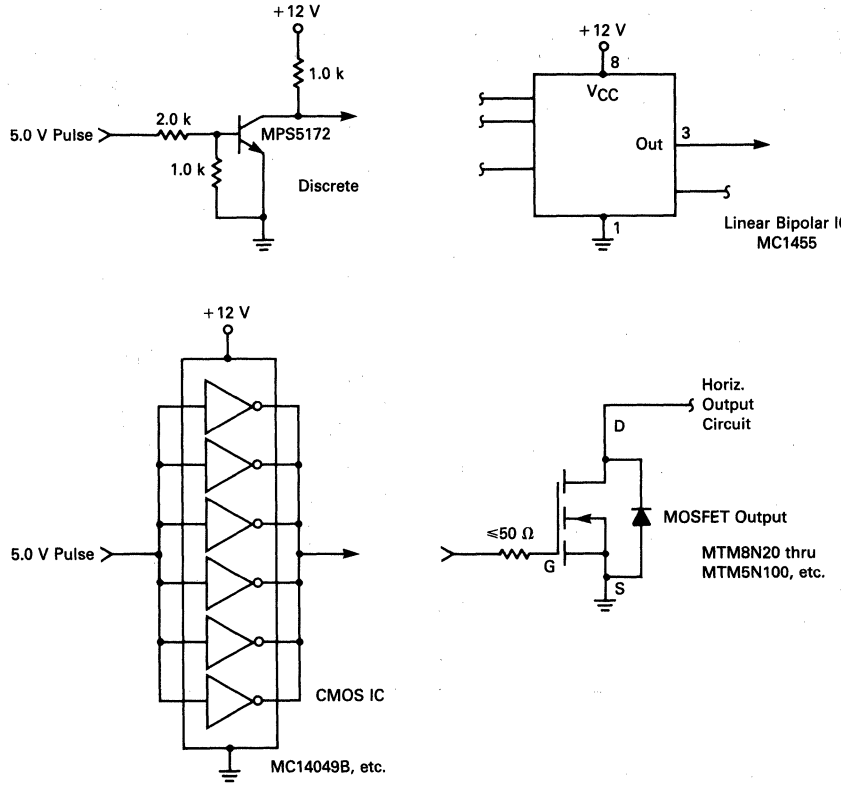


FIGURE 7-33 — MOSFET DRIVE CIRCUITS

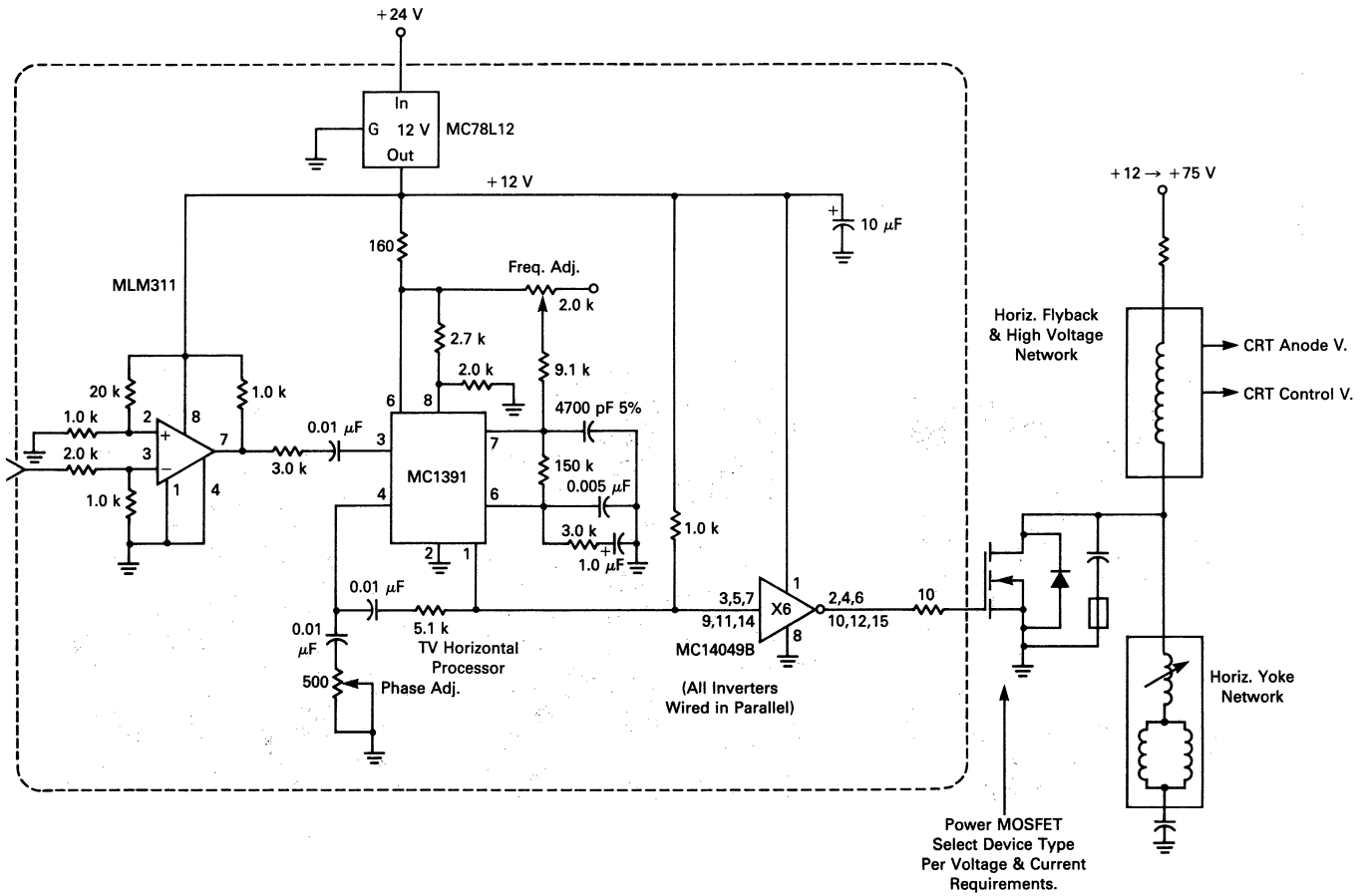


FIGURE 7-34 — POWER MOSFET HORIZONTAL SWEEP DESIGN

A

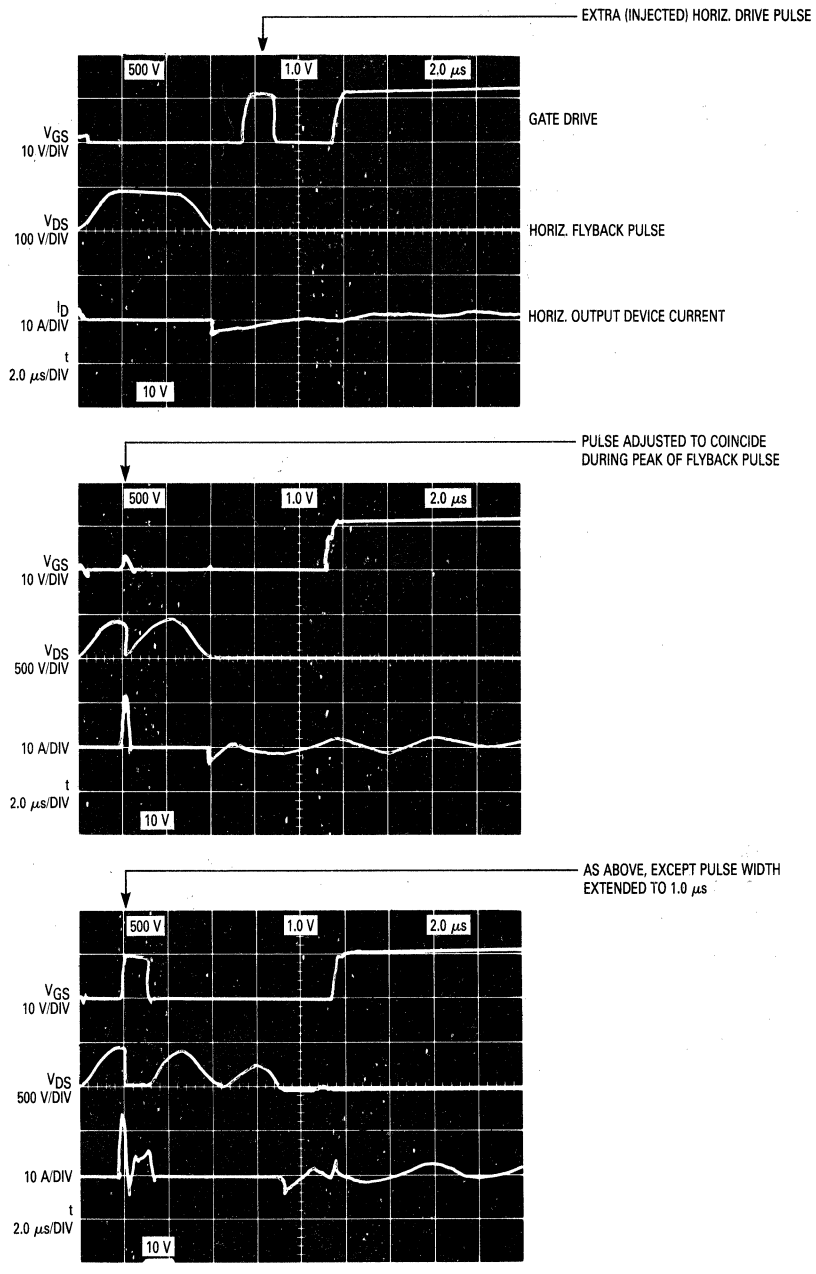
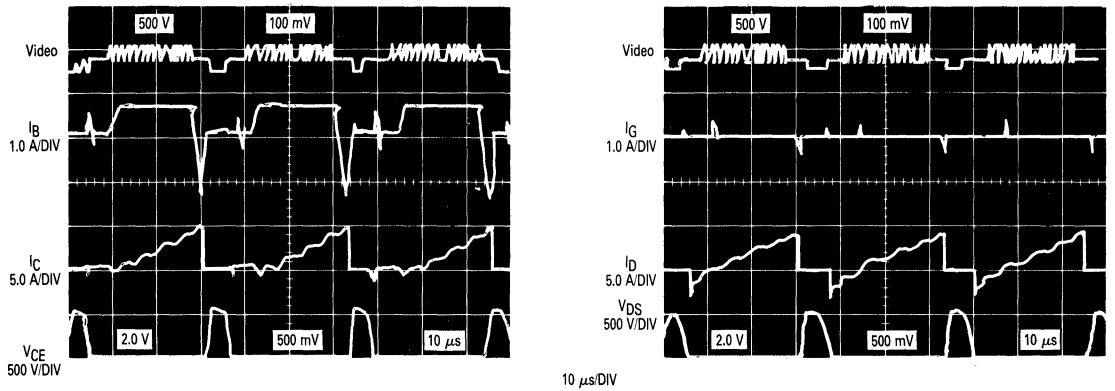


FIGURE 7-35 — HORIZONTAL DEFLECTION RETRACE PULSE TEST WAVEFORMS

BIPOLAR
$t_{off} \simeq 3.5\ \mu s$

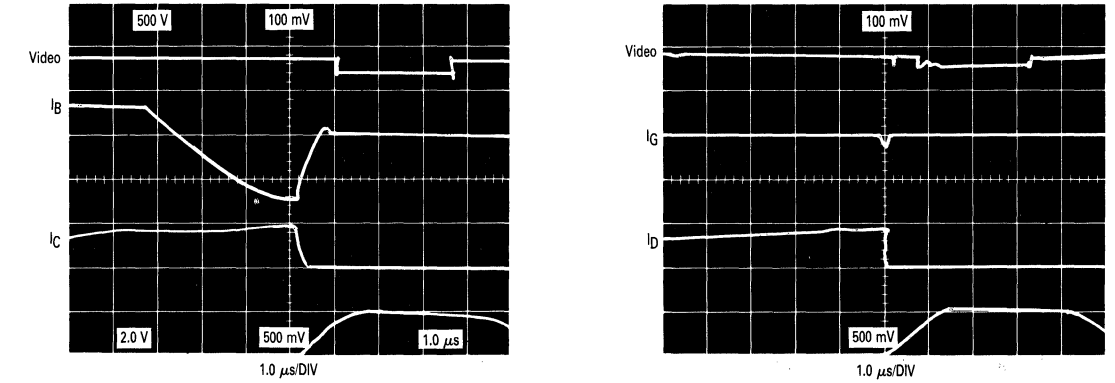
versus

MOSFET
$t_{off} \simeq 155$ ns



10 μs/DIV

Complete Waveforms

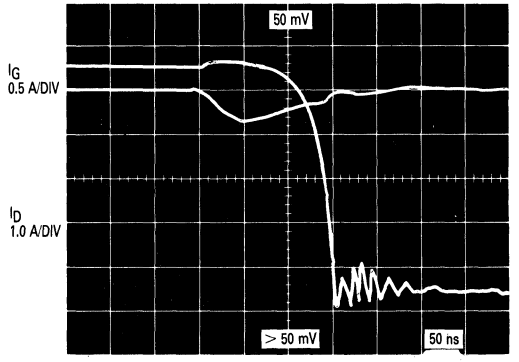


1.0 μs/DIV

1.0 μs/DIV

Time Expanded

Note:
External Damper
Rectifier left
in ckt to minimize
ringing during start
of negative yoke current



MOSFET CURRENTS EXPANDED
TURN-OFF WAVEFORMS

FIGURE 7-36 — BIPOLAR versus MOSFET

Resistor R_b, inserted in series with the drain lead of Q2 and the supply, sets the positive drive level. The resistor should be selected for a drive of 10 V or greater as well as the amount of desired current.

After the required on-time of the positive output current, the pulse generator returns to zero. Then, the RC differentiator network applies a positive voltage to the gate of MOSFET Q3, which supplies the negative polarity output. The values shown can be changed to lengthen the duration of the negative drive. The negative voltage remains for about 10 μs and then returns to zero, completing a single cycle.

The circuit can be used with FETs by replacing R_b with a short and the positive and negative voltages applied to the devices' gates. For controlled gate-impedance drive, resistors can be inserted in series with the gates. Similarly, a resistor added in series with the base of the bipolar transistor results in controlled base-current drive.

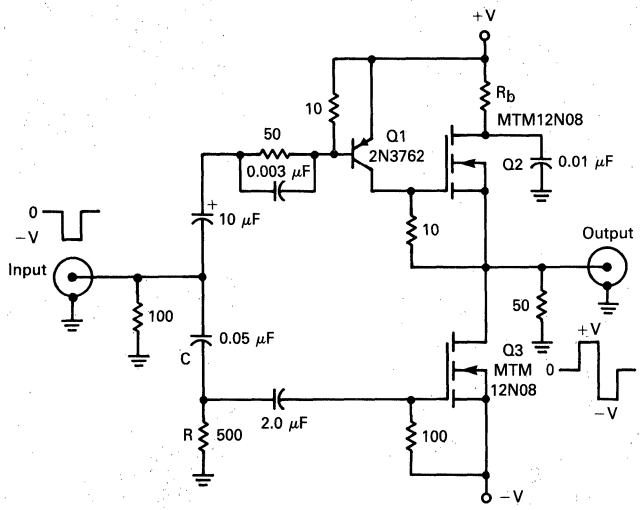


FIGURE 7-37 — MOSFET DRIVER CIRCUIT

Chapter 8: Spin-Off Technologies of TMOS

The GEMFET — A New Option for Power Control

The world of power switching is constantly searching for the ideal switch. Such a switch would have infinite resistance in the off-state, zero resistance in the on-state, instantaneous switching times, and require zero input power to operate. In a real switching application, one must choose the device that most closely approximates the ideal switch for that particular application. The choice involves considerations such as voltage, current, switching frequency, drive circuitry, inductive loads, temperature effects, etc. Every switching device has its strong points and weak points and the designer is always forced to make trade-offs to find the best switch for a given situation.

For a solid state switch, the three characteristics that are most desirable are fast switching speeds, simple drive requirements and low on-state losses. In low voltage applications, the new generations of power MOSFETs have very low on-resistance and closely model the ideal switch. But in high voltage devices, comparatively high on-resistance still limits the MOSFETs efficiency. Furthermore, future advances in decreasing $r_{DS(on)}$ will become more difficult as on-resistances fall closer to the theoretical minimum, which is determined by the optimum cell geometry and the resistivity of the N-epi layer. Therefore, subsequent large reductions in $r_{DS(on)}$ of high voltage MOSFETs will require new technologies.

The GEMFET (Gain Enhanced MOSFET) is the result of one such technological advance. It is a relatively new high voltage power semiconductor device with a combination of characteristics previously unavailable to the designer of power circuitry. Closely related to the power MOSFET in structure, this new device has forward voltage drop comparable to bipolars while maintaining the high input impedance and fast turn-on associated with the isolated gate of the MOSFET. Although turn-on speeds are very fast, current fall times of approximately 4.0 μs are quite slow, and may restrict the use of at least the first generation of these devices to lower frequency applications.

At switching frequencies below about 10 kHz, however, the GEMFET is an attractive alternative to the more traditional bipolars, power MOSFETs and thyristors. Compared to a standard thyristor, the GEMFET is faster and has a higher input impedance, better dv/dt immunity and, above all, gate turn-off capability. While some thyristors, e.g. GTOs, can be turned off at the gate, this requires substantial reverse gate-drive current, whereas, turning off the GEMFET requires only that the gate capacitance be discharged. On the other hand, thyristors generally have a slightly lower forward drop and a higher surge current rating than a comparable GEMFET.

In a comparison of drive requirements, the GEMFET clearly outperforms bipolar transistors. In a 10 A application, for instance, the bipolar requires 2.0 A of base drive (assuming a beta of 5.0) while the GEMFET requires only nanoamperes of gate current to remain in the "on" state. Without the large base-drive current required by the bipolar, the GEMFET gate-drive circuit can be much simpler and more efficient. Darlingtons also simplify drive requirements, but on-voltage is compromised in doing so.

Sometimes MOSFETs are used in low frequency applications because of their simple gate-drive requirements. In many low frequency, high voltage circuits, replacement of the MOSFET with a GEMFET improves efficiency or reduces the cost of the switch. Because their structures and gate-drive considerations are so similar, the change usually entails no significant circuit modifications. Substitution of a GEMFET with approximately the same die area dramatically improves on-state efficiency and current ratings.

If cost is a major concern, another option is to replace the power MOSFET with a GEMFET that has a smaller die area. The result can be a device with a similar current rating and comparable on-state losses. Except at higher frequencies, the cost/performance tradeoffs are substantially in favor of the GEMFET.

The GEMFET is suitable for high current, high voltage, low frequency applications because of its low forward drop and relatively long turn-off time. Appropriate applications for the GEMFET include motor drive circuits, automotive switches, programmable controllers, robotics, home appliances, machine tools, etc.

DEVICE STRUCTURE

The GEMFET is very similar to the double-diffused power MOSFET. Simply by varying starting materials and by altering certain process steps, a GEMFET may be produced from a power MOSFET mask set. Figure 8-1 illustrates that the two structures are identical except for the P^+ layer adjacent to the drain metalization. Additional current carriers in the form of holes are injected from the P^+ substrate into the normally high resistivity N-epi layer and markedly reduce the on-voltage. The resulting four layer structure (P-N-P-N) allows current densities much greater than those attainable in power MOSFETs and comparable to those of bipolars.

Like the power MOSFET, the gate of the GEMFET is electrically isolated from the rest of the chip by a thin layer of SiO_2. Accordingly, the GEMFET is also a high input impedance device and exhibits the associated advantages of modest gate-drive requirements and excellent gate-drive efficiencies. The uniqueness of the GEMFET is that low on-voltages as well as high input impedances are now available in high voltage power semiconductors.

The symbols and equivalent circuits of the GEMFET and MOSFET are shown in Figure 8-2. Because of its four layer structure, the GEMFET lacks the parasitic drain-source diode common to nearly all power MOSFETs.

DEVICE CHARACTERISTICS

Output Characteristics

In the forward conduction mode, the GEMFET closely resembles a power MOSFET. The equivalent circuit is best modeled as shown in Figure 8-2 in which a low voltage, low $r_{DS(on)}$, N-Channel MOSFET is driving a PNP transistor in a compound configuration. The PNP device not only helps lower the effective $r_{DS(on)}$, but also en-

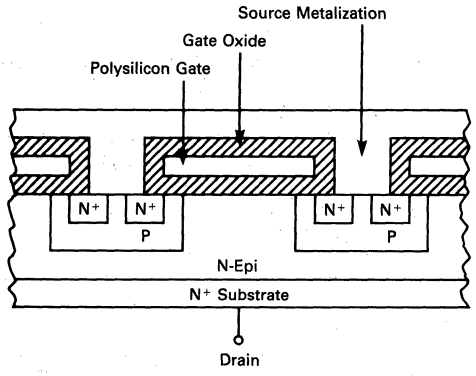


FIGURE 8-1a — CROSS SECTION OF TMOS CELL

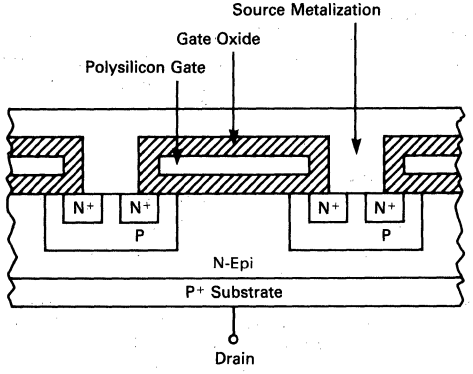


FIGURE 8-1b — CROSS SECTION OF GEMFET CELL

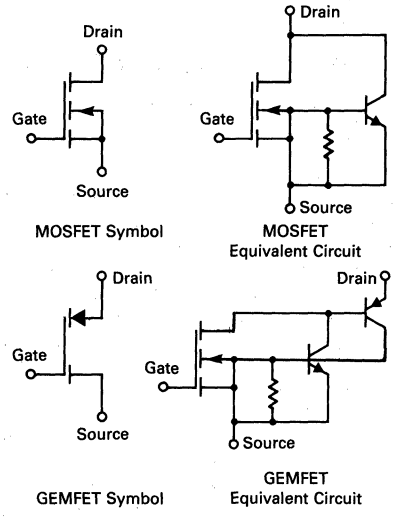


FIGURE 8-2 — MOSFET AND GEMFET SYMBOLS AND EQUIVALENT CIRCUITS

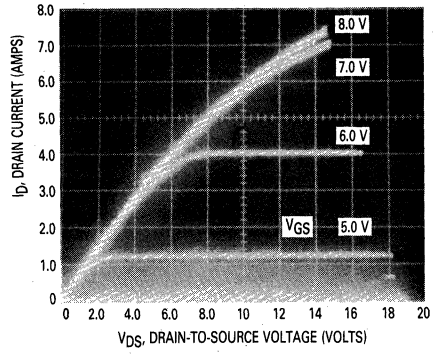


FIGURE 8-3a — OUTPUT CHARACTERISTICS OF POWER MOSFET (MTP4N50)

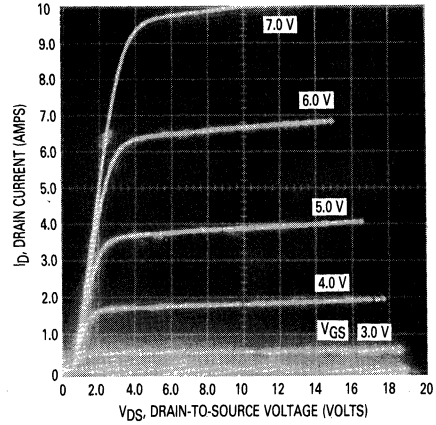


FIGURE 8-3b — OUTPUT CHARACTERISTICS OF GEMFET (MGP20N50)

hances the device gain (transconductance) at high drain currents. Except at excessive drain currents or junction temperatures, the NPN device is considered to be a parasitic and does not influence circuit operation.

The output characteristics of a popular power MOSFET (MTP4N50) and a GEMFET (MGP20N50) of identical die dimensions and similar breakdown voltages are shown in Figures 8-3a and 8-3b. The two major differences between the curves are:

1 — The GEMFET has a much lower on-resistance at currents greater than 2.0 A.

2 — Before the GEMFET can conduct current, the P-N junction formed by the P+ substrate and the N-epi layer must be forward biased. Consequently, the GEMFET curves are offset from the origin by a diode drop, similar to SCRs or Darlingtons.

Figure 8-4 indicates that at 25°C the 20 A, 500 V MGP20N50 gives no hint of a propensity to latch at currents up to 62 A, which is much larger than the pulsed current rating of the MOSFET.

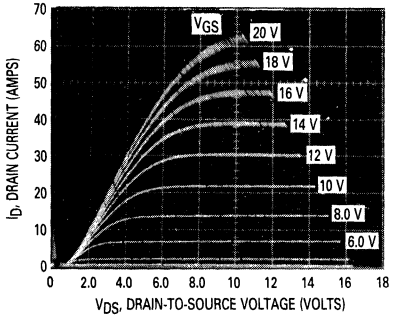


FIGURE 8-4 — OUTPUT CHARACTERISTICS OF GEMFET AT HIGH DRAIN CURRENTS

Switching Speeds

Presently, the feature that limits the GEMFET from serving a very wide range of applications is its relatively slow turn-off speed. While turn-on is fairly rapid, current fall times at turn-off can exceed 4.0 μs.

The turn-off of the GEMFET is rather slow because many minority carriers are stored in the N-epi region. When the gate is initially brought below threshold, the N-epi contains a very large concentration of electrons, consequently, there will be significant electron injection into the P^+ substrate and a corresponding hole current into N-epi.

As the electron concentration in the N-region decreases, the electron injection decreases, leaving the rest of the holes and electrons to recombine. The turn-off of the GEMFET should then have two phases: the injection phase where the drain current falls very quickly; and a recombination phase where the drain current decreases more slowly. Figure 8-5 shows the clamped inductive turn-off waveforms of the MGP20N50.

Although turn-off speeds are not impressive, this is the first generation of these devices and improvements in switching speeds can be expected. For GEMFETs, there is an $r_{DS(on)}$ — switching speed trade-off. Theoretically, turn-off times can be decreased without large increases in $r_{DS(on)}$ by controlling carrier lifetimes or by other proprietary methods.

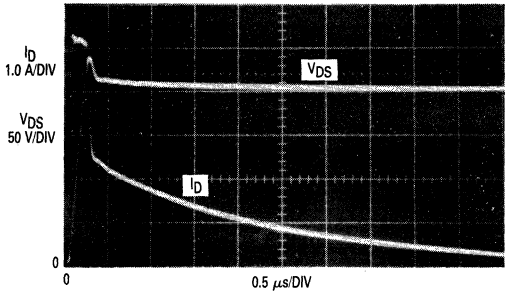


FIGURE 8-5 — CLAMPED INDUCTIVE TURN-OFF OF GEMFET

Even though MOSFETs are championed for their simple gate-drive requirements, at high operating frequencies sizable peak gate currents must be supplied to ensure rapid switching. Since this first generation GEMFET is, by comparison, much slower, the gate drive-impedance can be fairly high without affecting turn-off speeds. In the circuit shown in Figure 8-6, R_G was varied from 0 to 1.0 kΩ, but the current fall time essentially remained constant at 3.75 μs (Table 1).

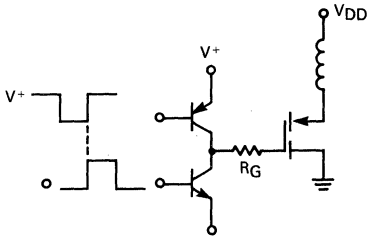


FIGURE 8-6 — CIRCUIT TO TEST VARIATIONS IN CURRENT FALL TIMES WITH CHANGES IN GATE DRIVE IMPEDANCE

TABLE 1 — Effect of Series Gate Resistance on Turn-off Speeds

Series Gate Resistance	0 Ω	50 Ω	100 Ω	200 Ω	500 Ω	1000 Ω
Drain Voltage Rise Time	140 ns	140 ns	150 ns	180 ns	350 ns	810 ns
Drain Current Fall Time	3.75 μs	3.75 μs	3.75 μs	3.75 μs	3.75 μs	3.75 μs

Comparison of On-State Losses

The most pronounced advantage of the GEMFET over the power MOSFET is its lower on-resistance. The $V_{DS(on)}$ of a high voltage MOSFET is fairly large and rises with increasing junction temperature and drain current. Conversely, the $V_{DS(on)}$ of a GEMFET decreases with increasing T_J and is not greatly affected by I_D. Figure 8-7 compares the on-voltages of the two technologies at various drain currents and at a T_J of 25°C and 100°C. Since the MOSFET does not have the GEMFET's offset voltage in its output characteristics, at low currents the MOSFET on-voltage is slightly lower. However, as the illustration suggests, at high currents and temperatures the difference is dramatic. For comparison, a bipolar transistor was also included in Figure 8-7. Its on-voltage is a function of the transistor's high current beta and the magnitude of the base current.

On-state efficiencies are not solely determined by on-voltages. Gate or base-drive currents are also contributing factors. Its high input impedance allows the GEMFET to rival the on-state efficiency of the bipolar transistor, even though its on-voltages are comparable to those of SCRs (one diode drop in addition to a bipolar saturation voltage). The bipolar device chosen for this comparison had a forced beta so low (about 5) at the desired collector current that the base current losses were important.

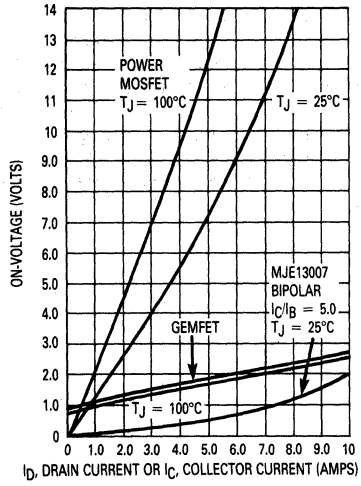


FIGURE 8-7 — ON-VOLTAGE versus DRAIN OR COLLECTOR CURRENT FOR A GEMFET, MOSFET AND BIPOLAR OF EQUIVALENT DIE SIZE

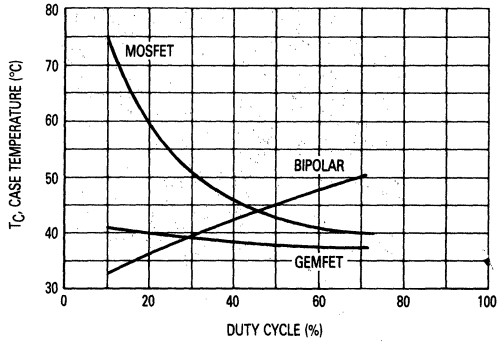


FIGURE 8-8 — ON-STATE EFFICIENCY COMPARISON — PULSE WIDTH MODULATION OF DC MOTOR

To illustrate the variation in the on-state efficiencies of each technology, a bipolar transistor, MOSFET and GEMFET were used as the switching element in an open loop PWM dc motor control circuit. The bipolar (MJE13007) was a 156 x 156 mil chip rated at 8.0 A, 400 volts. The 20 A, 500 volt GEMFET (MGM20N50) and the 4.0 A, 500 volt MOSFET (MTP4N50) had areas equivalent to a die size of 150 x 150 mil. To keep switching losses to a minimum, the frequency was held constant at about 90 Hz as the duty cycle was varied from 9% to 71%. Since a motor is a nonlinear load and conditions such as motor speed and back EMF change with pulse width, the results of the comparison (Table 2 and Figure 8-8) should be carefully interpreted.

The "relative power out" referred to in Table 2 is simply a measurement proportional to the motor speed and is inversely related to the saturation voltage. If the on-voltage is high, the potential across the motor is diminished and the speed is decreased. The "relative power in," a measure of forward base (or gate) current, is useful for comparing the required base or gate power necessary to control a five ampere load.

The following generalizations can be drawn from Table 2 and Figure 8-8:

1. Even though its on-voltage is very low, the bipolar is not the most efficient device at high duty cycles. The power consumed by the device due to its large base current is great enough to be reflected in an increase in case temperature. Because of the bi-

TABLE 2 — On-State Efficiency Testing: Pulse Width Modulation of DC Motor

	Pulse Width (ms)	Duty Cycle %	$I_{D(max)}$ (A)	Case Temp (°C)	Power Dissipation (W)	On Voltage (Volts)	V_{DS} or $V_{CE(pk)}$ (Volts)	Relative Power Out (Speed)	Relative Power In
GEMFET	8.0	71	0.75	37.2	0.69	1.0	1.75	78	2.0
	6.0	54	1.0	37.4	0.70	1.1	2.0	77	2.0
	4.0	36	1.6	38.5	0.75	1.1	2.5	73	2.0
	2.0	18	2.75	39	0.79	1.5	4.0	64	2.0
	1.0	9.0	4.50	40.9	0.86	2.0	6.5	49	2.0
TMOS	8.0	71	0.75	38.6	0.76	1.0	1.75	78	2.0
	6.0	54	0.80	42.1	0.91	1.3	2.25	77	2.0
	4.0	36	1.25	49.4	1.22	2.0	3.25	70	2.0
	2.0	18	2.25	62	1.77	4.5	6.50	48	2.0
	1.0	9.0	3.50	77.4	2.44	7.5	11.00	18	2.0
MJE13007	8.0	71	0.80	49.7	1.24	0.1	0.8	82	140
	6.0	54	1.1	45.7	1.06	0.2	1.0	81	104
	4.0	36	1.5	40.7	0.85	0.2	1.5	78	72
	2.0	18	2.75	34.8	0.59	0.3	3.0	70	36
	1.0	9.0	4.5	32.6	0.50	0.5	5.0	59	20

T = 11.2 ms T_A = 21.2°C f ≈ 90 Hz V_{DD} ≈ 14 V $R_{\theta HS}$ = 23°C/W

polar's low beta, the case temperature and power dissipation closely track the relative power in.

2. The bipolar invariably results in the highest motor speed for a given pulse width because its saturation voltage is always lowest.
3. For the MOSFET, high on-resistance, especially at higher currents and temperatures, influences the performance. As the duty cycle decreases, the motor speed and back EMF also decline. With the lower back EMF, the effective motor voltage is higher, allowing higher currents. The increasing current and on-resistance combine to elevate the case temperature at low duty cycles.
4. The case temperature of the GEMFET remains almost unchanged as conditions vary. Unlike the bipolar, its input power is very small and does not significantly affect the power dissipation at high duty cycles. At lower duty cycles and higher currents, the GEMFET on-voltage is much lower than the MOSFET's. Again, the result is cooler case temperatures.

While the GEMFET looks quite respectable in this comparison, the peak current chosen influences the relative efficiencies. If the motor supply voltage had been increased to obtain larger peak currents, the comparison would have been even more in favor of the GEMFET. The MOSFET would have performed more poorly due to its I_D-$r_{DS(on)}$ relationship, and the bipolar's base drive losses, due to forced betas' less than 5.0, would further reduce its efficiencies at large pulse widths.

Switching Losses

The present maximum operating frequency of the GEMFET is limited by its turn-off speed. Defining a specific upper limit could be misleading because the frequency limitation depends on heat sinking, drain current, drain supply voltage, gate-drive impedance, and drain-source flyback voltage. To set a benchmark for a specific set of conditions, the following test circuit and procedure was developed to compare the switching efficiencies of a GEMFET (MGP20N50), MOSFET (MTP4N50), and bipolar (MJE13007).

In the test procedure, the independent variable was switching frequency, which was varied by changing the timing capacitor C1 in the test circuit shown in Figure 8-9. By adjusting potentiometer R1 and by properly sizing the inductive load, the load current waveform was fixed to a 25% duty cycle and a peak of 5.0 A.

For the MJE13007, the forced beta of 5.0 required a base current of 1.0 A. Turn-off of all three types of devices was initiated by clamping the base (or gate) to −5.0 volts. The oscillograms in Figure 8-10 show the drain (or collector) current and drain-source (or collector-emitter) voltage of each device at 7.0 kHz.

Again, the test results were quite predictable, and the case temperature versus frequency for this specific case is plotted in Figure 8-11. The efficiency of the heat sink, in this instance a 4½" x 4½" x ⅛" copper plate ($R_{\theta CA}$ = 5°C/W), markedly influences the temperature rise results. A larger or smaller heat sink would have decreased, or increased, the noted temperature differences. The testing was restricted to lower frequencies because above 40 kHz

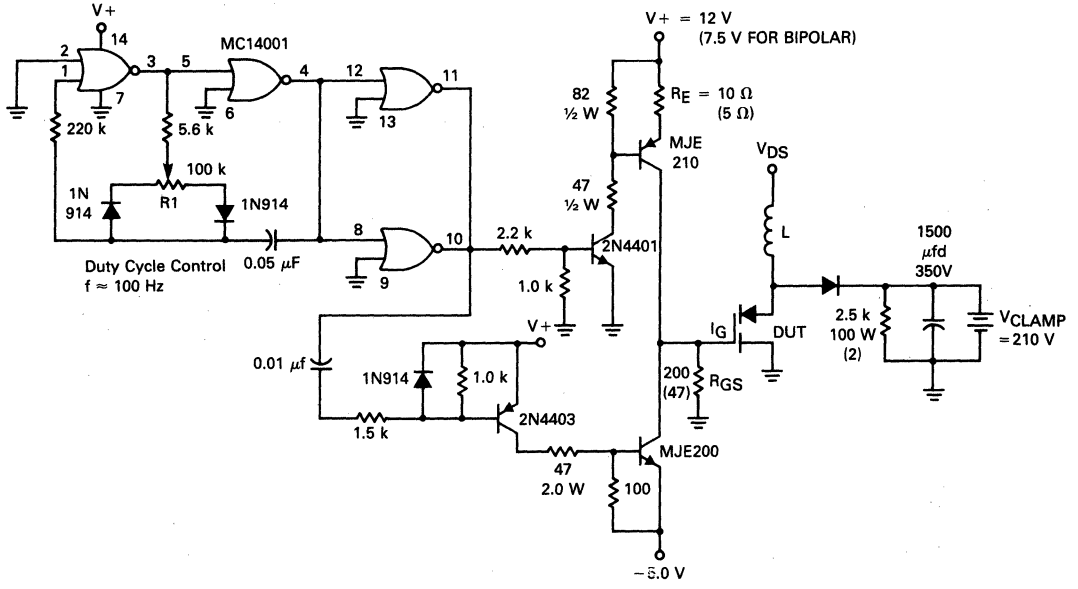


FIGURE 8-9 — CIRCUIT TO COMPARE SWITCHING EFFICIENCIES OF GEMFET, MOSFET AND BIPOLAR

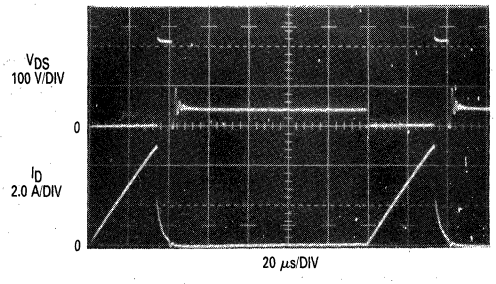


FIGURE 8-10a — CLAMPED INDUCTIVE SWITCHING WAVEFORMS AT 7.0 kHz — GEMFET

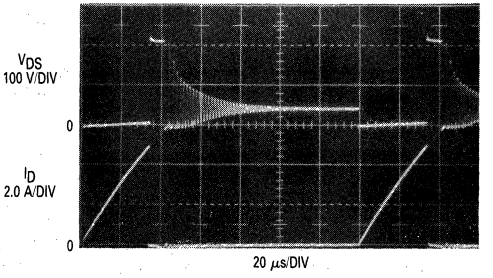


FIGURE 8-10b — CLAMPED INDUCTIVE SWITCHING WAVEFORMS AT 7.0 kHz — MOSFET

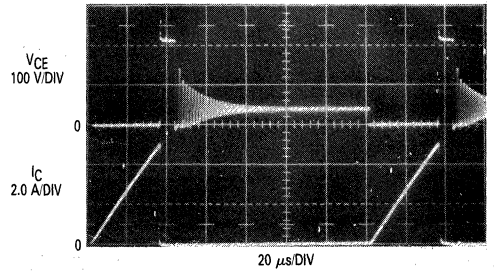


FIGURE 8-10c — CLAMPED INDUCTIVE SWITCHING WAVEFORMS AT 7.0 kHz — BIPOLAR

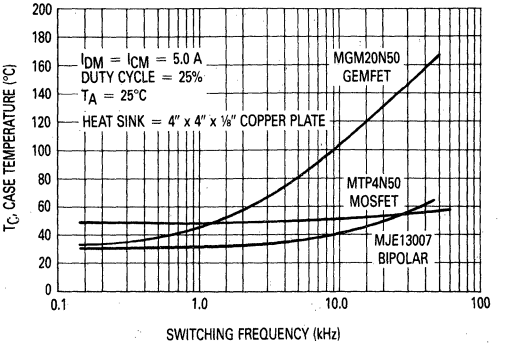


FIGURE 8-11 — COMPARISON OF CASE TEMPERATURE versus FREQUENCY FOR A GEMFET, MOSFET AND BIPOLAR

secondary effects began to influence and distort the comparison.

The GEMFET switching losses rose rapidly with frequency, illustrating its high-frequency limitations. By comparison, the bipolar's case temperature increased only slightly while the MOSFET proved its high frequency capability with virtually no case temperature rise.

Thermal Resistance, $R_{\theta JC}$

As expected, GEMFETs and power MOSFETs produced from the same mask set have very similar junction-to-case thermal resistances. $R_{\theta JC}$ of a power MOSFET can be determined by testing for variations in one of the following temperature sensitive parameters, or TSPs:

1. Drain-source diode on-voltage
2. Gate-source threshold voltage
3. Drain-source on-resistance

All previous thermal resistance testing of the TMOS power MOSFET was based on the temperature dependence of the on-voltage of its drain-source diode. For the MTP4N50, the results were typically about 0.79°C/W. Because the GEMFET has no parasitic diode, this method was inappropriate for the MGP20N50. Instead, $R_{\theta JC}$ of the GEMFET was determined by using a second circuit that detects variations in the gate-source threshold voltage due to changes in T_J. Before testing the GEMFET, correlation between the two test methods was obtained by comparing the results of testing the MOSFET in each circuit. By testing for variations in $V_{GS(th)}$, the $R_{\theta JC}$ of the MTP4N50 and the MGP20N50 were both typically 0.67°C/W. This suggests that the two methods are in fairly close agreement and that the thermal resistances of a MOSFET and GEMFET of equal die area are essentially the same.

Safe Operating Areas

Important ratings of any solid state switching element are its Safe Operating Areas. For the GEMFET, these include its Forward Biased SOA, or FBSOA, and Reverse Biased SOA, or RBSOA. Since non-destructive fixtures were used to determine both of these SOA limitations, an entire curve could be drawn with each device tested. With this capability, device trends readily became apparent.

Figure 8-12 shows the dc FBSOA limits of an MTP5N40 and an MGP20N50. Even though the curves are quite similar, at either end there are significant differences. At high voltages and low currents, the GEMFET's curve begins to roll off somewhat like the curve of a bipolar that is approaching a second breakdown limitation. This is not surprising since the parasitic PNP bipolar is instrumental in sustaining its unique mode of current conduction.

At the low voltage, high current portion of the FBSOA curve, the effect of $r_{DS(on)}$ is evidenced in two different ways. First, at very low drain-source voltages, $r_{DS(on)}$ can limit I_D. This is simply a manifestation of Ohm's Law and does not indicate a stress-related limit. As Figure 8-12 suggests, the wide difference in on-resistances between MOSFET and GEMFET is reflected in the $r_{DS(on)}$ limit

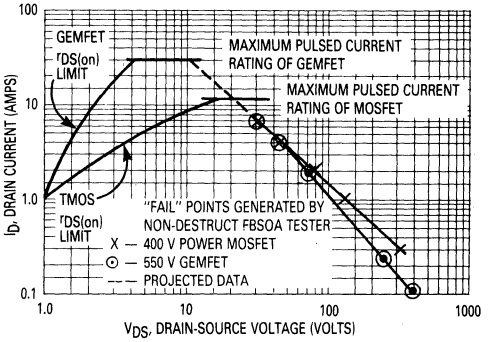


FIGURE 8-12 — COMPARISON OF FBSOA CURVES OF A 400 V MOSFET AND 550 V GEMFET OF EQUAL DIE AREA

of their respective FBSOA curves. Second, a lower on-resistance also increases a device's peak-current rating by virtue of its more efficient current conduction. This limit is stress related and also is illustrated for both devices in Figure 8-12.

An RBSOA rating details the maximum drain-current and drain-source voltage stress allowable during clamped inductive turn-off. If a device undergoes second breakdown at some combination of V_{DS} and I_D that is within its pulsed power dissipation capability, an RBSOA derating curve is in order. In essence, an RBSOA derating indicates that a device may fail due to localized hotspotting even though its average junction temperature is within its $T_{J(max)}$ rating. Second breakdown of the MOSFET only occurs when its maximum junction temperature is exceeded. Therefore, operation of the MOSFET is only limited by its $T_{J(max)}$, I_{DM} and V_{DSS} ratings.

As for the GEMFET, special RBSOA considerations are necessary to ensure optimum reliability. Junction temperature and turn-off speed are especially noteworthy parameters since they can dramatically alter the GEMFET RBSOA capability. With all other conditions fixed, an increase in T_J can lessen the reverse-biased safe operating area if the drain current is high. At turnoff, lower gate-drive impedances are also more stressful, as explained below.

Figures 8-13 and 8-14 outline the operating limits of typical MGM20N50 (20 A, 500 V GEMFET in a TO-204 (TO-3) Package). The figures are typical of the devices used in this evaluation and do not represent a guaranteed RBSOA rating. A more thorough evaluation is being conducted to provide guaranteed curves for the data sheet. The gate-drive circuit used (Figure 8-15) allows adjustment of the gate-drive output impedance at turn-off simply by varying R_{GS}.

To generate each "fail" point, a resistor, drain current and temperature were selected, then the magnitude of the clamp voltage was increased until the device either dissipated the coil's energy in avalanche or entered second breakdown. If the test device experienced a rapid collapse of its drain-source voltage (which is characteristic of second breakdown), the non-destruct fixture rapidly (150 ns) removed energy from the DUT before its die suffered damage.

Interestingly, the failure mechanism is not simply power related, i.e., slower switching speeds and greater crossover times tend to increase its RBSOA. This is clearly shown in the turn-off waveforms of Figures 8-16a and 8-16b. Even though the device enjoys lower switching losses with an R_{GS} of 51 Ω, its RBSOA is lessened. This phenomena may be due to a very rapid MOSFET turn-off that places a dv/dt stress on the PNP bipolar.

If the GEMFET is turned off more slowly, the MOSFET

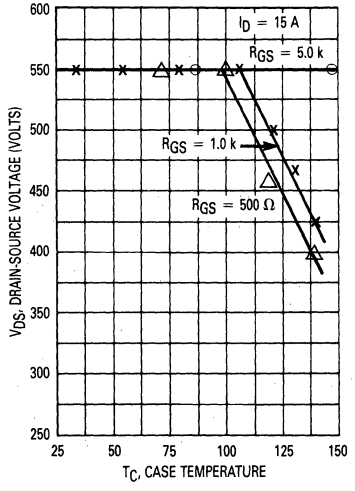


FIGURE 8-13 — EFFECT OF GATE DRIVE IMPEDANCE AND CASE TEMPERATURE ON GEMFET RBSOA

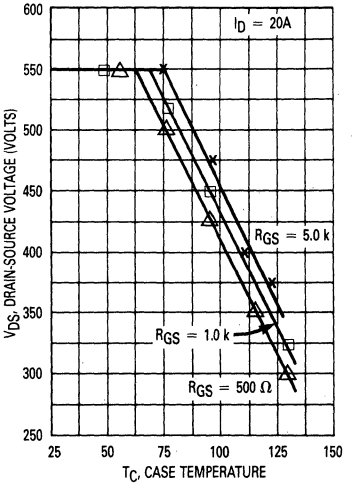


FIGURE 8-14 — EFFECT OF GATE DRIVE IMPEDANCE AND CASE TEMPERATURE ON GEMFET RBSOA

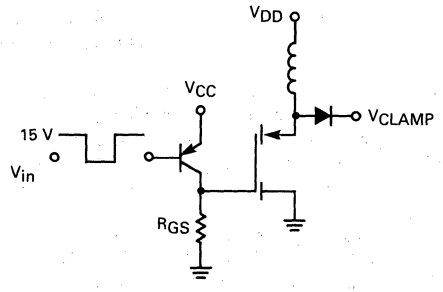


FIGURE 8-15 — GEMFET RBSOA GATE DRIVE CIRCUIT

carries a greater portion of the load current and lessens the strain on the bipolar during this critical portion of the switching cycle.

The GEMFET is poised to alter the options available to power circuit designers. While its slow turn-off speeds limit its potential applications at this point, the GEMFET's low $r_{DS(on)}$ and high input impedance make it the technology of choice for many applications requiring low frequency switching.

An Application of the GEMFET

An ideal example of a GEMFET application would highlight its three strongest features. It would require a switch with high blocking voltage capability, a large current rating and simple drive requirements. The switching element in an automotive electronic ignition control system is one of many such applications in which the GEMFET deserves consideration as an alternative to the switches currently in use.

Presently, high voltage Darlingtons are the most commonly used switch in automotive ignition systems. The advantage of using a GEMFET as its replacement is the elimination of the Darlington's base drive circuitry. Since the required switching frequency is below 1.0 kHz, the GEMFET's high input impedance and low drive requirements make it ideally suited to be driven directly from CMOS logic.

When the transistor — whether it be a Darlington, GEMFET, or Power MOSFET — turns on, the primary current ramps up to 3.0 to 7.0 A (6.0 A peak for this exercise). At turn-off, the inductive kick, or flyback voltage, is allowed to rise as high as practical to produce the very high transformer secondary voltages (20 kV) required to generate a spark. In the present systems that employ high voltage Darlingtons, voltage is often clamped to about 400 V by a zener placed from collector to base. As soon as the collector-base voltage exceeds the nominal zener voltage, the zener supplies the base current to the Darlington, turning it on and thus clamping V_{CE} to V_Z. In this mode the zener carries only a small fraction of the load current and its power dissipation rating can be sized accordingly (a collector-emitter zener must carry the full peak primary current). On the other hand, the transistor is acting as its own voltage clamp and must dissipate the energy contained in the inductive kick.

When a GEMFET is used in place of a Darlington, the same clamping scheme can be used. If the zener is placed across the drain and gate terminals, any zener avalanche current soon changes the GEMFET's input capacitance and initiates turn-on. With this clamping method, the GEMFET experiences the same high power dissipation interval as the Darlington. One additional component is needed in the GEMFET version of the clamp. A diode in series with the zener is needed to block any current that would otherwise flow if the gate were more positive than the drain [high V_{GS}, low V_{DS}].

Since the GEMFET performed very well in this evaluation, the question arises as to the applicability of the power MOSFET in this same circuit. Again the comparison is of the MGM20N50 and the MTM4N50, which are a GEMFET and a MOSFET of identical die size. The first consideration is that a peak drain current of 6.0 A exceeds the MOSFET's 4.0 A continuous rating. This in itself is not a problem, but thermal limitations are possible at higher duty cycles and elevated case temperatures.

Although the greatest stress on the switch occurs during the clamping of the inductive kick and generation of the spark, that clamping interval does not necessarily contribute more to the average power dissipation than does the interval in which the switch is on and current ramps up in the primary. This is especially true of the power MOSFET due to its high $r_{DS(on)}$.

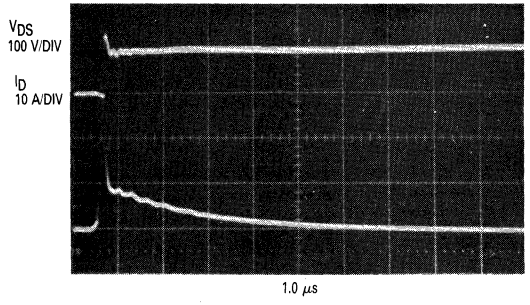


FIGURE 8-16a — CLAMPED INDUCTIVE TURN-OFF WAVEFORMS OF MGM20N50 – R_{GS} = 51 Ω

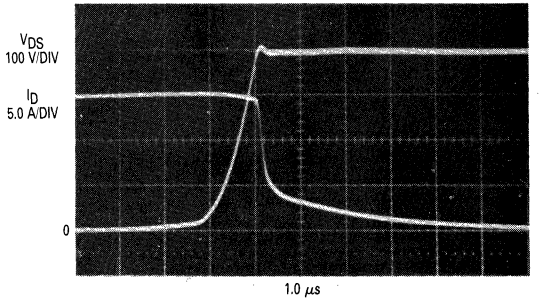
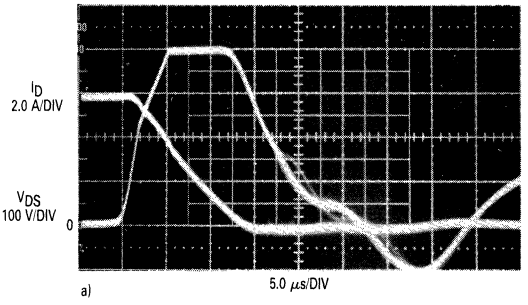


FIGURE 8-16b — CLAMPED INDUCTIVE TURN-OFF WAVEFORMS OF MGM20N50 – R_{GS} = 510 Ω



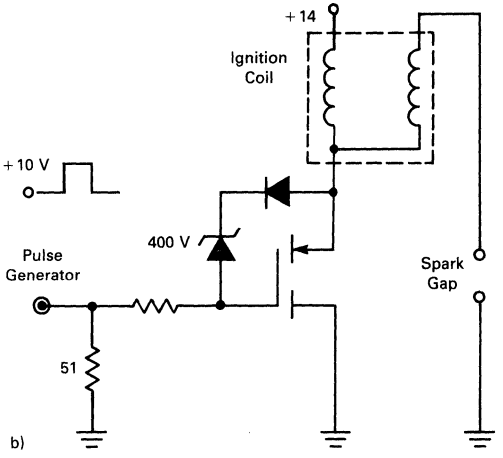


FIGURE 8-17 — AN AUTOMOTIVE ELECTRONIC IGNITION SYSTEM IS AN APPLICATION FOR WHICH THE GEMFET SHOWS GREAT PROMISE. THE SIMPLE GATE DRIVE CIRCUITRY (b) IS ONE OF THE MAJOR ADVANTAGES IN THIS SYSTEM. BECAUSE OF THE DRAIN-TO-GATE ZENER, CURRENT FALL TIME IS DICTATED BY THE AMOUNT OF ENERGY STORED IN THE INDUCTIVE KICK.

The difference between the $r_{DS(on)}$ of the MOSFET and the GEMFET becomes evident during the monitoring of the case temperatures. Under the same conditions (using a Thermalloy heat sink #6016B), the GEMFET's T_C is 37°C, while the MOSFET's is 59°C, representing a 2.5 W difference in power dissipation.

A second problem, again related to the MOSFET's higher $r_{DS(on)}$, also complicates its use in an electronic ignition control system. Due to the limited battery potential, especially during engine startup in very cold weather, the $r_{DS(on)}$ of the switch must remain low so as not to limit the peak current in the primary of the ignition coil. Therefore, the 1.5 Ω maximum specification for the MTM4N50 is probably too high for this application. In this test the "battery" voltage must be increased by about 30% to achieve the same primary current that the GEMFET conducted.

In addition to its higher on-state efficiency, the GEMFET can also offer a cost advantage over the power MOSFET. A large portion of a power transistor's cost is associated with its die area. Since the GEMFET can operate at current densities at least five times that of a high voltage MOSFET, significant savings can result from using a GEMFET with a smaller die size.

The MOS SCR, A New Thyristor Technology

With the introduction of the MOS SCR, the circuit designer is now offered a device which has the advantages of the high input impedance and fast turn-on of a power MOSFET and the regenerative, latching action of a thyristor. Consequently, a new device symbol had to be created, one that combines the features of both technologies, as proposed by the symbol in Figure 8-18, i.e., SCR with FET gate.

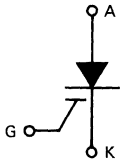


FIGURE 8-18 — PROPOSED MOS SCR SYMBOL

The MOS SCR was developed from the vertical structured TMOS where the substrate doping was changed from N+ material to P+. Thus, a four layer structure evolved (PNPN), creating the two-transistor analogue of an SCR controlled by an N-Channel MOSFET. This evolution is illustrated in Figure 8-19 whereby the power MOSFET symbol progresses through the various equivalent circuits to the final MOS SCR configuration. Note that Figure 8-19d contains the PNP transistor Q1 and the MOS parasitic NPN transistor Q2 of the SCR equivalent circuit and also that the MOSFET Q3 shunts transistor Q2.

Switching action starts by turning on FET Q3 with a positive gate-cathode (source) voltage V_{GT} (or $V_{GS(on)}$). The resulting drain current is the base current of Q1 which turns on this PNP transistor. As in a normal SCR, the collector current of Q1 supplies the base current to Q2 and if adequate loop gain exists $[(\alpha_1 + \alpha_2) > 1)]$, regeneration will occur, latching the device. The gate signal can then be removed and the device will remain latched until the principal current falls below the hold current — that current which satisfies the loop gain criteria.

Due to the MOSFET input, the device exhibits the characteristics of the basic power MOSFET, that is, high input impedance and fast turn-on. And, because of this high, static input impedance, the MOS SCR can be readily driven by standard CMOS logic.

Even though a power MOSFET has an extremely high static input impedance, in order for the device to switch in the tens of nanosecond range, the gate input capacitance must be quickly charged (or discharged during turn-off). The gate-source and gate-drain capacitance (and its

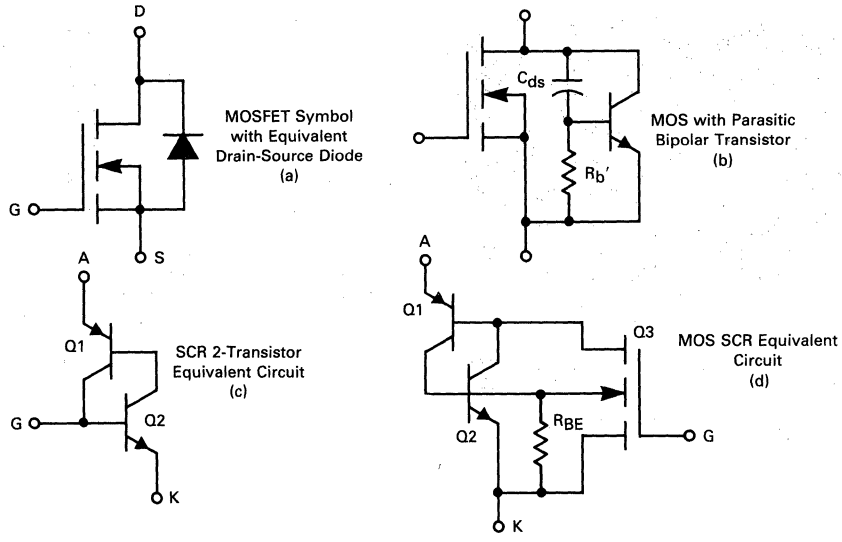


FIGURE 8-19 — EQUIVALENT CIRCUIT EVOLUTION OF THE MOS SCR

Miller capacitance effect) may require peak charging (dynamic) currents in the one-half to several ampere range. Thus, the gate-driver must supply these sometimes high, peak charging currents.

With this in mind, several CMOS gates were used, either individually or in parallel, to generate the MOS SCR gate capacitance charging currents (Figure 8-20). As an example, a single, standard CMOS gate (MC14001) is metallization limited to 10 mA, a quad gate in parallel, about 30 mA and six parallel connected hex buffer gates (MC14049) to perhaps 80 mA of sourcing current. Using the illustrated drivers, zero crossing turn-on characteristics of the ac powered MOS SCR was determined. For this exercise, the gate current limiting resistor R1 and the

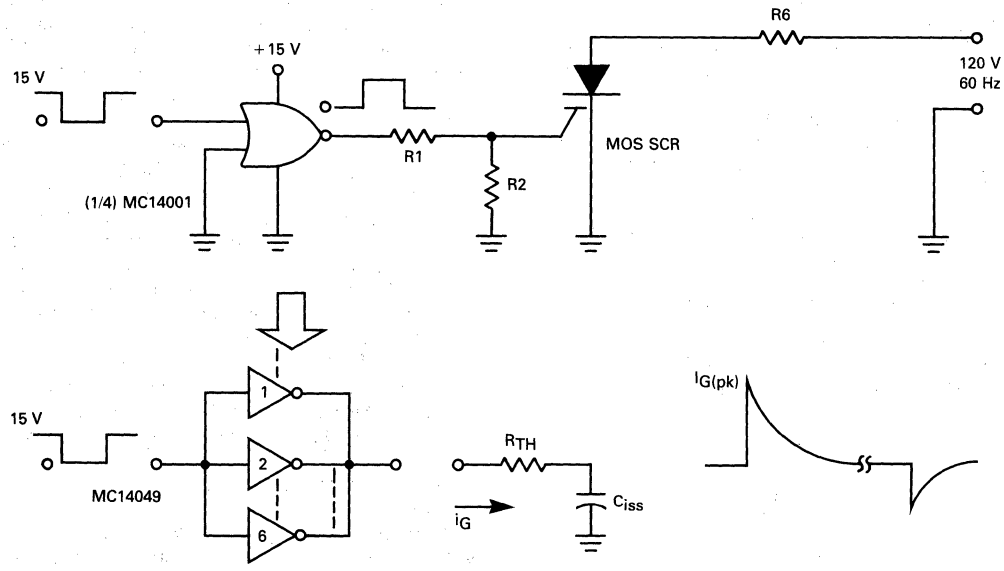
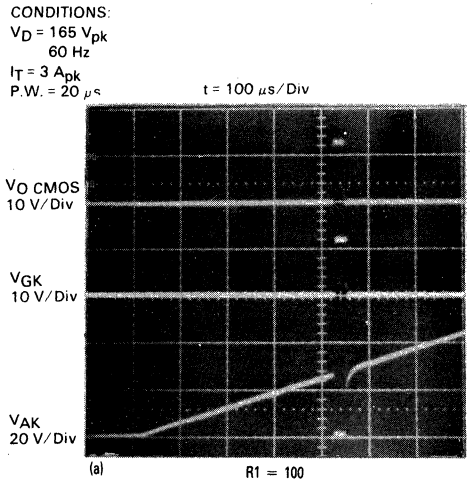
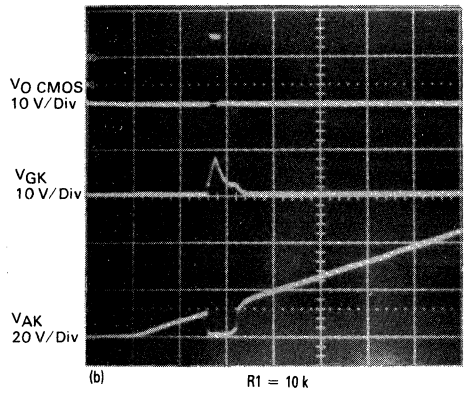


FIGURE 8-20 — EXAMPLES OF INDIVIDUAL OR PARALLEL CONNECTED CMOS DRIVERS FOR MOS SCR





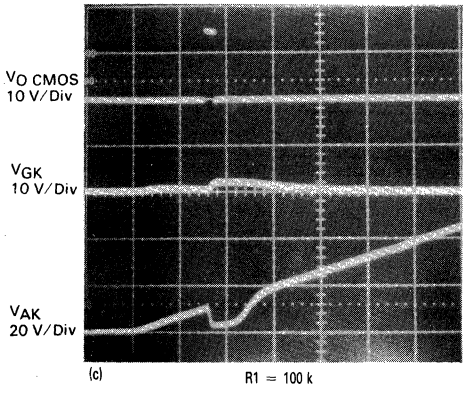


FIGURE 8-21 — MOS SCR TURN-ON WAVEFORMS

gate-cathode R2 were proportionally scaled, e.g., $R1_1$ = 100, $R2_1$ = 1.0 k; $R1_2$ = 10 k, $R2_2$ = 100 k; $R1_3$ = 100 k, $R2_3$ = 1.0 M. The input pulse width was phase delayed to the point just before the MOS SCR started to regenerate. Figures 8-21a, 8-21b and 8-21c illustrate the turn-on switching waveforms for the three gate impedance cases, with the top trace describing the gate compliance voltage (CMOS output), the middle trace, the gate-source voltage and the bottom trace, the anode-cathode voltage just before the MOS SCR fires (latches). For comparison, Figure 8-22 shows the anode-cathode voltage just before firing (not enough delay in the input pulse) and just after firing (input pulse delay increased slightly). Increasing the pulse delay or increasing the pulse width resulted in the same non-conduction angle (the point measured from positive zero crossing to where the SCR fired).

Note that the magnitude of the anode-cathode voltage near firing varied inversely with gate impedance, being about 30 V, 15 V and 15 V (due to longer gate capacitance discharge time) when R1 was 100 Ω, 10 k and 100 k respectively. The results were opposite of what were expected: the lower the gate limiting impedance, the earlier the SCR firing (lower non-conduction angle).

However, upon closer examination of the MOS SCR equivalent circuit (Figure 8-19d), the cause of this effect became apparent: FET Q3 shunts the NPN transistor Q2. With low gate-drive impedance, Q3 turns on very hard and thus offers a very low impedance shunt across Q2 ($r_{DS(on)}$ varies with gate-drive), effectively lowering the beta of Q2. Consequently a higher anode voltage is required to satisfy the loop gain criteria. This is illustrated in Figure 8-21c (R1 = 100 k) where V_{AK} does not drop as low as in Figure 8-21a (R1 = 100 Ω).

The conclusion is that rather than have a larger charging current capability, a lower one is more desirable. Second, the lower current (larger gate-series resistance) is more compatible with the output sourcing capability of standard CMOS gates; the less current that is sourced, the higher the CMOS high level output voltage will be due to the

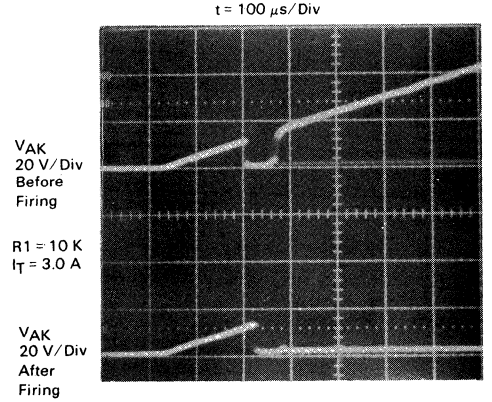


FIGURE 8-22 — ANODE-CATHODE VOLTAGE WAVEFORMS OF THE MOS SCR

$r_{DS(on)}$ I_{OH} voltage drop. This allows the high logic level output to be used for driving other CMOS logic, if so required.

However, the high gate impedance can create dv/dt problems. As in any semiconductor, be it a FET, bipolar or SCR, the junction capacitance (C_{ds} in Figure 8-19b) can couple into the input circuit of the device a capacitive current when a fast, positive going step function of voltage is applied to the output. If this current, or resulting voltage is large enough, the device can be inadvertently turned on. To minimize the dv/dt effect, the gate of the MOS SCR should be terminated in an impedance (similar to the gate-cathode resistance of a sensitive gate SCR or gate-source resistance of a power MOSFET).

The resistance bypasses the capacitive current from the input of the device, the lower the resistance, the greater the degree of shunting. Thus with lower resistance, the MOS SCR will have greater dv/dt immunity and consequently higher blocking voltage capability. This effect is illustrated in the curve of Figure 8-23 whereby a 150 V step function with controlled dv/dt is applied to the anode (through a limiting resistance) of the MOS SCR. The gate-cathode resistance is varied and the maximum dv/dt for that condition is noted. Typically, with a 1.0 k resistor, the device will block 150 V/μs and a 10 k resistor, about 10 V/μs. The 1.0 k gate-cathode resistor will also ensure peak forward blocking voltage V_{DRM} of 600 V peak, 60 Hz.

Thus, for an optimum CMOS-MOS SCR drive circuit, two impedance conditions should be satisfied:

1. The gate circuit should limit the degree of the MOSFET turn-on;
2. The gate-cathode impedance should be low to increase the device blocking voltage capability.

But how large should this limiting impedance be before the charging of the gate capacitance results in unacceptable delay times? To determine this, the circuit of Figure 24 was fashioned using a resistor, speed-up capacitor, and/or reverse diode combinations as the gate limiting impedance. The resistor R limits the gate overdrive; the diode D provides the low impedance gate-cathode path through the $r_{DS(on)}$ (typically 200 Ω) of the N-channel portion of the CMOS when its output is low (MOS SCR is off) and the speed-up capacitor produces just enough gate current peaking to minimize MOS SCR turn-on delay time when narrow input pulses are used (<5.0 μs). Using various combinations of resistor R (1.0 k to 100 k) and/or capacitor C (0.001 μF and 0.01 μF), but always with diode D, an optimum network was achieved — one that is compatible with the output sourcing limitations of the CMOS. With R = 10 k, C = 0.01 μF, the following turn-on times were achieved:

t_d = 40 ns

t_r = 80 ns

For this exercise, the anode supply voltage was a 150 V pulse with a dv/dt of 150 V/μs.

Anode voltage for this resistive load and gate voltage and current waveforms for the optimum drive circuit are shown in Figures 8-25a and 8-25b. Note that although the peak gate current is about 40 mA for about 1.0 μs, being limited by the $r_{DS(on)}$ and transconductance Y_{fs} of the CMOS gate, it is well within its CMOS average power limits.

The same gate-drive circuit was then used to fire an ac

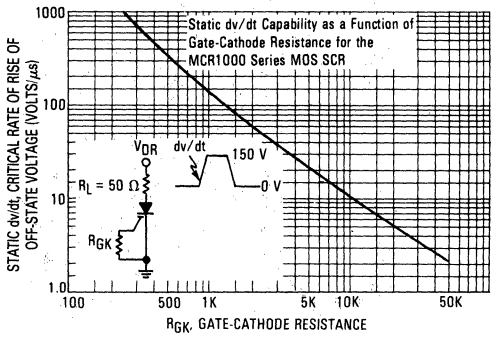


FIGURE 8-23 — TYPICAL dv/dt CAPABILITY OF THE MCR1000 MOS SCR

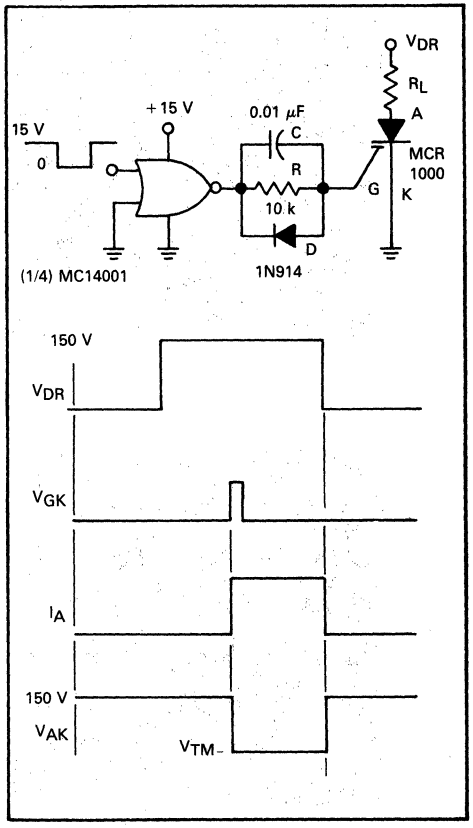


FIGURE 8-24 — PREFERRED CMOS DRIVE CIRCUIT AND WAVEFORMS

load at peak line voltage; the resulting turn-on times were the same as in the pulsed dc test. The gate pulse was then advanced to the zero voltage crossing of the ac line and the point at which the MOS SCR just fired was noted. The anode voltage at which this occurred was typically 15 V, resulting in an effective gate pulse width for this circuit of about 240 μs, (phase delay of 5°).

Finally the MOS SCR was characterized for its commutation time t_q; the test conditions were R_{GK} = 1.0 k, I_{TM} = 3.0 A, dv/dt = 100 V/μs. The typical commutation time was:

t_q = 6.0 μs

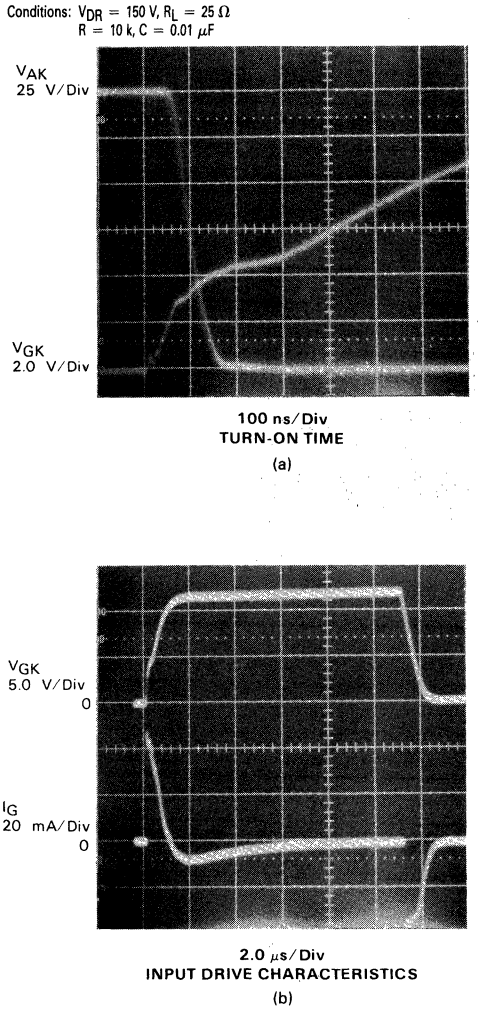


FIGURE 8-25 — SWITCHING CHARACTERISTICS OF THE MCR1000 WITH THE PREFERRED GATE-DRIVE CIRCUIT

APPLICATIONS OF THE MOS SCR

The following circuits illustrate the unique characteristics of the MOS SCR: high input impedance (low drive power), fast turn-on, and latch capability.

DC Static Switch

When an SCR, MOS or bipolar, is used in a dc circuit, some means is required to turn the device off. An example of a dc application using the MOS SCR being turned off is shown in Figure 8-26. For this illustration, the loads in the respective anode circuits of the two MOS SCR's are equal, resulting in a power flip-flop. They can be unequal, if so required, with the lighter load simply being the commutating source. Assuming that MOS SCR (Q1) is initially on, the commutating capacitor C will be charged through R_{L2} and R_S to the supply voltage V_{DR} (minus the "on" voltage V_{TM} of Q1); the capacitor is thus charged; negative on the left plate, positive on the right. When Q2 is then turned on, the right plate is pulled to near ground and since the voltage across the capacitor cannot change instantaneously, the left plate will consequently be pulled below ground. This momentary reverse bias of the anode of Q1 commutates the device off. The commutating capacitor will now start to charge up through R_{L1}, producing the exponentially rising voltage V_{D1} (Figure 8-27). To ensure stable commutation, the time required to charge up to zero volts should be greater than the t_q of the device.

In the example shown (R_{L1} = R_{L2} = 50 ohms, C = 0.22 μF), the time was about 6.0 μs, satisfying the t_q requirements of the MOS SCR. The maximum operating frequency is also dictated by the RC time constant, as the capacitor should be near full charge before the next cycle begins. The series resistor R_S limits the initial capacitor dump current as shown by the I_A waveform of Figure 8-27.

A simple and inexpensive circuit for toggling the flip-flop, one that uses a CMOS quad, 2 input NOR gate, is shown in Figure 8-26. Gates G1 and G2 comprise an astable multivibrator running at about 13 kHz with the duty cycle being set by potentiometer R1.

Gate G2 provides the buffered drive to MOS SCR Q1 and also the complementary drive through G4 to Q2. Both gate drivers are configured with the optimum circuit previously described. Thus, using MOS SCRs, a low drive power, fast turn-on, power flip-flop was readily achieved.

AC Static Switches

Examples of how the MOS SCR can be used in ac applications are shown in Figures 8-28 and 8-31. The first circuit, an ac power switch (Figure 8-28), uses a MOS SCR connected across the dc output of a rectifier bridge to switch an output ac load. The bridge rectifies the input ac, allowing the one MOS SCR to control both half-cycles of the input signal. As in the other examples, the gate of the MOS SCR is driven by a ground referenced CMOS gate, which means the power circuit must be floating (the alternative is to float the gate driver, and ground-reference the ac circuit). For gate full-wave rectified applications, the load should be placed in series with the MOS SCR across the bridge dc output terminals. Examples of both gated ac and full-wave rectified output waveforms are

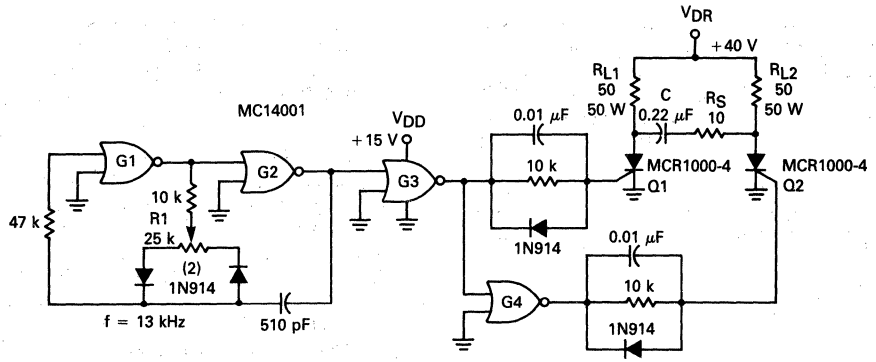


FIGURE 8-26 — POWER FLIP-FLOP USING MOS SCRs

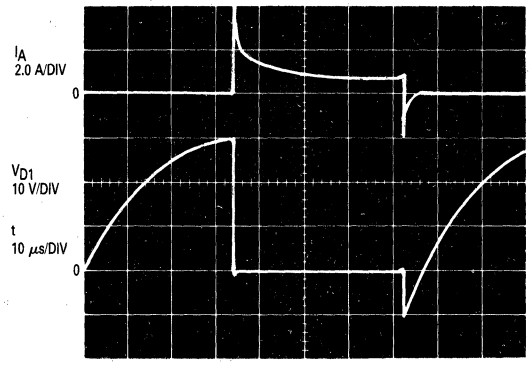


FIGURE 8-27 — OUTPUT WAVEFORMS OF POWER FLIP-FLOP

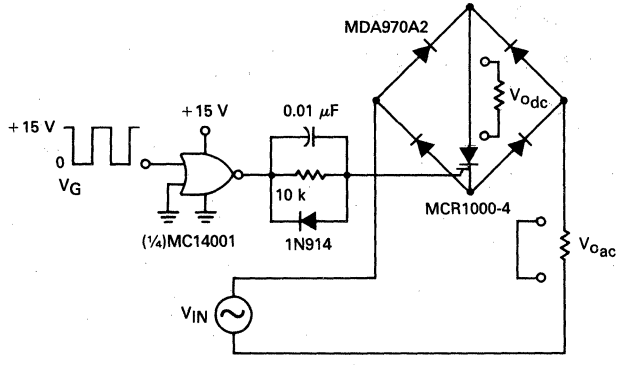


FIGURE 8-28 — AC POWER SWITCH USING THE MOS SCR

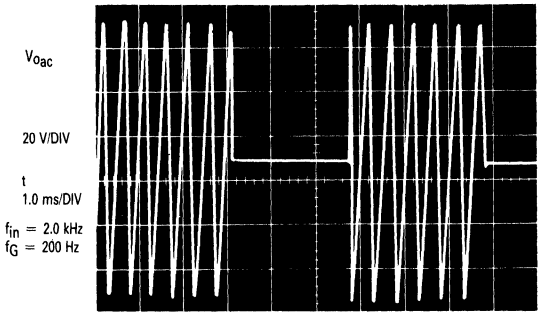


FIGURE 8-29 — OUTPUT WAVEFORM OF AC POWER SWITCH

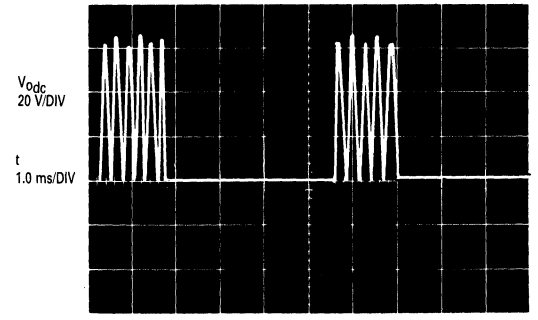


FIGURE 8-30 — GATED FULL-WAVE OUTPUT OF AC POWER SWITCH

shown in Figures 8-29 and 8-30 for the respective configurations where a 2.0 kHz signal is gated by a 200 Hz signal.

When higher frequencies have to be gated or modulated, particularly with inductive loads, then the two SCR configuration of an ac power switch (Figure 8-31) should be considered. Since each device is only operating for half of a cycle, the circuit commutation turn-off time t_q becomes the limiting parameter for high frequency operation.

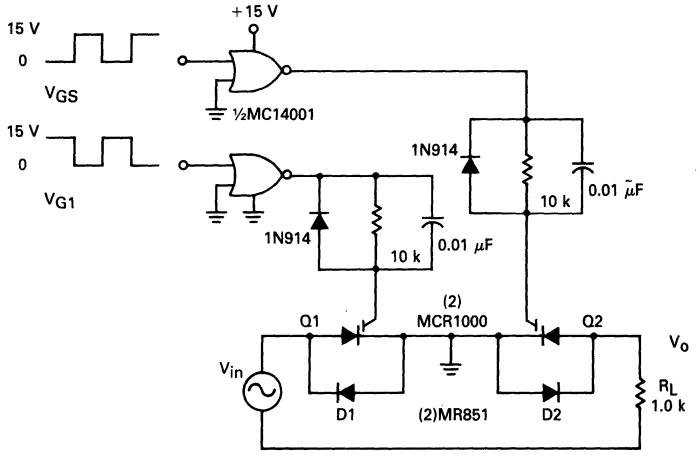


FIGURE 8-31 — BIDIRECTIONAL POWER SWITCH USING TWO MOS SCRs

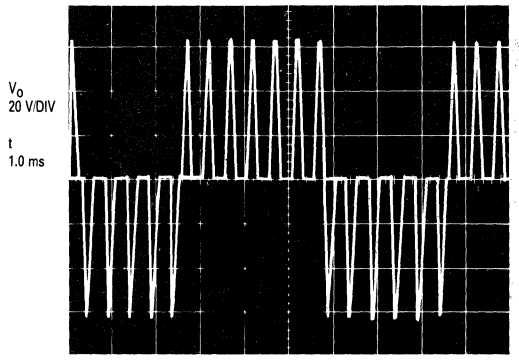


FIGURE 8-32 — 2.0 kHz SIGNAL GATED BY 200 Hz

The two MOS SCRs are driven in push-pull using the same CMOS drive circuits described in Figure 8-26. Consequently, when the ac input goes positive, and MOS SCR Q1 is turned on, the signal will be conducted to the load through diode D2. In a like manner, the negative-going signal will flow through D1 and Q2. An example of the output waveform that can be achieved is shown in Figure 8-32 where a 2.0 kHz input signal is gated by a 200 Hz control signal.

All of ac switches described were powered by a signal generator whose maximum peak output was 60 V into a 1.0 k load. This is not the power limitation of the circuit; the limitations are the MOS SCR which for the MCR1000 family is a V_{RRM} of 100 V and an anode current I_A of 15 A RMS.

IC Driver

Drivers for the MOS SCR are certainly not limited to only CMOS gates; in fact, any semiconductor device, or even mechanical switch, that satisfies the gate-impedance requirements can suffice. In Figure 8-33, an op-amp is used to interface between a fiber optic system and the MOS SCR to multi-cycle, half-wave control of a load. For this application, a 10 V power supply was available, large enough to drive the MOS SCR gate, but too large to power the MFOD405F fiber optics integrated detector/preamplifier (receiver) whose maximum V_{CC} is 7.5 V. This receiver has two complementary outputs, one at a quiescent level of about 0.6 V and the second at 3.0 V. By adding a 4.7 V zener in series with the return bus, the effective V_{CC} becomes 5.3 V and also the 0.6 V output level is translated up to about 5.3 V. This level is now compatible with the reference input (5.9 V) of the single-ended powered op-amp acting as a comparator.

Under no-signal conditions (fiber optic emitter de-energized), the receiver output is lower than the op-amp reference and, consequently, the op-amp output is high, turning on the MOS SCR. When the emitter is energized, the receiver output goes more positive, exceeding the reference to the op-amp and causing its output to switch low to near ground. The reference voltage should be compatible with the fiber optic sensitivity; for this illustration, pulsing the emitter with about 80 mA and using a one-meter fiber length resulted in a receiver output pulse of about 1.0 V. To ensure that the MOS SCR is cut-off, two diodes (D1 and D2) are placed in series with the gate. Thus, by varying the duty cycle to the emitter, the MOS SCR power controls the load on a multicycle, half-wave basis, but it can also be used in phase-control applications. Diode D3 is used to block the peak negative half of the ac input which would exceed the V_{RRM} spec of 100 V. The load can be resistive, a light dimmer as an example, or inductive. As with any thyristor inductive load, a snubber network may be required to minimize the dv/dt effects of that type of load.

CROWBAR

Another application which should serve the fast turn-on capability of the MOS SCR is as a crowbar. Experimentation has shown that the device can dump an 8,000 μF capacitor (simulating the output filter capacitor of a linear power supply) charged to 20 V with 0.1 Ω current-limiting resistance in the discharge path. The end result is peak-current pulse of about 140 A, decaying exponentially to its 10.0% value in about 3.5 ms. Related specifications of the MCR1000 family of MOS SCR's are: peak

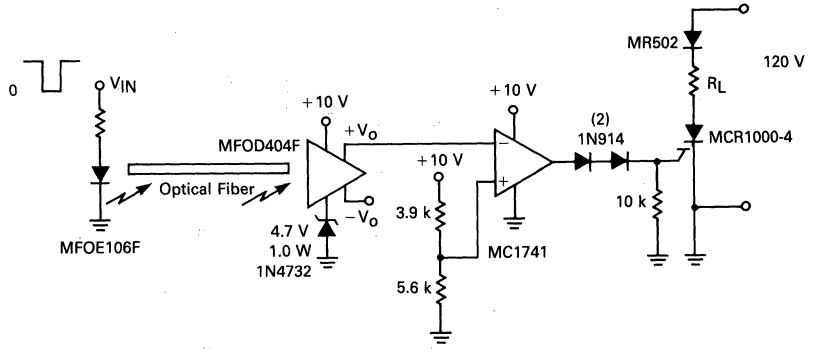


FIGURE 8-33 — OP-AMP GATE DRIVER IN A FIBER OPTIC SYSTEM

forward surge current I_{TSM} of 90 A and an I^2t rating of $34A^2S$.

In summary, the MOS SCR is a new device combining the properties of power MOSFETs and SCRs high input impedance, fast switching and latching action. It is easily driven by low power logic — CMOS in this case — but the driver can be any IC or circuit with pull-down (sinking) capability. Gate current can be limited to tens of microamps, if required, but switching speed trade-off must be made at these low currents. To ensure high blocking voltage and dv/dt immunity, the gate cathode should be terminated in a relative low impedance. A simple, inexpensive method of accomplishing this is to use the CMOS low-level output and a reverse diode.

Chapter 9: Relative Efficiencies of TMOS and Other Semiconductor Power Switches

The prime requisite of a power switch (semiconductor or mechanical) is to transfer the maximum power to the load. A comparison of the relative efficiencies of various power semiconductor switches will be demonstrated with three different switching loads: resistive, inductive and a dc motor.

There are four factors that contribute to the system losses: input or driving power losses due to the input current and/or voltage required to turn on the device; saturation or static losses when the device is ON (a product of the on-voltage and current); switching or dynamic losses that result from the transition times when the device is turned ON and OFF; and off losses due to the product of leakage current and the power supply voltage. Generally off losses are by far the least significant since modern semiconductors have low leakage currents and can be ignored in system loss calculations.

The variation of input power losses can be substantial for the various semiconductors. As an example, a high voltage switching transistor would have relatively low current gain and, consequently, requires relatively high input base current to turn it fully on whereas a MOSFET, with its extremely high static input impedance, would require very little input power to turn it on.

The output power losses are illustrated in Figure 9-1. It is apparent that the switching losses, depending on the switching frequency and transition times, can contribute a large share of the total system losses. Thus, for high frequency applications, where switching losses predominate, fast switching devices should be used. Conversely, for low switching frequency applications, low on or saturation losses are more important.

Power MOSFETs are recognized as being extremely fast switching devices, but are they more efficient than bipolars in all or many swithcing applications? The answer is — it depends. Efficiency is a measure of dissipation, which, in Switchmode circuits, consists primarily of switching losses, both turn-off and turn-on, and saturation losses. Since switching losses are a function of the switching frequency and saturation losses are relatively constant, a point is reached in the frequency spectrum where one loss predominates over the other. Thus, in low frequency applications, devices with low saturation or on-voltage would show lower losses as measured by the device case temperature, and at high frequencies, the fast switchers would run cooler. This applies to all types of semiconductors, be they power MOSFETs, Bipolars, Darlingtons, GTO (Gate Turn Off) SCRs or a GEMFET (Gain Enhanced MOSFET) (A standard SCR can also be used wiith commutating circuitry; however, it is not included in this evaluation due to the additional circuit requirements and associated costs.)

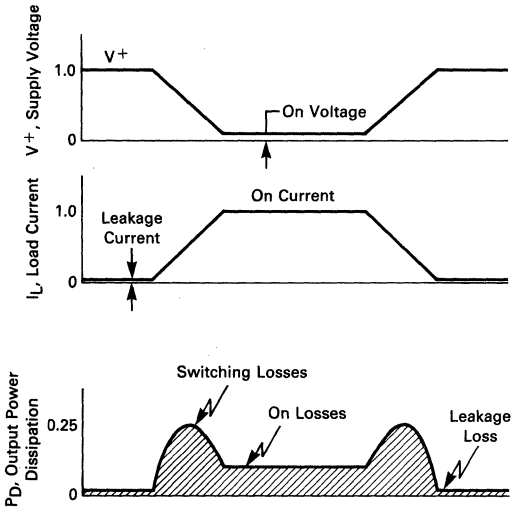


FIGURE 9-1 — NORMALIZED SWITCHING WAVEFORMS FOR A RESISTIVE LOAD

Temperature Testing High Voltage Devices TMOS versus Bipolar SMI and III

A simple way of measuring the relative efficiencies of the DUTs, one that measures the total device losses, is by measuring the case temperature. This is accomplished by attaching a thermocouple to the mounting flange of a TO-204 (TO-3) package or tab of a plastic (TO-220) package. The first evaluation was to compare the switching efficiency of three high voltage switching transistors — the 2N6545, one of the first transistors characterized for Switchmode applications, called Switchmode I, (SMI); the MJ16004, a state-of-the-art Switchmode III Transistor (SMIII) designed for higher frequencies; and the Power MOSFET MTM5N40. All these devices are of similar die size and have similar ratings (Table 1). All were tested with nearly identical loads and were driven by the same test circuit, except that the forward input current (I_{B1}) and input resistance were scaled for the particular DUT). Reverse current or turn-off current was derived from the same input clamp transistor switch and the magnitude of this current (I_{B2}) was dictated by the stored charge of the device under test (DUT).

Since the input drive for both turn-on and turn-off can be chosen to optimize the switching speed, the drives selected were those generally shown on the data sheet; i.e., forced gains of 5.0 and 7.0, respectively, for the 2N6545 and the MJ16004; off-bias voltages of −5.0 V and −2.0 V for the above; and a gate-drive of greater than 10 V for the MTM5N40.

Resistive loads were chosen for the temperature rise-versus-frequency test since the load current could be maintained at a constant 2.5 A as the frequency was varied. Recognizing that the "real world" load is usually inductive and that inductive turn-off switching losses are greater than turn-on due to the rectangular load line, a single frequency (75 kHz) inductive test was also run. Due to the different on-voltages and turn-off times for Bipolar and MOSFET devices, the load inductances had to be slightly different to achieve the same peak collector (drain)

TABLE 1 — Specifications of DUTs

	SMI 2N6545	SMIII MJ16004	TMOS MTM5N40
Die Size (Area)	160x160 mil (25600 mil^2)	157x175 mil (24649 mil^2)	126x182 mil (22932 mil^2)
I_C, I_D	8.0 A	5.0 A	5.0 A
V_{CEO}, V_{DSS}	400 V	450 V	400 V
$V_{CE(sat)max}$, $V_{DS(sat)max}$	1.5 V @ 5.0 A	2.5 V @ 3.0 A	2.5 V @ 2.5 A, $r_{DS(on)}$ max = 1.0 Ω
$V_{CE(sat)typ}$, $V_{DS(sat)typ}$	0.3 V	0.3 V	2.2 V @ 0.9 Ω
$h_{FE(min)}$, $g_{fs(min)}$	7.0 @ 5.0 A	7.0 @ 5.0 A	2.0 mhos @ 2.5 A

currents for a normalized test. For the 75 kHz test, the peak ramp current of about 3.0 A peak was achieved with inductances of 32 μH and 27 μH respectively when V_{CC} and V_{DD} were +16 V.

The temperature rise test fixture (Figure 9-2) consists of a clocked, three-phase counter sequentially driving the three respective switching circuits; thus, each device under test is driven at a 33% duty cycle. However, at high frequencies (low on times), DUTs with greater storage times will effectively be powered for longer duty cycles and therefore have greater saturation losses contributing to the device temperature rise. As an example, at 150 kHz (period of 6.7 μs) the 33% dc drive on-time of about 2.2 μs would result in about 48% power on-time with only 1.0 μs of storage time.

The clocks for this system, one for the resistive load case and the other for the inducutive load, consist of two CMOS gate configured RC astable multivibrators. Switchable timing capacitors set the frequencies for the resistive load at 5.0, 25, 75 and 150 kHz respectively; the inductive load clock is set at a fixed frequency of 75 kHz. The output of these MV's clock the MC14002 Octal Counter Divider connected as a three-phase ring counter whose respective emitter-follower, positive-going outputs control the three virtually identical drivers.

Forward base current for the bipolar transistors is set by turning on the NPN transistors Q2 and Q7 and the following PNP transistors Q3 and Q8. To minimize storage time, Q3 and Q8 are fashioned as constant-current generators, supplying the base currents to the 2N6545

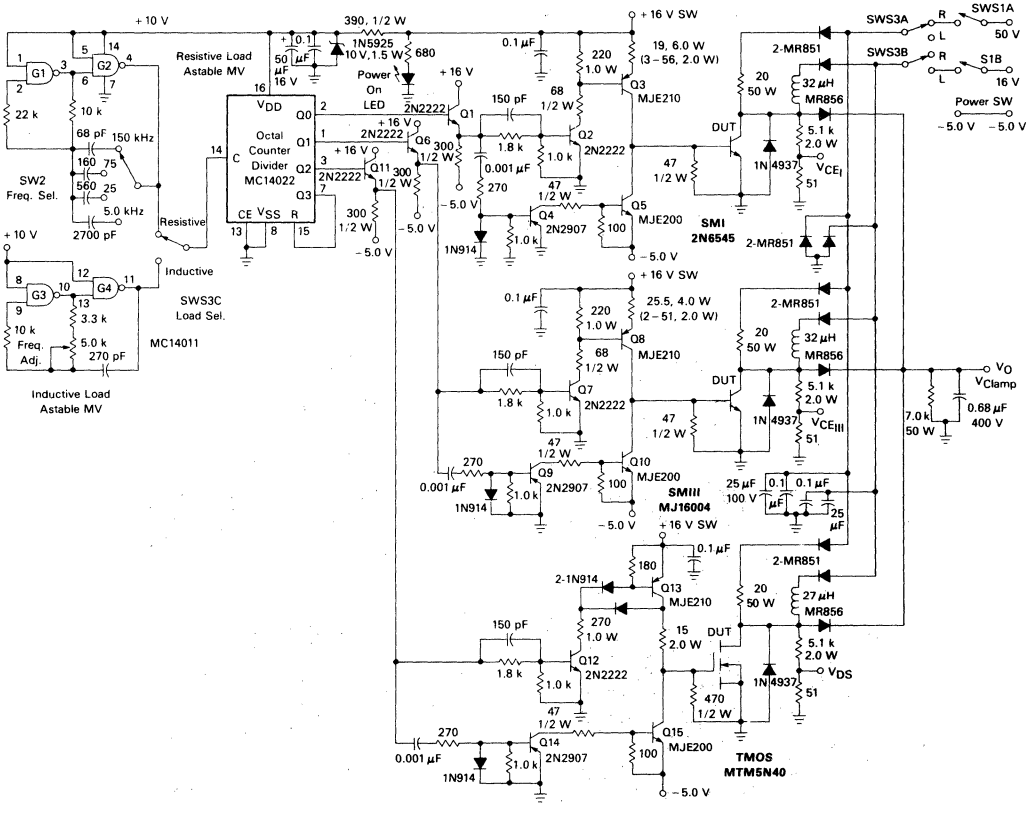


FIGURE 9-2 — TEMPERATURE RISE FIXTURE SWITCHMODE I, SWITCHMODE III, TMOS

($\beta_F = 5.0$, $I_{B1} = 600$ mA) and MJ16004 ($\beta_F = 7.0$, $I_{B1} = 430$ mA) for the inductive load current of 3.0 A peak. Forward gate voltage for the power MOSFET is generated by turning on PNP transistor Q13 (Baker clamped to minimize t_s) and thereby applying nearly the full 15 V rail voltage to the gate. The 15 ohm current limiting resistor provides the low source impedance for quickly charging (and thus switching) the MOSFET input capacitance C_{iss}.

Reverse bias voltage $V_{BE(off)}$ or $V_{GS(off)}$ for rapidly turning off the DUTs, are derived by differentiating the input pulse with the resistor-capacitor networks in the base circuits of Q4, Q9 and Q14. The resulting negative going pulses, which are coincident with the trailing edge of the input pulse, then turns on the following respective PNP transistors Q4, Q8 and Q13 for about 3.0 μs. These transistors then turn on NPN transistors Q5, Q10 and Q15 whose emitters are referenced to a negative power supply; thus, the reverse bias voltages and resulting reverse bias currents (I_{B2} for bipolars) are applied to the DUT for the 3.0 μs immediately following the turn-on pulse. This reverse bias voltage can then be varied to determine its effect on switching speeds, power dissipation and case temperature rise. For the following described temperature tests the bias voltages were set for -2.0 V and -5.0 V respectively, the presumed optimum values that are listed in the respective data sheets.

The resistive loads, being somewhat inductive wirewound resistors, have turn-on switching current rise times limited by the L/R time constant (Figure 9-3) and thus independent of input drive. However, the turn-off voltage and current switching times are affected by off-bias (Figure 9-4); thus at optimum bias voltage, the switching losses and therefore case temperature can be minimized. This is quite evident in the curves of Figure 9-5 showing temperature rise versus frequency at two off-bias voltages. All three devices showed slightly lower case temperatures (1.0 to 3.0°C) when the optimum off-bias was used at the higher frequencies where switching losses predominate.

The Power MOSFET also runs cooler at higher off-bias voltage. This is due to the charged input capacitance C_{iss} being discharged more quickly when clamped to a greater negative voltage; thus the turn-off switching speeds are improved.

As expected at low frequencies, where on losses predominate both the 2N6545 (SMI) and the MJ16004 (SMIII) have temperature rises proportional to $V_{CE(sat)}$, both being about 0.3 V at 2.5 A. The Power MOS transistor (TMOS), with a typical on-resistance $r_{DS(on)}$ of about 0.9 ohm [1.0 ohm(max)] has an on-voltage of about 2.2 V at

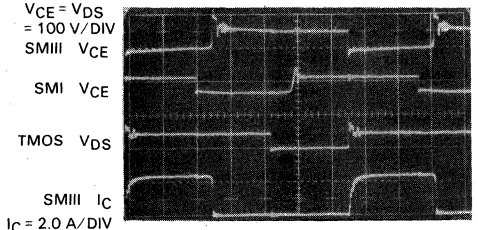


FIGURE 9-3 — RESISTIVE LOAD SWITCHING OF DUTs AT 75 kHz

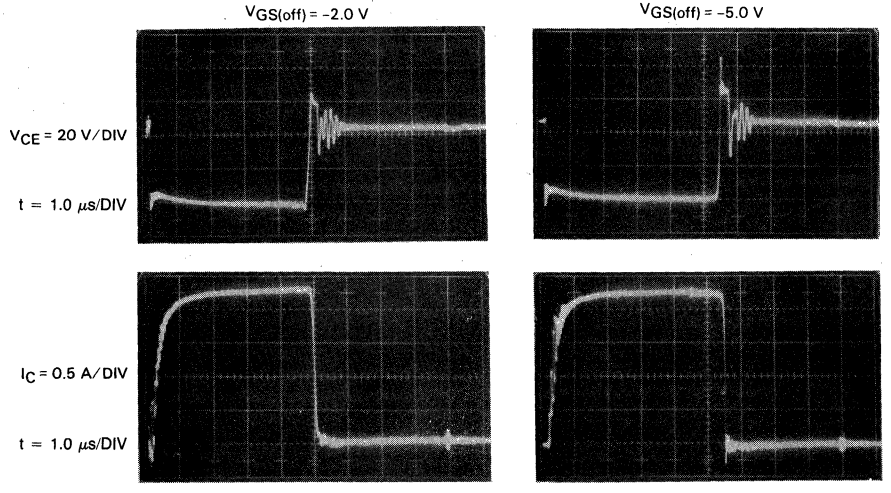


FIGURE 9-4 — RESISTIVE LOAD SWITCHING OF SWITCHMODE III MJ16004 AT TWO OFF-BIAS VOLTAGES

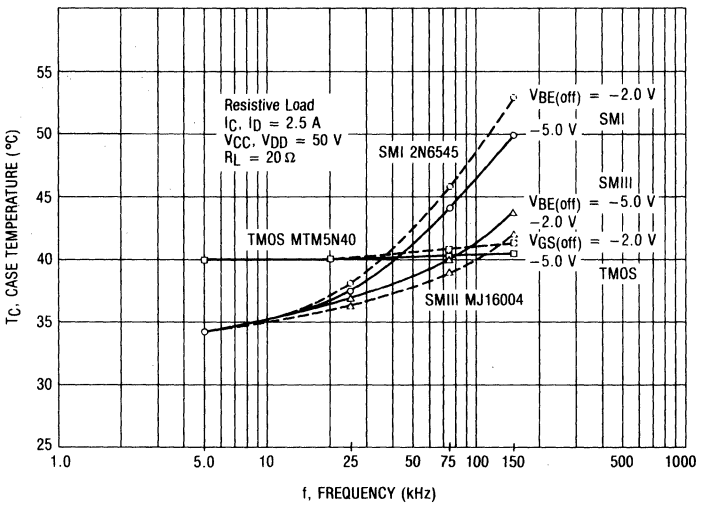


FIGURE 9-5 — TEMPERATURE RISE OF SWITCHMODE DEVICES AS A FUNCTION OF FREQUENCY

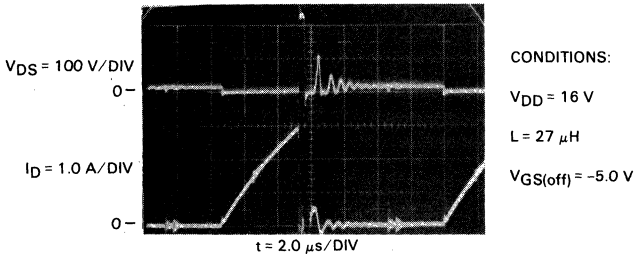


FIGURE 9-6 — CLAMPED INDUCTIVE LOAD SWITCHING WAVEFORMS OF TMOS MTM5N40

2.5 A, resulting in the higher case temperature. As the frequency is increased, the extremely fast switching MOSFET introduces little additional switching losses, resulting in a relatively constant case temperature.

The first generation SMI transistor shows the expected increasing temperature rise with increasing frequencies due to its relatively slow switching speed (the device was designed for 20 kHz applications). By contrast, the Switchmode III Transistor, MJ16004, which was designed for improved operation at higher frequencies with improved reverse bias safe operating area, shows a much lower case temperature rise; in fact, it typically operated cooler than the Power MOSFET up to the 75-100 kHz range.

The illustrated temperature rise curves were derived with typical devices. Testing of about ten sets of devices produced similar results, although in some cases the effects of off-bias were not as pronounced due to slight differences in device processing, temperature measurement repeatability and accuracy, particularly where small differences in temperature had to be determined.

Although the curves show defined temperatures, the magnitude of the rise is only relative as it is obviously a function of the size and efficiency of the heat sink chosen. For this exercise, small heat sinks were chosen to raise the case temperature for higher differential temperature measurements. Secondly, the heat sinks (both the small ones for the DUTs and the large ones for the resistive and inductive loads) were thermally isolated from each other to minimize mutual thermal coupling effects; (the DUT heat sinks were mounted on ceramic standoffs and the load sinks on plastic washers to reduce thermal conduction to the chassis and hence to each device).

The vertical temperature axis of Figure 9-5 could have been labeled Power Dissipation (P_D), knowing the thermal resistance of the heat sink ($R_{\theta SA}$) used and the relationship between case temperature and thermal resistance ($P_D = \frac{T_C - T_A}{R_{\theta CS} + R_{\theta SA}}$). However, for relative efficiency considerations, measuring the device case temperature will suffice.

For clamped inductive loads, the greatest switching dissipation generally occurs during turn-off where the device, due to the rectangular load line, can be stressed simultaneously with both high current and voltage. The illustrated inductive loads simulate a flyback switching regu-

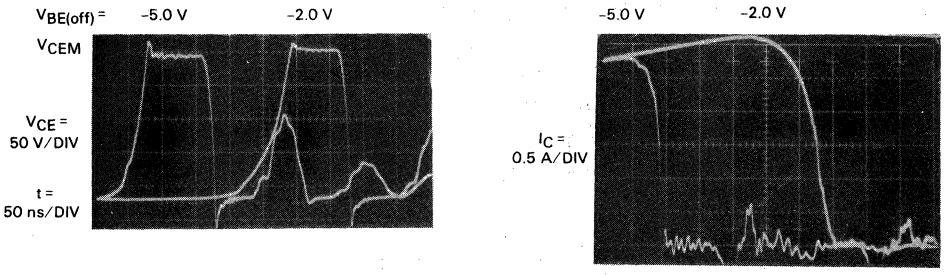


FIGURE 9-7 — CLAMPED INDUCTIVE LOAD TURN-OFF TIMES OF SWITCHMODE I 2N6545 WITH TWO OFF-BIAS VOLTAGES

lator where the energies stored in the inductors when the DUTs are turned on are transferred via their respective clamp diodes to the resistor-capacitor load during turn-off time. By proper selection of this load, the resulting clamp voltage was set for about 250 Vdc. The actual peak collector-to-emitter voltage V_{CEM} overshoot can be somewhat higher, being dependent on the rate of collector current fall time t_{fi}, the forward recovery time of the clamp diode and the degree of proper RF layout (Figure 9-7). It is not uncommon for this overshoot to exceed the clamp supply voltage by 100 Volts.

An example of how reverse bias affects the switching speed, and thus efficiency, of the 2N6545 is shown in the photos of Figure 9-7. Note the difference in t_s, t_{fi}, V_{CEM} and collector-emitter voltage rise time t_{rv}. At the optimum bias of about −5.0 V, the device turns off faster, there is less energy to be dissipated and a lower case temperature results. This is also true of the other two DUTs.

Although there is no "storage time" associated with FETs, there is a turn-off delay time $t_{d(off)}$ due to device capacitances having to be discharged. The photos of Figure 9-8 describe the turn-off times when the off-bias is varied from 0 V, −2.0 V and −5.0 V respectively. As mentioned previously, the greater off-bias results in the lowest turn-off times.

The average temperature rise measurements of the three DUTs for the inductive load case (Table 2) illustrates the effect of off-bias on device efficiency.

A direct point-by-point comparison between the inductive load and resistive load tests at 75 kHz can't be made since the respective load currents, and thus power dissipation are not the same. However, the trends can be compared; i.e., for the inductive load test, a greater temperature differential resulted between the optimum off-bias voltage and the second tested voltage, being as high as about 15°C for SMI. By comparison, the resistive load test showed only a few degrees difference. This is due to the change in turn-off switching time having a greater effect on the more energy stressful inductive load switching than on the resistive load.

In addition to driving the bipolar devices with the recommended forced beta, β_F of about 5.0 and 7.0 respec-

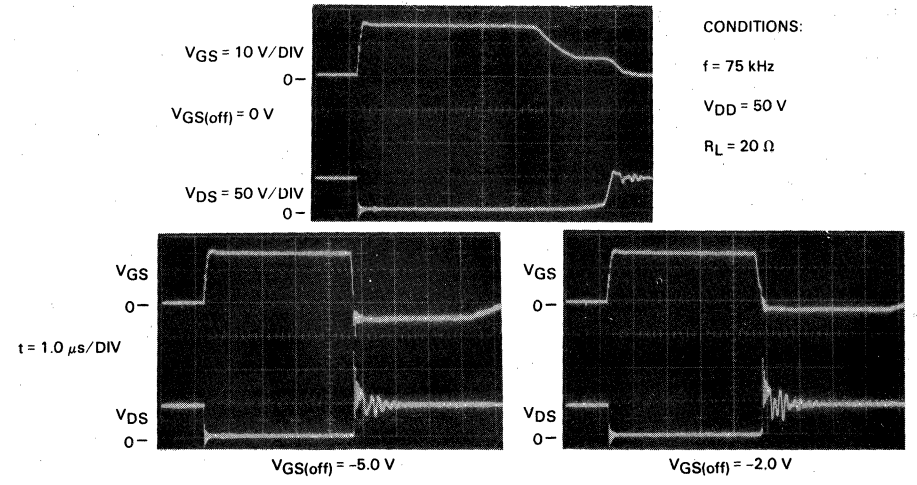


FIGURE 9-8 — THE EFFECT OF OFF-BIAS VOLTAGE $V_{GS(off)}$ ON TURN-OFF TIMES OF TMOS MTM5N40, RESISTIVE LOAD

TABLE 2
Temperature Rise of an Inductive Load
f = 75 kHz, I_{CM} = 3.0 A, V_{CEM} ≅ 250 V

Off-Bias Voltage	Case Temperature		
	SMI	SMIII	TMOS
-2.0 V	58°C	34°C	42°C
-5.0 V	43°C	39°C	38°C

tively for the 2N6545 and MJ16004, a brief test was conducted by reversing β_F (7.0 and 5.0 respectively). Although the dynamic saturation characteristic of the bipolars changed subtly due to different base drive, and the turn-off switching time (even with off-bias) changed by only a second order, the change in power dissipation was minimal, if any. Within measurement repeatability, the resultant case temperatures were about the same, suggesting no great requirement of maintaining a defined β_F.

Examination of the above test results, the resistive temperature curves and the photos of the switching waveforms lead to the following conclusions about the switching efficiency of the test devices:

- The temperature rise results are a measure of total device dissipation, including the input drive loss.
- The fast switching speeds of TMOS coupled with the low drive power requirements and relatively simple drive circuitry make the MOSFET an attractive high frequency device.
- Power MOSFETs become more efficient at frequencies beyond about 100 kHz when compared to the new generation of switchmode bipolar transistors.
- Power MOSFETs have lower $t_{d(off)}$ when sufficiently reverse biased than bipolar t_s, thus allowing a higher operating frequency.
- At low frequencies, ON (static) losses predominate; thus bipolars are presently more efficient than comparably sized first generation Power MOSFETs. Technology advancements of Motorola Power MOSFETs have been made to significantly reduce the on-resistance, $r_{DS(on)}$ to make these devices competitive with the bipolars.
- Switchmode III MJ16004 compares favorably to Power MOSFET MTM5N40 at 75 kHz with an off-bias of −5.0 V and generally runs cooler at the optimum bias of −2.0 V (relative to −5.0 V for TMOS). Although not described in this text, the SOA of SMI & SMIII is not as large as TMOS.
- For "real world" inductive loads, where the turn-off switching losses predominate, insufficient off-bias can produce higher case temperature rise for SMI transistors due to slower turn-off switching speeds (e.g., @ 75 kHz T_C = 58°C for $V_{BE(off)}$ = −2.0 V compared with 43°C for −5.0 V).
- Optimum off-bias will reduce turn-off switching times and thus switching losses for the bipolars and FET, but does not necessarily minimize the storage time (e.g., for SMIII $t_{fi(min)}$ and $t_{s(min)}$ occur at about −2.0 V and −5.0 respectively.
- Under optimum off-bias voltage condition, the t_f of SMIII approaches that of the very fast TMOS, however, drive power is high.
- Switchmode I 2N6545 can be comparably operated to 75 kHz when there is sufficient off-bias voltage (or reverse base current), approximately −5.0 V.
- Storage time, when it is not compensated for by circuit feedback techniques, somewhat affects efficiency at high frequencies due to increased ON losses.
- Specified force beta β_F of the bipolars are not too critical for efficiency considerations as the turn-on times are partially dictated by the load. Off-bias tends to minimize the storage time effects as β_F is varied; however, excessive overdrive can cause I_C tail lifts during turn-off which may contribute to larger temperature rise.

Low Voltage Devices: TMOS versus Bipolar, Darlington and GTO Devices

PWM DC Motor Controller Test

The load used in this test is a dc motor whose speed is controlled by PWM. Consequently, when narrow pulse widths are applied — low speed — the back emf is low and the load current (collector, drain or anode current) is high, about 11 A. To ensure device saturation under this worst case condition, adequate input current must be applied. For the devices tested, the forward input current for the bipolar, Darlington, TMOS and GTO were about 700 mA, 100 mA, 1.0 mA, and 120 mA, respectively.

Due to the motor time constant, the switching frequency was set for about 100 Hz and the min/max duty cycles were about 8% and 70% respectively. At this low frequency, the use of off-bias for the bipolar, Darlington and TMOS produces negligible improvement in efficiency as the decrease in turn-off time is extremely small for the time frame involved. However, the GTO does require off-bias which for this test circuit and DUT was as much as 2.2 A lasting for about 10 μs. This turn-off power should

be considered in the efficiency calculations. At low frequencies, it is relatively small, but as frequency increases, it can become substantial (refer to Figure 9-10 for drive circuits and input power equations).

The bipolar, Darlington, and TMOS are turned on by the input pulse whose width is a function of the required motor speed, whereas the GTO is turned on by a relatively narrow, positive gate current pulse and turned off by a narrow, negative gate current pulse. As the frequency is increased it is apparent that the GTO input power increases and will reach a point where its input power is greater than that of the bipolar or Darlington. This crossover frequency is a function of the power supplies used and the particular duty cycle chosen. As an example, for a 50% duty cycle with the illustrated power supplies, this crossover point between the Darlington and GTO would be about 2.0 kHz.

TEST CIRCUIT ANALYSIS

The test circuit, shown in Figure 9-9, consists of a two gate CMOS, astable multivibrator (MV) clocking a CMOS configured monostable multivibrator (MV) to produce the approximate 100 Hz, variable pulse width output. Darlington transistor Q1 furnishes the buffered output to drive the two channels of the power amplifier, with transistors Q2 and Q3 supplying the positive input current to the DUT and Q4 and Q5 the negative current. When the DUT Selector Switch S1 is in positions 1, 2, or 3, the full pulse width will be applied to the DUTs as differentiating capacitor C1 is shorted out. Thus, positive input current is generated by the direct coupled pulse turning on the NPN transistor Q2 and the following PNP transistor Q3 connected, in positions 1, 2, and 4, as a constant current source. The respective emitter resistors set the current I_{B1} or I_{GT} for the DUTs. Negative current is derived by differentiating the input pulse with C2, R2 and using the negative going, trailing edge pulse for turning on the following PNP transistors Q4 and NPN clamp transistor Q5. Thus, an off-bias voltage (clamped by diodes D1 and D2) is supplied to the selected DUT. If required, the off-bias can be removed by the Negative Bias Switch S2.

The GTO requires only a relatively narrow positive gate current pulse to turn it on. This pulse is derived from the differentiating network C1, R1 (switch S1A open), with the positive going, leading edge pulse turning on Q2 and Q3. For the component values shown, a turn-on, positive drive current pulse I_{GT} of about 120 mA in amplitude and 40

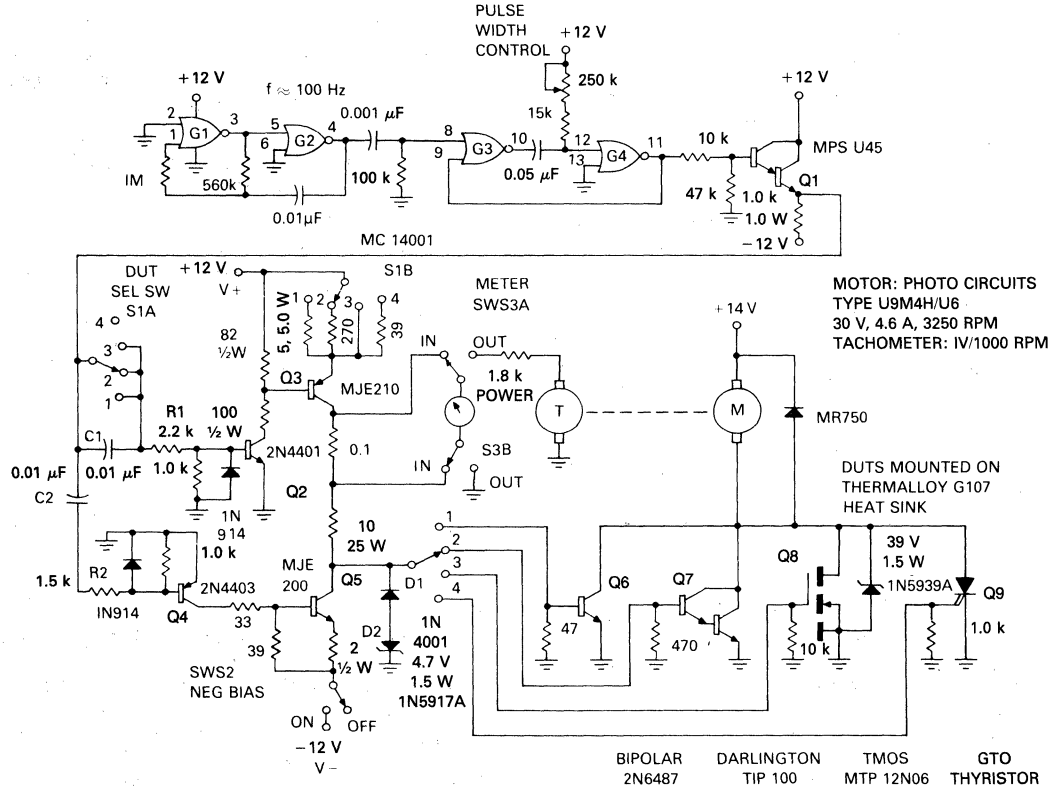


FIGURE 9-9 — TEST CIRCUIT FOR MEASURING RELATIVE EFFICIENCY OF DUT

μs wide is generated, followed by an approximate −6.0 V, 35 μs wide turn-off voltage pulse that is coincident with the trailing edge of the input pulse. This voltage pulse produces a reverse current I_{GR} of about 2.2 A for 10 μs (anode current of about 11 A) when the stored charge is depleted. Obviously, if no reverse bias is applied (Switch S2 open), the GTO will lose control, always being on, and the motor will run at its maximum speed.

RELATIVE EFFICIENCY MEASUREMENT OF DUTs

In order to measure the relative efficiencies of the DUTs, both input power and output power are recorded. This is simply done by switching in a current meter to measure the average input current, or a voltmeter to measure output RPM by means of a tachometer coupled to the motor. The output voltmeter, in effect, measures the relative saturation loss of the DUT since this voltage is subtracted from the applied motor voltage and, consequently, the motor speed will be indicative of this loss. Only the relative positive input current is measured as the reverse currents at this low frequency contribute very little additional drive power. However, as the power equations note in Figure 9-10, with increased operating frequency, this off-bias power can be substantial.

The relative efficiency measurements for the four DUTs are listed in Table 3. Of interest, in regard to efficiency, are the measured input currents (both pulsed and relative average), and tachometer outputs, on-voltages and case

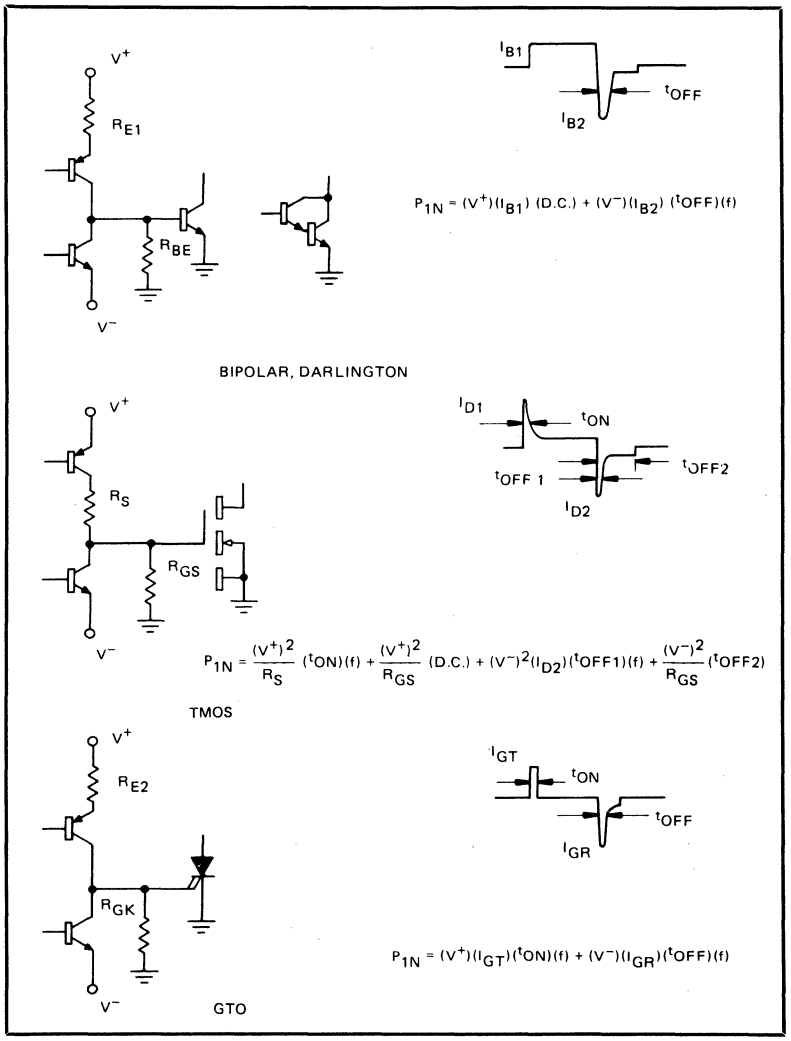


FIGURE 9-10 — DUT DRIVE AND INPUT POWER CALCULATION

temperatures. Within measurement repeatability, the DUTs with the highest on-voltage had the lowest relative output power due to reduced motor voltage and the case temperature rise correlated with the total power dissipation (input plus output). These readings generally confirmed what was expected:

TABLE 3 — Relative Efficiency Measurement of DUTs

DUT	Bipolar 2N6487			Darlington TIP 100			TMOS MTP12N06			GTO Thyristor		
Die Size (MIL)	110 x 130			120^2			120^2			180^2		
Voltage Rating	60 V			60 V			60 V			300 V		
Current Rating	15 A			8.0 A			12 A			10 A		
Switching Speeds (Relative)	Medium			Medium			Fast			Slow		
Input Current, (Forward/(P.W.)	700 mA			100 mA			1.0 mA			120 mA (40 μs)		
Input Current, Reverse/(P.W.)	1.0 A @ I_{MAX} (0.2 μs)			0.4 A @ I_{MAX} (0.1 μs)			0.2 @ I_{MAX} (0.1 μs)			2.2 @ I_{MAX} (10 μs)		
Duty Cycle	8%	12%	56%*	8%	12%	81%*	8%	12%	74%*	8%	12%	68%*
Load Current, Peak	11 A	5.0 A	0.9 A	11 A	5.0 A	0.9 A	11 A	5.0 A	0.9 A	11 A	5.0 A	0.9 A
Power In (Relative)	5.0	13	75	3.0	4.0	11	1.0	2.0	2.0	1.0	2.0	2.0
Power Out (Relative)	20	59	85	16	57	84	17	59	87	17	55	84
$V_{(on)IN}$	1.9 V	1.3 V	1.0 V	2.8 V	2.0 V	1.6 V	12 V	12 V	12 V	1.4 V	1.2 V	0.85 V
$V_{(on)OUT}$	1.2 V	0.4 V	0.12 V	2.1 V	1.3 V	0.78 V	1.7 V	0.9 V	0.15 V	2.0 V	1.5 V	1.0 V
Case Temp	36.6°C	32.9°C	38.3°C	43.6°C	41.3°C	40.4°C	42.3°C	36.0°C	29.5°C	39.5°C	41.1°C	38.2°C

*Clock varied with temperature

TMOS MTP12N06
At low frequency and low motor current, the TMOS is the most efficient device. Its input drive power is extremely low and its On voltage, due to the zero offset, relatively linear $r_{DS(on)}$ is low.

BIPOLAR 2N6487
The bipolar, with its low $V_{CE(sat)}$, has low output dissipation but its input power is the highest to satisfy high collector current — forced β conditions.

At medium and high load currents, the bipolar has the lowest On voltage followed by the TMOS with the Darlington and GTO being about equal in third place.

DARLINGTON TIP100
Total device dissipation and thus case temperature rise is due to input and output dissipation. The Darlington, with its high $V_{CE(sat)}$, can still have lower case temperature than the bipolar at some peak collector currents, due to its low drive power.

GTO THYRISTOR (Experimental)
The GTO is extremely efficient at low frequencies from a drive point of view since it requires only narrow turn-on and turn-off current pulses, but becomes less efficient as the frequency increases due to the higher duty cycles involved.

Efficiency as a Function of Frequency Tests

The PMW Motor Control Circuit was tested at a constant, low frequency, so the relative efficiencies measured were primarily due to static (saturation) losses. To determine the effect of the dynamic (switching) losses, which increase with increasing frequencies, the four different devices were tested with a resistive load, using a variable frequency, constant duty cycle (50%) input signal. The load current was set for about 4.0 A (V_{CC} = 28 V, R1≈7.0 Ω) and the same basic test circuit shown in Figure 9-9 was used. Most of the modifications were in the reverse bias circuit, with the off-bias voltage being either 0 V or −5.0 V for the bipolar, Darlington and TMOS tests and −12 V for the GTO.

Transistor Q4 emitter resistor (2.0 Ω) was shorted out to form an off-bias voltage source; Q3 emitter was tied to the +12 V bus to furnish drive to Q4 when $V_{BE(off)}$ was 0 V; and differentiating capacitor C2 was increased to 0.02 μF to allow greater turn-off time for the GTO. Also, the bipolar forward base current was set fo 600 mA, resulting in a β_F of about 7.0.

Test Results

The results of this efficiency versus frequency test, as measured by the case temperature rise using a small heatsink, are shown in Figure 9-11.

TMOS MTP12N06
As expected, the TMOS device ran the coolest at higher frequencies, being very constant in temperatures up to about 10 kHz and then rising slightly thereafter. At low frequencies, where static losses predominate, the TMOS MTP12N06 case temperature was only about 2°C warmer than the bipolar 2N6487, due to the respective saturation voltages of about 0.6 V ($r_{DS(on)}$ Typ = 0.15 Ω) and 0.4 V. Although not shown, increasing the off-bias voltage ($V_{GS(off)}$) from 0 V to −5.0 V showed only about a 2°C improvement at 33 kHz, due to slightly faster turn-off time; otherwise, at lower frequencies, the difference in turn-off time had little effect in case temperature.

BIPOLAR 2N6487
The bipolar transistor 2N6487 showed marked improve-

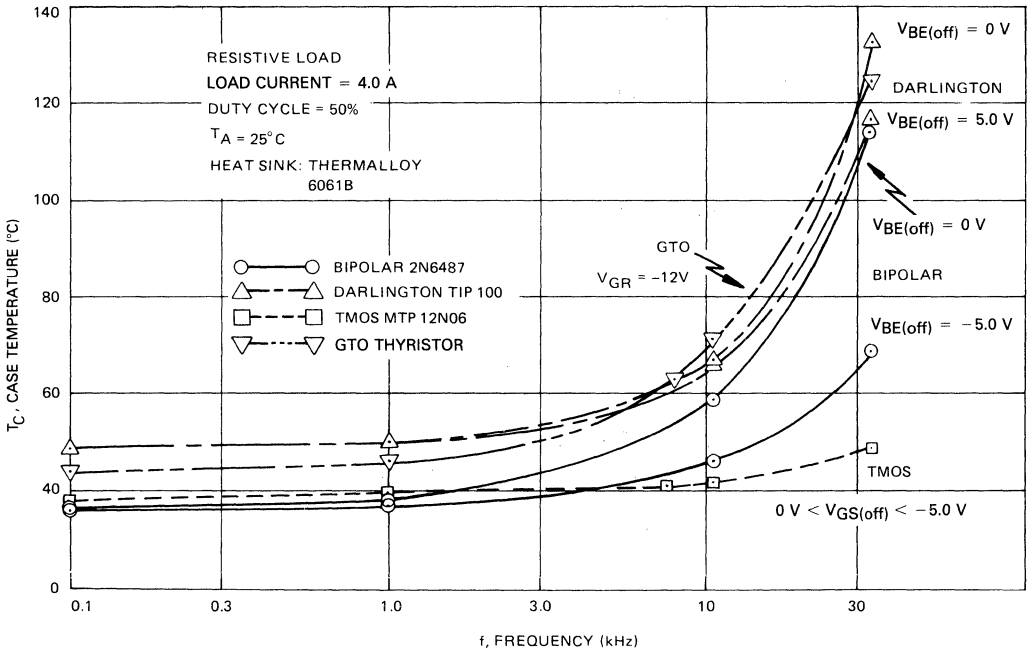


FIGURE 9-11 — TEMPERATURE RISE OF POWER SEMICONDUCTOR AS A FUNCTION OF FREQUENCY

ments in efficiency at the higher frequencies when the $V_{BE(off)}$ was increased from 0 V (base-emitter clamp) to −5.0 V. Without off-bias, the case temperature approached 115°C at 33 kHz, whereas, with −5.0 V, it was only about 70°C.

DARLINGTON TIP100

The low voltage TIP100 Darlington does not have a speed-up diode across its input emitter-base resistor and thus the stored charge of the output transistor cannot be efficiently removed. Consequently, there is no improvement in case temperature at low or nominal frequencies and only some moderate improvement at 33 kHz (117°C relative to 133°C) when the off-bias was increased to −5.0 V.

The Darlington, with the highest saturation voltage of the four devices, not surprisingly, had the highest case temperature at low frequencies and, beyond 5.0 kHz, was about as inefficient as the GTO.

GTO (EXPERIMENTAL)

The experimental GTO exhibited static losses somewhere between the bipolar and the Darlington due to its on-voltage of about 1.2 V at 4.0 A. The device did perform at 33 kHz, however, its case temperature rose to about 125°C. This was due to its relatively slower switching times, as shown by the oscillograms in Figure 9-12. Figure 9-12 (a), (b) and (c) show the 33 kHz waveforms of anode current, anode-cathode voltage and gate current, respectively, relative to the TMOS drain current (Figure 9-12d) and drain-source voltage (Figure 9-12e). Note that the load current rise time is limited by the inductance of the wire-wound load resistor and that the TMOS switches much faster. Second, to ensure turn-off of the GTO at elevated temperatures, the peak reverse gate current with V_{GR} of −12 V was about 6.0 A with a pulse width of about 1.0 μs at the 50% point.

The GEMFET versus the MOSFET and Bipolar

The GEMFET (Gain Enhanced MOSFET) is a new power semiconductor device with a combination of characteristics that were previously unavailable to the designer of power circuitry. Closely related to the power MOSFET in structure, this device has a forward voltage drop comparable to bipolars while maintaining the high input impedance and fast turn-on of its isolated gate. While turn-on speeds are very fast, turn-off is presently relatively slow and will restrict the use of at least the first generration of these devices to lower frequency applications.

The most pronounced advantage of the GEMFET over the power MOSFET is its lower on-resistance. The $r_{DS(on)}$ of a high voltage MOSFET is fairly large and rises with increasing junction temperature and drain current. Conversely, the $r_{DS(on)}$ of a GEMFET decreases with increasing T_J and is not greatly affected by I_D. Since the MOSFET does not have the GEMFET's offset voltage in its output transfer characteristics, at low currents the MOSFET on-resistance is slightly lower. However, at high currents and temperatures, the difference is dramatically in favor of the GEMFET.

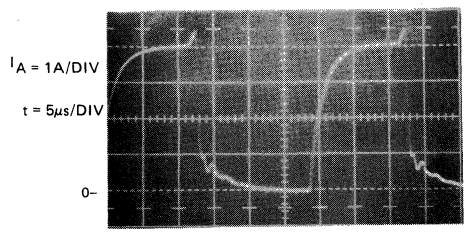


FIGURE 9-12a — GTO ANODE CURRENT

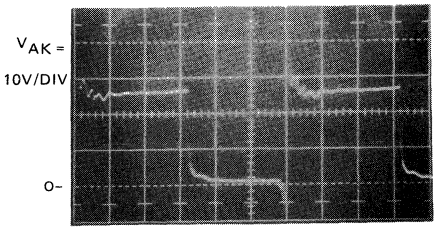


FIGURE 9-12b — GTO ANODE-CATHODE VOLTAGE

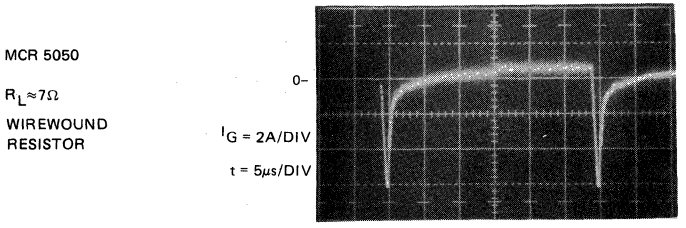


FIGURE 9-12c — GTO GATE CURRENT

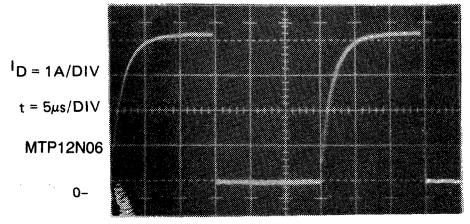


FIGURE 9-12d — TMOS DRAIN CURRENT

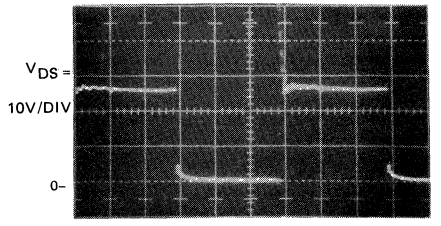


FIGURE 9-12e — TMOS DRAIN-SOURCE VOLTAGE

FIGURE 9-12 — COMPARATIVE SWITCHING OF A GTO AND TMOS AT 33 kHz

To illustrate the relative efficiencies of these two TO-220 devices — MGP20N50 GEMFET and MTP4N50 MOSFET — with that of a comparable die size, TO-220, high voltage Switchmode bipolar MJE13007, the low frequency, PWM motor controller test described in the previous section was performed. The results of a duty cycle versus case temperature rise test is shown in Figure 9-13. Note that at his low frequency test, where saturation losses predominate, the GEMFET is much more efficient than the MOSFET at low duty cycles (high motor armature currents), and even runs cooler than the bipolar device as the pulse width increases (motor current decreases).

The second test, comparing the three devices with an inductive load at several frequencies (the inductances were changed to maintain the same peak currents for all frequencies) is illustrated in Figure 9-14. Now, at the higher frequencies, the GEMFET runs the hottest — due to its slow turn-off switching time — and the MOSFET becomes more efficient than the bipolar at about 25 kHz.

For more information on the GEMFET, please refer to Chapter 8, the Spin-off Technologies of TMOS.

The Efficiency of TMOS versus Bipolar and Darlington Devices in the Energy Management Package

In high current packages, FETs add a new dimension of capabilities to power semiconductors. With ratings that allow operation in excess of 100 A, field-effect transistors now compete with other types of switches in heavy duty applications.

High current packages that were originally intended for bipolar Darlingtons are readily adapted to FETs. These Case 353 packages, labeled Energy Management Series (EMS) are shown in Figure 9-15.

In addition to testing relative efficiencies of devices encased in TO-204 (TO-3) and TO-220 packages, comparative temperature tests were also run on the EMS of transistors. The DUTs were the low-voltage, medium-current power MOSFET, MTE100N06 (100 A, 60 V) and similar die-size, low-voltage, experimental bipolar and Darlington transistors. The results of this resistor-load, variable-frequency test (100 Hz to 12 kHz) is shown in the temp-

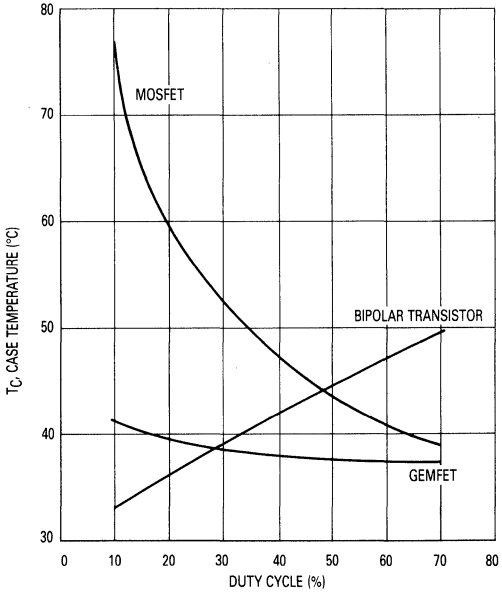


FIGURE 9-13 — ON-STATE EFFICIENCY COMPARISON — PWM OF DC MOTOR

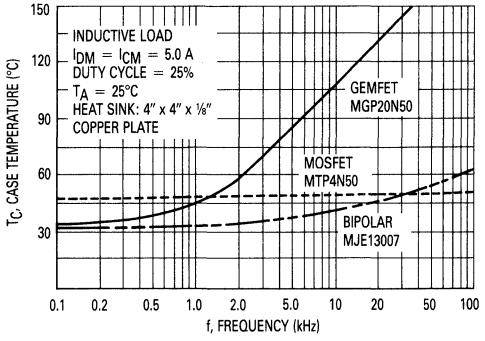


FIGURE 9-14 — COMPARISON OF CASE TEMPERATURE versus FREQUENCY FOR A GEMFET, MOSFET AND BIPOLAR TRANSISTOR

Case 353

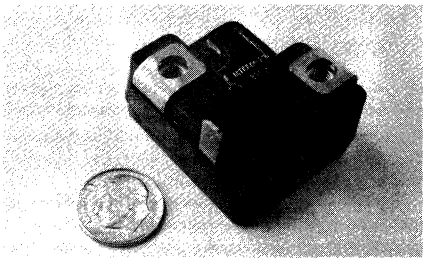


FIGURE 9-15 — HIGH CURRENT PACKAGE

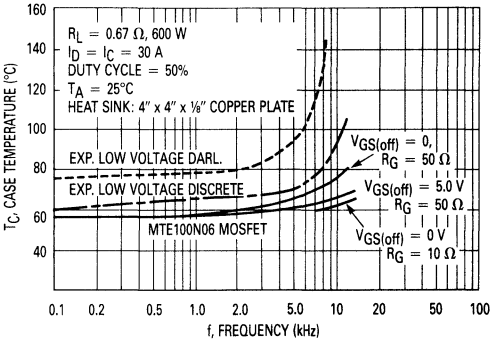


FIGURE 9-16 — CASE TEMPERATURE OF THE EMS PACKAGE FOR A RESISTIVE LOAD AS A FUNCTION OF OPERATING FREQUENCY

erature-rise curves of Figure 9-16. It is quite clear that this EMS TMOS is more efficient than the transistors, particularly at the 12 kHz end of the temperature-rise curve.

For details of this test refer to the section on the Medium Current Package, Chapter 10.

Chapter 10: Packaging

Using TMOS Die for Hybrid Assembly

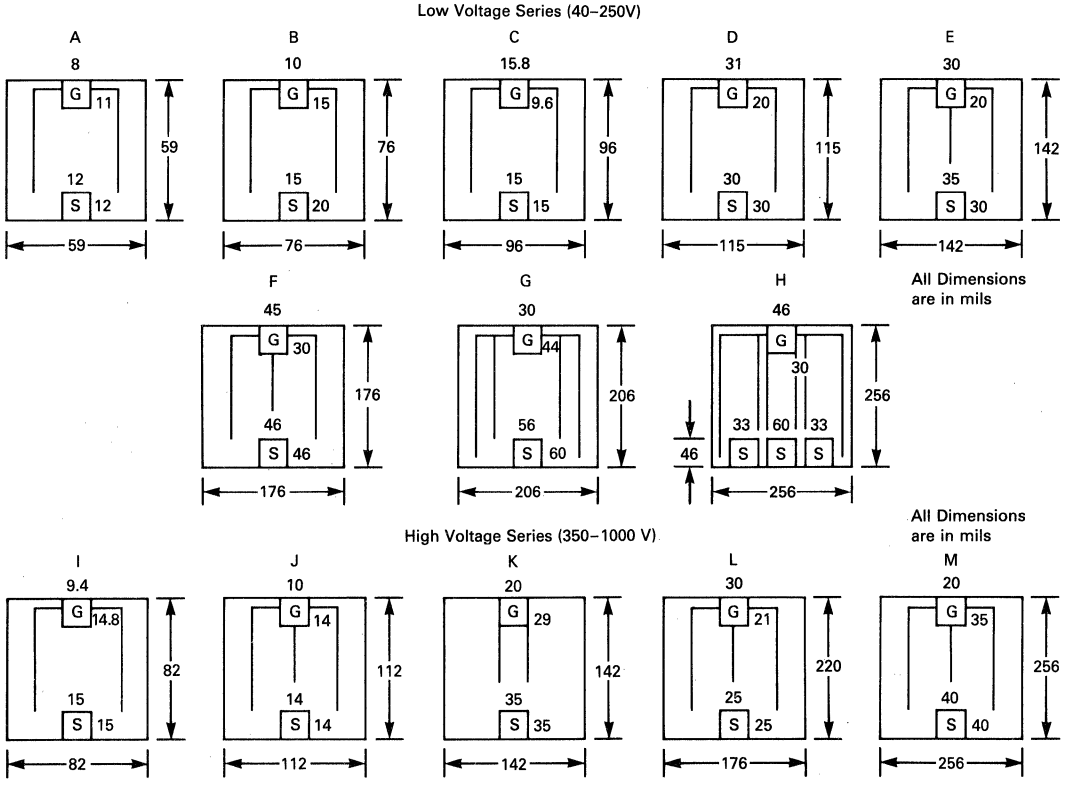
Substantial savings in weight and volume can be achieved by Hybrid Packaging Techniques. All Motorola TMOS packaged devices are available in die form* for custom hybrid assembly. The same advanced MOS processing techniques and silicon-gate structure available in packaged form is available in die form. The unique TMOS design utilizes thousands of source sites, interconnected in parallel, on a single die. This structure minimizes on-state voltage drop. The TMOS processing techniques result in an extremely reliable device which is highly reproducible in various die sizes.

*MTE Series and MTM15N35-50 are not available as these are multi-die devices, although the individual chips are available for paralleling in high power applications.

DIE CHARACTERISTICS

Currently, 12 die sizes are available. Seven with low-voltage (40–250 V) and five with high-voltage (350–1.0 kV) capabilities. Table 1 lists the available die sizes, their dimensions, bond pad dimensions and die thickness. Group A through H are low-voltage and I through M are high-voltage. All die sizes have one gate and one source

TABLE 1 — TMOS Die and Bond Pad Dimensions (Not Shown to Scale)



TMOS DIE AND BOND PAD DIMENSIONS	A	B	C	D	E	F	G	H	I	J	K	L	M
L (Inch)	0.059	0.076	0.096	0.115	0.142	0.176	0.206	0.256	0.082	0.112	0.142	0.220	0.256
W (Inch)	0.059	0.076	0.096	0.115	0.142	0.176	0.206	0.256	0.082	0.112	0.142	0.176	0.256
L Gate (Inch)	0.008	0.015	0.0096	0.020	0.020	0.030	0.030	0.030	0.094	0.010	0.020	0.021	0.020
W Gate (Inch)	0.011	0.010	0.0158	0.031	0.030	0.045	0.044	0.046	0.148	0.014	0.029	0.030	0.035
L Source (Inch)	0.012	0.020	0.015	0.030	0.030	0.046	0.056	0.046	0.015	0.014	0.035	0.025	0.040
W Source (Inch)	0.012	0.015	0.015	0.030	0.035	0.046	0.060	0.033/.060	0.015	0.014	0.035	0.025	0.040
Thickness (Inch)	0.011 nom	0.011 nom	0.011 nom	0.011 nom	0.011 nom	0.011 nom	0.011 nom	0.011 nom	0.011 nom	0.011 nom	0.011 nom	0.011 nom	0.11 nom

bond pad, with the exception of Series G, which has three source pads. All die are individually probed, at room temperature, to the electrical specifications shown in Table 2.

Due to limitations when probing in wafer form, some of the specifications of the equivalent packaged device cannot be tested and guaranteed in die form. These parameters are safe-operating area (SOA), thermal resistance ($R_{\theta JC}$), on-resistance $r_{DS(on)}$ at rated current. The above parameters depend on the assembly techniques of the individual user. The following specifications are a function of the die design and typical numbers for these parameters can be found on the data sheet of the equivalent packaged part. These specifications are C_{iss}, C_{oss}, C_{rss}, $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f. These values are available from the corresponding data sheets listed in Table 2.

Each die is 100% tested by state-of-the-art computer equipment for dc parameters at 25°C and visually inspected per MIL-STD-883 prior to shipment.

TABLE 2 — ELECTRICAL PROBE SPECIFICATIONS FOR TMOS DIE

Part Number	Die Size	Max Rated V_{DS}	$r_{DS(on)}$ Max V_{GS} = 10 V I_D=1.0 A	Corresponding Data Sheets	I_{DSS} @ 85% Rated V_{DS}	I_{GSS} @ V_{GS} = 20 V Max	$V_{GS(th)}$ I_D = 1.0 mA V_{DS} = V_{GS} Min	Max
MTC5N05	A	50	0.6	MTP5N05	0.25 mA	500 nA	2.0 V	4.5 V
MTC5N06	A	60	0.6	MTP5N06	0.25 mA	500 nA	2.0 V	4.5 V
MTC4N08	A	80	0.8	MTP4N08	0.25 mA	500 nA	2.0 V	4.5 V
MTC4N10	A	100	0.8	MTP4N10	0.25 mA	500 nA	2.0 V	4.5 V
MTC3N12	A	120	1.3	MTP3N12	0.25 mA	500 nA	2.0 V	4.5 V
MTC3N15	A	150	1.3	MTP3N15	0.25 mA	500 nA	2.0 V	4.5 V
MTC2N18	A	180	1.8	MTP2N18	0.25 mA	500 nA	2.0 V	4.5 V
MTC2N20	A	200	1.8	MTP2N20	0.25 mA	500 nA	2.0 V	4.5 V
MTC7N05	B	50	0.4	MTP7N05	0.25 mA	500 nA	2.0 V	4.5 V
MTC7N06	B	60	0.4	MTP7N06	0.25 mA	500 nA	2.0 V	4.5 V
MTC6N08	B	80	0.6	MTP6N08	0.25 mA	500 nA	2.0 V	4.5 V
MTC6N10	B	100	0.6	MTP6N10	0.25 mA	500 nA	2.0 V	4.5 V
MTC5N12	B	120	0.9	MTP5N12	0.25 mA	500 nA	2.0 V	4.5 V
MTC5N15	B	150	0.9	MTP5N15	0.25 mA	500 nA	2.0 V	4.5 V
MTC4N18	B	180	1.2	MTP4N18	0.25 mA	500 nA	2.0 V	4.5 V
MTC4N20	B	200	1.2	MTP4N20	0.25 mA	500 nA	2.0 V	4.5 V
MTC10N05	C	50	0.28	MTP10N05	0.25 mA	500 nA	2.0 V	4.5 V
MTC10N06	C	60	0.28	MTP10N06	0.25 mA	500 nA	2.0 V	4.5 V
MTC8N08	C	80	0.50	MTP8N08	0.25 mA	500 nA	2.0 V	4.5 V
MTC8N10	C	100	0.50	MTP8N10	0.25 mA	500 nA	2.0 V	4.5 V
MTC7N12	C	120	0.70	MTP7N12	0.25 mA	500 nA	2.0 V	4.5 V
MTC7N15	C	150	0.70	MTP7N15	0.25 mA	500 nA	2.0 V	4.5 V
MTC5N18	C	180	1.0	MTP5N18	0.25 mA	500 nA	2.0 V	4.5 V
MTC5N20	C	200	1.0	MTP5N20	0.25 mA	500 nA	2.0 V	4.5 V
MTC12N05	C	50	0.20	MTP12N05	0.25 mA	500 nA	2.0 V	4.5 V
MTC12N06	C	60	0.20	MTP12N06	0.25 mA	500 nA	2.0 V	4.5 V
MTC10N08	C	80	0.33	MTP10N08	0.25 mA	500 nA	2.0 V	4.5 V
MTC10N10	C	100	0.33	MTP10N10	0.25 mA	500 nA	2.0 V	4.5 V
MTC8N12	C	120	0.50	MTP8N12	0.25 mA	500 nA	2.0 V	4.5 V
MTC8N15	C	150	0.50	MTP8N15	0.25 mA	500 nA	2.0 V	4.5 V
MTC7N18	C	180	0.70	MTP7N18	0.25 mA	500 nA	2.0 V	4.5 V
MTC7N20	C	200	0.70	MTP7N20	0.25 mA	500 nA	2.0 V	4.5 V
MTC15N05	D	50	0.16	MTP15N05	0.25 mA	500 nA	2.0 V	4.5 V
MTC15N06	D	60	0.16	MTP15N06	0.25 mA	500 nA	2.0 V	4.5 V
MTC12N08	D	80	0.18	MTP12N08	0.25 mA	500 nA	2.0 V	4.5 V
MTC12N10	D	100	0.18	MTP12N10	0.25 mA	500 nA	2.0 V	4.5 V
MTC10N12	D	120	0.30	MTP10N12	0.25 mA	500 nA	2.0 V	4.5 V
MTC10N15	D	150	0.30	MTP10N15	0.25 mA	500 nA	2.0 V	4.5 V
MTC8N18	D	180	0.40	MTP8N18	0.25 mA	500 nA	2.0 V	4.5 V
MTC8N20	D	200	0.40	MTP8N20	0.25 mA	500 nA	2.0 V	4.5 V
MTC25N05	E	50	0.08	MTP25N05	0.25 mA	500 nA	2.0 V	4.5 V

TABLE 2 — ELECTRICAL PROBE SPECIFICATIONS FOR TMOS DIE (Continued)

Part Number	Die Size	Max Rated V_{DS}	$r_{DS(on)}$ Max V_{GS} = 10 V I_D=1.0 A	Corresponding Data Sheets	I_{DSS} @ 85% Rated V_{DS}	I_{GSS} @ V_{GS} = 20 V Max	$V_{GS(th)}$ I_D = 1.0 mA V_{DS} = V_{GS} Min	$V_{GS(th)}$ I_D = 1.0 mA V_{DS} = V_{GS} Max
MTC25N06	E	60	0.08	MTP25N06	0.25 mA	500 nA	2.0 V	4.5 V
MTC20N08	E	80	0.15	MTP20N08	0.25 mA	500 nA	2.0 V	4.5 V
MTC20N10	E	100	0.15	MTP20N10	0.25 mA	500 nA	2.0 V	4.5 V
MTC15N12	E	120	0.25	MTP15N12	0.25 mA	500 nA	2.0 V	4.5 V
MTC15N15	E	150	0.25	MTP15N15	0.25 mA	500 nA	2.0 V	4.5 V
MTC12N18	E	180	0.35	MTP12N18	0.25 mA	500 nA	2.0 V	4.5 V
MTC12N20	E	200	0.35	MTP12N20	0.25 mA	500 nA	2.0 V	4.5 V
MTC35N05	F	50	0.055	MTM35N05	0.25 mA	500 nA	2.0 V	4.5 V
MTC35N06	F	60	0.055	MTM35N06	0.25 mA	500 nA	2.0 V	4.5 V
MTC25N08	F	80	0.07	MTM25N08	0.25 mA	500 nA	2.0 V	4.5 V
MTC25N10	F	100	0.07	MTM25N10	0.25 mA	500 nA	2.0 V	4.5 V
MTC20N12	F	120	0.12	MTM20N12	0.25 mA	500 nA	2.0 V	4.5 V
MTC20N15	F	150	0.12	MTM20N15	0.25 mA	500 nA	2.0 V	4.5 V
MTC15N18	F	180	0.16	MTM15N18	0.25 mA	500 nA	2.0 V	4.5 V
MTC15N20	F	200	0.16	MTM15N20	0.25 mA	500 nA	2.0 V	4.5 V
MTC50N05	G	50	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC50N06	G	60	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC40N08	G	80	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC40N10	G	100	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC35N12	G	120	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC35N15	G	150	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC30N18	G	180	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC30N20	G	200	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC60N05	H	50	0.028	MTM60N05	0.25 mA	500 nA	2.0 V	4.5 V
MTC60N06	H	60	0.028	MTM60N06	0.25 mA	500 nA	2.0 V	4.5 V
MTC55N08	H	80	0.04	MTM55N08	0.25 mA	500 nA	2.0 V	4.5 V
MTC55N10	H	100	0.04	MTM55N10	0.25 mA	500 nA	2.0 V	4.5 V
MTC45N12	H	120	0.06	MTM45N12	0.25 mA	500 nA	2.0 V	4.5 V
MTC45N15	H	150	0.06	MTM45N15	0.25 mA	500 nA	2.0 V	4.5 V
MTC40N18	H	180	0.08	MTM40N18	0.25 mA	500 nA	2.0 V	4.5 V
MTC40N20	H	200	0.08	MTM40N20	0.25 mA	500 nA	2.0 V	4.5 V
MTC2N35	I	350	5.0	MTP2N35	0.25 mA	500 nA	2.0 V	4.5 V
MTC2N40	I	400	5.0	MTP2N40	0.25 mA	500 nA	2.0 V	4.5 V
MTC1N45	I	450	8.0	MTP1N45	0.25 mA	500 nA	2.0 V	4.5 V
MTC1N50	I	500	8.0	MTP1N50	0.25 mA	500 nA	2.0 V	4.5 V
MTC1N55	I	550	12.0	MTP1N55	0.25 mA	500 nA	2.0 V	4.5 V
MTC1N60	I	600	12.0	MTP1N60	0.25 mA	500 nA	2.0 V	4.5 V
MTC3N35	J	350	3.3	MTP3N35	0.25 mA	500 nA	2.0 V	4.5 V
MTC3N40	J	400	3.3	MTP3N40	0.25 mA	500 nA	2.0 V	4.5 V
MTC2N45	J	450	4.0	MTP2N45	0.25 mA	500 nA	2.0 V	4.5 V
MTC2N50	J	500	4.0	MTP2N50	0.25 mA	500 nA	2.0 V	4.5 V
MTC4N35	J	350	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC4N40	J	400	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC3N45	J	450	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC3N50	J	500	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC2N55	J	550	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC2N60	J	600	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC5N35	K	350	1.0	MTP5N35	0.25 mA	500 nA	2.0 V	4.5 V
MTC5N40	K	400	1.0	MTP5N40	0.25 mA	500 nA	2.0 V	4.5 V
MTC4N45	K	450	1.5	MTP4N45	0.25 mA	500 nA	2.0 V	4.5 V

TABLE 2 — ELECTRICAL PROBE SPECIFICATIONS FOR TMOS DIE (Continued)

Part Number	Die Size	Max Rated V_{DS}	$r_{DS(on)}$ Max V_{GS} = 10 V I_D=1.0 A	Corresponding Data Sheets	I_{DSS} @ 85% Rated V_{DS}	I_{GSS} @ V_{GS} = 20 V Max	$V_{GS(th)}$ I_D = 1.0 mA V_{DS} = V_{GS} Min	$V_{GS(th)}$ I_D = 1.0 mA V_{DS} = V_{GS} Max
MTC4N50	K	500	1.5	MTP4N50	0.25 mA	500 nA	2.0 V	4.5 V
MTC3N55	K	550	2.5	MTP3N55	0.25 mA	500 nA	2.0 V	4.5 V
MTC3N60	K	600	2.5	MTP3N60	0.25 mA	500 nA	2.0 V	4.5 V
MTC3N75	K	750	7.0	MTP3N75	0.25 mA	500 nA	2.0 V	4.5 V
MTC3N80	K	800	7.0	MTP3N80	0.25 mA	500 nA	2.0 V	4.5 V
MTC2N85	K	850	8.0	MTP2N85	0.25 mA	500 nA	2.0 V	4.5 V
MTC2N90	K	900	8.0	MTP2N90	0.25 mA	500 nA	2.0 V	4.5 V
MTC1N95	K	950	10.0	MTP1N95	0.25 mA	500 nA	2.0 V	4.5 V
MTC1N100	K	1000	10.0	MTP1N100	0.25 mA	500 nA	2.0 V	4.5 V
MTC8N35	L	350	0.55	MTM8N35	0.25 mA	500 nA	2.0 V	4.5 V
MTC8N40	L	400	0.55	MTM8N40	0.25 mA	500 nA	2.0 V	4.5 V
MTC7N45	L	450	0.80	MTM7N45	0.25 mA	500 nA	2.0 V	4.5 V
MTC7N50	L	500	0.80	MTM7N50	0.25 mA	500 nA	2.0 V	4.5 V
MTC6N55	L	550	1.2	MTM6N55	0.25 mA	500 nA	2.0 V	4.5 V
MTC6N60	L	600	1.2	MTM6N60	0.25 mA	500 nA	2.0 V	4.5 V
MTC15N35	M	350	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC15N40	M	400	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC15N45	M	450	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC15N50	M	500	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC12N55	M	550	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
MTC12N60	M	600	TBD	TBD	0.25 mA	500 nA	2.0 V	4.5 V
*MTC8P08	E	80	0.4	MTP8P08	0.25 mA	500 nA	2.0 V	4.5 V
*MTC8P10	E	100	0.4	MTP8P10	0.25 mA	500 nA	2.0 V	4.5 V
*MTC2P45	K	450	6.0	MTP2P45	0.25 mA	500 nA	2.0 V	4.5 V
*MTC2P50	K	500	6.0	MTP2P50	0.25 mA	500 nA	2.0 V	4.5 V

VISUAL INSPECTION OF DIE

All Motorola TMOS dice meet the visual inspection criteria of Mil-Standard 750B, Method 2073, with the exception of specific criteria listed below. All TMOS dice are visually screened to a 1.0% AQL level.

DIE BACKING

All standard TMOS dice come with Titanium-Nickel-Silver drain metallization. This metallization is suitable for solder pre-form mounting with solders such as 95/5 PbSn or 92.5/5.0/2.5 PbInAg. Commonly used header or substrate materials such as copper, nickel plated copper, gold plated molybdenum, beryllia and alumina are acceptable. The substrate material must be free of all oxides prior to assembly. Mounting is generally accomplished in a profiled belt furnace (hydrogen atmosphere is recommended). Gold backing is also available but the factory must be consulted.

WIRE BONDING

Electrical connection to the gate and source bond pads can be accomplished by ultrasonic wire bonding, using AlMg* wire having an elongation of 10%. Caution should be exercised during wire bonding to insure that the bonding footprint remains within the bonding pad area. Wire bond settings should be optimized and a wire pull test performed (see Method 2037, Mil Standard 750B) to monitor wire bond strength uniformity. Destructive sample testing and 100% non-destructive testing is recommended.

*Wire sizes of 15 mils and greater are pure Al.

ENCAPSULATION

Before encapsulation, the assembly must be kept in a moisture free environment. I_{GSS} and $V_{GS(th)}$ are sensitive to surface moisture. For a non-hermetic package, a high grade electronic coating such as Dow Corning RTV3140 should be applied (coating is optional with a hermetic package). Before encapsulation, a 150°C two-hour bake should be performed to remove any surface moisture and any capping of hermetic packages must be performed in a dry, nitrogen atmosphere.

HANDLING AND SHIPPING

TMOS Dice are available packaged several ways:

1. Anti-static MultiPak — Waffle type carrier with individual die package.
2. Scribed and Broken Wafers — Wafer on Mylar and vacuum sealed in plastic, with rejects inked.
3. Wafer Pak — Whole wafers, with rejects inked.
4. Circle Pak — Whole wafer is placed on sticky film before being sawed and broken. Special equipment is needed to remove die from sticky film, with rejects inked.

Upon opening the plastic container, dice should be stored in a nitrogen atmosphere to prevent oxidation of

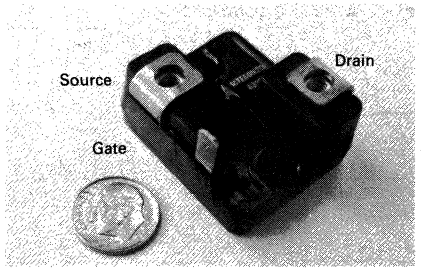


FIGURE 10-1a

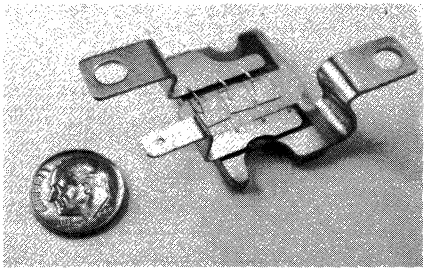


FIGURE 10-1b

FIGURE 10-1 — THE EMS PACKAGE AND LEADFRAME DETAILS

bond areas prior to assembly. All dice should be handled with teflon tipped probes to prevent any mechanical damage and the probe needles should be dipped in a conductive solution as teflon can cause ESD problems.

Multiple TMOS in the EMS Package

With the increasing use of higher power semiconductors for energy management and power conversion, the need for more efficient, cost-effective packages becomes more apparent. The old standby TO-204 (TO-3), while useful in its particular power niche, cannot reliably handle load currents beyond 60 A. Moreover, its feed-through terminals do not always accommodate all system packaging and bussing requirements. To overcome this limitation, Motorola has introduced a plastic package (Case 353) capable of handling up to 100 A continuous collector current and delivering up to 25 kVA. This new, medium current package, labeled "Energy Management Series" (EMS), is designed for a single-side mounting with bussable drain and source terminals. It is also mounting hole compatible with the TO-204, allowing for ease in retrofitting, and the terminal spacings meet U.L. requirements.

This high current package, (Figure 10-1a) originally intended for bipolar Darlingtons, is readily adapted to MOSFETs. The mechanical leadframe configuration (Figure 10-1b) allows adding other discrete devices to the package, e.g., speed-up diodes for Darlingtons, freewheeling diodes for bipolars and gate-suppressor resistors for power MOSFETs.

ADVANCES IN MULTIPLE DIE POWER MOSFETS

The judicious placement of multiple TMOS die in the package has already spawned a new generation of power MOSFETs with power handling capabilities up to 250 W, and the extension of this technology to the 500 W Case 346 package will soon make available devices with even greater current and power ratings.

Previously, two obstacles prevented the development of very large power MOSFETs. First, an attempt to increase the power ratings simply by using much larger die is economically impractical. As die areas become very large, the wafer defect density decreases the yield to the point that the remaining good units are prohibitively expensive.

Secondly, while paralleling multiple smaller chips circumvent the yield problems associated with very large single chips, multi-chip devices, until now, were prone to self-induced oscillations when slowly switched through or operated in the active region.

OSCILLATION PROBLEM RESOLVED

The high input impedance and high-frequency capabilities of the MOSFET present the possibility of self-induced oscillation in paralleled devices. The gate-to-drain parasitic capacitance influences the problem by providing a regenerative feedback loop to the gate and by forming a high-Q circuit with the gate and drain parasitic inductances (Figure 10-2).

Inserting small resistances in series with each gate defuses the problem by degrading the Q of the LC network formed by the circuit parasitics. The magnitude of these resistors can be fairly small so that switching speeds are not greatly compromised at the expense of circuit stability. While this remedy is conceptually simple, the proper package makes the device manufacturable. Conventional resistors in this package would be awkward, at best. Therefore, a technique is borrowed from RF Hybrids. Vertical silicon chip resistors are connected to the external gate lead via a die-bonding process. Forming the other half of the connection, each of the resistors are wirebonded to the gate pad on a corresponding FET. The resulting structure, Figure 10-1b, proved to be the ideal vehicle to pursue the multi-chip approach. The external gate lead is large enough to accept the die-bonding of three gate-suppression resistors. Since they conduct current vertically, electrical connections are complete when the resistors are wirebonded to the gates of the MOSFETs. An additional

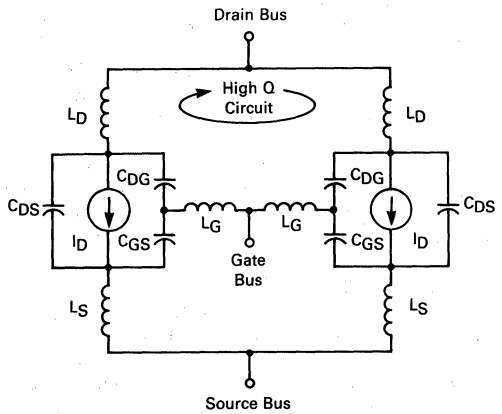


FIGURE 10-2 — PARASITIC HIGH Q CIRCUIT ACCOMPANYING PARALLELED MOSFETs WITH NO GATE DECOUPLING RESISTORS.

advantage of this method is that it does not introduce superfluous wirebonds that may compromise reliability.

ADVANTAGES OF THE MULTI-CHIP APPROACH

The most obvious advantage of the multiple-chip approach is the convenience afforded the user that no longer must parallel discretes. Mounting, heat sinking, circuit layout and gate-drives are all simplified when using a device paralleled by the manufacturer. In addition to offering greater convenience, the multi-chip MOSFET excels in other subtle, but important, ways.

Parameter variations in semiconductors are often due to slight process variations between different wafer lots or between wafers in the same lot. Parameters also vary radically on the same wafer. However, adjacent die undergo nearly identical processing and, consequently, tend to have very similar electrical characteristics. To enhance current sharing among the parallel chips, Motorola's multi-chip devices are manufactured using adjacent die from a wafer. Discretes would have to be matched very closely to achieve the degree of current sharing that is characteristic of adjacent die.

Especially for rapid switching, another important consideration for good current sharing during switching transitions is the symmetry of the circuit layout. The circuit symmetry attained in the medium current MOSFET is also difficult to duplicate with discrete devices.

Paralleling MOSFETs at the chip level has a subtle reliability advantage over paralleling discrete devices. The tendency to share current is forced by differences in junction temperature. Often the improvement in current sharing brought about by differences in temperature, due to variations in $r_{DS(on)}$, is not as great as is commonly believed. From a reliability standpoint, the increase in T_J of the device with the lowest $r_{DS(on)}$ may not be offset by the corresponding improvement in current distribution. While the degree of current sharing suffers slightly, close thermal coupling decreases the temperature differential between devices and improves reliability. Close thermal coupling without compromising heat sinking capability is most easily accomplished by paralleling chips on the same heat sink.

SPECIAL CONSIDERATIONS FOR USING HIGH POWER MOSFETs

Often accompanying significant gains in device technology are new considerations for proper use of those advances. Specifically, multi-chip MOSFETs are expanding the combination of high-current and fast-switching capabilities of solid-state devices. Since switching speeds and current magnitudes have a direct impact on the magnitude of the "flyback voltage" ($v = L\ di/dt$), this new technology demands that close attention be paid to protecting the device from excessive drain-to-source voltage.

Even at switching speeds normally considered slow for power MOSFETs, the di/dt at turn-off may be large, due to the switching of a sizable drain current. Consequently, though slower switching lessens the problem, circuits should be checked for excessive drain-source voltage spikes at turn-off, regardless of switching speeds. It is strongly recommended that product development begin with V_{DS} protection techniques that appear to be exorbitant for the application. If the clamping scheme appears excessive during later stages of development, it can then be simplified.

For rapid switching, drain-source overvoltage protection is a must. The clamping or snubbing networks employed must have response times commensurate with the MOSFET switching speeds. Typical forward recovery times of rectifiers limit their use as clamping schemes to slower switching transitions. Although zeners, surge suppressors and MOVs have response times appropriate for even the fastest MOSFET switching speeds, their effectiveness can be undermined by long lead lengths or by a high dynamic impedance, as explained below.

Because multi-chip MOSFETs can produce very large di/dt's, placement of the drain-source overvoltage protection network is critical. The following example underscores the importance of minimizing lead lengths.

Assume that a multi-chip MOSFET is switching 100 A in 100 ns and the parasitic wiring inductance is 10 nH. The flyback voltage induced in the wiring inductance is 10 V, which may be a considerable percent of the maximum V_{DS} rating.

To minimize the parasitic lead and wiring inductance, the ideal placement of a drain-source clamp is directly between the source lead and a heat sink that is not electrically isolated from the drain (Figure 10-3). This method bypasses the bulk of the drain-package inductance and usually facilitates heat sinking the clamp. Alternatively, the clamp can be placed directly across the drain-source terminals, but mounting and heat sinking may be more difficult.

The power rating of the clamping scheme obviously must be scaled to safely dissipate the energy stored in the inductor. If the energy to be clamped is large, a dual clamping scheme may provide the best protection. For instance, a zener may be used to clamp the flyback voltage during the first tens or hundreds of nanoseconds (Figure 10-4). The clamp network in parallel with the zener becomes the primary clamping element after the forward recovery time of its diode has elapsed. The nominal voltage of the zener should be greater than V_{CL} so that the conduction time of the zener, and consequently its power rating, can remain smaller than if it were the sole clamping element.

The large amount of current being clamped also merits special considerations. First, the clamp must be able to safely conduct the very high peak load currents. Second, clamping these currents must be accomplished without a large increase in the potential appearing across the clamp, due to its clamping factor. A 40 V zener, for instance, may only support 40 V at 1.0 A but 50 V at 20 A. Paralleling the "first-line" elements in dual clamping schemes increases the clamp's current capability and minimizes the

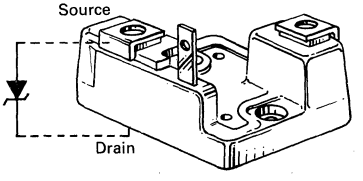


FIGURE 10-3 — OPTIMUM PLACEMENT OF V_{DS} CLAMP

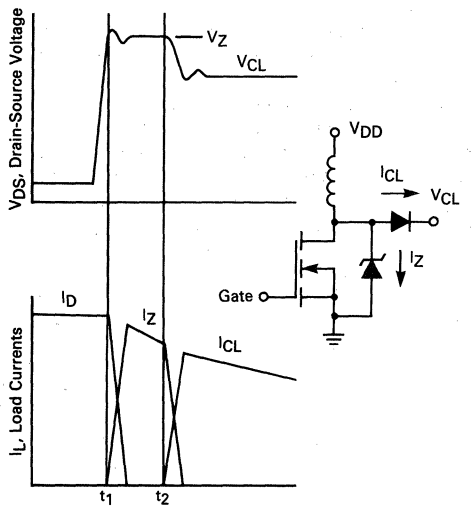


FIGURE 10-4 — IDEALIZED WAVEFORMS OF A DUAL CLAMPING SCHEME PROVIDING DRAIN-SOURCE OVERVOLTAGE PROTECTION

effect of the clamping factor. Automotive button surge suppressors, such as the MR2525, performed well during development and testing of Motorola's multi-chip power MOSFETs.

To ensure that the voltage appearing across the drain-source terminals does not exceed the maximum V_{DS} rating, proper measurement techniques are warranted. For very rapid switching, flyback voltage transients should be measured with a wideband oscilloscope and voltage probe (> 150 MHz). The use of probes with grounding leads is not recommended. Rather, a chassis-mount test jack, with its ground soldered directly to the source lead and its tip to the drain, is a more precise technique.

Even with an ideal RF layout and a perfect drain-source voltage clamp, large di/dt's may necessitate considerations of the effects of the parasitic package inductances.

V_{DS} DERATING FOR LARGE di/dt's

When a MOSFET, including both multiple and single-die devices, generates a large di/dt at turn-off, the source and drain package inductances can produce significant drain-source voltage stress in addition to that observed at the device terminals. This situation deserves special attention in multi-chip devices, in part due to the larger package inductances. The increased magnitude of the current being switched also exacerbates the problem.

Since the circuit designer has no control over internally generated voltages, a derating of the maximum allowable V_{DS} is warranted when large currents are switched rapidly.

The circuit elements internal to the "Medium Current" multi-chip MOSFET, including the significant parasitics, are illustrated in Figure 10-5. The three individual source inductances represent the inductance of the source wirebonds, and the inductances at the source and drain terminals model the source and drain bus. Figure 10-6 shows an oscillogram that compares the drain-source flyback voltage that appears at the terminals with the voltage between nodes A and B in Figure 10-5. The 55 to 60 V difference between the external and internal measurements emphasizes the need for some precautions. Although it is a much more accurate representation of V_{DS} at the chip, Figure 10-6 does not include the effects of the inductance of the source wirebonds. Because of the polarity of the voltage across the source wirebond inductance at turn-off, the peak V_{DS} at the chips is greater than that depicted by Figure 10-6.

The use of the di/dt derating curve, illustrated in Figure 10-7, assures that the peak voltage across the drain-source terminals, plus any internally generated voltages, will not exceed the device's maximum V_{DS} rating. If, for instance, the peak di/dt of the MTE100N06 is 500 A/μs, the maximum allowable peak V_{DS} at the terminals, concurrent with that di/dt, is about 48 volts. In effect, the turn-off SOA has been derated from 60 V to 48 V. As shown in Figure 10-8, the peak V_{DS} is usually larger than the intended clamp voltage.

The derating curve for all "Medium Current" MOSFETs are based on an effective total drain and source package inductance of 25 nH. This figure includes a 25% guard-band above the 20 nH that was derived from various vector impedance meter readings. This estimate was substantiated by analysis of waveforms such as Figure 10-6.

"ON" VOLTAGE COMPARISON

FETs are often associated with higher levels of on-state power dissipation than bipolars, particularly at higher power levels. While this perception is accurate at power-line voltages, at voltages below 100 volts, FETs have a distinct advantage. Figures 10-9 and 10-10 illustrate the

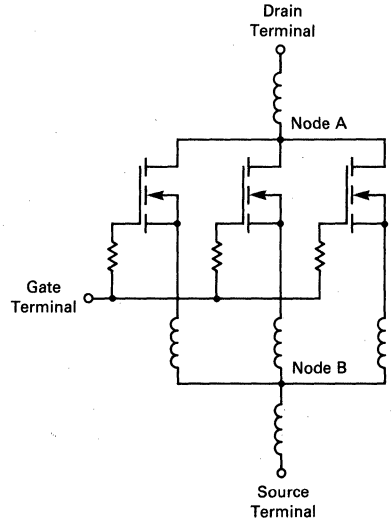


FIGURE 10-5 — INTERNAL CIRCUIT ELEMENTS OF MEDIUM CURRENT POWER MOSFET

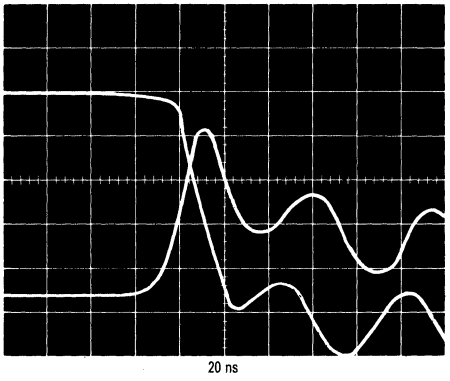


FIGURE 10-6a — DRAIN CURRENT AND DRAIN-SOURCE VOLTAGE APPEARING AT TERMINALS — MTE60N20 — OFF BIAS = −4.0 VOLTS

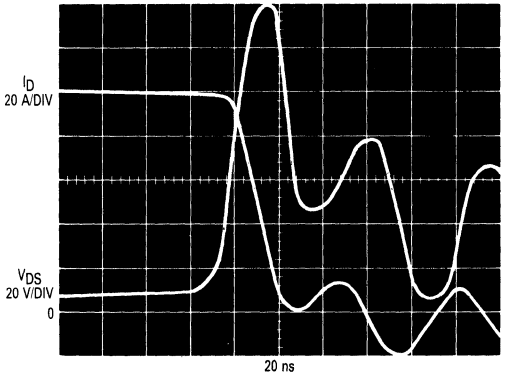


FIGURE 10-6b — DRAIN CURRENT AND DRAIN-SOURCE VOLTAGE APPEARING NEAR CHIPS — MTE60N20 — OFF BIAS = −4.0 VOLTS

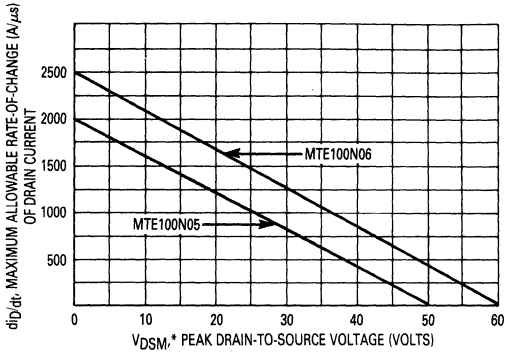


FIGURE 10-7 — MAXIMUM ALLOWABLE di_D/dt PEAK DRAIN-SOURCE VOLTAGE FOR MTE100N06

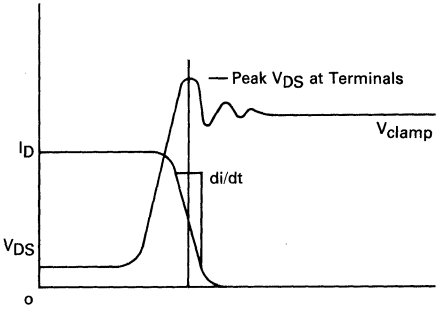


FIGURE 10-8 — CONDITION AT WHICH di/dt-V_{DS} DERATING IS COMPUTED

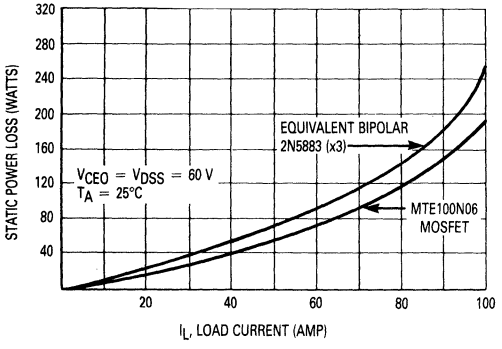


FIGURE 10-9 — STATIC POWER LOSS OF 60 V MOSFET AND EQUIVALENT BIPOLARS

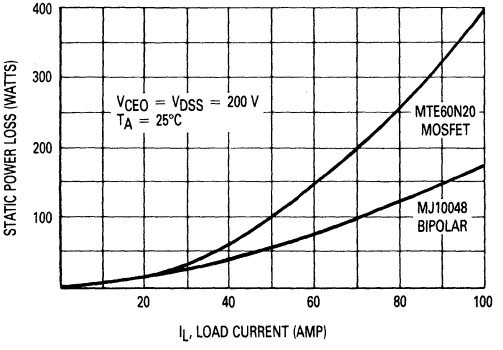


FIGURE 10-10 — STATIC POWER LOSSES OF 200 V MOSFET AND BIPOLARS

NOTE: FIGURES 10-9 AND 10-10 ASSUME THAT THE BIPOLAR IS DRIVEN FROM A 5.0 V SOURCE, AND THAT THE TOTAL POWER SUPPLIED FROM THE SOURCE IS AN ON-STATE POWER LOSS.

differences. Comparing the 60 V MTE100N06 to an equivalent bipolar, the advantage clearly lies with the FET. At 200 volts, however, the tables are turned. The MJ10048 bipolar Darlington has considerably lower "on" voltages.

These tradeoffs are not likely to remain static. Technology is improving FET "on" voltages at a rapid rate. As time goes on, FETs can be expected to gain an even greater advantage at low voltages, and narrow the gap at higher voltages.

SWITCHING CHARACTERISTICS

Dynamic operation of high current FETs differs considerably from what is generally experienced with lower power MOSFET transistors. Subtleties that are experienced as second order effects at 5.0 or 10 A become first order characteristics at 50 or 100 A. Differences are discussed in terms of resistive switching, temperature coefficient, gate bias, and di/dt limitations.

Resistive Switching:

In general, power MOS transistors are specified for resistive switching. Unlike bipolars, inductive switching is not normally specified, since performance in both types of circuits is very similar. For high current FETs, the situation is reversed. Inductive switching is specified, while resistive switching is omitted.

This departure from convention is the indirect result of very impressive performance. When high currents are switched at high rates of speed, there comes a point at which the inevitable inductance associated with a practical circuit no longer becomes negligible. FETs have reached this point. Resistive rise times tend to be limited more by the L/R ratio of the test circuit than by the switching time of the device. Consequently, inductive specs are better suited to high current FETs.

Temperature Coefficient:

Variation of switching times with temperature is not normally an issue with power FETs. Gate capacitance, upon which switching times depend, is very stable with respect to temperature. A single-die device, such as the MTM15N20, will typically repeat 25°C readings within 5% at 100°C. The temperature coefficient is so near zero that the high-temperature switching specs, popular with bipolar transistors, have not caught on with FETs.

Again, high-current FETs are somewhat different. Multiple-die construction introduces a new variable, the gate-ballast resistor. These silicon resistors have a positive temperature coefficient. Since FET switching times are proportional to gate resistance, the switching characteristics of the high current FET include a positive temperature coefficient. Figure 10-11 provides an illustration.

The curve shows a switching time increase of 3.0 ns going from 25°C to 100°C. Although this is a 33% increase, in practice, 3.0 ns is not enough of a change to make much difference. From a specification point of view, however, it is good engineering practice to specify parameters for their worst-case conditions. For that reason, high-temperature switching specs have been chosen as the standard format for high-current FETs.

In applications where the external driving impedance is much above 10 Ω, the temperature coefficient of the internal resistors is swamped out by the much larger external impedance. In these situations, the switching-time temperature coefficient of the high current FET can, for all practical purposes, be ignored. In such cases, it is the temperature coefficient of the driving impedance that determines the temperature dependence of switching time.

Gate Bias:

At currents less than 10 A, MOSFET turn-off times are only moderately sensitive to negative gate bias. An illustration appears in Figure 10-12. The 10 A curve shows only a modest 20% improvement in crossover time, going from $V_{GS(off)}$ = 0 volts to $V_{GS(off)}$ = −20 volts.

At higher currents, something interesting happens. MOSFET switching times, being relatively insensitive to current density, normally remain relatively constant as current is increased. Therefore, as drain current is increased, di/dt increases also. At drain currents of 50 to 100 A, di/dt's on the order of 5.0 A per nanosecond are readily achievable. At this speed, parasitic circuit inductances, which have second-order effects at lower currents, become first order determinants of performance. One result is an increased sensitivity to reverse gate bias.

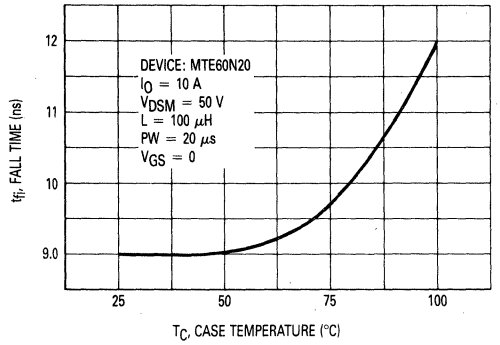


FIGURE 10-11 — FALL TIME versus CASE TEMPERATURE

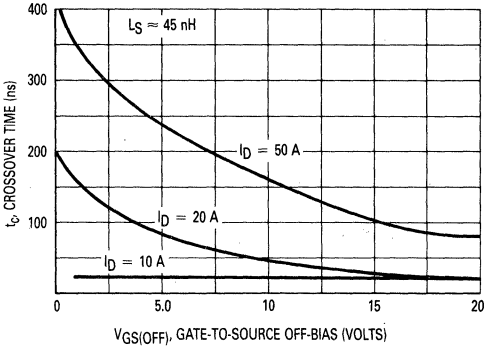


FIGURE 10-12 — CROSSOVER TIME versus OFF-BIAS WITH LARGER L_S

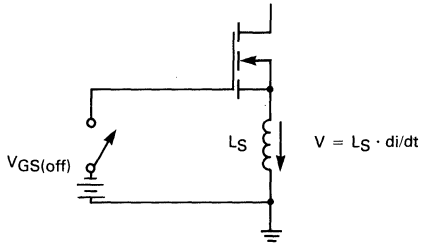


FIGURE 10-13 — PARASITIC SOURCE INDUCTANCE

Consider the circuit in Figure 10-13. As drain current (hence di/dt) is increased at turn-off, the voltage developed across parasitic inductance L_S increases. Since this voltage is in a direction to positively bias the gate, it is a limiting factor on switching speed.

Counteracting the voltage developed across L_S, with negative gate bias improves switching time and generates the off-bias dependent performance at higher currents, Figure 10-12. Picking a few numbers off the curves illustrates this point. Whereas a 10 volt negative gate bias improves performance by only 10% with a 10 A drain current, when current is increased to 50 A, the 10 volt bias reduces crossover time by a factor of four.

The data that was used to generate Figure 10-12 was taken in a circuit where L_S is determined by 1½ inches of #16 wire and a similar length of PC board ground plane. The data was retaken with the layout modified such that these dimensions are reduced to a total of ½ inch, reducing L_S by approximately 30 nH. The results appear in Figure 10-14. Note that the sensitivity to off-bias has been dramatically reduced by minimizing L_S. Note also that as L_S is reduced, the MOSFETs inherent insensitivity to current density becomes more apparent.

At high speeds, the presence of the gate suppression resistors also slightly modifies the phase relationship between the gate-source terminal voltage and the drain current. Figure 10-15 illustrates the delay between the fall of the gate voltage, as measured at the terminals, and the drain current fall time.

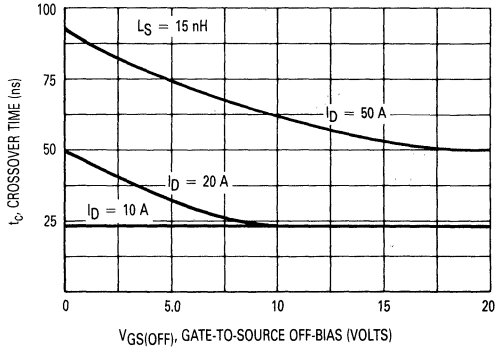


FIGURE 10-14 — CROSSOVER TIME versus GATE OFF-BIAS WITH LOWER L_S

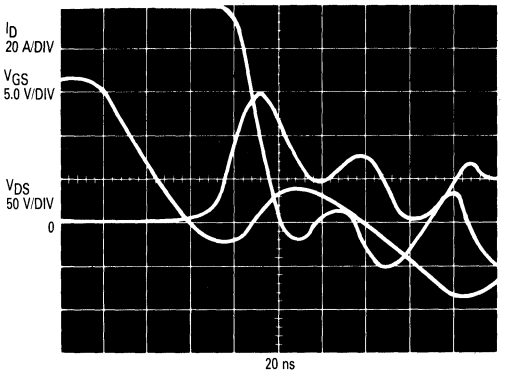


FIGURE 10-15 — V_{GS} — I_D DELAY DUE TO GATE SUPPRESSION RESISTORS

Comparison of Power MOSFETs and Bipolars in the EMS Package

At present, two technologies incorporating the EMS package have been introduced, the Switchmode High-Voltage Darlington MJ10041 series (250 V to 850 V, 25 A to 100 A, 250 W) and the low voltage MTE100N06 series of TMOS devices (50 V to 200 V, 60 A to 100 A). All of these new and potential products have certain applications in the energy management field, from low-voltage motor controllers to high-voltage, off-line, switching regulators and converters. Optimum matching of the product to the application will depend upon current and voltage capability, drive requirements, saturation voltage and switching speeds, all of which result in power dissipation and device/system efficiency.

RELATIVE EFFICIENCIES

To measure the relative efficiencies of the various technologies that can be incorporated in the EMS package, the low-voltage, medium-current power MOSFET MTE100N06 was compared to other experimental product, which, for a direct comparison, were of similar die size and, therefore, of similar current rating (25 A/die for the bipolar and 20 A/die for the Darlington). Consequently, all comparative testing of these three die packages were run at commensurate peak currents of 30 A. Forced β was set either to conform with that of the individual die data sheet specification or high enough to ensure device saturation (Table 3). As an example, the low β, low voltage, bipolar transistor had forced β of about 12 ($I_{\beta 1}$ = 2.5 A) and the low-voltage, high-β Darlington, forced β of about 250 (120 mA).

A simple way of measuring the relative efficiency of a device is to measure the case temperature rise under power; this technique not only measures the output dissipation losses — both static and dynamic — but also the input loss resulting from base-drive (or gate-drive) currents. Thus, a low-β bipolar would contribute higher input loss than a high-β Darlington.

TABLE 3 — Characteristics of EMS Test Devices

Type	Single Die				3 Die EMS			Figure	
	Device Equivalent	Die Size	$I_{C(max)}$	$h_{FE(min)}@I_C$	Forced h_{FE}	I_{B1}	I_{B2} (−5.0 V)	R_E	R_{BE}
LV Bipolar	2N5886	192 mils^2	25 A	20 @ 10 A	12	2.5 A	4.5 A	2.0 Ω 10 W	47
LV Darlington	2N6283	200 mils^2	20 A	750 @ 10 A	250	120 mA	1.6 A	43 2.0 W	100
MTE100N06, LV MED I TMOS		214 mils^2	100 A (3 DIE)	—	—	—	—	12 Ω	1.0 k
MJ10048, HV MED I DARL.		264 mils^2	100 A (2 DIE)	50 @ 50 A	Large die, not tested				

RESISTIVE LOAD TEST

Of interest in measuring efficiency is the effect of frequency on the dynamic switching loss, particularly at higher frequencies. In a similar manner, when static losses predominate, the performance of a device at low frequency is important. With this in mind, a resistive-load, variable frequency switching-loss (temperature-rise) test was conducted.

The duty cycle was set for 50% and the load current for 30 A($V_{CC} \approx 22$ V, $R_L = 0.67$ Ω, 600 W) using wire wound load resistors. These resistors are partially inductive and thus the maximum frequency before inductive rise times limit waveform integrity was about 12 kHz (Figure 10-16). All devices under test (DUTs) were bolted to the same heat sink, a relatively small (4″ x 4″ x 1/8″) copper plate used to produce higher than normal case temperatures for greater measurement differentials.

The DUTs were also tested with off-bias produced by a transistor clamp between the input of the device and a negative supply voltage (Figure 10-17). The bipolar and Darlington had a $V_{BE(off)}$ of −5.0 V to allow rapid "sweeping out" of the stored charge.

Since this low-voltage Darlington does not have a speed-up diode across its input transistor emitter-base, $V_{BE(off)}$ has little effect in improving the turn-off switching time of the output stage. This is evident by its extremely high case temperature of about 175°C when switched at 12 kHz (Figure 10-18). Also, the Darlington, due to its highest saturation voltage, had the greatest temperature rise, about 80°C at 1.0 kHz.

For the power MOSFET, off-bias allows the input capacitance C_{iss} to be quickly discharged, thus improving turn-off times. For this exercise, series-connected gate resistors of 50 Ω and 10 Ω were used to decrease the exceedingly fast turn-off dv/dt with off-bias voltages $V_{GS(off)}$ of 0 V and −5.0 V, respectively. The effect of off-bias and gate resistors on temperature rise is illustrated by the three MOSFET curves between 7.0 kHz and 12 kHz. As expected, the lower gate resistor and higher $V_{GS(off)}$ produce the lowest case temperature, about 68°C relative to 80°C at 12 kHz. By comparison, although not illustrated, when no off-bias or series gate resistor was used, the FET case temperature rose to about 170°C at 7.0 kHz.

Also of interest is that the power MOSFET ran slightly cooler at low frequencies than the comparably sized bipolar, indicating a lower ON voltage (415 mV relative to 650 mV at 30 A). This calculates to an $r_{DS(on)}$ of 14 mΩ (spec is 18 mΩ max at 50 A).

THE EFFECT OF MICA INSULATORS

These tests were run with the DUT bolted directly to the copper heat sink using only a silicon heat sink compound (Dow Corning 340). To determine the effect of mica insulators and mounting torque on thermal resistance $R_{\theta JS}$, measurements were made using a 4.0 mil and a 3.0 mil thick mica washers torqued down to the data sheet maximum mechanical rating of 8 in-lb. The changes in thermal resistance $\Delta R_{\theta CS}$ for the 3.0 mil and 4.0 mil washers over that of the no washer case were about 0.1°C/W and 0.3°C/W, respectively. When the mounting torque was reduced to 4 in-lb. for the 3.0 mil washer, no measurable difference in $R_{\theta CS}$ was noted.

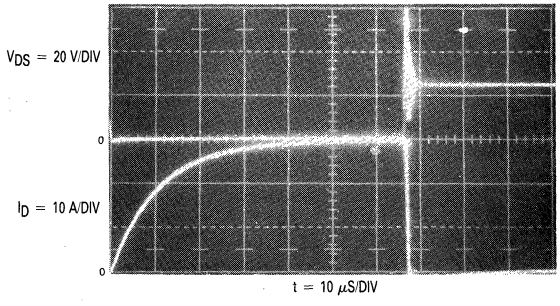


FIGURE 10-16 — RESISTIVE LOAD SWITCHING USING THE MTE100N06 POWER MOSFET

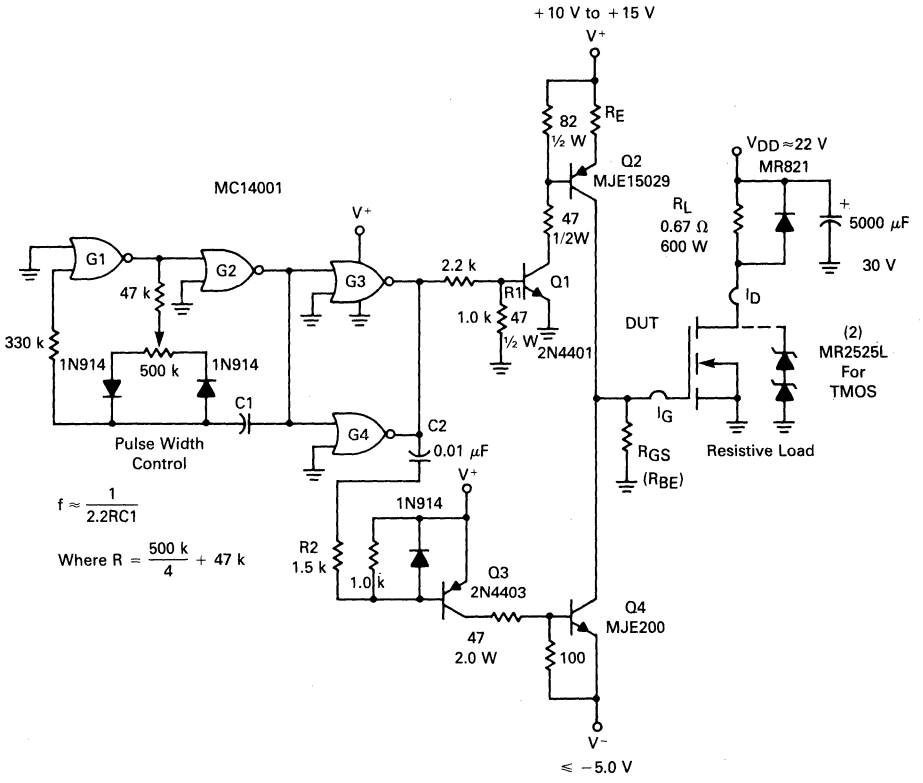


FIGURE 10-17 — TEST CIRCUIT FOR DRIVING DUTs

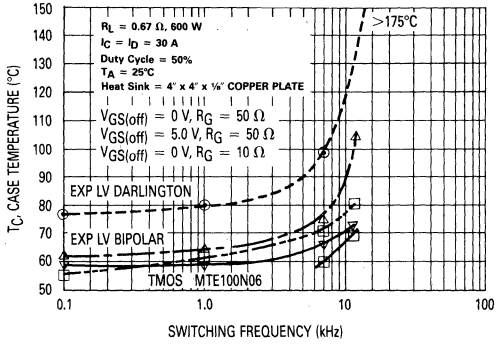


FIGURE 10-18 — CASE TEMPERATURE OF THE EMS PACKAGE FOR A RESISTIVE LOAD AS A FUNCTION OF FREQUENCY

TEST CIRCUIT

The test circuit used for driving the DUTs is shown in Figure 10-17. It consists of a buffered (gates G3 and G4 in parallel), CMOS astable multivibrator (gates G1 and G2), for frequency and pulse-width generation, driving the I_{B1} and $V_{BE(off)}$ (or I_{B2}) power amplifier. The positive going output of the MV turns on NPN transistor Q1 and the following PNP constant-current-configured transistor Q2, supplying up to as much as 8.0 A of I_{B1} to the DUT. Off-bias, coincident with the trailing edge of the input pulse, is provided by the negative-going differentiated pulse formed by C2-R2 turning on the following PNP transistor, Q3, and the NPN clamp transistor, Q4. Thus, the stored charge is swept out by this I_{B2} circuit, which, with the component values shown, can reach about 7.0 A peak when V− equals −5.0 V.

Chapter 11: Characterization and Measurements

FBSOA of Power MOSFETs

Power MOSFETs are essentially free of second breakdown; at least in the sense that second breakdown is defined for bipolar transistors. If second breakdown is defined as a region in which total allowable power dissipation decreases as drain-source voltage increases, the power MOSFETs do exhibit a second breakdown behavior. However, this phenomena occurs at power levels in excess of the device rating. In terms of measured safe-area capabilities, power FETs commonly show higher power dissipation capability at lower voltages than they do at voltages approaching $V_{(BR)DSS}$.

The phenomena which causes apparent second breakdown in FETs is similar to bipolar second breakdown in that increasing drain-source voltage widens depletion regions, allowing less of the silicon area to be used for current conduction. In FETs, higher voltages constrict the vertical channel somewhat, reducing the total area for current conduction and the maximum power dissipation capacity. Unlike bipolar transistors, there is no regenerative action associated with the current constriction. Its effects, therefore, are much less severe; so much so that FETs are generally regarded as being free of second breakdown. In general, consideration of the thermal ratings is all that is required when devices are operated within their current and voltage ratings.

To ensure that the power MOSFETs do not exhibit any limitation within the thermally limited portion of the FBSOA curve (the theoretical locus of constant power based on the thermal resistance), the DUTs were subjected to energy levels beyond the curve. As in turn-off switching SOA, a non-destruct tester would be advantageous, allowing one DUT to be used to generate a complete curve.

An important advantage of a non-destruct fixture is that it can give individual device trends and, from that, clues to the actual failure mechanism. Some have indicated that a steepening of the SOA slope at high-voltage, low-current indicates breakdown due to negative resistance effects (44,45).

The non-destruct fixture is also safer and is easier on larger power supplies. If a destructive tester were to short out a device, there is nothing to limit the current flow until the device heats to the point of opening up. This non-destruct fixture turns off the power supply and harmlessly dissipates the energy in the circuit.

Basic Theory

When a power MOSFET is operated just outside its SOA, the drain current, I_D, will suddenly increase very rapidly as the device breaks down. Unless the energy can be removed very quickly, the device will be destroyed. The basic idea of the non-destruct fixture is to sense this current surge and divert the energy from the Device Under Test as rapidly as possible. The fixture reacts within approximately 100 ns and usually saves the device.

Circuit Description

The circuit performs three main functions. First, it controls the desired drain-source voltage, V_{DS}, drain current, I_D, and pulse width in order to provide a defined energy to the DUT. Second, it protects the device just as it starts to fail; and third, once an overstress is detected, it removes power from the system.

The N-channel circuit is shown in Figure 11-1 and will be described. (The P-channel circuit is virtually identical except for inversion of power supplies, logic outputs and complementary transistors.) Controlled drain current is applied to the common source connected power MOSFET by means of the feedback loop around its gate-source with op-amp U1 being the error amplifier. The loop will force the source voltage (developed across the drain current sense-resistor R1) to be equal to the reference voltage that is applied to the non-inverting input of U1. The gate-source voltage will automatically assume that value required to produce the required drain current. Thus, by varying the reference voltage by means of the I_D Adjust control, a defined, accurate drain current can be chosen.

Drain-source voltage is applied to the DUT through a current-limiting inductor L1 (to reduce short-circuit current) and a series-connected Darlington NPN switch, Q9. Thus the drain voltage is approximately equal to the V_{DD} power supply (neglecting the $V_{CE(sat)}$ of Q9).

The series Darlington, configured as an emitter-follower, is controlled by level translating NPN high voltage transistor, Q7, and the following PNP high voltage transistor, Q8. Transistors Q8 and Q9 are in effect a compound Darlington and Q7 acts as a current source to minimize drive variations when V_{DD} is varied. System operation begins by applying a positive-going pulse by means of an external pulse generator to the base of Q7, thus turning on the switched drain supply. The gate is also turned on, but is slightly delayed by the R3C1 base integrating circuit of the unclamped transistor Q1 to minimize turn-on stress on the DUT.

A fast video amplifier, U2, also monitors the DUT source, looking for a current spike. This amplifier, connected to produce a voltage gain of 200 with a bandwidth of 40 MHz, will quickly detect the advent of the destructive current spike and amplify it to a level to trigger a fast discrete R/S flip-flop.

To "lock-out" false signals that may occur due to device turn-on, an N-channel FET series switch, Q2, is connected between the video amp and the flip-flop. This FET is controlled by PNP driver, Q10, NAND Gate, G3, and input-pulse-triggered monostable multivibrator G1 and G2. Thus, by varying the Pulse Width Adjust, R4, the first 5.0 to 50 ms of the switched drain current can be blanked to prevent false triggering of the circuit.

A "true" trigger will turn on PNP transistor Q3 of the flip-flop whose output is buffered by NPN transistor Q5. The positive-going signal will then turn on the fast crowbar power MOSFET Q6, thus quickly diverting the energy from the DUT. The high level flip-flop output from Q3 will also turn on the LED — indicating a crowbar occurrence — and clamp off the input pulse generator by means of turned on transistor Q11. Consequently, Darlington Q9 is

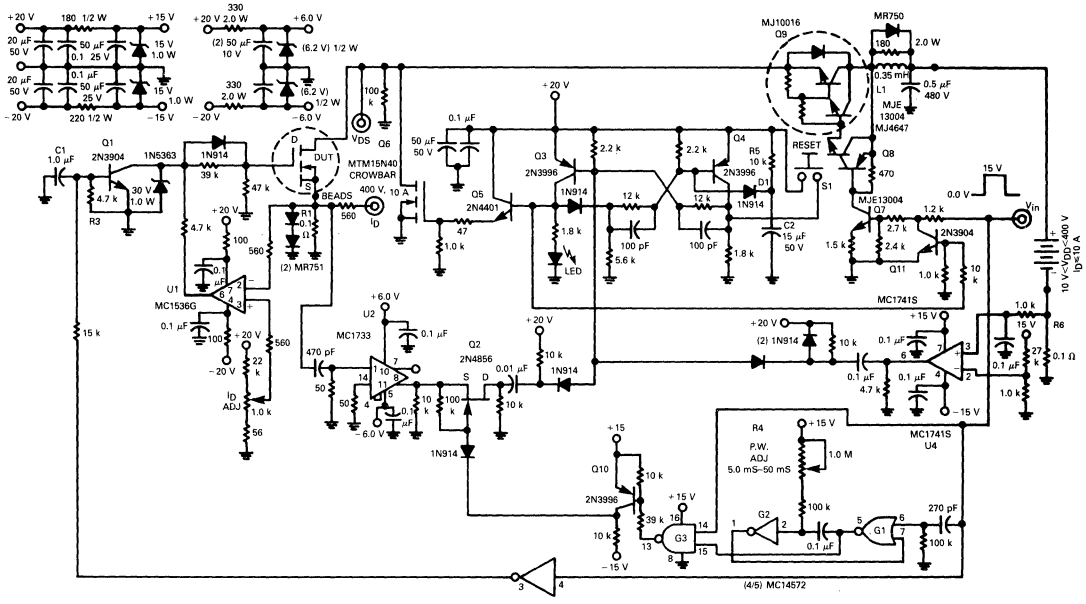


FIGURE 11-1 — N-CHANNEL POWER MOSFET NON-DESTRUCT FBSOA TESTER

also turned off. To protect the crowbar FET and Q9, which are both on for about 30 μs due to propagation delays, current limiting inductor L1 is placed in series with the power loop.

The system is reset by depressing push-button S1, thus placing the flip-flop in the proper state. The resistor R5, capacitor C2 and diode D1 network in the base circuit of Q4 ensure that the flip-flop will be in the proper state when power is first applied.

The circuit also has over-current protection. A second current sensing resistor R6 in the return bus of the V_{DD} supply monitors the input current and activates the flip-flop if more than 10 A is sensed. This is accomplished by comparator U4 and its associated pulse steering circuitry.

The P-channel fixture shown in Figure 11-2 is nearly identical to the N-channel except that it contains its own pulse generator and its supplies and transistors are inverted. The pulse generator uses a quad, two input NOR gate to produce the required astable multivibrator (A1 and A2) that clocks the following monostable multi-vibrator (A3 and A4).

Testing Mechanics

The intended use of the FBSOA test fixture is to ensure that device operation is limited only by its specified power rating based on a measured $R_{\theta JC}$ and not a second breakdown of the parasitic bipolar transistor or any other phenomena.

To determine if the device was actually facing failure when the fixture crowbarred, V_{DS} was held constant and I_D was gradually increased with successive pulses until the fixture crowbarred. Then the crowbar was disabled and the device was pulsed again. The device would fail indicating that the crowbar was only being activated when the device was beginning to fail.

Normally, a one second pulse was used, but other pulse durations were investigated. Time was allowed between pulses for cooling. A two second pulse did not significantly change the FBSOA curve. The device would handle about 20.0% more power during a 0.1 second pulse and the slope of the FBSOA curve remained the same (Figure 11-3).

During a 10 ms pulse, the device handled another 20.0% more power before failing. Since the blanking period lasts at least the first 5.0 ms of the 10 ms pulse, the fixture had difficulty saving units at this high energy level. The implication of this test is that the mechanism causing crowbarring is energy (time) dependent, tracking somewhat the thermal response of the device. Presumably, the junction temperature when the fixture crowbars is about the same for all pulse width variations.

Careful testing, i.e., slowly increasing the energy level, can ensure multiple crowbar activations of the DUT. One N-channel device went through 30 crowbars with no degradation in $r_{DS(on)}$, leakage current or drain-source breakdown voltage. Parts were either saved without degradation or destroyed, usually shorted from drain-to-source.

The case temperature of the TO-220 MTP5N20 ($R_{\theta JC}$ = 1.67°C/W), using a large finned, air cooled heat sink, rose to about 120°C when the DUT activated the crowbar. The applied power of 150 W thus produced a calculated junction temperature of about 370°C. At first glance, the Motorola parts appear to be rated with a fair amount of guardband. The actual FBSOA guardband is even larger since the rated curve assumes a case temperature of

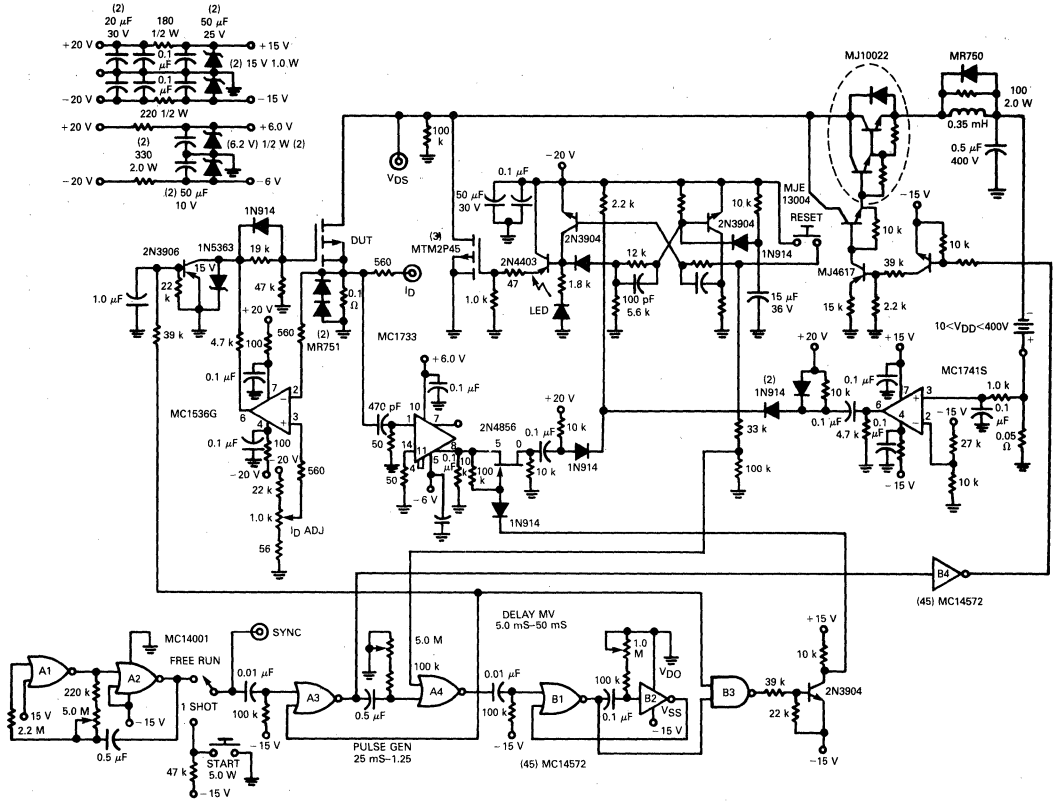


FIGURE 11-2 — P-CHANNEL POWER MOSFET NON-DESTRUCT FBSOA TESTER

25°C and the measured curve was derived at an elevated case temperature. Nevertheless, to ensure reliability, the user must operate the power MOSFET within the specified thermally limited curve.

RESULTS OF TESTING ONE PART ALONG THE ENTIRE CURVE

Many of the N-channel curves turned out to be very linear when plotted on log-log paper (Figures 11-3, 11-4). Within the same product line, the slope was very similar from device to device and always steeper than the −1.0 slope of the constant power dissipation curve. The plots from product line to product line also tended to be tightly clustered, with slopes varying from about −1.2 to −1.5 over the eight different lines tested.

Some have reported a steepening of the SOA curve at higher voltage and that this is due to a negative resistance phenomena. This occurs when avalanche breakdown takes place in the drain junction which increases I_D. Because of the finite resistance of the substrate, the increase in I_D causes an increase in the potential in the substrate. If I_D and the substrate resistance are large enough, the source junction can become forward biased, which would intensify the avalanche multiplication. N-channel devices with short channels are susceptible to this phenomena, but the problem can be alleviated by decreasing the substrate resistance or increasing the channel length. This negative resistance effect on SOA is illustrated in Figure 11-5. The intent is to compare slopes and not to compare power handling capabilities of equivalent die sizes (43,44,45).

Testing indicates that the Motorola Power MOSFETs are not influenced by the negative resistance effect even though they utilize very short channels to decrease on-resistance. This is because of the additional P+ plug that is diffused beneath the source contact. When the device goes into avalanche breakdown, as illustrated in Figure 11-6b, the preferred avalanche current path is from N substrate through the P+ plug and into the source. This keeps the forward voltage drop of the source junction low, or below turn on. This avalanche current is quite possibly the current surge that the FBSOA tester detects when the fixture activates the crowbar.

At still higher power levels current may flow, as in Figure 11-6c, increasing the voltage in the P region. The forward voltage drop across the source junction may rise to above turn-on, establishing the negative resistance phenomena. This produces a positive feedback mechanism because the source is now injecting electrons into the substrate and thus intensifying the avalanching, effectively turning on the parasitic transistor. Such an avalanche injection would most likely destroy the device.

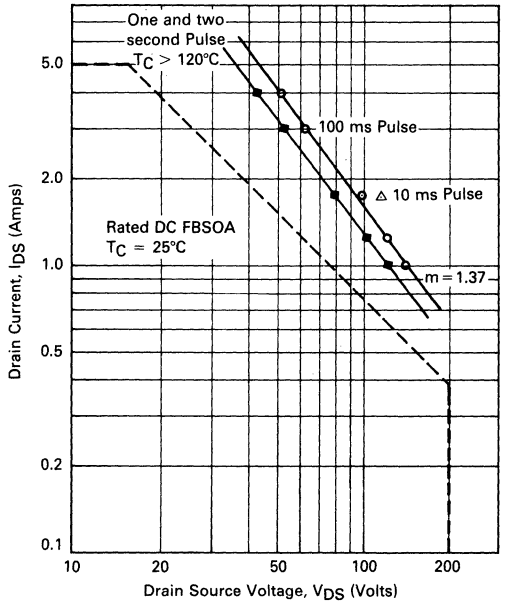


FIGURE 11-3 — DC FBSOA OF MTM5N20

The questions "Why does the empirical FBSOA slope deviate from the −1.0 slope of constant power?" and "What is the significance of the slope on the SOA curves?" still remain. Since thermal resistance of bipolars decreases with increasing current at a constant power level, it was thought that the same may be true for power MOSFETs and that this could steepen the SOA slope (46). If $R_{\theta JC}$ increases with voltage (decreasing current), the device would not be able to dissipate as much power at the high voltage, low current end of the curve.

To investigate this premise, many thermal resistance measurements were taken on the DUTs, all at a constant power level, but varying I_D and V_{DS} (V_{DS1} I_{D1} = V_{DS2} I_{D2}, etc.). A thermal resistance fixture that used a switching technique to measure the voltage drop across the parasitic drain-to-source diode was used initially. The inherent measurement error in this method tended to suppress any trends in the variation of $R_{\theta JC}$ with I_D.

A second method that measures the junction temperature of a decapped device with an infrared microradiometer proved to be more accurate. The instrument read out an average temperature of about 10.0% of the die area that was located in the center or the hottest part of the chip. Again, I_D and V_{DS} were varied while P_D was held constant. As shown in Figure 11-7, $R_{\theta JC}$ does decrease with increasing I_D at a constant P_D, like bipolars, but the 10.0% change in $R_{\theta JC}$ is not enough to account for the approximate 30.0% change in power handling capabilities (m = 1.4). Although $R_{\theta JC}$ varies and does steepen the FBSOA slope, it has only a partial effect under these test conditions. These results must be qualified because the equipment did not allow the measurement of $R_{\theta JC}$ at a power level near the FBSOA limits where the change in $R_{\theta JC}$ could be more or less significant.

The failure mechanism and thus the slope of the curves obtained from the FBSOA test fixture, is a function of junction temperature, V_{DS}, I_D and a variable thermal resistance. Because the junction temperature rose so high, the device could be going into avalanche breakdown which would be a strong function of V_{DS}, as the curves indicate. This temperature at failure is above $T_{J(max)}$ ratings and demonstrates why users must not exceed published SOA curves.

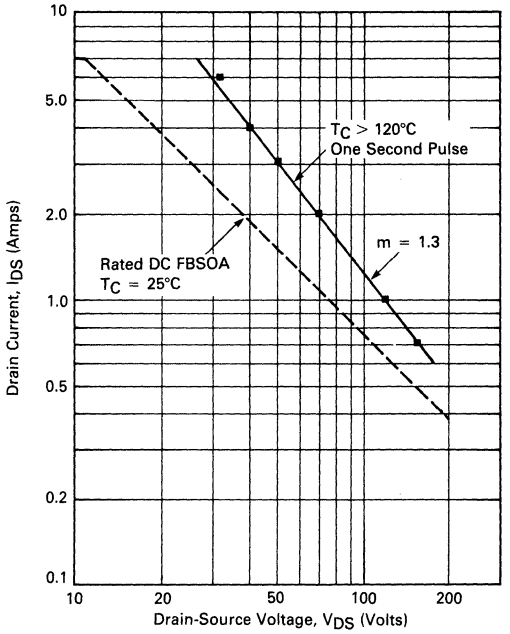


FIGURE 11-4 — DC FBSOA TEST ON MTP7N20

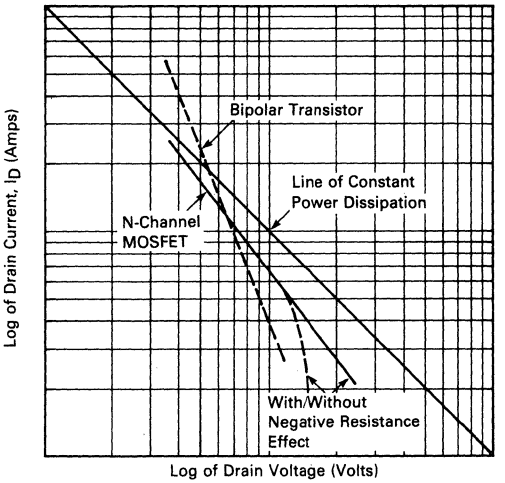


FIGURE 11-5 — COMPARISON OF TYPICAL FBSOA SLOPES

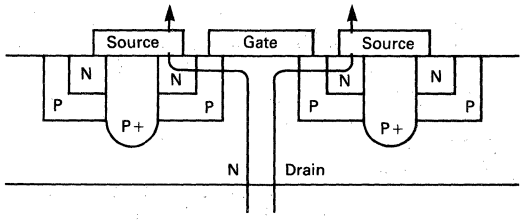


FIGURE 11-6a — TYPICAL CURRENT FLOW IN TMOS POWER MOSFET

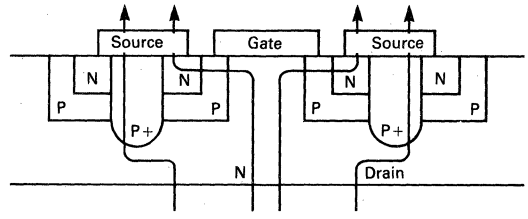


FIGURE 11-6b — CURRENT FLOW DURING AVALANCHE

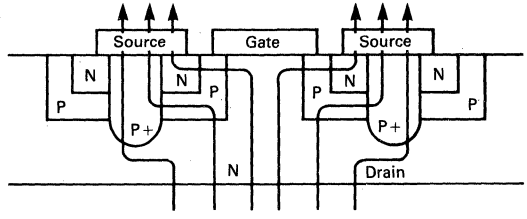


FIGURE 11-6c — CURRENT FLOW DURING NEGATIVE RESISTANCE BREAKDOWN

Since power MOSFETs or, for that matter, bipolar transistors, do change their thermal resistance as operating conditions vary, this could warrant a change in the published SOA curves. The thermally limited portion of the curve is presently based on one thermal resistance reading taken at a single operating condition. If this is a worst case reading (taken at low current, high voltage), this could significantly underrate the device at the high-current, low-voltage portion of the curve. Conversely, if the reading is taken at the high-current end, this could overrate the device at the low-current end. Further study needs to be done to determine if the change in $R_{\theta JC}$ is significant enough to alter the way manufacturers derive published SOA curves.

The significance of the slope greater than minus one, as accurately derived from the non-destruct FBSOA tester, is that a simple power limit of, say, 75 W may not be appropriate because it could overrate a device under certain conditions and underrate the same device at the same power level but lower voltage and higher current. Motorola establishes conservative derating of $R_{\theta JC}$ to ensure reliable operation under all bias conditions.

Turn-off Switching SOA of Power MOSFETs

One of the advantages of power MOSFETs over bipolars is its superior reverse bias safe operating area (RBSOA) performance. Power MOSFET RBSOA curves are generally "square" at $I_{D(max)}$ and $V_{(BR)DSS}$, (Figure 11-8) indicating that performance is bounded only by maximum voltage and maximum pulsed current ratings. In other words, MOSFETs are not generally RBSOA limited. There are possible exceptions to this rule, however. As noted in the dv/dt section outlined earlier in Chapter 4, rapid changes in drain-source voltages can limit the RBSOA (turn-off switching SOA) capability of the MOSFET due to the injected current into the C_{rss} capacitance inadvertently biasing-on the MOSFET.

Many practical power loads are inductive which can cause severe stress on the power switching device during turn-off. Due to the nature of an inductive load line, the switch, be it a power MOSFET or bipolar transistor, can simultaneously experience a high current and high

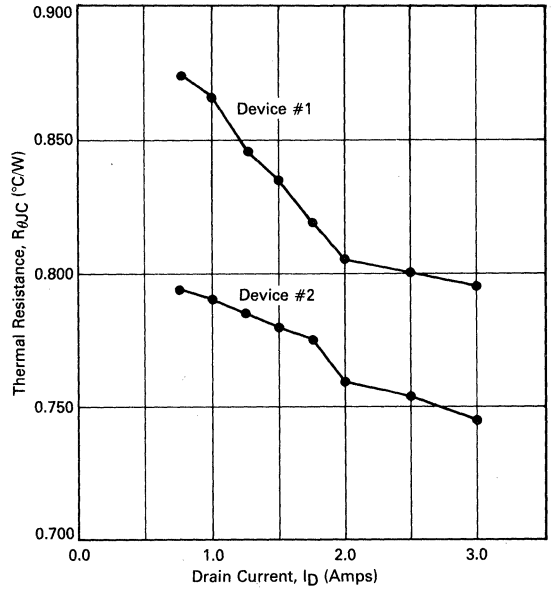


FIGURE 11-7 — THERMAL RESISTANCE OF MTM12N10 versus DRAIN CURRENT AT P_D = 50 W

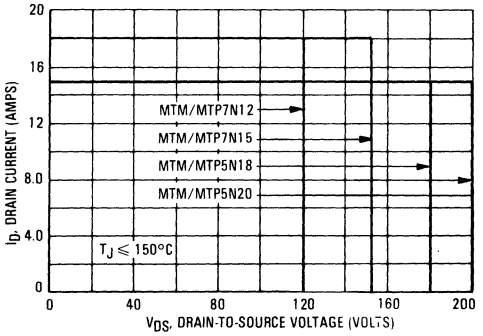


FIGURE 11-8 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

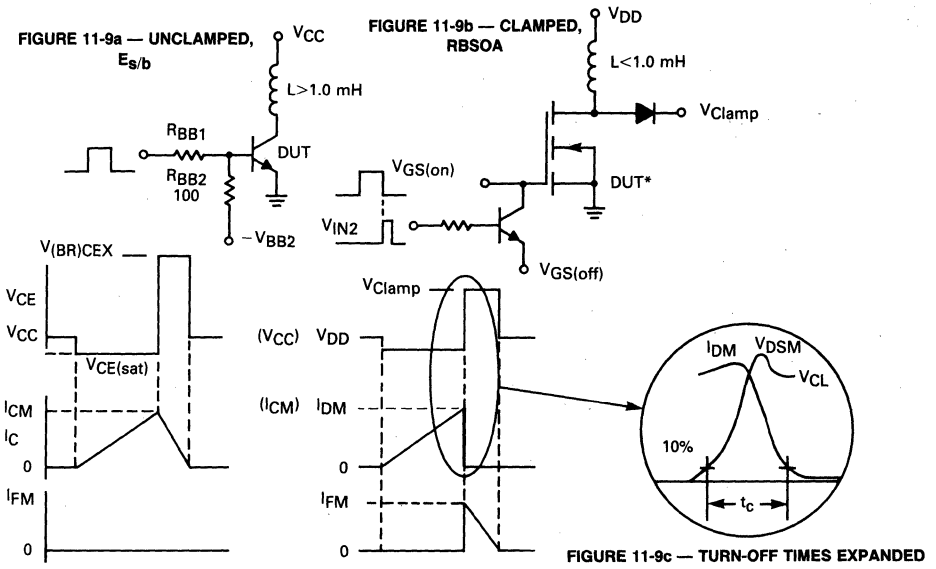
voltage. Depending on whether the switch is unclamped (Figure 11-9a) or protected with a clamp circuit (Figure 11-9b) will determine the two energy limitations during inductive turn-off: Second Breakdown Energy ($E_{S/b}$) and RBSOA.

SECOND BREAKDOWN ENERGY ($E_{S/b}$)

Power transistors were originally characterized with an unclamped inductive load (Figure 11-9a). The Device Under Test (DUT), typically a low voltage, extremely rugged transistor, is turned on by applying a positive pulse to its base through a resistive network terminated in a reverse bias voltage V_{BB2}. Collector current then ramps up at a rate dictated by the time-constant of the relatively large inductance in the collector circuit. When the DUT turns off, the energy stored in the inductor ($E = 1/2LI_{CM}^2$) has to be dissipated in the transistor since there is no external circuit, or clamp, to "catch" this energy as the current ramps down. Also, immediately at turn-off, the collector-emitter voltage flies back up due to the "inductive kick" ($v = L\ di/dt$). If the stored energy is great enough and the transistor turn-off time fast enough, this voltage will fly back to the breakdown voltage of the device ($V_{(BR)CEX}$), causing the transistor to avalanche. The transistor thus has to dissipate the energy due to this unclamped operation by sustaining its breakdown voltage until the collector current falls to zero and the inductor discharges. The maximum energy that the device can sustain, defined as Second Breakdown Energy ($E_{S/b}$), is determined by increasing the collector current until the device fails. Usually this current is below the nominal operating current of the device since the transistor has to absorb the relatively high inductor energy and generally cannot sustain its maximum specified current. Theory and practice have shown that most low-voltage transistors have decreasing $E_{S/b}$ capability with increasing reverse-bias voltage due to current crowding.

The unclamped inductive loads stress the power MOSFET in a similar manner. Now, the falling drain current will cause the flyback voltage to avalanche the drain-source of the MOSFET ($V_{(BR)DSS}$).

The problem with this $E_{S/b}$ rating is that the derived energy is only related to that particular inductance and is highly dependent on its Q (quality factor, i.e., series re-



*Waveforms shown for MOSFET DUT.
Bipolar Terms in Parentheses.

FIGURE 11-9 — INDUCTIVE LOAD SWITCHING

sistance). Additionally, the inductance specified to achieve $E_{S/b}$ is generally quite large, 10 mH or greater, and does not represent the real world inductance seen in Switchmode applications. Finally, and most important, most applications use some form of clamping to prevent drain-voltage breakdowns. For this reason, most high voltage switching transistors are specified with a clamped inductive load.

RBSOA

A more precise and definite inductive turn-off rating is the clamped inductive turn-off rating labeled RBSOA. In the simplified test circuit of Figure 11-9b, the DUT is subjected to a real world clamped condition. The inductance need be only large enough to ensure that the flyback time is greater than the drain current fall time, generally resulting in inductances from 100 μH to 1.0 mH. These values also more accurately represent the leakage inductances encountered in switching applications.

To subject the device to the greatest stress during turn-off, the inductance should be of high Q to ensure that the peak drain current, I_{DM}, and flyback voltage, V_{DSM}, are simultaneously presented to the DUT, Figure 11-9c, resulting in a turn-off load line that approximates a rectangle. Under these conditions, I_D will start to fall when V_{DS} forward biases the clamp diode, at which time the stored inductor energy (current) will be transferred to the external diode circuit.

To determine the RBSOA capability of the device, I_{DM} is set to a typical operating current and the clamp voltage is increased until the transistor goes into second breakdown. Then other current levels are tested until the complete RBSOA curve is established. These second breakdown points relate to the energy dissipated in the device during turn-off, specifically the crossover time t_c, (Figure 11-9c) and represents the energy encountered in inductive switching applications, (whereas, the lower I_{DM} for the unclamped $E_{S/b}$ mode does not). Reverse biasing in this example is provided by a transistor clamp from the gate of the N-Channel MOSFET to either a negative voltage or ground.

SWITCHING SAFE OPERATING AREA (SSOA)

The term Switching Safe Operating Area is the generalized SOA limitation during turn-on and turn-off of the power MOSFET. Turn-off switching SOA is equivalent to RBSOA for bipolar devices and will henceforth be used to describe this characteristic.

The straightforward method of determining the turn-off switching SOA is through destructively testing the power MOSFET in the clamped inductive turn-off circuit. This is accomplished by setting the drain current to a specified value by either adjusting the applied input pulse width (t_{PW}) or the drain supply voltage V_{DD} since $I_D \cong \frac{V_{DD}\, t_{PW}}{L}$. Then the clamp supply voltage is gradually increased until one of two conditions occurs. If the specified I_D is less than the I_{DM} rating, the clamp voltage can be increased until the device avalanches and begins dissipating the inductor's energy. Since the MOSFET is operating in an $E_{S/b}$ mode at this point, failures may occur.

At drain currents greater than I_{DM}, the device is operating outside its current ratings and the MOSFET may fail at clamp voltages less than $V_{(BR)DSS}$. In short, the MOSFET's SSOA curves guarantee that the locus of failures is outside the I_{DM} — $V_{(BR)DSS}$ boundaries. The SSOA curve shown in Figure 11-8 is applicable for both turn-on and turn-off of devices with switching times less than one microsecond.

Normally a destructive fixture is used to ensure that the fail points lie outside the turn-off SOA boundaries. This requires testing of many devices and device trends are difficult to determine. The use of a non-destructive fixture greatly simplifies establishing the SSOA ratings since usually only one DUT can be used to generate a complete turn-off switching SOA curve.

N-CHANNEL NON-DESTRUCT TURN-OFF SWITCHING SOA TEST FIXTURE

In order to save the DUT from the normally destructive second breakdown energy, the stored inductive energy must be quickly diverted from the transistor to an external crowbar circuit. A test fixture, based on the work done at the United States National Bureau of Standards,[31] was designed to have the capability of crowbarring as much as 50 A and blocking as much as 1000 V. The 10 A crowbarred propagation delay was about 70 ns and the current rise time was about 40 ns. Triggering of the crowbar was accomplished by detecting the fast rate of change of the collapsing drain-source voltage once the device went into second breakdown. Using this test fixture, a complete SOA curve can often be formed using only one DUT; consequently, the DUT must sustain as many as 30 or 40 crowbars (second breakdowns) to establish the curve. Not all devices will survive so many crowbars without degradation or failure, but a large percentage do, allowing a relatively simple and non-ambiguous curve to be generated. Degradation is measured by a relatively large change in drain leakage current, I_{DSS}, after testing. For this magnitude of leakage current change, subsequent retesting will usually show a decrease in device turn-off SOA capability.

The main elements of the non-destruct SOA test fixture are illustrated in the block diagram of Figure 11-10. Of these blocks the most important are the Drive Circuit consisting of the $V_{GS(on)}$ and $V_{GS(off)}$ Transistor Switches, the Detector/Crowbar and a Pulse Generator capable of being inhibited when crowbarring occurs. Of secondary importance are the V_{DD} Switch, and a Greater than 10% Duty Cycle Lockout circuit. Also required is an externally connected inductor, typically about 200 μH.

Referring to Figure 11-10, the circuit operates as follows: An input pulse, V_{in}, is applied to the input of the Drive Circuit controlling the three respective switches, $V_{GS(on)}$, $V_{GS(off)}$, and V_{DD}. The $V_{GS(on)}$ switch supplies the positive turn-on gate voltage and concurrent with its turn-off, the $V_{GS(off)}$ switch is turned on. The drain supply is also turned on (V_{DD} switch) when positive gate voltage is applied and, to ensure proper system operation, will remain on for several microseconds (due to drive transistor storage time) after removal of the input pulse. During this on-time, the collector current ramps-up and, upon

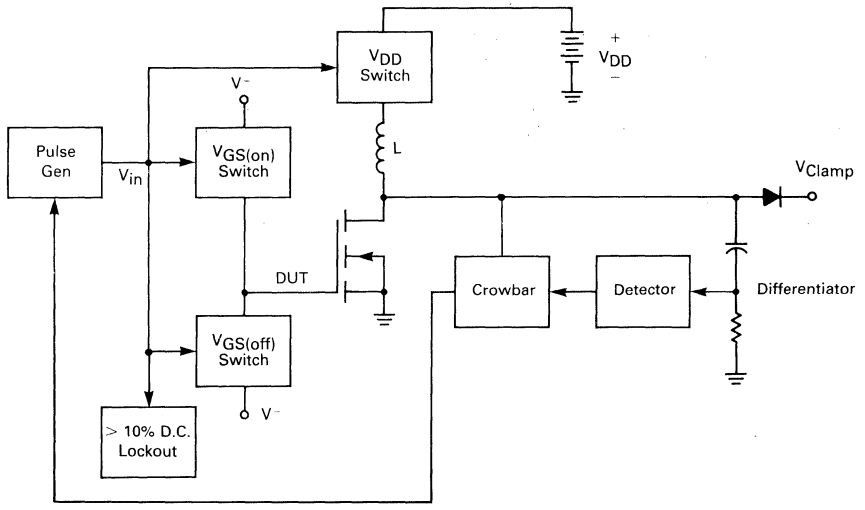


FIGURE 11-10 — BLOCK DIAGRAM OF THE N-CHANNEL NON-DESTRUCT TURN-OFF SWITCHING SOA TEST FIXTURE

turn-off, the drain voltage flies back. When the flyback voltage reaches the clamp voltage, the inductor current is transferred to the clamp circuit. The drain voltage will then fall at a relatively slow rate, typically a couple of hundred nanoseconds, as the energy stored in the inductor is completely discharged.

If, however, excessive energy is applied to the DUT during this switching time, the FET can go into second breakdown. Then the drain voltage falls very rapidly, possibly in less than 10 ns. When this occurs, the low R-C time-constant Differentiator detects this fast falling waveform — discriminating against the normal slow falling waveform — and produces a negative-going pulse which ultimately triggers the crowbar. The crowbar fires and the current in the DUT is quickly diverted to the crowbar, removing the turn-off energy stress from the transistor. The Pulse Generator is also disabled, preventing any successive pulses from being reapplied until the system is reset.

DRIVE CIRCUIT

The drive circuit for the SOA test fixture is shown in Figure 11-11 and consists of the three aforementioned switches. A Darlington transistor, Q1, is used to buffer the CMOS-derived input pulse of 15 V from the drive circuit.

Positive gate voltage is generated by turning on the NPN transistor, Q2, with the positive going input pulse. This stage supplies drive to the PNP Baker-clamp-configured transistor, Q3, whose output feeds the gate of the DUT, turning it on.

Reverse bias is derived by differentiating the input pulse with the R1C1 network. The generated negative-going pulse, which is coincident with the trailing edge of the input pulse, then turns on PNP transistor, Q4, and the following NPN transistor, Q5.

This off-bias voltage pulse is set by R1C1 and, for the values chosen, is about 10 μs. Also, due to the trailing edge coincidence of the two pulses (plus approximately equal propagation delays through the two respective switches), the transition time between $V_{GS(on)}$ and $V_{GS(off)}$ can be relatively fast for some DUTs and operating conditions, approaching less than 200 ns.

The drain switch is used as a safety device, removing current from the inductor if the DUT were to fail short. This circuit utilizes two cascaded Baker-clamped monolithic Darlingtons (NPN Q6 and PNP Q7) to reach the 50 A capability of the fixture. The Baker-clamp diodes (D3, D4 and D5, D6) minimize the storage time of this switch after the DUT is turned off.

Once the DUT is turned off, the inductor-stored energy is dissipated through the two clamp diodes (D7 and D8 for high-voltage capability), the clamp supply and filter network, and Q7 clamp diode D9. Diodes D10 and D11 in the drain circuit of the DUT are used to prevent reverse drain currents from flowing and also to ensure that the crowbar saturation voltage is lower than the parasitic transistor second breakdown voltage, thus diverting the drain current.

Drain current can be monitored by the current loop as shown. Additionally, the current-sense resistor, R2, can be used to monitor I_D, but care must be taken in the layout to minimize ground loops which can distort this current replica. As in any high-speed, high-current switch, good RF techniques should be used in the layout.

DETECTOR/CROWBAR CIRCUIT

As previously mentioned, an RC differentiator is used to discriminate between the normal V_{DS} fall time and second breakdown fall time; the components used are a 1.0 kV capacitor, C2, fixed resistor R3, and Sensitivity Control R4.

Originally, the output pulse from this network fired a 25 A

SCR as a crowbar, but the turn-on time of about 600 ns proved to be too long to save the DUT. What is required is a fast latching crowbar. This is now achieved by using a common-base-connected NPN transistor, Q10, as a level detector-pulse amplifier, triggering a fast, discrete monostable multivibrator (MV) consisting of PNP transistors Q11 and Q12. This 25 μs MV, which allows adequate time for the inductor stored energy to be dissipated, then drives the direct-coupled NPN transistor, Q13, and following PNP transistor, Q14, to a power level capable of turning on the crowbar. Diode D12 is used to block any noise pulses on the V_{DD} line from false triggering the monostable MV.

The crowbar consists of four parallel MJ10011 monolithic Darlington transistors (Q15–Q18) selected for V_{CEO} greater than 1000 V. This transistor, designed for horizontal deflection circuits, offers the best blocking voltage-switching speed tradeoff of the several different devices tested. By using fast, wide-band transistors throughout, propagation delay and rise time of 70 ns and 40 ns, respectively, were measured at an I_C of 10 A.

Diode D13 and resistor R5 prevent possible high dv/dt

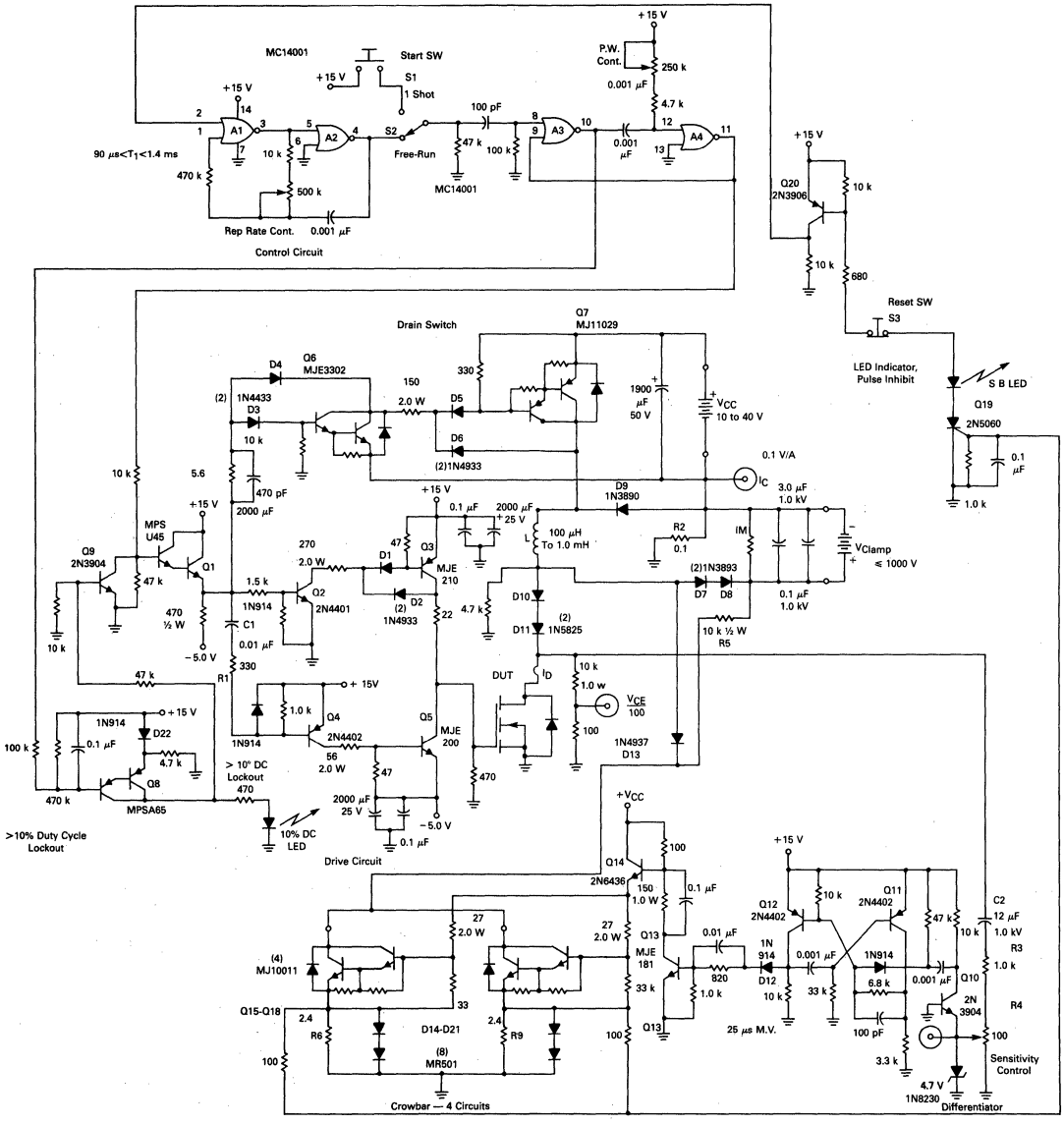


FIGURE 11-11 — N-CHANNEL POWER MOSFET NON-DESTRUCT TURN-OFF SWITCHING SOA TESTER 1000 V, 50 A

flyback voltages from falsely turning on the crowbar.

The resistor-diode networks (R6–9, D14–21) in the respective Darlington emitter circuits serve both as a ballasting-voltage clipping circuit and a crowbar indication source for the second breakdown LED indicator circuit.

PULSE GENERATOR

The timing functions for the Non-Destruct Turn-off SOA Test Fixture are generated by a quad, 2-input NOR gate, MC14001. These gates are configured as an astable MV (gates A1 and A2) clocking a monostable MV (gates A3 and A4) for pulse-width generation. By setting the Rep-Rate Control and the Pulse-Width Control, periods of from 90 μs to 1.4 ms and pulse-widths of 4.0 μs to 180 μs are achievable.

The Control Circuit produces free running pulses whose duty cycle should be maintained at less than 10% (limited by the driver circuit resistor power ratings). One-shot operation can also be generated by simply setting switch S2 to the one shot position and depressing the pushbutton start switch S1, thus providing a trigger to the Pulse-Width Mono MV.

COMPLETE N-CHANNEL NON-DESTRUCT SOA SYSTEM

Included in Figure 11-11, the complete N-channel Non-Destruct Turn-off Switching Tester, are two other circuits not previously described. They are:

1. The Greater Than 10% Duty Cycle Lockout Circuit.
2. The LED Indicator/Pulse Inhibit Circuit.

The 10% Duty Cycle circuit integrates the input pulse train with an RC network in the base circuit of the small-signal PNP Darlington MPSA65 (Q8). The resultant dc base voltage is compared with the emitter reference voltage derived from a 1N914 diode (D20). At duty cycles greater than about 15–20%, the Darlington will turn-on, lighting a LED indicator and turning on the NPN 2N3904 (Q9) transistor clamp across the input of the MPSU45 emitter follower (Q1). This effectively limits the duty cycle and the power dissipated in the drive circuit.

The LED Indicator/Pulse Inhibit circuit is enabled when the crowbar fires. The control signal is derived from the emitters of the Darlington crowbars and fed to the gate of the second breakdown SCR (Q19), turning it on. Placed in the anode circuit of this SCR are the series-connected second breakdown LED, reset switch (S3) and base biasing resistors for the 2N3906 pulse inhibit transistor (Q20). Thus, when the SCR fires, the LED will turn on, indicating second breakdown. The inhibit transistor will also turn on, placing the input to astable MV (A1) high, thereby disabling the pulse train. The system is enabled by opening (depressing) the normally closed pushbutton reset switch, thus unlatching the SCR.

Characterizing Drain-To-Source Diodes Of Power MOSFET For Switchmode Applications

When turning off inductive loads with a semiconductor switch, some means must be used to suppress, limit or clamp the resulting "inductive kick" from exceeding the breakdown voltage of the switch. Various types of suppressors or "snubber" circuits such as Zeners, MOVs, RC networks and clamp or "free-wheeling" diodes are generally used. The energy stored in the inductor is diverted from the transistor at turn-off and is harmlessly dissipated in the snubber, thus protecting the transistor switch.

To protect single power MOSFET switches, the snubber can be placed across either the inductor or the MOSFET. A Zener diode or RC snubber circuit can protect the drain-source of the power MOSFET but a simple clamp diode across these terminals will not, as it will only come into operation if its reverse blocking voltage is exceeded. However, in the multitransistor configurations commonly used for switching regulators, inverters and motor controllers, clamp diodes across the semiconductor switches are frequently used (Figure 11-12). The diodes do not protect their respective FETs but rather the complementary FET. As an example, in the totem-pole configuration of Figure 11-12c, diode D2 protects Q1 and D1 protects Q2.

To illustrate this, assume Q2 is initially conducting, causing load current to flow up through the inductor from ground. When Q2 turns off, the inductive current will continue but now through D1, through the power supply V^+ and return to the ground side of the inductor. Consequently, the fly-back voltage will be clamped to V^+ (from V^-), resulting in an amplitude of 2.0 V^+ when V^+ equals V^-.

If the output power devices are power MOSFETs with D-S diodes, the question arises as to whether these diodes are capable of adequately clamping the turn-off inductive load current. In other words, do the diodes switch fast enough and can they take the commutated load current?

The following discussion characterizes the D-S diode of a number of power MOSFETs so that the circuit designer can make the performance/cost comparisons between using these internal diodes or discrete outboard ones.

SWITCHING CHARACTERISTICS

The important switching characteristics of clamp diodes in switchmode applications are reverse recovery time, t_{rr}, and turn-on time, t_{on}. Diodes with long t_{rr} times can cause excessive turn-on stress on the FET they should be protecting as both the diode and the FET will be conducting during this time interval. The result will be a feed through drain current spike which could exceed the forward bias SOA of the FET. If the diode has relatively slow t_{on} times or high overshoot voltage — modulation voltage $V_{FM(DYN)}$ — then, in a similar manner, the FET might not adequately be protected during inductive turn-off.

In the past, most semiconductor manufacturers would characterize and specify (if they did it at all) the internal diodes for switching, using the JEDEC suggested circuits of Figure 11-13a and 11-13b. There are several problems associated with these circuits; for one, they were originally developed for sine-wave rectifier applications. As such, the t_{rr} test circuit would produce a half sine-wave of controllable current amplitude, I_{FM}, and di/dt of the current fall time. However, since the current waveform was derived from a capacitor dump, tuned circuit, the resulting

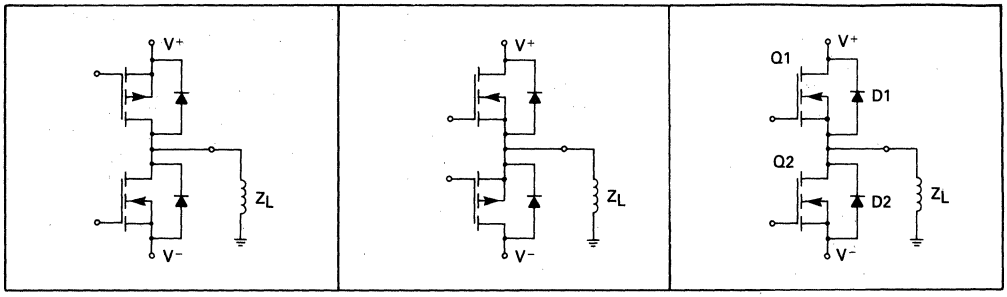


FIGURE 11-12a — COMMON SOURCE

FIGURE 11-12b — COMMON DRAIN D-S

FIGURE 11-12c — TOTEM-POLE

Complementary Push-Pull

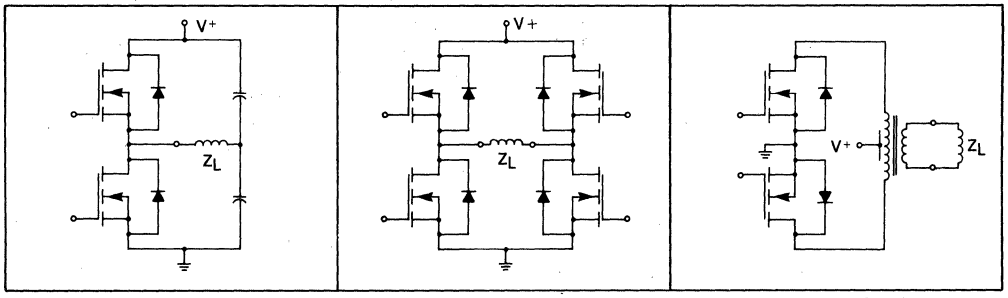


FIGURE 11-12d — 1/2 BRIDGE

FIGURE 11-12e — H BRIDGE

FIGURE 11-12f — TRANSFORMER PUSH-PULL

FIGURE 11-12 — MULTIPLE POWER FET DRIVE CONFIGURATIONS USING D-S DIODES

current duration t_p was dictated by I_{FM} and di/dt. Under some high di/dt conditions, t_p can become relatively short compared to the t_{rr} of the device under test (DUT) and consequently the diode is not fully turned on, thus producing inaccurate t_{rr} measurements. To ensure adequate DUT turn-on, t_p should exceed five times t_{rr}.

Second, since t_{rr} is dependent on I_{FM} and di/dt, what should these variables be set to? I_{FM} is obvious: it should be the diverted drain current, but di/dt could be anything, be it 25 A/μs or 100 A/μs, etc. In reality, this diode current turn-off time is controlled by the complementary FET turn-on time.

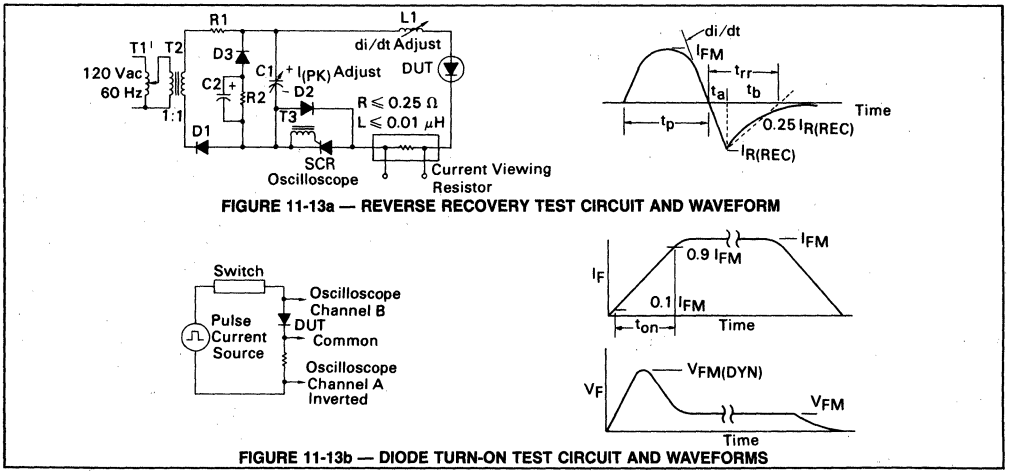


FIGURE 11-13a — REVERSE RECOVERY TEST CIRCUIT AND WAVEFORM

FIGURE 11-13b — DIODE TURN-ON TEST CIRCUIT AND WAVEFORMS

FIGURE 11-13 — JEDEC SUGGESTED DIODE SWITCHING TEST CIRCUITS

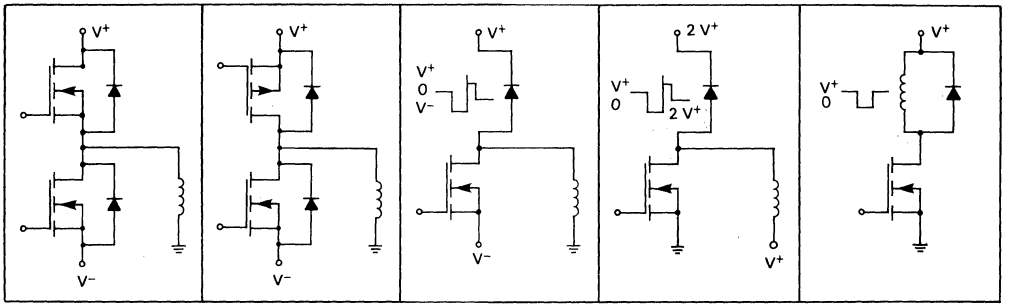


FIGURE 11-14a — TOTEM-POLE | FIGURE 11-14b — COMPLEMENTARY | FIGURE 11-14c — SIMPLIFIED CLAMP CIRCUIT | FIGURE 11-14d — LEVEL TRANSLATED | FIGURE 11-14e — TEST CIRCUIT

FIGURE 11-14 — EVOLUTION OF INDUCTIVE CLAMP TEST CIRCUIT

The problem with the t_{on} test circuit was the difficulty in defining and controlling the rise time of the current pulse applied to the DUT. Since this current pulse affects the measured $V_{FM(DYM)}$ and t_{on} of the DUT, its shape should be related to the real world conditions.

This is what the proposed test circuit does. Its configuration is derived from a typical two transistor Switchmode application, be it a totem-pole for characterizing N-channel D-S diodes or a complementary common source for characterizing P-channel D-S diodes (Figure 11-14). These configurations reduce to the simple, single-ended inductive clamp circuit (Figure 11-14e) whereby the clamp diode would be the D-S diode of either the N-channel FET (totem-pole) or the complementary P-channel FET.

The reverse recovery time is of greatest significance for continuous load currents common in switching inductive loads. Figure 11-15a describes the idealized current waveforms when a continuous inductive load current I_L is commutated between the FET (I_D) and clamp diode (I_F). Figure 11-15b shows the time expansion of both the leading and trailing edges of I_D and I_F. Note that the drain current fall time t_{fIC} controls the diode current rise time t_{fID} (or t_{on}) and in a similar manner, the dI_D/dt (or t_{rID}) of the drain current turn-on time dictates the dI_F/dt of the diode current turn-off time. Thus, the faster the FET switches, the greater is the di/dt applied to the diode. The diode di/dt then dictates the magnitude of the reverse recovery time t_{rr} and current $I_{RM(REC)}$. Since the current through the inductor is equal to I_D plus I_F the peak drain current I_{DM} at turn-on will consequently have the magnitude of I_{DM} impressed on it. This is illustrated in Figure 11-16 whereby the switching times of I_D and I_F are the mirror image of each other; the sum of the two waveforms would yield the inductor current, whose ripple magnitude is dependent on the switching frequency and load inductance.

An example of discontinuous and continuous load current waveforms are shown in Figures 11-17a and 11-17b respectively. Note that for the discontinuous case, where the inductor current I_L is allowed to completely discharge, the di/dt of I_F is extremely low, thus producing no I_{RM} or t_{rr}. For the continuous current case, the resultant di/dt produces significant I_{RM} and t_{rr}.

The size of the inductor used has little, if any, effect on the t_{rr} measurements as shown in Figures 11-18a and 11-18b; Figure 11-18a shows the full cycle and time expanded waveform of diode current for inductances of

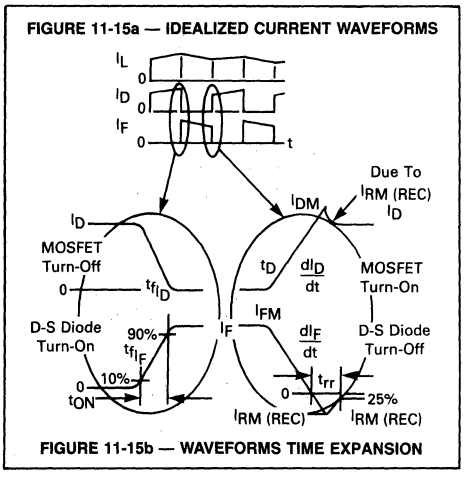


FIGURE 11-15 — CONTINUOUS LOAD CURRENT SWITCHING WAVEFORMS

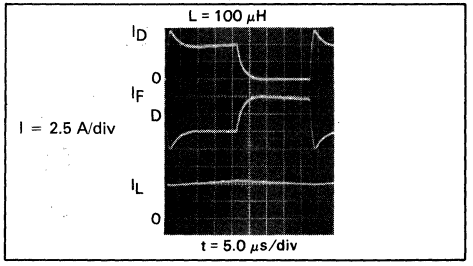


FIGURE 11-16 — SWITCHING CURRENTS OF A CLAMPED INDUCTIVE LOAD

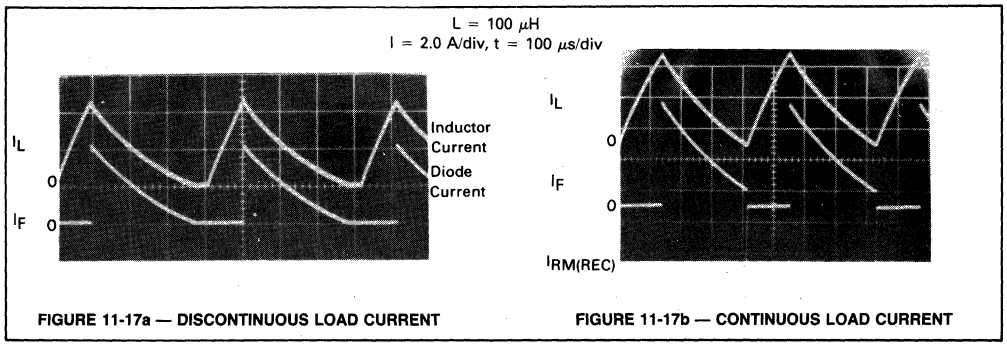


FIGURE 11-17a — DISCONTINUOUS LOAD CURRENT

FIGURE 11-17b — CONTINUOUS LOAD CURRENT

FIGURE 11-17 — THE EFFECT OF SWITCHING INDUCTIVE LOAD CURRENT ON t_{rr} AND $I_{RM(REC)}$ OF D-S DIODE

100 μH (air core) and Figure 11-18b for a 10 mH (iron core) inductor. The major difference is the magnitude of the ripple current, the larger inductor producing a more constant current source.

TEST CIRCUIT

The test circuit used for generating the diode switching characteristics, a translation of the "real world" circuit of Figure 11-14e, is shown in Figure 11-19. It consists of a CMOS, astable multivibrator (Gates G1 and G2) driving two parallel connected Gates 3 and 4 as a buffer. Potentiometer R1 varies the duty cycle of the approximately 25 kHz output which therefore sets the magnitude of the DUT current (along with V_{DD}). The positive-going output from the buffer is direct-coupled to turn on the NPN transistor Q1 and the following Baker-clamped PNP transistor Q2.

To produce an off-bias to the driver, which can shape its turn-off time and consequently the diode turn-on time, the negative going edge of the output pulse from the buffer is used. Capacitor C1 and resistor R2 form a differentiating circuit to produce the negative pulse for turning on PNP transistor Q3 and the following NPN transistor Q4. This transistor acts as the off-bias switch, applying to the driver a negative voltage pulse (approximately V^-) coincident with the trailing edge of the input pulse and lasting as long as the R2C1 time constant, about 5.0 μs for the component values shown.

SWITCHING TEST RESULTS

TMOS D-S diodes are usually tested at the rated continuous drain current. The supply voltage V_{DD} should be greater than 10 V to ensure that the DUT driver is operating with typical transconductance. Since the DUT current is a function of duty cycle and/or V_{DD}, reducing the input pulse width will allow a greater V_{DD} to be used, if so required.

Although it is not always possible to test the DUT with its real world supply voltage (i.e., high voltage devices with higher V_{DD}s than low voltage devices), the results would be more indicative if it were possible, since g_{fs} and switching speeds will vary somewhat with V_{DD}.

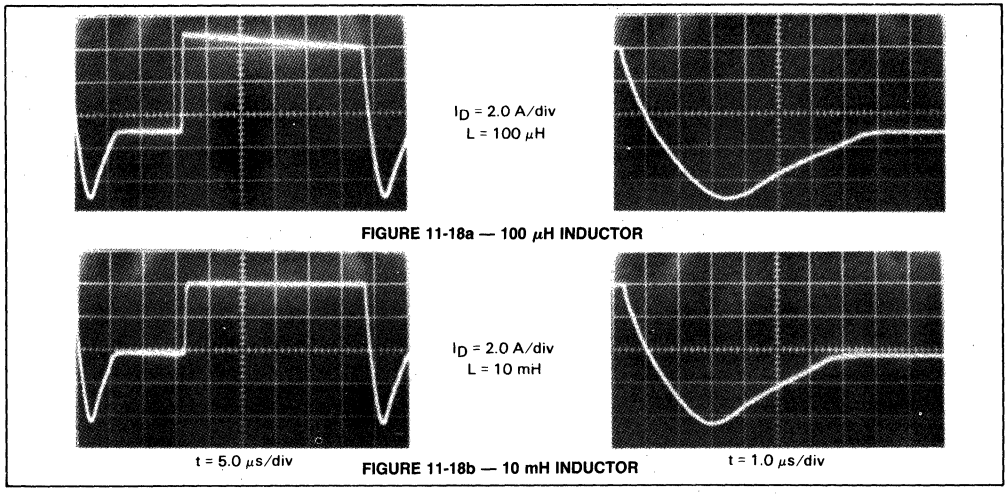
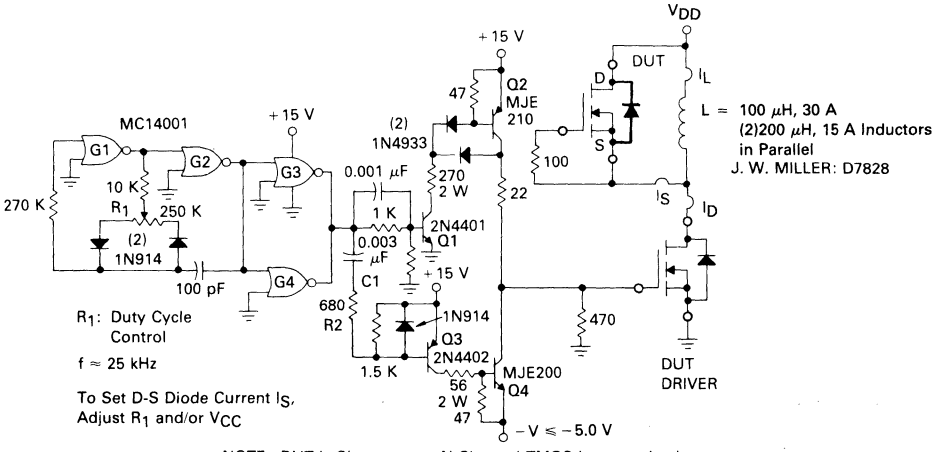


FIGURE 11-18a — 100 μH INDUCTOR

FIGURE 11-18b — 10 mH INDUCTOR

FIGURE 11-18 — THE EFFECTS OF LOAD INDUCTANCE ON D-S DIODE REVERSE RECOVERY CHARACTERISTICS



NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

FIGURE 11-19 — TMOS D-S DIODE SWITCHING TIME TESTER

Testing of several different FETs as a function of V_{DD} showed a second order variation in t_{rr} measurements. At any rate, to ensure measurement repeatability, V_{DD}, frequency, duty cycle and inductor specification should be listed. For most of the TMOS FETs tested, the inductor was either one 200 μH, 15 A rated air core or two in parallel (100 μH, 30 A). Whatever the conditions, the DUT driver and diode under test should be adequately heat sunk to minimize excessive case temperature rise.

The switching characteristics of an MTM15N15 as shown in Figure 11-20, and the complete switching results for the TMOS FETs tested are compiled in Table 1.

Also shown (Figure 11-21) for comparison, are switching photos of discrete rectifiers. Note that the fast recovery rectifier, as expected, had the lowest t_{rr} and that the standard rectifier, the largest t_{rr}. But of even more interest, the TMOS D-S diode had the lowest t_{rr} of all diodes tested (Table 1).

From this data, the circuit designer can now decide if the switching characteristics of the diode are adequate for his application.

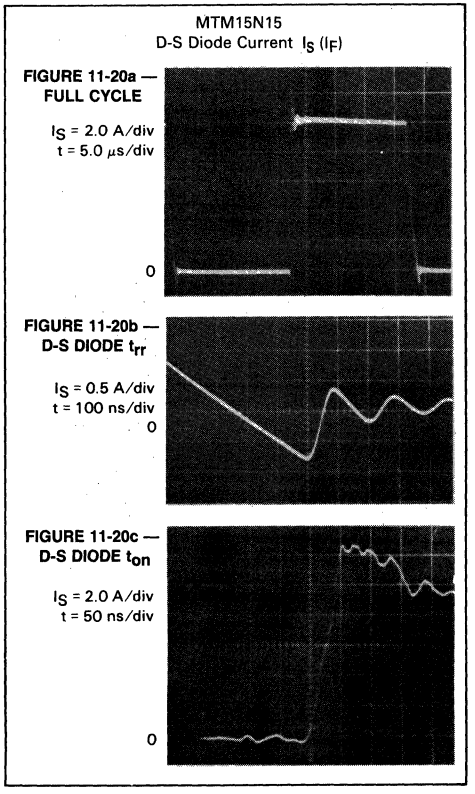


FIGURE 11-20 — SWITCHING CHARACTERISTICS OF A TMOS D-S DIODE

SURGE CHARACTERISTICS

An equally important consideration is whether the diode can handle the commutated load current in which, under continuous load current, high duty cycle conditions, the energy can be quite high.

The TMOS D-S diode is the result of the parasitic NPN transistor across the FET and as such, actually has more die area available to conduct diode current than the FET has for drain current. For data sheet purposes, the drain-source diode current, labeled I_S, is made equal to the drain current I_D.

To verify these current ratings, the D-S diodes were subjected to two different pulse width surge tests, a one

TABLE 1 — Switching and Surge Current Characteristics of TMOS D-S Diodes

Device	Type (Chan)	Spec I_D Cont (A)	Switching					Surge Current	
			I_{FM} (A)	di/dt (A/μs)	I_{RM} (A)	t_{rr} (μs)	t_{on} (μs)	300 μs 60 pps (A)	1.0 s 1 Shot (A)
MTM8N10	N	8.0	6.0	8.5	1.0	0.20	0.20	30	11
MTM15N06	N	15	10	9.0	1.0	0.24	0.29	80	24
MTM15N15	N	15	10	5.0	0.8	0.28	0.05	120	19
MTP1N60	N	1.0	1.0	10	0.3	2.0	0.03	25	6.0
MTP5N06	N	5.0	5.0	3.7	0.24	0.14	0.09	50	12
MTP25N06	N	25	25	10	1.0	0.20	1.0	140	35

second, one-shot pulse and a 300 μs, 1.8% duty cycle (60 Hz rep rate) pulse train. The one second test, which approximates a dc test, was run with the DUT bolted to a four inch square copper heat sink, initially water cooled and then in free air. The DUT forward current was then increased until the device was destroyed. The test results on one product line for the water cooled versus free air cooled were virtually identical so all subsequent tests were done in free air. The results of these tests are shown in the surge current sections of Table 1.

For power dissipation purposes and clamping efficiency determination, the typical forward characteristics of the diodes were also taken, as shown in Figure 11-22. These V_F-I_F curves were derived from a curve tracer using a 300 μs current pulse at 60 PPS; the low duty cycle ensured low case temperature readings. For comparison purposes, Figure 11-23 describes the forward characteristics of discrete diodes under the same test conditions. Knowing the voltage drop and current, the diode dissipation can be calculated. For any combination of power dissipation, the total diode and FET dissipations should not exceed the rating of the devices. After determining the switching characteristics and the power handling capability of the diodes, a cost/performance trade-off can be made. If the switcher is in the development phase, it is relatively simple to determine the effects of using the internal monolithic diode over a discrete, outboard diode, i.e. measuring case temperature rise, current and voltage waveforms, load lines to ensure safe SOA, device and system efficiency, etc.

Diode Current I_F = 0.5 A/div. t = 1.0 μS/div

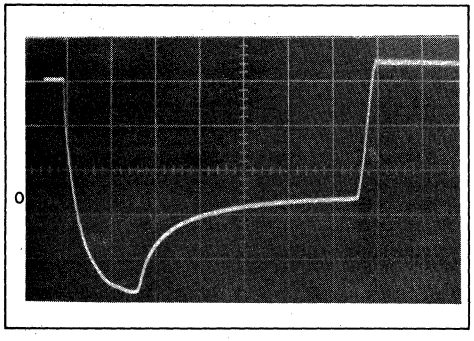


FIGURE 11-21a — 1N4001 STANDARD RECTIFIER

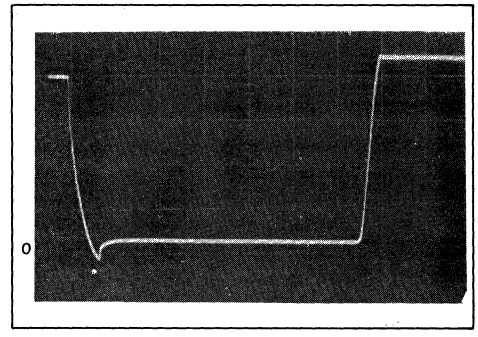


FIGURE 11-21b — 1N4935 FAST RECOVERY RECTIFIER

FIGURE 11-21 — COMPARISON OF DISCRETE RECTIFIERS FOR REVERSE RECOVERY CHARACTERISTICS

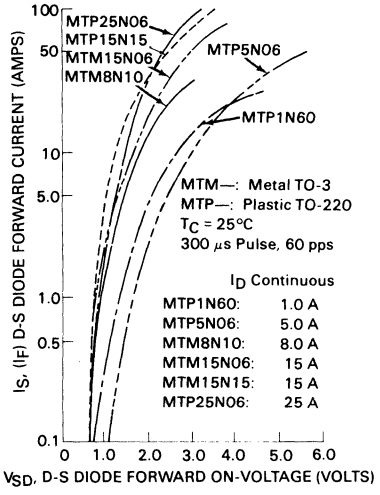


FIGURE 11-22 — FORWARD CHARACTERISTICS OF POWER MOSFETs D-S DIODES

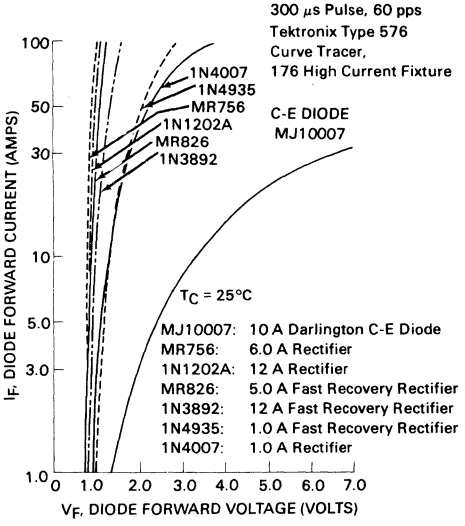


FIGURE 11-23 — FORWARD CHARACTERISTICS OF DISCRETE RECTIFIERS

Thermal Measurements

STEADY STATE THERMAL RESISTANCE MEASUREMENTS

It is a well known fact that, for reliable operation of a semiconductor, junction temperature is of great concern. All semiconductor die have a critical temperature which must not be exceeded or failure will occur. Also, semiconductor operating life can be either extended or shortened by its operating temperature.

The usual semiconductor die is enclosed in some type of package which prevents a direct temperature measurement. Due to the inaccessibility of the die, an indirect method must be used to determine the junction temperature. A common method is to use a temperature sensitive electrical parameter. The parameter used can vary, depending upon the type of semiconductor measured.

A basic block diagram for steady-state thermal resistance measurements for bipolar transistors is shown in Figure 11-24. The forward biased base-emitter-junction is used as the temperature sensitive parameter. This junction is calibrated at an elevated temperature in the forward direction, with a low calibration current (I_M), and should be in the linear region above the diode knee. Also, I_M should not contribute significantly to junction temperature nor turn-on the transistor; typical values are 2.0 to 10 mA.

The calibration procedure can be performed in a temperature chamber, with the temperature set for a normal operating temperature value for the semiconductor being measured. A typical temperature for a silicon die is around 100°C. The base-emitter forward voltage is measured and recorded at I_M and at the calibration temperature.

After calibration, a power switching fixture (Figure 11-24) is used to alternately apply and interrupt the power to the test device. The transistor is operated in the active region and power dissipation can be adjusted by varying I_E and/or V_{CE} until the junction is at the calibration temperature. This condition is known by monitoring the base-emitter voltage during the time when I_M only is flowing, with either an oscilloscope or a sample-and-hold circuit. When V_{BE} is equal to the value obtained in the calibration procedure, the junction temperature is known. The case temperature is noted at this time, as well as I_E and V_{CE}.

The heating period is long, so the temperature of the transistor case is stabilized and the interval of power interruption short, usually 300 μs, so junction cooling will be minimal.

The steady state thermal resistance can be easily calculated from the information obtained in the calibration and power dissipation procedures. The simple formula is derived from the basic thermal resistance model (Figure 11-25) showing the thermal to electrical analogy for a semiconductor.

Steady state thermal resistance, junction-to-case, is as follows:

$$R_{\theta JC} = \frac{T_J - T_C}{V_{CE} \times I_E}$$

$$\text{or } \frac{\Delta T}{P_D}$$

For junction-to-case measurements, sufficient heat sinking should be provided to prevent excessive junction temperature. Measurement accuracy is improved with a large temperature delta between the junction and case. This delta can be achieved by using an efficient heat sink permitting a power dissipation (I_E V_{CE}) of sufficient magnitude to reach the calibration temperature.

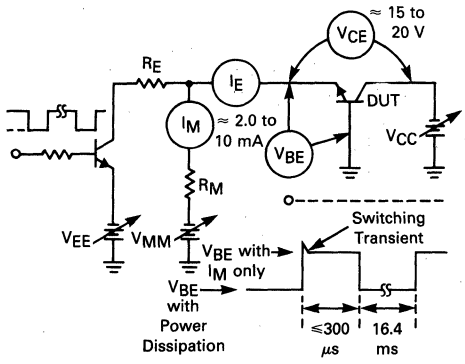


FIGURE 11-24 — BASIC BLOCK DIAGRAM OF STEADY STATE THERMAL RESISTANCE TEST CIRCUIT FOR BIPOLAR TRANSISTORS

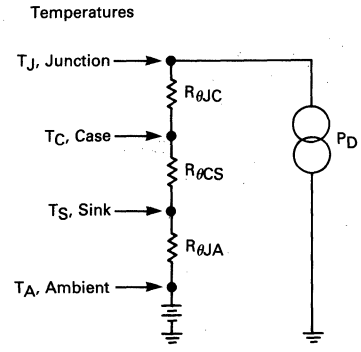


FIGURE 11-25 — BASIC THERMAL RESISTANCE MODEL SHOWING THERMAL TO ELECTRICAL ANALOGY FOR A SEMICONDUCTOR

USING TEMPERATURE SENSITIVE PARAMETERS FOR MEASURING POWER MOSFETs THERMAL RESISTANCE

In order to determine the thermal resistance of any semiconductor device, an accurate and repeatable method of measuring the device temperature is required. The linear temperature dependence of the on-voltage of a forward biased semiconductor junction has proven to be a reliable parameter and is consequently used for bipolar transistors (emitter-base or collect-base junctions), rectifiers, zeners and thyristors. Because of their intrinsic D-S diode, this technique is also applicable to TMOS power MOSFETs.

When measuring the thermal resistance of power MOSFETs, the gate-source threshold voltage or the drain-source on-resistance $r_{DS(on)}$ can be used in addition to the on-voltages of the drain-source diode. Knowing the temperature characteristics of these parameters — by measuring the voltage or resistance variations with temperature in an oven, as an example — the device temperature, when powered, can be determined and the thermal resistance can be calculated.

These temperature sensitive parameters (TSP) of a power MOSFET with their approximate temperature coefficients are listed as follows:

Drain-Source Diode ≈ −2.0 mV/°C

Gate-Source Threshold Voltage ≈ −2.0 to −6.0 mV/°C

Drain-Source On-Resistance ≈ +7.0 mΩ/°C when $r_{DS(on)}$ = 1.0 Ω

How these TSP can be measured is described in the simplified schematics of Figure 11-26, with Figure 11-26a using the D-S diode, Figure 11-26b, the $V_{GS(th)}$ and Figure 11-26c, the $r_{DS(on)}$.

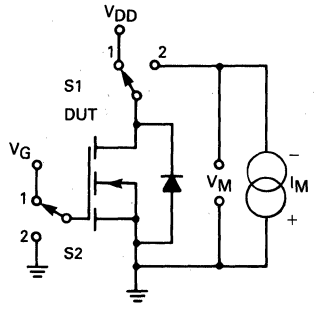


FIGURE 11-26a — DRAIN-SOURCE DIODE VOLTAGE

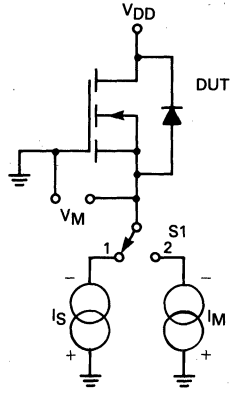


FIGURE 11-26b — GATE-SOURCE THRESHOLD VOLTAGE

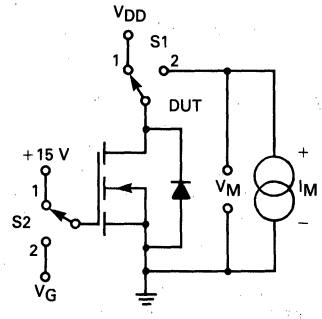


FIGURE 11-26c — DRAIN-SOURCE ON RESISTANCE

FIGURE 11-26 — CIRCUIT CONFIGURATIONS FOR MEASURING TSP

D-S Diode TSP

Generally, the most often used circuit for measuring $R_{\theta JC}$ of power MOSFETs uses the D-S diode. When electronic switches S1 and S2 are in position 1, the FET is biased on and the heating power ($V_{DS}I_D$) is applied to the FET for a relatively long period. Then the switches are thrown to position 2 for a short period of time (sense time) so that the FET temperature will not change appreciably. Next, the FET is turned off and a constant current I_M (the same sense current at which the TSP was temperature calibrated) is applied to the forward biased D-S diode. By measuring the forward voltage drop of the diode and comparing it to the calibration curve, the FET junction temperature can be ascertained. Knowing the input power and the junction temperature, the thermal resistance can be calculated. In practice, the input power, either voltage or current, is varied until the D-S diode drop is equal to a calibration point, thus simplifying the test procedure by not having to generate a complete calibration curve.

Gate-Source Threshold Voltage TSP

This thermal resistance test circuit is extremely useful for measuring $R_{\theta JC}$ of GEMFETs since this device has no parasitic diode. As in the D-S diode tester, heating power is applied to the DUT when switch S1 is in position 1. Then, switch S1 is briefly thrown to position 2, applying the sense current to the FET (I_D at $V_{GS(th)}$) and the gate-source threshold voltage is measured. Input power (V_{DS}-I_S) is varied to make $V_{GS(th)}$ equal to the elevated temperature, calibration reading resulting in a known junction temperature and thus $R_{\theta JC}$.

Drain-Source On-Resistance

This circuit is conceptually similar to the D-S diode tester. However, now when the switch is in position 2 (Sense Time), a positive constant current I_M and +15 V gate bias are applied to the device, turning it on. I_M should be of a value to produce about 0.5 V V_{DS}. The voltage V_{DS} measured (V_M) is related to $r_{DS(on)}$ by:

$$r_{DS(on)} = V_M/I_M$$

Thermal Test Fixtures

D-S DIODE THERMAL FIXTURE

$R_{\theta JC}$

The D-S diode Thermal Fixture, shown in Figure 11-27, is partially an implementation of the simplified circuit of Figure 11-26. It also contains circuitry for measuring transient thermal resistance r(t) and the analogue circuits for reading out the drain-source diode forward voltage and input power (V_{DS} and I_D). Thermal resistance is measured when the Mode Selector Switch S1 is in position 1, $R_{\theta JC}$. System timing is line synchronized and is derived from the Schmitt trigger (gates G1A and G1B) shaping circuit clocking the 300 μs Sense Time Monostable Multivibrator (gates G2A and G2B). Thus, the power MOSFET DUT is turned on via the Drain Switch circuit (cascade transistor Q1 and Q2) and unclamped gate transistor Q3 for 8.0 ms (full-wave rectified line rate minus 300 μs) and off for the 300 μs sense time. Drain current is set and readily controlled by I_D Control potentiometer R1 in the gate-source, closed loop, regulator circuit (op-amp U5).

During the sense interval, DUT power is turned off (Q2 is off, Q3 is on) and the sense current I_S is applied to the now forward biased D-S diode by means of turned on transistors Q4 and Q5. The resultant D-S diode voltage can be observed by a scope or measured by the Sample and Hold circuit consisting of series FET switch Q6, buffer amp U6, sample driver Q7 and line synchronized, Delay Monostable MV gates G2C and G2D. The Delay Control of this MV allows the sample pulse to be positioned some time after the start of the Sense time so as to measure the settled voltage of the D-S diode, ignoring the possible thermal and/or electrical switching transients on the leading edge of the sense pulse. This delay time is typically 50 μs to 150 μs.

Using similar sample-and-hold circuitry, the applied power ($V_{DS/10}$ and $I_{D/10}$) can be measured. This is accomplished by the respective FETs Q8 and Q9, sample driver Q10, buffer U3A and U3B and difference connected op-amps U4A and U4B.

Transient Thermal Resistance r(t)

Transient thermal resistance, r(t), is measured when switch S1 is in position 2. Now the system timing is derived by the 22 second astable MV (gates G1C and G1D) which turns the DUT on and off for about 11 seconds each. During the off time, cooling cycle, the voltage of the D-S diode can be measured at any selected period of time. This is accomplished by selecting the various resistor-capacitor timing components of the Delay MV, thus positioning the sample pulse accordingly. The six switchable capacitors, by means of Selector Switch S2, will produce the six time decades of control (100 μs to 10 s) and the three resistors (switch S3), the multipliers within the decade, e.g., 0.2, 0.5 and 1.0.

GATE THRESHOLD VOLTAGE $V_{GS(th)}$ THERMAL FIXTURE

The Gate-Source Threshold Voltage ($V_{GS(th)}$) Thermal Fixture, Figure 11-28, was specifically designed for measuring the thermal resistance of GEMFETs as this device does not have a D-S diode. Since it detects temperature induced variations in the gate-source threshold voltage, it can also be used for power MOSFETs. Its line synchronization and current regulator loop around the gate and source make it very similar to D-S Diode Thermal Fixture. The major difference is the setting of the two different drain currents (or source currents), the power current, I_S, and sense current I_M. This is accomplished by switching two different reference voltages to the positive input of the loop regulator op-amp U3. As in any regulator loop of this type, the voltage at the negative input of the op-amp, as derived from the voltage drop across the source sense resistor R1, will be driven by the closed loop to a value equal to the reference input. Thus, if a heating current, I_S, of say 10 A is required, the reference voltage should be 3.0 V (10 A x 0.3 Ω). If a sense current I_M of 10 mA is specified, V_{REF} should be 3.0 mV.

Although most power MOSFETs are specified for a 1.0

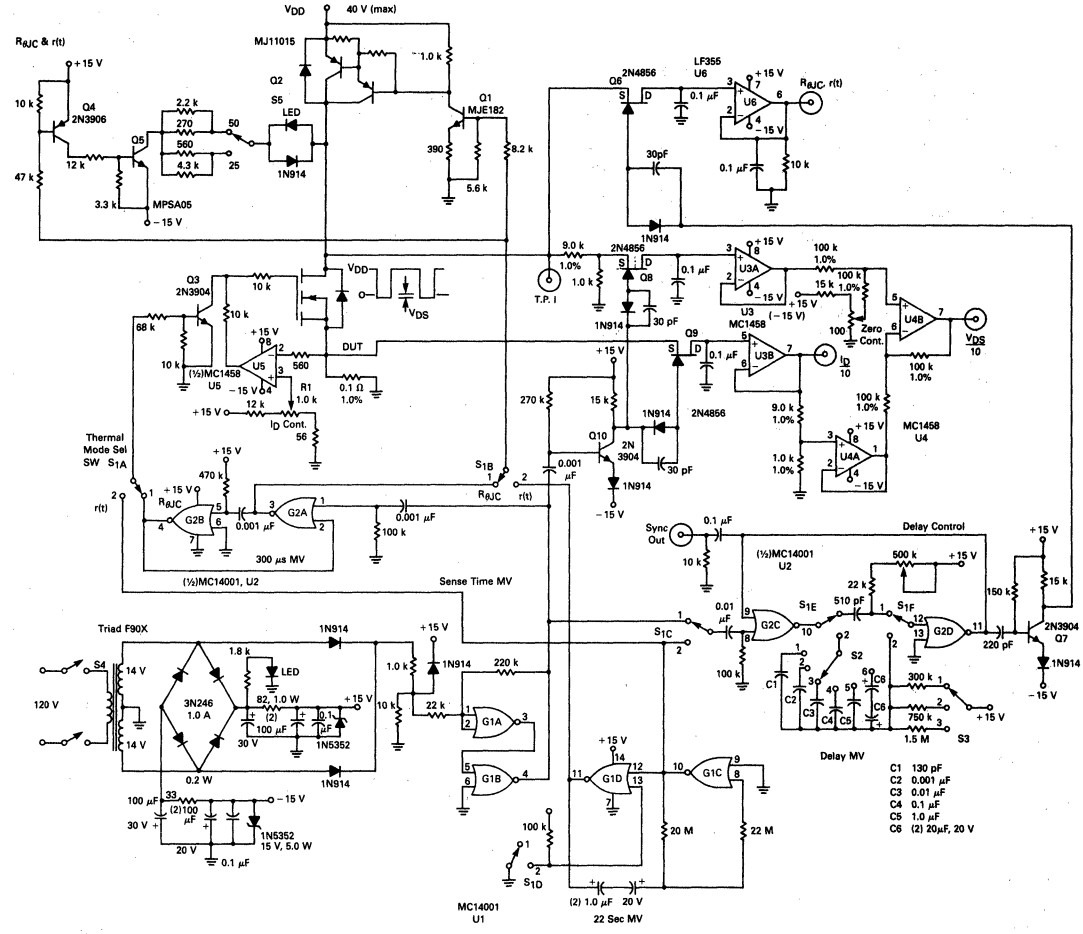


FIGURE 11-27 — POWER MOSFET THERMAL FIXTURE

mA drain current at $V_{GS(th)}$, the 10 mA level was chosen for measurement simplicity; in reality, there is negligible difference in the test results at either currents.

As in the D-S Diode Fixture, the system timing is line synchronized by Schmitt Trigger U1A and U1B, whose complementary outputs are used to clock the 370 μs sense MV (U1C and U1D), and the variable delay MV (U1E and U1F) for the sample pulse. This type of line synchronization offers several advantages: at high power heating drain currents, it simplifies the oscilloscope viewing, particularly when the external power supplies are not well regulated, and it is easily derived from one hex gate CMOS IC MC14572.

During the 370 μs sense time, the output of U1D is high; thus, PNP Darlington, Q1 is Off and the reference voltage is determined solely by the voltage divider R2 (the 10 mA Set Control), R4 and R5. To set R2, switch S2 is opened and the drain current is monitored for the required 10 mA.

When U1D goes low for the approximate 8.0 ms power cycle, Q1 is turned on, placing R3, the I_S control, into the reference voltage circuit. Consequently, the reference voltage will be switched from the 3.0 mV sense voltage to the I_S control voltage.

During the sense time the magnitude of the gate-source voltage, can be monitored with a scope or read out with the sample-and-hold circuit consisting of FET series switch Q3, buffer amps U2A and U2B, sample driver Q2 and delay MV U1E and U1F. Power to the DUT is then varied, either V_{DS} or I_D, to make $V_{GS(th)}$ equal to the calibrated value; thus, T_J and P_{IN} are known and $R_{\theta JC}$ can be calculated ($R_{\theta JC} = \frac{(T_J - T_C)}{P_{IN}}$).

POWER MOSFET MEASUREMENT TECHNIQUES FOR THE CURVE TRACER

The curve tracer is an extremely useful tool in measuring the pertinent power MOSFET parameters. The

techniques are not dissimilar to those used for measuring bipolar transistors. Table 2 lists the equivalent parameters between the two.

No FET parameters are measured in an open gate condition. To prevent damage to the part, the gate should always be terminated with a resistor (typically R_{GS} = 1.0 MΩ) or a short for the appropriate test condition.

DEFINITIONS OF ELECTRICAL CHARACTERISTICS

Off Characteristics

$V_{(BR)DSS}$, Drain-Source Breakdown Voltage — Maximum sustaining voltage between the drain and source, measured at a specific drain current, I_D; Gate shorted to the source.

I_{DSS}, Drain-Current With Zero Gate Voltage — Drain leakage current at a specified drain-source voltage, V_{DSS}; Gate shorted to source.

I_{GSS}, Gate Body Leakage Current — Gate leakage current for a specified gate-source voltage; Drain shorted to source.

On Characteristics

$V_{GS(th)}$, Gate Threshold Voltage — Value of the gate voltage that must be applied to initiate conduction. It has

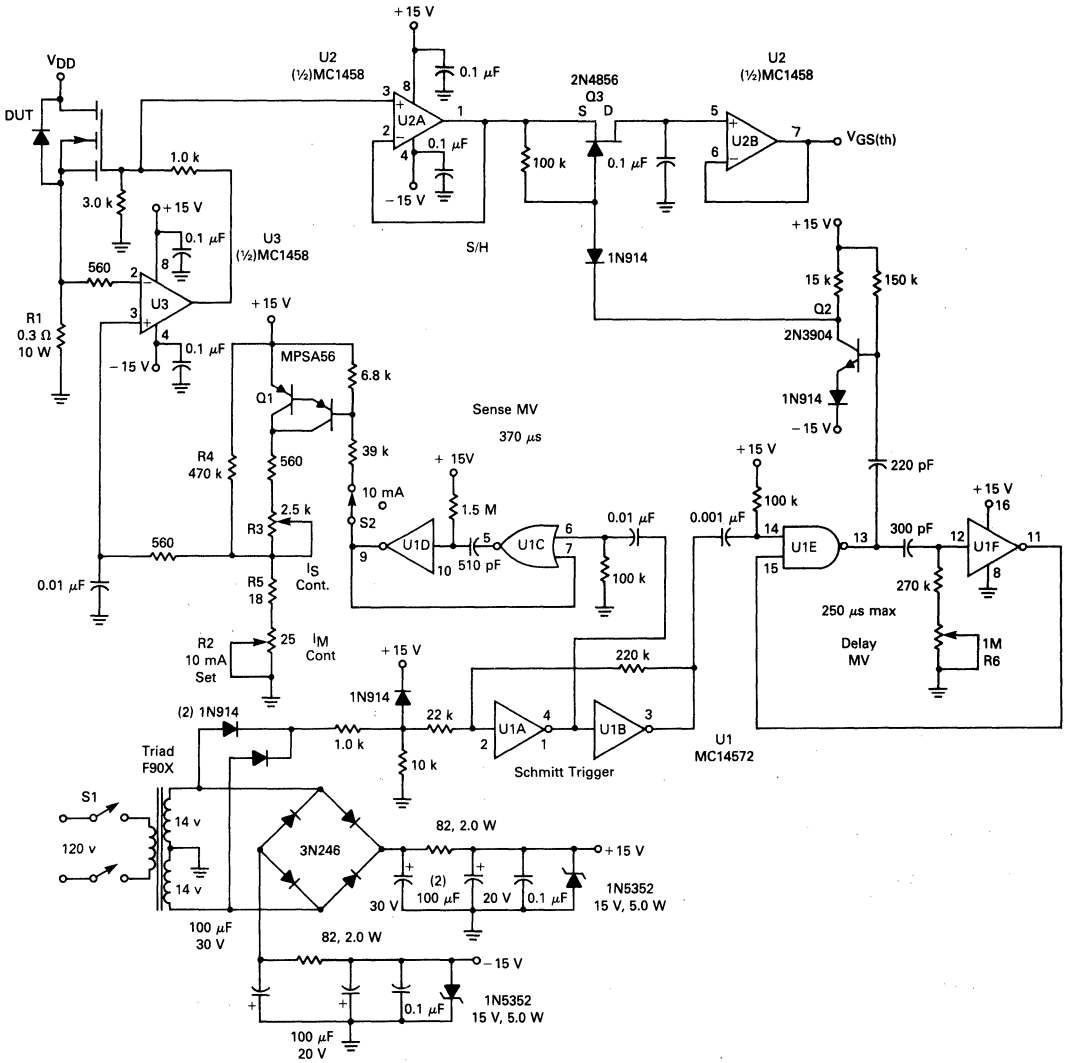


FIGURE 11-28 — POWER MOSFET $V_{GS(th)}$ THERMAL FIXTURE

TABLE 2

Transistor	MOSFET
Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGR}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{FE}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$
V_{EC}	V_{SD}

a negative temperature coefficient of about −6.7 mV/°C.

$V_{DS(on)}$, Drain-Source On-Voltage — Voltage drop measured between the drain and source at a specified drain current and specified gate-source voltage.

$r_{DS(on)}$, Drain-Source On-Resistance — Value of the resistance measured between drain and source at a specified drain current and a specified gate-source voltage. It is defined as:

$$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$$

g_{fs}, Forward Transconductance — The MOSFET gain parameter. It is the ratio between the change in drain current, I_D, for a given change in gate-source voltage, at a specified drain-source voltage and specified drain current. In algebraic form:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

V_{SD}, Diode Forward On-Voltage — The forward voltage drop between the source and drain at a specified S-D diode current I_S.

Curve Tracer Measurements

The following explains how to measure the parameters listed above on a curve tracer. Although the set-up charts correspond to the Tektronic Type 576 Curve Tracer, the same measurements can be performed on a Tektronix Type 577 Curve Tracer.

Before applying power to MOSFETs on a curve tracer, the following precautions should be observed:

1 — Test stations should be protected from Electro-Static Discharge.

2 — When inserting parts into a curve tracer, voltage should not be applied until all terminals are solidly connected in the socket.

3 — A resistor of 100 Ω should be connected in series with the gate to damp spurious oscillations that can occur on the tracer.

4 — When switching from one test range to another, voltage settings should be reduced to zero to avoid generation of potentially destructive voltage surges during switching.

The test set-ups to follow are for the Motorola MTP12N10 Power MOSFET, which is a 12 Amp, 100 volt N-Channel device in the TO-220 package.

$V_{(BR)DSS}$ — Also known as BV_{DSS}. Specified at an I_D of 5.0 mA at T_C = 25°C.

Test set-up and Source Trace (See Figure 11-29).

1 — Set maximum peak volts on 350, Series Resistors on 3.0 k.

2 — Polarity to NPN, Mode to Norm.

3 — Vertical on 1.0 mA/Division, Display Offset on 0, Horizontal on 20 volts/Division.

4 — Step Generator is not used for this measurement.

5 — Emitter grounded; Base Term on short.

6 — With device in socket, adjust variable collector supply until trace breaks and reaches 5.0 mA.

I_{DSS} — Specified at 85% of rated $V_{(BR)DSS}$. Maximum allowable leakage is 250 μA at T_C = 25°C.

Test Set-Up

Set-up is the same as $V_{(BR)DSS}$/except:

1 — Set Mode Switch to Leakage.

2 — Set Vertical to 50 μA/Division

3 — Adjust variable collector supply to 85 volts and read leakage. If Leakage reads 0, adjust Vertical to desired level (This increases sensitivity on low leakage devices).

I_{GSS} — Specified at V_{GS} = ±20 volts, maximum allowable leakage is 500 nA at T_C − 25°C.

Test Set-Up

1 — Drain and gate connections on socket are reversed so drain is shorted to source.

2 — Set maximum peak volts to 75, and Series Resistors to 140 Ω.

3 — Polarity to NPN and Mode Switch to Leakage.

4 — Vertical on 50 nA/Division, Display Offset on 0, Horizontal on 2.0 Volts/Division.

5 — Step generator is not used for this measurement.

6 — Emitter grounded; Base Term on short.

7 — With device in socket, adjust variable collector supply to 20 volts and read Leakage. If leakage reads 0, adjust vertical to desired level.

$V_{GS(th)}$ — Specified at 1.0 mA with limits of 2.0 volts minimum and 4.5 volts maximum at T_C = 25°C.

(Figure 11-30)

1 — Set Maximum Peak Volts to 15, Series Resistors to 0.3 Ω.

2 — Polarity to NPN, Mode Switch on Normal.

3 — Vertical on 0.2 mA/Division, Display Offset on 0, Horizontal on 2.0 Volts/Division.

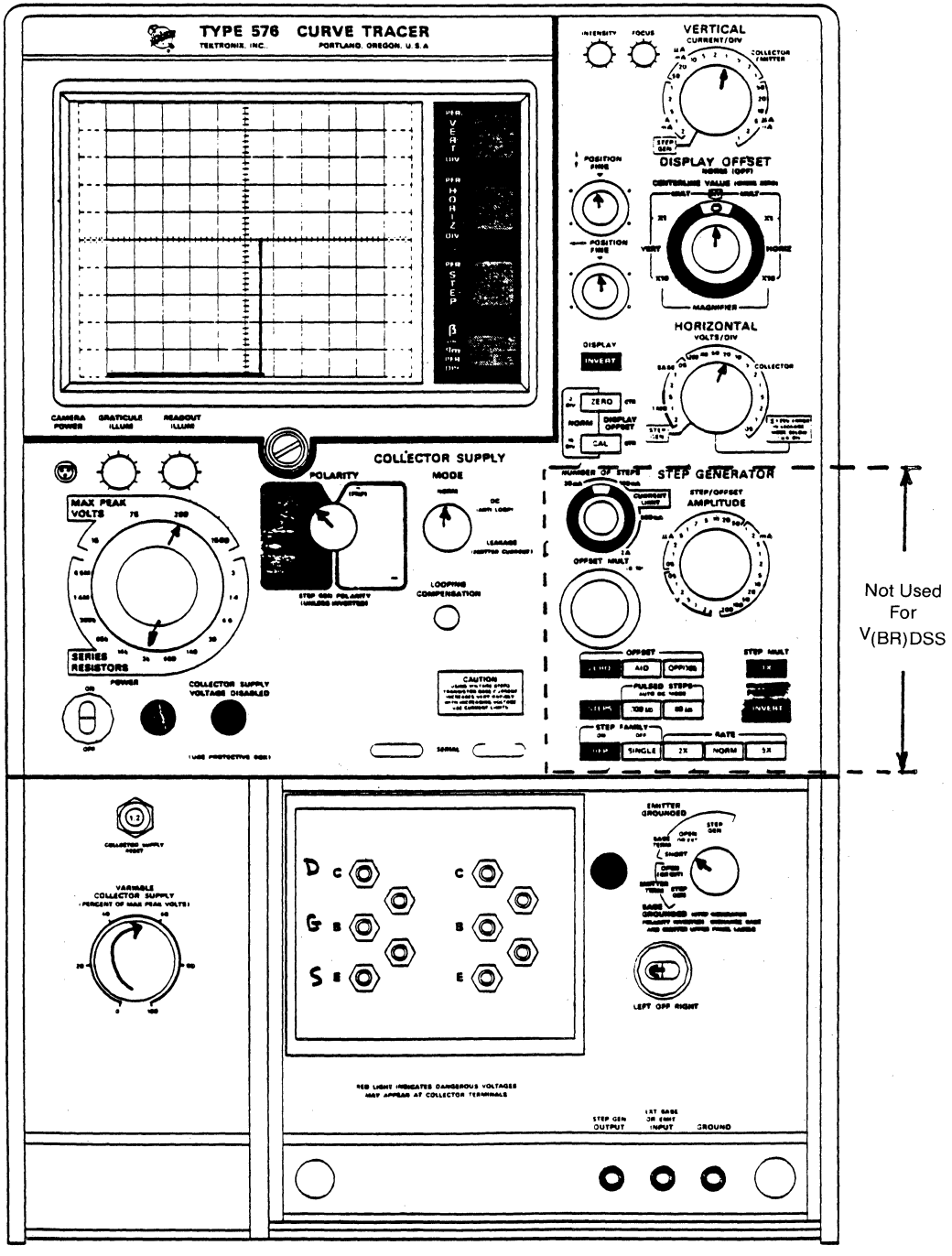


FIGURE 11-29 — TEST SET-UP CHART TYPE 576 FOR MEASURING POWER MOSFET PARAMETERS

4 — Step Generator; number of steps = 1, Offset Mult on 0, Offset on Aid, Steps Button in, Step Family on Single, Rate on Norm, Step offset amplitude = 1.0 V.

5 — Emitter grounded; Base Term on Step Generator.

6 — With device in socket, adjust variable collector supply to 10 volts, then adjust Offset Mult until trace reaches 1.0 mA. Read $V_{GS(th)}$ directly from Offset Mult Control.

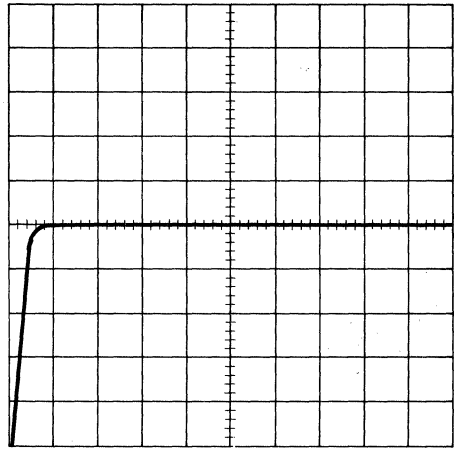


FIGURE 11-30 — CURVE TRACER PRESENTATION FOR $V_{GS(th)}$ — MTP12N10

$V_{DS(on)}$ — Specified at V_{GS} = 10 volts and at one half rated I_D. $r_{DS(on)}$ is calculated from measured $V_{DS(on)}$ value.

(Figure 11-31)

1 — Set Maximum Peak Volts on 15, Series Resistors on 0.3 Ω.

2 — Polarity on NPN, Mode to Norm.

3 — Vertical on 1.0 A/Division, Display Offset on 0, Horizontal on 0.5 Volts/Division.

4 — Step Generator; number of steps — 10, Offset on zero, pulsed steps on 300 μs, Step Family on Rep, rate on Norm, Step Offset/Amplitude = 1.0 V.

5 — Emitter grounded; Base Term on Step Gen.

6 — With device in socket, adjust variable collector supply until the top left dot on trace reaches 6.0 Amps then read $V_{DS(on)}$ off horizontal scale.

g_{fs} — Specified at one half rated I_D at V_{DS} = 15 volts.

(Figure 11-32)

1 — Maximum Peak Volts on 15, Series Resistors on 0.3 Ω.

2 — Polarity on NPN, Mode to Norm.

3 — Vertical on 1.0 Amp/Division/Display Offset on zero, Horizontal on 2.0 Volts/Division.

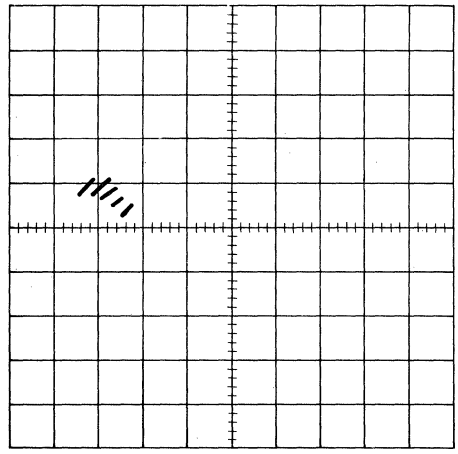


FIGURE 11-31 — CURVE TRACER PRESENTATION FOR $V_{DS(on)}$

4 — Step Generator; number of steps = 10, Offset on zero, Pulsed Steps on 300 μs, Step Family on Rep, rate on Norm, Step Offset Amplitude −1.0 V.

5 — Emitter grounded; Base Term on Step Gen.

6 — Readout illum turned fully clockwise.

7 — With device in socket, adjust variable collector supply until trace with steps closest to 6.0 Amps reaches 15 volts. g_{fs} is the number of divisions between those two steps, as designated by the right hand corner of the screen labeled g_m per Division.

V_{SD} — Specified at rated I_D with V_{GS} = 0.

(Figure 11-33)

1 — Set Maximum Peak Volts on 15 and Series Resistors on 0.3 Ω.

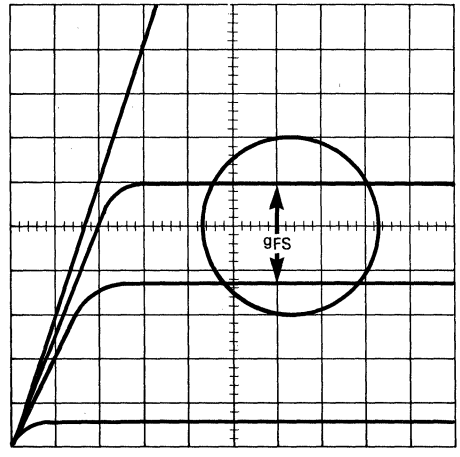


FIGURE 11-32 — CURVE TRACER FOR g_{fs}

2 — Polarity on PNP, Mode on Norm.

3 — Vertical on 2.0 Amps/Division, Display Offset on 0, Horizontal on 0.5 Volts/Division.

4 — Push Display Invert in.

5 — Step Generator is not used for this measurement.

6 — With device in socket, adjust variable collector supply until trace reaches 12 Amps and read voltage.

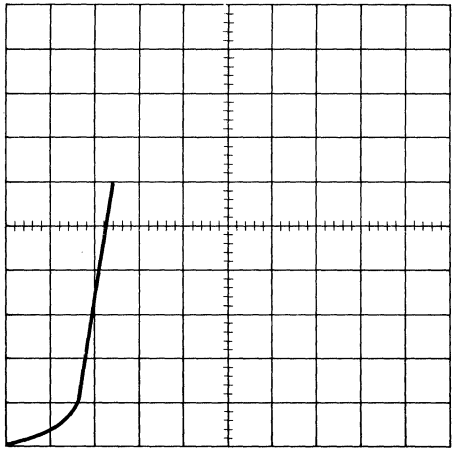


FIGURE 11-33 — CURVE TRACER PRESENTATION FOR V_{SD}

Additional Reference Material: Measurement Concepts From Tektronix.

Characterizing Power MOSFETs For Unspecified Parameters

Although many modern data sheets characterize power MOSFETs specifically for operation in power conversion equipment, it is not practical to guarantee operation for every conceivable set of operating conditions. Therefore, equipment design frequently requires the use of power MOSFETs in conditions for which they are not specified. To compensate for the unknowns, use of a relatively large design sample is common practice. A relatively large sample gives a feeling of statistical security. All too often, the sample comes from transistors purchased in a single group, with predictably unfortunate results. A common scenario goes something like this.

DESIGN SCENARIO

The designer orders as many as 100 of each of the key components to try in this equipment. He may simply verify that the equipment performs satisfactorily, or he may attempt to do a worst case analysis based upon parametric variations. Either way, it is believed that the 100 pieces constitute a statistically conservative sample.

With performance and worst case analysis indicating satisfactory performance, the design is finalized. Preproduction begins with components from the initial 100 piece order. Except for routine debugging, all goes well. Hard tooling is committed. Initially, or months, or even years later, the equipment begins to fail as it comes off the production line. Perhaps with less fortune, the equipment fails in the field. The reason, which is at first elusive, boils down to the equipment requiring a combination of non-reproducible characteristics in one or more of the key components.

All too many people have been adversely affected by just this kind of scenario. Yet, minimizing the risks associated with component selection is considerably easier than might be expected. Guidelines for minimizing the risks, with respect to power MOSFETs, are presented here. In addition to general guidelines, a straightforward method for determining safe operating safety margin is highlighted. The discussion begins with statistical concepts.

Semiconductor components have three statistical populations which are relevant to the equipment designer. They are:

1) Wafer lot
2) Wafer
3) Individual component

A wafer lot is a group of wafers which are processed together. A typical example for switching power supply output transistors is fifty wafers per lot and 100 transistors per wafer, for a total of roughly 5,000 transistors per wafer lot. The statistical considerations arise from the way semiconductors are batch processed in wafer lots. The cookie analogy is a helpful illustration.

Suppose a baker has three groups of raw cookies. Each group is sufficiently large to fully use available space in the baking oven. The three groups are therefore baked sequentially. The first group is slightly overdone and relatively dark. The second group comes out slightly underdone and very light. The third group turns out medium.

Lightness or darkness of the individual cookies will vary somewhat within each group, but probably not by very much. Variations in color are much more dependent upon which group a cookie was baked in than which individual cookie was chosen from a given group. A sample of cookies chosen from any one group will poorly predict the variations expected from the baking process.

Semiconductor characteristics vary in much the same way. Many characteristics are far more dependent upon the wafer lot in which a device is processed than upon which individual device is chosen from a given wafer lot. An illustration is shown in Figure 11-34.

Population densities for transistors in two different wafer lots, curves A and A′, are plotted on the same scale as the wafer lot distribution for the same parameter. It is clear that a sample selected from wafer lot A will poorly predict the performance expected from transistors in lot A′. These curves are typical of the way many transistor parameters vary. They are also descriptive of batch processed components in general.

From an equipment design point of view, these characteristics have serious implications. The validity of a 100 piece design sample becomes questionable, when the possibility that all 100 devices may be from the same wafer lot is considered. In fact, the validity of using 100 devices,

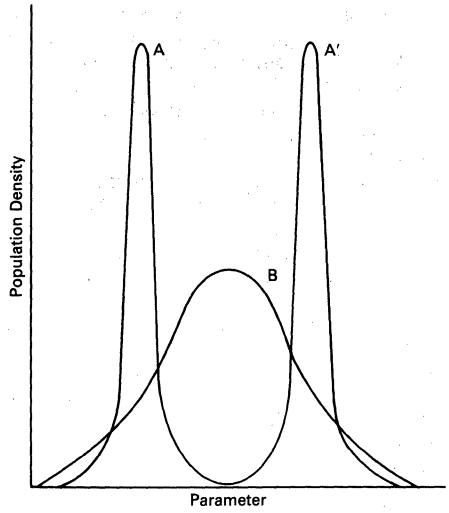


FIGURE 11-34 — EXAMPLE PROBABILITY DISTRIBUTIONS

which are purchased all in one group, is more than questionable. For those parameters which are highly wafer lot dependent, such a sample is, in effect, not a 100 piece sample, but a one piece sample, since there is a very high probability that only one wafer lot is represented.

The unfortunate circumstances in the opening scenario are a direct result of a one piece wafer lot sample. The one piece sample does not buy much statistical insurance. Surprises are likely, since a false sense of security is generated when it is believed that 100 physical units in a design sample represent a 100 piece statistical sample. The results are predictable and unpleasant for all concerned.

DESIGN SAMPLES

A key factor in top notch design work is obtaining statistically relevant samples of key components. With respect to power transistors, this means including a number of different wafer lots in the design sample. This task can be seemingly difficult since, in general, the number of wafer lots in a given sample is not known. However, the minimum number of wafer lots in a sample can be determined by assuming that each date code consists of separate wafer lots. There may be many wafer lots in a date code, but usually two date codes will not contain transistors from the same wafer lot.

Often, transistors have two date codes, one which corresponds to the time period in which they are tested and the other which denotes the time period in which they were assembled. The assembly date code is by far the more valuable of the two. As an example, Motorola TO-204 transistors have a three-digit assembly date code stamped on the ear. The first digit is coded to the year. The second and third digits correspond to workweek. A transistor built in the last workweek of 1982 would read 252.

Sample selection, then, hinges on being able to obtain transistors from a number of different date codes. Here are some suggestions.

1) Place several small orders sequentially in time.
2) Order from several different distributors, preferably in more than one geographic location. Five 20 piece shipments from five different distributors will cost more than a single shipment of 100 pieces, but the benefits dwarf the added expense.
3) Ask the manufacturer for assistance.

As a practical matter, it will generally be rather difficult to obtain a sample with more than four or five wafer lots represented. Since this is a relatively small sample, a working knowledge of parameter variations is very helpful. This is particularly true of Safe Operating Area (SOA) which is presented here as a special case.

Safe Operating Area

Safe Operating Area is probably the most troublesome of the unspecified parameters. Operation in unspecified regions is difficult to avoid since it is not practical to guarantee the transistor for all conditions in which it can be used. Usually, unspecified operation is related to the fact that SOA curves are drawn for given circuit configurations and bias conditions. Operation in conditions other than specified is not necessarily guaranteed. Therefore, it is often easy to operate fully within the boundaries of an SOA curve, yet be in an unspecified region because of differences in circuit configuration or bias.

At times like this, a straightforward test can be very effective. The steps are as follows:

1. Starting with the equipment in which the transistor will operate, or a suitable test circuit, raise the input bus voltage to 1.25 × its worst case value. Test the equipment for survivability. If any transistors in the design sample fail, there is not enough safety margin. Future trouble is almost guaranteed. If none fail, proceed to Step 2.
2. Raise the bus voltage to 1.33 × its worst case value. Repeat the testing. If more than 50% of the sample transistors survive, then SOA safety margin is probably more than adequate.
3. Recognize that worst case SOA stress, in switching power conversion systems, will often occur at conditions other than full load and high temperature. It is important to either choose conditions which maximize transistor stress, or cycle the equipment through its mini-max load and temperature ranges. Successful results will depend largely on attention to test conditions. An example is noteworthy.

   SOA stress is often maximized in the first or last switching cycle, when the equipment is turned-on or turned-off. Load lines for the first or last cycle often have larger excursions than steady state full load operation. A single excursion to a high voltage is usually more hazardous than operating at a lower voltage on a continuous basis.

These steps are very effective at eliminating unwanted surprises, provided transistors from at least three wafer lots are included in the test. They form the same basic

procedure that is used to generate data sheet SOA curves.

General Guidelines

It is often of interest to obtain reasonable limits for parameters other than SOA. A discussion of expected variations is a good place to start.

Variations within a given sample are obvious. Of interest here is the expected worst case variations over the life of a multi-year production run. Table 2 gives an indication of what can generally be expected for various parameters. Measured mean values come from data taken on transistors in the design sample. They are normalized to 1.0 for ease of comparison. It is important to note that Table 2 applies only if at least three wafer lots are included in the sample data.

Although some of the resulting tolerances may seem rather large, they are realistic when production runs spanning a number of years are considered. It is far better to face these numbers up front, than be surprised downstream with equipment failures.

TABLE 2

Parameter	Measured Mean Value	Expected Min	Expected Max
Leakage Currents	1.0	10^{-3}	10^{+3}
Breakdown Voltages	1.0	0.7	1.5
Gain	1.0	0.5	4.0
Turn-On Delay Time	1.0	0.7	1.5
Rise Time	1.0	0.5	2.0
Turn-Off Delay Time	1.0	0.5	2.0
Fall Time	1.0	0.5	2.0
Crossover Time	1.0	0.5	2.0
Gate Threshold Voltage	1.0	0.6	1.5
$r_{DS(on)}$	1.0	0.5	2.0
$V_{DS(on)}$	1.0	0.5	2.0
C_{iss}	1.0	0.7	1.5
C_{oss}	1.0	0.5	2.0
C_{rss}	1.0	0.6	1.6

Conclusion

The risk of equipment failure can be significantly reduced by straightforward improvements in the selection of design samples. Risks are further minimized with realistic estimation of worst case parameter variations, and the proper choice of test conditions for maximum stress.

Chapter 12: Reliability and Quality

Introduction

Quality and reliability are two essential elements in order for a semiconductor company to be successful in the marketplace today. Quality and reliability are interrelated because reliability is quality extended over the expected life of the product.

Quality is: The assurance that a product will fulfill customers' expectations.

Reliability is: The probability that a product will perform its intended function satisfactorily for a prescribed life under certain stated conditions.

In today's market, with customer expectations for better and better quality and ever increasing reliability, the old standards of quality and reliability are not acceptable.

For a manufacturer to remain in the semiconductor business at all, his product must inherently meet and exceed basic quality/reliability standards. Motorola, as the world's largest supplier of semiconductors, has successfully achieved inherent reliability that meets the most strenuous applications and the most adverse environments. Motorola's TMOS products are no exception.

The quality and reliability of Motorola TMOS products are achieved with a four step program:

1. Thoroughly tested designs and materials.
2. Stringent in-process controls and inspections.
3. Process average testing along with 100% quality assurance redundant testing.
4. Reliability verifications through audits and reliability studies.

These steps are detailed in the following pages to provide the reader with a greater insight into the quality and reliability capabilities of Motorola TMOS products.

Reliability Tests

Motorola TMOS products are subjected to a series of extensive reliability tests to verify conformance. These tests are designed to accelerate the failure mechanisms encountered in practical applications, thereby ensuring satisfactory reliable performance in "real world" applications.

The following describes the reliability tests that are routinely performed on Motorola's TMOS devices.

HIGH TEMPERATURE REVERSE BIAS (HTRB) PER MIL-STD-750, METHOD 1039:

The HTRB test is designed to check the stability of the device under "reverse bias" conditions of the main blocking junction at high temperature, as a function of time.

The stability and leakage current over a period of time, for a given temperature and voltage applied across the junction, is indicative of junction surface stability. It is therefore a good indicator of device quality and reliability.

For TMOS devices, voltage is applied between drain and source, and I_{DSS} is monitored. The gate is shorted to the source, to prevent damage due to buildup of charges on the gate.

A failure occurs when the leakage achieves such a high level that the power dissipation causes the device to go into a thermal runaway.

The leakage current of a stable device should remain relatively constant, or increase slightly over the period of the test, typically 1000 hours.

Typical conditions:

T_A = 125°C on product ≥ 500 V V_{DS}

T_A = 150°C on product ≤ 500 V V_{DS}

V_{DS} = 80% of maximum rating

V_{GS} = 0 (shorted)

INTERMITTENT OPERATING LIFE: (IOL OR POWER CYCLING) PER MIL-STD-750, METHOD 1037.

The purpose of the IOL test is to determine the integrity of the chip and/or package assembly to cycling on (device thermally heated due to power dissipation) and cycling off (device thermally cooling due to removal of power applied) as is normally experienced in a "real world" environment.

DC power is applied to the device until the desired function temperature is reached. The power is then switched off, and forced air cooling applied until the junction temperature decreases to ambient temperature.

$$\Delta T_J = \Delta T_C + R_{\theta JC}Pd$$

$$\Delta T_J = 100°C$$

(typically, which is an accelerated condition)

$$\Delta T_C = T_{C\,HIGH} - T_{C\,LOW}$$

The sequence is repeated for the specified number of cycles. The temperature excursion is carefully maintained for repeatability of results.

The Intermittent Operating Life test indicates the degree of thermal fatigue of the die bond interface between the chip and the mounting surface and between the chip and the wire bond interface.

For TMOS devices, parameters used to monitor performance are thermal resistance, threshold voltage, on-resistance, gate-source leakage current and drain-source leakage current.

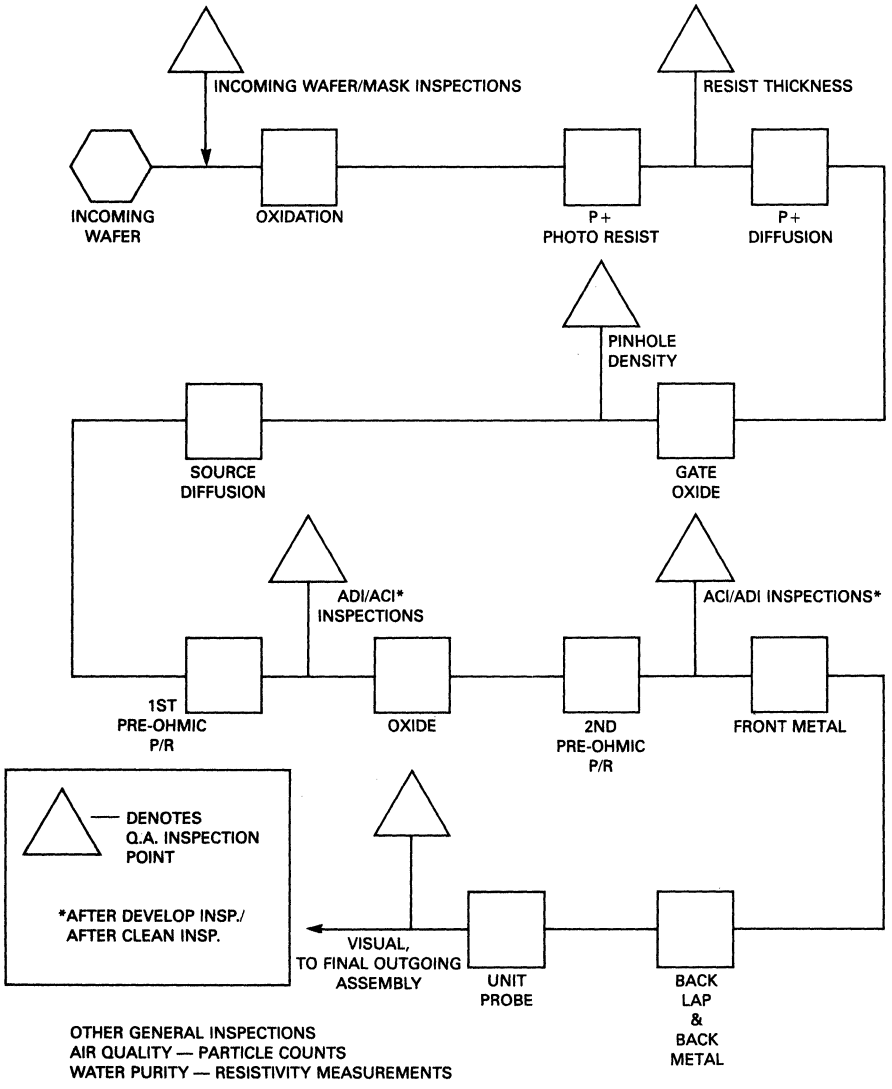
A failure occurs when thermal fatigue causes the thermal resistance or the on-resistance to increase beyond the maximum value specified by the manufacturer's data sheets.

TEMPERATURE CYCLE (TC) PER MIL-STD-750, METHOD 1051:

The purpose of the Temperature Cycle Test is to determine the resistance of the device to high and low temperature excursions in an air medium and the effects of cycling at these extremes.

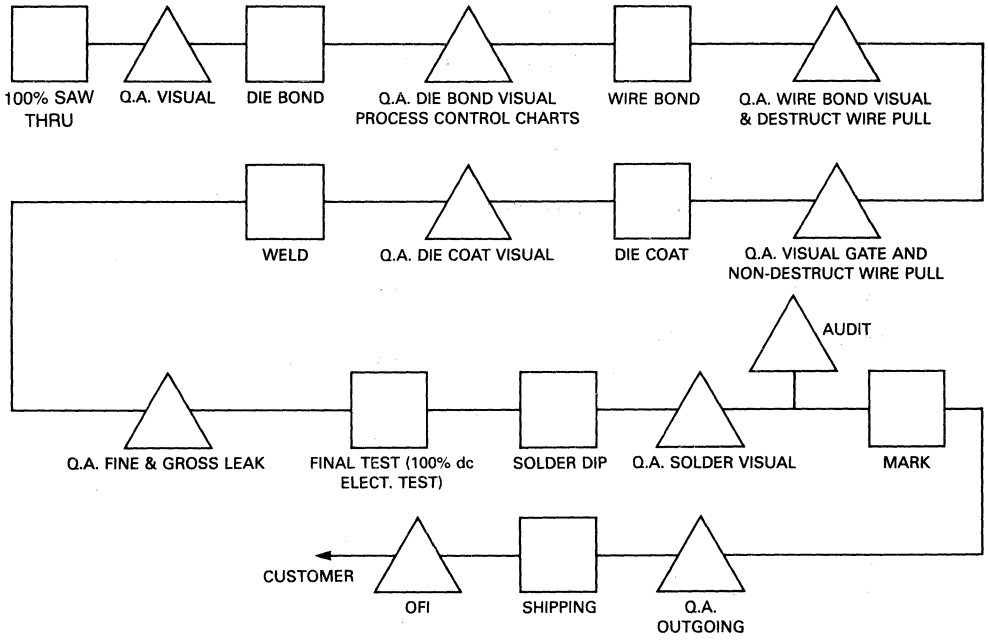
The test is performed by placing the devices alternatively in separate chambers set for high and low temperatures. The air temperature of each chamber is evenly maintained by means of circulation. The chambers have sufficient thermal capacity so that the specified ambient is reached after the devices have been transferred to the chamber.

WAFER PROCESS INSPECTION POINTS
TMOS

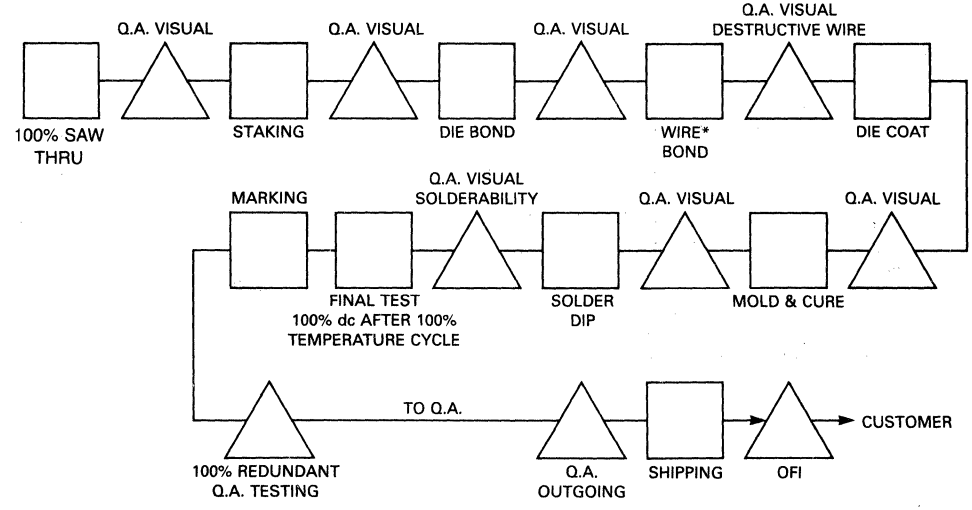


OTHER GENERAL INSPECTIONS
AIR QUALITY — PARTICLE COUNTS
WATER PURITY — RESISTIVITY MEASUREMENTS

IPQA INSPECTION POINTS
POWER METAL TMOS



IPQA INSPECTION POINTS FOR PLASTIC POWER TMOS



*100% NON-DESTRUCT WIRE PULL AFTER WIRE BOND

Each cycle consists of an exposure to one extreme temperature for 15 minutes minimum, then immediately transferred to the other extreme temperature for 15 minutes minimum; this completes one cycle. Note that it is an immediate transfer between temperature extremes and thereby stressing the device greater than non-immediate transfer.

Typical Extremes

(Metal) TO-204 Package device: −65/+200°C

(Plastic) TO-220 Package device: −65/+150°C

The number of cycles can be correlated to the severity of the expected environment. It is commonly accepted in the industry that ten cycles is sufficient to determine the quality of the device.

Typical Cycles for Evaluations and Audits:

TO-204 and TO-220 devices: Minimum 100 cycles

TO-204 and TO-220 devices: Maximum 1000 cycles

Temperature cycling identifies any excessive strains set up between materials within the device due to differences in coefficients of expansion.

A failure occurs when there is a change in the device's parameters beyond specified levels, or when a device checks electrically as "open" or "short".

THERMAL SHOCK (TC) PER MIL-STD-750, METHOD 1056:

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature.

The test is performed by placing the devices in a mesh basket, then alternatively immerse in baths of liquid (maintained at −55°C and +150°C). They are kept for thirty seconds in each bath and immediately transferred to the alternate bath.

This test produces sudden heating and cooling of the device, and produces unusual stresses due to the short term temperature gradients that are set up. It is commonly accepted in the industry that five cycles is sufficient to determine the quality of the device.

A failure occurs when there is a change in the device's parameters beyond specified levels, or when a device checks electrically as "open" or "short".

PRESSURE COOKER TEST (OR AUTOCLAVE TEST):

The purpose of the "pressure cooker" test is to determine the resistance of the device to moisture by subjecting it to relatively high steam pressure levels. This is only performed on nonhermetic packages (i.e., plastic/epoxy encapsulated devices), and not on hermetic packages (i.e., metal can devices).

A "pressure cooker" providing a pressure of 15 pounds per square inch over atmosphere is used (1 atmosphere = 14.7 psig). A wire mesh tray is constructed inside to keep the devices approximately two inches above the surface of deionized water and to prevent condensed water from collecting on them.

After achieving the working value, the pressure is maintained for a minimum of 24 hours (reliability evaluations have demonstrated conclusively that particular epoxies are very near hermetic). The devices are then removed and air dried for a minimum of four hours and a maximum of 24 hours before data is recorded.

Parameters that are usually monitored are leakage currents and voltage.

HIGH TEMPERATURE GATE BIAS (HTGB): PER MIL-STD-750, METHOD 1039:

The HTGB test is designed to electrically stress the gate oxide at the maximum rated dc bias voltage at high temperature. The test is designed to detect for drift caused by random oxide defects and ionic oxide contamination.

For TMOS devices, a voltage of ±20 V is applied between the gate-source. The drain is shorted to the source which is at ground potential. Typical temperature, T_A = 150°C, time = 168 hours ≥ t ≤ 1000 hours.

Any oxide defects present will lead to early device failure in the form of I_{GSS} short.

HIGH TEMPERATURE STORAGE LIFE (HTSL) TEST: PER MIL-STD-750, METHOD 1032.

The HTSL test is designed to indicate the stability of the devices, their potential to withstand high temperatures and the internal manufacturing integrity of the package. Although devices are not exposed to such extreme high temperatures in the field, the purpose of this test is to accelerate any failure mechanisms that could occur during long periods at storage temperatures.

The test is performed by placing the devices in a mesh basket, then placed in a high temperature chamber at a controlled ambient temperature, as a function of time. Typical conditions:

T_A = 150°C on Plastic package

T_A = 200°C on Metal package

t = 1000 hours

HIGH HUMIDITY HIGH TEMPERATURE REVERSE BIAS (H^3TRB) TEST: PER MIL-STD-750, METHOD 1039.

The H^3TRB test is designed to determine the resistance of component parts and constituent materials to the combined deteriorative effects of prolonged operation in a high temperature/high humidity environment. This test only applies to nonhermetic devices.

Humidity has been a traditional enemy of semiconductors, particularly plastic packaged devices. Most moisture related degradations result, directly or indirectly, from penetration of moisture vapor through passivating materials, and from surface corrosion. At Motorola, this former problem has been effectively addressed and controlled through use of junction "passivation" process, die coating, and proper selection of package materials.

For TMOS devices, voltage is applied between drain and source. The gate is shorted to the source, to prevent damage due to buildup of charges on the gate. The test is performed in a chamber at 85 percent relative humidity and 85°C. Typical time = 168 hours ≥ t ≤ 1000 hours.

ENVIRONMENTAL PACKAGE RELATED TEST PROGRAMS:

A. Physical Dimensions — Mil-Std-750, Method 2066. This test is performed to determine the conformance to device outline drawing specifications.

B. Visual and mechanical examination — Mil-Std-750, Method 2071. A test to determine the acceptability of product to certain cosmetic and functional criteria such as marking legibility, stains, etc.

C. Resistance to Solvents — Mil-Std-202, Method 2025.3. A test to determine the solderability of device terminals.

D. Terminal Strength — Mil-Std-750, Method 2036. This test is a lead bend test to check for lead strength.

E. Constant Acceleration — Mil-Std-750, Method 2006. The parts are accelerated to 20,000 G's and higher to check for defects that would show up in this environment.

F. Vibration Variable Frequency — Mil-Std-750, Method 2056. Parts are vibrated in different planes and at different frequencies to check for loose particles or ruptured wire or die bonds.

Every manufacturing process exhibits a quality and reliability distribution. This distribution must be controlled to assure a high mean value, a narrow range and a consistent shape. Through proper design and process control this can be accomplished, thereby reducing the task of screening programs which attempt to eliminate the lower tail of the distribution.

ACCELERATED STRESS TESTING

The nature of some tests in this report is such that they far exceed that which the devices would see in normal operating conditions. Thus, the test conditions "accelerate" the failure mechanisms in question and allow Motorola to predict failure rates in a much shorter amount of time than otherwise possible. Failure modes that are temperature dependent are characterized by the Arrhenius model.

$$AF = e^{\frac{EA}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)}$$

EA = Activation Energy, approximately 1.0 ev

K = Boltzman's Constant = 8.62×10^{5} ev/°K

T2 = Operating Temperature

T1 = Test Temperature

Therefore, actual device hours (at test conditions) = AF (accumulated device hours at operating temperature). See following charts.

REVIEW OF DATA

High Temperature Reverse Bias (HTRB) indicates the stability of leakage current, which is related to the field distortion of TMOS devices. HTRB enhances the failure mechanism by high temperature reverse bias testing, and therefore is a good indicator of device quality and reliability, along with verification that process controls are effective. Motorola has processed through HTRB 6,166 devices (plastic and metal TMOS) with a total of three failures, which equates to equivalent device hours at 90°C of 1.8×10^{8} or 20 fits.* In terms of customer expectation, this relates to a mean (average) time between failure of 5,723.4 years.

High Temperature Gate Bias (HTGB) checks the stability of the device under "gate bias" forward conditions at accelerated high temperature, as a function of time. This test is performed to electrically stress the gate oxide to detect for drift caused by random oxide defect. This failure mechanism appears in the infant and random zones of the reliability "bath tub curve" at a very low rate of defect. Motorola has processed 812 devices (plastic and metal TMOS) with a total of one failure, which equates to equivalent device hours at 90°C of 2.4×10^{7} or 68 fits. In terms of customer expectation, this relates to a mean (average) time between failures of 1,717.0 years.

Intermittent Operating Life (IOL) is an excellent accelerated stress test to determine the integrity of the chip and/or package assembly to cycling on (device thermally heated due to power dissipation) and cycling off (device thermally cooling due to removal of power applied). This test is perhaps the most important test of all, along with simulating what is normally experienced in a "real world" environment. IOL exercises die bond, wire bonds, turning on the device, turning off the device, relates the device performance, and verifying the thermal expansion of all materials are compatible. Motorola performs extensive IOL testing as a continual process control monitor that best relates to the "device system**" as a whole. Motorola also performs extensive analysis and comparison of delta junction temperatures. Motorola has determined that to effectively stress the device a delta T_j of 100°C is necessary therefore, far exceeding many customers' application and better determine the reliability modeling of the device. Motorola has processed 6,429 devices (plastic and metal TMOS) with a total of 2 failures, which equates to actual device cycles of 2.3×10^{7} or 115 fits. In terms of customer expectation, this relates to a mean (average) time between failures of 1,007.3 years.

Temperature Cycling (TC) is also an excellent stress test to determine the resistance of the device to high and low temperature excursions in an air medium. Where IOL electrically stresses the "device system" from internally, temperature cycle stresses the "device system" thermally from external environment conditions. Motorola has processed 14,149 devices (plastic and metal TMOS) with a total of zero failures, which equates to actual device cycles of 9.4×10^{5} or 800 fits. In terms of customer expectation, this mean (average) time between failures of 143.1 years.

High Temperature Storage Life (HTSL), High Humidity Temperature Reverse Bias (H^3TRB), Thermal Shock (TC) and "Pressure Cooker" (Autoclave) are routinely tested, however it is felt by Motorola Reliability Engineering that HTRB, HTGB, IOL and TC are the most important tests

*fit(s): The value of fit is calculated directly from the failure rate which is a calculation based upon the number of rejects and total device hours/cycles. One fit represents one failure in one billion hours.

**Device System: The mechanical and physical properties combination which, once manufactured result in the form of a device.

and therefore the area of concentration. Motorola has been in the semiconductor industry for many, many years and would not have remained there without our continued reliability, quality and customer relations.

TABLE 1

Test	Total No. of Devices	Total No. of Failures	Actual Device Hrs. or Cycles	Equivalent Device Hrs. @ 90°C	Random Failure Rate %/1000 hrs.	Fits Note 2	MTBF (Hours) Note 3	MTBF (Years)
HTRB V_{DS} = 80% max rating V_{GS} = 0 (shorted), T_A = 125°C on product ≥ 500 V V_{DS} T_A = 150°C on product < 500 V V_{DS}	6,166	3	1.8×10^6	1.8×10^8	0.0020	20	5.0×10^7	5,723.4
HTGB V_{GS} = +20 V V_{DS} = 0 (shorted) T_A = 150°C	812	1	2.3×10^5	2.4×10^7	0.0068	68	1.5×10^7	1,717.0
H^3TRB 85°C @ 85% RH V_{GS} = 0 (shorted) V_{DS} = 80% max rating up to 500 V	213 /	0	2.1×10^5	—	0.3200	3,200	3.1×10^5	35.0
HTSL T_A = 150°C for TO-220 T_A = 200°C for TO-204 (TO-3)	369	0	3.7×10^5	3.820×10^7	0.0019	19	5.4×10^7	6,181.3
IOL ΔT_j = 100°C Free Air	6,429	2	2.3×10^7	—	0.0115	115	8.8×10^6	1007.
TEMPERATURE CYCLE TO-220 −65/+150°C extremes TO-204 (TO-3) −65/+200°C extremes	14,149	0	9.4×10^5	—	0.0800	800	1.3×10^6	143.1
THERMAL SHOCK −55/+150°C extremes	329	0	3.3×10^4	—	2.1	21,000	4.7×10^4	5.4
PRESSURE COOKER P = 14.7psig, no bias, T = 121°C	830	2	6.2×10^4	—	4.1	41,000	2.4×10^4	2.7

NOTE 2: *Failure Unit (FIT):*
Modern electronic system reliability utilizing today's semiconductor devices requires quite low component failure rates, and therefore requires a workable number. This number called a FIT (Failure Unit) is defined as: FIT = one failure on 10^9 device hours.

NOTE 3: *Mean Time Between Failures (MTBF):*
The significant distribution properties of electronic system reliability is expressed as MTBF, which is defined as:

$t = 1/\lambda$
Where, t = time, hours
λ = failure rate

Audit Program and AOQ Monitors

AUDIT PROGRAM

Motorola has maintained a real time process control audit program for a number of years since entering the TMOS marketplace. The audit is continually expanding and being refined, through short and long-term stress testing. The concept of Motorola's real time short-term stress testing is to detect infant mortality defects, failure modeling through identification of failure mode/mechanism, and data base generation that verifies all process controls are effective. Once these defects are highlighted in the audit testing, the system requires rapid corrective action so that problems are kept within the factory and are not sent to the customer. The concept of the long-term stress testing is to detect random failure and wear out phenomenon along with the associated failure modeling. Through proper failure identification and modeling, Motorola's Reliability engineers can effectively calculate meaningful failure rates.

AVERAGE OUTGOING QUALITY (AOQ)

With the industry trend to average outgoing qualities (AOQ) of less than 100 ppm, the role of device final test, and final outgoing quality assurance have become a key ingredient to success. At Motorola, all parts are 100% tested to process average limits then the yields are monitored closely by product engineers, and abnormal areas of fallout are held for engineering investigation. Motorola also 100% redundant tests all DC parameters again after

marking the device to further reduce any mixing problems associated with the first test. Prior to shipping, the parts are again sampled, tested to a tight sampling plan by our Quality Assurance department, and finally our OFI inspection checks for paperwork, mixed product, visual and mechanical prior to packaging to the customers.

AVERAGE OUTGOING QUALITY (AOQ)

$$AOQ = \text{Process Average} \times \text{Probability of Acceptance} \times 10^6 \text{ (PPM)}$$

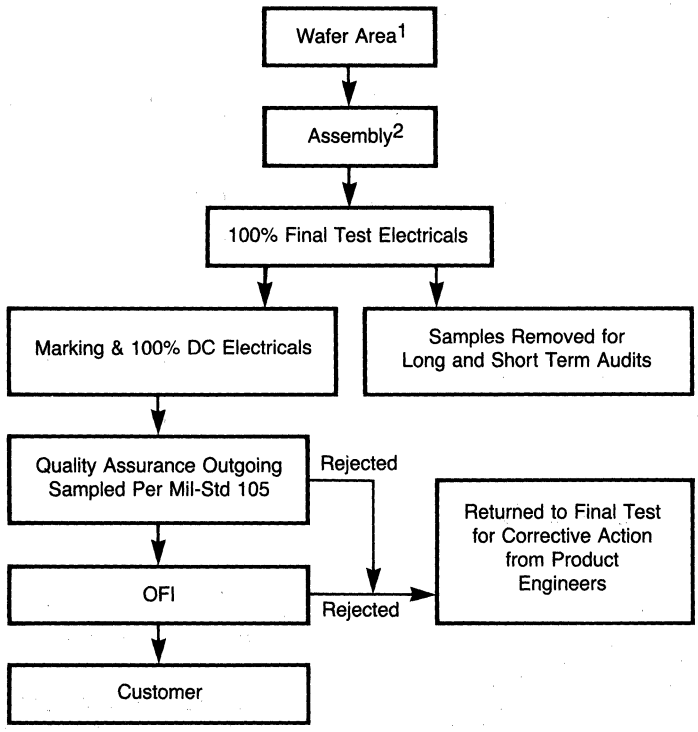
$$\text{Process Average} = \frac{\text{No. of Reject Devices}}{\text{No. of Devices Tested}}$$

$$\text{Probability of Acceptance} = \left(1 - \frac{\text{No. of Lots Rejected}}{\text{No. of Lots Tested}}\right)$$

$$10^6 = \text{To Convert to Parts Per Million}$$

$$AOQ = \frac{\text{No. of Reject Devices}}{\text{No. of Devices Tested}} \times \left(1 - \frac{\text{No. of Lots Rejected}}{\text{No. of Lots Tested}}\right) \times 10^6 \text{ (PPM)}$$

FLOW CHART OF TMOS PRODUCTS



Note 1: See Wafer Flow Chart (Page 12-2)
Note 2: See Assembly Flow Chart (Page 12-3)

Essentials of Reliability:

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of trouble free service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. Reliability can be redefined as the probability of failure free performance, under a given manufacturer's specifications, for a given period of time. The failure rate of semiconductors in general, when plotted versus a long period of time, exhibit what has been called the "bath tub curve" (Figure 12-1).

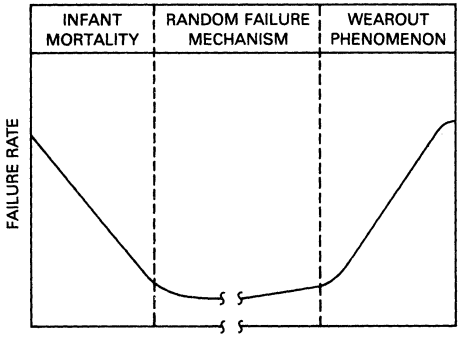


FIGURE 12-1 — FAILURE RATE OF SEMICONDUCTOR

RELIABILITY MECHANICS

Since reliability evaluations usually involve only samples of an entire population of devices, the concept of the central limit theorem applies and a failure rate is calculated using the λ^2 distribution through the equation:

$$\lambda \leq \frac{\lambda^2\,(\alpha,\ 2r + 2)}{2\ nt}$$

λ^2 = chi squared distribution

where $\alpha = \frac{100 - cl}{100}$

λ = Failure rate

cl = Confidence limit in percent

r = Number of rejects

n = Number of devices

t = Duration of tests

The confidence limit is the degree of conservatism desired in the calculation. The central limit theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate, and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 12-2).

The term $(2r + 2)$ is called the degrees of freedom and is an expression of the number of rejects in a form suitable

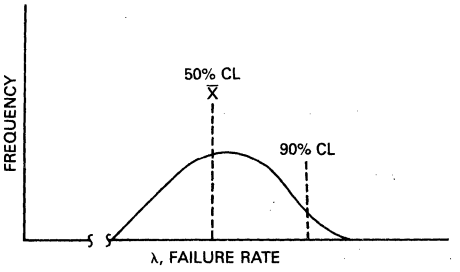


FIGURE 12-2 — CONFIDENCE LIMITS AND THE DISTRIBUTION OF SAMPLE FAILURE RATES

to λ^2 tables. The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the λ^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate. Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_o(t)e^{-o/KT}$$

Where R(t) = reaction rate as a function of time and temperature

R_o = A constant

t = Time

T = Absolute temperature, °Kelvin (°C + 273°)

o = Activation energy in electron volts (ev)

K = Boltzman's constant = 8.62×10^{-5} ev/°K

This equation can also be put in the form:

AF = Acceleration factor

T2 = User temperature

T1 = Actual test temperature

The Arrhenius equation states that reaction rate increases exponentially with the temperature. This produces a straight line when plotted on log-linear paper with a slope expressed by o. o may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The overall activation energy exhibited by TMOS Power FETs is 1.0 ev.

RELIABILITY QUALIFICATIONS/EVALUATIONS OUTLINE:

Some of the functions of Motorola Reliability and Quality Assurance Engineering is to evaluate new products for introduction, process changes (whether minor or major), and product line updates to verify the integrity and reliability of conformance, thereby ensuring satisfactory performance in the field. The reliability evaluations may be subjected to a series of extensive reliability testing, such

as those outlined in the "Tests Performed" section, or special tests, depending on the nature of the qualification requirement.

High Reliability Power MOSFET Products

Motorola has the broadest line of MIL-qualified discrete and integrated circuits for the widest range of designs. Power MOSFETs are being processed at this time to join the qualified products portfolio available from Motorola.

Complete facilities are available to conduct all three product levels of testing on Power MOSFETs in TO-204AA (TO-3), TO-205AF (TO-39), and TO-213AA (TO-66) hermetic packages. Devices designated as "JAN" or equivalent, receive lot sampling only while "JTX" and "JTXV" devices or equivalents receive 100% screening.

Motorola offers Power MOSFETs of a custom nature which have been processed to the specific high reliability requirements of a critical scientific or industrial application.

Figure 12-3 illustrates the processing flow for JAN, JTX, and JTXV and their equivalent Power MOSFETs in accordance with MIL-S-19500.

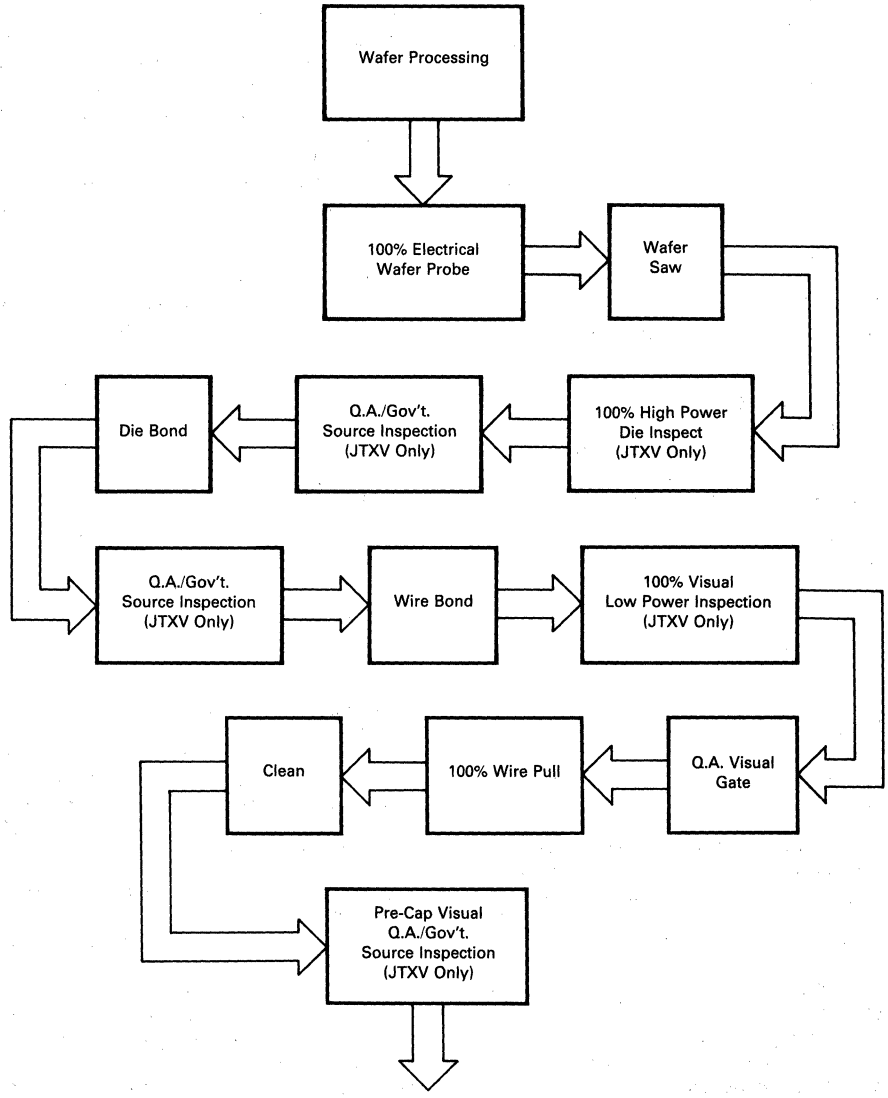
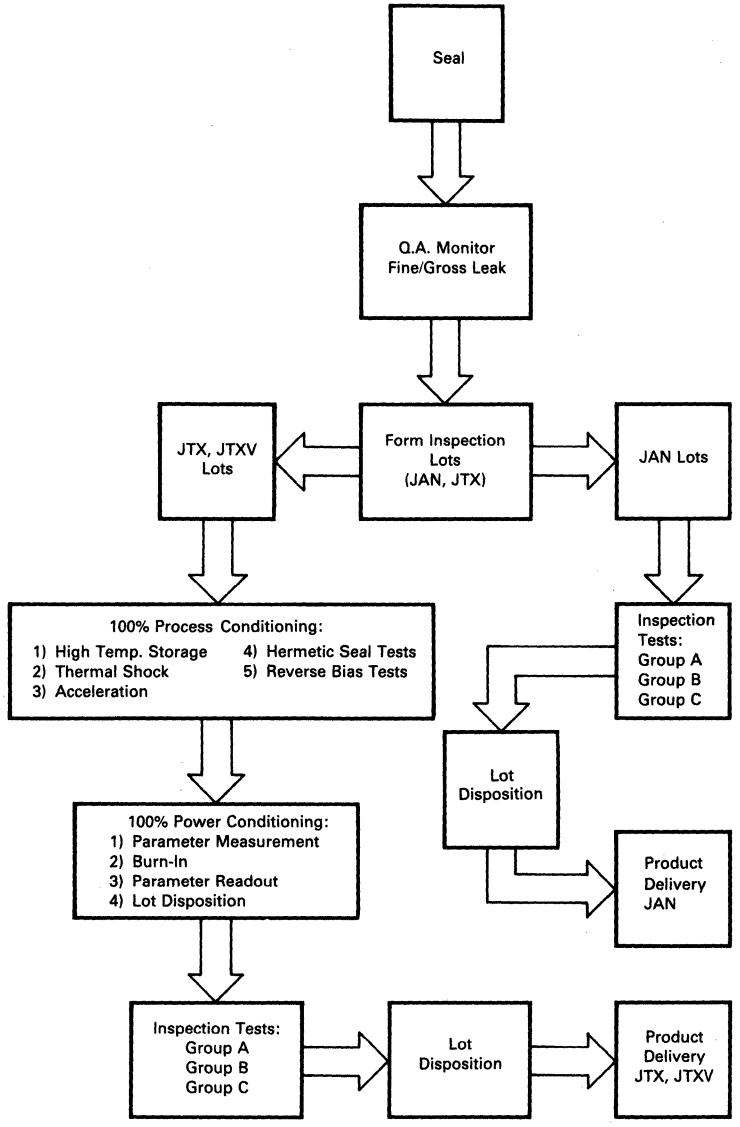


FIGURE 12-3 — JAN, JTX, JTXV AND/OR EQUIVALENT PROCESS FLOW:


Seal
Q.A. Monitor
Fine/Gross Leak
JTX, JTXV
Lots
Form Inspection
Lots
(JAN, JTX)
JAN Lots
100% Process Conditioning:
1) High Temp. Storage
2) Thermal Shock
3) Acceleration
4) Hermetic Seal Tests
5) Reverse Bias Tests
Inspection
Tests:
Group A
Group B
Group C
Lot
Disposition
Product
Delivery
JAN
100% Power Conditioning:
1) Parameter Measurement
2) Burn-In
3) Parameter Readout
4) Lot Disposition
Inspection Tests:
Group A
Group B
Group C
Lot
Disposition
Product
Delivery
JTX, JTXV

Motorola High Reliability Parts Pending QUAL as of JAN 1984

Device Type	MIL-S 19500/	Package	*QUAL Status	P_T (W)	I_D (A)	$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	C_{iss} (pF)	C_{oss} (pF)	C_{rss} (pF)
2N6756 JAN	542A	TO-204AA TO-3	IP	75	14	100	0.18	800	500	150
JTX	542A	TO-204AA TO-3	IP	75	14	100	0.18	800	500	150
JTXV	542A	TO-204AA TO-3	IP	75	14	100	0.18	800	500	150
2N6758 JAN	542A	TO-204AA TO-3	IP	75	9.0	200	0.4	800	450	150
JTX	542A	TO-204AA TO-3	IP	75	9.0	200	0.4	800	450	150
JTXV	542A	TO-204AA TO-3	IP	75	9.0	200	0.4	800	450	150
2N6760 JAN	542A	TO-204AA TO-3	IP	75	5.5	400	1.0	800	300	80
JTX	542A	TO-204AA TO-3	IP	75	5.5	400	1.0	800	300	80
JTXV	542A	TO-204AA TO-3	IP	75	5.5	400	1.0	800	300	80
2N6762 JAN	542A	TO-204AA TO-3	IP	75	4.5	500	1.5	800	200	60
JTX	542A	TO-204AA TO-3	IP	75	4.5	500	1.5	800	200	60
JTXV	542A	TO-204AA TO-3	IP	75	4.5	500	1.5	800	200	60
2N6764 JAN	543A	TO-204AE TO-3	P	150	38	100	0.055	3000	1500	500
JTX	543A	TO-204AE TO-3	P	150	38	100	0.055	3000	1500	500
JTXV	543A	TO-204AE TO-3	P	150	38	100	0.055	3000	1500	500
2N6766 JAN	543A	TO-204AE TO-3	P	150	30	200	0.085	3000	1200	500
JTX	543A	TO-204AE TO-3	P	150	30	200	0.085	3000	1200	500
JTXV	543A	TO-204AE TO-3	P	150	30	200	0.085	3000	1200	500
2N6768 JAN	543A	TO-204AA TO-3	P	150	14	400	0.3	3000	600	200
JTX	543A	TO-204AA TO-3	P	150	14	400	0.3	3000	600	200
JTXV	543A	TO-204AA TO-3	P	150	14	400	0.3	3000	600	200
2N6770 JAN	543A	TO-204AA TO-3	P	150	12	500	0.4	3000	600	200
JTX	543A	TO-204AA TO-3	P	150	12	500	0.4	3000	600	200
JTXV	543A	TO-204AA TO-3	P	150	12	500	0.4	3000	600	200
2N6823 JAN	543A	TO-204AA TO-3	*P*	100	3.0	600	2.8	1000	400	100
JTX	543A	TO-204AA TO-3	*P*	100	3.0	600	2.8	1000	400	100
JTXV	543A	TO-204AA TO-3	P	100	3.0	600	2.8	1000	400	100
2N6826 JAN	543A	TO-204AA TO-3	*P*	150	8.0	600	0.9	1500	400	180
JTX	543A	TO-204AA TO-3	P	150	8.0	600	0.9	1500	400	180

Motorola High Reliability Parts Pending QUAL as of JAN 1984 (Continued)

Device Type	MIL-S 19500/	Package	*QUAL Status	P_T (W)	I_D (A)	$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	C_{iss} (pF)	C_{oss} (pF)	C_{rss} (pF)
JTXV	543A	TO-204AA TO-3	P	150	8.0	600	0.9	1500	400	180
2N6782 JAN	556	TO-205AF TO-39	P	15	3.5	100	0.6	200	100	25
JTX	556	TO-205AF TO-39	P	15	3.5	100	0.6	200	100	25
JTXV	556	TO-205AF TO-39	P	15	3.5	100	0.6	200	100	25
2N6784 JAN	556	TO-205AF TO-39	P	15	2.25	200	1.5	200	80	25
JTX	556	TO-205AF TO-39	P	15	2.25	200	1.5	200	80	25
JTXV	556	TO-205AF TO-39	P	15	2.25	200	1.5	200	80	25
2N6786 JAN	556	TO-205AF TO-39	P	15	1.25	400	3.6	200	50	15
JTX	556	TO-205AF TO-39	P	15	1.25	400	3.6	200	50	15
JTXV	556	TO-205AF TO-39	P	15	1.25	400	3.6	200	50	15
2N6788 JAN	555	TO-205AF TO-39	P	20	6.0	100	0.3	600	400	100
JTX	555	TO-205AF TO-39	P	20	6.0	100	0.3	600	400	100
JTXV	555	TO-205AF TO-39	P	20	6.0	100	0.3	600	400	100
2N6790 JAN	555	TO-205AF TO-39	P	20	3.5	200	0.8	600	300	80
JTX	555	TO-205AF TO-39	P	20	3.5	200	0.8	600	300	80
JTXV	555	TO-205AF TO-39	P	20	3.5	200	0.8	600	300	80
2N6792 JAN	555	TO-205AF TO-39	P	20	2.0	400	1.8	600	200	40
JTX	555	TO-205AF TO-39	P	20	2.0	400	1.8	600	200	40
JTXV	555	TO-205AF TO-39	P	20	2.0	400	1.8	600	200	40
2N6794 JAN	555	TO-205AF TO-39	P	20	1.5	500	3.0	600	150	40
JTX	555	TO-205AF TO-39	P	20	1.5	500	3.0	600	150	40
JTXV	555	TO-205AF TO-39	P	20	1.5	500	3.0	600	150	40
2N6796 JAN	557	TO-205AF TO-39	P	25	8.0	100	0.18	900	500	150
JTX	557	TO-205AF TO-39	P	25	8.0	100	0.18	900	500	150
JTXV	557	TO-205AF TO-39	P	25	8.0	100	0.18	900	500	150
2N6798 JAN	557	TO-205AF TO-39	P	25	5.5	200	0.4	900	450	100
JTX	557	TO-205AF TO-39	P	25	5.5	200	0.4	900	450	100
JTXV	557	TO-205AF TO-39	P	25	5.5	200	0.4	900	450	100
2N6800 JAN	557	TO-205AF TO-39	P	25	3.0	400	1.0	900	300	80

Motorola High Reliability Parts Pending QUAL as of JAN 1984 (Continued)

Device Type	MIL-S 19500/	Package	*QUAL Status	P_T (W)	I_D (A)	$V_{(BR)DSS}$ (V)	Ω $r_{DS(on)}$	C_{iss} (pF)	C_{oss} (pF)	C_{rss} (pF)
JTX	557	TO-205AF TO-39	P	25	3.0	400	1.0	900	300	80
JTXV	557	TO-205AF TO-39	P	25	3.0	400	1.0	900	300	80
2N6802 JAN	557	TO-205AF TO-39	P	25	2.5	500	1.5	900	200	60
JTX	557	TO-205AF TO-39	P	25	2.5	500	1.5	900	200	60
JTXV	557	TO-205AF TO-39	P	25	2.5	500	1.5	900	200	60

*IP denotes qualification in process
**P denotes proposed qualifications

Chapter 13: Mounting Techniques For Power MOSFETs

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, semiconductor-industry field history indicates that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction temperature from 160°C to 135°C.*

Many failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from mounting securely to a warped surface. With the widespread use of various plastic-packaged semiconductors, the dimension of mechanical damage becomes very significant.

Figure 13-1 shows an example of doing nearly everything wrong. In this instance, the device to be victimized is in the TO-220 package. The leads are bent to fit into a socket — an operation which, if not properly done, can crack the package, break the bonding wires, or crack the dice. The package is fastened with a sheet-metal screw through a ¼"-hole containing a fiber-insulating sleeve. The force used to tighten the screw pulls the package into the hole, causing enough distortion to crack the dice. Even if the dice were not cracked, the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heat sink surface and some burns around the hole are present, many — but unfortunately not all — poor mounting practices are covered.

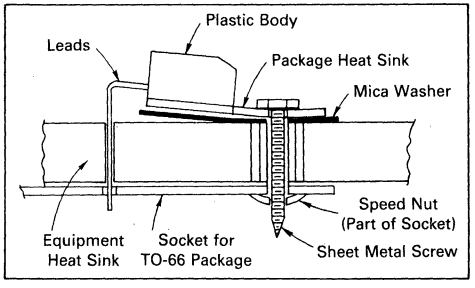


FIGURE 13-1 — EXTREME CASE OF IMPROPERLY MOUNTING A SEMICONDUCTOR (DISTORTION EXAGGERATED)

In many situations the case of the semiconductors must be isolated electrically from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are being handled. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures necessitate attention to the following areas:

1. Mounting surface preparation
2. Application of thermal compounds
3. Installation of the insulator
4. Fastening of the assembly
5. Lead bending and soldering

In this Chapter, the procedures are discussed in general terms. Specific details for each class of packages are given in the figures and in Table 1. Appendix A contains a brief review of thermal resistance concepts, and Appendix B lists sources of supply for accessories. Motorola supplies hardware for most power packages. It is detailed on separate data sheets for each package type.

Mounting Surface Preparation

In general, the heat-sink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heat-sink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 13-2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e. Δh/TIR, is satisfactory in most cases if less than 4.0 mils per inch, which is normal for extruded aluminum — although disc type devices usually require 1.0 mil per inch.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory*; a finer finish is costly to achieve and does not significantly lower contact resistance. Most commercially available cast or extruded heat sinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger packages having mounting holes removed from the semiconductor die location, such as TO-204AA (TO-3), may successfully be used with larger holes to accommodate an insulating bushing, but Thermopad plastic packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heat sink around the mounting hole can cause two problems.

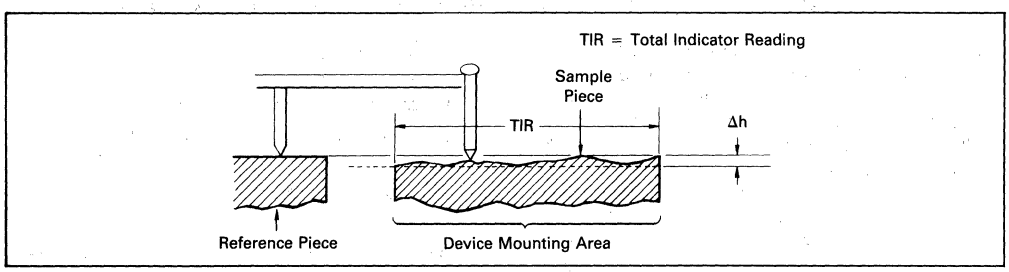


FIGURE 13-2 — SURFACE FLATNESS

The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heat sink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heat sink. The first effect may often be detected immediately by visible cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heat sinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heat sinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. The edges should be broken to remove burrs which cause poor contact between device and heat sink and may puncture isolation material.

Many aluminum heat sinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heat sinks. For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heat sink, anodized or painted surfaces may be more effective than other insulating materials which tend to creep (i.e., they flow), thereby reducing contact pressure.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Unless used immediately after machining, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse. Thermal grease should be immediately applied thereafter and the semiconductor attached as the grease readily collects dust and metal particles.

Thermal Compounds

To improve contacts, thermal joint compounds or greases are used to fill air voids between all mating surfaces. Values of thermal resistivity vary from 0.10°C-in/W for copper film to 1200°C-in/W for air, whereas satisfactory joint compounds will have a resistivity of approximately 60°C-in/W. Therefore, the voids, scratches, and imperfections which are filled with a joint compound, will have a thermal resistance of about 1/20th of the original value which makes a significant reduction in the overall interface thermal resistance.

Joint compounds are a formulation of fine zinc particles in a silicon oil which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Experience will indicate whether the quantity is sufficient, as excess will appear around the edges of the contact area. To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the assembly.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator and is therefore highly desirable despite the handling problems

*Tests run by Thermalloy (Catalog #74-INS-3, page 14) using a copper TO-204AA (TO-3) package with a typical 32-microinch finish, showed that finishes between 16 and 64 μ-in caused less than ± 2.5% difference in interface thermal resistance.

TABLE 1 — Approximate Values for Interface Thermal Resistance and Other Package Data (See Table 2 for Case Number to JEDEC Outline Cross-Reference)

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heat sink. (See Note 3)

Package Type and Data					Interface Thermal Resistance (°C/W)					
					Metal-to-Metal		With Insulator			
JEDEC Outline	Description	Recommended Mounting Hole and Drill Size	Machine Screw Size[2]	Torque In-Lb	Dry	Lubed	Dry	Lubed	Type	See Note
TO-204AA (TO-3)	Diamond Flange	0.140, #28	6-32	6.0	0.5	0.2	1.3	0.36	3 mil Mica	1
TO-213AA (TO-66)	Diamond Flange	0.140, #28	6-32	6.0	1.5	0.5	2.3	0.9	2 mil Mica	
TO-218AC	5/8" x 1/2"	0.140, #28	6-32	6.0	0.75	0.40	1.60	0.7	2 mil Mica	
TO-220AB	Thermowatt	0.140, #28	6-32	8.0	1.2	1.0	3.4	1.6	2 mil Mica	1, 2
TO-225AA (TO-126)	Thermopad 1/4" x 3/8"	0.113, #33	4-40	6.0	2.0	1.3	4.3	3.3	2 mil Mica	
CASE 346-01	2" x 2 1/8"	0.191, #11	10.32	20	0.19	0.07	0.4	0.20	3 mil Mica	
CASE 353-01	1 1/8" x 1 1/2"	0.140, #28	6-32	8.0	0.57	0.1	0.96	0.30	3 mil Mica	

Note 1: See Figures 13-3 and 13-4 for additional data on TO-204AA (TO-3) and TO-220 packages.

Note 2: Screw not insulated.

Note 3: Measurement of Interface Thermal Resistance. Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the device, a thermocouple on the heat sink, and a means of applying and measuring dc power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by the surface flatness and finish and the amount of pressure on the surfaces. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are in poor agreement.

created by its affinity for foreign matter. Some sources of supply for joint compounds are shown in Appendix B.

Some users and heat-sink manufacturers prefer not to use compounds. This necessitates use of a heat sink with lower thermal resistance which imposes additional cost, but which may be inconsequential when low power is being handled. Others design on the basis of not using grease, but apply it as an added safety factor, so that if improperly applied, operating temperatures will not exceed the design values.

Consider the TO-220 package shown in the accompanying figure. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO-220 packages are slightly concave and use of a spreader bar under the screw lessens the lifting, but some is inevitable with a single-ended package.

The thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heat sink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The EIA location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

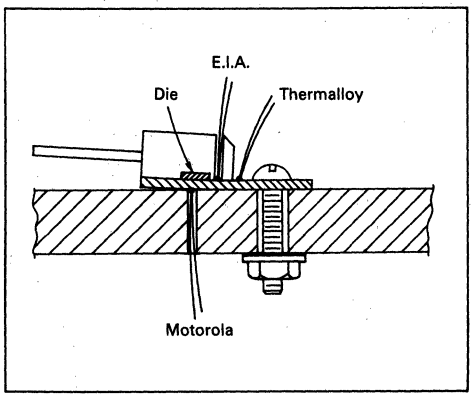
c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the EIA location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance is constant for a given setup, junction-to-case values decrease and case-to-sink values increase as the case thermocouple readings become warmer.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heat sink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heat sink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple temperature at the Thermalloy location could be close to the temperature at the EIA location as the lateral heat flow is generally small.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power

JEDEC TO-220 Package mounted to heat sink showing various thermocouple locations and lifting caused by pressure at one end.



ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the higher temperature of the case at a point where, hopefully, the device is making contact to the heat sink, since heat sinks are measured from the point of device contact to the ambient. Once the special heat sink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1.0°C/W for a TO-220 package mounted to a heat sink without thermal grease and no insulator. This error is small when compared to the heat dissipators often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant, and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heat sink. The washer is flat to within 1.0 mil/inch, has a finish better than 63 μ-inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use and yields reproducible results. At this printing, however, sufficient data to compare results to other methods is not available.

The only way to get accurate measurements of the interface resistance is to also test for junction-to-case thermal resistance at the same time. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

TABLE 2 — Cross Reference Chart

Motorola Case Number to JEDEC Outline Number and Table 1 Reference

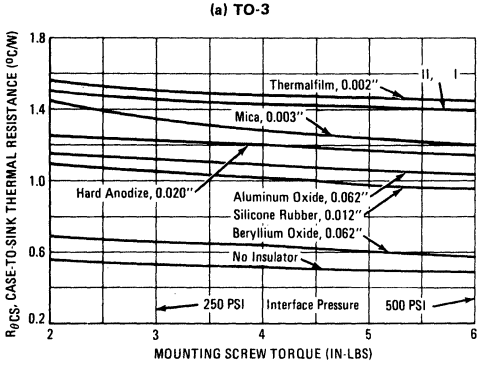
Motorola Number	JEDEC Number	Reference in Table 1
1	TO-204AA (TO-3)	TO-204AA (TO-3)
77	TO-225AA (TO-126)	TO-225AA (TO-126)
80	TO-213AA (TO-66)	TO-213AA (TO-66)
197	TO-204AE	TO-204AE
221A	TO-220AB	TO-220AB
340	TO-218AC	TO-218AC
346	MO-040AA	CASE 346
353	—	CASE 353

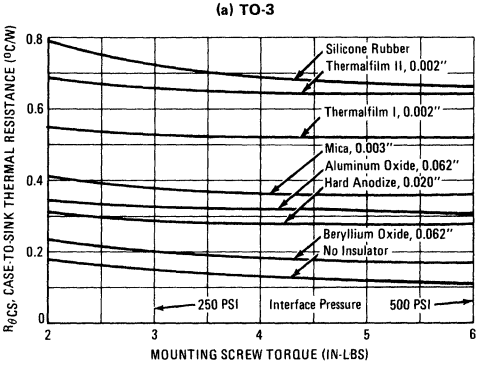
Insulation Considerations

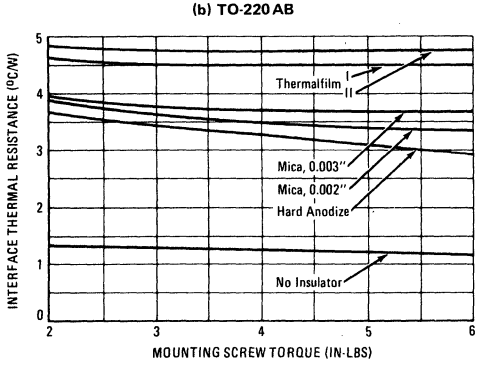
Since it is most expedient to manufacture power MOSFETs with drains electrically common to the case, the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, it is best to isolate the entire heat sink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heat sink. Where heat sink isolation is not possible, because of safety reasons or in instances where a chassis serves as a heat sink or where a heat sink is common to several devices, insulators are used to isolate the individual components from the heat sink.

When an insulator is used, thermal grease assumes greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a markedly uneven surface. Reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torque applied to TO-204AA (TO-3) and TO-220 packages, are shown in Figure 13-3 for bare surfaces and Figure 13-4 for greased surfaces. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case). When high power is handled, beryllium oxide is unquestionably the best choice. Thermafilm is Thermalloy's trade name for a polyimide material which is also commonly known as Kapton; this material is fairly popular for low power applications because it is low cost, withstands high temperatures and is easily handled, in contrast to mica which chips and flakes easily.







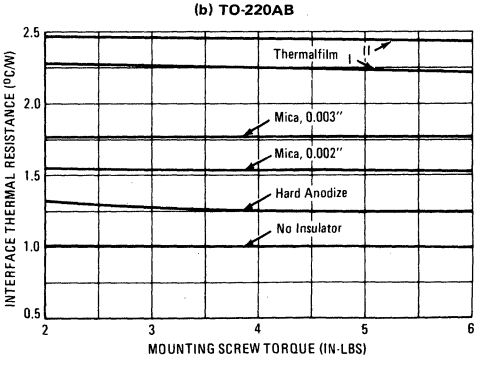


FIGURE 13-3 — INTERFACE THERMAL RESISTANCE WITHOUT THERMAL GREASE AS A FUNCTION OF MOUNTING SCREW TORQUE USING VARIOUS INSULATING MATERIALS

FIGURE 13-4 — INTERFACE THERMAL RESISTANCE USING THERMAL GREASE AS A FUNCTION OF MOUNTING SCREW TORQUE USING VARIOUS INSULATING MATERIALS

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly so that having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the breakdown voltage of the insulation system. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed. In some situations, it may be necessary to substitute "empty" packages for the semiconductor to avoid shorting them or to prevent the semiconductors from limiting the voltage applied during the hi-pot test.

Fastener and Hardware Characteristics

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Washers

A very useful piece of hardware is the bell-type compression washer. As shown in Figure 13-5, it has the ability to maintain a fairly constant pressure over a wide range of physical deflection — generally 20% to 80% — thereby maintaining an optimum force on the package. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package or insulating washer caused by temperature changes. Bell type washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme.

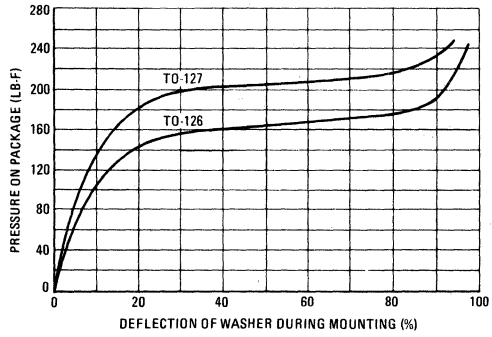


FIGURE 13-5 — CHARACTERISTICS OF THE BELL COMPRESSION WASHERS DESIGNED FOR USE WITH THERMOPAD SEMICONDUCTORS

Motorola washers designed for use with the Thermopad package maintain the proper force when properly secured. They are used with the large face contacting the packages.

Machine Screws

Machine screws and nuts form a trouble-free fastener system for all types of packages which have mounting holes. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of any of the Thermopad plastic package types as the screw heads are not sufficiently flat to provide properly distributed force.

Self-Tapping Screws

Under some conditions, sheet-metal screws are acceptable. However, during the tapping process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; a very unsatisfactory surface results. When used, a speed-nut must be used to secure a standard screw, or the type of screw must be used which roll-forms machine screw threads.

Eyelets

Successful mounting can also be accomplished with hollow eyelets provided an adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Rivets

When a metal flange-mount package is being mounted directly to a heat sink, rivets can be used. Rivets are not a recommended fastener for any of the plastic packages except for the tab-mount type. Aluminum rivets are preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

Insulators and Plastic Hardware

Because of its relatively low cost and low thermal resistance, mica is still widely used to insulate semiconductor packages from heat sinks despite its tendency to chip and flake. It has a further advantage in that it does not creep or flow so that the mounting pressure will not reduce with time in use. Plastic materials, particularly Teflon, will flow. When plastic materials form parts of the fastening system, a compression washer is a valuable addition which assures that the assembly will not loosen with time.

Fastening Techniques

Each of the various types of packages in use requires different fastening techniques. Details pertaining to each type are discussed in the following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heat sinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Manufacturers which provide heat sinks for general use and other associated hardware are listed in Appendix B. Manufacturer's catalogs should be consulted to obtain more detailed information. Motorola also has mounting hardware available for a number of different packages. Consult the Hardware Data Sheet for dimension of the components and part numbers.

Specific fastening techniques are discussed in the remainder of this section for the following categories of semiconductor packages.

1. Flange Mount: TO-204AA (TO-3), TO-204AE, TO-213AA.
2. Plastic Packages: TO-218AC, TO-220AB, TO-225AA, TO-225AB (TO-127).
3. Energy Management Series: Case 346, Case 353.

Flange Mount

Few known mounting difficulties exist with this type of package. The rugged base and distance between dice and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. A typical mounting installation is shown in Figure 13-6. Machine screws, self-tapping screws, eyelets, or rivets may be used to secure the package.

Thermopad: TO-225AA and To-225AB

The Motorola Thermopad plastic power packages have been designed to feature minimum size with no compromise in thermal resistance. This is accomplished by die-bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting, i.e., plastic is molded enveloping the chip but leaving the mounting hole open. The benefits of this construction are obtained at the expense of a requirement that strict attention be paid to the mounting procedure. Success in mounting Thermopad devices depends largely upon using a compression washer which provides a controllable pressure across a

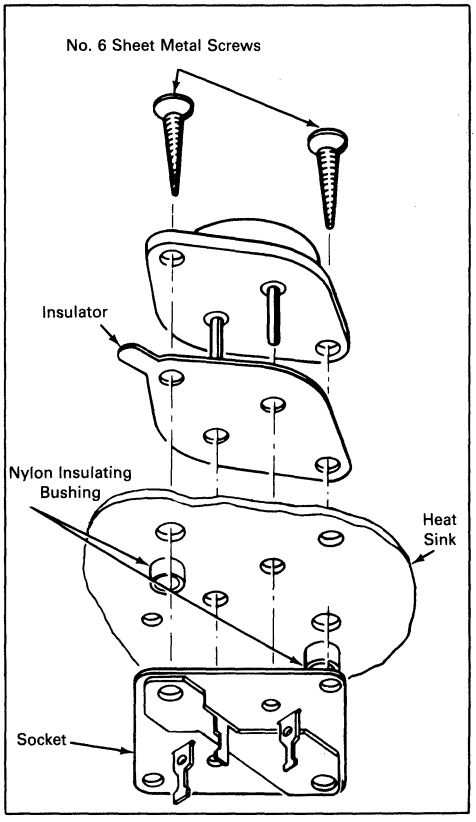


FIGURE 13-6 — MOUNTING DETAILS FOR FLAT-BASE MOUNTED SEMICONDUCTORS (TO-204AA (TO-3) SHOWN).

When not using a socket, maching screws tightened to their torque limits will produce lowest thermal resistance.

large bearing surface. Having a small hole with no chamfer and a flat, burr-free, well-finished heat sink are also important requirements.

Several types of fasteners may be used to secure the Thermopad package; machine screws, eyelets, or clips are preferred. With screws or eyelets, a bell compression washer should be used which applies the proper force to the package over a fairly wide range of deflection. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of the recommended washers are shown in Figure 13-5.

Figure 13-7 shows details of mounting TO-225AA and TO-225AB devices. Use of the clip requires that caution be exercised to insure that adequate mounting force is applied. When electrical isolation is required, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

Thermowatt: TO-220

The popular TO-220 Thermowatt package also requires attention to mounting details. Figure 13-8 shows suggested mounting arrangements and hardware. The rectangular washer shown in Figure 13-8a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque or 8 inch-pounds is suggested when using a 6-32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

In situations where the Thermowatt package is making direct contact with the heat sink, an eyelet may be used, provided sharp blows or impact shock is avoided.

Mounting TO-218AC

Non-isolated and isolated mounting hardware and procedures are shown in Figure 13-9. Generally, the precautions listed for the TO-220AB package are applicable to the TO-218AC package.

Energy Management Series

Recommended mounting procedure and hardware for Case 346-01 and Case 353-01 is shown in Figure 13-10. Although Case 353-01 is smaller than Case 346-01 and requires different hardware, mounting procedure and precautions are similar.

Belleville Washers are recommended under the heads of the heat sink mounting screws for both packages, as shown in Figure 13-10. The screw heads should not contact the plastic surface of the package; they should ride on the Belleville washer to prevent possible case damage. Also, the Belleville washers provide a constant load torque to the package over a broad range of device operating temperature. To utilize the larger power dissipation that these packages can provide, it is essential that a heat sink compound (DC340 or similar) be used and that the case and sink surfaces be flat.

Lead terminal attachment torque should not exceed 20 in-lb for either package. Terminal screws should not penetrate more than 0.50 inch for either package.

By observing these precautions, heat sink mounting should not present any special problems.

Free Air Power Dissipation

Frequently it is asked, "What is the maximum power dissipation capability of a particular semiconductor package without heat sinking?" The question arises more often

for plastic encapsulated packages than for metal ones. Unfortunately, there is no exact maximum power dissipation for any semiconductor package without known heat sinking properties.

Power dissipation capability of a semiconductor is based upon the maximum junction temperature specification. For a silicon die, $T_{J(max)}$ is usually 200°C, when mounted in a metal package, and normally 150°C, when housed in plastic, with the plastic being the limiting factor.

Typical junction-to-ambient ($R_{\theta JA}$) thermal resistance values and the resulting power dissipation capability is shown in Table 3 for some popular package types. These values are typical when there is no heat sink attached to the case. Obviously, electrical connections have to be made to the package and this is one of the several variables.

There are seven factors which determine the power dissipation capability of a given package and they are: Attachment, Power Dissipation, Package Orientation, Still Free Air, Ambient Temperature, Lead Length (if applicable), and $T_{J(max)}$.

One of the chief variables is mounting attachments. For maximum power dissipation, it is helpful if the electrical connection to the terminal which will permit the greatest heat removal be as massive as possible. For a metal package, it would be the case and for a plastic package lead mounted, it would be the drain lead for a power MOSFET.

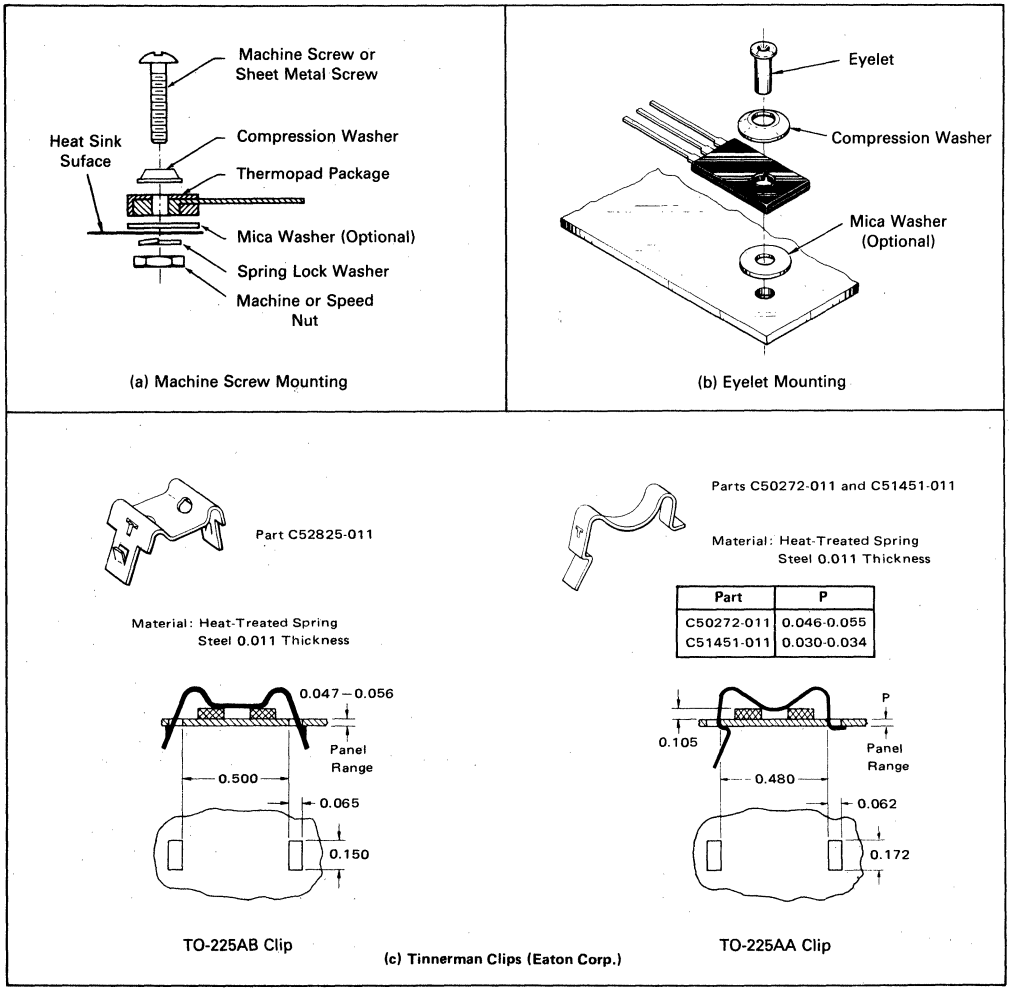


FIGURE 13-7 — RECOMMENDED MOUNTING ARRANGEMENTS FOR TO-225AA (TO-126)

Free Air and Socket Mounting

In applications where average power dissipation is of the order of a watt or so, power semiconductors may be mounted with little or no heat sinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked glass-to-metal seals around the leads. The plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heat sink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance.

In many situations, because its leads are fairly heavy, the TO-225AB package has supported a small heat sink; however, no definitive data is available. When using a small heat sink, it is good practice to have the sink rigidly

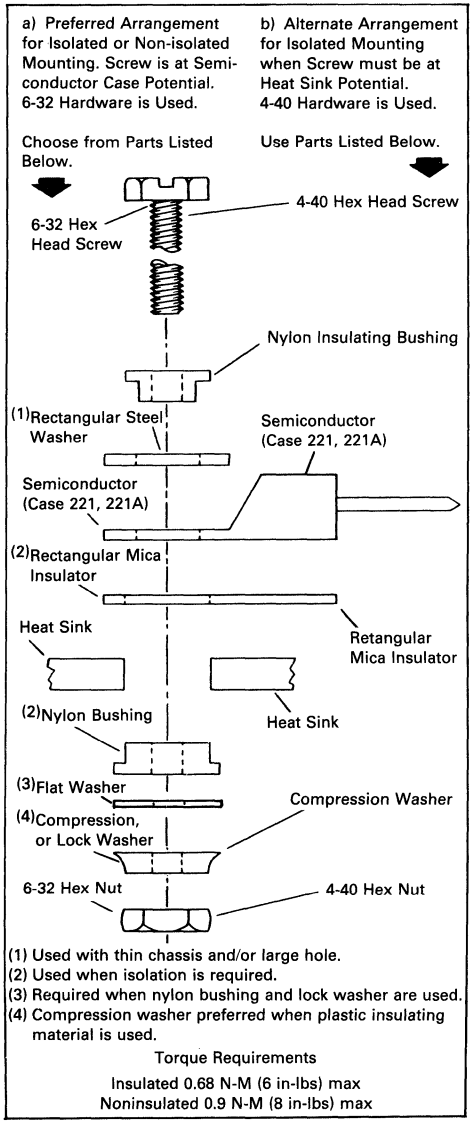


FIGURE 13-8 — MOUNTING ARRANGEMENTS FOR THERMOWATT PACKAGES (TO-220)

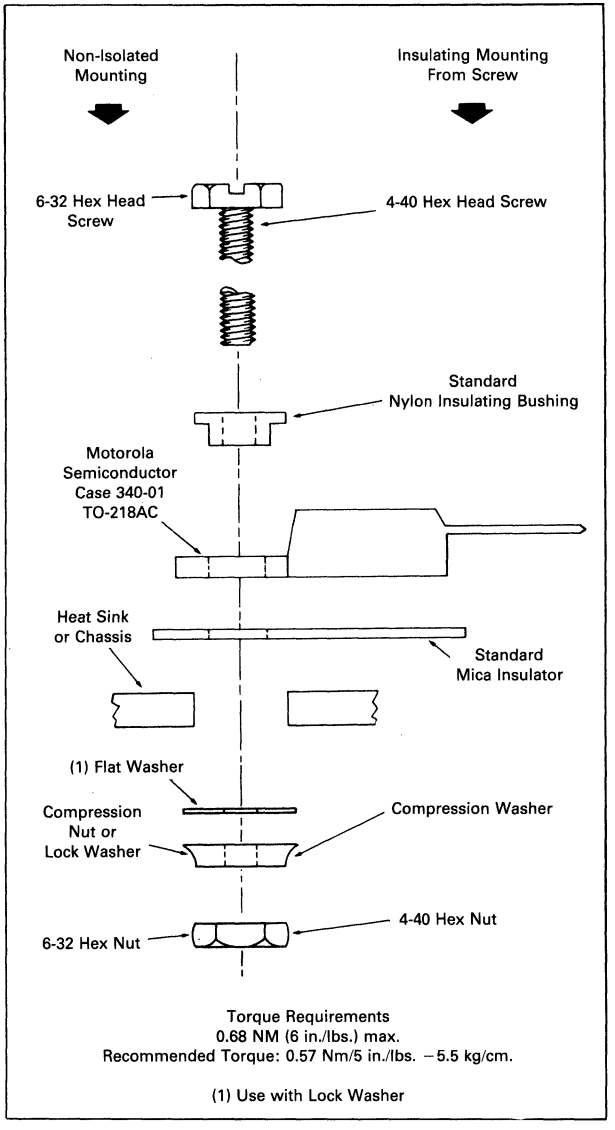


FIGURE 13-9 — MOUNTING METHODS FOR TO-218AC PACKAGE

mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 13-11. The arrangement of part (a) could be used with any plastic package, but the scheme of part (b) is more practical with Case 77. With the other package types, mounting the transistor on top of the heat sink is more practical.

In certain situations, in particular where semiconductor testing is required, sockets are desirable. Manufacturers have provided sockets for all the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details.

Handling Pins, Leads, and Tabs

The pins and lugs of metal-packaged devices are not designed for any bending or stress. If abused, the glass-to-metal seals could crack. Wires may be attached using sockets, crimp connectors, or solder, provided the data sheet ratings are observed.

The leads and tabs of the plastic packages are more flexible and can be reshaped, although this is not a recommended procedure for users to do. In some cases, a heat sink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming options are available from Motorola. Preformed leads remove the risk of device damage caused by bending from the users.

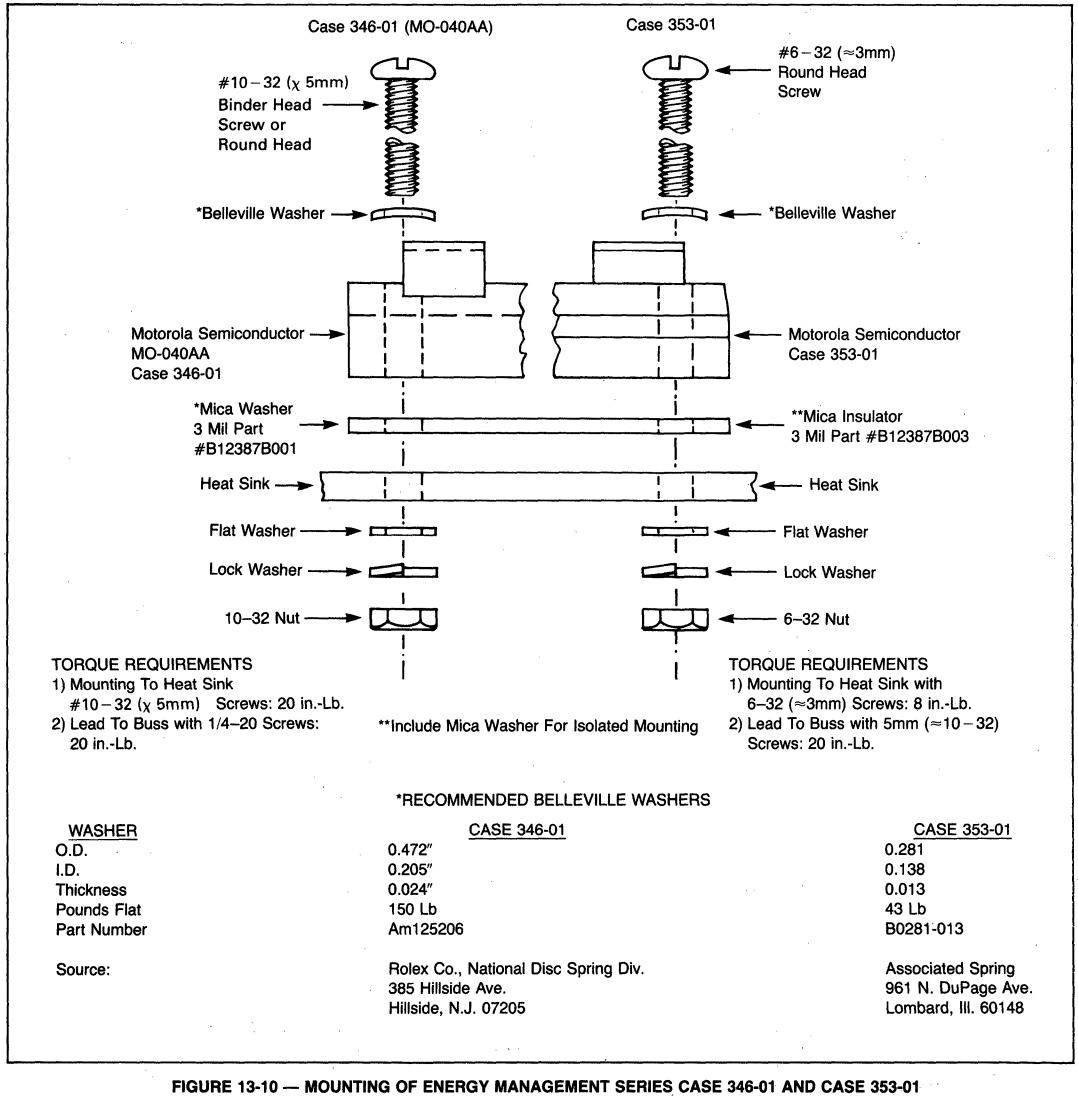


FIGURE 13-10 — MOUNTING OF ENERGY MANAGEMENT SERIES CASE 346-01 AND CASE 353-01

TABLE 3 — Typical Junction-to-Ambient Thermal Resistance and Typical Power Dissipation for Various Transistor Packages Without Heat Sinking

Motorola Case Number	JEDEC Number	Without Heat Sink in Free Air	
		Typical $R_{\theta JA}$ (°C/W)	Typical Power Dissipation (Watts)
1	TO-204AA (TO-3)	50	3.5
77	TO-225AA (TO-126)	83	1.5
80	TO-213AA (TO-66)	60	2.9
197	TO-204AE (TO-3)	50	3.5
221A	TO-220AB	62	2.0
340	TO-218AC	45	2.8

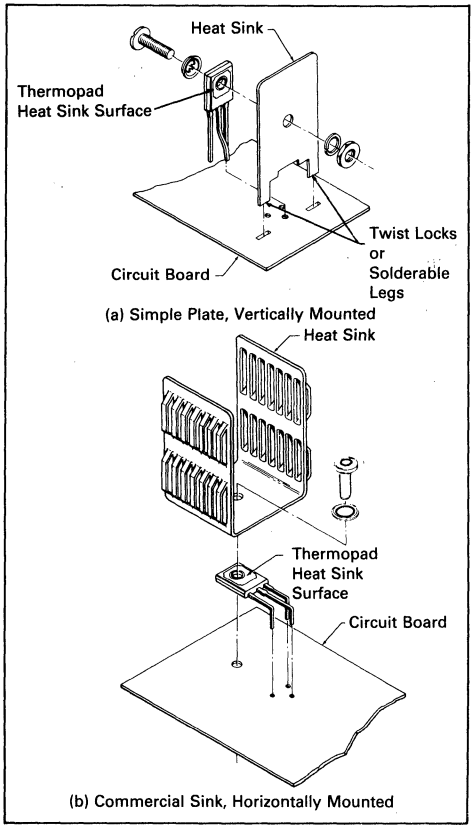


FIGURE 13-11 — METHODS OF USING SMALL HEAT SINKS WITH PLASTIC SEMICONDUCTOR PACKAGES

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A lead-bend radius greater than 1/16 inch is advisable for the TO-225AA and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than four pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. An acceptable lead-forming method that provides this relief is to incorporate an S-bend into the lead. Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than five seconds at a distance greater than 1/8 inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead-to-plastic junctions.

Cleaning Circuit Boards

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices.

Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline may cause the encapsulant to swell, possibly damaging the transistor die. Likewise, chlorinated Freon solvents are unsuitable, since they may cause the outer package to dissolve and swell.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if the packages are free-standing without support.

Thermal System Evaluation

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN-569.

Other applications including switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A) A fine thermocouple should be used, such as #32AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where

T_J = junction temperature (°C)
T_C = case temperature (°C)
$R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet (°C/W)
P_D = power dissipated in the device (W).

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A

THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D),
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that ΔT could be thought of as a voltage; thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where T_J = junction temperature,
P_D = power dissipation,
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heat sink),
$R_{\theta SA}$ = heat sink thermal resistance (heat sink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result. The value for the interface thermal resistance, $R_{\theta CS}$, is affected by the mounting procedure and may be significant compared to the other thermal-resistance terms.

The thermal resistance of the heat sink is not constant; it decreases as ambient temperature increases and is affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. In some applications such as in RF power amplifiers and short-pulse applications, the concept may be invalid because of localized heating in the semiconductor chip.

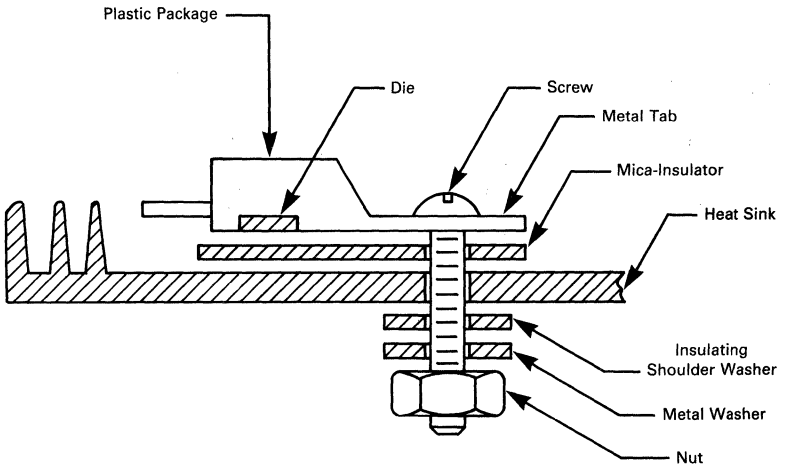


FIGURE A1 — BASIC THERMAL RESISTANCE MODEL SHOWING THERMAL TO ELECTRICAL ANALOGY FOR A SEMICONDUCTOR

APPENDIX B
SOURCES OF ACCESSORIES

		Insulators						Heat Sinks					
Manufacturer	Joint Compound	BeO	$Al0_2$	Anodize	Mica	Plastic Film	Silicone Rubber	Stud	Flange	Disc	Thermowatt	Unit/Duo Watt	RF Stripline
Aavid Eng.	Ther-o-link 1000	—	—	—	—	—	—	X	X	—	X	—	—
AHAM	—	—	—	—	—	—	—	X	X	—	X	—	—
Astrodyne	#829	—	—	—	—	—	—	X	X	X	X	X	—
Delbert Blinn	—	X	—	X	X	X	X	X	X	—	—	—	—
IERC	Thermate	—	—	—	—	—	—	X	X	—	X	X	X
Staver	—	—	—	—	—	—	—	X	X	—	X	X	X
Thermalloy	Thermacote	X	X	X	—	X	—	X	X	X	X	X	X
Tor	TJC	X	—	X	X	X	—	X	X	—	X	—	—
Tran-tec	XL500	X	—	—	—	X	X	X	X	X	X	X	X
Wakefield Eng.	Type 120	X	—	X	—	—	—	X	X	X	X	X	—
Wei Corp.	—	—	—	—	—	—	—	X	X	—	—	—	—

Other sources for Joint Compounds: Dow Corning, Type 340
Emerson & Cuming, Eccoshield — SO (Electrically Conducting)
Emerson & Cuming, Eccotherm — TC-4 (Electrically Insulating)

APPENDIX B

SUPPLIERS ADDRESSES

Aavid Engineering, Inc., 30 Cook Court, Laconia, New Hampshire 03246 (603) 524-4443

AHAM Heat Sinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151

Astrodyne, Inc., 353 Middlesex Avenue, Wilmington, Massachusetts 01887 (617) 272-3850

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91766 (714) 623-1257

Dow Corning, Savage Road Building, Midland, Michigan 48640 (517) 636-8000

Dayton Corporation, Engineered Fasteners Division, Tinnerman Plant, P.O. Box 6688, Cleveland, Ohio 44101 (216) 523-5327

Emerson & Cuming, Inc., Dielectric Materials Division, 869 Washington Street, Canton, Massachusetts 02021 (617) 828-3300

International Electronics Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849-2481

The Staver Company, Inc., 41-51 North Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666-8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321

Tor Corporation, 14715 Arminta Street, Van Nuys, California 91402 (213) 786-6524

Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748

Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900

Wei Corporation, 1405 South Village Way, Santa Ana, California 92705 (614) 834-9333

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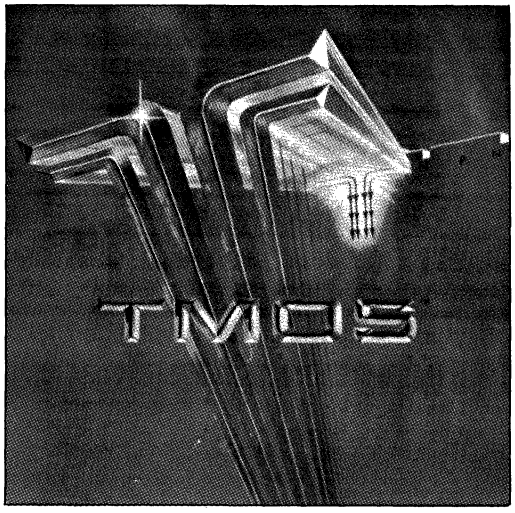
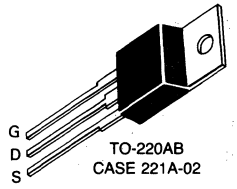


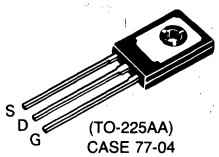
Selector Guide

Table 1 — Plastic TMOS Power MOSFETs



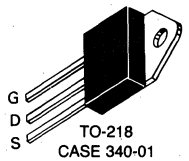
TO-220AB
CASE 221A-02

(MTP and IRF devices in TO-220)



(TO-225AA)
CASE 77-04

(MTA devices are in TO-225AA)



TO-218
CASE 340-01

(MTH devices are in TO-218)

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}@I_D$ (Ohms) Max	Amps	Device	I_{D}Cont Amps Max	P_D @ T_C = 25°C Watts
1000	10	0.5	MTP1N100	1.0	75
950			MTP1N95		
900	8.0	1.0	MTP2N90	2.0	
850			MTP2N85		
600	12	0.5	MTP1N60	1.0	
	2.5	1.5	MTP3N60	3.0	
	1.2	3.0	MTH6N60	6.0	150
550	12	0.5	MTP1N55	1.0	40
	2.5	1.5	MTP3N55	3.0	75
	1.2	3.0	MTH6N55	6.0	150
500	8.0	0.5	MTP1N50	1.0	50
	6.0	1.0	MTP2P50*	2.0	75
	4.0		MTP2N50		
	2.0	1.5	IRF832	4.0	
	1.5		IRF830	4.5	
		2.0	MTP4N50	4.0	
	0.8	3.5	MTH7N50	7.0	150
450	8.0	0.5	MTP1N45	1.0	50
	6.0	1.0	MTP2P45*	2.0	75
	4.0		MTP2N45		
	2.0	2.5	IRF833	4.0	
	1.5		IRF831	4.5	
		2.0	MTP4N45	4.0	
	0.8	3.5	MTH7N45	7.0	150
400	5.0	1.0	MTP2N40	2.0	50
	3.3	1.5	MTP3N40	3.0	75
	1.5	3.0	IRF732	4.5	
	1.0		IRF730	5.5	
		2.5	MTP5N40	5.0	
	0.55	4.0	MTH8N40	8.0	150
350	5.0	1.0	MTP2N35	2.0	50
	3.3	1.5	MTP3N35	3.0	75
	1.5	3.0	IRF733	4.5	
	1.0		IRF731	5.5	
		2.5	MTP5N35	5.0	
	0.55	4.0	MTH8N35	8.0	150
250	0.50	5.0	MTP10N25	10	100
	2.0	1.0	MTP2N25	2.0	50
200	2.4	1.25	IRF612		20
	1.8	1.0	MTP2N20		50
	1.5	1.25	IRF610	2.5	20
	1.2	2.0	MTA4N20	4.0	30
		2.5	IRF622		40
	1.0	2.5	MTP5N20	5.0	75
	0.8		IRF620	5.0	40
	0.7	3.5	MTP7N20	7.0	75
	0.6	5.0	IRF632	8.0	
	0.4		IRF630	9.0	
		4.0	MTP8N20	8.0	
	0.35	6.0	MTP12N20	12	100
	0.22	10	IRF642	16	125
	0.18	10	IRF640	18	
	0.16	7.5	MTH15N20	15	150

*Indicates P-Channel

Table 1 — Plastic TMOS Power MOSFETs
TO-220AB, TO-225AA and TO-218AC (continued)

CASE 221A-02, CASE 77-04 CASE 340-01

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_{DCont} Amps Max	P_D @ T_C = 25°C Watts
180	1.8	1.0	MTP2N18	2.0	50
	1.2	2.0	MTA4N18	4.0	30
	1.0	2.5	MTP5N18	5.0	75
	0.7	3.5	MTP7N18	7.0	
	0.4	4.0	MTP8N18	8.0	
	0.35	6.0	MTP12N18	12	100
	0.16	7.5	MTH15N18	15	150
150	2.4	1.25	IRF613	2.0	20
	1.5		IRF611	2.5	
	1.3	1.5	MTP3N15	3.0	50
	1.2	2.5	IRF623	4.0	40
	0.9		MTA5N15	5.0	30
	0.8		IRF621	4.0	40
	0.7	3.5	MTP7N15	7.0	75
	0.6	5.0	IRF633	8.0	
	0.5	4.0	MTP8N15	8.0	
	0.4	5.0	IRF631	9.0	
	0.3	5.0	MTP10N15	10	
	0.25	7.5	MTP15N15	15	100
	0.22	10	IRF643	16	125
	0.18		IRF641	18	
	0.12		MTH20N15	20	150
120	1.3	1.5	MTP3N12	3.0	50
	1.2	2.5	MTA5N12	5.0	30
	0.7	3.5	MTP7N12	7.0	75
	0.5	4.0	MTP8N12	8.0	
	0.3	5.0	MTP10N12	10	
	0.25	7.5	MTP15N12	15	100
	0.12	10	MTH20N12	20	150
100	0.8	2.0	MTP4N10	4.0	50
			IRF512	3.5	20
	0.6		IRF510	4.0	
		3.0	MTA6N10	6.0	30
	0.5	4.0	MTP8N10	8.0	75
	0.4		MTP8P10*		
			IRF522	7.0	40
	0.33	5.0	MTP10N10	10	75
	0.3	4.0	IRF520	8.0	40
	0.25	8.0	IRF532	12	75
	0.18		IRF530	14	
		6.0	MTP12N10	12	
	0.15	10	MTP20N10	20	100
	0.11	15	IRF542	24	125
	0.085		IRF540	27	
	0.070	12.5	MTH25N10	25	150
80	0.8	2.0	MTP4N08	4.0	50
	0.6	3.0	MTA6N08	6.0	30
	0.5	4.0	MTP8N08	8.0	75
	0.4		MTP8P08*		
	0.33	5.0	MTP10N08	10	
	0.18	6.0	MTP12N08	12	
	0.15	10	MTP20N08	20	100
	0.07	12.5	MTH25N08	25	150

*Indicates P-Channel

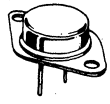
Table 1 — Plastic TMOS Power MOSFETs TO-220AB, TO-225AA and TO-218AC (continued)

CASE 221A-02, CASE 77-04 CASE 340-01

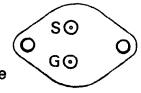
$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_{D}Cont Amps Max	P_D @ T_C = 25°C Watts
60	0.8	2.0	IRF513	3.5	20
	0.6		IRF511	4.0	
		2.5	MTP5N06	5.0	50
	0.4	3.5	MTA7N06	7.0	30
		4.0	IRF523		40
	0.3		IRF521	8.0	
	0.28	5.0	MTP10N06	10	75
	0.25	8.0	IRF533	12	
	0.20	6.0	MTP12N06		
	0.18	8.0	IRF531	14	
	0.16	7.5	MTP15N06	15	
	0.11	15	IRF543	24	125
	0.085		IRF541	27	
	0.08	12.5	MTP25N06	25	100
	0.055	17.5	MTH35N06	35	150
50	0.8	2.5	MTP5N05	5.0	50
	0.4	3.5	MTA7N05	7.0	30
	0.28	5.0	MTP10N05	10	75
	0.20	6.0	MTP12N05	12	
	0.16	7.5	MTP15N05	15	
	0.10	6.0	BUZ10	12	
	0.08	12.5	MTP25N05	25	100
	0.055	17.5	MTH35N05	35	150

Table 2 — Metal TMOS Power MOSFETs TO-204 (Formerly TO-3)

CASE 1-04 and CASE 1-05



Drain connected to case



$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_{D}Cont Amps Max	P_D @ T_C = 25°C Watts
1000	10	0.5	MTM1N100	1.0	75
950			MTM1N95		
900	8.0	1.0	MTM2N90	2.0	
850			MTM2N85		
600	2.5	1.5	MTM3N60	3.0	
	1.2	3.0	MTM6N60	6.0	150
550	2.5	1.5	MTM3N55	3.0	75
	1.2	3.0	MTM6N55	6.0	150
500	6.0	1.0	MTM2P50*	2.0	75
	4.0		MTM2N50		
	2.0	2.5	IRF432	4.0	
	1.5		IRF430	4.5	
		2.0	MTM4N50	4.0	
		3.0	2N6762	4.5	
	0.8	3.5	MTM7N50	7.0	150
	0.4	7.5	MTM15N50	15	250
450	6.0	1.0	MTM2P45*	2.0	75
	4.0		MTM2N45		
	2.0	2.5	IRF433, 2N6761	4.0	
	1.5		IRF431	4.5	
		2.0	MTM4N45	4.0	
	0.8	3.5	MTM7N45	7.0	150
	0.40	7.5	MTM15N45	15	250
400	3.3	1.5	MTM3N40	3.0	75
	1.5	3.0	IRF332	4.5	
	1.0		IRF330	5.5	
		2.5	MTM5N40	5.0	
		3.5	2N6760	5.5	
	0.55	4.0	MTM8N40	8.0	150
	0.30	7.5	MTM15N40	15	250

*Indicates P-Channel

Table 2 — Metal TMOS Power MOSFETs
TO-204 (Formerly TO-3) (continued)

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_{DCont} Amps Max	P_D @ T_C = 25°C Watts
350	3.3	1.5	MTM3N35	3.0	75
	1.5	3.0	IRF333, 2N6759	4.5	
	1.0		IRF331	5.5	
		2.5	MTM5N35	5.0	
	0.55	4.0	MTM8N35	8.0	150
	0.30	7.5	MTM15N35	15	250
250	0.50	5.0	MTM10N25	10	100
200	1.2	2.5	IRF222	4.0	40
	1.0		MTM5N20	5.0	75
	0.8		IRF220		
	0.7	3.5	MTM7N20	7.0	
	0.6	5.0	IRF232	8.0	
	0.4		IRF230	9.0	
		6.0	2N6758		
		4.0	MTM8N20	8.0	
	0.35	6.0	MTM12N20	12	100
	0.22	10	IRF242	16	125
	0.18		IRF240	18	
	0.16	7.5	MTM15N20	15	150
	0.12	16	IRF252	25	
	0.085		IRF250	30	
	0.08	20	MTM40N20	40	250
180	1.0	2.5	MTM5N18	5.0	75
	0.70	3.5	MTM7N18	7.0	
	0.40	4.0	MTM8N18	8.0	
	0.35	6.0	MTM12N18	12	100
	0.16	7.5	MTM15N18	15	150
	0.08	20	MTM40N18	40	250
150	1.2	2.5	IRF223	4.0	40
	0.8		IRF221	5.0	
	0.7	3.5	MTM7N15	7.0	75
	0.6	5.0	2N6757	8.0	
			IRF233		
	0.5	4.0	MTM8N15		
	0.4	5.0	IRF231	9.0	
	0.3		MTM10N15	10	
	0.25	7.5	MTM15N15	15	150
	0.22	10	IRF243	16	125
	0.18		IRF241	18	
	0.12		MTM20N15	20	150
		16	IRF253	25	
	0.085		IRF251	30	
	0.06	22.5	MTM45N15	45	250
120	0.70	3.5	MTM7N12	7.0	75
	0.50	4.0	MTM8N12	8.0	
	0.30	5.0	MTM10N12	10	
	0.25	7.5	MTM15N12	15	150
	0.12	10	MTM20N12	20	
	0.06	22.5	MTM45N12	45	250
100	0.5	4.0	MTM8N10	8.0	75
	0.4		MTM8P10*		
			IRF122	7.0	40
	0.33	5.0	MTM10N10	10	
	0.3	4.0	IRF120	8.0	40
	0.25	8.0	IRF132	12	75
	0.18		IRF130	14	
		6.0	MTM12N10	12	
		9.0	2N6756	14	
	0.15	10	MTM20N10	20	100
	0.11	15	IRF142	24	125
	0.085		IRF140	27	
	0.08	20	IRF152	33	150
	0.07	12.5	MTM25N10	25	
	0.055	20	IRF150	40	
	0.04	27.5	MTM55N10	55	250

*Indicates P-Channel

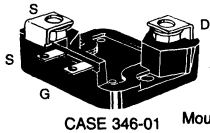
Table 2 — Metal TMOS Power MOSFETs
TO-204 (Formerly TO-3) (continued)

CASE 1-04 and CASE 1-05

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_{DCont} Amps Max	P_D @ T_C = 25°C Watts
80	0.50	4.0	MTM8N08	8.0	75
	0.40		MTM8P08*		
	0.33	5.0	MTM10N08	10	
	0.18	6.0	MTM12N08	12	
	0.15	10	MTM20N08	20	100
	0.07	12.5	MTM25N08	25	150
	0.04	27.5	MTM55N08	55	250
60	0.4	4.0	IRF123	7.0	40
	0.3		IRF121	8.0	
	0.28	5.0	MTM10N06	10	75
	0.25	8.0	IRF133, 2N6755	12	
	0.20	6.0	MTM12N05		
	0.18	8.0	IRF131	14	
	0.16	7.5	MTM15N06	15	
	0.11	15	IRF143	24	125
	0.85		IRF141	27	
	0.08	12.5	MTM25N06	25	100
		20	IRF153	33	150
	0.055	17.5	MTM35N06	35	
		20	IRF151	40	
	0.028	30	MTM60N06	60	250
50	0.28	5.0	MTM10N05	10	75
	0.20	6.0	MTM12N06	12	
	0.16	7.5	MTM15N05	15	
	0.08	12.5	MTM25N05	25	100
	0.055	17.5	MTM35N05	35	150
	0.028	30	MTM60N06	60	250

*Indicates P-Channel

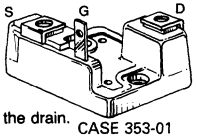
Table 3 — Energy Management Series TMOS Power MOSFETs



$P_D = 500W$

CASE 346-01

Mounting base is connected to the drain.

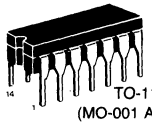


$P_D = 250W$

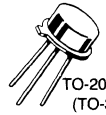
CASE 353-01

V_{DSS} (Volts)	$r_{DS(on)}$ @ I_D (Ohms)	(Amp)	Device	$I_{D(Cont)}$ (Amps)	P_D @ T_C = 25°C (Watts)
200	0.048	30	MTE60N20	60	250
	0.024	60	MTE120N20	120	500
180	0.048	30	MTE60N18	60	250
	0.024	60	MTE120N18	120	500
150	0.038	32.5	MTE65N15	65	250
	0.020	65	MTE130N15	130	500
120	0.038	32.5	MTE65N12	65	250
	0.020	65	MTE130N12	130	500
100	0.028	37.5	MTE75N10	75	250
	0.012	75	MTE150N10	150	500
80	0.028	37.5	MTE75N08	75	250
	0.012	75	MTE150N08	150	500
60	0.018	50	MTE100N06	100	250
	0.009	100	MTE200N06	200	500
50	0.018	50	MTE100N05	100	250
	0.009	100	MTE200N05	200	500

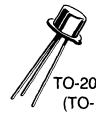
Table 4 — TMOS Small-Signal MOSFETs



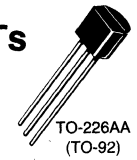
TO-116 (MO-001 AA)



TO-205AD (TO-39)



TO-206AA (TO-18)



TO-226AA (TO-92)

TO-226AE

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_{D}Cont Amps Max	P_D @ T_C = 25°C Watts	Package
200	14	0.2	BS107	0.25	0.6	TO-226AA (TO-92)
	6.0	0.1	MPF9200	0.40		
			MFE9200		1.8	TO-206AA (TO-18)
	5.0	0.2	BS170	0.50	0.6	TO-226AA (TO-92)
90	5.0	1.0	VN90AB	2.0	6.25	TO-205AD
	4.5		VN99AB			(TO-39)
	4.0		MPF6661		2.5	TO-226AE
			2N6661		6.25	TO-205AD (TO-39)
	2.0		MPF990		2.5	TO-226AE
			MFE990		6.25	TO-205AD (TO-39)
			MFQ990C		4.0	TO-116
60	5.0	0.5	MPF910/MPF10LM	0.5	2.5	TO-226AE
			MFE910		6.25	TO-205AD
		0.3	VN67AB			(TO-39)
	3.0	1.0	MPF6660	2.0	2.5	TO-226AE
			2N6660		6.25	TO-205AD (TO-39)
	1.7		MPF960		2.5	TO-226AE
			MFE960		6.25	TO-205AD (TO-39)
			MFQ960C		4.0	TO-116
35	2.5		VN35AB		6.25	TO-205AD (TO-39)
	1.4		MPF930		2.5	TO-226AB
			MFE930		6.25	TO-205AD (TO-39)
			MFQ930C		4.0	TO-116

Table 5 — TMOS Product Matrix

I_D (AMP) / $V_{(BR)DSS}$ Volts	≤1	2–2.9	3–3.9	4–5	5–6	7	8	9–10	12–13	14–19	20–24	25–29	30–40	50–75	100–200
1000 950	MTM/MTP 1N100/95		MTM 3N10/95	MTM 4N100/95											
900 850		MTM/MTP 2N90/85		MTM 4N90/85	MTM 5N90/85										
600 550	MTP 1N60/55	MTM/MTP 2N60/55	MTM/MTP 3N60/55		MTM/MTH 6N60/55		MTM 8N60/55				MTE 20N60/55		MTE 40N60/55		
500 450	MTP 1N50/45	MTM/MTP 2N50/45 MTM/MTP 2P50/45		MTM/MTP 4N50/45 2N6761 2N6762 IRF430-33 IRF830-33		MTM/MTH 7N50/45	IRF440 IRF441 IRF740 IRF741	MTM/MTH 10N50/45	IRF450 IRF451	MTM15N 50/45		MTE 25N50/45		MTE 50N50/45	
400 350		MTP 2N40/35	MTM/MTP 3N40/45	2N6759	MTM/MTP 5N40/35 2N6760 IRF330-33 IRF730-33		MTM/MTH 8N40/35		MTM/MTH 12N40/35	MTM 15N40/35 IRF350 IRF351			MTE 30N40/35	MTE 60N40/35	
250 180	MFE9200 MPF9200 BS170 BS107	MTP 2N20/18 MTP 2N25 IRF610-12		IRF222 IRF622 MTA 4N18/20 IRF220 IRF620	MTM/MTP 5N20/18	MTM/MTP 7N20/18	MTM/MTP 8N20/18 IRF232 IRF632	MTM/MTP 10N25 2N6758 IRF230 IRF630	MTM/MTP 12N20/18	IRF240,640 MTM 15N20/18 IRF242,642 MTH 15N20/18		IRF252	IRF250 MTM 40N20/18 MTH 30N20/18	MTE 60N20/18	MTE 120N20/18
150 120		IRF611-13	MTP 3N15/12	IRF223,623 MTA 5N12/15 IRF221 IRF621	IRF221 IRF621	MTM/MTP 7N15/12	IRF233 IRF633 2N6757 MTM/MTP 8N12/15	MTM/MTP 10N15/12 IRF231 IRF631 2N6757		MTM/MTP 15N15/12 IRF241,641 IRF243,643	MTM/MTH 20N15/12	IRF253	IRF251 MTM 45N15/12 MTH 35N15/20	MTE 65N15/12	MTE 130N15/12
100 80		2N6661 MPF6661 MPF990 MFE990 MFQ990C	IRF512	MTP 4N10/08 IRF510	MTA 6N08/10	IRF122 IRF522	MTM/MTP 8N10/08 MTM/MTP 8P10/08 IRF120 IRF520	MTM/MTP 10N10/08	MTM/MTP 12N10/08 IRF132 IRF532	2N6756 IRF130 IRF530	MTM/MTP 20N10/08 IRF142 IRF542	MTM 25N10/08 MTH 25N10/08 IRF140 IRF540	IRF150,152 MTH40N 10/08	MTE 75N10/08 MTM 55N10/08	150N10/08
60 50	MFE910 MPF910	2N6660 MPF6660 MFE960 MPF960 MFQ960	IRF513	IRF511	MTP 5N06/05	IRF123 IRF523 MTA 7N05/06	IRF121 IRF521	MTM/MTP 10N06/05	MTM/MTP 12N06/05 2N6755 IRF133 IRF533 BUZ10	MTM/MTP 15N06/05 IRF131 IRF531	IRF143 IRF543	MTM/MTP 25N06/05 IRF141 IRF541	MTM/MTP 35N06/05 IRF151 IRF153 MTH 40N06/05	MTM 60N06/05	MTE 100N06/05 MTE 200N06/05

MTM Prefix — TO-204
MTP Prefx — TO-220AB
MTH Prefix — TO-218AC
MTA Prefix — TO-225AA

MFE Prefix — TO-205AD (TO-39)
MPF Prefix — TO-226AA (TO-92)
MFQ Prefix — TO-116
MTE Prefix — Case 346 or 353

IRF100 thru 400 Series — TO-204
IRF500 thru 800 Series — TO-220AB

Devices in the shaded area will be introduced in 1984.

Power Data Sheets

C

Data sheets are arranged in alphanumeric sequence except when information applies to more than one device, e.g., MTM10N08, MTM10N10, MTP10N08 and MTP10N10. Consult the table of contents for these part numbers.

2N6755
2N6756

MOTOROLA

C

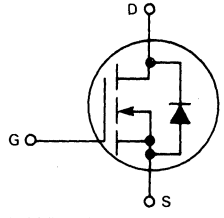
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

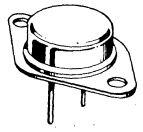
TMOS™



12 and 14 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.25 OHM
60 VOLTS
$r_{DS(on)}$ = 0.18 OHM
100 VOLTS



MAXIMUM RATINGS

Rating	Symbol	2N6755	2N6756	Unit
Drain-Source Voltage	V_{DSS}	60*	100*	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60*	100*	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current				Adc
Continuous T_C = 25°C	I_D	12.0*	14*	
T_C = 100°C	I_D	8.0*	9.0*	
Pulsed	I_{DM}	25*	30*	
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C	P_D	75*		Watts
Derate above 25°C		0.6*		W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55* to 150*		°C

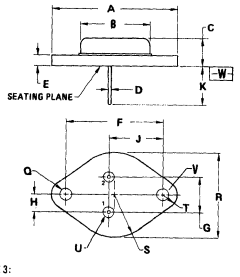
THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67*	
Junction to Ambient	$R_{\theta JA}$	30*	
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for seconds	T_L	300*	°C

*JEDEC Registered Values

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ ⌀ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ ⌀ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA
(TO-3 TYPE)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1.0 mA)	2N6755	$V_{BR(DSS)}$	60	—	—	Vdc
	2N6756		100	—	—	
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS})		I_{DSS}	—	—	1.0*	mAdc
T_J = 125°C			—	—	4.0*	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 V)		I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 V)		I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0*	—	4.0*	Vdc
T_J = 100°C			1.5	—	3.5	
Static Drain-Source On-Resistance (1)		$r_{DS(on)}$				Ohms
(V_{GS} = 10 Vdc, I_D = 8.0 Adc)	2N6755		—	—	0.25*	
T_C = 125°C			—	—	0.45*	
(V_{GS} = 10 Vdc, I_D = 9.0 Adc)	2N6756		—	—	0.18*	
T_C = 125°C			—	—	0.33*	
Drain-Source On-Voltage (V_{GS} = 10 V) (1)		$V_{DS(on)}$				Vdc
(I_D = 12 Adc)	2N6755		—	—	3.0*	
(I_D = 14 Adc)	2N6756		—	—	2.52*	
Forward Transconductance (1) (V_{DS} = 15 V, I_D = 9.0 A)		g_{fs}	4.0*	—	12.0*	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	350*	—	800*	pF
Output Capacitance		C_{oss}	150*	—	500*	
Reverse Transfer Capacitance		C_{rss}	50*	—	150*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} = 36 V, I_D = 9.0 Adc Z_o = 15 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	30*	ns
Rise Time		t_r	—	—	75*	
Turn-Off Delay Time		$t_{d(off)}$	—	—	40*	
Fall Time		t_f	—	—	45*	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0)		V_F				Vdc
I_S = 12 A	2N6755		0.85*	—	1.7*	
I_S = 14 A	2N6756		0.90*	—	1.8*	
Continuous Source Current, Body Diode	2N6755	I_S	—	—	12*	Adc
	2N6756		—	—	14*	
Pulsed Source Current, Body Diode	2N6755	I_{SM}	—	—	25	A
	2N6756		—	—	30	
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	250	—	ns
Reverse Recovery Time		t_{rr}	—	325	—	

*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

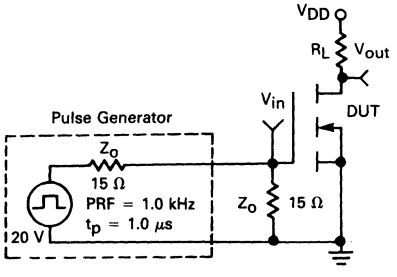
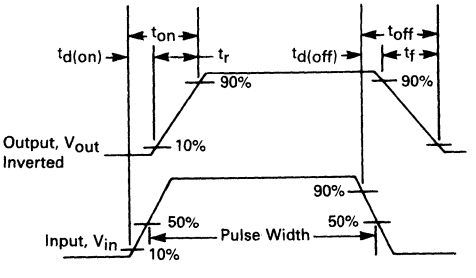


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — ON-REGION CHARACTERISTICS

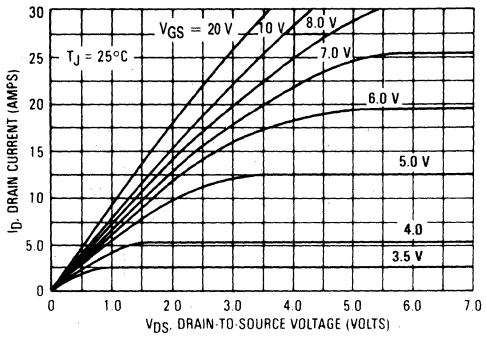


FIGURE 4 — ON-RESISTANCE VARIATION

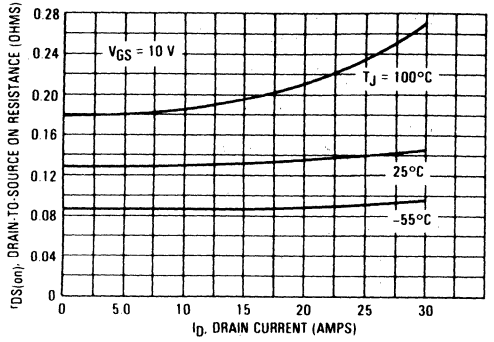


FIGURE 5 — TRANSFER CHARACTERISTICS

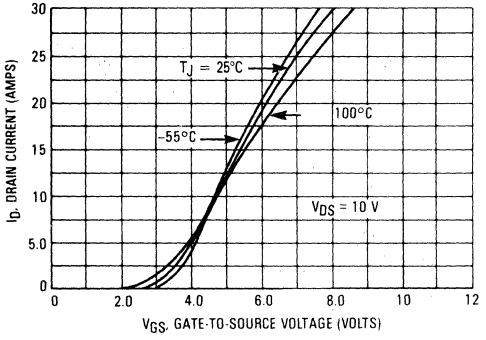


FIGURE 6 — GATE THRESHOLD VOLTAGE VARIATION

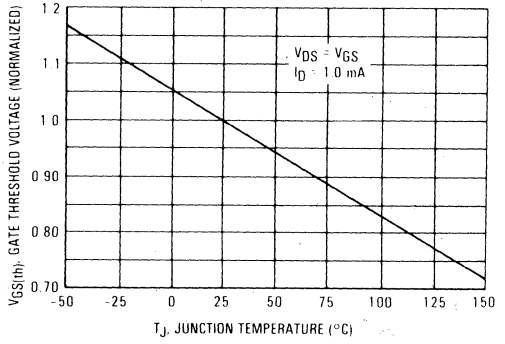
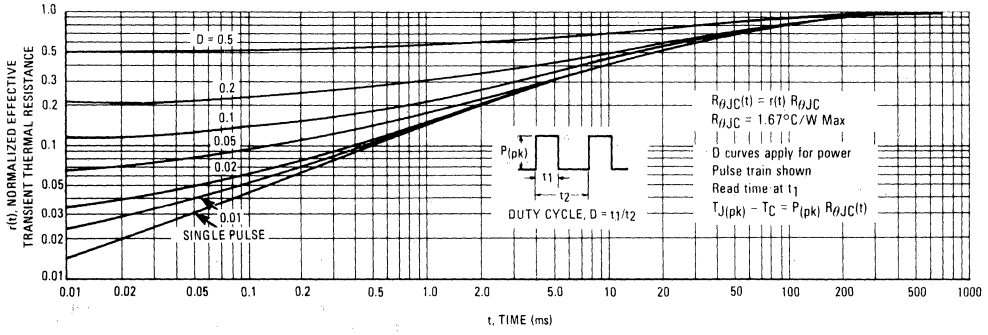


FIGURE 7 — THERMAL RESPONSE



OPERATING AREA INFORMATION

FIGURE 8 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6755

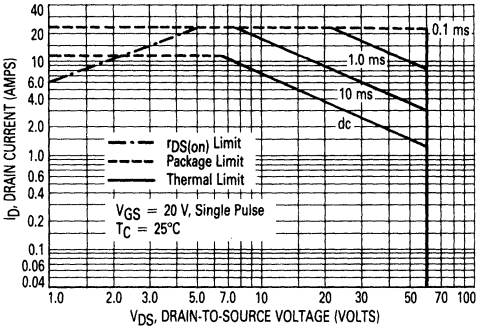


FIGURE 9 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

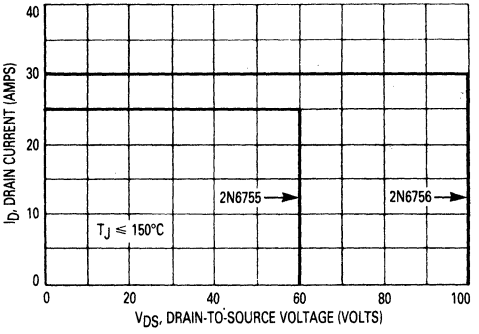
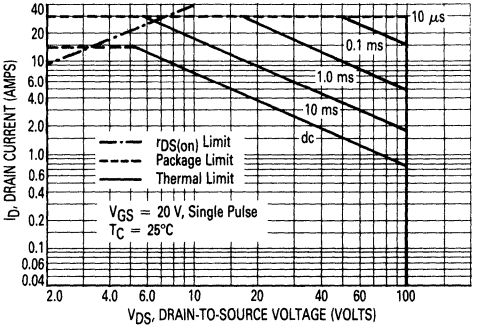


FIGURE 10 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6756



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 8 and 10 are based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figure or
T_{Jmax} = Rated maximum junction temperature
T_C = Device case temperature
P_D = Rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = Rated steady state thermal resistance
r(t) = Normalized thermal response from Figure 7.

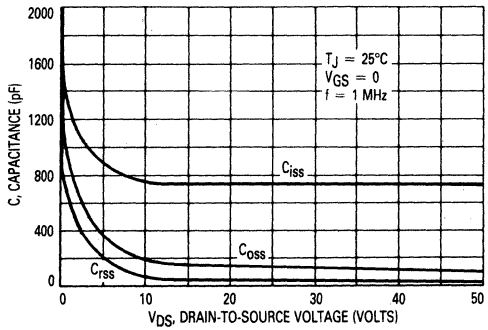
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

FIGURE 11 — CAPACITANCE VARIATION



2N6757
2N6758

MOTOROLA

C

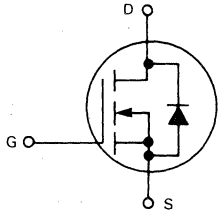
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

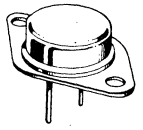
TMOS™



8.0 and 9.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.6 OHM
150 VOLTS
$r_{DS(on)}$ = 0.4 OHM
200 VOLTS



MAXIMUM RATINGS

Rating	Symbol	2N6757	2N6758	Unit
Drain-Source Voltage	V_{DSS}	150*	200*	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	150*	200*	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous T_C = 25°C T_C = 100°C Pulsed	 I_D I_{DM}	 8.0* 5.0* 12.0*	 9.0* 6.0* 15.0*	Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75* 0.6*		Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55* to 150*		°C

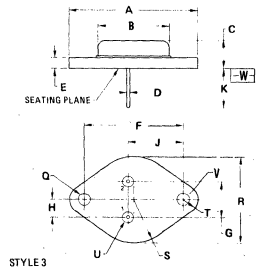
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for seconds	T_L	300*	°C

*JEDEC Registered Values

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ ⌀ 0.25 (0.010) Ⓜ W V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ ⌀ 0.30 (0.012) Ⓜ W V Ⓜ Q Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA
(TO-3 TYPE)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1.0 mA)	2N6757	$V_{BR(DSS)}$	150	—	—	Vdc
	2N6758		200	—	—	
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS})		I_{DSS}	—	—	1.0*	mAdc
T_J = 125°C			—	—	4.0*	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 V)		I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 V)		I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0*	—	4.0*	Vdc
T_J = 100°C			1.5	—	3.5	
Static Drain-Source On-Resistance (1) (V_{GS} = 10 Vdc, I_D = 5.0 Adc)	2N6757	$r_{DS(on)}$	—	—	0.6*	Ohms
T_C = 125°C			—	—	1.13*	
(V_{GS} = 10 Vdc, I_D = 6.0 Adc)	2N6758		—	—	0.4*	
T_C = 125°C			—	—	0.75*	
Drain-Source On-Voltage (V_{GS} = 10 V) (1) (I_D = 8.0 Adc)	2N6757	$V_{DS(on)}$	—	—	4.8*	Vdc
(I_D = 9.0 Adc)	2N6758		—	—	3.6*	
Forward Transconductance (1) (V_{DS} = 15 V, I_D = 6.0 A)		g_{fs}	3.0*	—	9.0*	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	350*	—	800*	pF
Output Capacitance		C_{oss}	100*	—	450*	
Reverse Transfer Capacitance		C_{rss}	40*	—	150*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} = 175 V, I_D = 3.5 Adc Z_o = 15 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	30*	ns
Rise Time		t_r	—	—	50*	
Turn-Off Delay Time		$t_{d(off)}$	—	—	50*	
Fall Time		t_f	—	—	40*	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0)		V_F				Vdc
I_S = 8.0 A	2N6757		0.75*	—	1.50*	
I_S = 9.0 A	2N6758		0.8*	—	1.60*	
Continuous Source Current, Body Diode	2N6757	I_S	—	—	8.0*	Adc
	2N6758		—	—	9.0*	
Pulsed Source Current, Body Diode	2N6757	I_{SM}	—	—	12	A
	2N6758		—	—	15	
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	250	—	ns
Reverse Recovery Time		t_{rr}	—	325	—	

*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

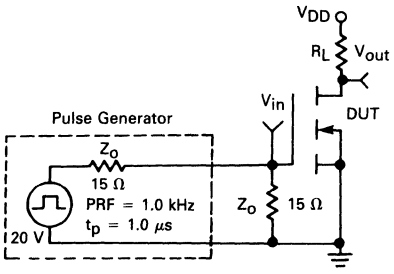
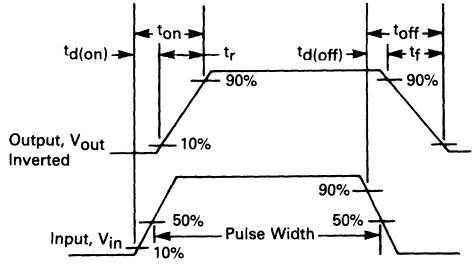


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — ON-REGION CHARACTERISTICS

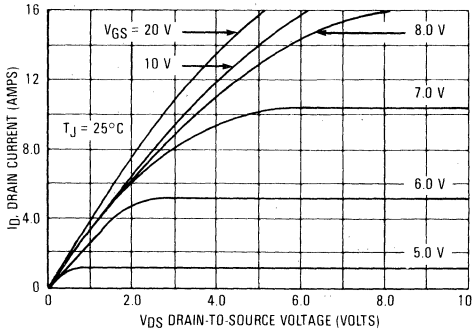


FIGURE 4 — ON-RESISTANCE VARIATION

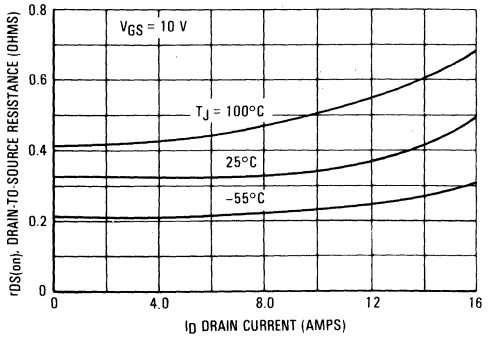


FIGURE 5 — TRANSFER CHARACTERISTICS

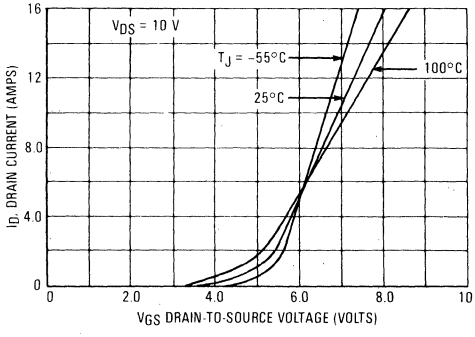


FIGURE 6 — GATE THRESHOLD VOLTAGE VARIATION

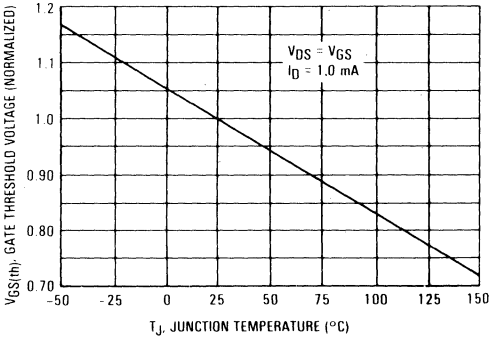
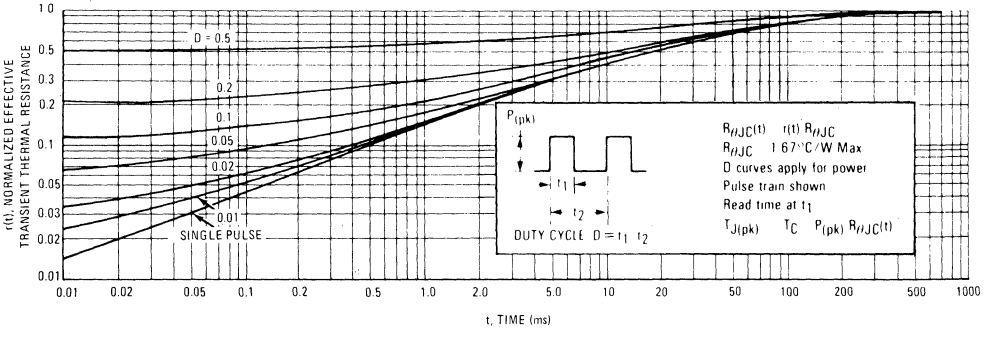


FIGURE 7 — THERMAL RESPONSE



OPERATING AREA INFORMATION

FIGURE 8 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6757

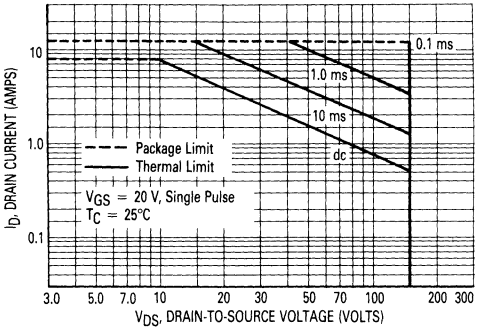


FIGURE 9 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

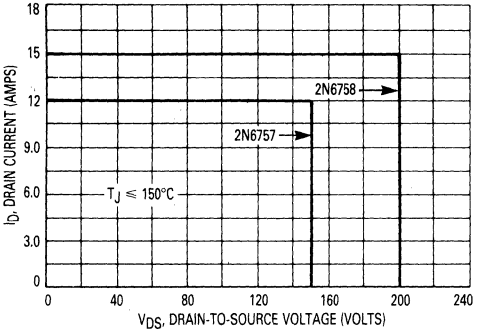
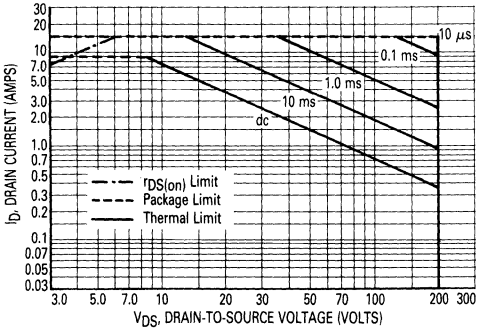


FIGURE 10 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6758



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 8 and 10 are based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figure or
T_{Jmax} = Rated maximum junction temperature
T_C = Device case temperature
P_D = Rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = Rated steady state thermal resistance
r(t) = Normalized thermal response from Figure 7.

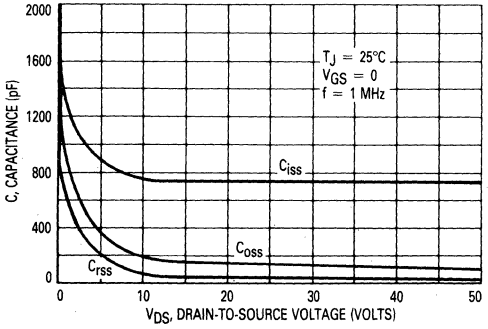
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

FIGURE 11 — CAPACITANCE VARIATION



2N6759
2N6760

MOTOROLA

C

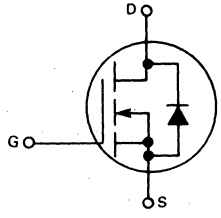
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

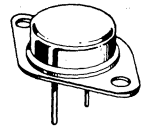


4.5 and 5.5 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 1.5 OHM
350 VOLTS

$r_{DS(on)}$ = 1.0 OHM
400 VOLTS



MAXIMUM RATINGS

Rating	Symbol	2N6759	2N6760	Unit
Drain-Source Voltage	V_{DSS}	350*	400*	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	350*	400*	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current				Adc
Continuous T_C = 25°C	I_D	4.5*	5.5*	
Continuous T_C = 100°C		3.0*	3.5*	
Pulsed	I_{DM}	7.0	8.0	
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C	P_D	75*		Watts
Derate above 25°C		0.6*		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55* to 150*		°C

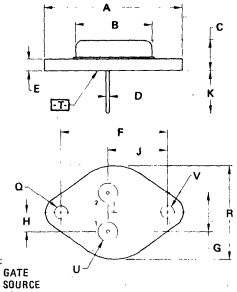
THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67*	
Junction to Ambient	$R_{\theta JA}$	30*	
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for seconds	T_L	300*	°C

*JEDEC Registered Values

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ⌀.13 (0.005) M | T | V M
   FOR LEADS:
   ⌖ | ⌀.13 (0.005) M T | V M | Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(TO-3 TYPE)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1.0 mA)	2N6759	$V_{BR(DSS)}$	350	—	—	Vdc
	2N6760		400	—	—	
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, I_D = 1.0 mA)		I_{DSS}	—	—	1.0*	mAdc
T_J = 125°C			—	—	4.0*	
Gate-Body Leakage Current, Forward (V_{GSF} = 20V)		I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20V)		I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0*	—	4.0*	Vdc
T_J = 100°C			1.5	—	3.5	
Static Drain-Source On-Resistance (1)		$r_{DS(on)}$				Ohms
(V_{GS} = 10 Vdc, I_D = 3.0 Adc)	2N6759		—	—	1.5*	
T_C = 125°C			—	—	3.3*	
(V_{GS} = 10 Vdc, I_D = 3.5 Adc)	2N6760		—	—	1.0*	
T_C = 125°C			—	—	2.2*	
Drain-Source On-Voltage (V_{GS} = 10 V) (1)		$V_{DS(on)}$				Vdc
(I_D = 4.5 Adc)	2N6759		—	—	7.0*	
(I_D = 5.5 Adc)	2N6760		—	—	6.7*	
Forward Transconductance (1) (V_{DS} = 15 V, I_D = 3.5 A)		g_{fs}	3.0*	—	9.0*	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	350*	—	800*	pF
Output Capacitance		C_{oss}	50*	—	300*	
Reverse Transfer Capacitance		C_{rss}	20*	—	80*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} = 175 V, I_D = 3.5 Adc Z_o = 15 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	30*	ns
Rise Time		t_r	—	—	35*	
Turn-Off Delay Time		$t_{d(off)}$	—	—	55*	
Fall Time		t_f	—	—	35*	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0)		V_{SD}				Vdc
I_S = 4.5 A	2N6759		0.70*	—	1.40*	
I_S = 5.5 A	2N6760		0.75*	—	1.50*	
Continuous Source Current, Body Diode		I_S				Adc
	2N6759		—	—	4.5*	
	2N6760		—	—	5.5*	
Pulsed Source Current, Body Diode	2N6759	I_{SM}	—	—	7.0	A
	2N6760		—	—	8.0	
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	250	—	ns
Reverse Recovery Time		t_{rr}	—	420	—	

*JEDEC registered values. (1) Pulse Test = Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

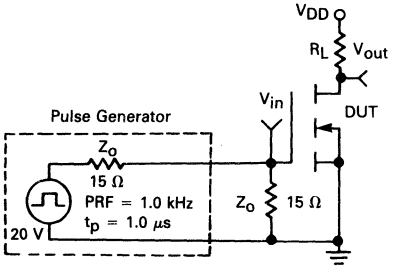
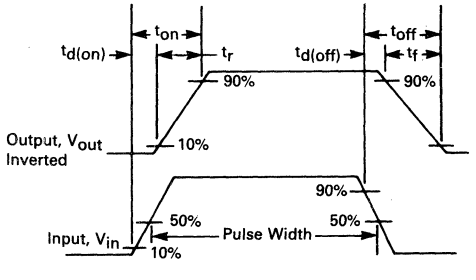


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — ON-REGION CHARACTERISTICS

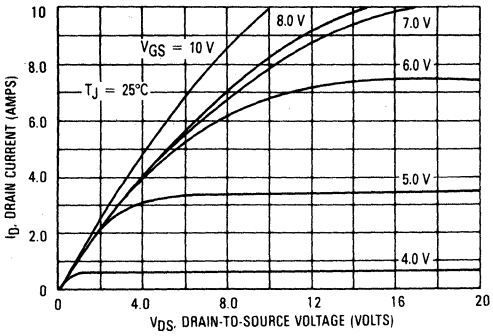


FIGURE 4 — ON-RESISTANCE VARIATION

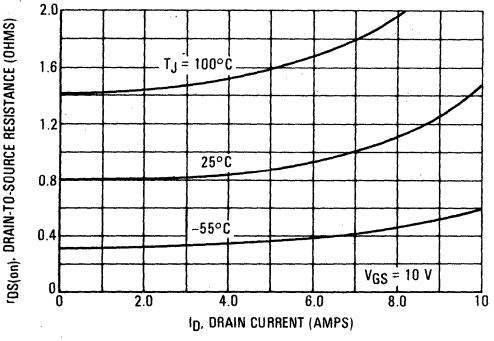


FIGURE 5 — TRANSFER CHARACTERISTICS

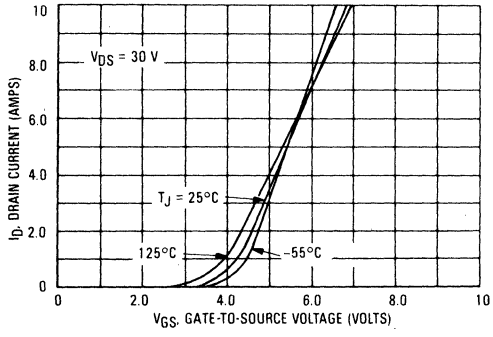


FIGURE 6 — GATE-THRESHOLD VOLTAGE VARIATION

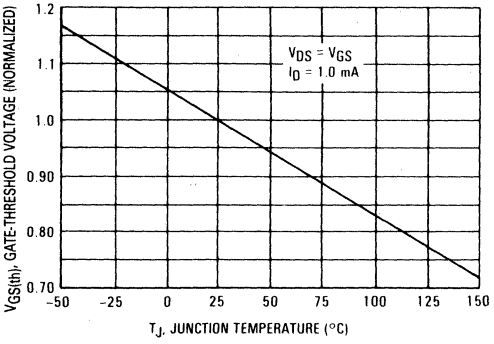
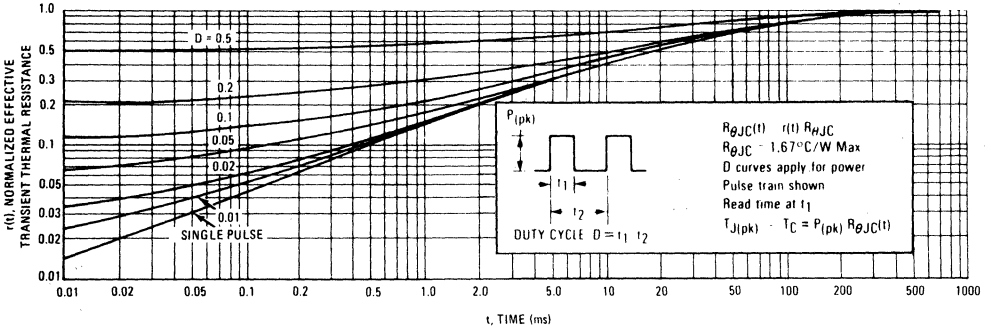


FIGURE 7 — THERMAL RESPONSE



OPERATING AREA INFORMATION

FIGURE 8 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6759

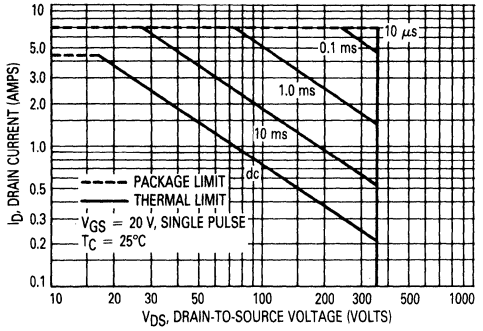


FIGURE 9 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

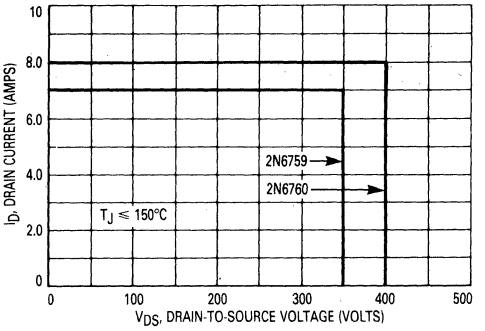
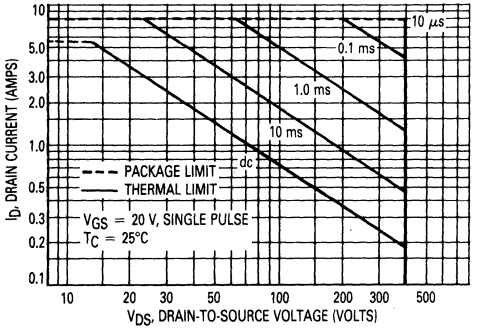


FIGURE 10 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6760



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 8 and 10 are based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

$I_{D\ (25°C)}$ = dc drain current at T_C = 25°C from Figure or

T_{Jmax} = Rated maximum junction temperature

T_C = Device case temperature

P_D = Rated power dissipation at T_C = 25°C

$R_{\theta JC}$ = Rated steady state thermal resistance

r(t) = Normalized thermal response from Figure 7.

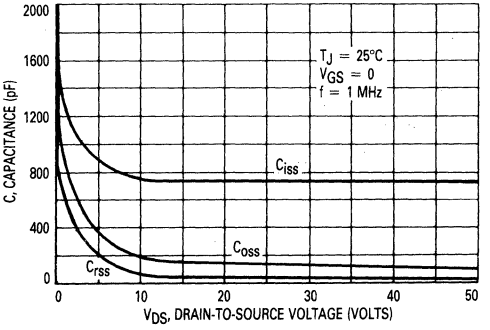
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

FIGURE 11 — CAPACITANCE VARIATION



2N6761
2N6762

MOTOROLA

C

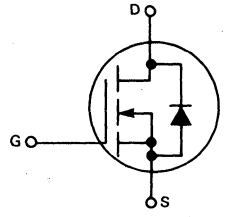
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

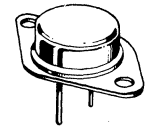
TMOS™



4.0 and 4.5 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 2.0 OHMS
450 VOLTS
$r_{DS(on)}$ = 1.5 OHMS
500 VOLTS



MAXIMUM RATINGS

Rating	Symbol	2N6761	2N6762	Unit
Drain-Source Voltage	V_{DSS}	450*	500*	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	450*	500*	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current				Adc
Continuous T_C = 25°C	I_D	4.0*	4.5*	
T_C = 100°C	I_D	2.5*	3.0*	
Pulsed	I_{DM}	6.0	7.0	
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C	P_D	75*		Watts
Derate above 25°C		0.6*		W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55* to 150*		°C

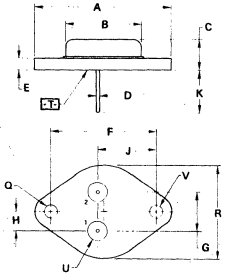
THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67*	
Junction to Ambient	$R_{\theta JA}$	30*	
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for seconds	T_L	300*	°C

*JEDEC Registered Values

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ϕ0.13 (0.005) M | T | V M
   FOR LEADS:
   ⌖ | ϕ0.13 (0.005) M T | V M | Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(TO-3 TYPE)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 4.0 mA)	2N6761	$V_{BR(DSS)}$	450	—	—	Vdc
	2N6762		500	—	—	
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, I_D = 1.0 mA)		I_{DSS}	—	—	1.0*	mAdc
T_J = 125°C			—	—	4.0*	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc)		I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc)		I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0*	2.7	4.0*	Vdc
T_J = 100°C			1.5	2.2	3.5	
Static Drain-Source On-Resistance (1)		$r_{DS(on)}$				Ohms
(V_{GS} = 10 Vdc, I_D = 2.5 Adc)	2N6761		—	—	2.0*	
T_C = 125°C			—	—	4.4*	
(V_{GS} = 10 Vdc, I_D = 3.0 Adc)	2N6762		—	—	1.5*	
T_C = 125°C			—	—	3.3*	
Drain-Source On-Voltage (V_{GS} = 10 V) (1)		$V_{DS(on)}$				Vdc
(I_D = 4.0 Adc)	2N6761		—	—	8.0*	
(I_D = 4.5 Adc)	2N6762		—	—	7.7*	
Forward Transconductance (1) (V_{DS} = 15 V, I_D = 3.0 A)		g_{fs}	2.5*	—	7.5*	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	350*	—	800*	pF
Output Capacitance		C_{oss}	25*	—	200*	
Reverse Transfer Capacitance		C_{rss}	15*	—	60*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} = 225 V, I_D = 3.0 Adc Z_o = 15 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	30*	ns
Rise Time		t_r	—	—	30*	
Turn-Off Delay Time		$t_{d(off)}$	—	—	55*	
Fall Time		t_f	—	—	30*	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0)		V_{SD}				Vdc
I_S = 4.0 A	2N6761		0.65*	1.10	1.3*	
I_S = 4.5 A	2N6762		0.70*	1.15	1.4*	
Continuous Source Current, Body Diode	2N6761	I_S	—	—	4.0*	Adc
	2N6762		—	—	4.5*	
Pulsed Source Current, Body Diode	2N6761	I_{SM}	—	—	6.0	A
	2N6762		—	—	7.0	
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	250	—	ns
Reverse Recovery Time		t_{rr}	—	420	—	

*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

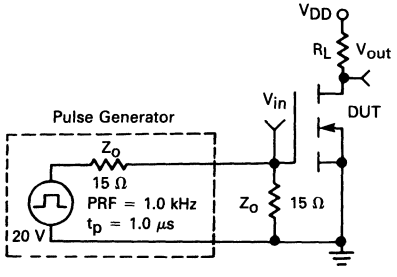
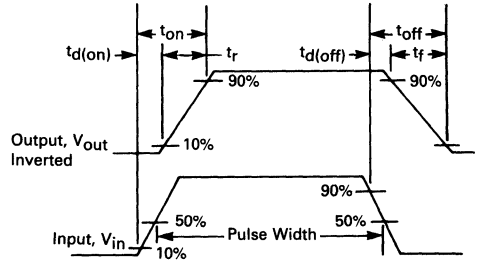


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — ON-REGION CHARACTERISTICS

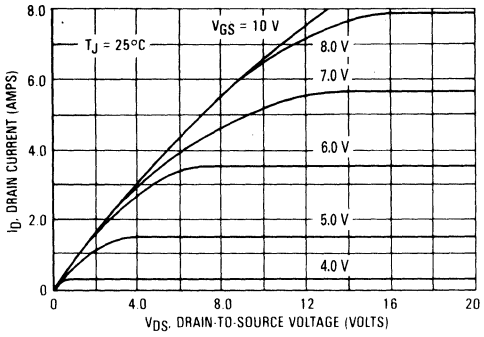


FIGURE 4 — ON-RESISTANCE VARIATION

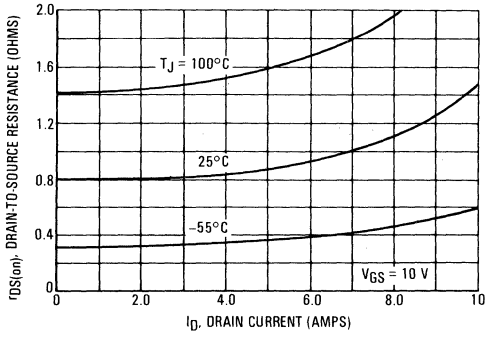


FIGURE 5 — TRANSFER CHARACTERISTICS

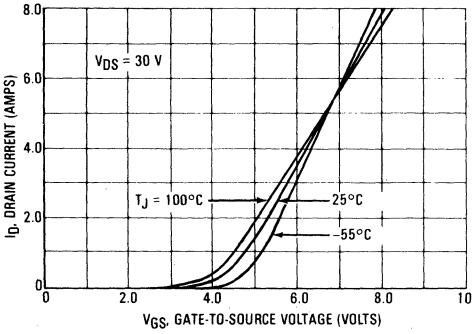


FIGURE 6 — GATE THRESHOLD VOLTAGE VARIATION

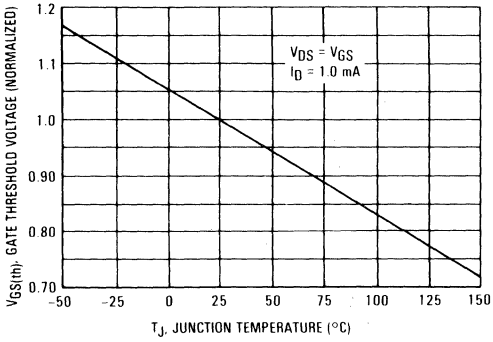
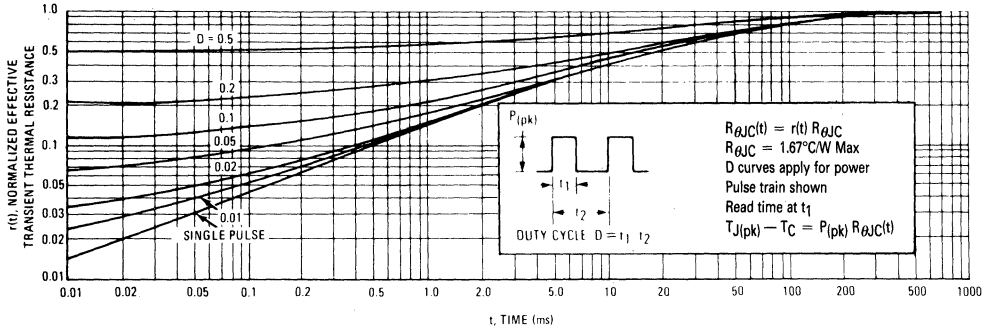


FIGURE 7 — THERMAL RESPONSE



OPERATING AREA INFORMATION

FIGURE 8 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA, 2N6761

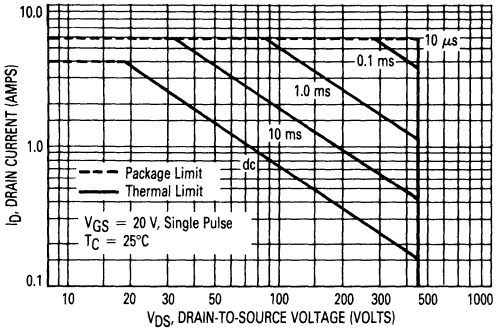


FIGURE 9 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

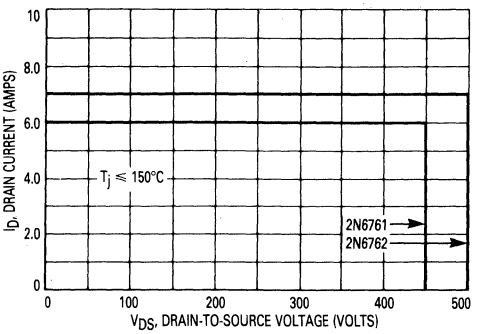
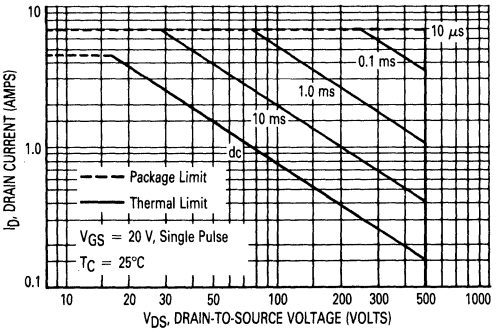


FIGURE 10 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6762



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 8 and 10 are based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figure or
T_{Jmax} = Rated maximum junction temperature
T_C = Device case temperature
P_D = Rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = Rated steady state thermal resistance
r(t) = Normalized thermal response from Figure 7.

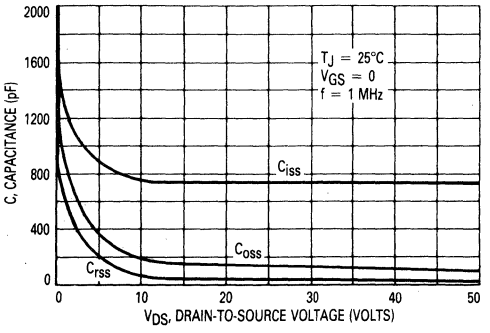
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

FIGURE 11 — CAPACITANCE VARIATION



IRF120 IRF520
IRF121 IRF521
IRF122 IRF522
IRF123 IRF523

MOTOROLA

C

Advance Information

Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF120/520	100 V	0.3 Ω	8.0 A
IRF121/521	60 V	0.3 Ω	8.0 A
IRF122/522	100 V	0.4 Ω	7.0 A
IRF123/523	60 V	0.4 Ω	7.0 A

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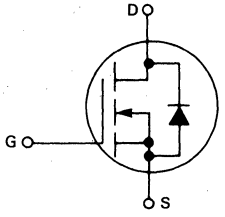
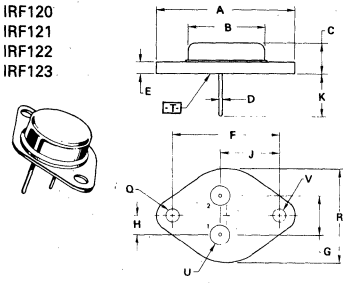
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



IRF120
IRF121
IRF122
IRF123



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-05
TO-204AA
(TO-3)

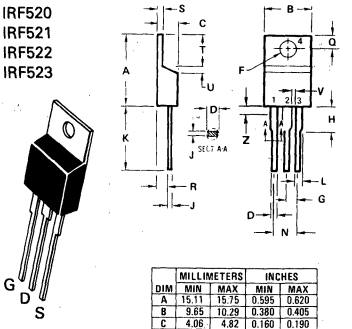
MAXIMUM RATINGS

Rating	Symbol	IRF 120 520	IRF 121 521	IRF 122 522	IRF 123 523	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	8.0	8.0	7.0	7.0	Adc
Continuous Drain Current T_C = 100°C	I_D	5.0	5.0	4.0	4.0	Adc
Drain Current — Pulsed	I_{DM}	32	32	28	28	Adc
Gate Current — Pulsed	I_{GM}	±1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	3.12	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

IRF520
IRF521
IRF522
IRF523



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF121,123,521,523	$V_{(BR)DSS}$	60	—	—	Vdc
	IRF120,122,520,522		100	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} Rated V_{DSS})		I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)			—	—	1.0	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF120,121,520,521	$I_{D(on)}$	8.0	—	—	Adc
	IRF122,123,522,523		7.0	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 4.0 A)	IRF120,121,520,521	$r_{DS(on)}$	—	—	0.30	Ohms
	IRF122,123,522,523		—	—	0.40	
Forward Transconductance (V_{DS} = 15 V, I_D = 4.0 A)		g_{fs}	1.5	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	600	pF
Output Capacitance		C_{oss}	—	—	400	
Reverse Transfer Capacitance		C_{rss}	—	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	$V_{DD} \cong 0.5\ V_{DSS}$, I_D = 4.0 A, Z_o = 50 Ω	$t_{d(on)}$	—	—	40	ns
Rise Time		t_r	—	—	70	
Turn-Off Delay Time		$t_{d(off)}$	—	—	100	
Fall Time		t_f	—	—	70	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.3	Vdc
Reverse Recovery Time		t_{rr}	280	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

FIGURE 1 — SWITCHING TEST CIRCUIT

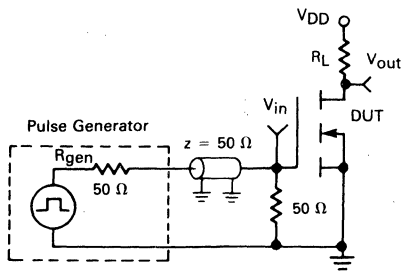
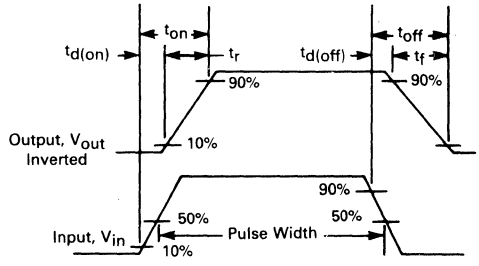


FIGURE 2 — SWITCHING WAVEFORMS



IRF140 IRF540
IRF141 IRF541
IRF142 IRF542
IRF143 IRF543

MOTOROLA

C

Advance Information

Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF140/540	100 V	0.085 Ω	27 A
IRF141/541	60 V	0.085 Ω	27 A
IRF142/542	100 V	0.11 Ω	24 A
IRF143/543	60 V	0.11 Ω	24 A

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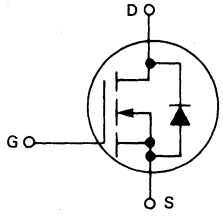
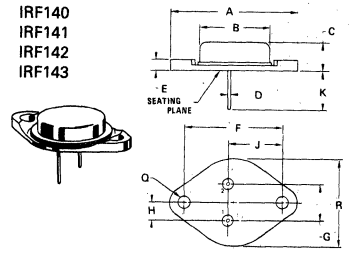
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



IRF140
IRF141
IRF142
IRF143



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

CASE 197-01
TO-204AE
(TO-3 TYPE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.69	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

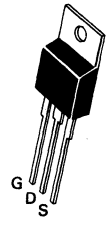
MAXIMUM RATINGS

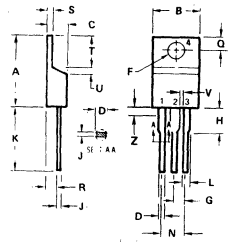
Rating	Symbol	IRF 140 541 542 543	Unit
Drain-Source Voltage	V_{DSS}	100 / 60 / 100 / 60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100 / 60 / 100 / 60	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Continuous Drain Current T_C = 25°C	I_D	27 / 27 / 24 / 24	Adc
Continuous Drain Current T_C = 100°C	I_D	17 / 17 / 15 / 15	Adc
Pulsed Drain Current	I_{DM}	108 / 108 / 96 / 96	Adc
Gate Current — Pulsed	I_{GM}	1.5	Adc
Total Power Dissipation @ T_C = 25°C	P_D	125	Watts
Derate above 25°C		1.0	W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

IRF540
IRF541
IRF542
IRF543





STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	
Z	–	2.03	–	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF140,142,540,542	$V_{(BR)DSS}$	100	—	—	Vdc
	IRF141,143,541,543		60	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS})		I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)			—	—	1.0	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF140,141,540,541	$I_{D(on)}$	27	—	—	Adc
	IRF142,143,542,543		24	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 15 A)	IRF140,141,540,541	$r_{DS(on)}$	—	—	0.085	Ohm
	IRF142,143,542,543		—	—	0.11	
Forward Transconductance (V_{DS} = 15 V, I_D = 15 A)		g_{fs}	6.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	1600	pF
Output Capacitance		C_{oss}	—	—	800	
Reverse Transfer Capacitance		C_{rss}	—	—	300	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	V_{DD} ≈ 30 V, I_D = 15 A, Z_o = 4.7 Ω	$t_{d(on)}$	—	—	30	ns
Rise Time		t_r	—	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	—	80	
Fall Time		t_f	—	—	30	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.3	Vdc
Reverse Recovery Time		t_{rr}	500	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

FIGURE 1 — SWITCHING TEST CIRCUIT

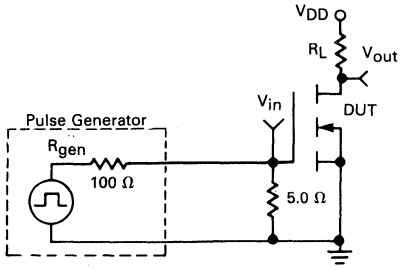
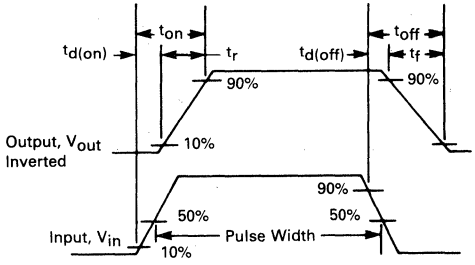


FIGURE 2 — SWITCHING WAVEFORMS



C

IRF150
IRF151
IRF152
IRF153

MOTOROLA

C

Advance Information

Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF150	100 V	0.055 Ω	40 A
IRF151	60 V	0.055 Ω	40 A
IRF152	100 V	0.08 Ω	33 A
IRF153	60 V	0.08 Ω	33 A

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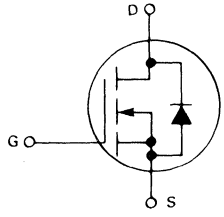
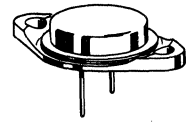
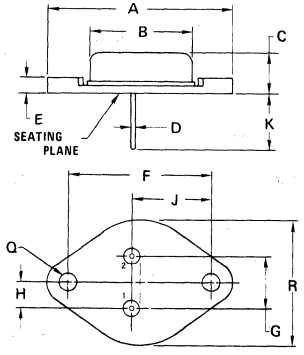
TMOS™



IRF150
IRF151
IRF152
IRF153





Pin 1: Gate
2: Source
Case: Drain

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE (TYPE)
(TO-3 TYPE)

MAXIMUM RATINGS

Rating	Symbol	IRF 150	IRF 151	IRF 152	IRF 153	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	40	40	33	33	Adc
Continuous Drain Current T_C = 100°C	I_D	25	25	20	20	Adc
Drain Current — Pulsed	I_{DM}	160	160	132	132	Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C	P_D	150				Watts
Derate above 25°C		1.2				W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF150,152	$V_{(BR)DSS}$	100	—	—	Vdc
	IRF151,153		60	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS})		I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)			—	—	1.0	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF150,151	$I_{D(on)}$	40	—	—	Adc
	IRF152,153		33	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 20 A)	IRF150,151	$r_{DS(on)}$	—	—	0.055	Ohm
	IRF152,153		—	—	0.08	
Forward Transconductance (V_{DS} = 15 V, I_D = 20 A)		g_{fs}	9.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	3000	pF
Output Capacitance		C_{oss}	—	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	—	500	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	$V_{DD} \simeq$ 24 V, I_D = 20 A, Z_o = 4.7 Ω	$t_{d(on)}$	—	—	35	ns
Rise Time		t_r	—	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	—	125	
Fall Time		t_f	—	—	100	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.3	Vdc
Reverse Recovery Time		t_{rr}	600	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

FIGURE 1 — SWITCHING TEST CIRCUIT

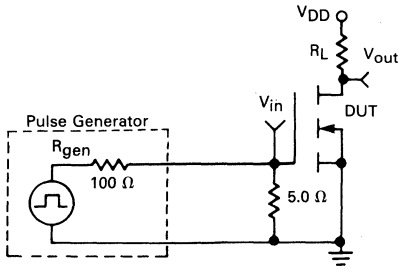
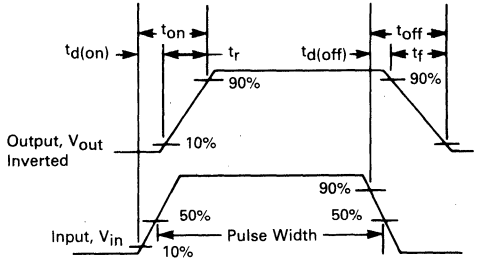


FIGURE 2 — SWITCHING WAVEFORMS



C

IRF220 IRF620
IRF221 IRF621
IRF222 IRF622
IRF223 IRF623

MOTOROLA

C

Advance Information

Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF220/620	200 V	0.8 Ω	5.0 A
IRF221/621	150 V	0.8 Ω	5.0 A
IRF222/622	200 V	1.2 Ω	4.0 A
IRF223/623	150 V	1.2 Ω	4.0 A

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

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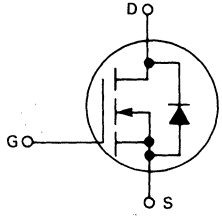
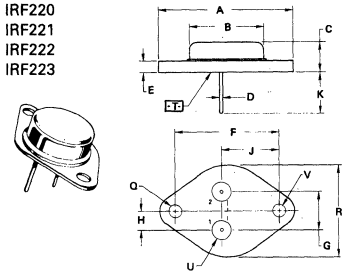
- Silicon Gate for Fast Switching Speeds
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



IRF220
IRF221
IRF222
IRF223

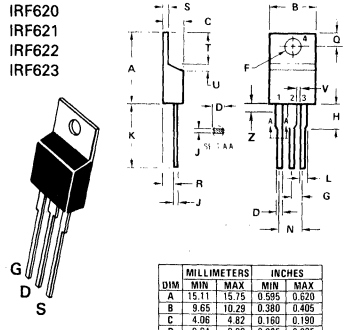


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-05
TO-204AA
(TO-3 TYPE)

IRF620
IRF621
IRF622
IRF623



G
D
S

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	IRF 220 620	IRF 221 621	IRF 222 622	IRF 223 623	Unit
Drain-Source Voltage	V_{DSS}	200	150	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	5.0	5.0	4.0	4.0	Adc
Continuous Drain Current T_C = 100°C	I_D	3.0	3.0	2.5	2.5	Adc
Drain Current — Pulsed	I_{DM}	20	20	16	16	Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	3.12	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF220,222,620,622	$V_{(BR)DSS}$	200	—	—	Vdc
	IRF221,223,621,623		150	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS})		I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)			—	—	1.0	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF220,221,620,621	$I_{D(on)}$	5.0	—	—	Adc
	IRF222,223,622,623		4.0	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 2.5 A)	IRF220,221,620,621	$r_{DS(on)}$	—	—	0.8	Ohms
	IRF222,223,622,623		—	—	1.2	
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)		g_{fs}	1.3	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	600	pF
Output Capacitance		C_{oss}	—	—	300	
Reverse Transfer Capacitance		C_{rss}	—	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	$V_{DD} \simeq 0.5\ V_{DSS}$, I_D = 2.5 A, Z_o = 50 Ω	$t_{d(on)}$	—	—	40	ns
Rise Time		t_r	—	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	—	100	
Fall Time		t_f	—	—	60	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.8	Vdc
Reverse Recovery Time		t_{rr}	450	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — SWITCHING TEST CIRCUIT

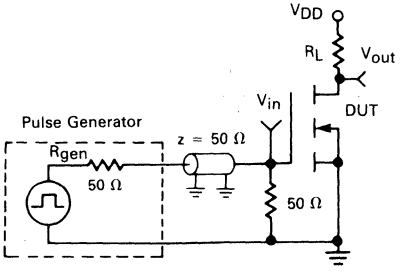
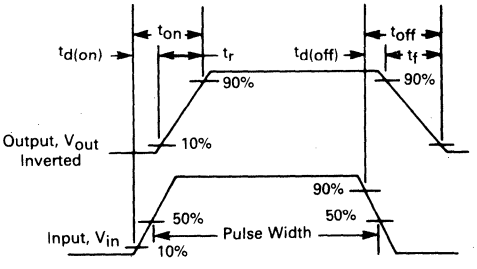


FIGURE 2 — SWITCHING WAVEFORMS



IRF230 IRF630
IRF231 IRF631
IRF232 IRF632
IRF233 IRF633

MOTOROLA

C

Advance Information

Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF230/630	200 V	0.4 Ω	9.0 A
IRF231/631	150 V	0.4 Ω	9.0 A
IRF232/632	200 V	0.6 Ω	8.0 A
IRF233/633	150 V	0.6 Ω	8.0 A

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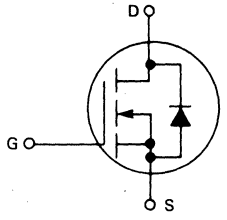
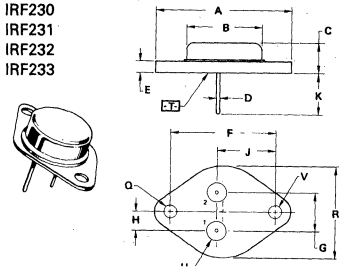
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



IRF230
IRF231
IRF232
IRF233

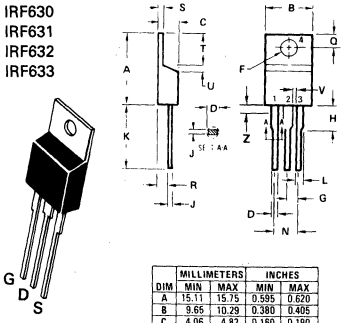


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-05
TO-204AA
(TO-3)

IRF630
IRF631
IRF632
IRF633



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	
Z	–	2.03	–	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	IRF 230 630	IRF 231 631	IRF 232 632	IRF 233 633	Unit
Drain-Source Voltage	V_{DSS}	200	150	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	9.0	9.0	8.0	8.0	Adc
Continuous Drain Current T_C = 100°C	I_D	6.0	6.0	5.0	5.0	Adc
Drain Current — Pulsed	I_{DM}	36	36	32	32	Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF230,232,630,632	$V_{(BR)DSS}$	200	—	—	Vdc
	IRF231,233,631,633		150	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS})		I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)			—	—	1.0	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF230,231,630,631	$I_{D(on)}$	9.0	—	—	Adc
	IRF232,233,632,633		8.0	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 5.0 A)	IRF230,231,630,631	$r_{DS(on)}$	—	—	0.4	Ohm
	IRF232,233,632,633		—	—	0.6	
Forward Transconductance (V_{DS} = 15 V, I_D = 5.0 A)		g_{fs}	3.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	800	pF
Output Capacitance		C_{oss}	—	—	450	
Reverse Transfer Capacitance		C_{rss}	—	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	V_{DD} ≃ 90 V, I_D = 5.0 A, Z_o = 15 Ω	$t_{d(on)}$	—	—	30	ns
Rise Time		t_r	—	—	50	
Turn-Off Delay Time		$t_{d(off)}$	—	—	50	
Fall Time		t_f	—	—	40	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.8	Vdc
Reverse Recovery Time		t_{rr}	450	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

FIGURE 1 — SWITCHING TEST CIRCUIT

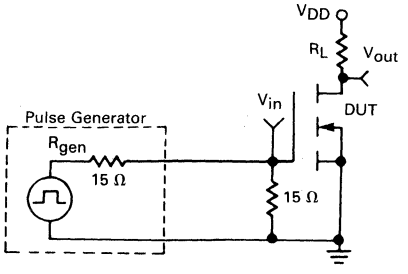
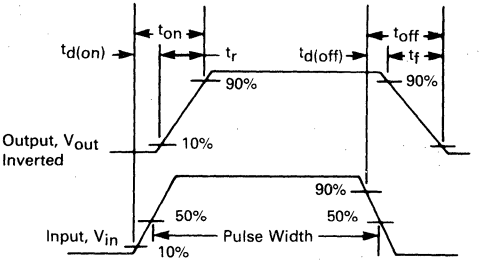


FIGURE 2 — SWITCHING WAVEFORMS



IRF240 IRF640
IRF241 IRF641
IRF242 IRF642
IRF243 IRF643

MOTOROLA

C

Advance Information

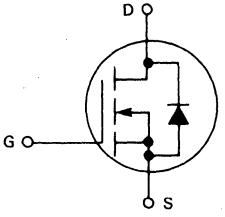
Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF240/640	200 V	0.18 Ω	18 A
IRF241/641	150 V	0.18 Ω	18 A
IRF242/642	200 V	0.22 Ω	16 A
IRF243/643	150 V	0.22 Ω	16 A

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

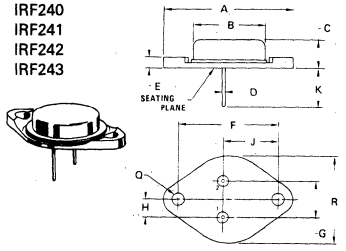
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



IRF240
IRF241
IRF242
IRF243



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

CASE 197-01
TO-204AE
(TO-3 TYPE)

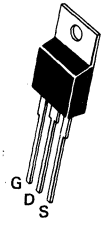
MAXIMUM RATINGS

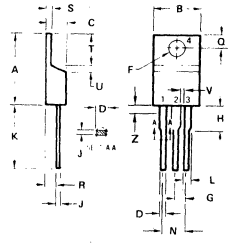
Rating	Symbol	IRF 240 640	IRF 241 641	IRF 242 642	IRF 243 643	Unit
Drain-Source Voltage	V_{DSS}	200	150	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	18	18	16	16	Adc
Continuous Drain Current T_C = 100°C	I_D	11	11	10	10	Adc
Drain Current — Pulsed	I_{DM}	72	72	64	64	Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

IRF640
IRF641
IRF642
IRF643





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF240,242,640,642	$V_{(BR)DSS}$	200	—	—	Vdc
	IRF241,243,641,643		150	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS})		I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)			—	—	1.0	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF240,241,640,641	$I_{D(on)}$	18	—	—	Adc
	IRF242,243,642,643		16	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 10A)	IRF240,241,640,641	$r_{DS(on)}$	—	—	0.18	Ohm
	IRF242,243,642,643		—	—	0.22	
Forward Transconductance (V_{DS} = 15 V, I_D = 10 A)		g_{fs}	6.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	1600	pF
Output Capacitance		C_{oss}	—	—	750	
Reverse Transfer Capacitance		C_{rss}	—	—	300	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	V_{DD} ≈ 75 V, I_D = 10 A, Z_o = 4.7 Ω	$t_{d(on)}$	—	—	30	ns
Rise Time		t_r	—	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	—	80	
Fall Time		t_f	—	—	60	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.9	Vdc
Reverse Recovery Time		t_{rr}	650	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

FIGURE 1 — SWITCHING TEST CIRCUIT

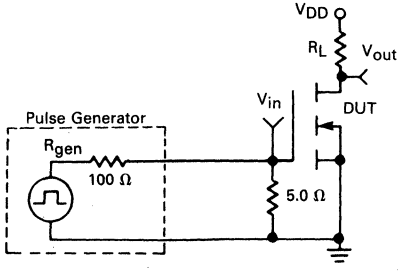
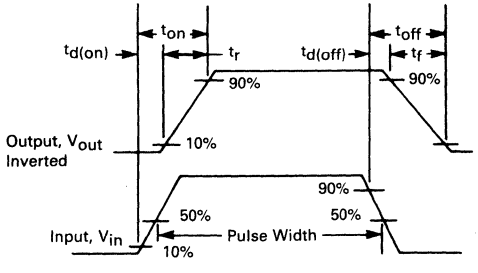


FIGURE 2 — SWITCHING WAVEFORMS



IRF250
IRF251
IRF252
IRF253

MOTOROLA

C

Advance Information

Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF250	200 V	0.085 Ω	30 A
IRF251	150 V	0.085 Ω	30 A
IRF252	200 V	0.120 Ω	25 A
IRF253	150 V	0.120 Ω	25 A

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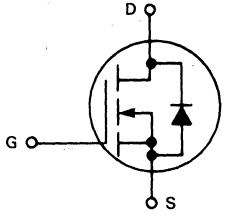
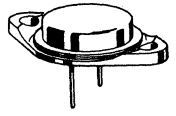
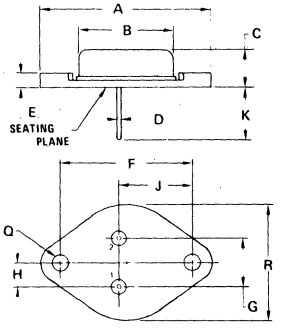
- Silicon Gate for Fast Switching Speeds
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



IRF250
IRF251
IRF252
IRF253





STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE
(TO-3 TYPE)

MAXIMUM RATINGS

Rating	Symbol	IRF 250	IRF 251	IRF 252	IRF 253	Unit
Drain-Source Voltage	V_{DSS}	200	150	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	30	30	25	25	Adc
Continuous Drain Current T_C = 100°C	I_D	19	19	16	16	Adc
Pulsed Drain Current	I_{DM}	120	120	100	100	Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF250,252	$V_{(BR)DSS}$	200	—	—	Vdc
	IRF251,253		150	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS})		I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)			—	—	1.00	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF250,251	$I_{D(on)}$	30	—	—	Adc
	IRF252,253		25	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 16 A)	IRF250,251	$r_{DS(on)}$	—	—	0.085	Ohm
	IRF252,253		—	—	0.120	
Forward Transconductance (V_{DS} = 15 V, I_D = 16 A)		g_{fs}	8.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	3000	pF
Output Capacitance		C_{oss}	—	—	1200	
Reverse Transfer Capacitance		C_{rss}	—	—	500	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	V_{DD} = 95 V, I_D = 16 A, Z_o = 4.7 Ω	$t_{d(on)}$	—	—	35	ns
Rise Time		t_r	—	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	—	125	
Fall Time		t_f	—	—	100	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.8	Vdc
Reverse Recovery Time		t_{rr}	750	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

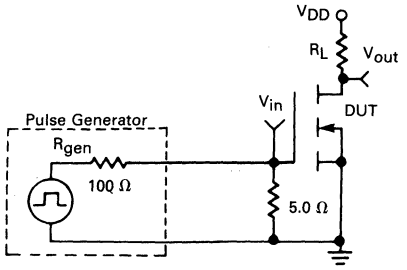
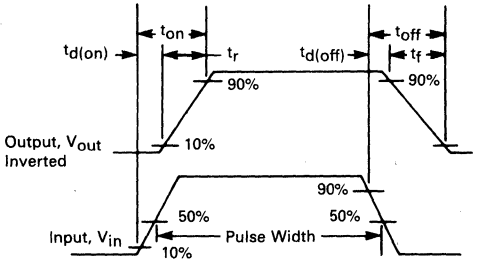


FIGURE 2 — SWITCHING WAVEFORMS



IRF330-333/430-433
IRF730-733/830-833

MOTOROLA

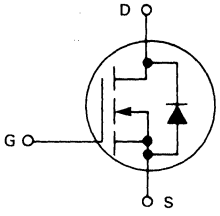
C

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

. . . designed for high-voltage, high-speed power-switching applications, such as line-operated switching regulators, converters, solenoid and relay drivers. These devices are direct replacements for International Rectifier (IR) Power MOSFETs.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at Elevated Temperatures.
- Rugged — SOA Is Power Dissipation Limited
- Low Drive Requirement, $V_{GS(th)}$ = 4.0 Volts (max)

TMOS™



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	See Table 2, TO-204AA See Table 3, TO-220AB	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	See Table 2, TO-204AA See Table 3, TO-220AB	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

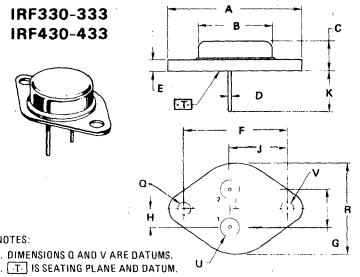
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

4.0–5.5 AMPERE

N-CHANNEL TMOS POWER FETs

IRF330-333
IRF430-433



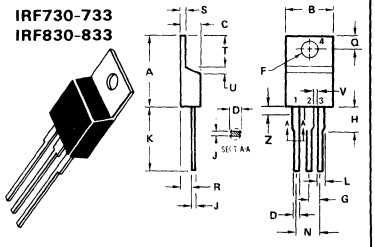
NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ϕ0.13 (0.005) Ⓜ | T | V Ⓜ |
   FOR LEADS:
   ⌖ | ϕ0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-05
TO-204AA

IRF730-733
IRF830-833



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3 ONLY.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.
5. CONTROLLING DIMENSION: INCH.

TABLE 2 — TO-204AA (Formerly TO-3)

	MAXIMUM RATINGS		ELECTRICAL CHARACTERISTICS						
Device	V_{DSS} (Volts)	I_D (Amp)	$r_{DS(on)}$ (Ohm) Max	@ I_D (Amp)	$V_{GS(th)}$ (Volts) Min/Max	g_{fs} (mho) Min	t_{on} (ns) Max	t_{off} (ns) Max	@ I_D (Amp)
IRF330	400	5.5	1.0	3.0	2.0/4.0	3.0	110	85	3.0
IRF331	350								
IRF332	400	4.5	1.5						
IRF333	350								
IRF430	500			2.5		2.5	90	85	2.5
IRF431	450								
IRF432	500	4.0	2.0						
IRF433	450								

TABLE 3 — TO-220AB

	MAXIMUM RATINGS		ELECTRICAL CHARACTERISTICS						
Device	V_{DSS} (Volts)	I_D (Amp)	$r_{DS(on)}$ (Ohm) Max	@ I_D (Amp)	$V_{GS(th)}$ (Volts) Min/Max	g_{fs} (mho) Min	t_{on} (ns) Max	t_{off} (ns) Max	@ I_D (Amp)
IRF730	400	5.5	1.0	3.0	2.0/4.0	3.0	110	85	3.0
IRF731	350								
IRF732	400	4.5	1.5						
IRF733	350								
IRF830	500			2.5		2.5	90	85	2.5
IRF831	450								
IRF832	500	4.0	2.0						
IRF833	450								

IRF510
IRF511
IRF512
IRF513

MOTOROLA

C

Advance Information

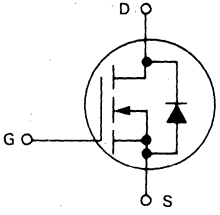
Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF510	100 V	0.6 Ω	4.0 A
IRF511	60 V	0.6 Ω	4.0 A
IRF512	100 V	0.8 Ω	3.5 A
IRF513	60 V	0.8 Ω	3.5 A

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

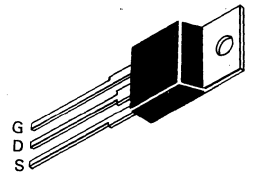
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

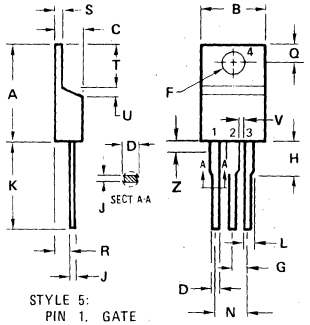
- Silicon Gate for Fast Switching Speeds
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



IRF510
IRF511
IRF512
IRF513





STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3 ONLY.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.
5. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-
Z	—	2.03	—	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	IRF 510	IRF 511	IRF 512	IRF 513	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	4.0	4.0	3.5	3.5	Adc
Continuous Drain Current T_C = 100°C	I_D	2.5	2.5	2.0	2.0	Adc
Drain Current Pulsed	I_{DM}	16	16	14	14	Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	6.4	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF510,512	$V_{(BR)DSS}$	100	—	—	Vdc
	IRF511,513		60	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS})		I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)			—	—	1.0	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF510,511	$I_{D(on)}$	4.0	—	—	Adc
	IRF512,513		3.5	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 2.0 A)	IRF510,511	$r_{DS(on)}$	—	—	0.6	Ohms
	IRF512,513		—	—	0.8	
Forward Transconductance (V_{DS} = 15 V, I_D = 2.0 A)		g_{fs}	1.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	150	pF
Output Capacitance		C_{oss}	—	—	100	
Reverse Transfer Capacitance		C_{rss}	—	—	25	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	V_{DD} ≈ 0.5 V_{DSS}, I_D = 2.0 A, Z_o = 50 Ω	$t_{d(on)}$	—	—	20	ns
Rise Time		t_r	—	—	25	
Turn-Off Delay Time		$t_{d(off)}$	—	—	25	
Fall Time		t_f	—	—	20	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.0	Vdc
Reverse Recovery Time		t_{rr}	230	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

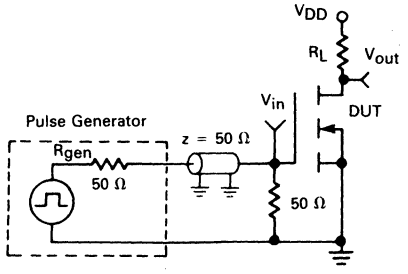
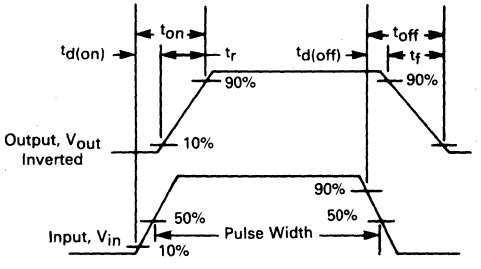


FIGURE 2 — SWITCHING WAVEFORMS



IRF530 IRF130
IRF531 IRF131
IRF532 IRF132
IRF533 IRF133

MOTOROLA

C

Advance Information

Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF530/130	100 V	0.18 Ω	14 A
IRF531/131	60 V	0.18 Ω	14 A
IRF532/132	100 V	0.25 Ω	12 A
IRF533/133	60 V	0.25 Ω	12 A

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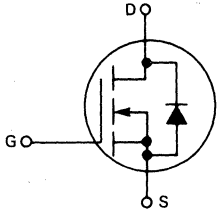
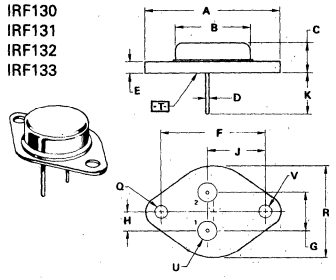
TMOS™



IRF130
IRF131
IRF132
IRF133

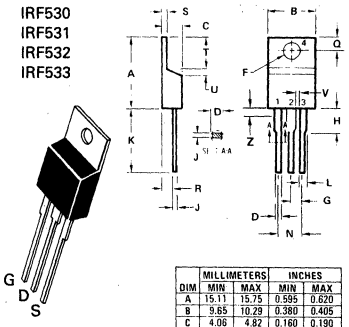


STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(TO-3 TYPE)

IRF530
IRF531
IRF532
IRF533



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	IRF 530 130	IRF 531 131	IRF 532 132	IRF 533 133	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	14	14	12	12	Adc
Continuous Drain Current T_C = 100°C	I_D	9.0	9.0	8.0	8.0	Adc
Drain Current — Pulsed	I_{DM}	56	56	48	48	Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF130,132,530,532	$V_{(BR)DSS}$	100	—	—	Vdc
	IRF131,133,531,533		60	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS})		I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)			—	—	1.0	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF130,131,530,531	$I_{D(on)}$	14	—	—	Adc
	IRF132,133,532,533		12	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 8.0 A)	IRF130,131,530,531	$r_{DS(on)}$	—	—	0.18	Ohm
	IRF132,133,532,533		—	—	0.25	
Forward Transconductance (V_{DS} = 15 V, I_D = 8.0 A)		g_{fs}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	800	pF
Output Capacitance		C_{oss}	—	—	500	
Reverse Transfer Capacitance		C_{rss}	—	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	V_{DD} ≃ 36 V, I_D = 8.0 A, Z_o = 15 Ω	$t_{d(on)}$	—	—	30	ns
Rise Time		t_r	—	—	75	
Turn-Off Delay Time		$t_{d(off)}$	—	—	40	
Fall Time		t_f	—	—	45	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.3	Vdc
Reverse Recovery Time		t_{rr}	360	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

FIGURE 1 — SWITCHING TEST CIRCUIT

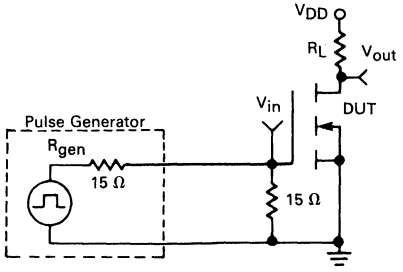
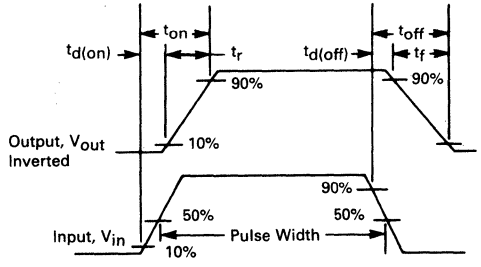


FIGURE 2 — SWITCHING WAVEFORMS



IRF610
IRF611
IRF612
IRF613

MOTOROLA

C

Advance Information

Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF610	200 V	1.5 Ω	2.5 A
IRF611	150 V	1.5 Ω	2.5 A
IRF612	200 V	2.4 Ω	2.0 A
IRF613	150 V	2.4 Ω	2.0 A

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- Silicon Gate for Fast Switching Speeds
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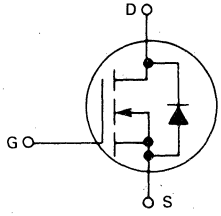
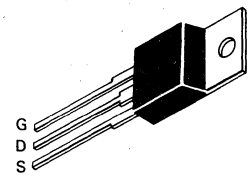
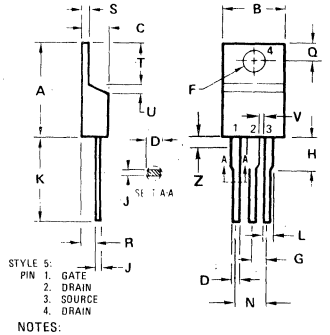
TMOS™



IRF610
IRF611
IRF612
IRF613





NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3 ONLY.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.
5. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-
Z	—	2.03	—	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	IRF 610	IRF 611	IRF 612	IRF 613	Unit
Drain-Source Voltage	V_{DSS}	200	150	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	2.5	2.5	2.0	2.0	Adc
Continuous Drain Current T_C = 100°C	I_D	1.5	1.5	1.25	1.25	Adc
Drain Current — Pulsed	I_{DM}	10	10	8.0	8.0	Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	6.4	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF610,612	$V_{(BR)DSS}$	200	—	—	Vdc
	IRF611,613		150	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS})		I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)			—	—	1.0	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF610,611	$I_{D(on)}$	2.5	—	—	Adc
	IRF612,613		2.0	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 1.25 A)	IRF610,611	$r_{DS(on)}$	—	—	1.5	Ohms
	IRF612,613		—	—	2.4	
Forward Transconductance (V_{DS} = 15 V, I_D = 1.25 A)		g_{fs}	0.8	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	150	pF
Output Capacitance		C_{oss}	—	—	80	
Reverse Transfer Capacitance		C_{rss}	—	—	25	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	V_{DD} ≃ 0.5 V_{DSS}, I_D = 1.25 A, Z_o = 50 Ω	$t_{d(on)}$	—	—	15	ns
Rise Time		t_r	—	—	25	
Turn-Off Delay Time		$t_{d(off)}$	—	—	15	
Fall Time		t_f	—	—	15	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.8	Vdc
Reverse Recovery Time		t_{rr}	290	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

FIGURE 1 — SWITCHING TEST CIRCUIT

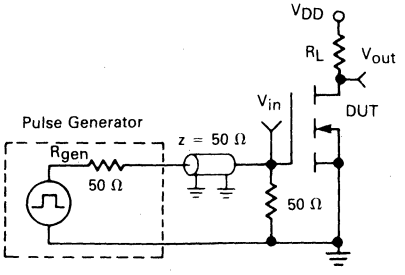
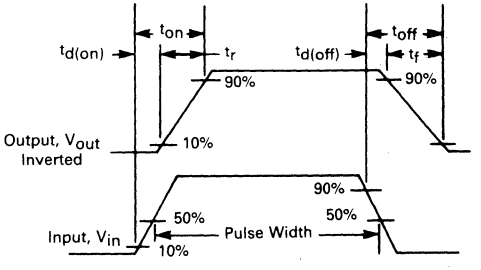


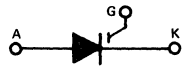
FIGURE 2 — SWITCHING WAVEFORMS



MCR1000 series

MOTOROLA

C



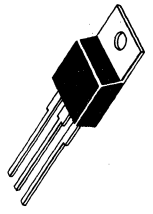
TMOS™

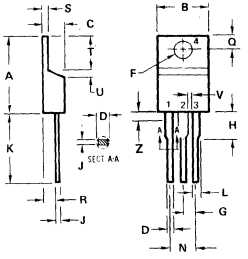
THYRISTORS
15 AMPERES RMS
200-400-600 VOLTS
ASYMMETRICAL

SILICON CONTROLLED RECTIFIERS

. . . designed primarily for very high speed switching, high current pulse applications — laser modulators, printers, florescent lighting, switching power supplies and particle accelerators.

- Asymmetrical Blocking Voltage To 600 V
- Very High dv/dt - 1000 V/μs @ T_J = 125°C*
- Very Fast Switching - t_q @ T_J = 25°C, 8.0 μs Max
- Technology Leadership TMOS SCR
- For More Information See EB-103





STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

NOTES:
1. DIMENSIONS L AND H APPLIES TO ALL LEADS.
2. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-
Z	—	2.03	—	0.080

CASE 221A-02
TO-220 AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Forward Blocking Voltage MCR1000-4 MCR1000-6 MCR1000-8	V_{DRM}	 200 400 600	Volts
Forward Current RMS (T_C = 25°C) (All Conduction Angles)	$I_{T(RMS)}$	15	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz) T_J = 125°C)	I_{TSM}	90	Amps
Circuit Fusing Considerations (T_J = 0 to +125°C, t = 1.0 to 8.3 ms)	I^2t	34	A^2s
Peak Gate Voltage	V_{GM}	±20	Volts
Forward Peak Gate Current	I_{GM}	1.5	Amps
Operating Junction Temperature Range	T_J	-0 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)	I_{DRM}	—	—	2.0	mA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)	I_{RRM}	—	—	2.0	mA
Peak Reverse Blocking Voltage	V_{RRM}	—	—	100	Volts
Forward "On" Voltage (I_{TM} = 20 A Peak)	V_{TM}	—	3.5	4.0	Volts
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms) (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	 V_{GT} V_{GD}	 — 0.2	 2.0 —	 2.5 —	Volts Volts
Holding Current (Anode Voltage = 12 Vdc)	I_H	—	10	40	mA
Turn-On Time (See Figure 6)	t_{gt}	—	—	200	ns
Turn-Off Time (V_{DRM} = rated voltage) (I_{TM} = 3.0 A, I_R = 2.0 A, dv/dt = 100 V/μs)	t_q	—	—	8.0	μs
Forward Voltage Application Rate (T_J = 125°C, $R_{GK} \leq 200\ \Omega$) (See Figure 7)	dv/dt	1000	—	—	V/μs
Maximum Rate of Change of On State Current (Rated V_{DRM}, I_{TM} = 20 A peak, T_J = 125°C)	di/dt	—	—	100	A/μs

C

FIGURE 1 — AVERAGE CURRENT DERATING

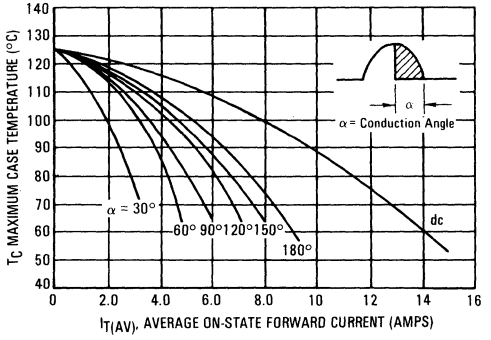


FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION

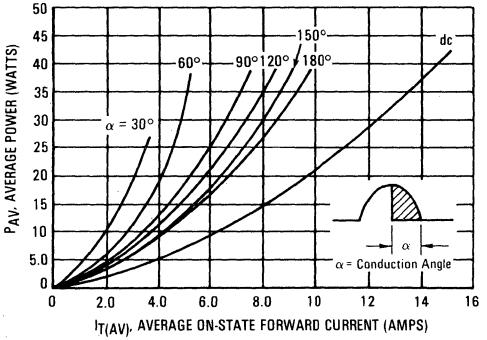


FIGURE 3 — TYPICAL GATE TRIGGER VOLTAGE

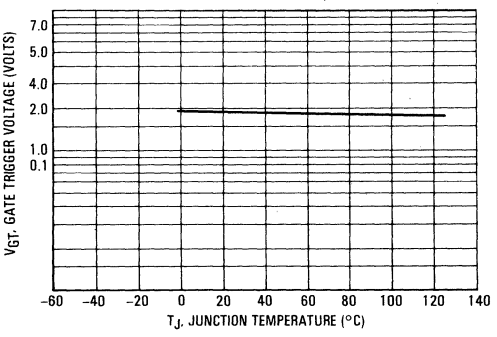


FIGURE 4 — TYPICAL HOLDING CURRENT

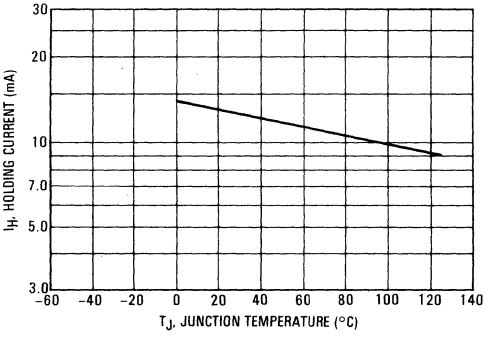


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FIGURE 5 — THERMAL RESPONSE

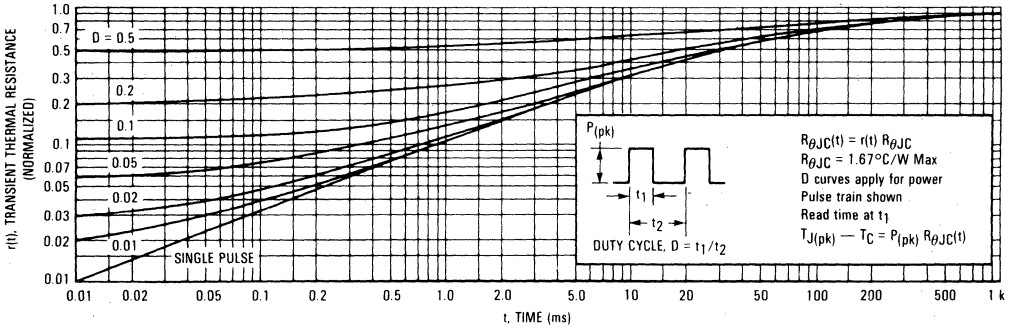


FIGURE 6 — MCR1000 SERIES TYPICAL TURN-ON CIRCUIT WITH CMOS GATING

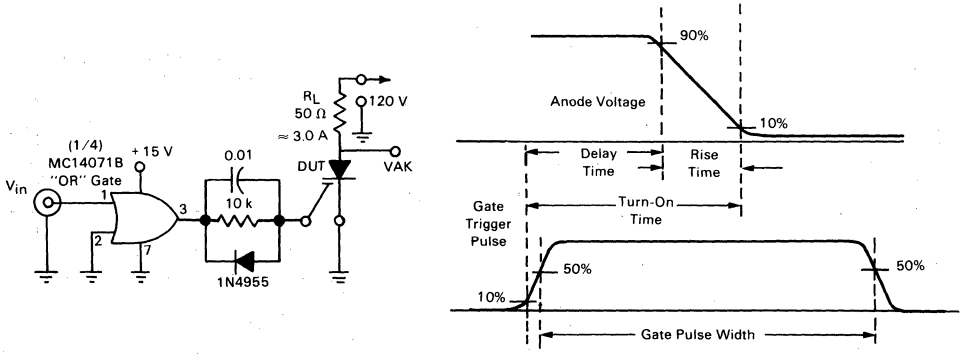
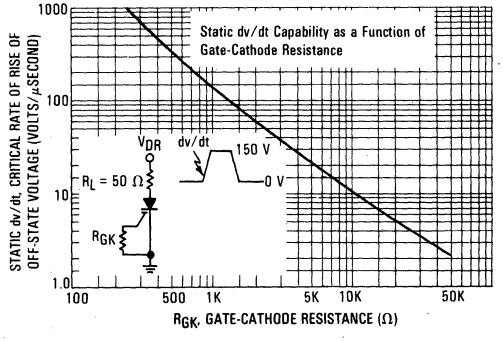


FIGURE 7 — TYPICAL dv/dt CAPABILITY



MOTOROLA

MGM20N45
MGM20N50
MGP20N45
MGP20N50

C

Designer's Data Sheet

20 AMPERE

N-CHANNEL TMOS GEMFET

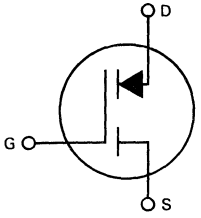
$r_{DS(on)}$ = 0.27 Ohm
450 and 500 Volts

N-CHANNEL ENHANCEMENT MODE SILICON GATE, GAIN ENHANCED MOS FIELD EFFECT TRANSISTOR

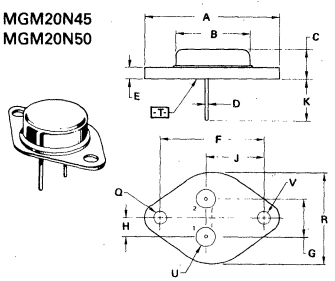
These GEMFETS are designed for high voltage, high current power controls such as line operated motor controls and converters.

- High Input Impedance
- Low On-Voltage, 2.7 V max @ 10 A
- High Peak Current Capability — 30 A
- Voltage Driven Device

TMOS™



MGM20N45
MGM20N50

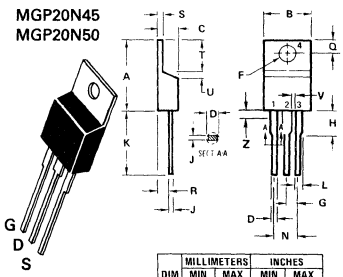


STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

TO-204AA
CASE 1-05
(TO-3 TYPE)

MGP20N45
MGP20N50



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MGM20N45 MGP20N45	MGM20N50 MGP20N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 20 30		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 100 0.8		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MGM20N45, MGP20N45	$V_{(BR)DSS}$	450	—	Vdc
	MGM20N50, MGP20N50		500	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_J = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Drain-Source On-Voltage (I_D = 10 Adc, V_{GS} = 10 V)		$V_{DS(on)}$	—	2.7	Vdc
(I_D = 20 Adc, V_{GS} = 15 V)			—	5.0	
(I_D = 10 Adc, V_{GS} = 10 V, T_J = 100°C)			—	3.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$r_{DS(on)}$	—	0.27	Ohms
Forward Transconductance (V_{DS} = 10 V, I_D = 10 A)		g_{fs}	3.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	950	pF
Output Capacitance		C_{oss}	—	150	pF
Reverse Transfer Capacitance		C_{rss}	—	60	pF

SWITCHING CHARACTERISTICS* (T_J = 100°C)

RESISTIVE SWITCHING					
Turn-On Delay Time	(V_{DS} = 250 V, I_D = 20 A, R_G = 1.0 kΩ, V_{in} = 15 V)	$t_{d(on)}$	—	0.075	μs
Rise Time		t_r	—	0.150	μs
Turn-Off Delay Time		$t_{d(off)}$	—	4.0	μs
Fall Time		t_f	—	8.0	μs
INDUCTIVE SWITCHING					
Turn-Off Delay Time	(V_{clamp} = 250 V, I_{DM} = 20 A, L = 180 μH, V_{in} = 15 V) R_G = 1.0 kΩ	$t_{d(off)}$	—	4.0	μs
Crossover Time		t_c	—	6.0	μs
Turn-Off Delay Time	R_G = 4.0 kΩ	$t_{d(off)}$	—	9.5	μs
Crossover Time		t_c	—	9.5	μs

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

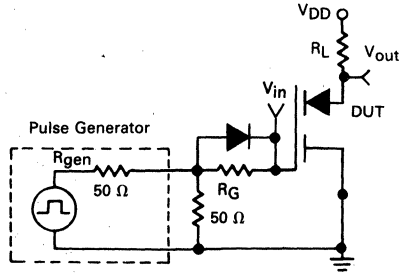
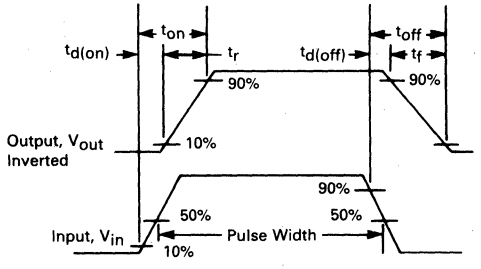


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

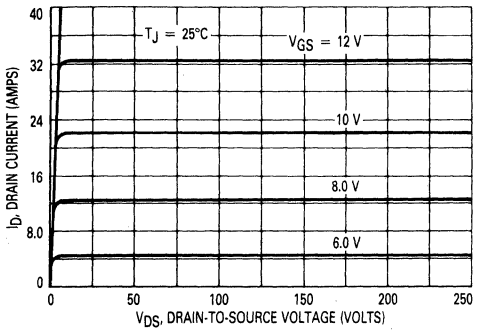


FIGURE 4 — ON-REGION CHARACTERISTICS

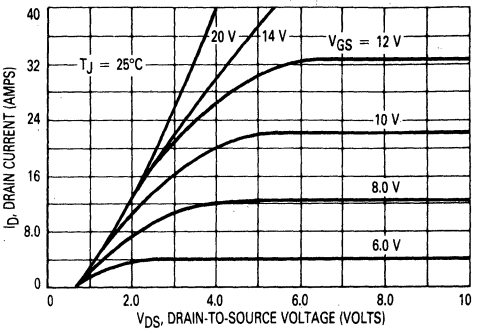


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

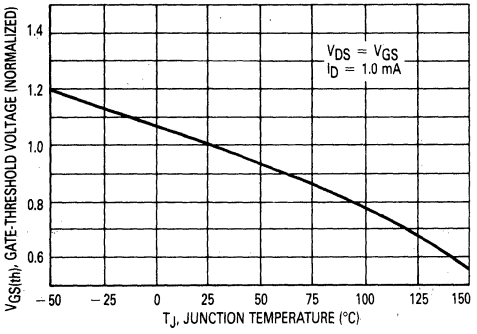


FIGURE 6 — TRANSFER CHARACTERISTICS

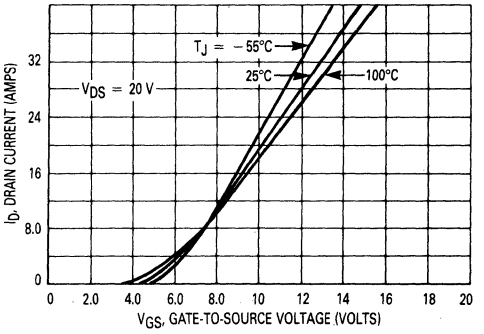


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

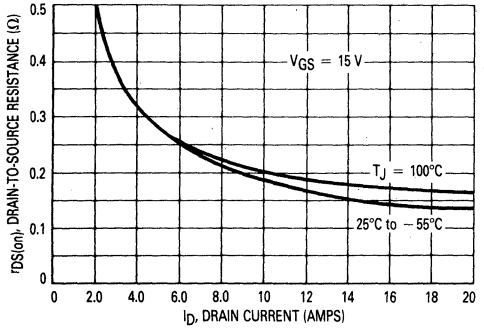
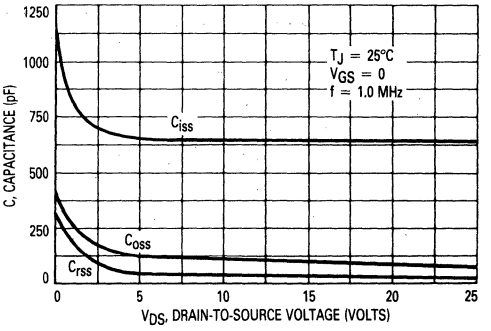


FIGURE 8 — CAPACITANCE VARIATION



C

FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

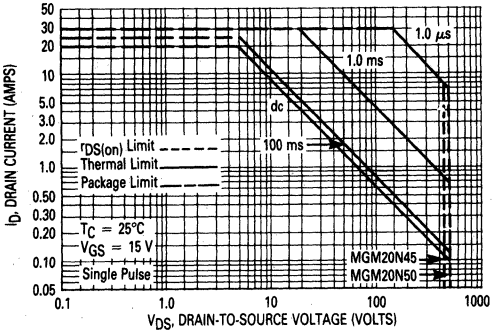
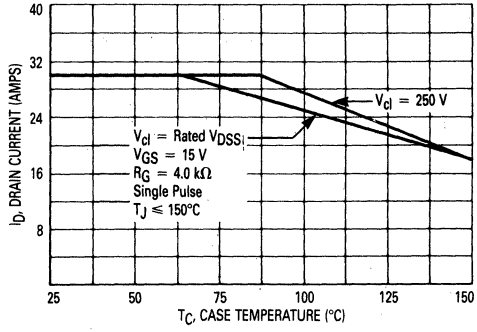


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SSOA) of a GEMFET device is a composite function of gate turn-off time, inductive clamp voltage (Vcl) and device junction temperature (T_J). Figure 10 illustrates that I_D is 30 A for Vcl ≤ 250 V and T_J ≤ 87.5°C, and for Vcl ≤ 500 V and T_J ≤ 62.5°C. Additionally, it is seen that for a peak drain current of 24 A, T_J must be maintained less than 118°C for V_{cl} = 250 V, and less than 106°C for V_{cl} = 500 V.

T_J may be calculated from the equation:

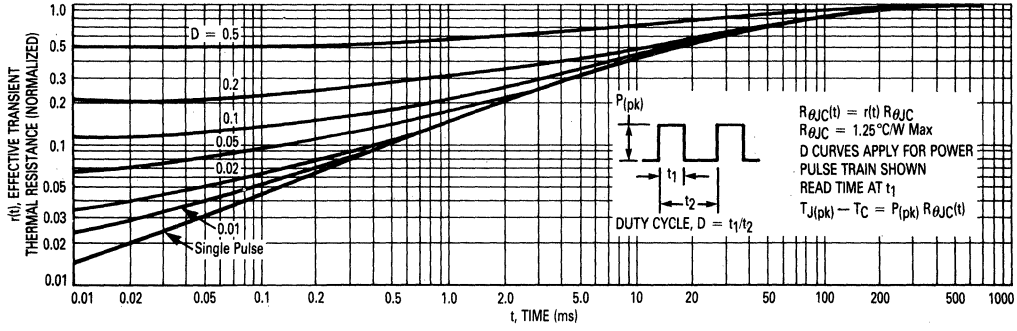
$$T_J = T_C + P_D \cdot R_{\theta JC} \cdot r(t)$$

where

P_D is the power averaged over a complete switching cycle.

Generally, SSOA current declines with decreasing gate turn-off time. Gate turn-off time is controlled by R_G; lowering R_G decreases gate turn-off time. A suggested rule-of-thumb is to derate the I_D of Figure 10 by 2.5 A for every 1100 ohms of R_G below 4.0 kΩ for case temperatures greater than 55°C.

FIGURE 11 — THERMAL RESPONSE



MOTOROLA

MTA5N12
MTA5N15
MTA4N18
MTA4N20

Designer's Data Sheet

4.0 and 5.0 AMPERE

N-CHANNEL TMOS POWER FETs

$r_{DS(on)}$ = 0.9 OHM
120 and 150 VOLTS

$r_{DS(on)}$ = 1.2 OHM
180 and 200 VOLTS

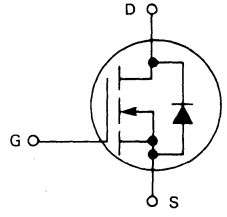
C

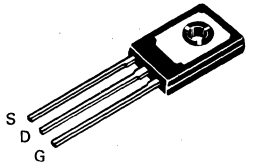
N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

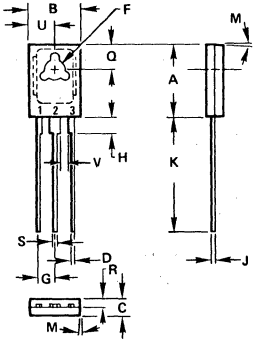
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™







STYLE 9:
PIN 1. GATE
2. DRAIN
3. SOURCE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04

MAXIMUM RATINGS

Rating	Symbol	MTA 5N12	5N15	4N18	4N20	Unit
Drain-Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous	I_D	5.0		4.0		Adc
Pulsed	I_{DM}	10		8.0		
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C	P_D	30				Watts
Derate above 25°C		0.32				W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	3.12	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTA5N12	$V_{BR(DSS)}$	120	—	Vdc
	MTA5N15		150	—	
	MTA4N18		180	—	
	MTA4N20		200	—	
Zero Gate Voltage Drain Current (V_{DSS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_C = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100 °C			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	MTA5N12/MTA5N15	$r_{DS(on)}$	—	0.9	Ohm
(V_{GS} = 10 Vdc, I_D = 2.0 Adc)	MTA4N18/MTA4N20		—	1.2	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 5.0 Adc)	MTA5N12/MTA5N15		—	6.4	
(I_D = 2.5 Adc, T_J = 100°C)	MTA5N12/MTA5N15		—	4.5	
(I_D = 4.0 Adc)	MTA4N18/MTA4N20		—	6.0	
(I_D = 2.0 Adc, T_C = 100°C)	MTA4N18/MTA4N20		—	4.8	
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)	MTA5N12/MTA5N15	g_{fs}	0.75	—	mhos
(V_{DS} = 15 V, I_D = 2.0 A)	MTA4N18/MTA4N20		0.75	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	—	250	pF
Output Capacitance		C_{oss}	—	100	
Reverse Transfer Capacitance		C_{rss}	—	40	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 1 and 2	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	20	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	50	

SOURCE-DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0 See Figures 16 and 17)	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	150	ns
Reverse Recovery Time		t_{rr}	250	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

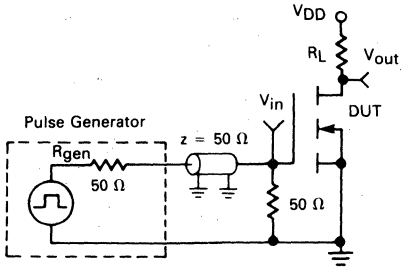
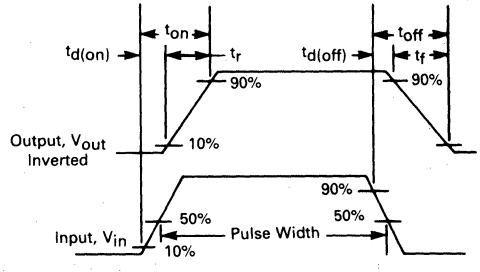


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

MTA5N12, MTA5N15

FIGURE 3 — ON-REGION CHARACTERISTICS

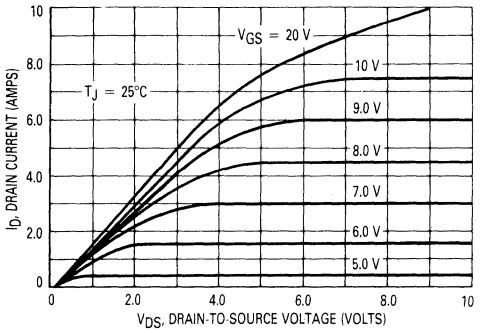


FIGURE 5 — TRANSFER CHARACTERISTICS

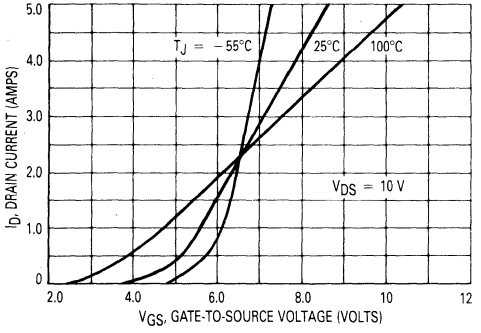
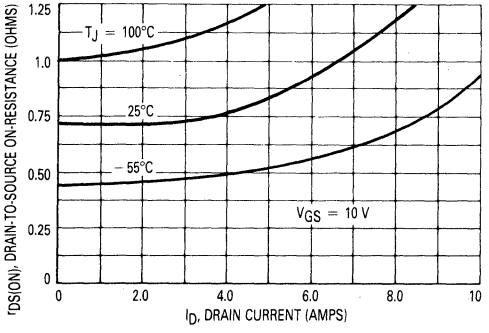


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT



MTA4N18, MTA4N20

FIGURE 4 — ON-REGION CHARACTERISTICS

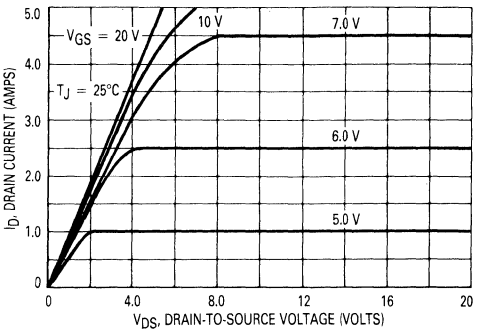


FIGURE 6 — TRANSFER CHARACTERISTICS

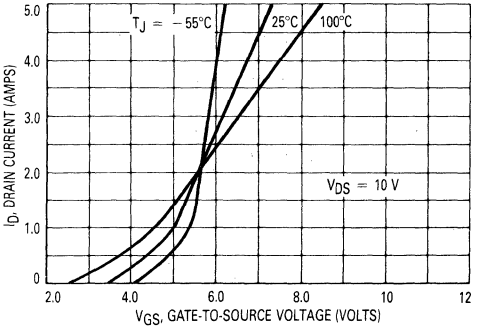
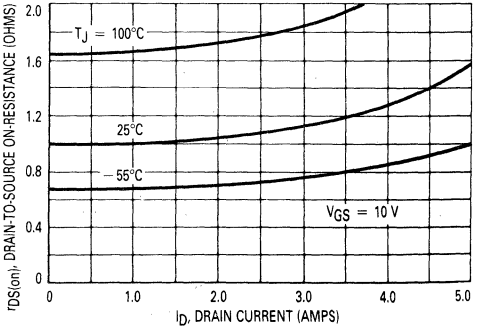


FIGURE 8 — ON-RESISTANCE versus DRAIN CURRENT



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C

TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

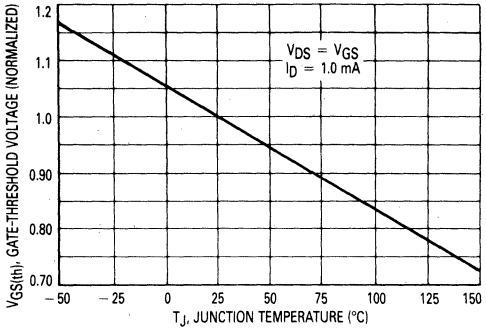


FIGURE 10 — CAPACITANCE VARIATION

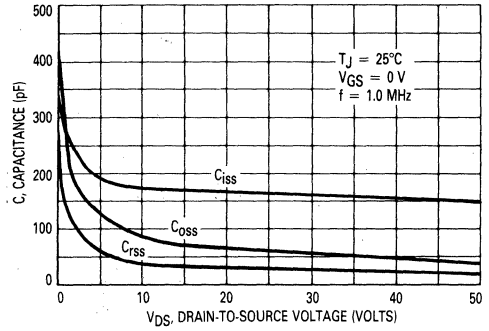
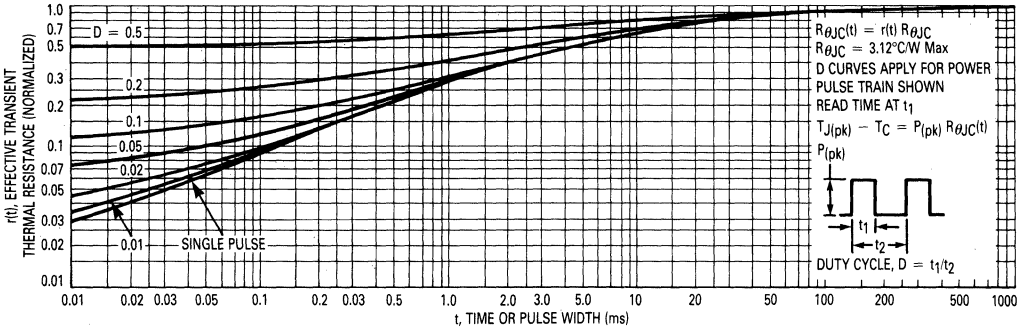


FIGURE 11 — THERMAL RESPONSE
MTA5N12, MTA5N15, MTA4N18, MTA4N20



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 0.5 Amp. (See Figures 5 and 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTA5N12, MTA5N15

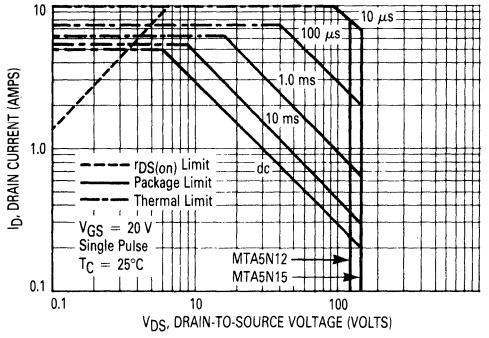
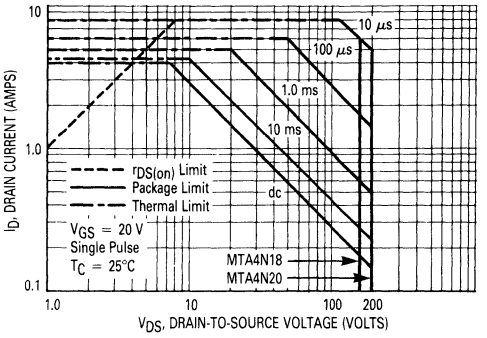


FIGURE 13 — MTA4N18, MTA4N20



FORWARD BIASED SAFE OPERATING AREA

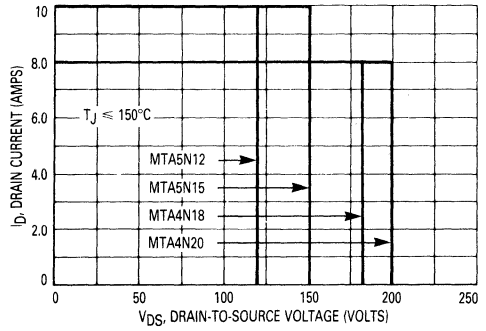
The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 12 and 13
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

TMOS SOURCE-TO-DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

C

FIGURE 15 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

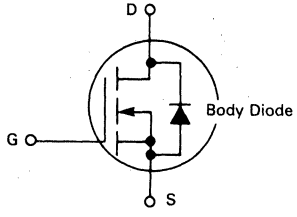


FIGURE 16 — DIODE SWITCHING WAVEFORM

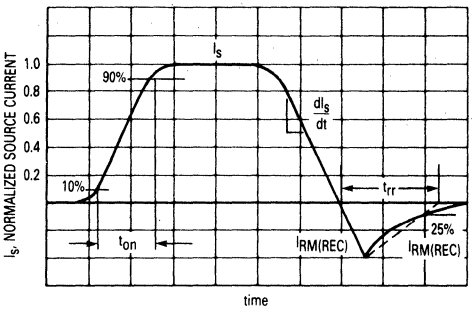
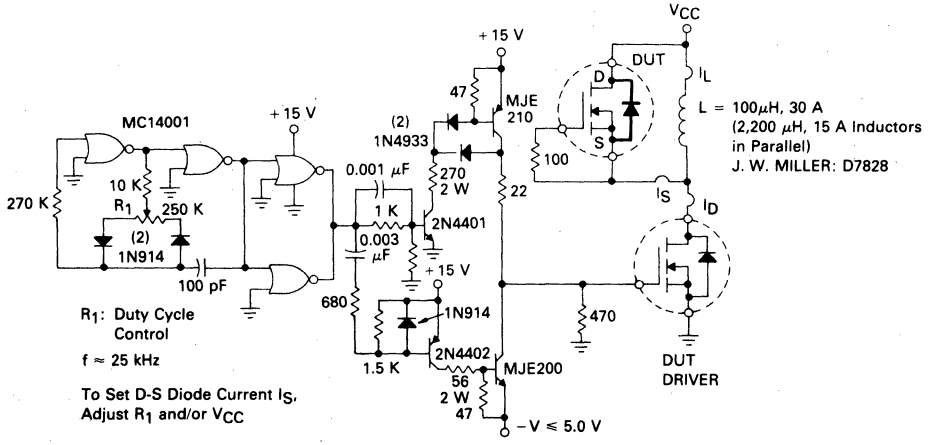


FIGURE 17 — TMOS DIODE SWITCHING TEST CIRCUIT



NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

MOTOROLA

MTA6N08
MTA6N10
MTA7N05
MTA7N06

Designer's Data Sheet

6.0 and 7.0 AMPERE

N-CHANNEL TMOS POWER FETs

$r_{DS(on)}$ = 0.6 OHM
80 and 100 VOLTS

$r_{DS(on)}$ = 0.4 OHM
50 and 60 VOLTS

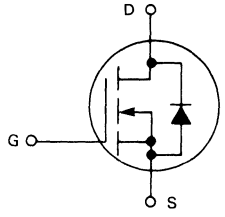
C

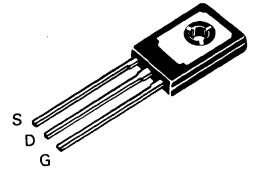
N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™





MAXIMUM RATINGS

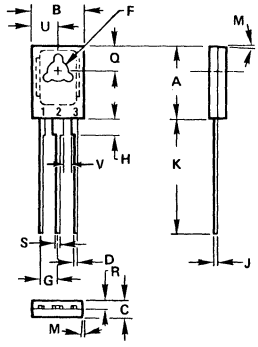
Rating	Symbol	MTA 7N05	MTA 7N06	MTA 6N08	MTA 6N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 7.0 14		 6.0 12		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.32				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	3.12	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 9:
PIN 1. GATE
2. DRAIN
3. SOURCE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTA7N05	$V_{BR(DSS)}$	50	—	Vdc
	MTA7N06		60	—	
	MTA6N08		80	—	
	MTA6N10		100	—	
Zero Gate Voltage Drain Current (V_{DSS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_C = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100 °C			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc)	MTA7N05/MTA7N06	$r_{DS(on)}$	—	0.4	Ohm
(V_{GS} = 10 Vdc, I_D = 3.0 Adc)	MTA6N08/MTA6N10		—	0.6	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 7.0 Adc)	MTA7N05/MTA7N06		—	3.4	
(I_D = 3.5 Adc, T_J = 100°C)	MTA7N05/MTA7N06		—	2.8	
(I_D = 6.0 Adc)	MTA6N08/MTA6N10		—	4.5	
(I_D = 3.0 Adc, T_C = 100°C)	MTA6N08/MTA6N10		—	3.6	
Forward Transconductance (V_{DS} = 15 V, I_D = 3.5 A)	MTA7N05/MTA7N06	g_{fs}	1.0	—	mhos
(V_{DS} = 15 V, I_D = 3.0 A)	MTA6N08/MTA6N10		1.0	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	—	300	pF
Output Capacitance		C_{oss}	—	160	
Reverse Transfer Capacitance		C_{rss}	—	50	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 1 and 2	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	25	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	50	

SOURCE-DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.5	Vdc
Forward Turn-On Time		t_{on}	150	ns
Reverse Recovery Time		t_{rr}	250	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

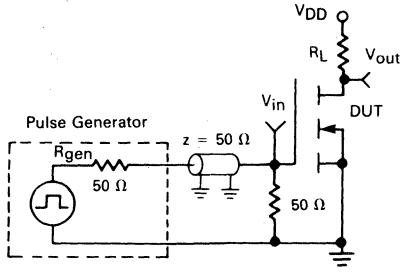
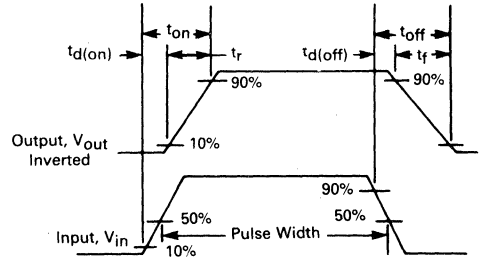


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

MTA7N05, MTA7N06

FIGURE 3 — ON-REGION CHARACTERISTICS

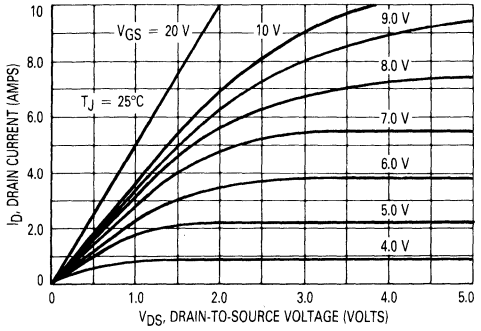


FIGURE 5 — TRANSFER CHARACTERISTICS

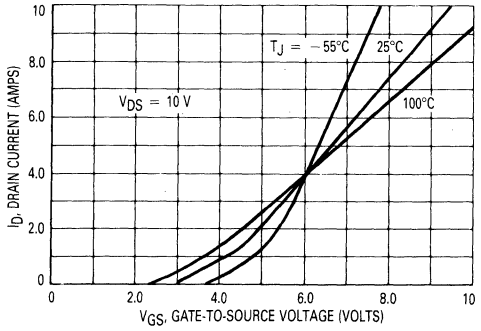
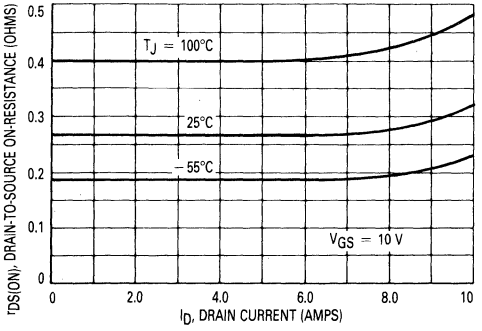


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT



MTA6N08, MTA6N10

FIGURE 4 — ON-REGION CHARACTERISTICS

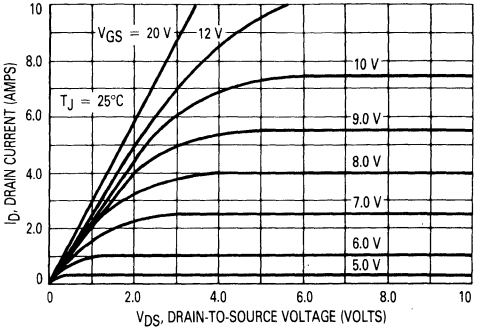


FIGURE 6 — TRANSFER CHARACTERISTICS

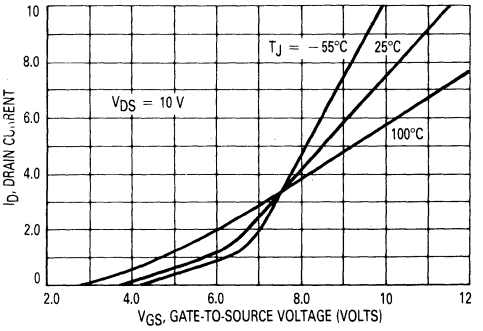
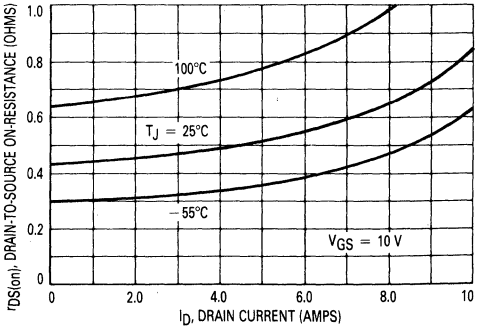


FIGURE 8 — ON-RESISTANCE versus DRAIN CURRENT



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TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

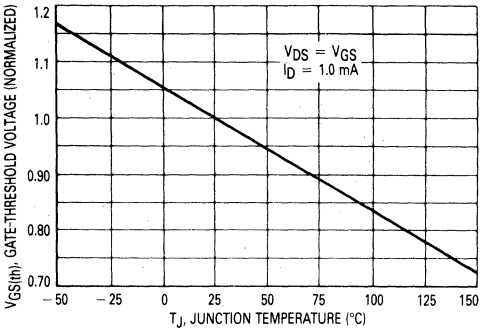


FIGURE 10 — CAPACITANCE VARIATION

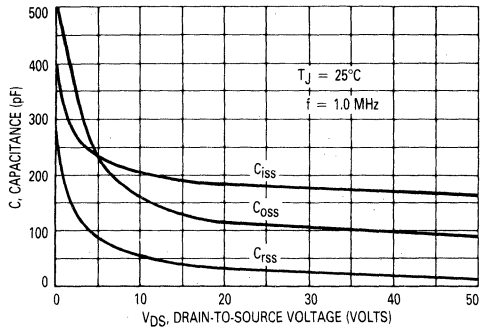
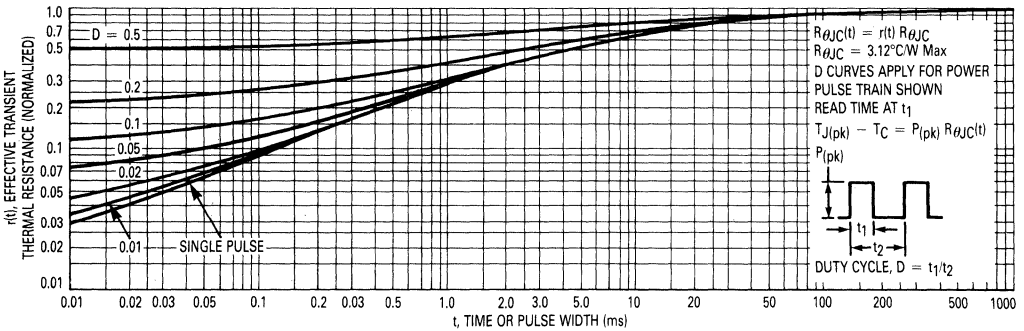


FIGURE 11 — THERMAL RESPONSE



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 0.5 Amp. (See Figures 5 and 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTA7N05, MTA7N06

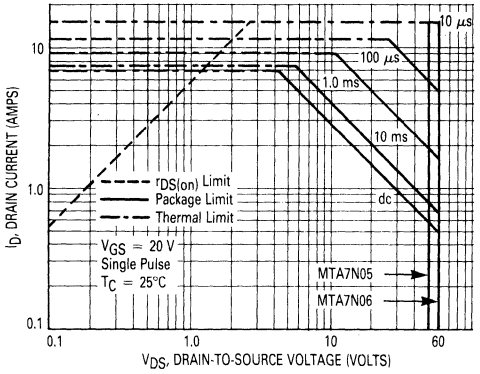
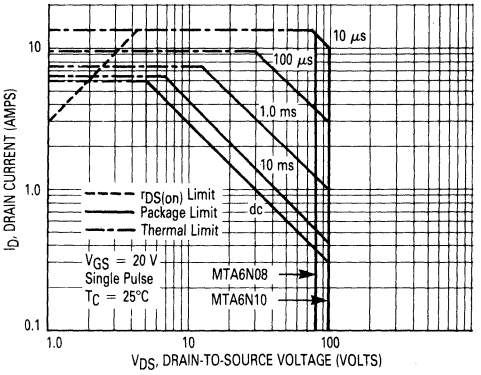


FIGURE 13 — MTA6N08, MTA6N10



FORWARD BIASED SAFE OPERATING AREA

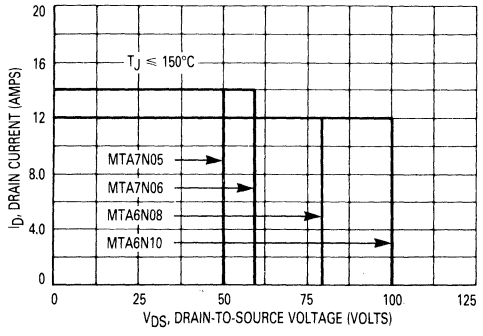
The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 12 and 13
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
$r(t)$ = normalized thermal response from Figure 11

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MTE60N18
MTE60N20
MTE65N12
MTE65N15

MOTOROLA

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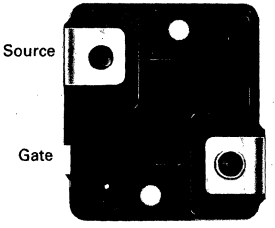
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTORS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- High di/dt Capability
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Multi-chip Construction Internally Decoupled

TMOS™



60 and 65 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.048 OHM
180 and 200 VOLTS

$r_{DS(on)}$ = 0.038 OHM
120 and 150 VOLTS

Designer's Data for "Worst-Case" Conditions

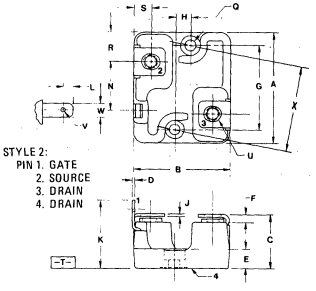
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst-case" design.

MAXIMUM RATINGS

Rating	Symbol	MTE 65N12	MTE 65N15	MTE 60N18	MTE 60N20	Unit
Drain-Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 65 200		 60 180		Adc
Turn-Off Rate of Change	di_D/dt	See Note 4 and Figure 18, in Considerations				A/μs
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 2.0				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−65 to +150				°C
Mounting Torque (To heat sink with 6–32 screw) (1)	τ(m)	8.0				in-lb
Lead Torque (Lead to bus with 5 mm screw) (2)	τ(l)	20				in-lb
Per Unit Weight	W	41				grams

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ B Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIMENSION: INCH EXCEPT FOR METRICALLY THREADED INSERTS.
5. MOUNTING HOLE CENTERS (DIMENSION X) SAME AS TO-204 (TO-3) FAMILY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	39.11	40.13	1.540	1.580
B	33.93	34.95	1.336	1.376
C	–	20.32	–	0.800
D	0.68	0.83	0.027	0.033
E	8.30	8.81	0.327	0.347
F	–	4.44	–	0.175
G	29.67 BSC		1.168 BSC	
H	5.08 BSC		0.200 BSC	
J	0.93	1.09	0.037	0.043
K	–	25.40	–	1.000
L	2.92	3.30	0.115	0.130
N	17.14	17.39	0.675	0.685
Q	3.73	3.88	0.147	0.153
R	10.41	10.79	0.410	0.425
S	5.84	6.35	0.230	0.250
U	M5 .8 (METRIC THRD)			
V	1.27	1.52	0.050	0.060
W	4.69	4.85	0.185	0.191
X	30.15 BSC		1.187 BSC	

CASE 353-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTE65N12	$V_{(BR)DSS}$	120	—	Vdc
	MTE65N15		150	—	
	MTE60N18		180	—	
	MTE60N20		200	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 32.5 Adc)	MTE65N12	$r_{DS(on)}$	—	0.038	Ohms
	MTE65N15				
(V_{GS} = 10 Vdc, I_D = 30 Adc)	MTE60N18		—	0.048	
	MTE60N20				
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 65 Adc)	MTE65N12		—	2.9	
	MTE65N15				
(I_D = 32.5 Adc, T_J = 100°C)	MTE65N12		—	2.2	
	MTE65N15				
(I_D = 60 Adc)	MTE60N18		—	3.2	
	MTE60N20				
(I_D = 30 Adc, T_J = 100°C)	MTE60N18		—	2.6	
	MTE60N20				
Forward Transconductance (V_{DS} = 15 V, I_D = 32.5 A)	MTE65N12	g_{fs}	16	—	mhos
	MTE65N15				
(V_{DS} = 15 V, I_D = 30 A)	MTE60N18		14	—	
	MTE60N20				
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	7000	pF
Output Capacitance		C_{oss}	—	3000	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* T_J = 100°C					
Inductive Load, Clamped — MTE65N12 and MTE65N15					
Turn-Off Delay Time	(V_{clamp} = 75 V, I_D = 32.5 A, V_{in} = 10 Vdc, R_{gen} = 50 Ω, L = 50 μH) See Figures 16 and 17.	t_{dv}	—	700	ns
Crossover Time		t_c	—	500	
Current Fall Time		t_{fi}	—	200	
Inductive Load, Clamped — MTE60N18 and MTE60N20					
Turn-Off Delay Time	(V_{clamp} = 75 V, I_D = 30 A V_{in} = 10 Vdc, R_{gen} = 50 Ω L = 50 μH) See Figures 16 and 17.	t_{dv}	—	700	ns
Crossover Time		t_c	—	300	
Current Fall Time		t_{fi}	—	100	

SOURCE-DRAIN DIODE CHARACTERISTICS*		Symbol	Typical	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0) See Figures 10 and 11.	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	50	ns
Reverse Recovery Time		t_{rr}	450	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

C

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 1 — MTE60N18, MTE60N20

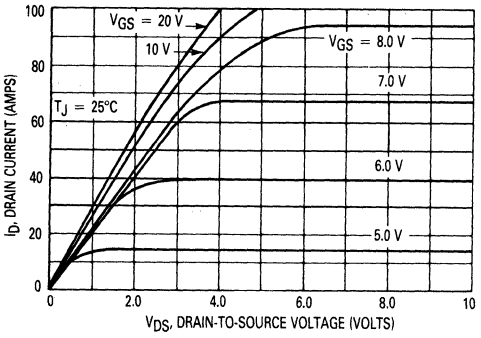
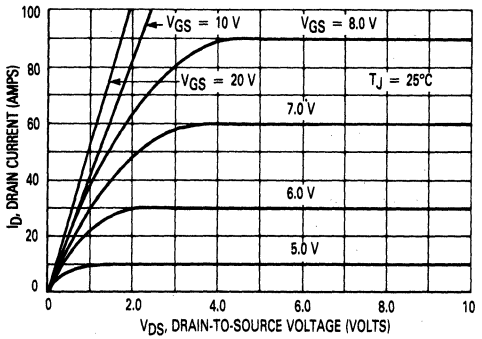


FIGURE 2 — MTE65N12, MTE65N15



TRANSFER CHARACTERISTICS

FIGURE 3 — MTE60N18, MTE60N20

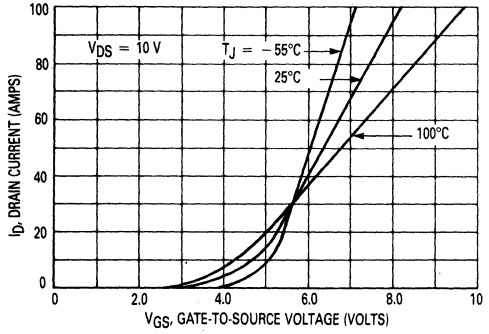
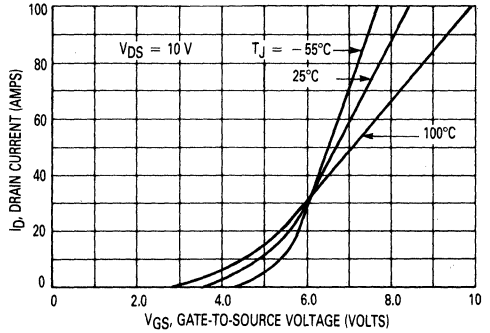


FIGURE 4 — MTE65N12, MTE65N15



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 5 — MTE60N18, MTE60N20

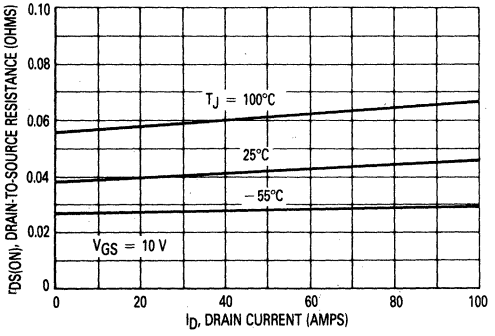
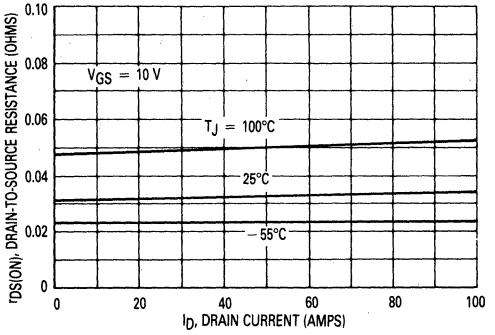


FIGURE 6 — MTE65N12, MTE65N15



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

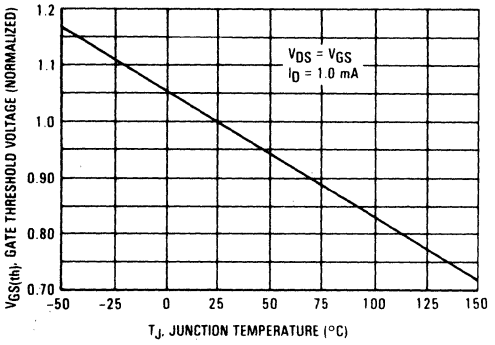
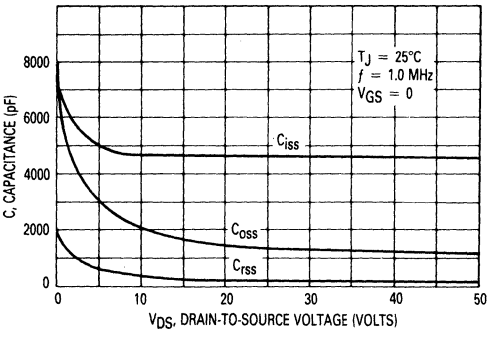


FIGURE 8 — CAPACITANCE VARIATION



TMOS SOURCE-TO-DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 9. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 9 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

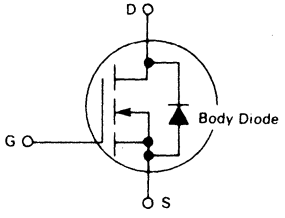


FIGURE 10 — DIODE SWITCHING WAVEFORM

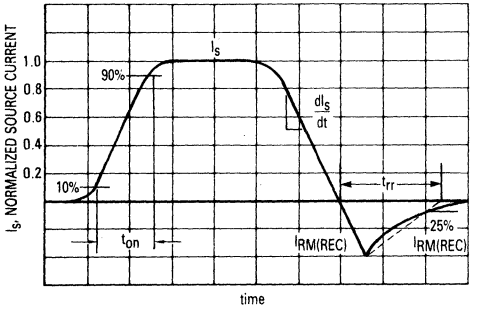
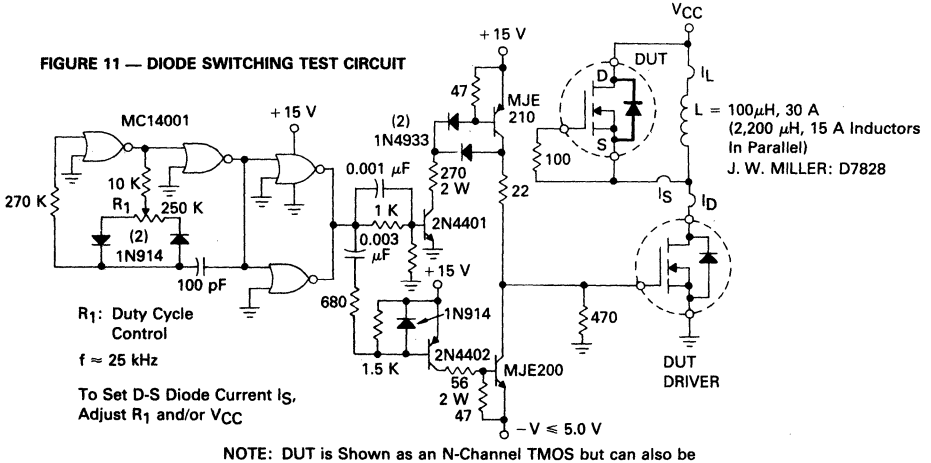


FIGURE 11 — DIODE SWITCHING TEST CIRCUIT



NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

C

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTE60N18, MTE60N20

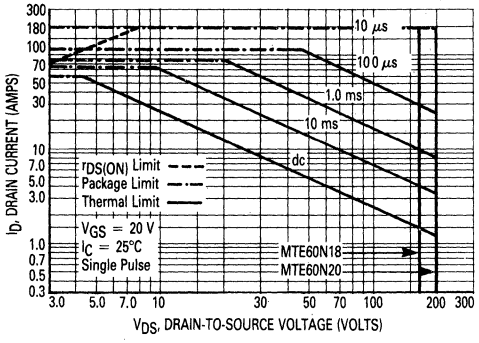


FIGURE 13 — MTE65N12, MTE65N15

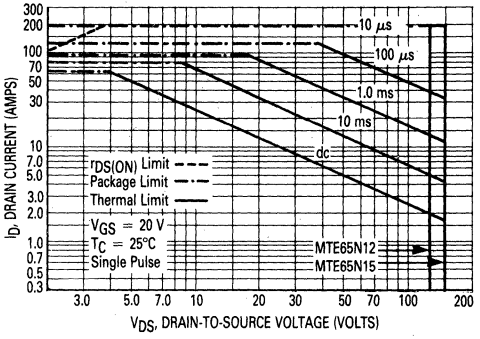


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

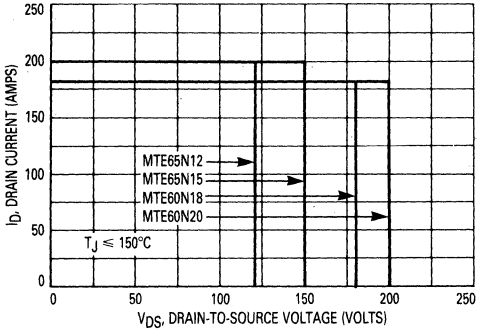
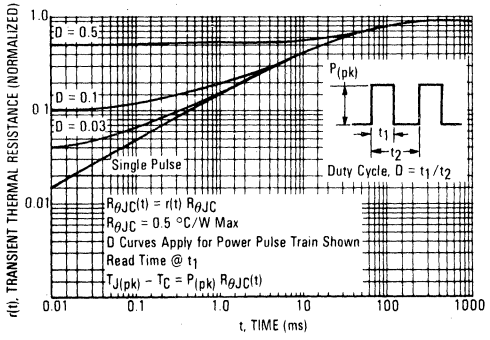


FIGURE 15 — THERMAL RESPONSE



GUARANTEED SAFE OPERATING AREA

The dc data presented in Figures 12 and 13 is for a single one second pulse, applied while maintaining the case temperature T_C at 25°C. For multiple pulses and case temperatures other than 25°C, the dc drain current at a case temperature of 25°C should be de-rated as follows:

$$I_{D(T)} = I_D\,(25°C)\left[\frac{150 - T_C}{P_D \cdot R_{\theta JC} \cdot r_{(t)}}\right]$$

where P_D is the maximum power rating at 25°C, $R_{\theta JC}$ is the junction-to-case thermal resistance, and $r_{(t)}$ is the normalized thermal response from Figure 15, corresponding to the appropriate pulse width and duty cycle.

EXAMPLE: Determine the maximum allowable drain current for an MTE60N18 at 25 volts drain voltage, with a pulse width of 10 ms and duty cycle of 50%, at a case temperature of 80°C.

From Figure 13, the dc drain current at V_{DS} = 25 volts is 10 A. For a 10 ms pulse and duty cycle of 50%, Figure 15 gives an $r_{(t)}$ of 0.6; then, with P_D = 250 watts at 25°C and $R_{\theta JC}$ = 0.5 °C/W.

$$I_D = 10 \times \frac{150 - 80}{250 \times 0.5 \times 0.6} = 9.33\ A$$

The switching safe operating area in Figure 14 is the boundary that the load line may traverse without incurring damage to the device. The fundamental limits are the maximum rated peak drain current I_{DM}, the minimum drain-to-source breakdown voltage $V_{BR(DSS)}$ and the maximum rated junction temperature. The boundaries are applicable for both turn-on and turn-off of the devices for rise and fall times of less than one microsecond.

FIGURE 16 — INDUCTIVE LOAD SWITCHING CIRCUIT

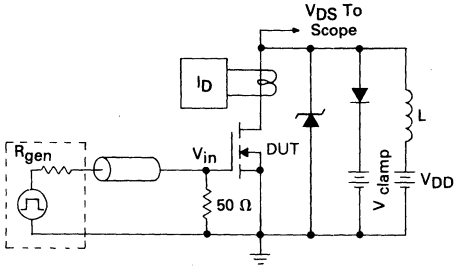
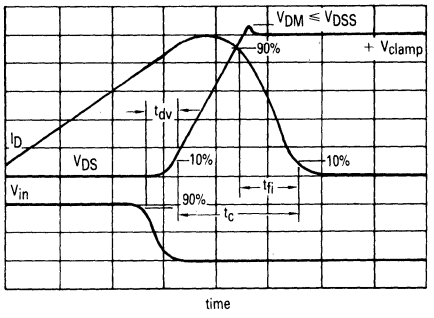


FIGURE 17 — CLAMPED INDUCTIVE LOAD SWITCHING WAFEFORMS



CONSIDERATION IN DESIGNING WITH POWER MOSFETS

Depending on the frequency of operation, certain precautions must be taken to insure optimum reliability. When switching near the device maximum frequency, the high current and very fast switching capability of this device necessitates the use of the following protective measures:

Note 1 As in any wideband circuit, good RF layout techniques must be maintained, i.e., short lead lengths, adequate ground planes and decoupled power supplies.

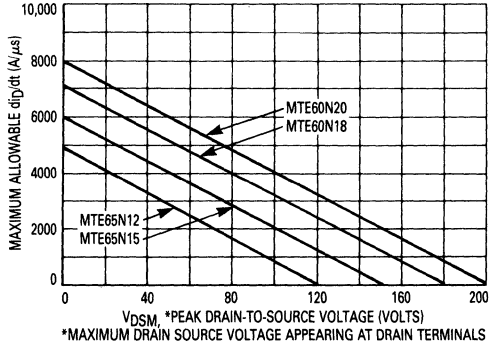
Note 2 All overvoltage protection circuitry — free wheeling diodes, zeners, MOVs, snubber networks — should be placed directly between the drain-source or between the drain and a good, low inductance ac ground.

Note 3 Since most "real world" loads are inductive, the fast turn-off peak flyback voltage (e = L di/dt) must not exceed the $V_{BR(DSS)}$ rating, an instantaneous voltage limit. The protective circuitry, including parasitics, must have response times commensurate with the Power MOSFET switching speed, e.g., rectifiers must have very short recovery times. The forward recovery time t_{fr}, overshoot voltage $V_{FM(DYN)}$ and reverse recovery time t_{rr} should be low to minimize the switching stress on the transistor.

Note 4 Even with good RF layout and ideal clamping below the maximum $V_{(BR)DSS}$ of the device, significant potentials may be generated across the package drain and source parasitic inductances during rapid turn off of a large magnitude of current. These induced voltages which are internal to the package add to the clamp voltage. Therefore, to protect the chips from excessive voltage, the di_D/dt must be limited in accordance to the peak voltage seen across the terminals of the device. The *MAXIMUM ALLOWABLE* di_D/dt must be limited in accordance to the peak V_{DS} appearing at the device terminals as shown in Figure 18.

For applications requiring slower switching speeds, increasing the gate drive impedance will increase the switching times. This can be accomplished by adding a resistor in series with the gate.

FIGURE 18 — MAXIMUM ALLOWABLE di_D/dt versus PEAK DRAIN-TO-SOURCE VOLTAGE



*MAXIMUM DRAIN SOURCE VOLTAGE APPEARING AT DRAIN TERMINALS

MTE75N08
MTE75N10
MTE100N05
MTE100N06

MOTOROLA

C

Designer's Data Sheet

75 and 100 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.028 OHM
80 and 100 VOLTS

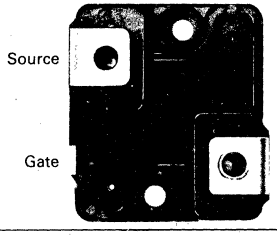
$r_{DS(on)}$ = 0.018 OHM
50 and 60 VOLTS

ENERGY MANAGEMENT SERIES
N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTORS

These TMOS Power FETs are designed for high current, high speed power switching applications such as switching regulators, converters, and motor controls.

- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- High di/dt Capability
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Multi-chip Construction Internally Decoupled

TMOS™



Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst-case" design.

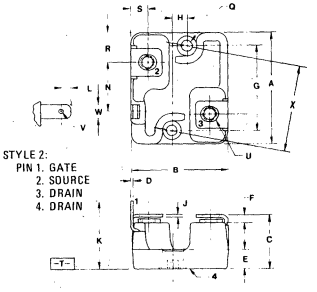
MAXIMUM RATINGS

Rating	Symbol	MTE 100N05	MTE 100N06	MTE 75N08	MTE 75N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current						Adc
Continuous	I_D	100		75		
Pulsed	I_{DM}	500		400		
Turn-Off Rate of Change	di_D/dt	See Note 4 and Figure 18 in Considerations				A/μs
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C	P_D	250				Watts
Derate above 25°C		2.0				W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150				°C
Mounting Torque (To heat sink with 6–32 screw) (1)	τ(m)	8.0				in-lb
Lead Torque (Lead to bus with 5 mm screw) (2)	τ(l)	20				in-lb
Per Unit Weight	W	41				grams

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1" from case for 5 seconds	T_L	275	°C

1. A Belleville washer of 0.281" O.D., 0.138" I.D., 0.013" thick and 43 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.50".



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ ⌀ 0.25 (0.010) Ⓜ T Ⓐ Ⓜ B Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIMENSION: INCH EXCEPT FOR METRICALLY THREADED INSERTS.
5. MOUNTING HOLE CENTERS (DIMENSION X) SAME AS TO-204 (TO-3) FAMILY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	39.11	40.13	1.540	1.580
B	33.93	34.95	1.336	1.376
C	–	20.32	–	0.800
D	0.68	0.83	0.027	0.033
E	8.30	8.81	0.327	0.347
F	–	4.44	–	0.175
G	29.67 BSC		1.168 BSC	
H	5.08 BSC		0.200 BSC	
J	0.93	1.09	0.037	0.043
K	–	25.40	–	1.000
L	2.92	3.30	0.115	0.130
N	17.14	17.39	0.675	0.685
Q	3.73	3.88	0.147	0.153
R	10.41	10.79	0.410	0.425
S	5.84	6.35	0.230	0.250
U	M5 .8 (METRIC THRD)			
V	1.27	1.52	0.050	0.060
W	4.69	4.85	0.185	0.191
X	30.15 BSC		1.187 BSC	

CASE 353-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTE100N05	$V_{(BR)DSS}$	50	—	Vdc
	MTE100N06		60	—	
	MTE75N08		80	—	
	MTE75N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 50 Adc)	MTE100N05 MTE100N06	$r_{DS(on)}$	—	0.018	Ohms
(V_{GS} = 10 Vdc, I_D = 37.5 Adc)	MTE75N08 MTE75N10		—	0.028	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 100 Adc)	MTE100N05 MTE100N06		—	2.10	
(I_D = 50 Adc, T_J = 100°C)	MTE100N05 MTE100N06		—	1.70	
(I_D = 75 Adc)	MTE75N08 MTE75N10		—	2.25	
(I_D = 37.5 Adc, T_J = 100°C)	MTE75N08 MTE75N10		—	1.88	
Forward Transconductance (V_{DS} = 15 V, I_D = 50 A)	MTE100N05 MTE100N06	g_{fs}	18	—	mhos
(V_{DS} = 15 V, I_D = 37.5 A)	MTE75N08 MTE75N10		16	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	6000	pF
Output Capacitance		C_{oss}	—	4500	
Reverse Transfer Capacitance		C_{rss}	—	1200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Inductive Load, Clamped — MTE100N05 and MTE100N06					
Turn-Off Delay Time	(V_{clamp} = 25 Vdc, I_D = 50 Adc	t_{dv}	—	700	ns
Crossover Time	L = 50 μH, V_{in} = 10 Vdc	t_c	—	900	
Current Fall Time	R_{gen} = 50 Ω) See Figures 16 and 17	t_{fi}	—	200	
Inductive Load, Clamped — MTE75N08 and MTE75N10					
Turn-Off Delay Time	(V_{clamp} = 25 Vdc, I_D = 37.5 Adc	t_{dv}	—	700	ns
Crossover Time	L = 50 μH, V_{in} = 10 Vdc	t_c	—	600	
Current Fall Time	R_{gen} = 50 Ω) See Figures 16 and 17	t_{fi}	—	200	
SOURCE-DRAIN DIODE CHARACTERISTICS*			**Symbol**	**Typical**	**Unit**
Forward On Voltage	(I_S = Rated I_D, V_{GS} = 0)		V_{SD}	1.9	Vdc
Forward Turn-On Time			t_{on}	50	ns
Reverse Recovery Time			t_{rr}	450	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

C

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 1 — MTE75N08, MTE75N10

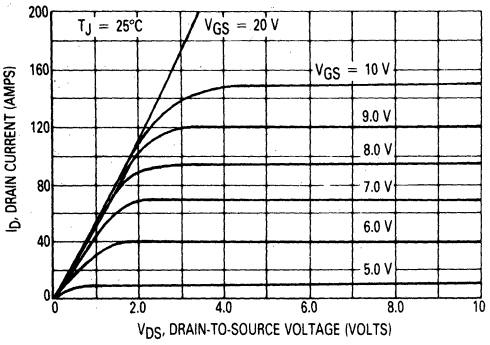
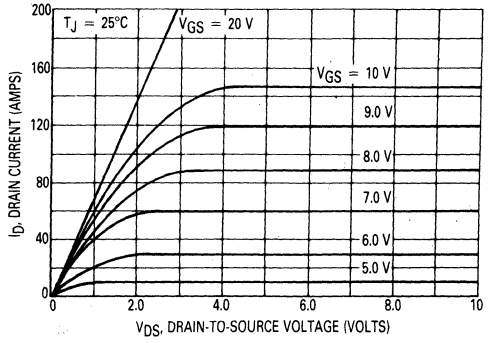


FIGURE 2 — MTE100N05, MTE100N06



TRANSFER CHARACTERISTICS

FIGURE 3 — MTE75N08, MTE75N10

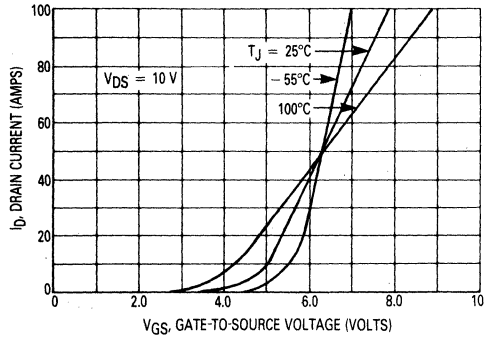
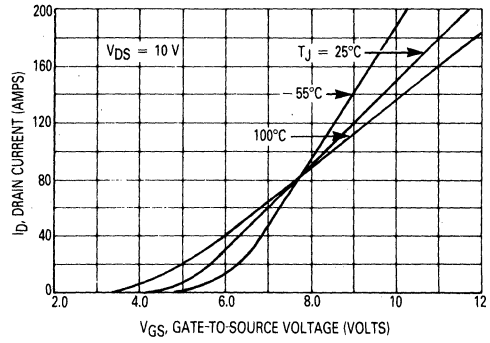


FIGURE 4 — MTE100N05, MTE100N06



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 5 — MTE75N08, MTE75N10

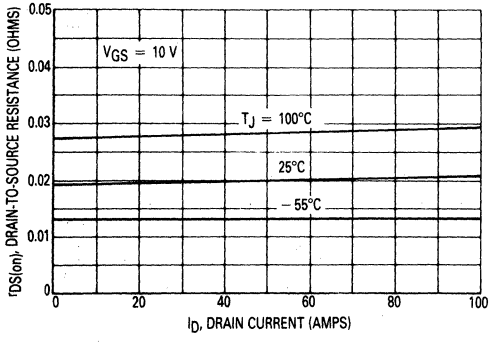
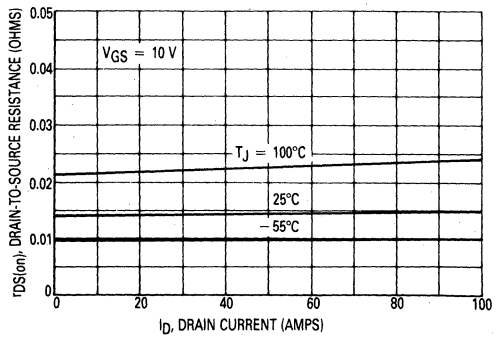


FIGURE 6 — MTE100N05, MTE100N06



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

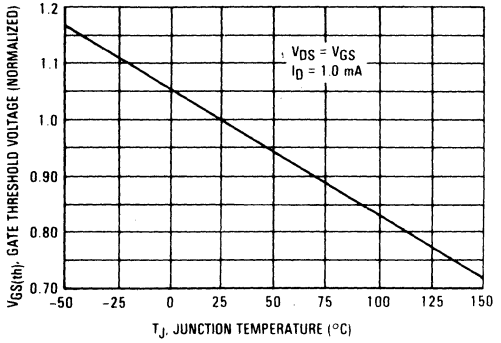
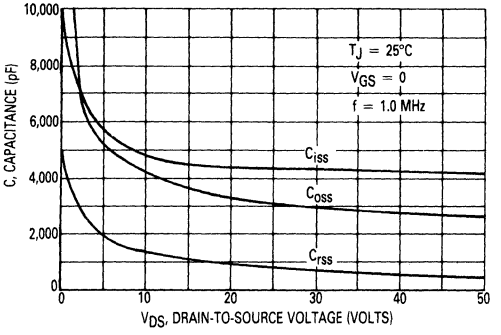


FIGURE 8 — CAPACITANCE VARIATION



C

TMOS SOURCE-TO-DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 9. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 9 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

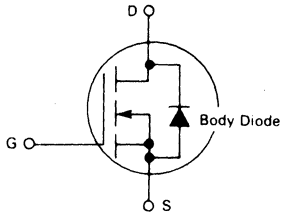


FIGURE 10 — DIODE SWITCHING WAVEFORM

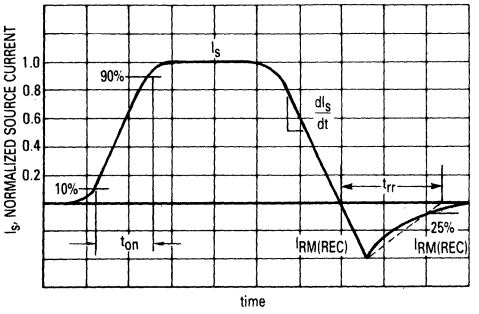
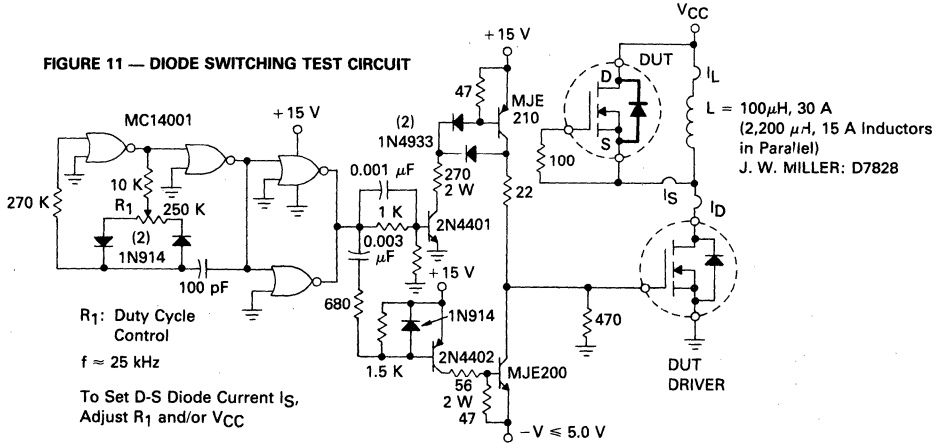


FIGURE 11 — DIODE SWITCHING TEST CIRCUIT



NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

C

SAFE OPERATING AREA INFORMATION
MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTE75N08, MTE75N10

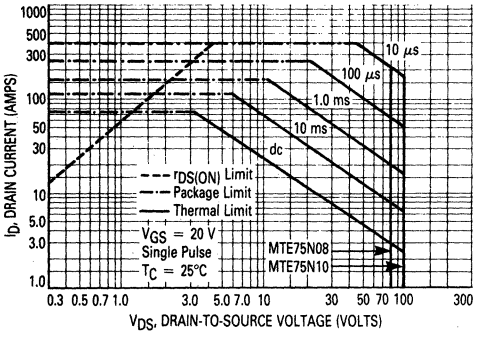


FIGURE 13 — MTE100N05, MTE100N06

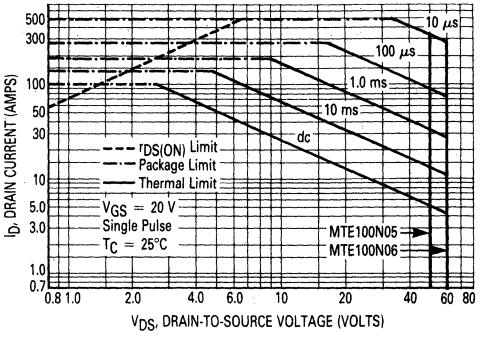


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

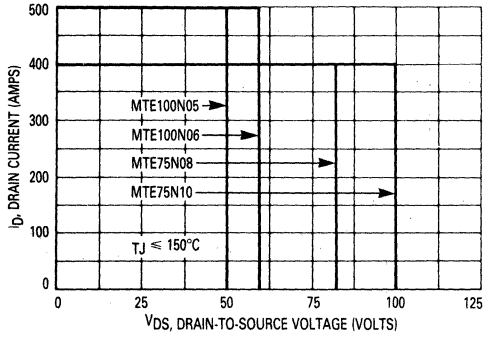
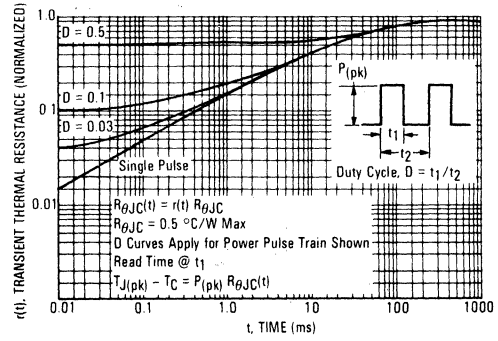


FIGURE 15 — THERMAL RESPONSE



GUARANTEED SAFE OPERATING AREA

The dc data presented in Figures 12 and 13 is for a single one second pulse, applied while maintaining the case temperature T_C at 25°C. For multiple pulses and case temperatures other than 25°C, the dc drain current at a case temperature of 25°C should be de-rated as follows:

$$I_{D(T)} = I_{D\ (25°)} \left[\frac{150 - T_C}{P_D \cdot R_{\theta JC} \cdot r_{(t)}} \right]$$

where P_D is the maximum power rating at 25°C, $R_{\theta JC}$ is the junction-to case thermal resistance, and $r_{(t)}$ is the normalized thermal response from Figure 15, corresponding to the appropriate pulse width and duty cycle.

EXAMPLE: Determine the maximum allowable drain current for an MTE100N05 at 25 volts drain voltage, with a pulse width of 10 ms and duty cycle of 50%, at a case temperature of 80°C.

From Figure 13, the dc drain current at V_{DS} = 25 volts is 10 A. For a 10 ms pulse and duty cycle of 50%, Figure 15 gives an $r_{(t)}$ of 0.6; then, with P_D = 250 watts at 25°C and $R_{\theta JC}$ = 0.5°C/W

$$I_D = 10 \times \frac{150 - 80}{250 \times 0.5 \times 0.6} = 9.33\ A$$

The switching safe operating area in Figure 14 is the boundary that the load line may traverse without incurring damage to the device. The fundamental limits are the maximum rated peak drain current I_{DM}, the minimum drain-to-source breakdown voltage $V_{BR(DSS)}$ and the maximum rated junction temperature. The boundaries are applicable for both turn-on and turn-off of the devices for rise and fall times of less than one microsecond.

FIGURE 16 — INDUCTIVE LOAD SWITCHING CIRCUIT

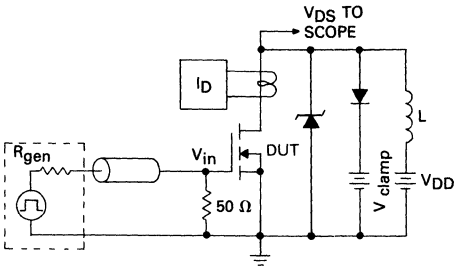
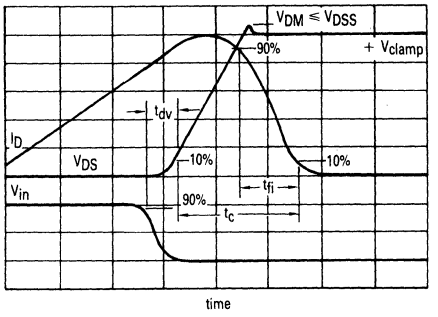


FIGURE 17 — CLAMPED INDUCTIVE LOAD SWITCHING WAFEFORMS



CONSIDERATION IN DESIGNING WITH POWER MOSFETS

Depending on the frequency of operation, certain precautions must be taken to insure optimum reliability. When switching near the device maximum frequency, the high current and very fast switching capability of this device necessitates the use of the following protective measures:

Note 1 As in any wideband circuit, good RF layout techniques must be maintained, i.e., short lead lengths, adequate ground planes and decoupled power supplies.

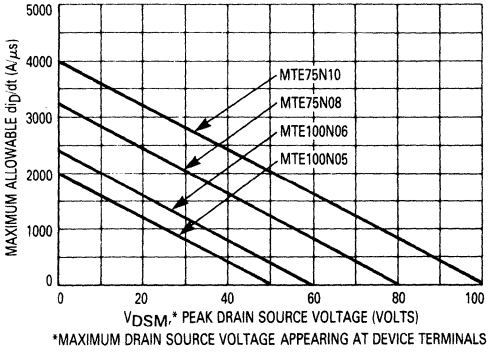
Note 2 All overvoltage protection circuitry — free wheeling diodes, zeners, MOVs, snubber networks — should be placed directly between the drain-source or between the drain and a good, low inductance ac ground.

Note 3 Since most "real world" loads are inductive, the fast turn-off peak flyback voltage (e = L di/dt) must not exceed the $V_{BR(DSS)}$ rating, an instantaneous voltage limit. The protective circuitry, including parasitics, must have response times commensurate with the Power MOSFET switching speed, e.g., rectifiers must have very short recovery times. The forward recovery time t_{fr}, overshoot voltage $V_{FM(DYN)}$ and reverse recovery time t_{rr} should be low to minimize the switching stress on the transistor.

Note 4 Even with good RF layout and ideal clamping below the maximum $V_{(BR)DSS}$ of the device, significant potentials may be generated across the package drain and source parasitic inductances during rapid turn off of a large magnitude of current. These induced voltages which are internal to the package add to the clamp voltage. Therefore, to protect the chips from excessive voltage, the di_D/dt must be limited in accordance to the peak voltage seen across the terminals of the device. The *MAXIMUM ALLOWABLE* di_D/dt must be limited in accordance to the peak V_{DS} appearing at the device terminals as shown in Figure 18.

For applications requiring slower switching speeds, increasing the gate drive impedance will increase the switching times. This can be accomplished by adding a resistor in series with the gate.

FIGURE 18 — MAXIMUM ALLOWABLE di_D/dt versus PEAK DRAIN SOURCE VOLTAGE



*MAXIMUM DRAIN SOURCE VOLTAGE APPEARING AT DEVICE TERMINALS

MTE120N18
MTE120N20
MTE130N12
MTE130N15

MOTOROLA

C

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTORS

These TMOS Power FETs are designed for high current, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- High di/dt Capability
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Multi-chip Construction Internally Decoupled

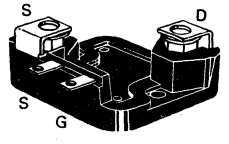
TMOS™

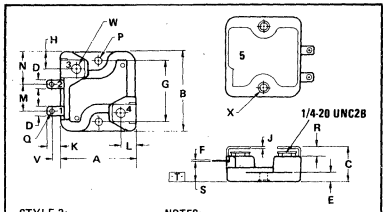
120 and 130 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.020 OHM
120 and 150 VOLTS

$r_{DS(on)}$ = 0.024 OHM
180 and 200 VOLTS





STYLE 2:
PIN 1. GATE
2. SOURCE
3. SOURCE
4. DRAIN
5. DRAIN

NOTES:
1. DIMENSION A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ ⌀ 0.36 (0.014)Ⓜ T AⓂ BⓂ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	–	26.67	–	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01
MO-040AA

MAXIMUM RATINGS

Rating	Symbol	MTE 130N12	130N15	120N18	120N20	Unit
Drain-Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	I_D I_{DM}	130 500		120 400		Adc
Turn-Off Rate of Change	di_D/dt	See Note 4 and Fig. 18 in Considerations				A/μs
Gate Current — Pulsed	I_{GM}	2.0				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	500 4.0				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150				°C
Mounting Torque (To heat sink with 10-32 screw)(1)	τ(m)	20				in-lb
Lead Torque (Lead to bus with ¼-20 screw)(2)	τ(l)	20				in-lb
Per Unit Weight	W	120				grams

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.25	°C/W
Maximum Lead Temp. for Soldering Purposes, ⅛" from case for 5 seconds	T_L	275	°C

1. A Belleville washer of 0.472" O.D., 0.205" I.D., 0.024" thick and 150 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.75".

0.003" thick mica insulator available as a separate item. Motorola P/N 48ASB12387B001

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$			Vdc
(V_{GS} = 0, I_D = 5.0 mA)	MTE130N12		120	—	
	MTE130N15		150	—	
	MTE120N18		180	—	
	MTE120N20		200	—	
Zero Gate Voltage Drain Current		I_{DSS}			mAdc
(V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)			—	0.25	
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current		I_{GSS}	—	500	nAdc
(V_{GS} = 20 Vdc, V_{DS} = 0)					
ON CHARACTERISTICS*					
Gate Threshold Voltage		$V_{GS(th)}$			Vdc
(I_D = 1.0 mA, V_{DS} = V_{GS})			2.0	4.5	
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance		$r_{DS(on)}$			Ohms
(V_{GS} = 10 Vdc, I_D = 65 Adc)	MTE130N12			0.020	
	MTE130N15				
(V_{GS} = 10 Vdc, I_D = 60 Adc)	MTE120N18			0.024	
	MTE120N20				
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 130 Adc)	MTE130N12		—	3.1	
	MTE130N15				
(I_D = 65 Adc, T_J = 100°C)	MTE130N12		—	2.6	
	MTE130N15				
(I_D = 120 Adc)	MTE120N18		—	3.4	
	MTE120N20				
(I_D = 60 Adc, T_J = 100°C)	MTE120N18		—	2.9	
	MTE120N20				
Forward Transconductance		g_{fs}			mhos
(V_{DS} = 15 V, I_D = 65 A)	MTE130N12		35	—	
	MTE130N15				
(V_{DS} = 15 V, I_D = 60 A)	MTE120N18		35	—	
	MTE120N20				
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	18,000	pF
Output Capacitance		C_{oss}	—	10,000	
Reverse Transfer Capacitance		C_{rss}	—	4,000	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Inductive Load, Clamped — MTE130N12 and MTE130N15					
Turn-Off Delay Time	(V_{clamp} = 25 Vdc, I_D = 65 Adc	t_{dv}	—	1,400	ns
Crossover Time	L = 25 μH, V_{GS} = 10 Vdc	t_c	—	1,000	
Current Fall Time	R_{gen} = 50 Ω) See Figures 16 and 17	t_{fi}	—	400	
Inductive Load, Clamped — MTE120N18 and MTE120N20					
Turn-Off Delay Time	(V_{clamp} = 25 Vdc, I_D = 60 Adc	t_{dv}	—	1,400	ns
Crossover Time	L = 25 μH, V_{GS} = 10 Vdc	t_c	—	600	
Current Fall Time	R_{gen} = 50 Ω) See Figures 16 and 17	t_{fi}	—	200	
SOURCE-DRAIN DIODE CHARACTERISTICS*			**Symbol**	**Typical**	**Unit**
Forward On Voltage	(I_S = Rated I_D, V_{GS} = 0)		V_{SD}	2.0	Vdc
Forward Turn-On Time			t_{on}	50	ns
Reverse Recovery Time			t_{rr}	450	ns

*Pulses Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

C

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 1 — MTE120N18, MTE120N20

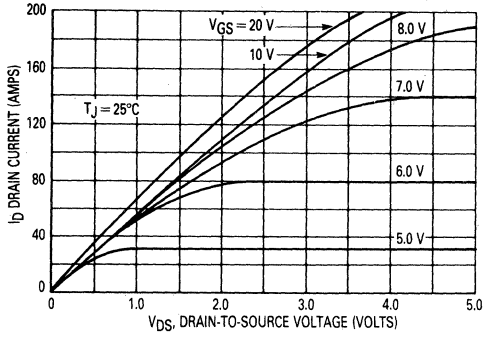
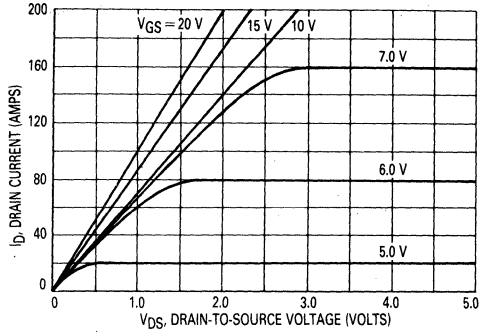


FIGURE 2 — MTE130N15, MTE130N15



TRANSFER CHARACTERISTICS

FIGURE 3 — MTE120N18, MTE120N20

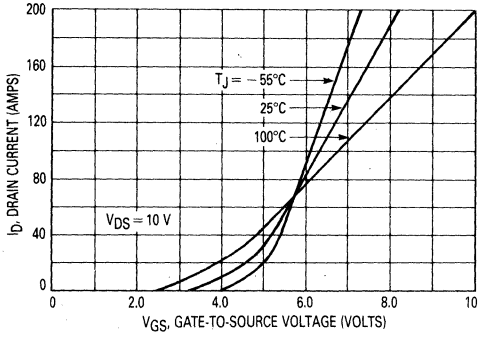
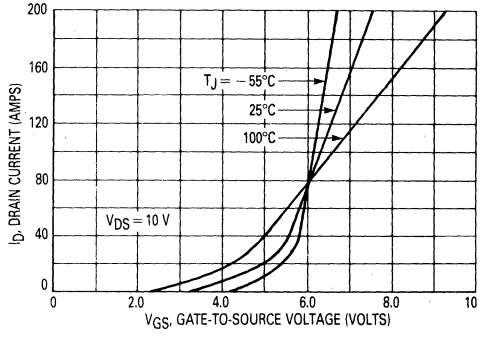


FIGURE 4 — MTE130N12, MTE130N15



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 5 — MTE120N18, MTE120N20

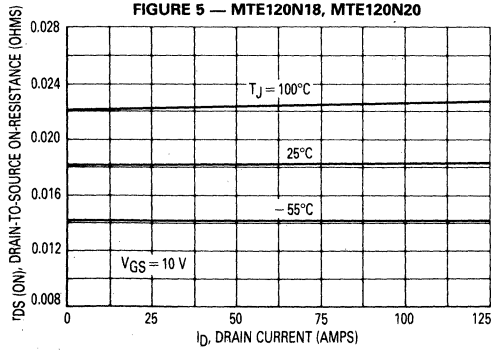
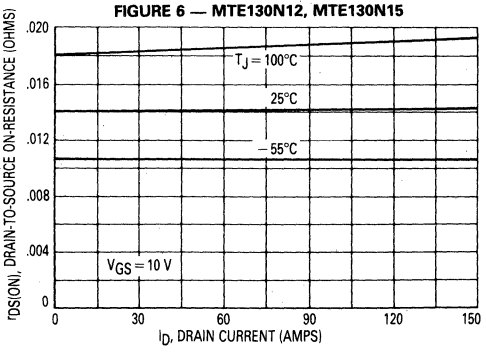


FIGURE 6 — MTE130N12, MTE130N15



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

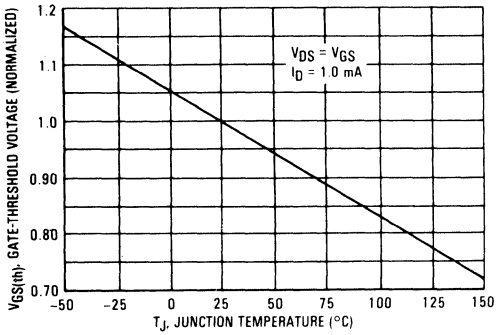
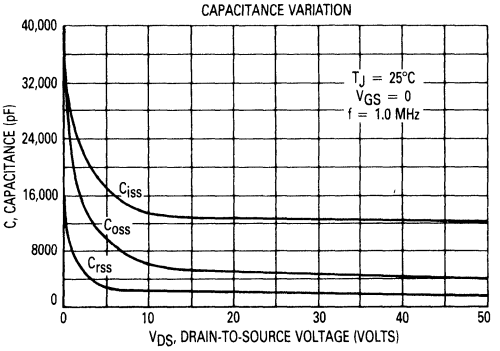


FIGURE 8 — CAPACITANCE VARIATION



TMOS SOURCE-TO-DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 9. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on-voltage, forward turn-on and reverse recovery times are given.

FIGURE 9 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

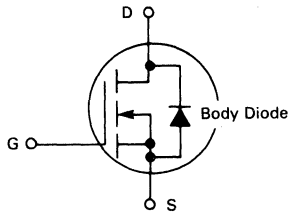


FIGURE 10 — DIODE SWITCHING WAVEFORM

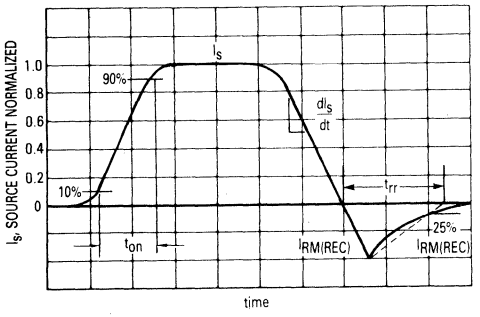
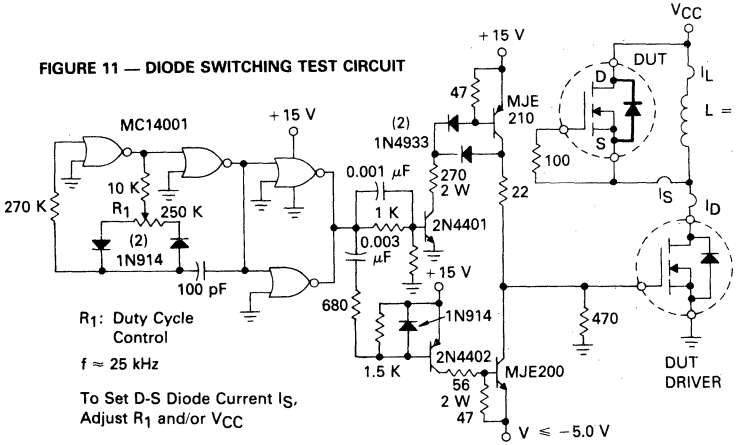


FIGURE 11 — DIODE SWITCHING TEST CIRCUIT



NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

C

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTE120N18, MTE120N20

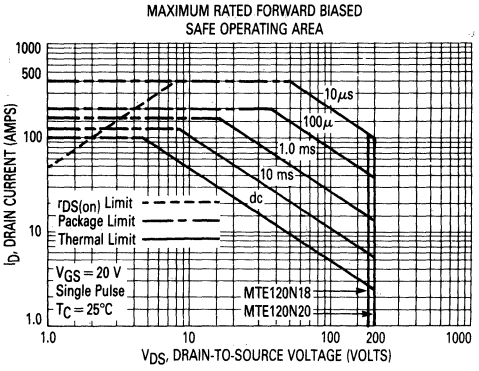


FIGURE 13 — MTE120N12, MTE130N15

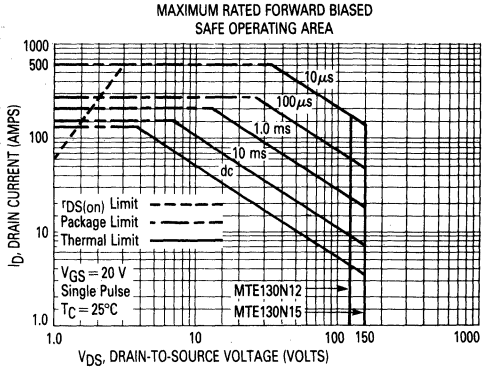


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

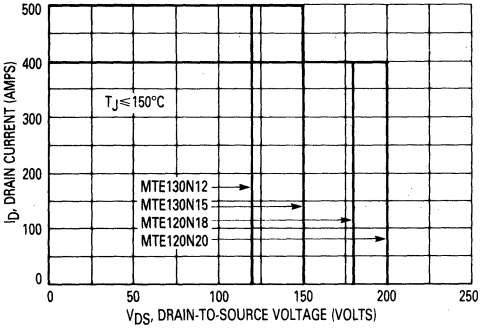
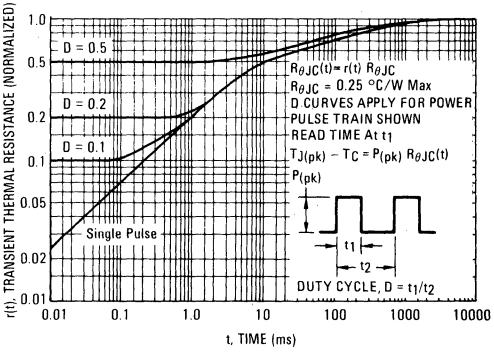


FIGURE 15 — THERMAL RESPONSE



GUARANTEED SAFE OPERATING AREA

The dc data presented in Figures 12 and 13 is for a single 1-second pulse, applied while maintaining the case temperature T_C at 25°C. For multiple pulses and case temperatures other than 25°C, the dc drain current at a case temperature of 25°C should be de-rated as follows:

$$I_{D(T)} = I_{D\ (25°)} \left[\frac{150 - T_C}{P_D \cdot R_{\theta JC} \cdot r_{(t)}} \right]$$

where P_D is the maximum power rating at 25°C, $R_{\theta JC}$ is the junction-to case thermal resistance, and $r_{(t)}$ is the normalized thermal response from Figure 15, corresponding to the appropriate pulse width and duty cycle.

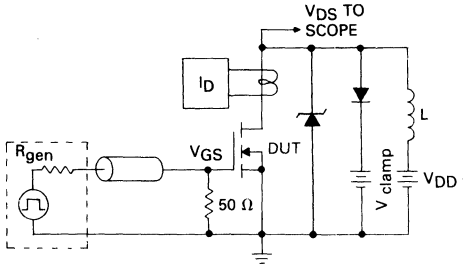
EXAMPLE: Determine the maximum allowable drain current for an MTE120N20 at 25 volts drain voltage, with a pulse width of 10 ms and duty cycle of 50%, at a case temperature of 80°C.

From Figure 12, the dc drain current at V_{DS} = 25 volts is 40 A. For a 10 ms pulse and duty cycle of 50%, Figure 15 gives an $r_{(t)}$ of 0.6; then, with P_D = 500 watts at 25°C and $R_{\theta JC}$ = 0.25°C/W

$$I_D = 40 \times \frac{150 - 80}{500 \times .25 \times 0.6} = 37.33\ A$$

The switching safe operating area in Figure 14 is the boundary that the load line may traverse without incurring damage to the device. The fundamental limits are the maximum rated peak drain current I_{DM}, the minimum drain-to-source breakdown voltage $V_{BR(DSS)}$ and the maximum rated junction temperature. The boundaries are applicable for both turn-on and turn-off of the devices for rise and fall times of less than one microsecond.

FIGURE 16 — INDUCTIVE LOAD SWITCHING CIRCUIT



CONSIDERATIONS IN DESIGNING WITH POWER MOSFETS

Depending on the frequency of operation, certain precautions must be taken to insure optimum reliability. When switching near the device maximum frequency, the high current and very fast switching capability of this device necessitates the use of the following protective measures:

Note 1 As in any wideband circuit, good RF layout techniques must be maintained, i.e., short lead lengths, adequate ground planes and decoupled power supplies.

Note 2 All overvoltage protection circuitry — free wheeling diodes, zeners, MOVs, snubber networks — should be placed directly between the drain-source or between the drain and a good, low inductance ac ground.

FIGURE 18 — MAXIMUM ALLOWABLE di_D/dt versus PEAK DRAIN SOURCE VOLTAGE

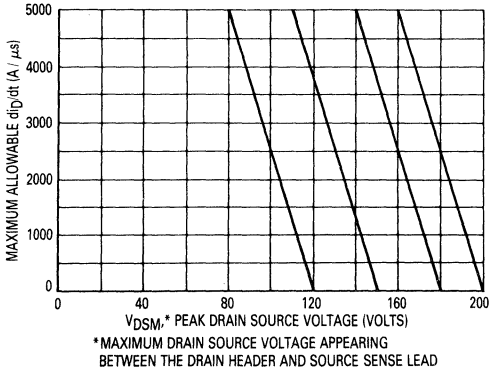
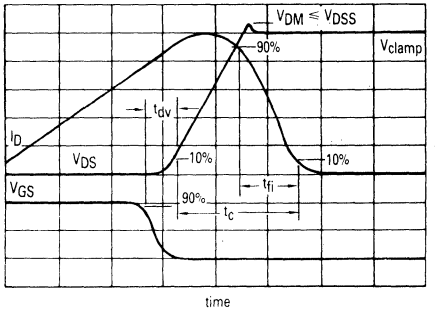


FIGURE 17 — CLAMPED INDUCTIVE LOAD SWITCHING WAFEFORMS



Note 3 Since most "real world" loads are inductive, the fast turn-off peak flyback voltage ($e = L\ di/dt$) must not exceed the $V_{BR(DSS)}$ rating, an instantaneous voltage limit. The protective circuitry, including parasitics, must have response times commensurate with the Power MOSFET switching speed, e.g., rectifiers must have very short recovery times. The forward recovery time t_{fr}, overshoot voltage $V_{FM(DYN)}$ and reverse recovery time t_{rr} should be low to minimize the switching stress on the transistor.

Note 4 Even with good RF layout and ideal clamping below the maximum $V_{(BR)DSS}$ of the device, significant potentials may be generated across the package drain and source parasitic inductances during rapid turn off of a large magnitude of current. These induced voltages, which are internal to the package, add to the clamp voltage.

Monitoring V_{DS} by observing the potential that appears across the drain header (package heat sink) and the source sense terminal gives the best indication of the potential appearing at the chip. Due to the source and drain bus inductances, sensing V_{DS} across the drain and source terminals may yield a significantly lower result.

Regardless of where V_{DS} is measured, at very large di_D/dt's the package inductance (e.g., the source wirebonds) will induce drain-source voltages at the die that are greater than those observable externally. To guard against excessive voltages, V_{DS} should be monitored across the drain header and source sense terminal, and the maximum allowable di_D/dt should be derated in accordance with the pack V_{DS} as shown in Figure 18.

MTE150N08
MTE150N10
MTE200N05
MTE200N06

MOTOROLA

C

Designer's Data Sheet

150 and 200 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.009 OHM
50 and 60 VOLTS

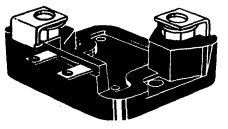
$r_{DS(on)}$ = 0.012 OHM
80 and 100 VOLTS

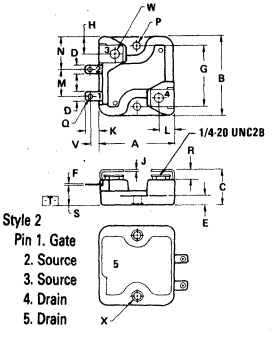
ENERGY MANAGEMENT SERIES
N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTORS

These TMOS Power FETs are designed for high current, high speed power switching applications such as switching regulators, converters, and motor controls.

- I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- High di/dt Capability
- Silicon Gate for Fast Switching Speeds
- Multi-chip Construction
- Gates Internally Decoupled

TMOS™





NOTES:
1. DIMENSION A AND B ARE DATUMS.
2. T IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ ∅ 0.36 (0.014)Ⓜ T AⓂ BⓂ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	–	26.67	–	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01
MO-040AA

MAXIMUM RATINGS

Rating	Symbol	MTE 200N05	MTE 200N06	MTE 150N08	MTE 150N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	I_D I_{DM}	200 800		150 600		Adc
Turn-Off Rate of Change	di_D/dt	See Note 4 and Figure 18 in Considerations				A/μs
Gate Current — Pulsed	I_{GM}	2.0				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	500 4.0				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150				°C
Mounting Torque (To heat sink with 10–32 screw)(1)	τ(m)	20				in-lb
Lead Torque (Lead to bus with ¼–20 screw) (2)	τ(l)	20				in-lb
Per Unit Weight	W	120				grams

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.25	°C/W
Maximum Lead Temp. for Soldering Purposes, ⅛" from case for 5 seconds	T_L	275	°C

1. A Belleville washer of 0.472" O.D., 0.205" I.D., 0.024" thick and 150 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.75".

.003" thick mica insulator available as a separate item. Motorola P/N 48ASB1238TB001

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTE200N05	$V_{(BR)DSS}$	50	—	Vdc
	MTE200N06		60	—	
	MTE150N08		80	—	
	MTE150N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 100 Adc)	MTE200N05	$r_{DS(on)}$	—	0.009	Ohms
	MTE200N06				
(V_{GS} = 10 Vdc, I_D = 75 Adc)	MTE150N08		—	0.012	
	MTE150N10				
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 200 Adc)	MTE200N05		—	2.1	
	MTE200N06				
(I_D = 100 Adc, T_J = 100°C)	MTE200N05		—	1.8	
	MTE200N06				
(I_D = 150 Adc)	MTE150N08		—	2.2	
	MTE150N10				
(I_D = 75 Adc, T_J = 100°C)	MTE150N08		—	1.8	
	MTE150N10				
Forward Transconductance (V_{DS} = 15 V, I_D = 100 A)	MTE200N05	g_{fs}	40	—	mhos
	MTE200N06				
(V_{DS} = 15 V, I_D = 75 A)	MTE150N08		40	—	
	MTE150N10				
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	18,000	pF
Output Capacitance		C_{oss}	—	10,000	
Reverse Transfer Capacitance		C_{rss}	—	4,000	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Inductive Load, Clamped — MTE200N05 and MTE200N06					
Turn-Off Delay Time	(V_{clamp} = 25 Vdc, I_D = 100 Adc	t_{dv}	—	1400	ns
Crossover Time	L = 25 μH, V_{in} = 10 Vdc	t_c	—	2000	
Current Fall Time	R_{gen} = 50 Ω) See Figures 16 and 17	t_{fi}	—	700	
Inductive Load, Clamped — MTE 150N08 and MTE150N10					
Turn-Off Delay Time	(V_{clamp} = 25 Vdc, I_D = 75 Adc	t_{dv}	—	1400	ns
Crossover Time	L = 25 μH, V_{in} = 10 Vdc	t_c	—	1200	
Current Fall Time	R_{gen} = 50 Ω) See Figures 16 and 17	t_{fi}	—	400	

SOURCE-DRAIN DIODE CHARACTERISTICS*		Symbol	Typical	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	50	ns
Reverse Recovery Time		t_{rr}	650	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

C

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TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 1 — MTE150N08, MTE150N10

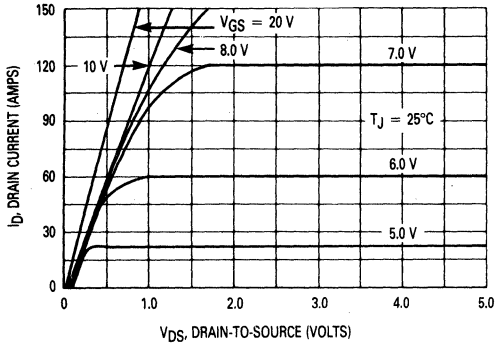
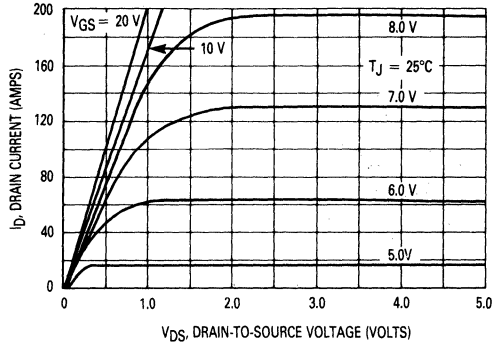


FIGURE 2 — MTE200N05, MTE200N06



TRANSFER CHARACTERISTICS

FIGURE 3 — MTE150N08, MTE150N10

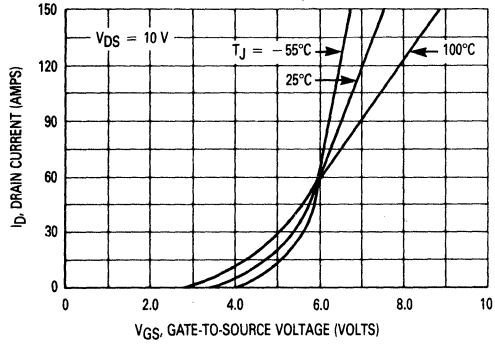
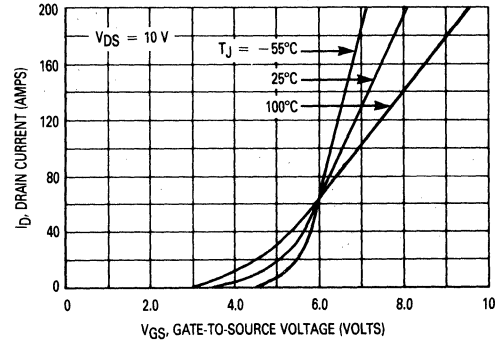


FIGURE 4 — MTE200N05, MTE200N06



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 5 — MTE150N08, MTE150N10

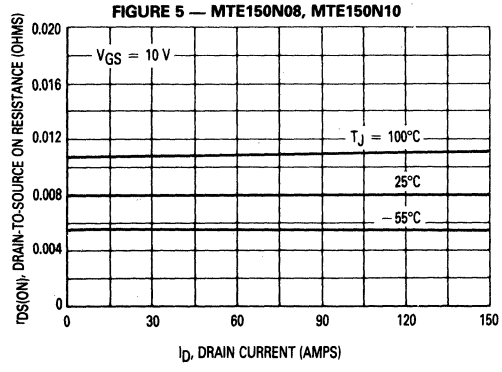
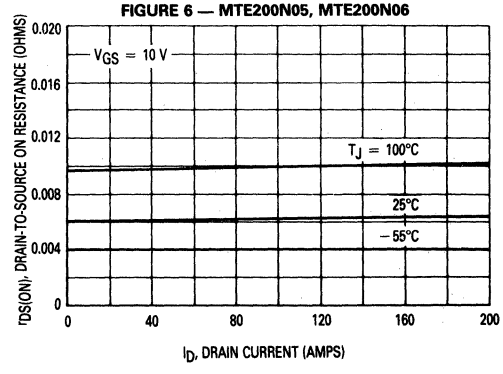


FIGURE 6 — MTE200N05, MTE200N06



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

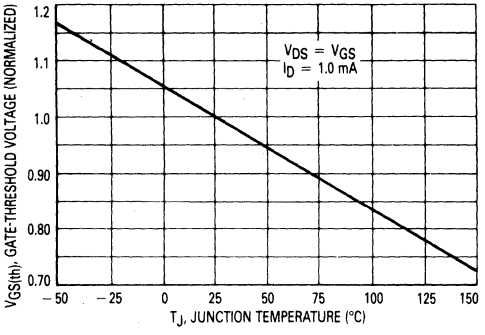
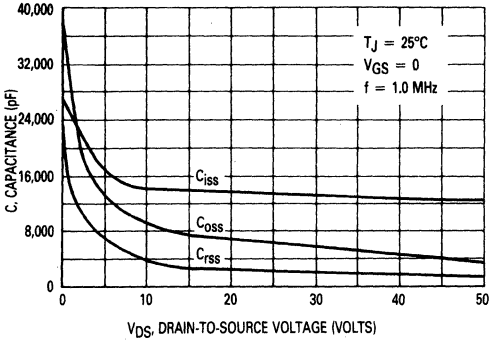


FIGURE 8 — CAPACITANCE VARIATION



C

TMOS SOURCE-TO-DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 9. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on-voltage, forward turn-on and reverse recovery times are given.

FIGURE 9 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

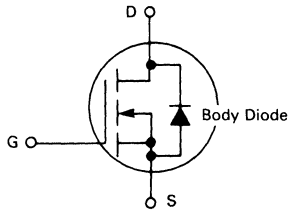


FIGURE 10 — DIODE SWITCHING WAVEFORM

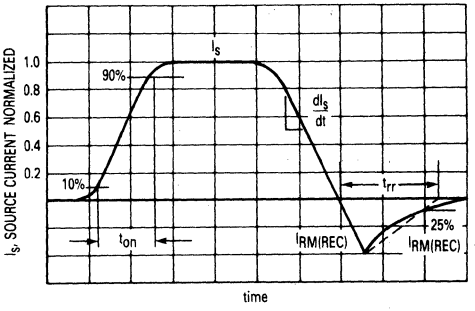
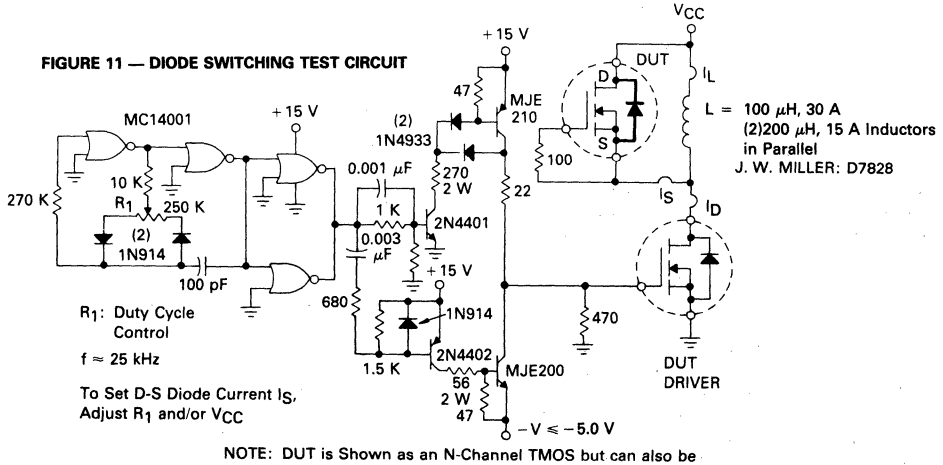


FIGURE 11 — DIODE SWITCHING TEST CIRCUIT



NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

C

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTE150N08, MTE150N10

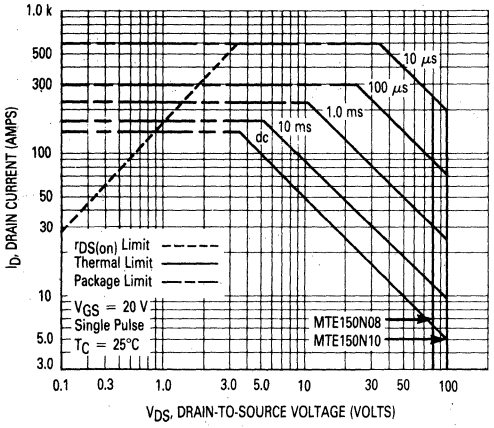


FIGURE 13 — MTE200N05, MTE200N06

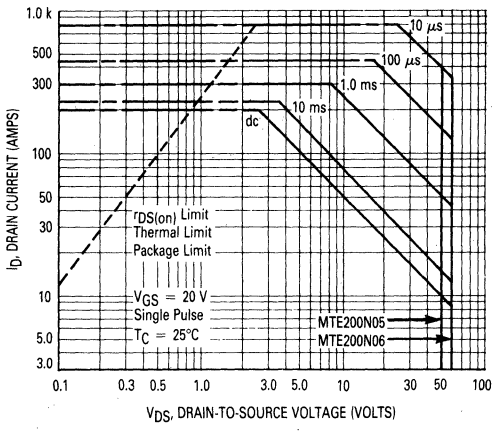


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

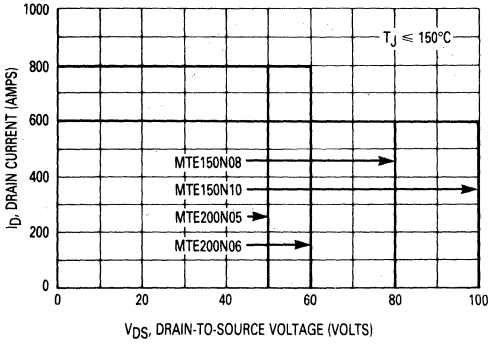
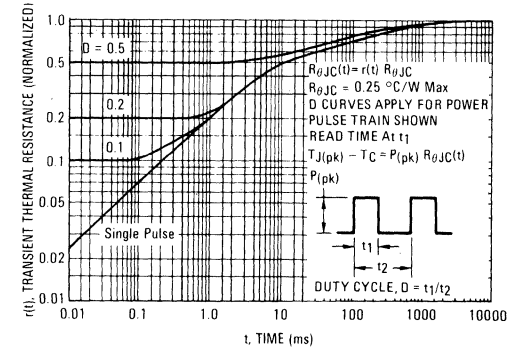


FIGURE 15 — THERMAL RESPONSE



GUARANTEED SAFE OPERATING AREA

The dc data presented in Figures 12 and 13 is for a single 1-second pulse, applied while maintaining the case temperature T_C at 25°C. For multiple pulses and case temperatures other than 25°C, the dc drain current at a case temperature of 25°C should be de-rated as follows:

$$I_D(T) = I_D(25°)\left[\frac{150 - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where P_D is the maximum power rating at 25°C, $R_{\theta JC}$ is the junction-to case thermal resistance, and $r(t)$ is the normalized thermal response from Figure 15, corresponding to the appropriate pulse width and duty cycle.

EXAMPLE: Determine the maximum allowable drain current for an MTE200N05 at 25 volts drain voltage, with a pulse width of 10 ms and duty cycle of 50%, at a case temperature of 80°C.

From Figure 13, the dc drain current at V_{DS} = 25 volts is 30 A. For a 10 ms pulse and duty cycle of 50%, Figure 15 gives an $r(t)$ of 0.6; then, with P_D = 500 watts at 25°C and $R_{\theta JC}$ = 0.25°C/W

$$I_D = 30 \times \frac{150 - 80}{500 \times 0.25 \times 0.6} = 28 \text{ A}$$

The switching safe operating area in Figure 14 is the boundary that the load line may traverse without incurring damage to the device. The fundamental limits are the maximum rated peak drain current I_{DM}, the minimum drain-to-source breakdown voltage $V_{BR(DSS)}$ and the maximum rated junction temperature. The boundaries are applicable for both turn-on and turn-off of the devices for rise and fall times of less than one microsecond.

FIGURE 16 — INDUCTIVE LOAD SWITCHING CIRCUIT

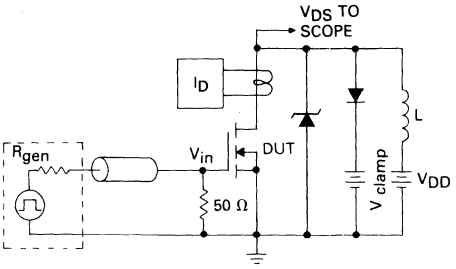
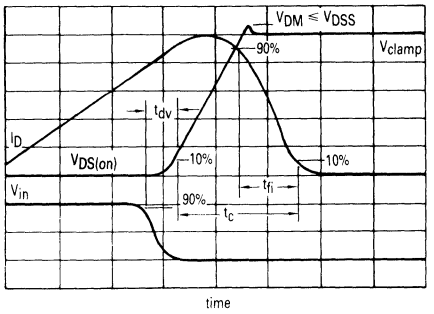


FIGURE 17 — CLAMPED INDUCTIVE LOAD SWITCHING WAVEFORMS



CONSIDERATIONS IN DESIGNING WITH POWER MOSFETS

Depending on the frequency of operation, certain precautions must be taken to insure optimum reliability. When switching near the device maximum frequency, the high current and very fast switching capability of this device necessitates the use of the following protective measures:

Note 1 As in any wideband circuit, good RF layout techniques must be maintained, i.e., short lead lengths, adequate ground planes and decoupled power supplies.

Note 2 All overvoltage protection circuitry — free wheeling diodes, zeners, MOVs, snubber networks — should be placed directly between the drain-source or between the drain and a good, low inductance ac ground.

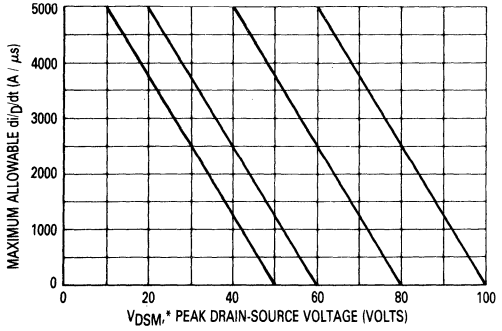
Note 3 Since most "real world" loads are inductive, the fast turn-off peak flyback voltage ($e = L\ di/dt$) must not exceed the $V_{BR(DSS)}$ rating, an instantaneous voltage limit. The protective circuitry, including parasitics, must have response times commensurate with the Power MOSFET switching speed, e.g., rectifiers must have very short recovery times. The forward recovery time t_{fr}, overshoot voltage $V_{FM(DYN)}$ and reverse recovery time t_{rr} should be low to minimize the switching stress on the transistor.

Note 4 Even with good RF layout and ideal clamping below the maximum $V_{(BR)DSS}$ of the device, significant potentials may be generated across the package drain and source parasitic inductances during rapid turn off of a large magnitude of current. These induced voltages which are internal to the package add to the clamp voltage.

Monitoring V_{DS} by observing the potential that appears across the drain header (package heat sink) and the source sense terminal gives the best indication of the potential appearing at the chip. Due to the source and drain bus inductances, sensing V_{DS} across the drain and source terminals may yield a significantly lower result.

Regardless of where V_{DS} is measured, at very large di_D/dt's the package inductance (e.g., the source wirebonds) will induce drain-source voltages at the die that are greater than those observable externally. To guard against excessive voltages, V_{DS} should be monitored across the drain header and source sense terminal, and the maximum allowable di_D/dt should be derated in accordance with the peak V_{DS} as shown in Figure 18.

FIGURE 18 — MAXIMUM ALLOWABLE di_D/dt versus PEAK DRAIN SOURCE VOLTAGE



* MAXIMUM DRAIN-SOURCE VOLTAGE APPEARING BETWEEN THE DRAIN HEADER AND THE SOURCE SENSE LEAD

MTH15N18
MTH15N20
MTH20N12
MTH20N15

MOTOROLA

C

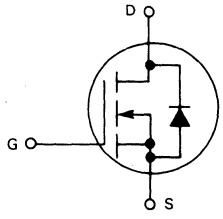
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTORS

These TMOS Power FETs are designed for high-speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads

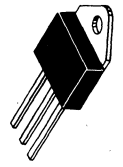
TMOS™

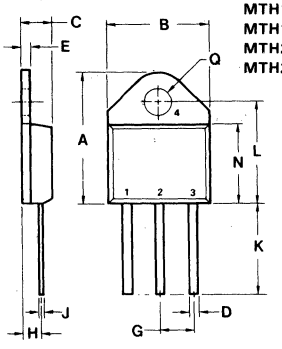


15 and 20 AMPERE

N-CHANNEL TMOS POWER FETs

$r_{DS(on)}$ = 0.16 OHM
180 and 200 VOLTS
$r_{DS(on)}$ = 0.12 OHM
120 and 150 VOLTS





MTH15N18
MTH15N20
MTH20N12
MTH20N15

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH 20N12	MTH 20N15	MTH 15N18	MTH 15N20	Unit
Drain-Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current — Continuous	I_D	20		15		Adc
Drain Current — Pulsed	I_{DM}	100		80		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C	P_D	150				Watts
Derate above 25°C		1.2				W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTH20N12	$V_{(BR)DSS}$	120	—	Vdc
	MTH20N15		150	—	
	MTH15N18		180	—	
	MTH15N20		200	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_J = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Static Drain-Source On-Resistance		$r_{DS(on)}$			Ohm
(V_{GS} = 10 Vdc, I_D = 10 Adc)	MTH20N12/MTH20N15		—	0.12	
(V_{GS} = 10 Vdc, I_D = 7.5 Adc)	MTH15N18/MTH15N20		—	0.16	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 20 Adc)	MTH20N12/MTH20N15		—	3.0	
(I_D = 10 Adc, T_J = 100°C)	MTH20N12/MTH20N15		—	2.4	
(I_D = 15 Adc)	MTH15N18/MTH15N20		—	3.0	
(I_D = 7.5 Adc, T_J = 100°C)	MTH15N18/MTH15N20		—	2.4	
Forward Transconductance		g_{fs}			mhos
(V_{DS} = 15 V, I_D = 10 A)	MTH20N12/MTH20N15		8.0	—	
(V_{DS} = 15 V, I_D = 7.5 A)	MTH15N18/MTH15N20		4.0	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	700	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 1 and 2	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	220	
Fall Time		t_f	—	250	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	50	ns
Reverse Recovery Time		t_{rr}	450	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

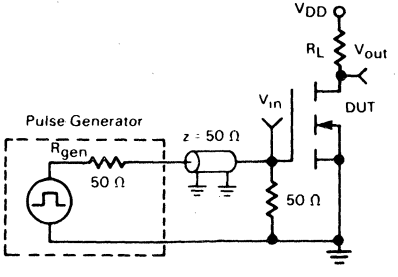
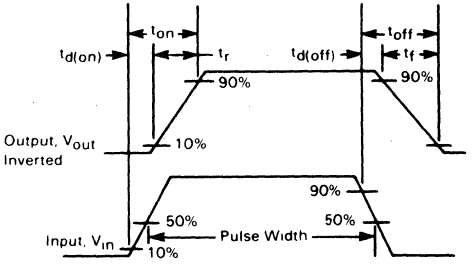


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTH20N12, MTH20N15

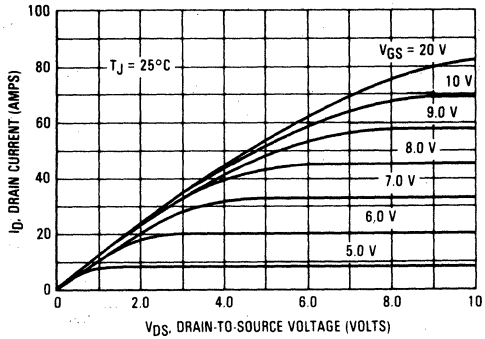
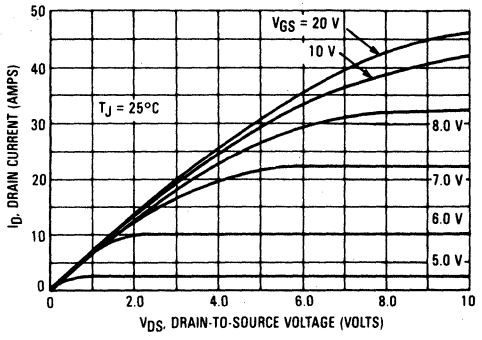


FIGURE 4 — MTH15N18, MTH15N20



TRANSFER CHARACTERISTICS

FIGURE 5 — MTH20N12, MTH20N15

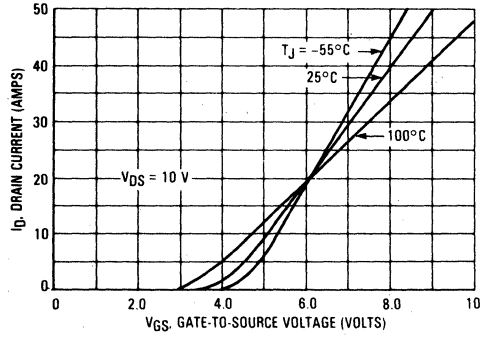
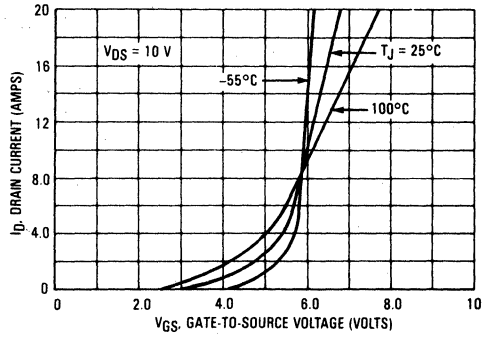


FIGURE 6 — MTH15N18, MTH15N20



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTH20N12, MTH20N15

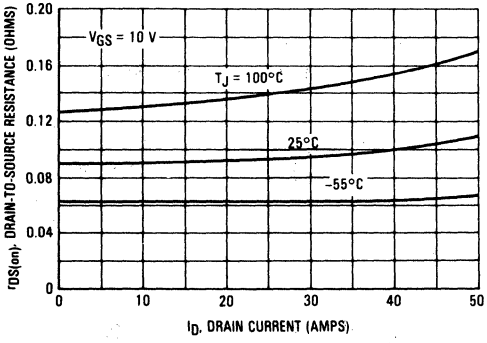
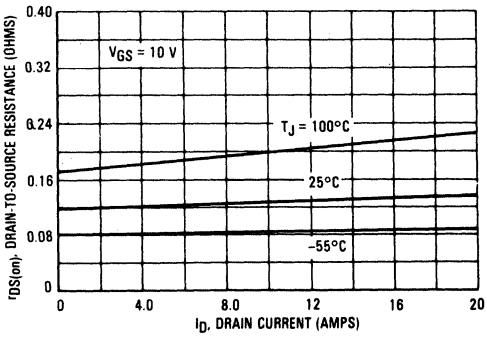


FIGURE 8 — MTH15N18, MTH15N20



TYPICAL CHARACTERISTICS

FIGURE 9 — GATE THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

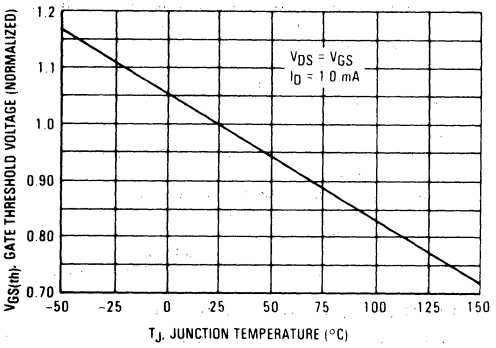
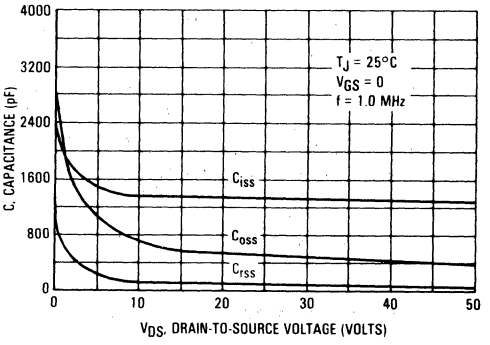
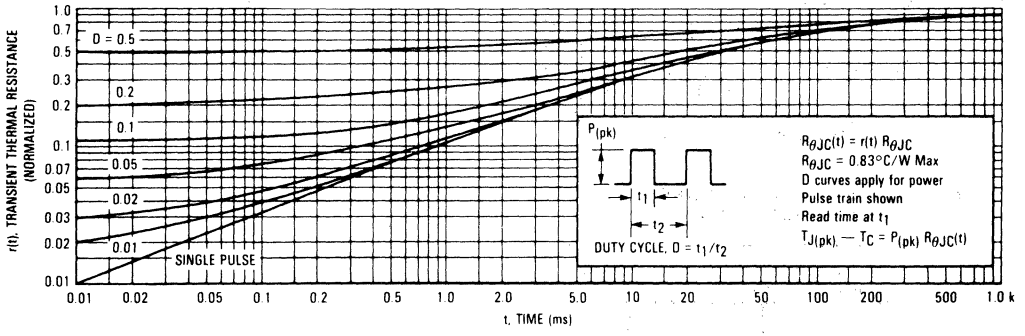


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTH15N18, MTH15N20, MTH20N12, MTH20N15



RATED SAFE OPERATING AREA INFORMATION

FIGURE 12 — MTH20N12, MTH20N15

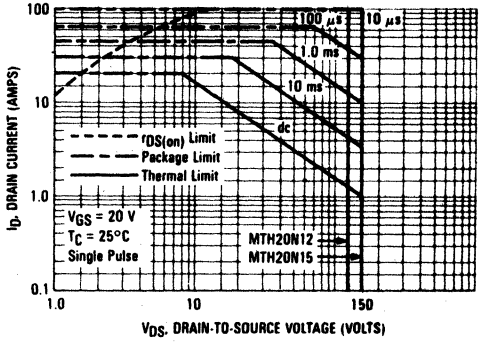


FIGURE 13 — MTH15N18, MTH15N20

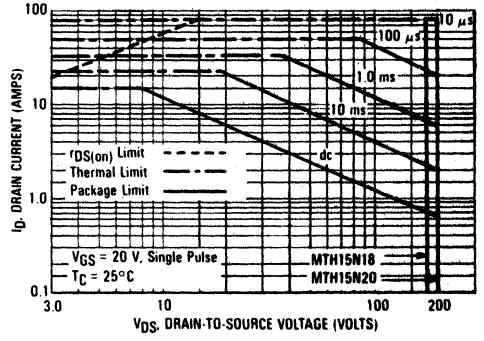
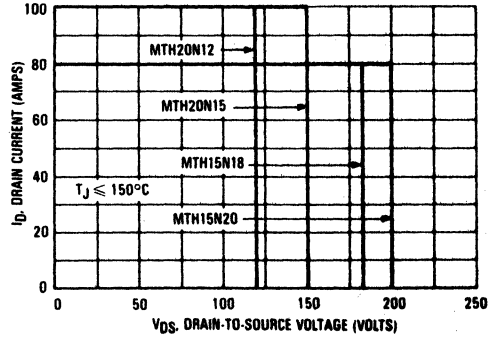


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_D(25°C)\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

Where

I_D (25°C) = the dc drain current at T_C = 25°C from Figures 12 and 13
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MOTOROLA

MTH25N08
MTH25N10
MTH35N05
MTH35N06

C

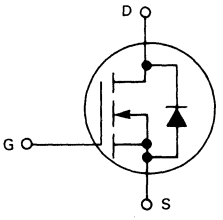
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTORS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads

TMOS™

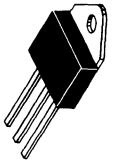


25 and 35 AMPERE

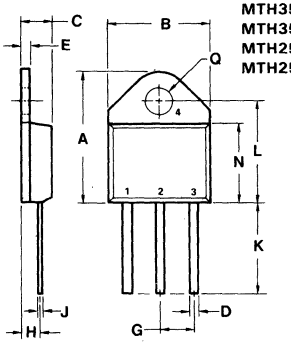
N-CHANNEL TMOS POWER FETs

$r_{DS(on)}$ = 0.075 OHM
80 and 100 VOLTS

$r_{DS(on)}$ = 0.055 OHM
50 and 60 VOLTS



MTH35N05
MTH35N06
MTH25N08
MTH25N10



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH 35N05	MTH 35N06	MTH 25N08	MTH 25N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current — Continuous Pulsed	I_D I_{DM}	35 150		25 125		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTH35N05	$V_{(BR)DSS}$	50	—	Vdc
	MTH35N06		60	—	
	MTH25N08		80	—	
	MTH25N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_C = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Static Drain-Source On-Resistance		$r_{DS(on)}$			Ohm
(V_{GS} = 10 Vdc, I_D = 17.5 Adc)	MTH35N05/MTH35N06		—	0.055	
(V_{GS} = 10 Vdc, I_D = 12.5 Adc)	MTH25N08/MTH25N10		—	0.075	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 35 Adc)	MTH35N05/MTH35N06		—	2.3	
(I_D = 17.5 Adc, T_J = 100°C)	MTH35N05/MTH35N06		—	1.9	
(I_D = 25 Adc)	MTH25N08/MTH25N10		—	2.25	
(I_D = 12.5 Adc, T_C = 100°C)	MTH25N08/MTH25N10		—	1.8	
Forward Transconductance		g_{fs}			mhos
(V_{DS} = 15 V, I_D = 17.5 A)	MTH35N05/MTH35N06		8.0	—	
(V_{DS} = 10 V, I_D = 12.5 A)	MTH25N08/MTH25N10		5.0	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 1 and 2	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	300	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.5	Vdc
Forward Turn-On Time		t_{on}	50	ns
Reverse Recovery Time		t_{rr}	450	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

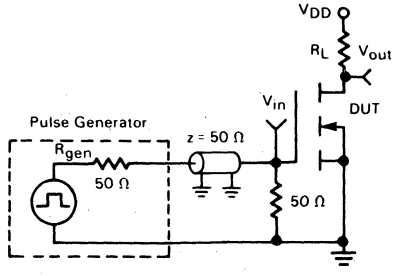
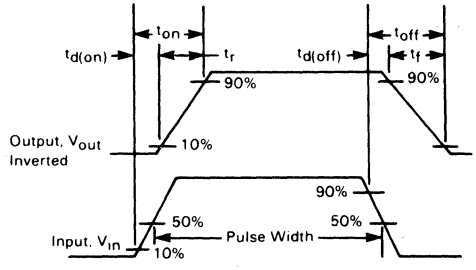


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

MTH25N08, MTH25N10

FIGURE 3 — ON-REGION CHARACTERISTICS

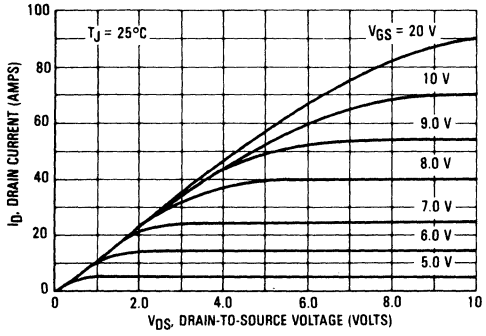


FIGURE 5 — TRANSFER CHARACTERISTICS

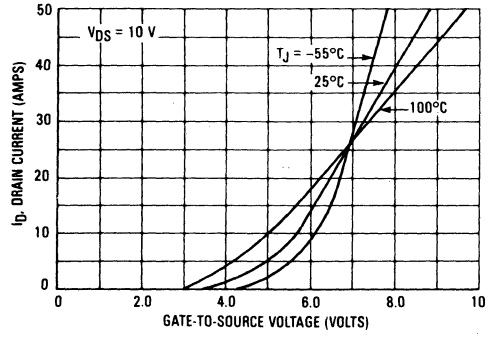
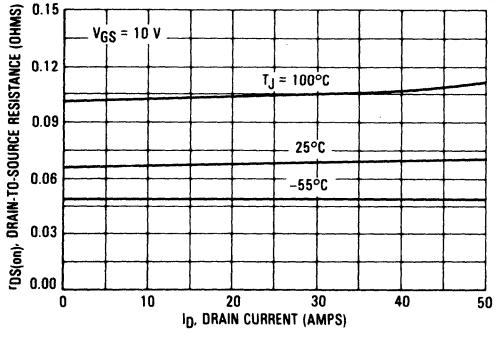


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT



MTH35N05, MTH35N06

FIGURE 4 — ON-REGION CHARACTERISTICS

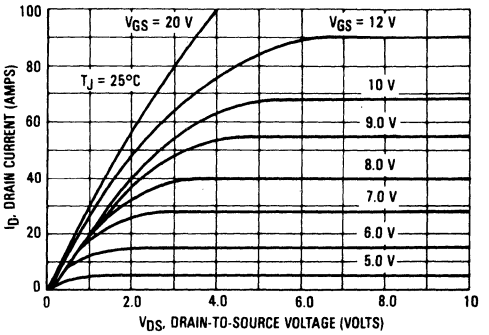


FIGURE 6 — TRANSFER CHARACTERISTICS

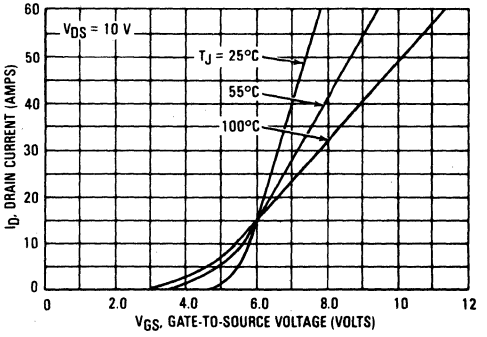
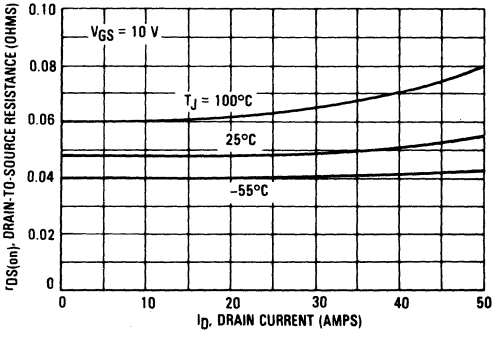


FIGURE 8 — ON-RESISTANCE versus DRAIN CURRENT



C

TYPICAL CHARACTERISTICS

FIGURE 9 — GATE THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

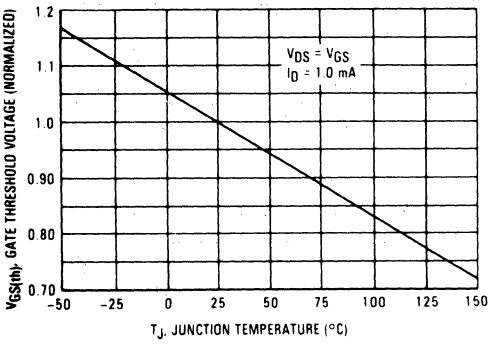
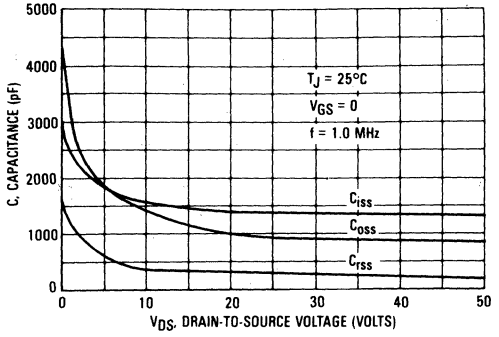
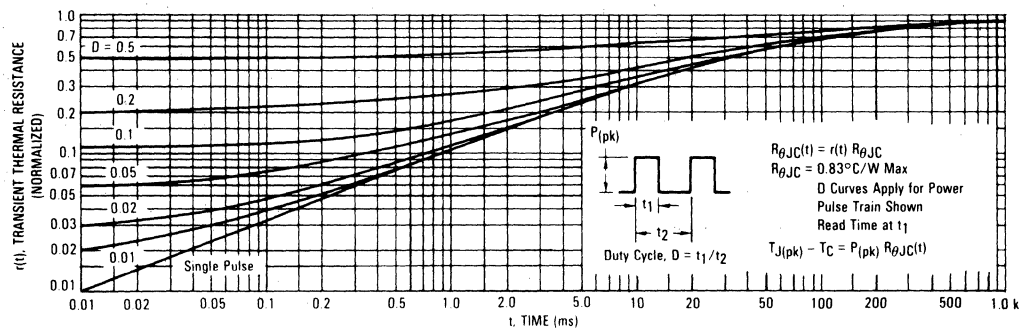


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTH25N08/MTH25N10
MTH35N05/MTH35N06



OPERATING AREA INFORMATION

FIGURE 12 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

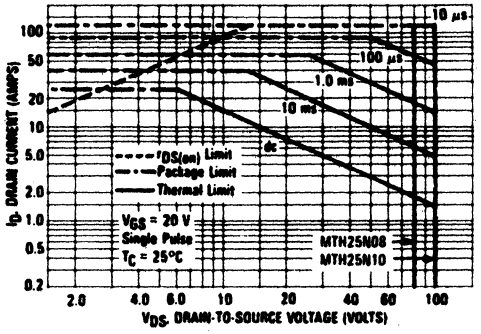


FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

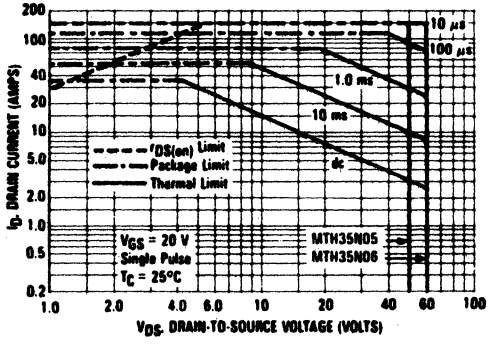
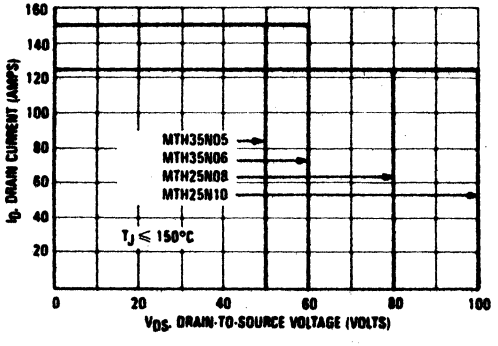


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_D(25°C)\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

Where

$I_D(25°C)$ = dc drain current at T_C = 25°C from Figures 12 and 13
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
$r(t)$ = normalized thermal response from Figure 11

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off to the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MTM1N95, MTM1N100
MTP1N95, MTP1N100

MOTOROLA

C

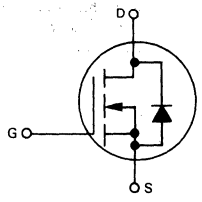
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, and converters or high voltage linear applications such as high voltage power supplies.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

TMOS™

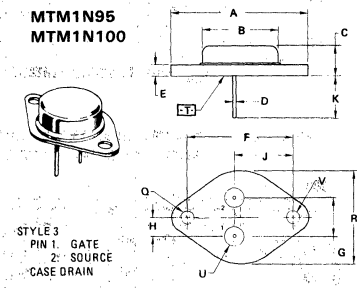


1.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 10 OHMS
950 and 1000 VOLTS

MTM1N95
MTM1N100

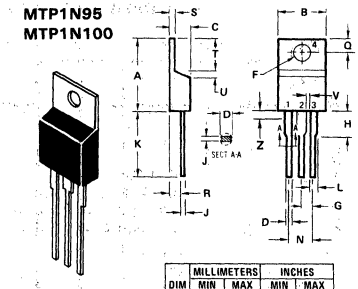


CASE 1-05
TO-204AA
(TO-3 TYPE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ ϕ.13 (0.005) M T V M
   FOR LEADS:
   ⌖ ϕ.13 (0.005) M T V M Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

MTP1N95
MTP1N100



CASE 221A-02
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

MAXIMUM RATINGS

Rating	Symbol	MTM1N95 MTP1N95	MTM1N100 MTP1N100	Unit
Drain-Source Voltage	V_{DSS}	950	1000	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	950	1000	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 1.0 6.0		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM1N95/MTP1N95 MTM1N100/MTP1N100	$V_{(BR)DSS}$	950 1000	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 0.5 Adc) (I_D = 1.0 Adc) (I_D = 0.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	5.0 12 10	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$r_{DS(on)}$	—	10	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 0.5 A)		g_{fs}	0.5	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 0.5 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 1.0 A V_{GS} = 0	V_{SD}	1.0	Vdc
Forward Turn-On Time		t_{on}	250	ns
Reverse Recovery Time		t_{rr}	420	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

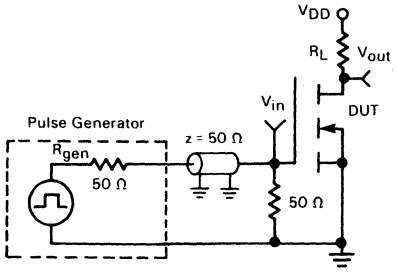
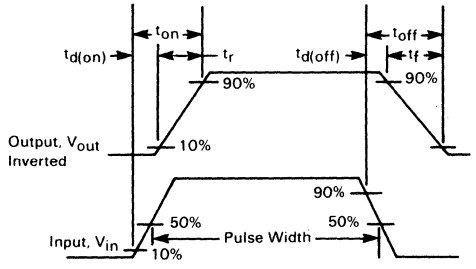


FIGURE 2 — SWITCHING WAVEFORMS



C

FIGURE 3 — OUTPUT CHARACTERISTICS

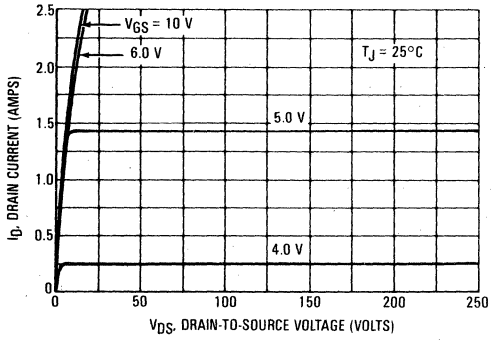


FIGURE 4 — ON-REGION CHARACTERISTICS

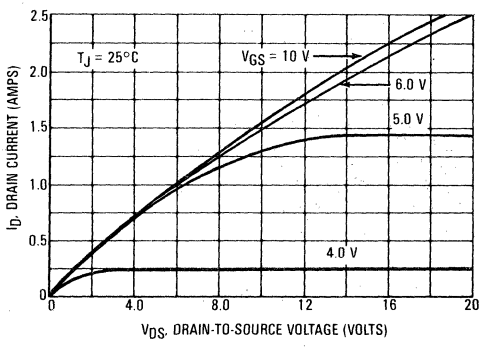


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

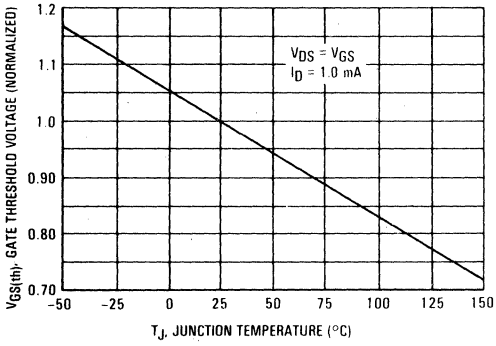


FIGURE 6 — TRANSFER CHARACTERISTICS

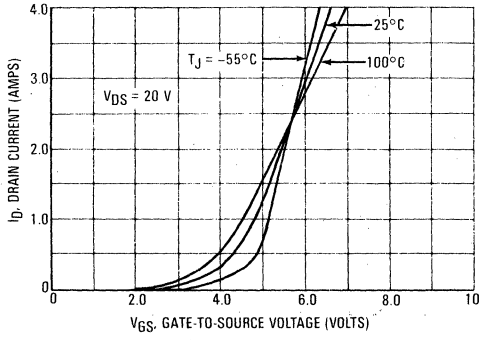


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

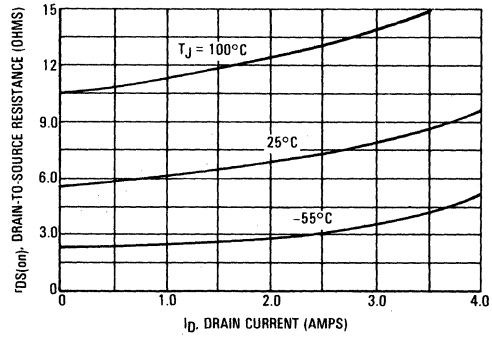
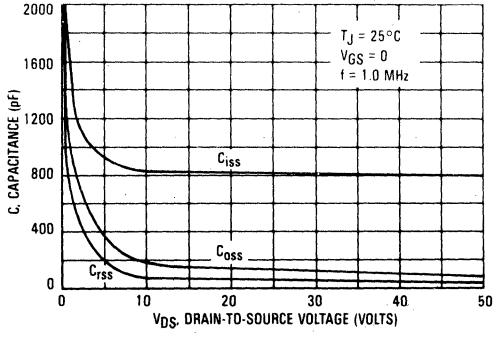


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

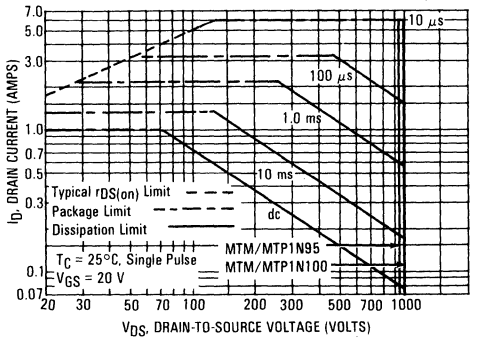
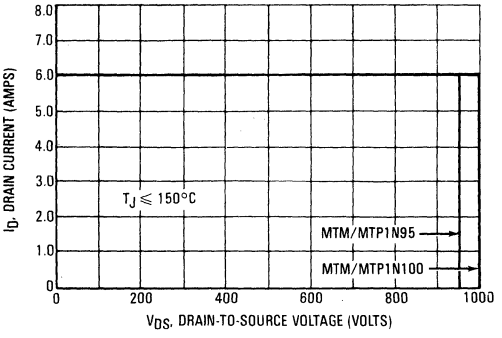


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figures 11 or 12.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10 is the boundary that the load line may traverse without incurring damage to the MOSFET. The Fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

THERMAL RESPONSE

FIGURE 11 — MTM1N95/MTM1N100

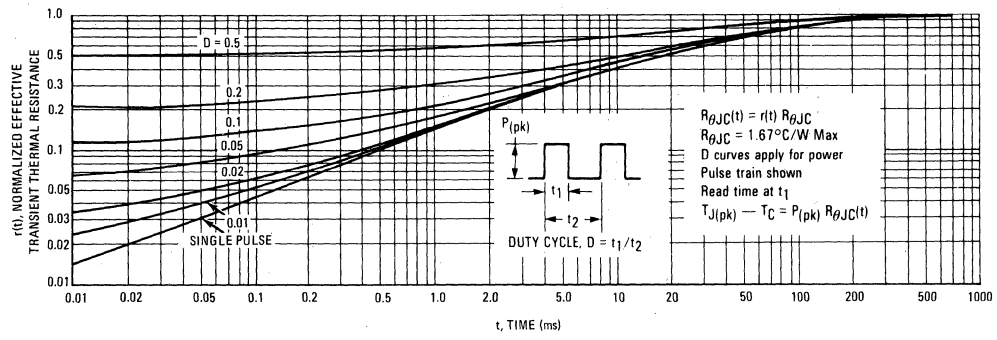
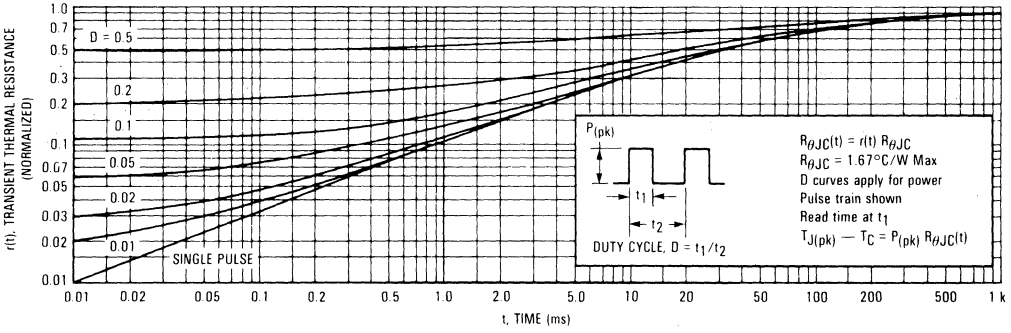


FIGURE 12 — MTP1N95/MTP1N100



MOTOROLA

MTM2N45, MTM2N50
MTP2N45, MTP2N50

C

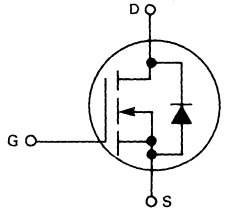
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

TMOS™

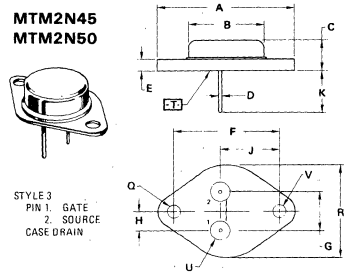


2.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 4.0 OHMS
450 and 500 VOLTS

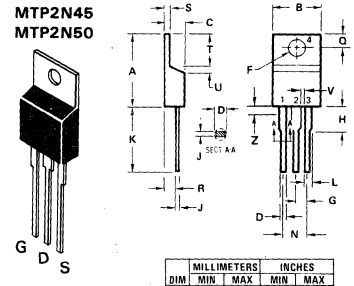
MTM2N45
MTM2N50



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(TO-3 TYPE)

MTP2N45
MTP2N50



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM2N45 MTP2N45	MTM2N50 MTP2N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 2.0 7.0		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM2N45/MTP2N45 MTM2N50/MTP2N50	$V_{(BR)DSS}$	 450 500	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	 2.0 1.5	 4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 1.0 Adc) (I_D = 2.0 Adc) (I_D = 1.0 Adc, T_J = 100°C)		$V_{DS(on)}$	 — — —	 4.0 10 8.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$r_{DS(on)}$	—	4.0	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 1.0 A)		g_{fs}	1.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	100	pF
Reverse Transfer Capacitance		C_{rss}	—	50	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 1.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	60	ns
Turn-Off Delay Time		$t_{d(off)}$	—	60	ns
Fall Time		t_f	—	30	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 2.0 A V_{GS} = 0	V_{SD}	1.0	Vdc
Forward Turn-On Time		t_{on}	150	ns
Reverse Recovery Time		t_{rr}	200	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 – SWITCHING TEST CIRCUIT

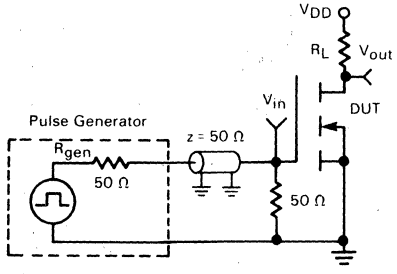
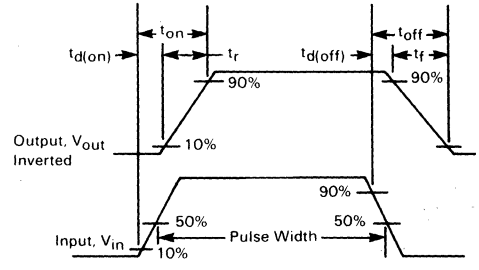


FIGURE 2 – SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

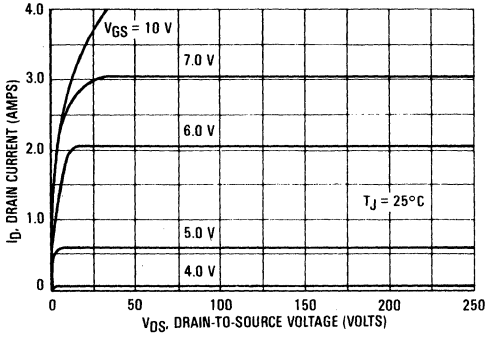


FIGURE 4 — ON-CHARACTERISITCS

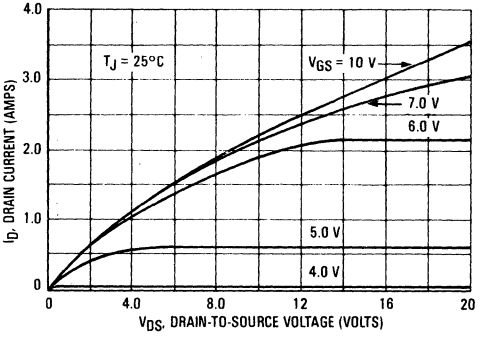


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

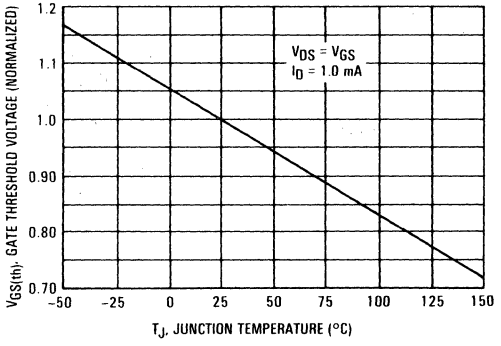
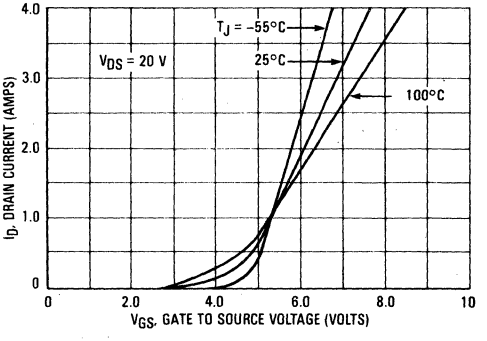


FIGURE 6 — TRANSFER CHARACTERISTICS



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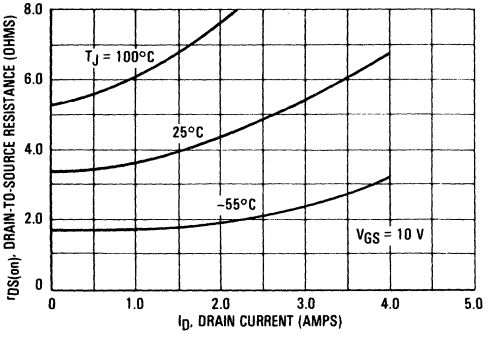

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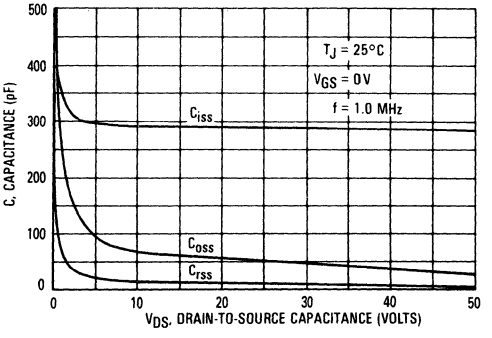

C

SAFE OPERATING AREA INFORMATION

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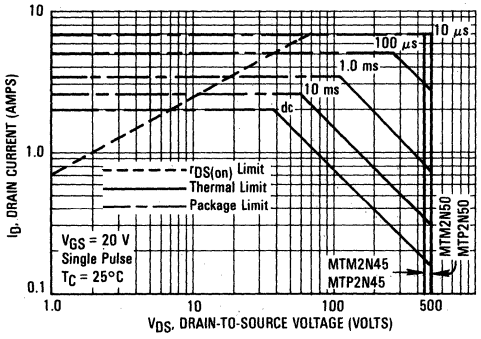
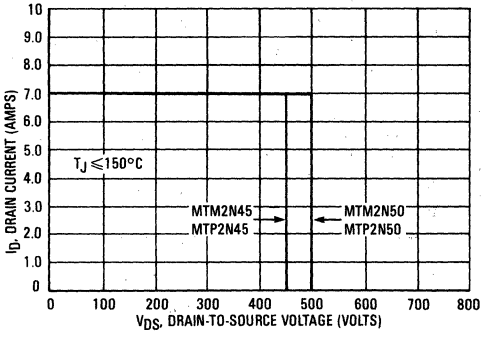


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figures 11 or 12.

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The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

FIGURE 11 — MTM2N45/MTM2N50

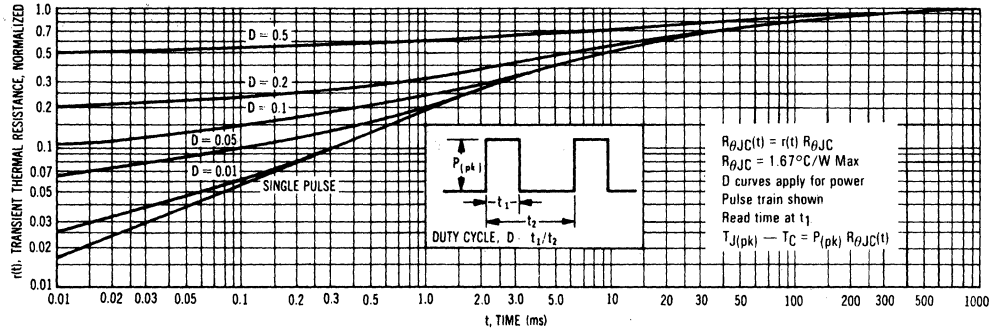
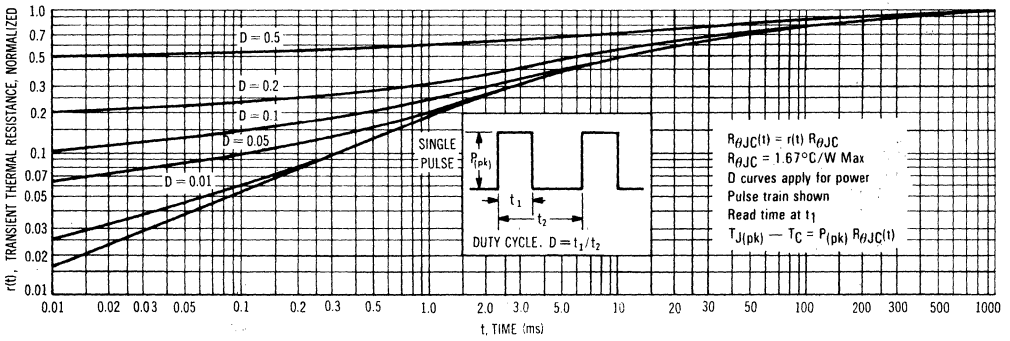


FIGURE 12 — MTP2N45/MTP2N50



TMOS POWER FET CONSIDERATIONS

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MTM2N85, MTM2N90
MTP2N85, MTP2N90

MOTOROLA

C

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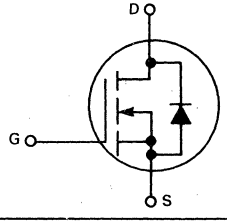
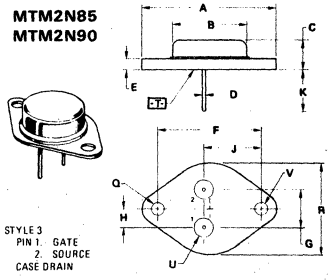
TMOS™



2.0 AMPERE
N-CHANNEL TMOS POWER FET
$r_{DS(on)}$ = 8.0 OHMS
850 and 900 VOLTS

MTM2N85
MTM2N90



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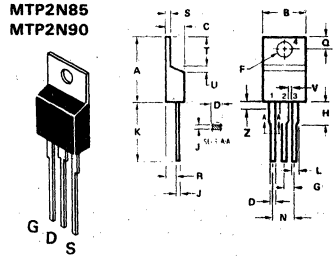
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(TO-3 TYPE)

MTP2N85
MTP2N90



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.78	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM2N85 MTP2N85	MTM2N90 MTP2N90	Unit
Drain-Source Voltage	V_{DSS}	850	900	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	850	900	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 2.0 7.0		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM2N85/MTP2N85 MTM2N90/MTP2N90	$V_{(BR)DSS}$	 850 900	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	 2.0 1.5	 4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 1.0 Adc) (I_D = 2.0 Adc) (I_D = 1.0 Adc, T_J = 100°C)		$V_{DS(on)}$	 — — —	 8.0 20 16	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$r_{DS(on)}$	—	8.0	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 1.0 A)		g_{fs}	0.5	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 1.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 2.0 A V_{GS} = 0	V_{SD}	1.0	Vdc
Forward Turn-On Time		t_{on}	250	ns
Reverse Recovery Time		t_{rr}	420	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

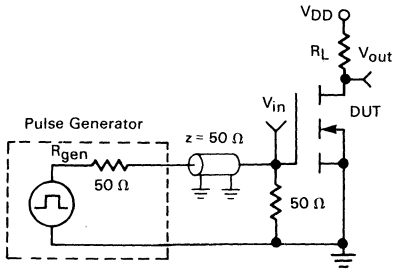
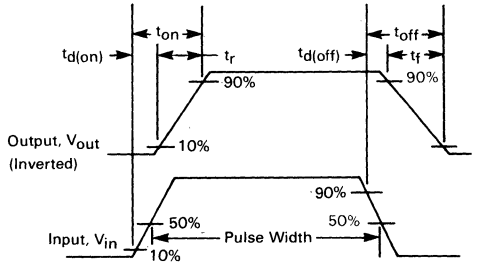


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

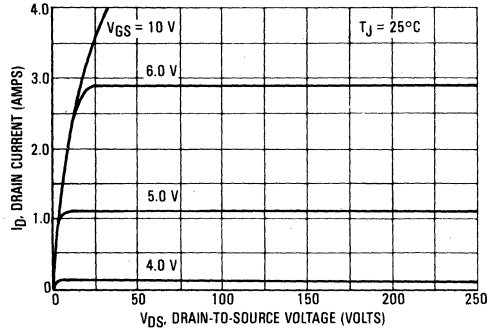


FIGURE 4 — ON-REGION CHARACTERISTICS

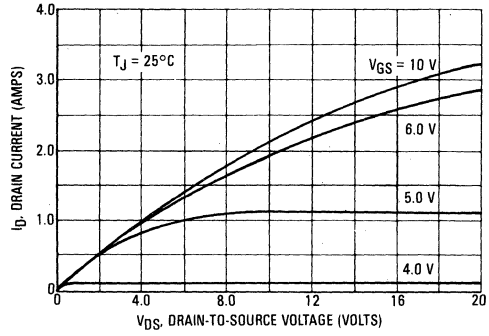


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

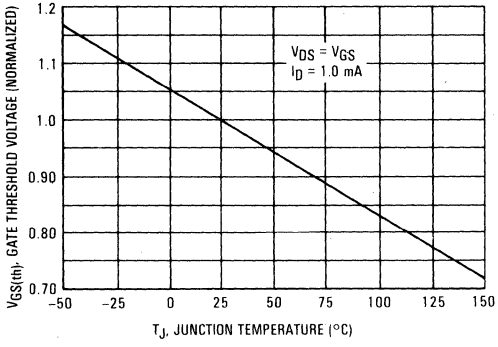


FIGURE 6 — TRANSFER CHARACTERISTICS

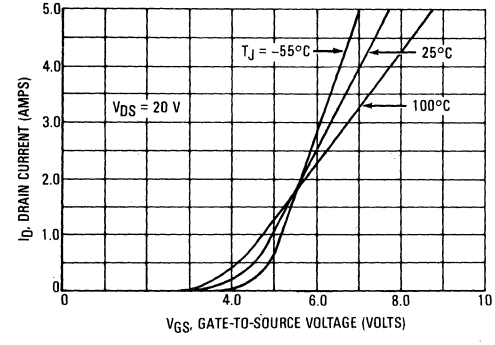


FIGURE 7 — ON RESISTANCE versus DRAIN CURRENT

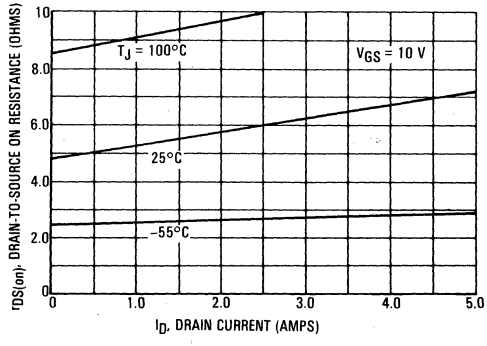
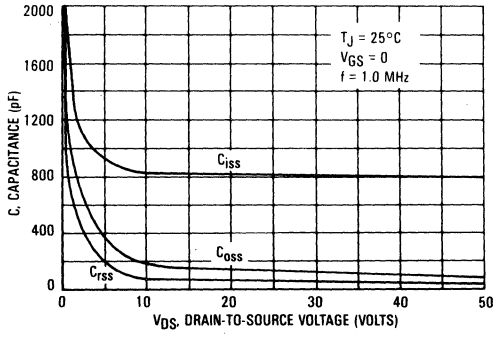


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

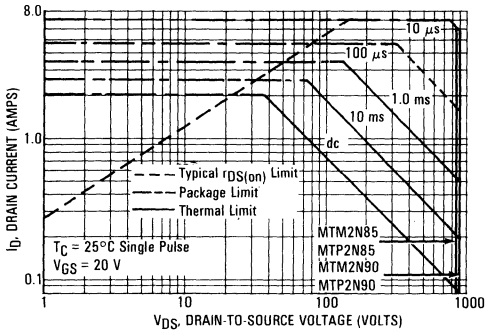
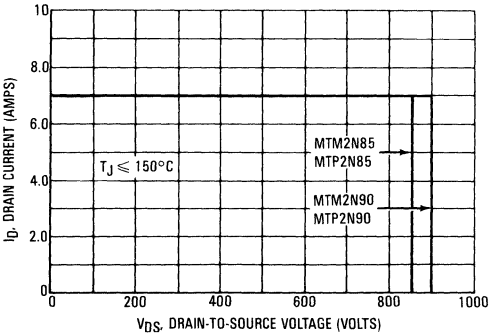


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figure 12.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10 is the boundary that the load line may traverse without incurring damage to the MOSFET. The Fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

C

THERMAL RESPONSE

FIGURE 11 — MTM2N85/MTM2N90

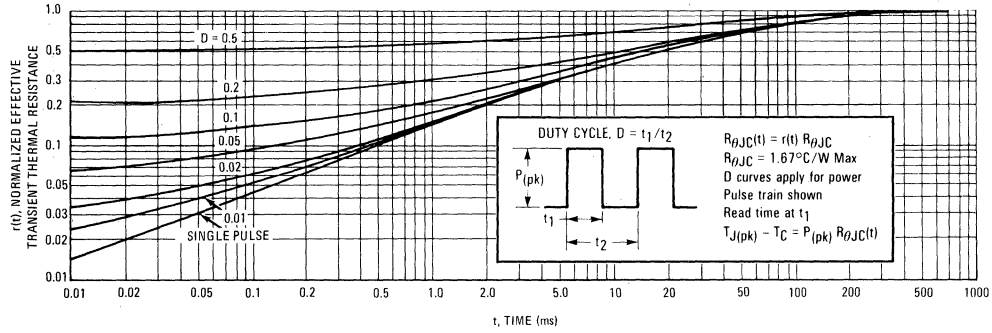
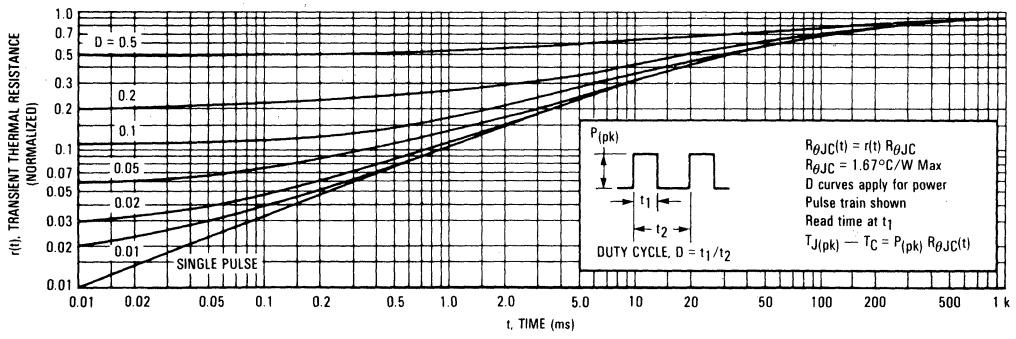


FIGURE 12 — MTP2N85/MTP2N90



MOTOROLA

MTM2P45, MTM2P50
MTP2P45, MTP2P50

Designer's Data Sheet

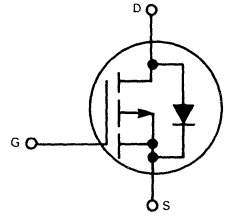
C

P-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

TMOS™

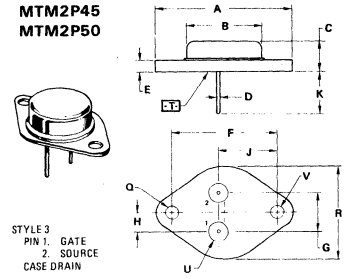


2.0 AMPERE

P-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 6.0 OHMS
450 and 500 VOLTS

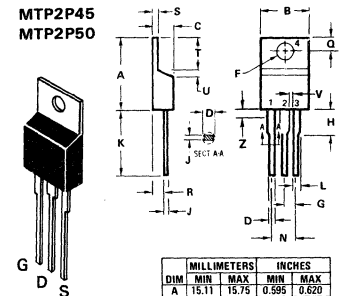
MTM2P45
MTM2P50



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(TO-3 TYPE)

MTP2P45
MTP2P50



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM2P45 MTP2P45	MTM2P50 MTP2P50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 2.0 8.0		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS*					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM2P45/MTP2P45 MTM2P50/MTP2P50	$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (T_C = 25°C) (I_D = 1.0 mA, V_{DS} = V_{GS}, T_J = 100°C)		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 1.0 Adc) (I_D = 2.0 Adc) (I_D = 1.0 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	6.0 12.5 12.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$r_{DS(on)}$	—	6.0	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 1.0 A)		g_{fs}	0.5	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA		See Figure 9	
Switching Safe Operating Area		SSOA		See Figure 10	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	200	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 1.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	100	ns
Turn-Off Delay Time		$t_{d(off)}$	—	150	ns
Fall Time		t_f	—	50	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 2.0 A V_{GS} = 0	V_{SD}	1.8	Vdc
Forward Turn-On Time		t_{on}	50	ns
Reverse Recovery Time		t_{rr}	120	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

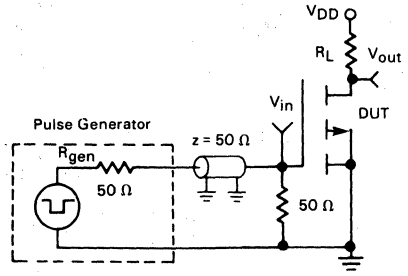
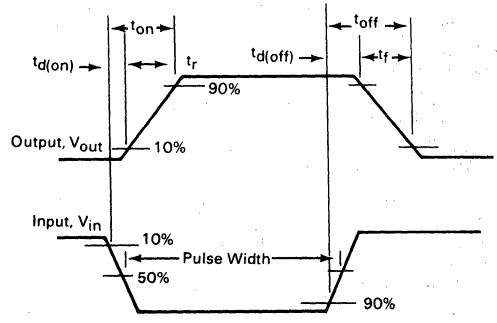


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

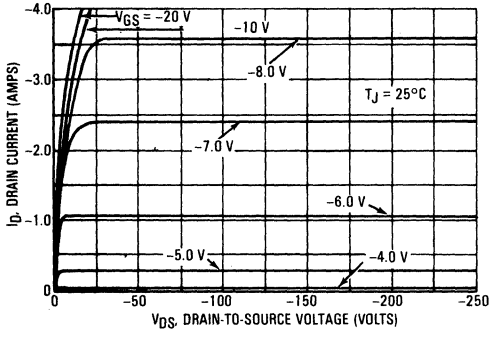


FIGURE 4 — ON-CHARACTERISTICS

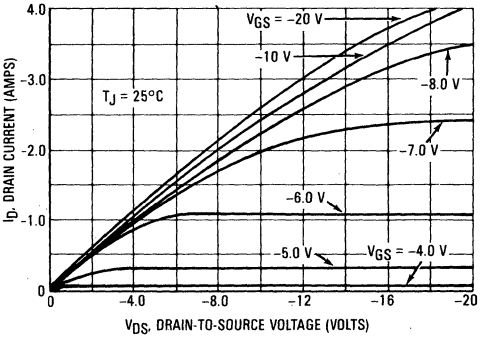


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

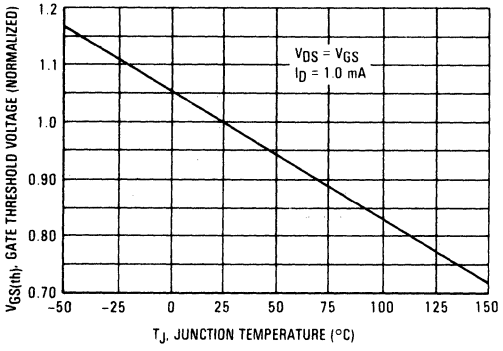


FIGURE 6 — TRANSFER CHARACTERISTICS

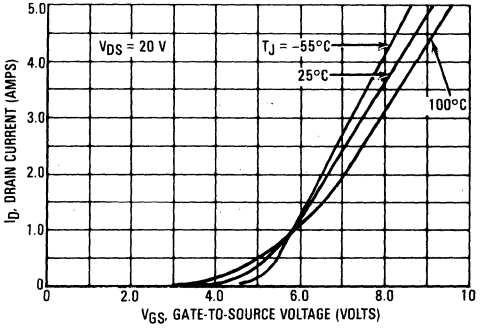


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

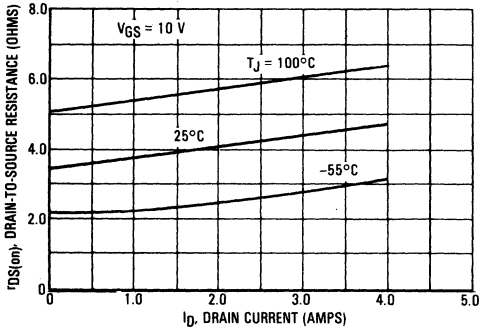
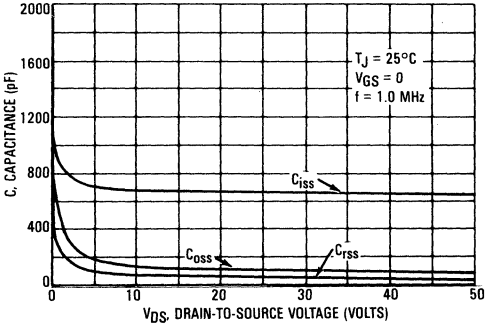


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

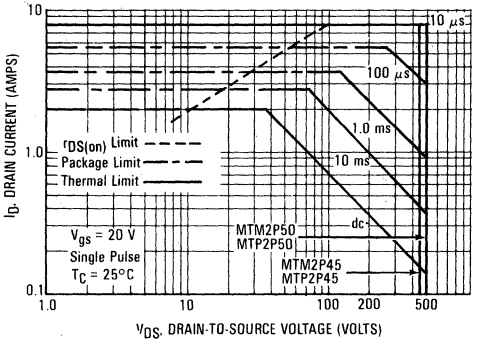
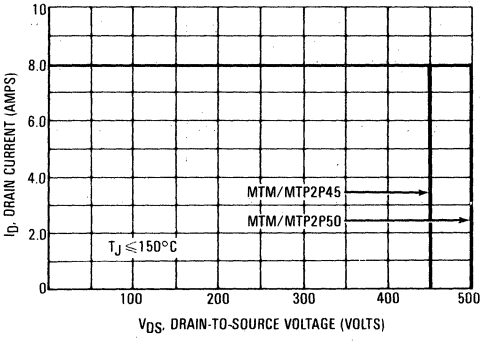


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figures 11 or 12.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10 is the boundary that the load line may traverse without incurring damage to the MOSFET. The Fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

THERMAL RESPONSE

FIGURE 11 — MTM2P45/MTM2P50

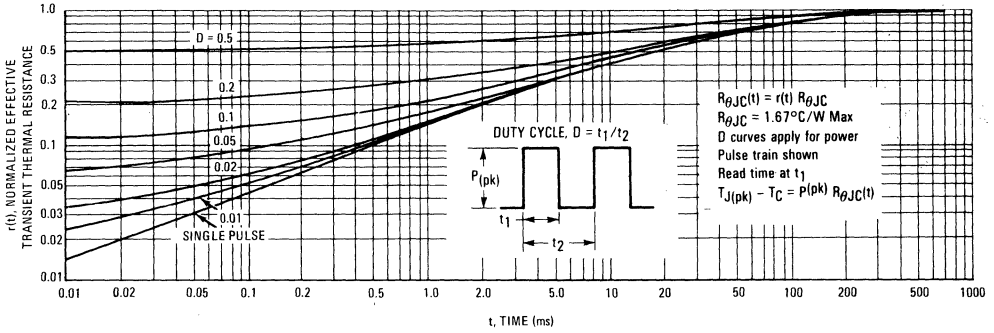
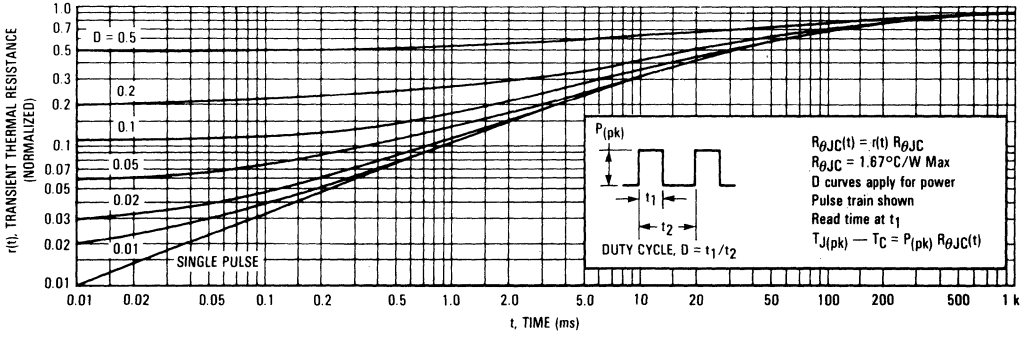


FIGURE 12 — MTP2P45/MTP2P50



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

MTM3N35, MTM3N40
MTP3N35, MTP3N40

MOTOROLA

C

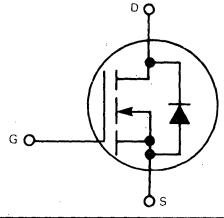
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

TMOS™

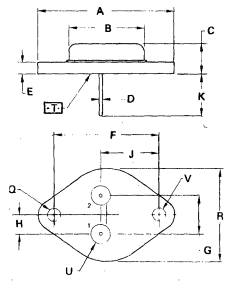


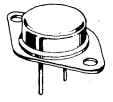
3.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 3.3 OHMS
350 and 400 VOLTS

MTM3N35
MTM3N40



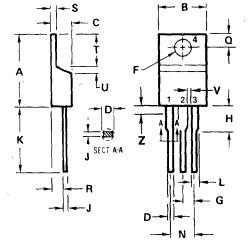


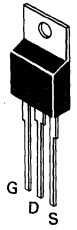
STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-05
TO-204AA
(TO-3 TYPE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

MTP3N35
MTP3N40





STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

MAXIMUM RATINGS

Rating	Symbol	MTM3N35 MTP3N35	MTM3N40 MTP3N40	Unit
Drain-Source Voltage	V_{DSS}	350	400	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	350	400	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 3.0 8.0		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R\theta_{JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM3N35/MTP3N35 MTM3N40/MTP3N40	$V_{(BR)DSS}$	350 400	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 1.5 Adc) (I_D = 3.0 Adc) (I_D = 1.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	5.0 12 10	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$r_{DS(on)}$	—	3.3	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 1.5 A)		g_{fs}	0.75	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	100	pF
Reverse Transfer Capacitance		C_{rss}	—	50	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 1.5 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	60	ns
Turn-Off Delay Time		$t_{d(off)}$	—	60	ns
Fall Time		t_f	—	30	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 3.0 A V_{GS} = 0	V_{SD}	1.0	Vdc
Forward Turn-On Time		t_{on}	190	ns
Reverse Recovery Time		t_{rr}	300	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

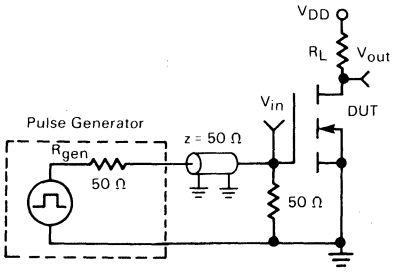
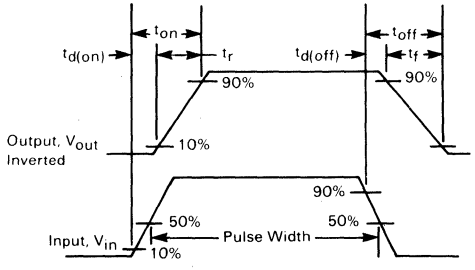


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

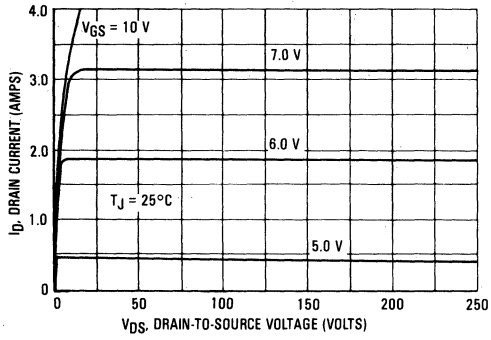
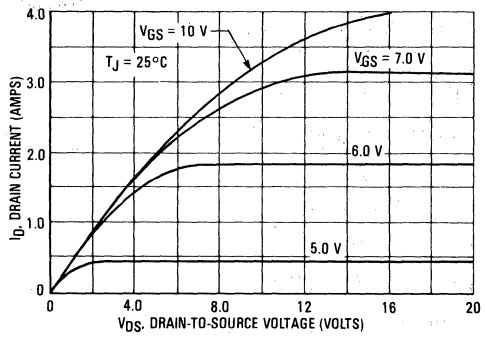


FIGURE 4 — ON-CHARACTERISTICS



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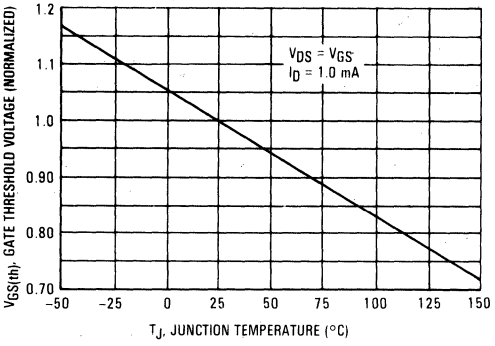

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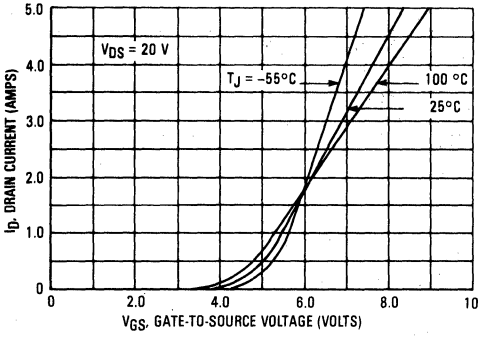

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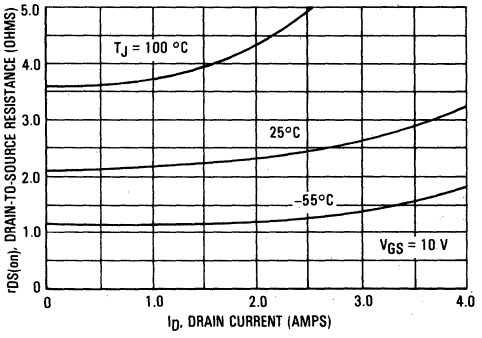

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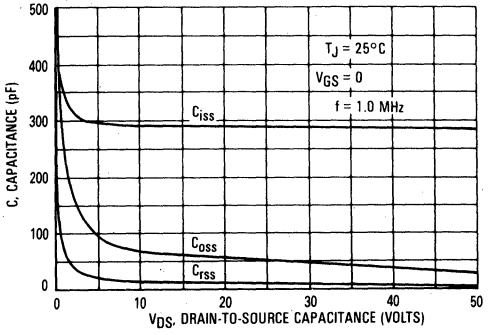


SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

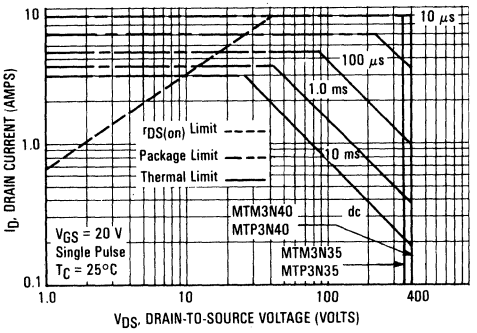
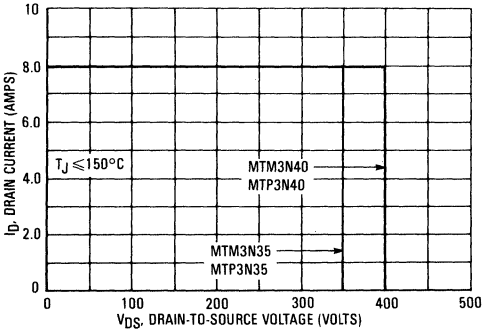


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

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$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figures 11 or 12.

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The switching safe operating area (SOA) of Figure 10 is the boundary that the load line may traverse without incurring damage to the MOSFET. The Fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

C

THERMAL RESPONSE

FIGURE 11 — MTM3N35/MTM3N40

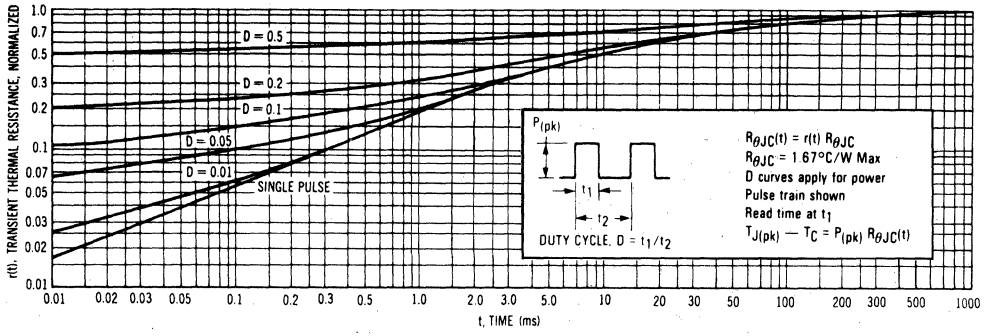
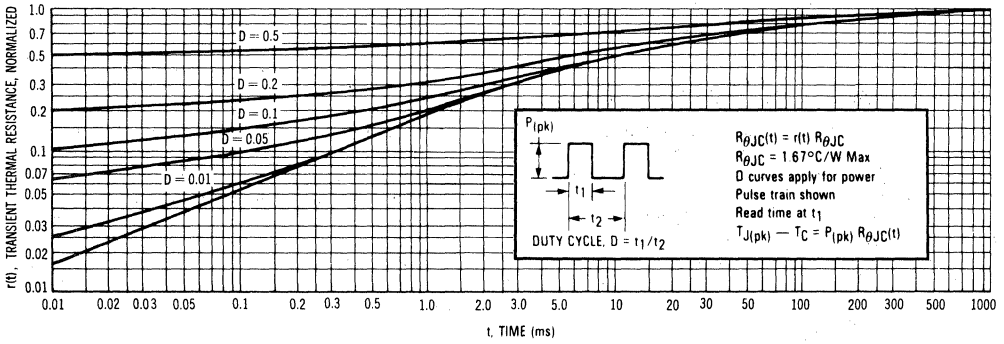


FIGURE 12 — MTP3N35/MTP3N40



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MOTOROLA

MTM3N55, MTM3N60
MTP3N55, MTP3N60

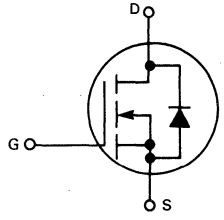
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

TMOS™

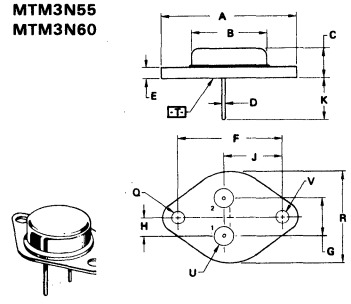


3.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 2.5 OHMS
550 and 600 VOLTS

MTM3N55
MTM3N60

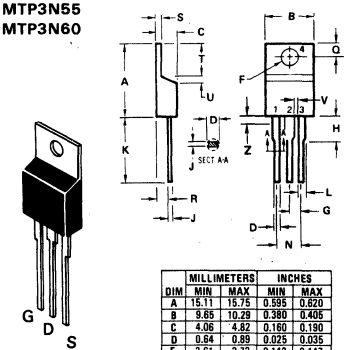


STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA
(TO-3 TYPE)

MTP3N55
MTP3N60



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM3N55 MTP3N55	MTM3N60 MTP3N60	Unit
Drain-Source Voltage	V_{DSS}	550	600	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	550	600	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 3.0 10		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM3N55/MTP3N55 MTM3N60/MTP3N60	$V_{(BR)DSS}$	550 600	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 1.5 Adc) (I_D = 3.0 Adc) (I_D = 1.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	3.75 9.0 7.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$r_{DS(on)}$	—	2.5	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 1.5 A)		g_{fs}	1.5	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 1.5 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	100	ns
Turn-Off Delay Time		$t_{d(off)}$	—	180	ns
Fall Time		t_f	—	80	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 3.0 A V_{GS} = 0, di/dt = 25 A/μs	V_{SD}	1.1	Vdc
Forward Turn-On Time		t_{on}	70	ns
Reverse Recovery Time		t_{rr}	165	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

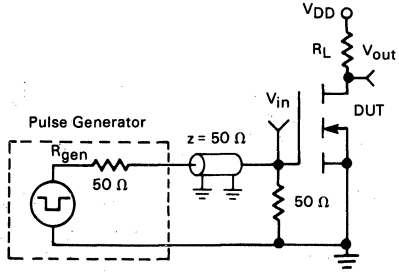


FIGURE 2 — SWITCHING WAVEFORMS

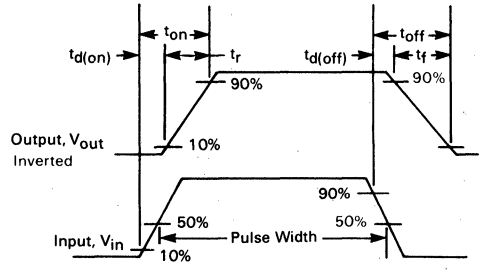


FIGURE 3 — OUTPUT CHARACTERISTICS

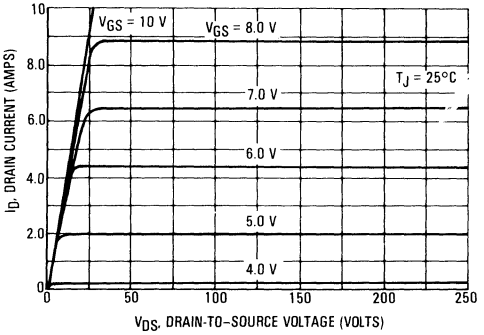


FIGURE 4 — ON-REGION CHARACTERISTICS

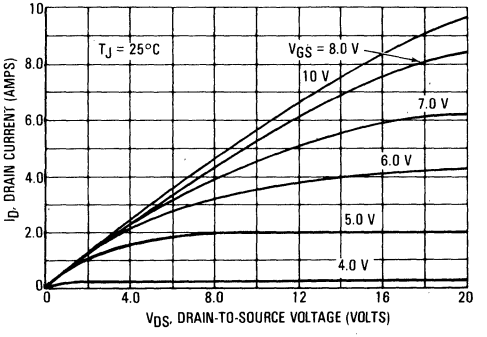


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

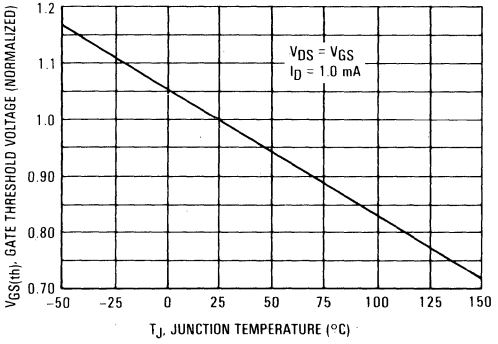


FIGURE 6 — TRANSFER CHARACTERISTICS

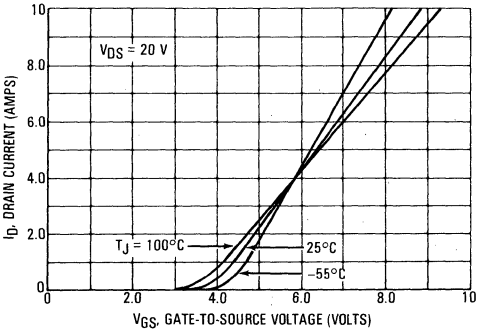


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

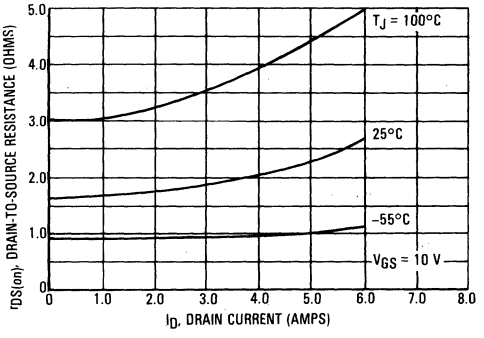
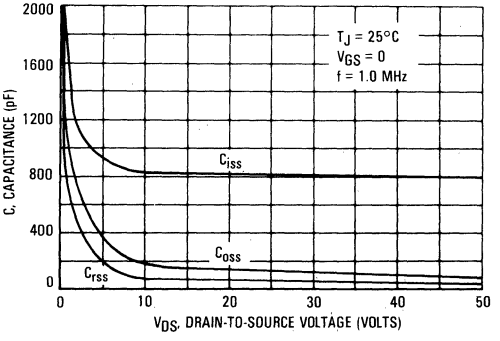


FIGURE 8 — CAPACITANCE VARIATION



C

SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM FORWARD BIASED SAFE OPERATING AREA

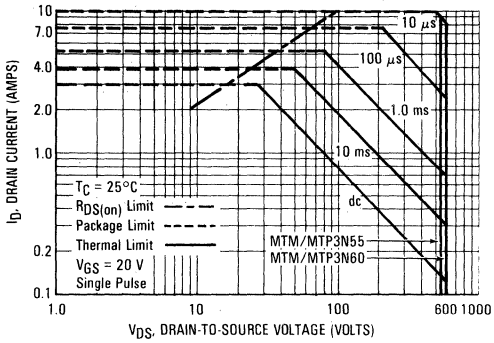
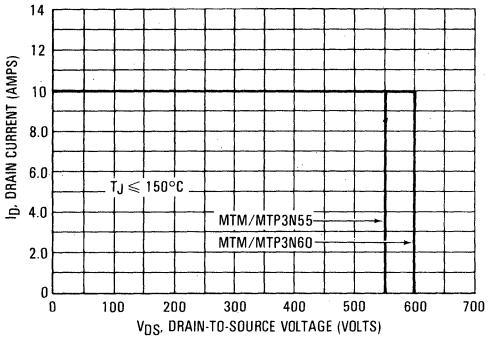


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
$r(t)$ = normalized thermal response from Figures 11 or 12.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10 is the boundary that the load line may traverse without incurring damage to the MOSFET. The Fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 2.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

THERMAL RESPONSE

FIGURE 11 — MTM3N55/MTM3N60

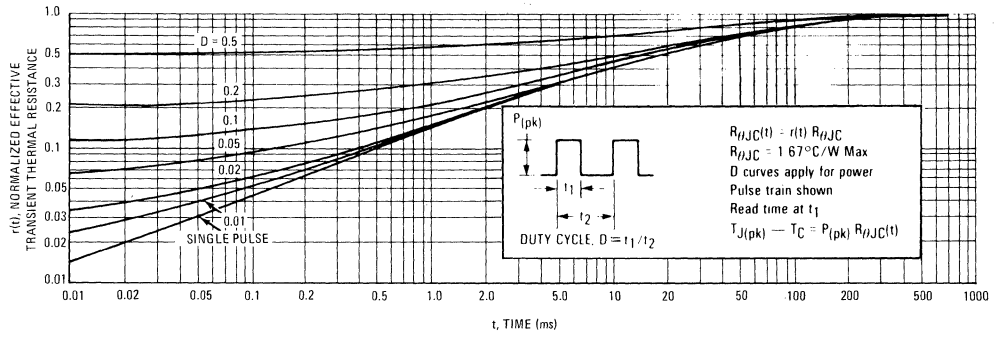
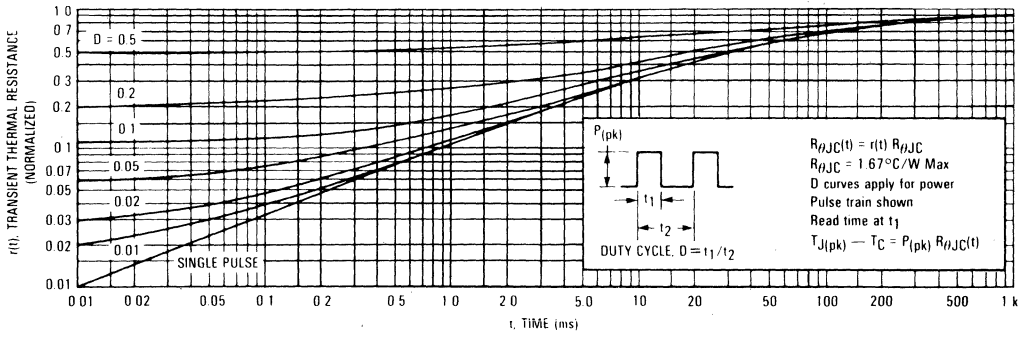


FIGURE 12 — MTP3N55/MTP3N60



MTM3N75 MTP3N75
MTM3N80 MTP3N80

MOTOROLA

C

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

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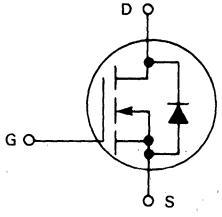
- Designers Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)

TMOS™

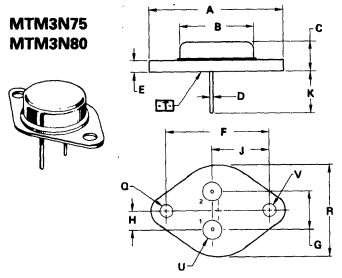


3.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 7.0 OHMS
750 and 800 VOLTS

MTM3N75
MTM3N80



STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
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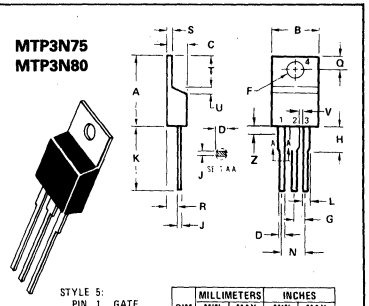
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

TO-204AA
CASE 1-05
(FORMERLY TO-3)

MTP3N75
MTP3N80



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
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K	12.70	14.27	0.500	0.562
L	1.14	1.38	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

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Drain-Gate Voltage (R_{GS} = 1.0 mΩ)	V_{DGR}	750	800	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 3.0 8.0		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM3N75/MTP3N80 MTM3N75/MTP3N80	$V_{(BR)DSS}$	750 800	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 1.5 Adc) (I_D = 3.0 Adc) (I_D = 1.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	10.5 21.0 21.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$r_{DS(on)}$	—	7.0	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 1.5 A)		g_{fs}	0.5	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 1.5 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 3.0 A	V_{SD}	1.0	Vdc
Forward Turn-On Time	V_{GS} = 0	t_{on}	250	ns
Reverse Recovery Time	See Figures 14 and 15	t_{rr}	420	ns

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

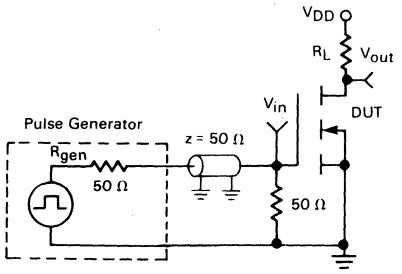
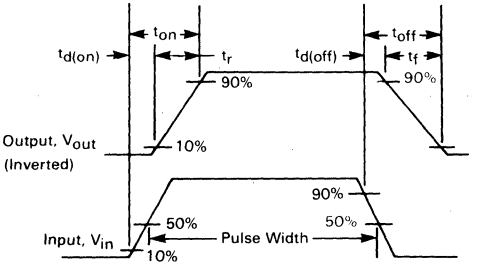


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

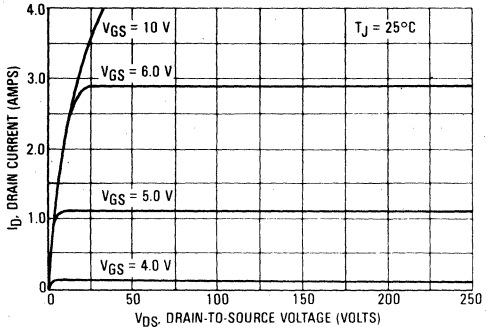


FIGURE 4 — ON-REGION CHARACTERISTICS

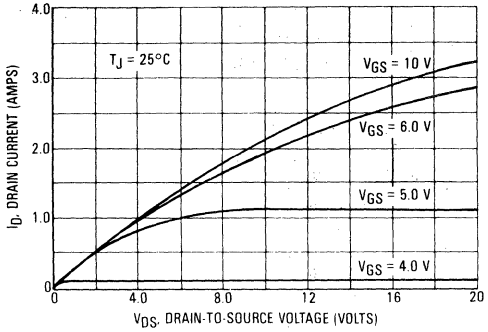


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

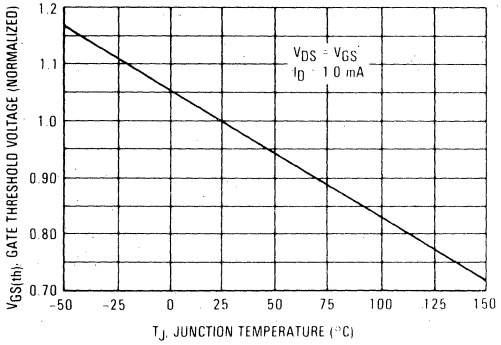


FIGURE 6 — TRANSFER CHARACTERISTICS

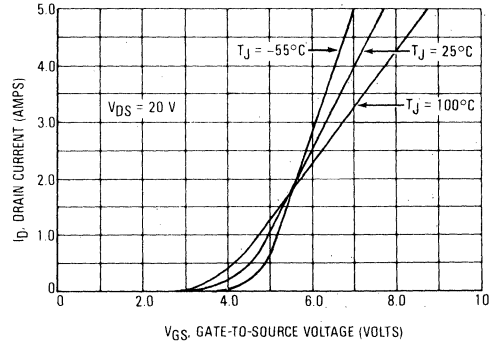


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

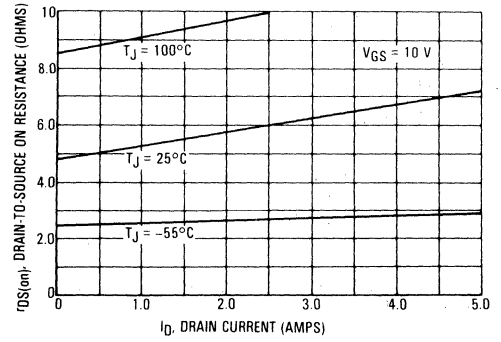
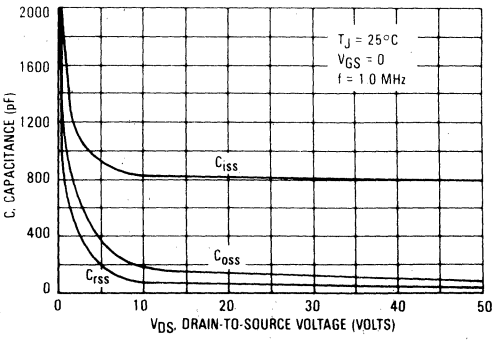


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

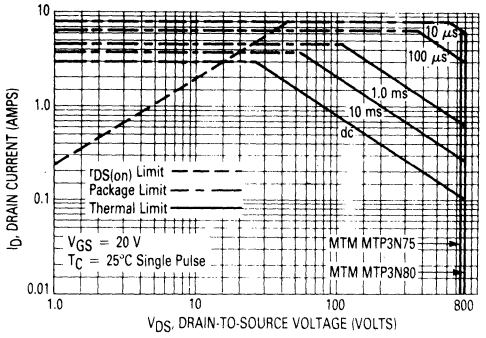
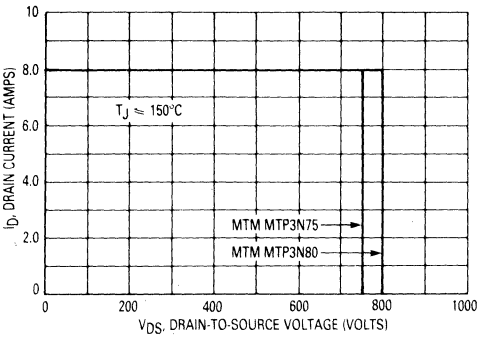


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 9 and 13.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figure 11 or Figure 12.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

THERMAL RESPONSE

C

FIGURE 11 — MTM3N75/MTM3N80

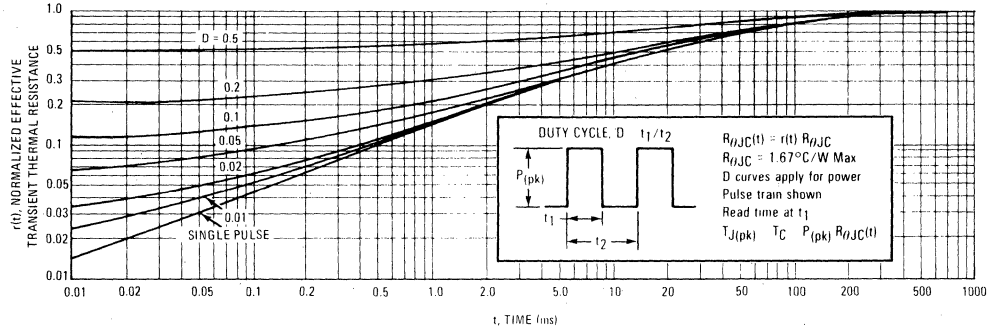
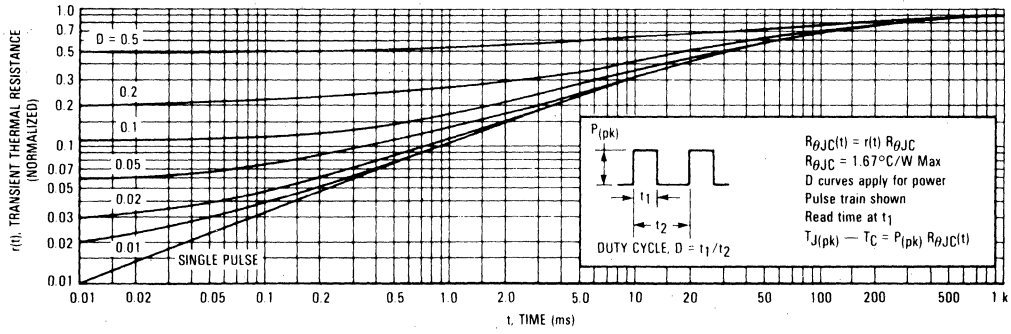


FIGURE 12 — MTP3N75/MTP3N80



MOTOROLA

MTM4N45, MTP4N45
MTM4N50, MTP4N50
MTM5N35, MTP5N35
MTM5N40, MTP5N40

C

Designer's Data Sheet

4.0 and 5.0 AMPERE
N-CHANNEL TMOS POWER FET
$r_{DS(on)}$ = 1.5 OHMS
450 and 500 VOLTS

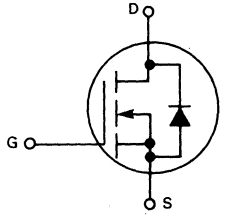
$r_{DS(on)}$ = 1.0 OHM
350 and 400 VOLTS

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

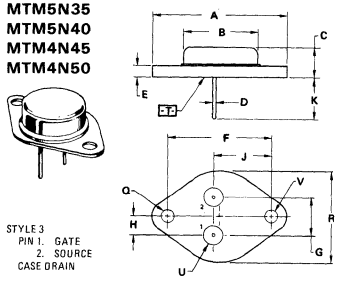
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



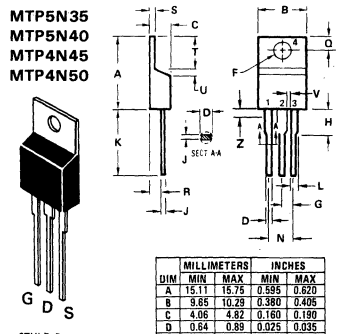
MTM5N35
MTM5N40
MTM4N45
MTM4N50



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(TO-3 TYPE)

MTP5N35
MTP5N40
MTP4N45
MTP4N50



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.85	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 5N35	MTM or MTP 5N40	MTM or MTP 4N45	MTM or MTP 4N50	Unit
Drain-Source Voltage	V_{DSS}	350	400	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	350	400	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous / Pulsed	I_D / I_{DM}	5.0 / 12		4.0 / 10		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C / Derate above 25°C	P_D	75 / 0.6				Watts / W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM5N35/MTP5N35	$V_{(BR)DSS}$	350	—	Vdc
	MTM5N40/MTP5N40		400	—	
	MTM4N45/MTP4N45		450	—	
	MTM4N50/MTP4N50		500	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	MTM5N35/MTM5N40 MTP5N35/MTP5N40	$r_{DS(on)}$	—	1.0	Ohms
(V_{GS} = 10 Vdc, I_D = 2.0 Adc)	MTM4N45/MTM4N50 MTP4N45/MTP4N50		—	1.5	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5.0 Adc)	MTM5N35/MTM5N40 MTP5N35/MTP5N40	$V_{DS(on)}$	—	6.2	Vdc
(I_D = 2.5 Adc, T_J = 100°C)	MTM4N45, MTM4N50 MTP4N45/MTP4N50		—	5.0	
(I_D = 4.0 Adc)	MTM5N35, MTM5N40 MTP5N35/MTP5N40		—	7.5	
(I_D = 2.0 Adc, T_J = 100°C	MTM4N45/MTM4N50 MTP4N45/MTP4N50		—	6.0	
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)	MTM5N35/MTM5N40 MTP5N35/MTP5N40	g_{fs}	2.0	—	mhos
(V_{DS} = 15 V, I_D = 2.0 A)	MTM4N45/MTM4N50 MTP4N45/MTP4N50		1.5	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, f = 1.0 MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	100	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0,	V_{SD}	1.1	Vdc
Forward Turn-On Time		t_{on}	250	ns
Reverse Recovery Time		t_{rr}	420	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

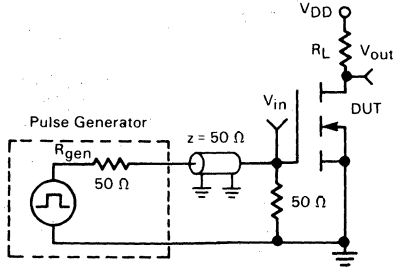
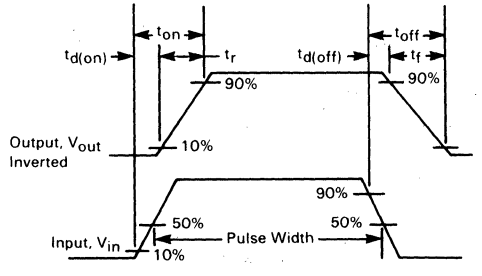


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTM5N35, MTM5N40
MTP5N35, MTP5N40

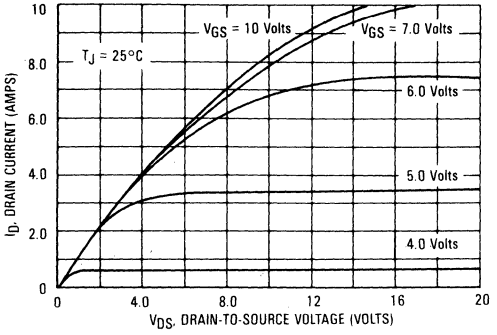
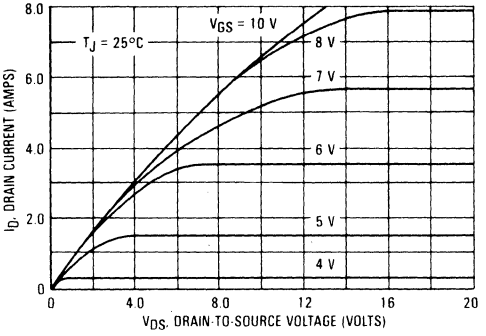


FIGURE 4 — MTM4N45, MTM4N50
MTP4N45, MTP4N50



TRANSFER CHARACTERISTICS

FIGURE 5 — MTM5N35, MTM5N40
MTP5N35, MTP5N40

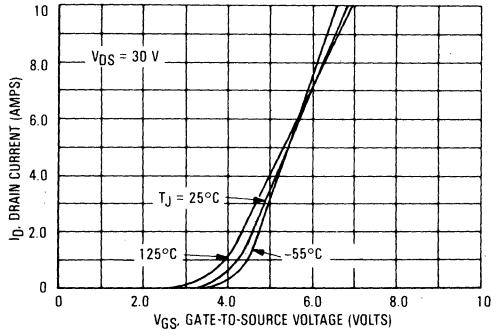
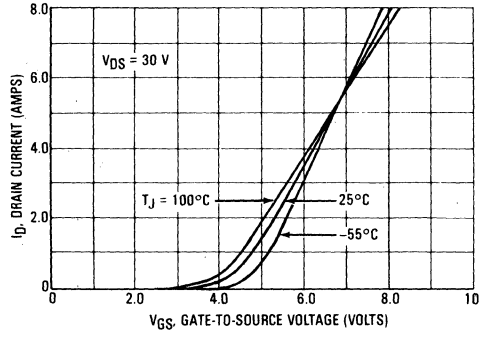


FIGURE 6 — MTM4N45, MTM4N50
MTP4N45, MTP4N50



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — ON-RESISTANCE versus DRAIN CUURRENT

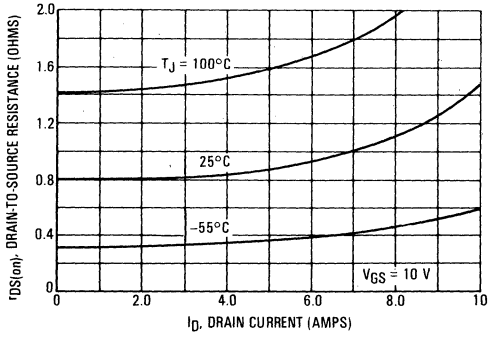
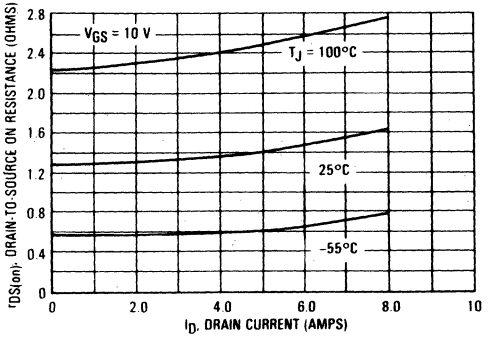


FIGURE 8 — MTM4N45, MTM4N50
MTP4N45, MTP4N50



C

TYPICAL CHARACTERISTICS (continued)

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

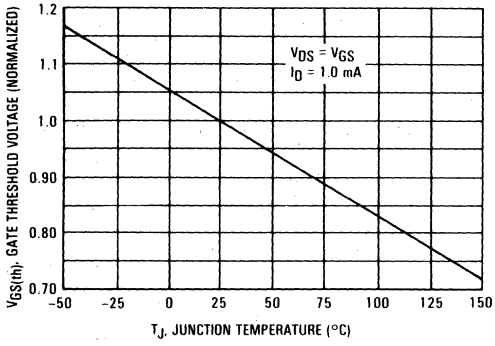
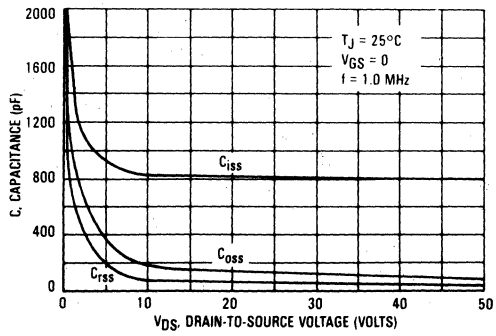


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM4N45, MTM4N50, MTM5N35, MTM5N40

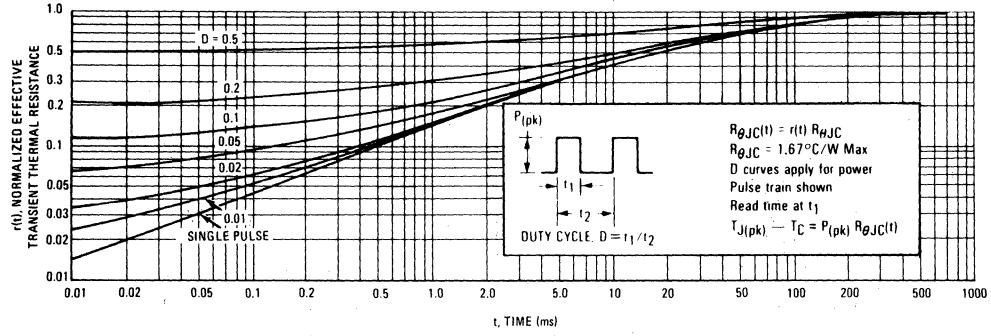
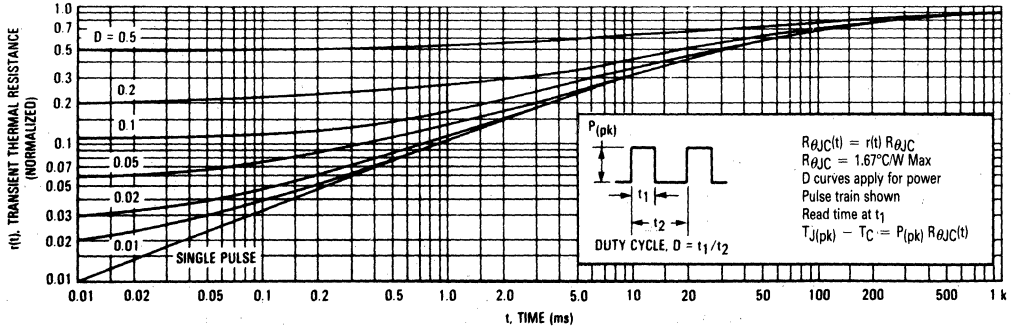


FIGURE 12 — MTP4N45, MTP4N50, MTP5N35, MTP5N40



RATED SAFE OPERATING AREA INFORMATION

FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

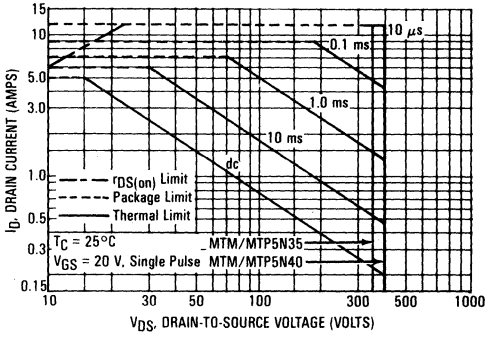


FIGURE 14 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

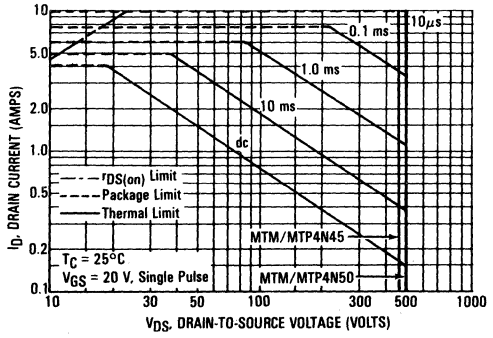
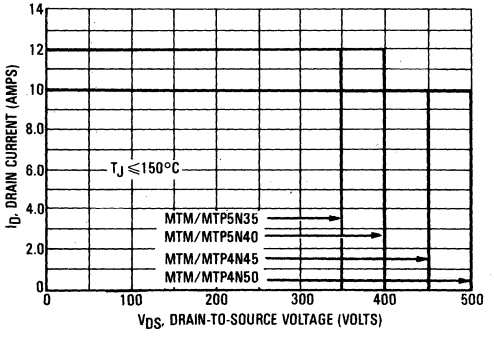


FIGURE 15 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 13 and 14 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 13 and 14
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
$r(t)$ = normalized thermal response from Figures 11 and 12

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 15, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MTM5N18, MTP5N18
MTM5N20, MTP5N20
MTM7N12, MTP7N12
MTM7N15, MTP7N15

MOTOROLA

C

Designer's Data Sheet

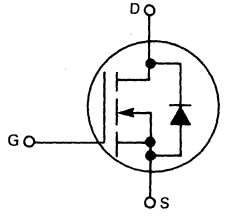
5.0 and 7.0 AMPERE
N-CHANNEL TMOS POWER FET
$r_{DS(on)}$ = 1.0 OHM
180 and 200 VOLTS
$r_{DS(on)}$ = 0.7 OHM
120 and 150 VOLTS

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

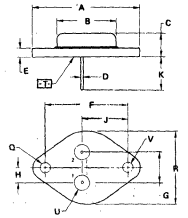
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

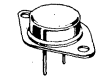


MTM5N18
MTM5N20
MTM7N12
MTM7N15



STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⌖ ⌀.13 (0.005) M T V M
FOR LEADS:
⌖ ⌀.13 (0.005) M T V M Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.



CASE 1-05
TO-204AA
(TO-3 TYPE)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 7N12	7N15	5N18	5N20	Unit
Drain-Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous	I_D	7.0		5.0		Adc
Pulsed	I_{DM}	18		15		
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C	P_D	75				Watts
Derate above 25°C		0.6				W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

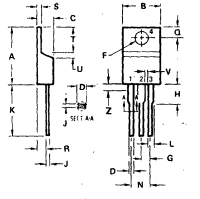
THERMAL CHARACTERISTICS

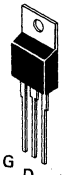
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

MTP5N18
MTP5N20
MTP7N12
MTP7N15





STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3 ONLY.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.
5. CONTROLLING DIMENSION: INCH.

CASE 221A-02
TO-220AB

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	
Z	–	2.03	–	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM7N12/MTP7N12	$V_{(BR)DSS}$	120	—	Vdc
	MTM7N15/MTP7N15		150	—	
	MTM5N18/MTP5N18		180	—	
	MTM5N20/MTP5N20		200	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc)	MTM7N12/MTM7N15 MTP7N12/MTP7N15	$r_{DS(on)}$	—	0.7	Ohms
(V_{GS} = 10 Vdc, I_D = 2.5 Adc)	MTM5N18/MTM5N20 MTP5N18/MTP5N20		—	1.0	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 7.0 Adc)	MTM7N12/MTM7N15 MTP7N12/MTP7N15		—	5.9	
(I_D = 3.5 Adc, T_J = 100°C)	MTM5N18, MTM5N20 MTP5N18/MTP5N20		—	5.0	
(I_D = 5.0 Adc)	MTM7N12/MTM7N15 MTP7N12/MTP7N15		—	6.0	
(I_D = 2.5 Adc, T_J = 100°C)	MTM5N18/MTM5N20 MTP5N18/MTP5N20		—	5.0	
Forward Transconductance (V_{DS} = 15 V, I_D = 3.5 A)	MTM7N12/MTM7N15 MTP7N12/MTP7N15	g_{fs}	1.5	—	mhos
(V_{DS} = 15 V, I_D = 2.5 A)	MTM5N18/MTM5N20 MTP5N18/MTP5N20		1.5	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	175	pF
Reverse Transfer Capacitance		C_{rss}	—	30	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms, See Figures 1 and 2)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	50	ns
Fall Time		t_f	—	50	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0,	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	200	ns
Reverse Recovery Time		t_{rr}	300	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 1 — SWITCHING TEST CIRCUIT

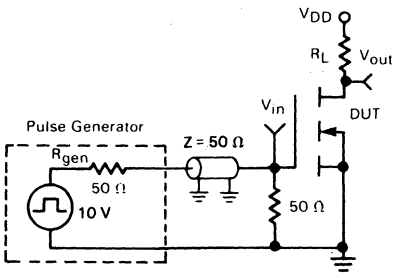
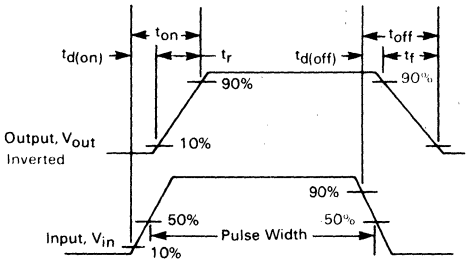


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTM5N18, MTM5N20
MTP5N18, MTP5N20

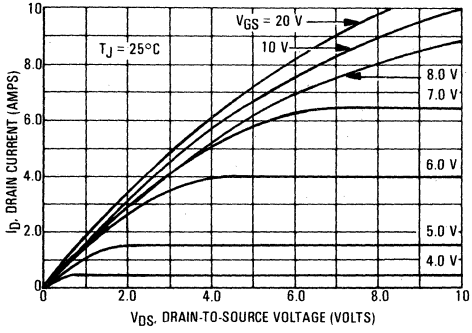
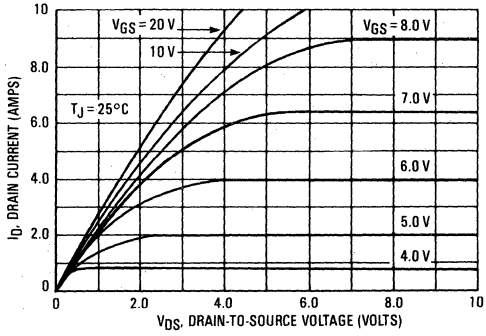


FIGURE 4 — MTM7N12, MTM7N15
MTP7N12, MTP7N15



TRANSFER CHARACTERISTICS

FIGURE 5 — MTM5N18, MTM5N20
MTP5N18, MTP5N20

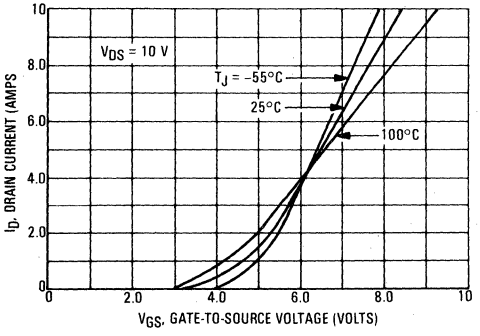
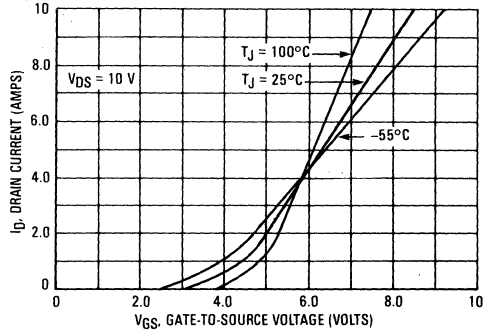


FIGURE 6 — MTM7N12, MTM7N15
MTP7N12, MTP7N15



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTM5N18, MTM5N20
MTP5N18, MTP5N20

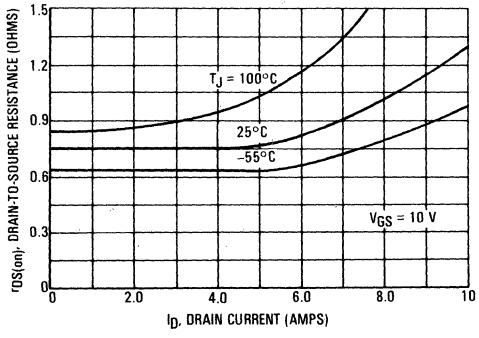
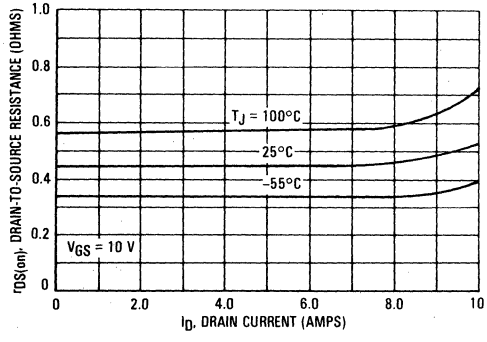


FIGURE 8 — MTM7N12, MTM7N15
MTP7N12, MTP7N15



TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

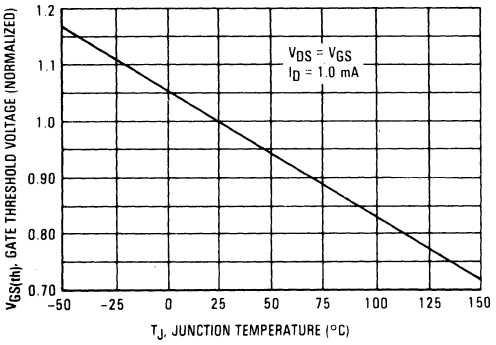
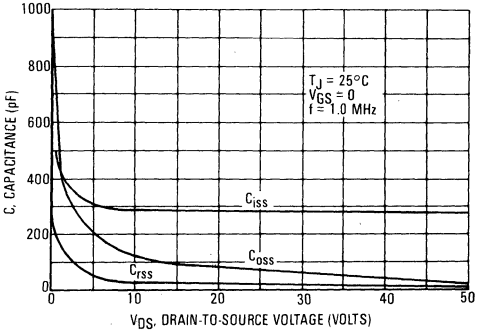


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM7N12, MTM7N15, MTM5N18 AND MTM5N20

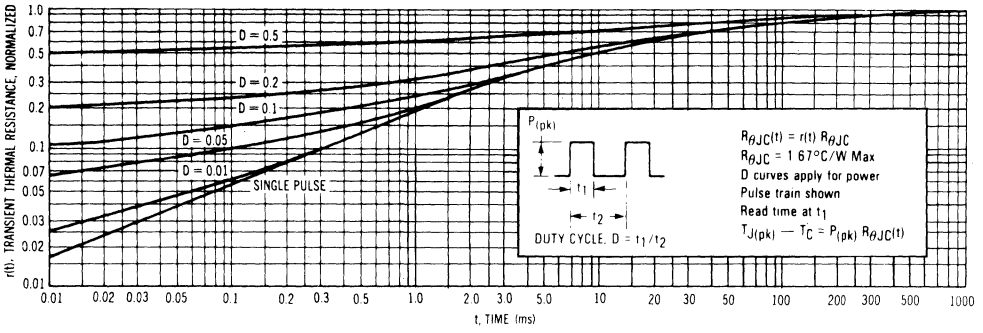
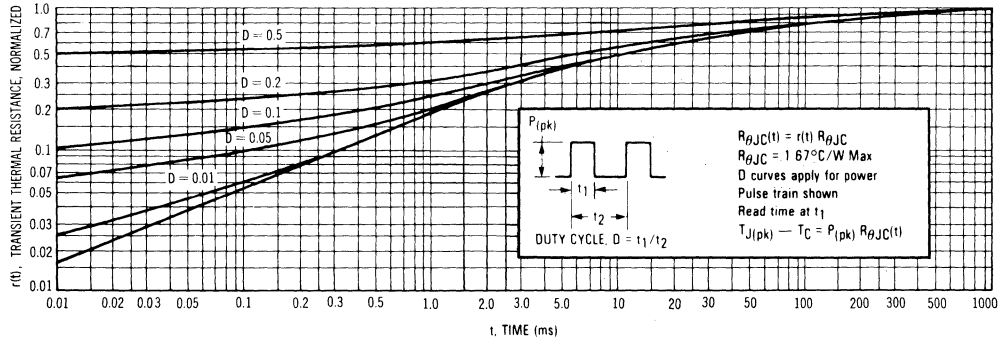


FIGURE 12 — MTP7N12, MTP7N15, MTP5N18 AND MTP5N20



C

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 13 — MTM5N18, MTM5N20
MTP5N18, MTP5N20

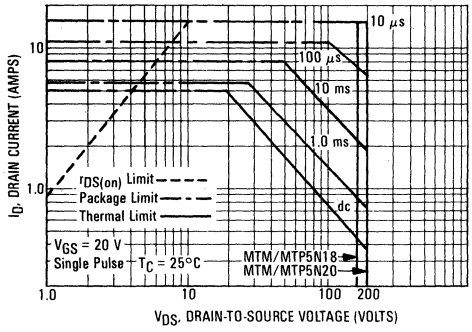
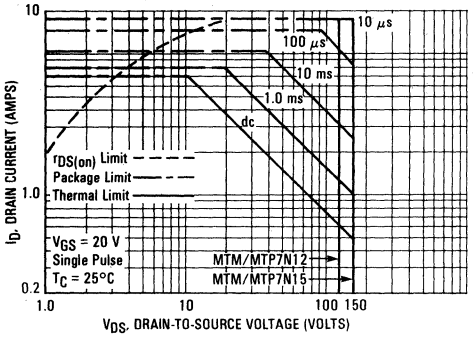


FIGURE 14 — MTM7N12, MTM7N15
MTP7N12, MTP7N15



FORWARD BIASED SAFE OPERATING AREA

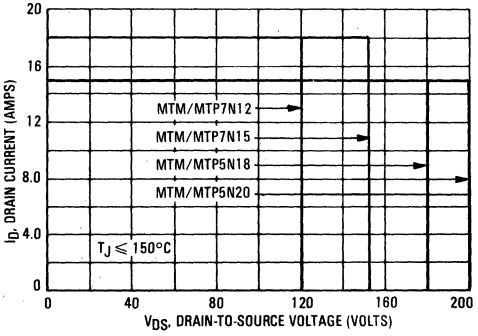
The dc data of Figures 13 and 14 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 13 and 14
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
$r(t)$ = normalized thermal response from Figures 11 and 12

FIGURE 15 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 15, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 15 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MOTOROLA

MTM6N55
MTM6N60
MTH6N55
MTH6N60

C

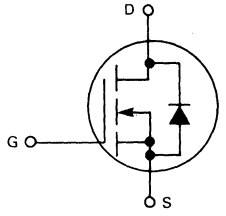
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

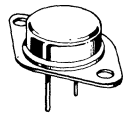


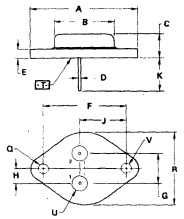
6.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 1.2 OHMS
550 and 600 VOLTS

MTM6N55
MTM6N60



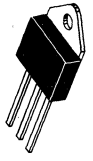


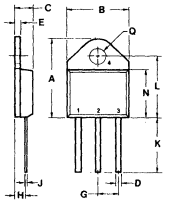
STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.87	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(Formerly TO-3)

MTH6N55
MTH6N60





STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTM6N55 MTH6N55	MTM6N60 MTH6N60	Unit
Drain – Source Voltage	V_{DSS}	550	600	Vdc
Drain – Gate Voltage (R_{GS} = 1.0 mΩ)	V_{DGR}	550	600	Vdc
Gate – Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 6.0 30		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM6N55/MTH6N55 MTM6N60/MTH6N60	$V_{(BR)DSS}$	 550 600	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 BV_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	 2.0 1.5	 4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3.0 Adc) (I_D = 6.0 Adc) (I_D = 3.0 Adc, T_J = 100°C)		$V_{DS(on)}$	 — — —	 3.6 9.0 7.2	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$r_{DS(on)}$	—	1.2	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 3.0 A)		g_{fs}	2.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	pF
Reverse Transfer Capacitance		C_{rss}	—	150	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 125 V, I_D = 3.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	120	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 6.0 A	V_{SD}	1.3	Vdc
Forward Turn-On Time	V_{GS} = 0, di/dt = 25 A/μs	t_{on}	175	ns
Reverse Recovery Time		t_{rr}	600	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

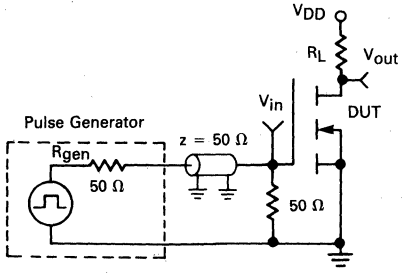
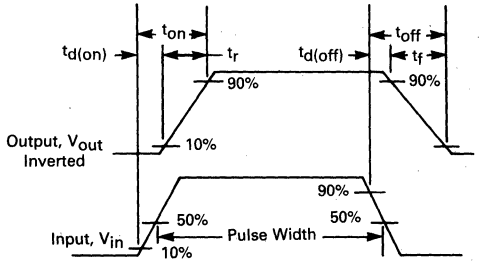


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

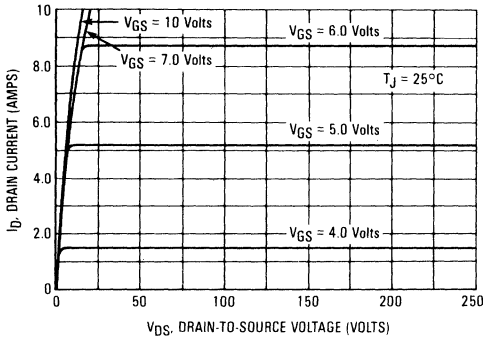


FIGURE 4 — ON-REGION CHARACTERISTICS

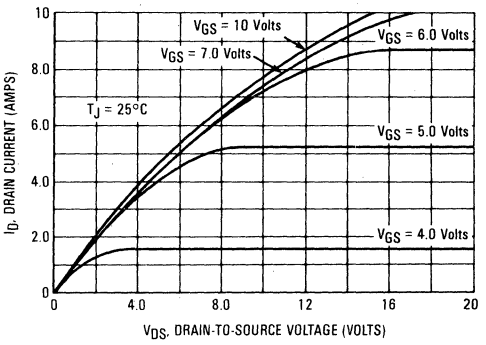


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

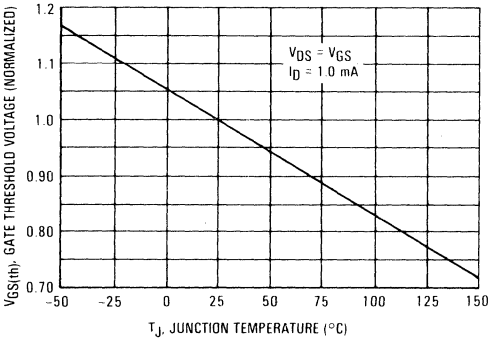


FIGURE 6 — TRANSFER CHARACTERISTICS

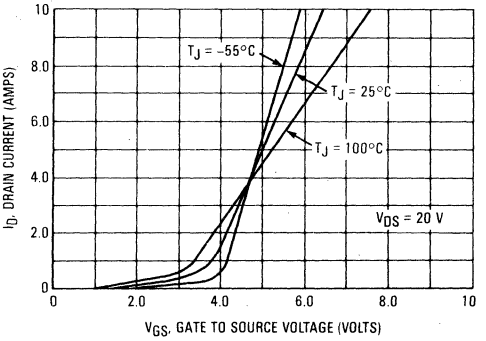


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

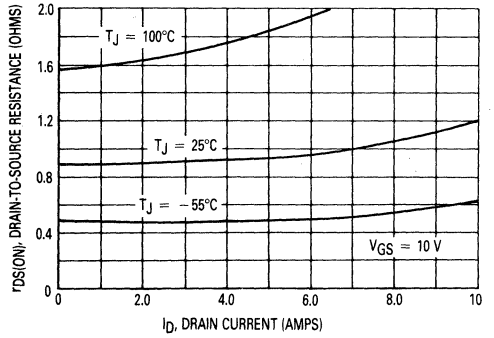
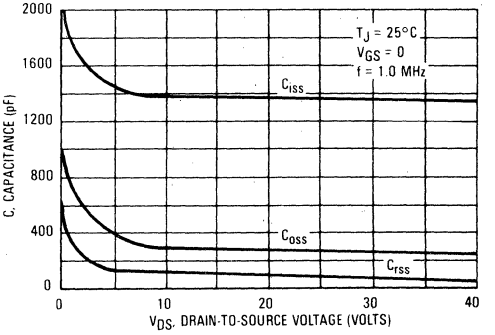


FIGURE 8 — CAPACITANCE VARIATION



C

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

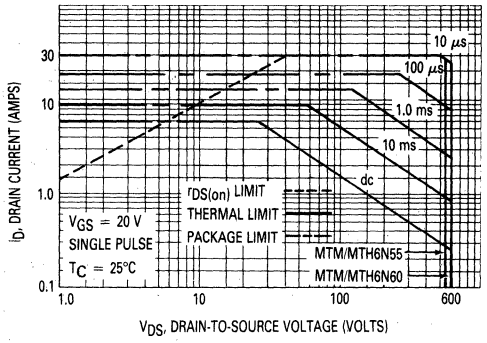
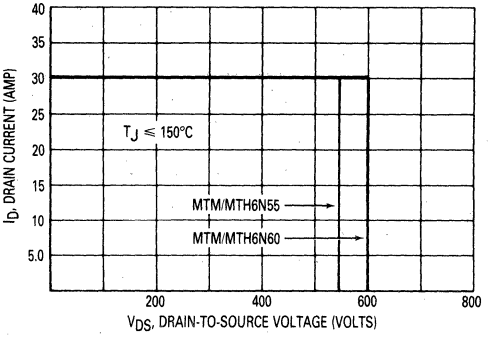


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11

SWITCHING SAFE OPERATING AREA

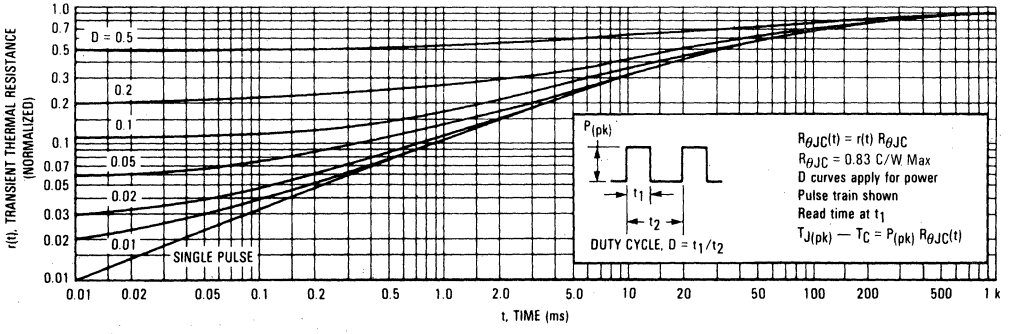
The switching safe opprating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

THERMAL RESPONSE

FIGURE 11 — MTM6N55/MTM6N60/MTH6N55/MTH6N60



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

MTM7N18, MTP7N18
MTM7N20, MTP7N20
MTM8N12, MTP8N12
MTM8N15, MTP8N15

MOTOROLA

C

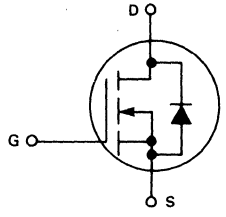
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

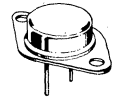
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

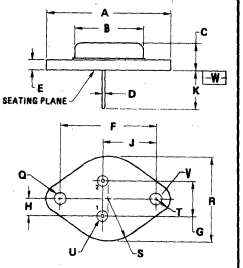
TMOS™



7.0 and 8.0 AMPERE
N-CHANNEL TMOS POWER FET
$r_{DS(on)}$ = 0.7 OHM
180 and 200 VOLTS
$r_{DS(on)}$ = 0.5 OHM
120 and 150 VOLTS

MTM7N18
MTM7N20
MTM8N12
MTM8N15



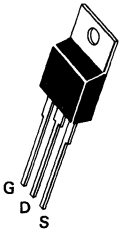


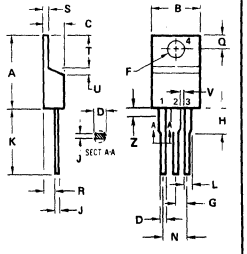
STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA
(TO-3 TYPE)

MTP7N18
MTP7N20
MTP8N12
MTP8N15





STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 8N12	8N15	7N18	7N20	Unit
Drain-Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 8.0 20		 7.0 18		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM8N12/MTP8N12	$V_{(BR)DSS}$	120	—	Vdc
	MTM8N15/MTP8N15		150	—	
	MTM7N18/MTP7N18		180	—	
	MTM7N20/MTP7N20		200	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)	MTM8N12/MTM8N15 MTP8N12/MTP8N15	$r_{DS(on)}$	—	0.5	Ohms
(V_{GS} = 10 Vdc, I_D = 3.5 Adc)	MTM7N18/MTM7N20 MTP7N18/MTP7N20		—	0.7	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 8.0 Adc)	MTM8N12/MTM8N15		—	4.5	
(I_D = 4.0 Adc, T_J = 100°C)	MTP8N12/MTP8N15		—	3.2	
(I_D = 7.0 Adc)	MTM7N18, MTM7N20		—	5.9	
(I_D = 3.5 Adc, T_J = 100°C)	MTP7N18/MTP7N20		—	5.0	
Forward Transconductance (V_{DS} = 15 V, I_D = 4.0 A)	MTM8N12/MTM8N15 MTP8N12/MTP8N15	g_{fs}	2.0	—	mhos
(V_{DS} = 15 V, I_D = 3.5 A)	MTM7N18/MTM7N20 MTP7N18/MTP7N20		1.5	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	700	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	—	300	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 1 and 2	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	100	ns
Fall Time		t_f	—	50	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0,	V_{SD}	1.7	Vdc
Forward Turn-On Time		t_{on}	80	ns
Reverse Recovery Time		t_{rr}	700	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 1 — SWITCHING TEST CIRCUIT

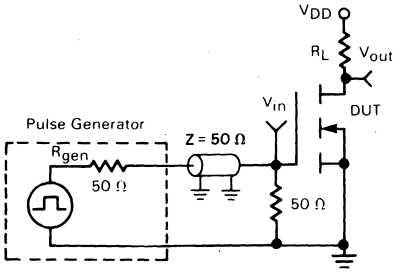
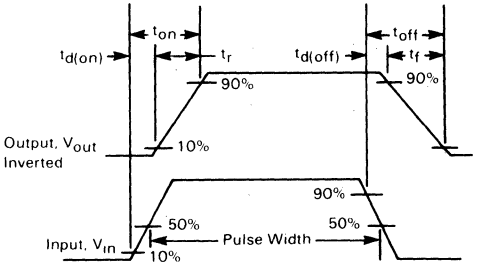


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTM7N18, MTM7N20
MTP7N18, MTP7N20

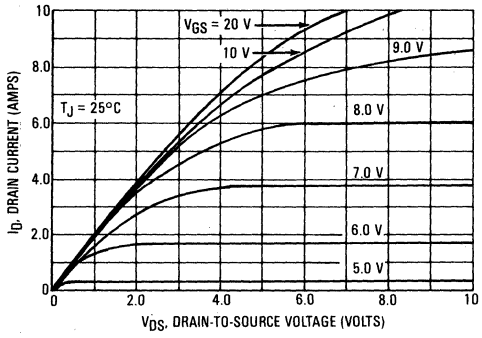
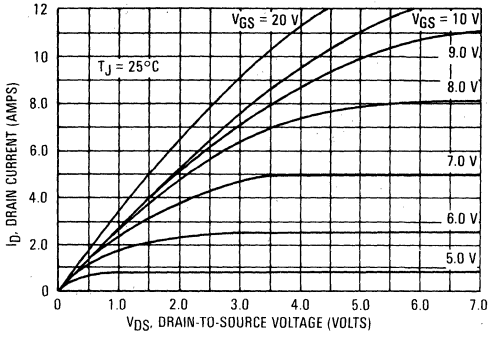


FIGURE 4 — MTM8N12, MTM8N15
MTP8N12, MTP8N15



TRANSFER CHARACTERISTICS

FIGURE 5 — MTM7N18, MTM7N20
MTP7N18, MTP7N20

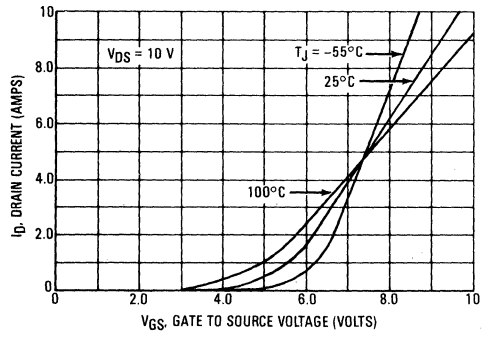
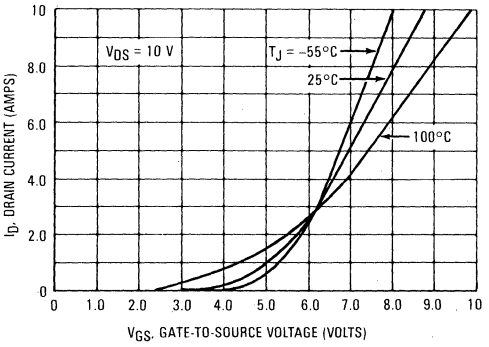


FIGURE 6 — MTM8N12, MTM8N15
MTP8N12, MTP8N15



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTM7N18, MTM7N20
MTP7N18, MTP7N20

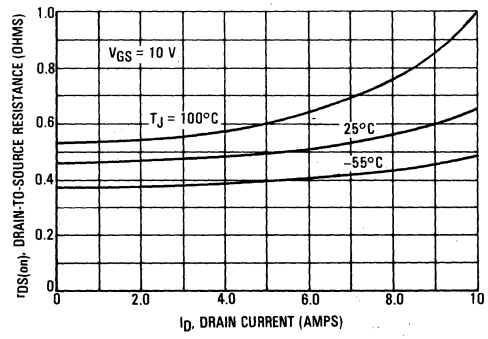
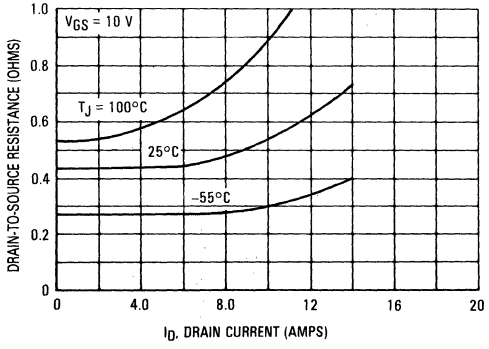


FIGURE 8 — MTM8N12, MTM8N15
MTP8N12, MTP8N15



TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

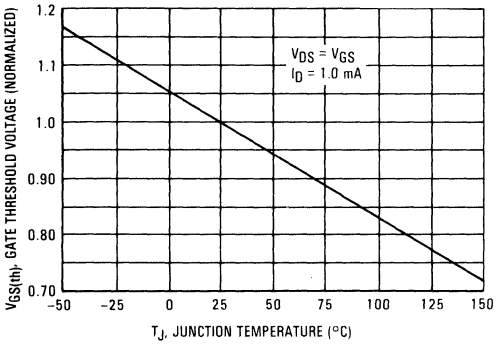
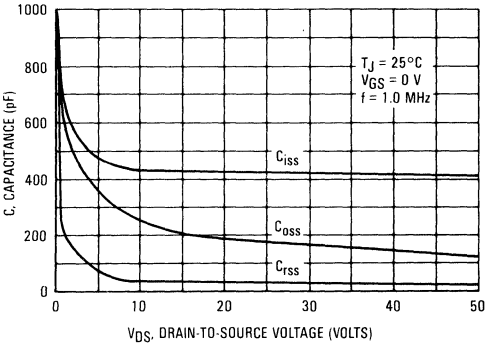


FIGURE 10 — CAPACITANCE VARIATION



C

THERMAL RESPONSE

FIGURE 11 — MTM7N18, MTM7N20, MTM8N12, MTM8N15

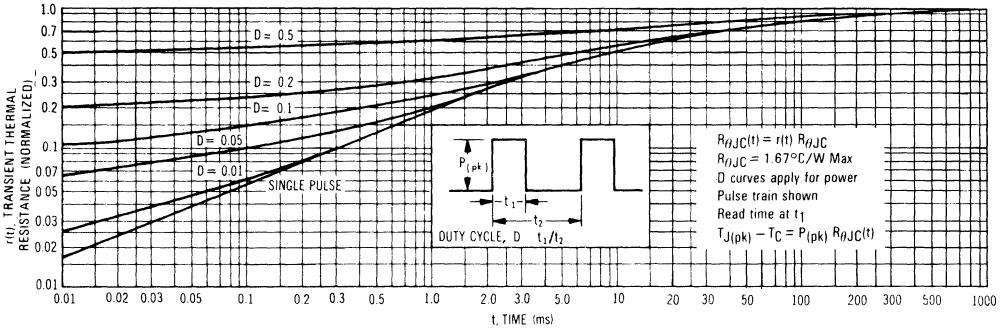
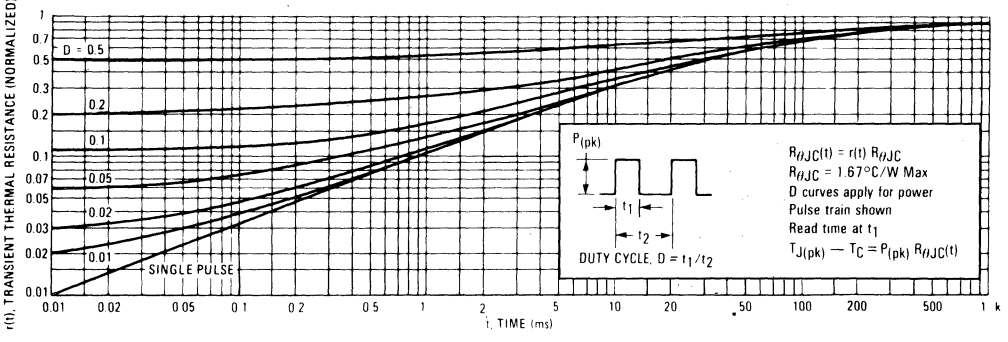


FIGURE 12 — MTP7N18, MTP7N20, MTP8N12, MTP8N15



C

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 13 — MTM7N18, MTM7N20
MTP7N18, MTP7N20

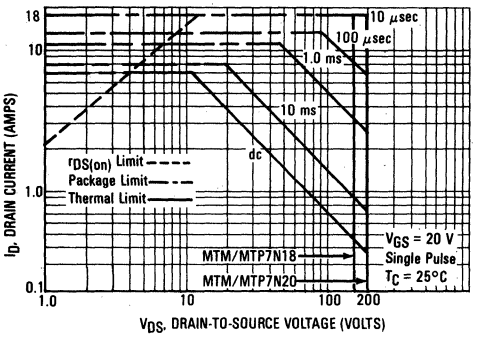
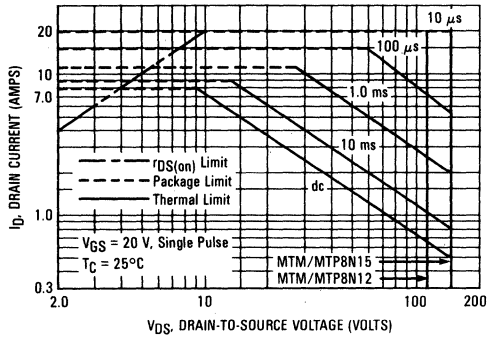


FIGURE 14 — MTM8N12, MTM8N15
MTP8N12, MTP8N15



FORWARD BIASED SAFE OPERATING AREA

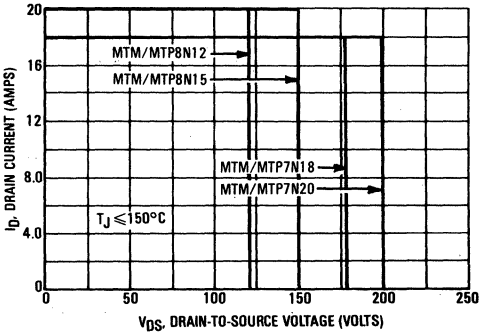
The dc data of Figures 13 and 14 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

Where

- $I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 13 or 14
- $T_{J(max)}$ = rated maximum junction temperature
- T_C = device case temperature
- P_D = rated power dissipation at T_C = 25°C
- $R_{\theta JC}$ = rated steady state thermal resistance
- r(t) = normalized thermal response from Figures 11 and 12

FIGURE 15 — MAXIMUM RATED SWITCHING
SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 15, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 15 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MOTOROLA

MTM7N45 MTH7N45
MTM7N50 MTH7N50
MTM8N35 MTH8N35
MTM8N40 MTH8N40

C

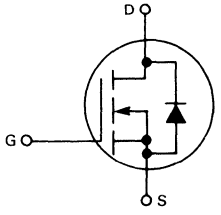
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

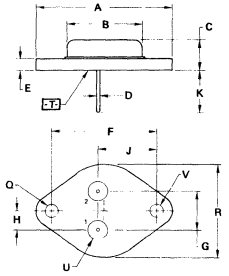


7.0 and 8.0 AMPERE

N-CHANNEL TMOS POWER FETs

$r_{DS(on)}$ = 0.8 OHM
450 and 500 VOLTS
$r_{DS(on)}$ = 0.55 OHM
350 and 400 VOLTS

MTM7N45
MTM7N50
MTM8N35
MTM8N40

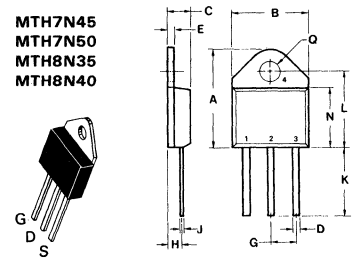


STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	17.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA
(TO-3 TYPE)

MTH7N45
MTH7N50
MTH8N35
MTH8N40



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTM or MTH 8N35	8N40	7N45	7N50	Unit
Drain-Source Voltage	V_{DSS}	350	400	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	350	400	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	I_D I_{DM}	8.0 48		7.0 40		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM8N35/MTH8N35	$V_{(BR)DSS}$	350	—	Vdc
	MTM8N40/MTH8N40		400	—	
	MTM7N45/MTH7N45		450	—	
	MTM7N50/MTH7N50		500	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_C = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)	MTM8N35/MTH8N35	$r_{DS(on)}$	—	0.55	Ohm
	MTM8N40/MTH8N40				
(V_{GS} = 10 Vdc, I_D = 3.5 Adc)	MTM7N45/MTH7N45		—	0.80	
	MTM7N50/MTH7N50				
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 8.0 Adc)	MTM8N35/MTH8N35		—	5.3	
	MTM8N40/MTH8N40				
(I_D = 4.0 Adc, T_J = 100°C)	MTM8N35/MTH8N35		—	4.4	
	MTM8N40/MTH8N40				
(I_D = 7.0 Adc)	MTM7N45/MTH7N45		—	7.0	
	MTM7N50/MTH7N50				
(I_D = 3.5 Adc, T_C = 100°C)	MTM7N45/MTH7N45		—	5.6	
	MTM7N50/MTH7N50				
Forward Transconductance (V_{DS} = 10 V, I_D = 4.0 A)	MTM8N35/MTH8N35	g_{fs}	3.0	—	mhos
	MTM8N40/MTH8N40				
(V_{DS} = 10 V, I_D = 3.5 A)	MTM7N45/MTH7N45		2.0	—	
	MTM7N50/MTH7N50				

DYNAMIC CHARACTERISTICS

Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	150	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 10 and 11	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	120	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = Rated I_D V_{GS} = 0	V_{SD}	1.1 (1)	Vdc
Forward Turn-On Time		t_{on}	175	ns
Reverse Recovery Time		t_{rr}	600	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.
(1) Add 0.5 V to V_{SD} for MTM/MTH8N35 and MTM/MTH8N40.

TYPICAL CHARACTERISTICS

MTM7N45, MTM7N50, MTH7N45, MTH7N50

MTM8N35, MTM8N40, MTH8N35, MTH8N40

FIGURE 1 — ON-REGION CHARACTERISTICS

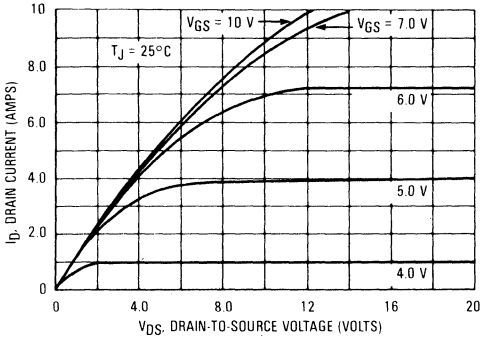


FIGURE 2 — ON-REGION CHARACTERISTICS

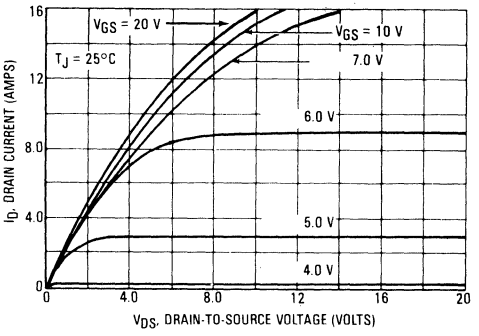


FIGURE 3 — TRANSFER CHARACTERISTICS

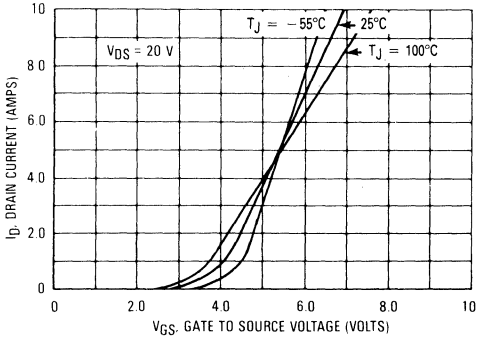


FIGURE 4 — TRANSFER CHARACTERISTICS

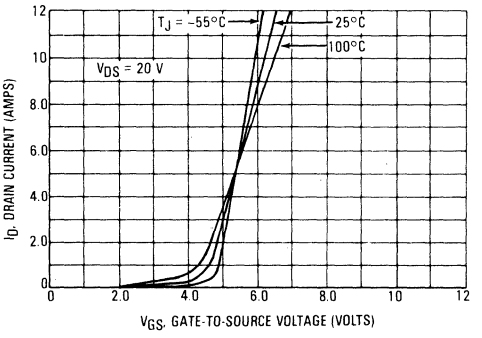


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT

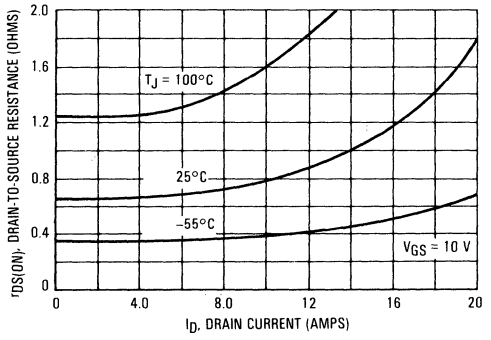
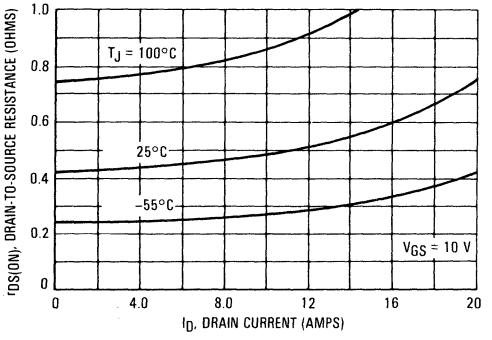


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT



C

C

TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

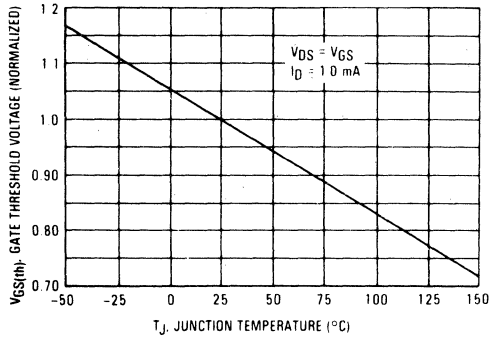


FIGURE 8 — CAPACITANCE VARIATION

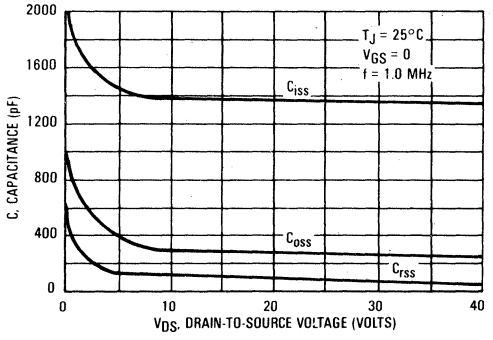
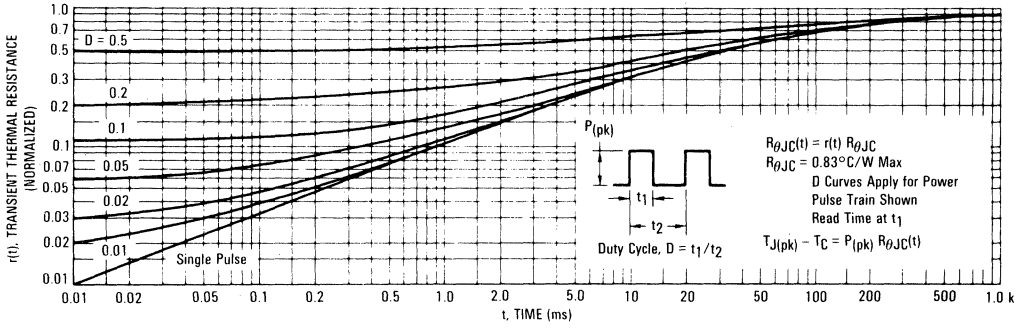


FIGURE 9 — THERMAL RESPONSE (ALL TYPES)



RESISTIVE SWITCHING

FIGURE 10 — SWITCHING TEST CIRCUIT

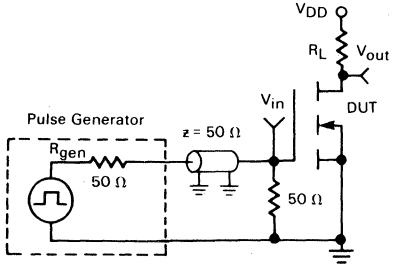
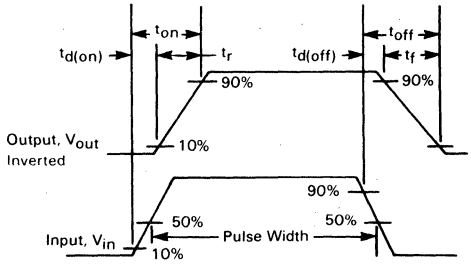


FIGURE 11 — SWITCHING WAVEFORMS



OPERATING AREA INFORMATION

FIGURE 12 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

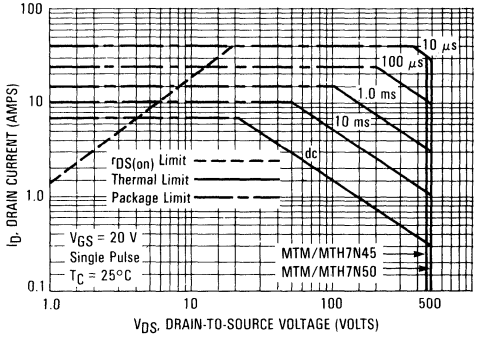


FIGURE 13 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

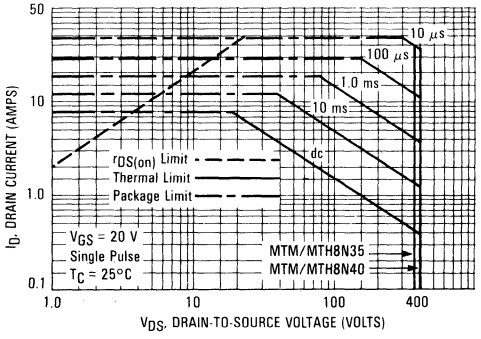
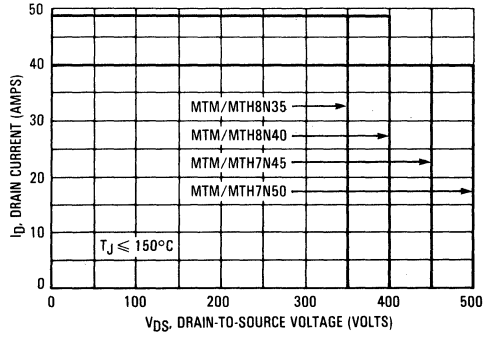


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figures 12 or 13
T_{Jmax} = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
$r(t)$ = normalized thermal response from Figure 9

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

MTM8N08, MTP8N08
MTM8N10, MTP8N10
MTM10N05, MTP10N05
MTM10N06, MTP10N06

MOTOROLA

C

Designer's Data Sheet

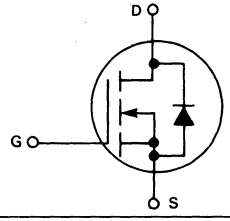
8.0 and 10 AMPERE
N-CHANNEL TMOS
POWER FET
$r_{DS(on)}$ = 0.5 OHM
80 and 100 VOLTS
$r_{DS(on)}$ = 0.28 OHM
50 and 60 VOLTS

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

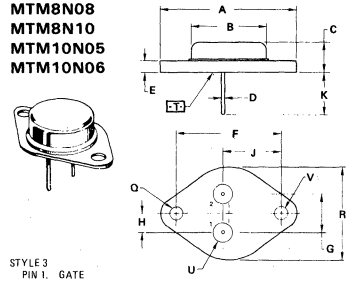
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



MTM8N08
MTM8N10
MTM10N05
MTM10N06

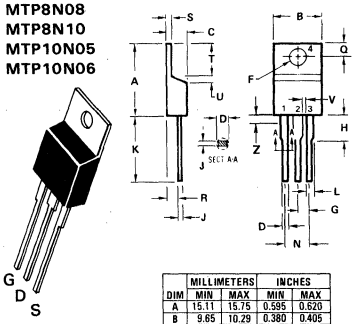


STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.82	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(TO-3 TYPE)

MTP8N08
MTP8N10
MTP10N05
MTP10N06



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 10N05	MTM or MTP 10N06	MTM or MTP 8N08	MTM or MTP 8N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 10 28		 8.0 20		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM10N05/MTP10N05	$V_{(BR)DSS}$	50	—	Vdc
	MTM10N06/MTP10N06		60	—	
	MTM8N08/MTP8N08		80	—	
	MTM8N10/MTP8N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)	MTM10N05/MTM10N06 MTP10N05/MTP10N06	$r_{DS(on)}$	—	0.28	Ohms
(V_{GS} = 10 Vdc, I_D = 4.0 Adc)	MTM8N08/MTM8N10 MTP8N08/MTP8N10		—	0.50	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 10 Adc)	MTM10N05/MTM10N06 MTP10N05/MTP10N06	$V_{DS(on)}$	—	3.4	Vdc
(I_D = 5.0 Adc, T_J = 100°C)	MTM8N08, MTM8N10 MTP8N08/MTP8N10		—	2.8	
(I_D = 8.0 Adc)	MTM10N05, MTM10N06 MTP10N05/MTP10N06		—	4.8	
(I_D = 4.0 Adc, T_J = 100°C)	MTM8N08/MTM8N10 MTP8N08/MTP8N10		—	4.0	
Forward Transconductance (V_{DS} = 15 V, I_D = 5.0 A)	MTM10N05/MTM10N06 MTP10N05/MTP10N06	g_{fs}	2.5	—	mhos
(V_{DS} = 15 V, I_D = 4.0 A)	MTM8N08/MTM8N10 MTP8N08/MTP8N10		1.5	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms See Figures 1 and 2)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	120	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	60	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0,	V_{SD}	1.9	Vdc
Forward Turn-On Time		t_{on}	200	ns
Reverse Recovery Time		t_{rr}	300	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 1 — SWITCHING TEST CIRCUIT

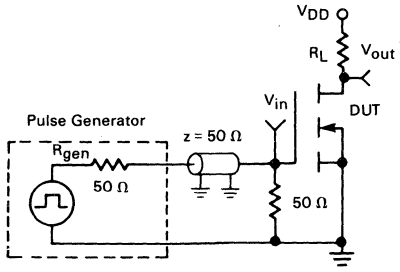
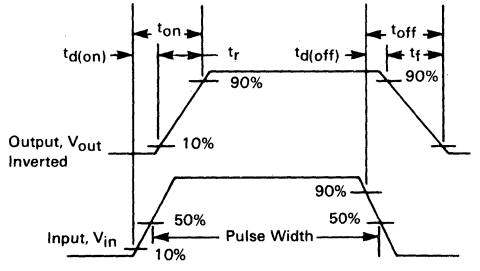


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTM8N08, MTM8N10
MTP8N08, MTP8N10

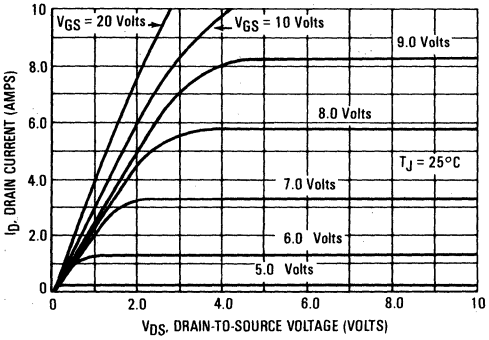
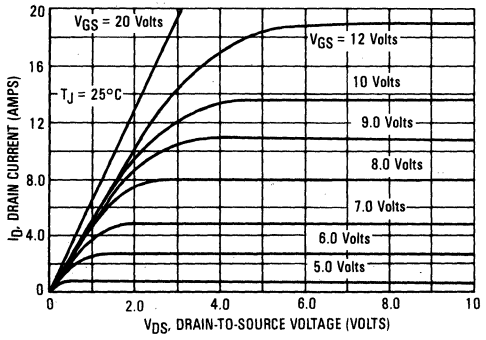


FIGURE 4 — MTM10N05, MTM10N06
MTP10N05, MTP10N06



TRANSFER CHARACTERISTICS

FIGURE 5 — MTM8N08, MTM8N10
MTP8N08, MTP8N10

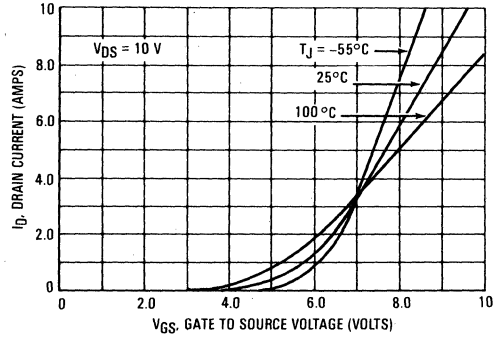
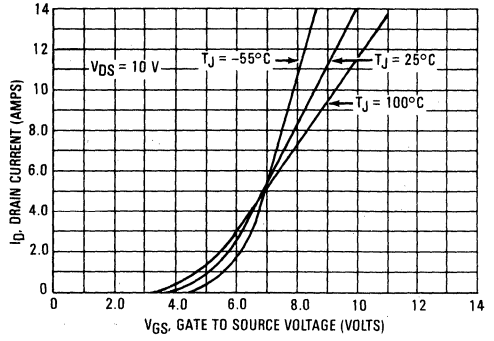


FIGURE 6 — MTM10N05, MTM10N06
MTP10N05, MTP10N06



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTM8N08, MTM8N10
MTP8N08, MTP8N10

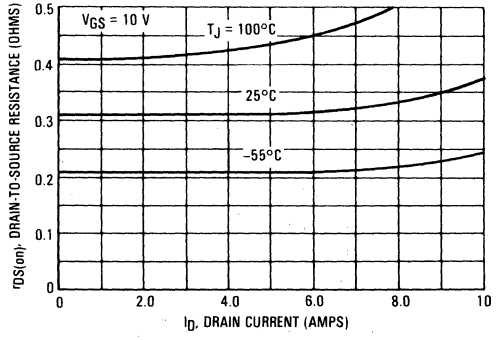
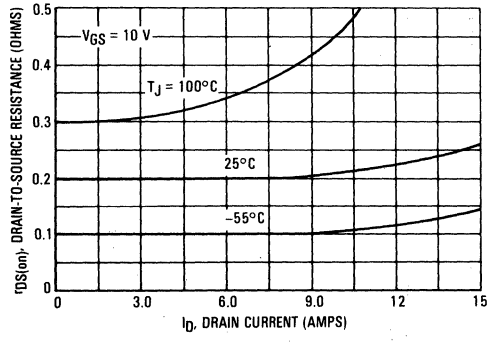


FIGURE 8 — MTM10N05, MTM10N06
MTP10N05, MTP10N06



TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

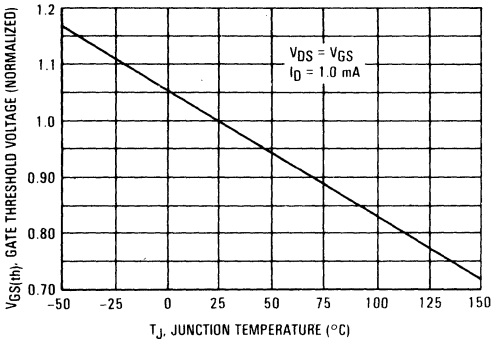
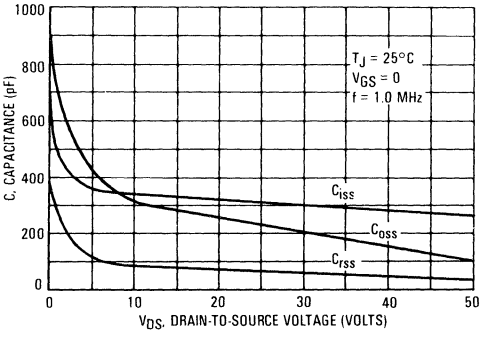


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM8N08, MTM8N10, MTM10N05, MTM10N06

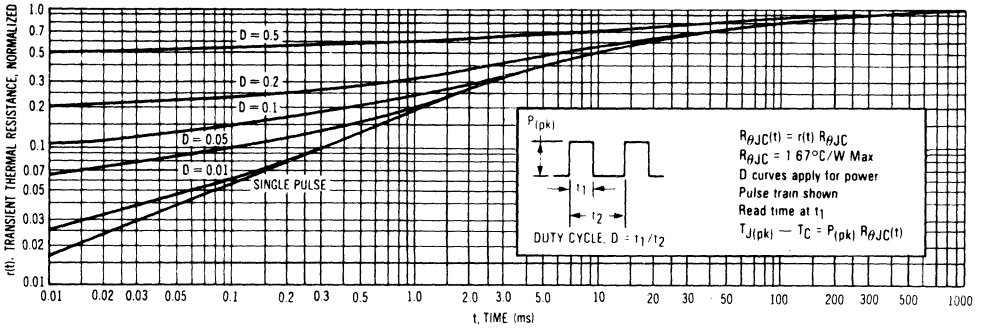
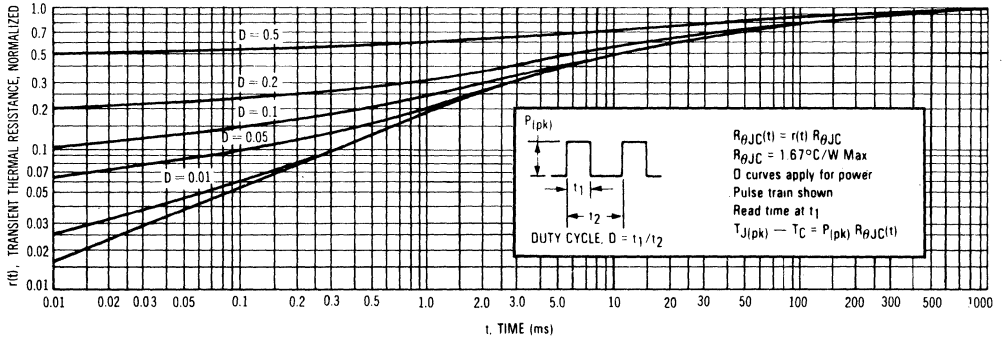


FIGURE 12 — MTM8N08, MTM8N10, MTM10N05, MTM10N06



C

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 13 — MTM8N08, MTM8N10
MTP8N08, MTM8N10

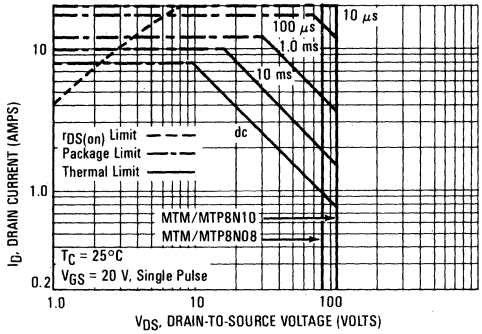
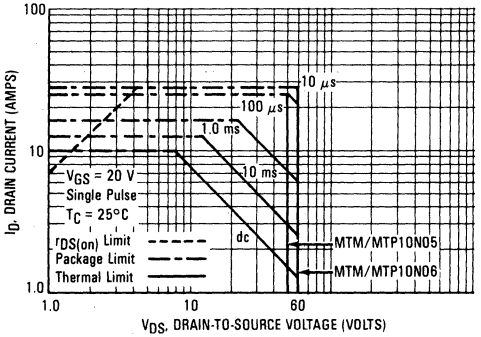


FIGURE 14 — MTM10N05, MTM10N06
MTP10N05, MTM10N06



FORWARD BIASED SAFE OPERATING AREA

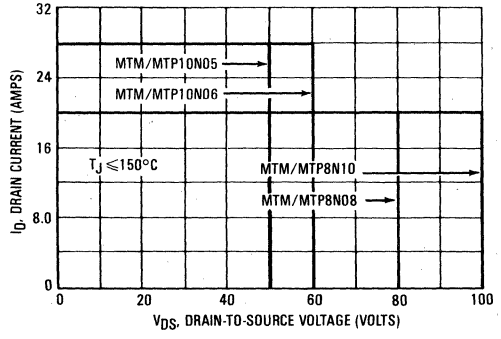
The dc data of Figures 13 and 14 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 13 and 14.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figures 11 or 12.

FIGURE 15 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 15 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 15 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MOTOROLA

MTM8N18, MTM8N20
MTP8N18, MTP8N20

C

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

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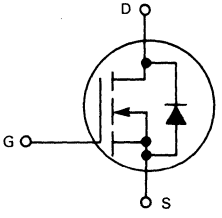
- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

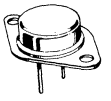


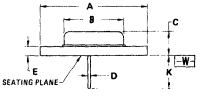
8.0 AMPERE

N-CHANNEL TMOS POWER FET

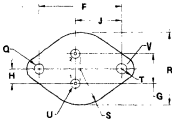
$r_{DS(on)}$ = 0.4 OHM
180 and 200 VOLTS

MTM8N18
MTM8N20





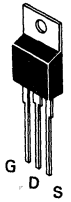
STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

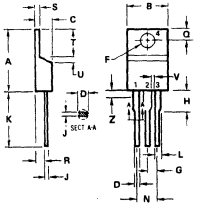


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	8.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA
(TO-3 TYPE)

MTP8N18
MTP8N20





STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM8N18 MTP8N18	MTM8N20 MTP8N20	Unit
Drain-Source Voltage	V_{DSS}	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 8.0 25		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM8N18/MTP8N18 MTMN818/MTP8N20	$V_{(BR)DSS}$	 180 200	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 BV_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})	T_J = 100°C	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 4.0 Adc) (I_D = 8.0 Adc) (I_D = 4.0 Adc, T_J = 100°C)		$V_{DS(on)}$	 — — —	 1.6 4.0 3.2	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)		$r_{DS(on)}$	—	0.4	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 4.0 A)		g_{fs}	3.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 12		
Switching Safe Operating Area		SSOA	See Figure 13		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 4.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	100	ns
Fall Time		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 8.0 A V_{GS} = 0	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	250	ns
Reverse Recovery Time		t_{rr}	325	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

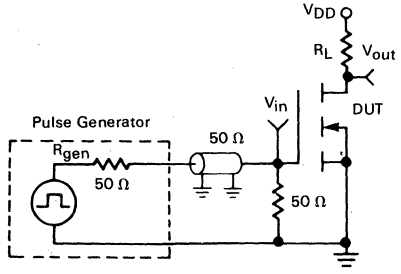
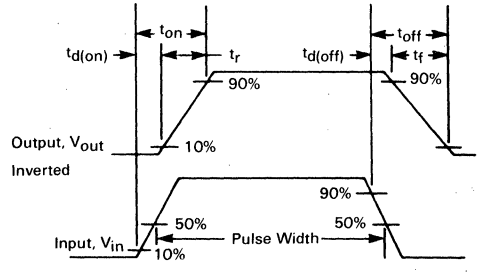


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

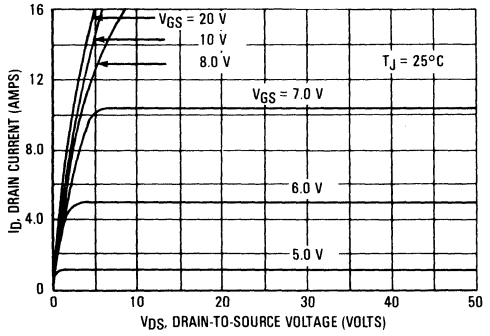


FIGURE 4 — ON-REGION CHARACTERISTICS

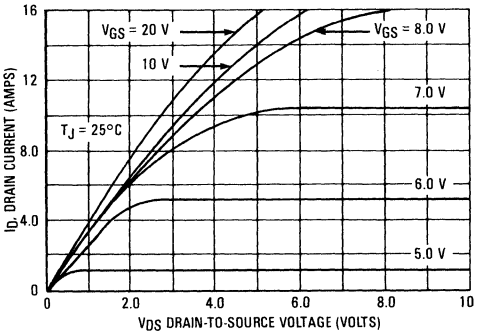


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

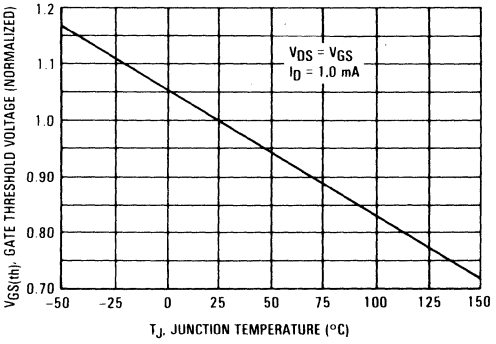


FIGURE 6 — TRANSFER CHARACTERISTICS

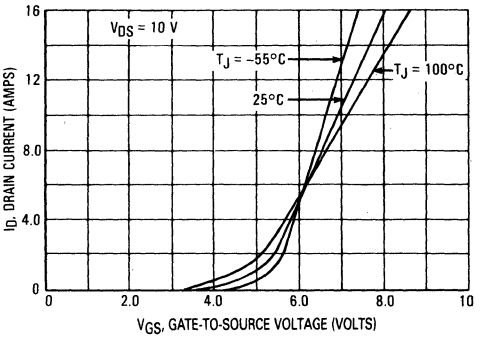


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

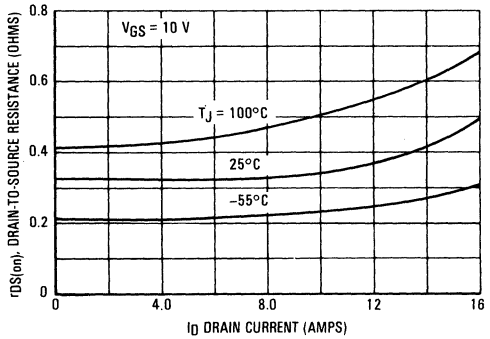
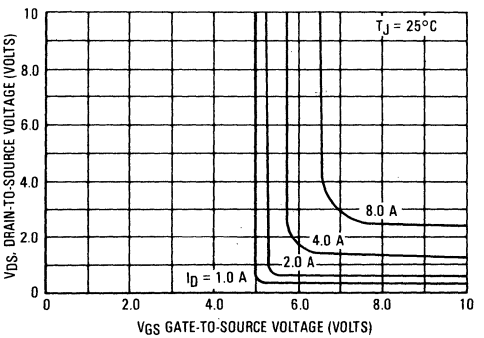


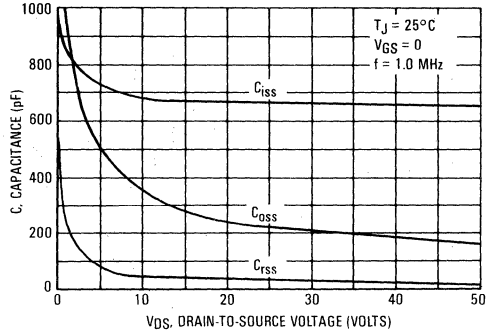
FIGURE 8 — ON-VOLTAGE VARIATION



C

TYPICAL CHARACTERISTICS

FIGURE 9 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 10 — MTM8N18/MTM8N20

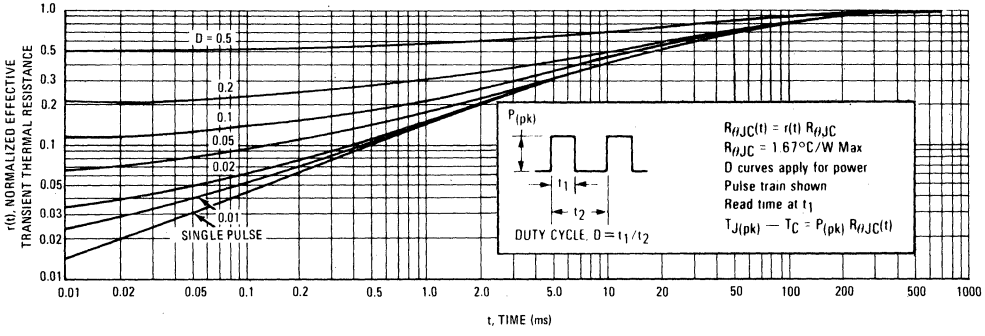
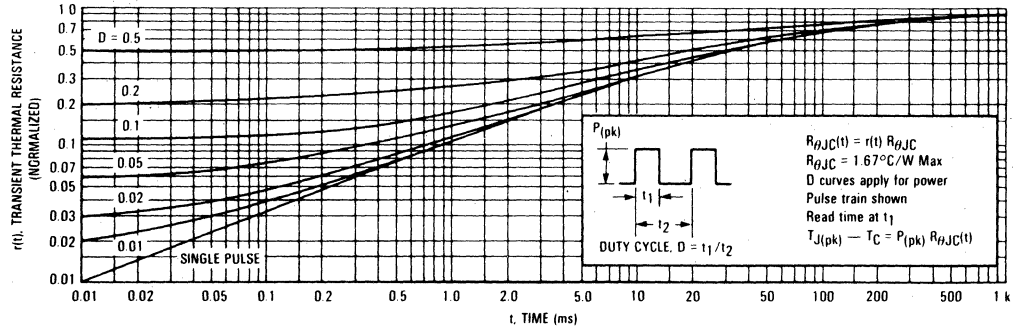


FIGURE 11 — MTP8N18/MTP8N20



SAFE OPERATING AREA INFORMATION

FIGURE 12 — MAXIMUM FORWARD BIASED SAFE OPERATING AREA

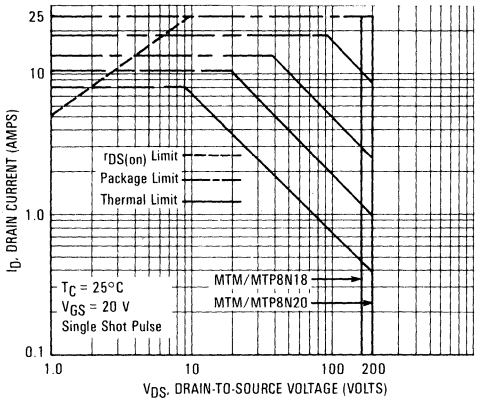
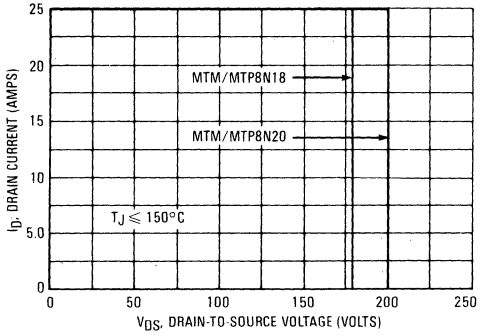


FIGURE 13 — MAXIMUM SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 12 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 12.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
$r(t)$ = normalized thermal response from Figures 10 or 11.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 13 is the boundary that the load line may traverse without incurring damage to the MOSFET. The Fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 13 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 2.0 A. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

MTM8P08, MTM8P10
MTP8P08, MTP8P10

(Formerly MTM/MTP 814, 815)

MOTOROLA

C

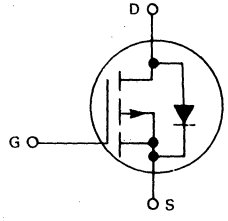
Designer's Data Sheet

P-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

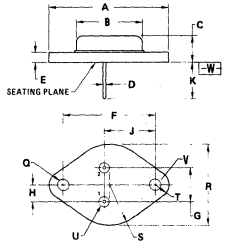


8.0 AMPERE

P-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.4 OHMS
80 and 100 VOLTS

MTM8P08
MTM8P10

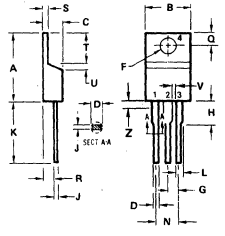


STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA
(TO-3 TYPE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

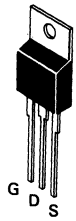
MTP8P08
MTP8P10



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	
Z	–	2.03	–	0.080



MAXIMUM RATINGS

Rating	Symbol	MTM8P08 MTP8P08	MTM8P10 MTP8P10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage e	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 8.0 25		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM8P08/MTP8P08 MTM8P10/MTP8P10	$V_{(BR)DSS}$	80 100	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 4.0 Adc) (I_D = 8.0 Adc) (I_D = 4.0 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	1.6 4.8 3.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)		$r_{DS(on)}$	—	0.4	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 4.0 A)		g_{fs}	2.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 13		
Switching Safe Operating Area		SSOA	See Figure 14		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	600	pF
Reverse Transfer Capacitance		C_{rss}	—	180	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 4.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	80	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	150	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 8.0 A V_{GS} = 0	V_{SD}	1.3	Vdc
Forward Turn-On Time		t_{on}	250	ns
Reverse Recovery Time		t_{rr}	325	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

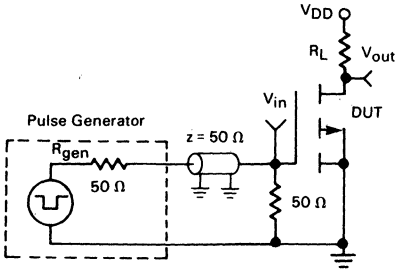
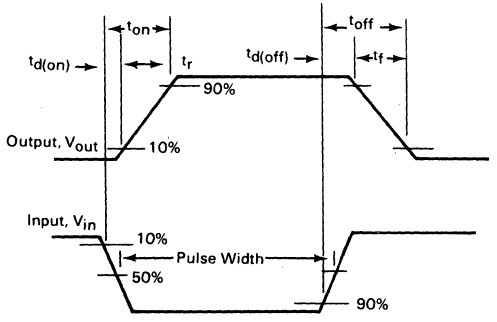


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 OUTPUT CHARACTERISTICS

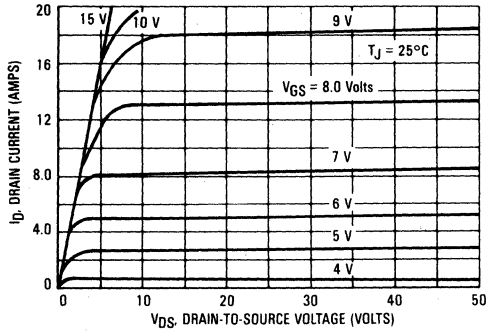


FIGURE 4 — ON-REGION CHARACTERISTICS

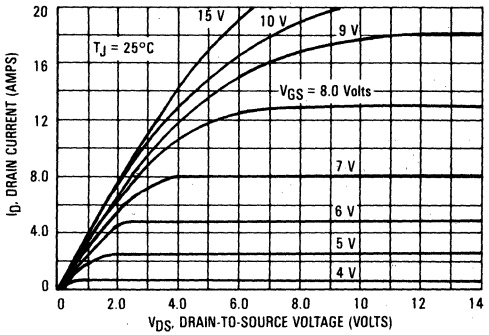


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

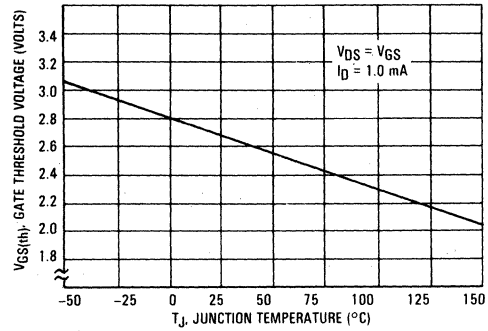


FIGURE 6 — TRANSFER CHARACTERISTICS

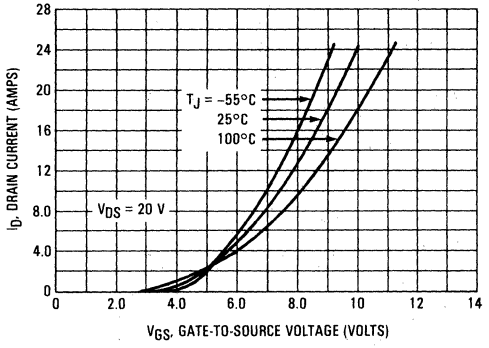


FIGURE 7 — ON-VOLTAGE versus TEMPERATURE

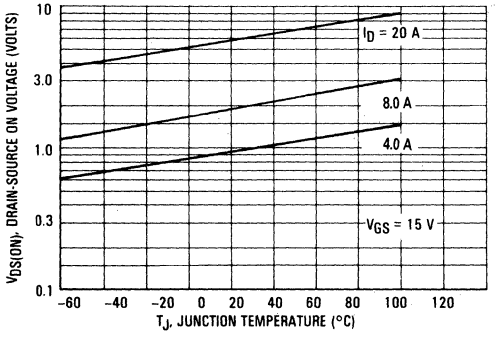
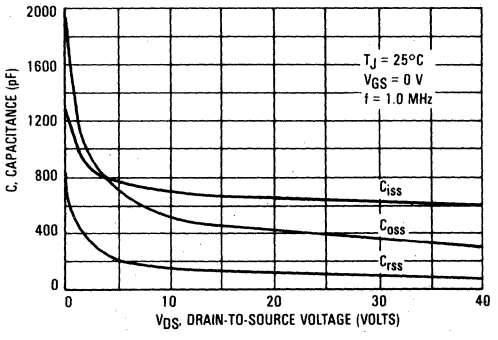


FIGURE 8 — CAPACITANCE VARIATION



TYPICAL CHARACTERISTICS

FIGURE 9 — ON-RESISTANCE versus DRAIN CURRENT

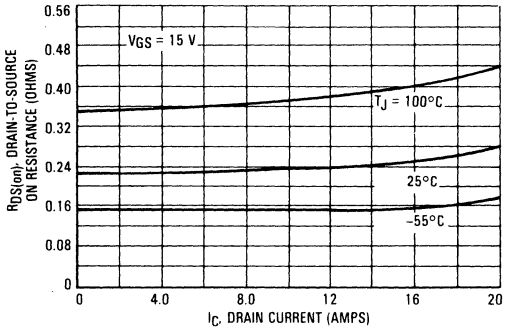
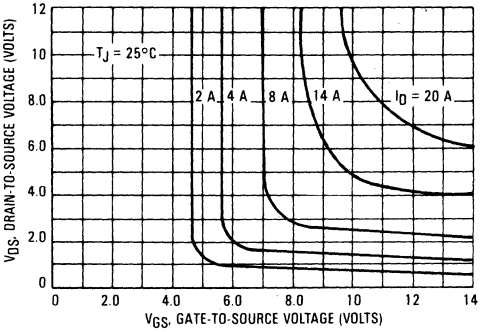


FIGURE 10 — ON-VOLTAGE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM8P08/MTM8P10

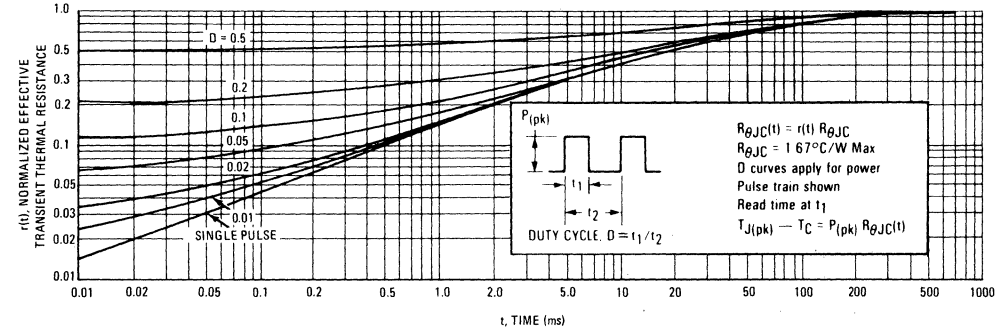
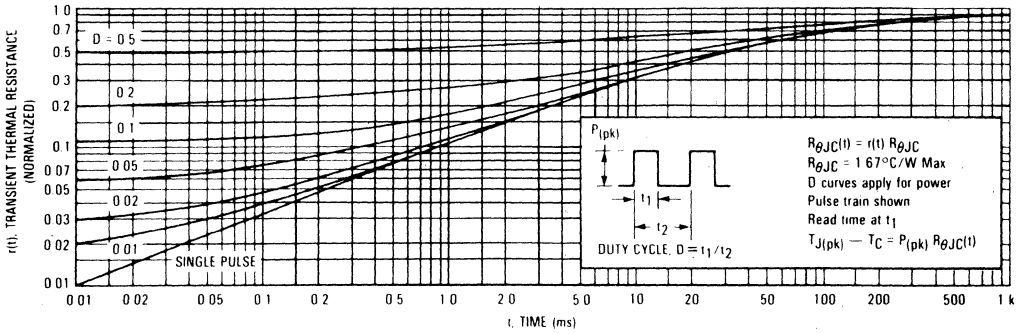


FIGURE 12 — MTP8P08/MTP8P10



C

SAFE OPERATING AREA INFORMATION

FIGURE 13 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

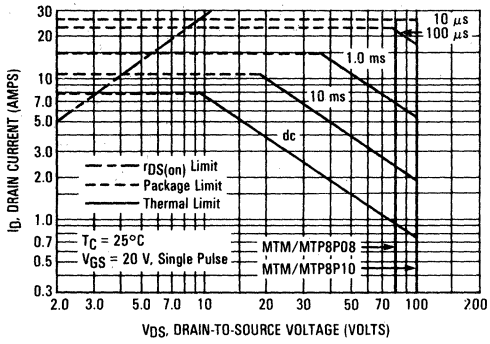
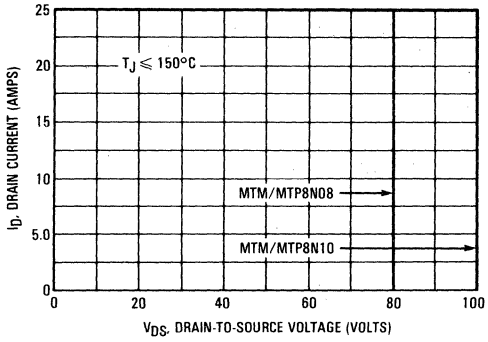


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_D(25°C)\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_D(25°C)$ = the dc drain current at T_C = 25°C from Figure 13
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figures 11 and 12

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 15 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

MOTOROLA

MTM10N08
MTM10N10
MTP10N08
MTP10N10

Designer's Data Sheet

10 AMPERE

N-CHANNEL TMOS POWER FET

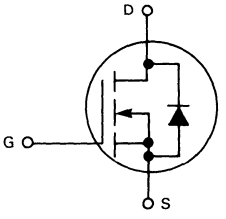
$r_{DS(on)}$ = 0.33 OHM
80 and 100 VOLTS

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



MAXIMUM RATINGS

Rating	Symbol	MTM10N08 MTP10N08	MTM10N10 MTP10N10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 10 25		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

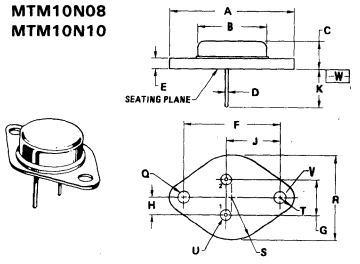
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

MTM10N08
MTM10N10



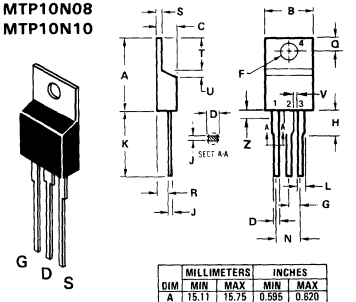
NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA
(TO-3 TYPE)

MTP10N08
MTP10N10



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM10N08/MTP10N08 MTM10N10/MTP10N10	$V_{(BR)DSS}$	80 100	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5.0 Adc) (I_D = 10 Adc) (I_D = 5.0 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	1.65 4.0 3.3	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)		$r_{DS(on)}$	—	0.33	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 5.0 A)		g_{fs}	2.5	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	600	pF
Output Capacitance		C_{oss}	—	400	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 5.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	100	ns
Fall Time		t_f	—	50	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 10 A V_{GS} = 0	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	80	ns
Reverse Recovery Time		t_{rr}	700	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

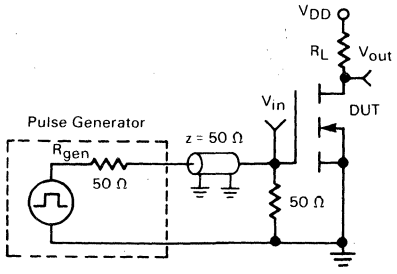
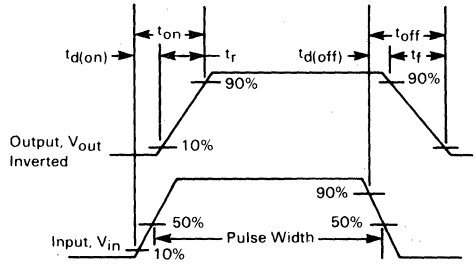


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

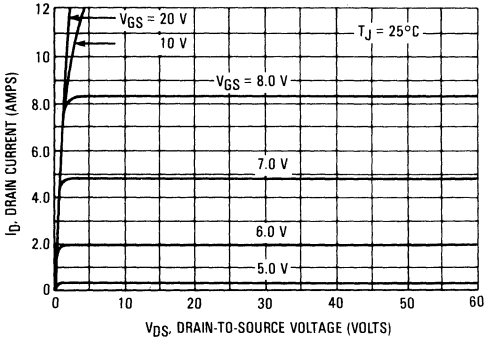


FIGURE 4 — ON-REGION CHARACTERISTICS

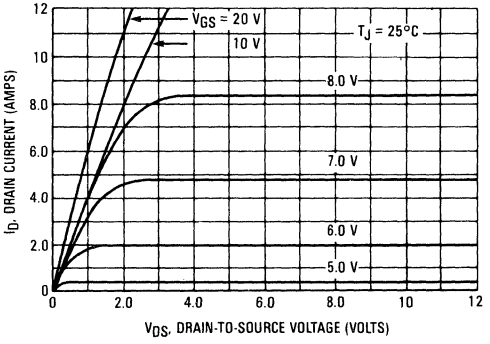


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

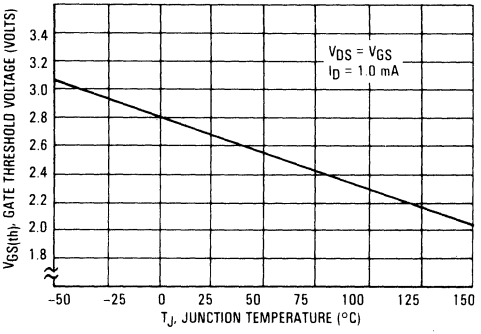


FIGURE 6 — TRANSFER CHARACTERISTICS

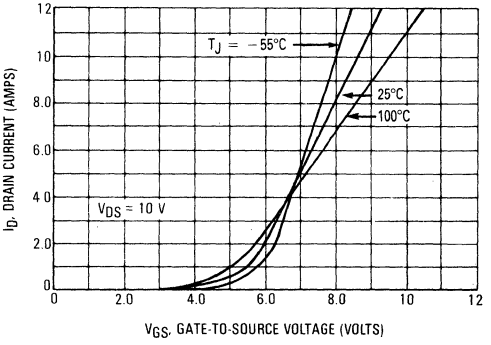


FIGURE 7 — $r_{DS(on)}$, ON-RESISTANCE versus DRAIN CURRENT

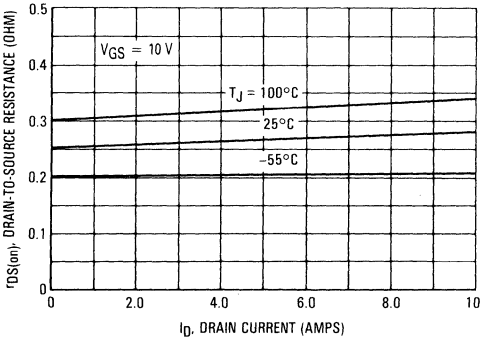
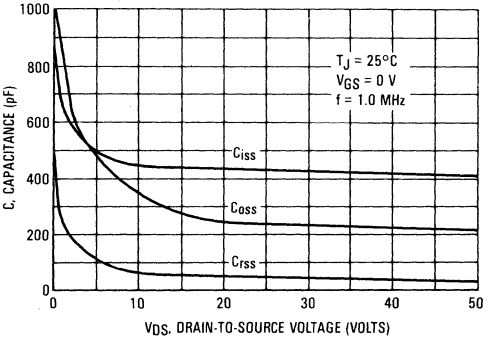


FIGURE 8 — CAPACITANCE VARIATION



C

C

SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

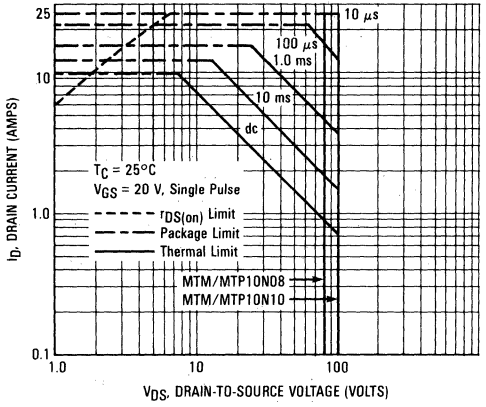
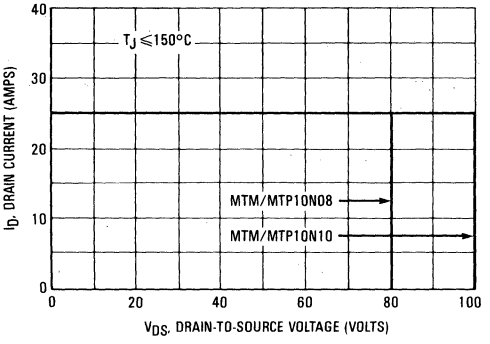


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figures 11 or 12.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10 is the boundary that the load line may traverse without incurring damage to the MOSFET. The Fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

THERMAL RESPONSE

FIGURE 11 — MTM10N08/10N10

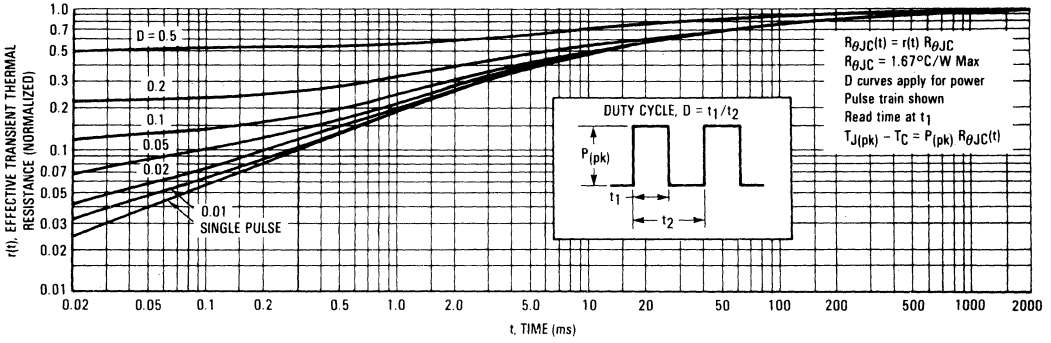
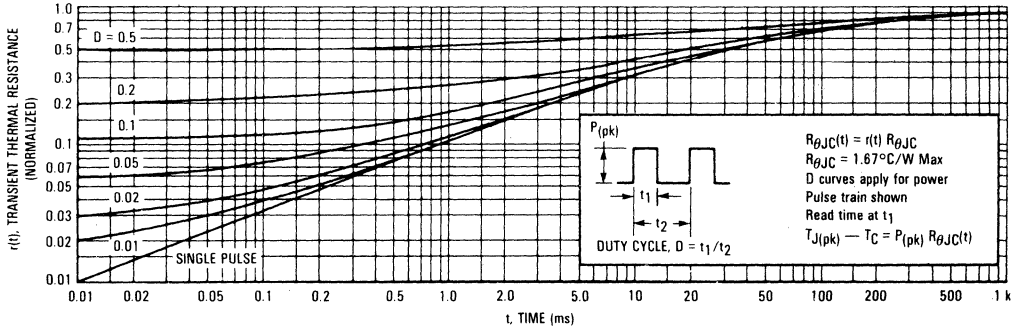


FIGURE 12 — MTP10N08/10N10



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 1.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

MTM10N12, MTP10N12
MTM10N15, MTP10N15

(Formerly MTM/MTP1034, 1035)

MOTOROLA

C

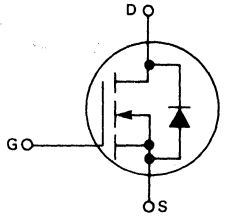
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

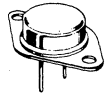


10 AMPERE

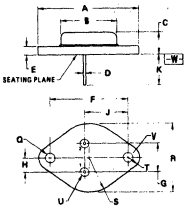
N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.3 OHM
120 and 150 VOLTS

MTM10N12
MTM10N15



STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN



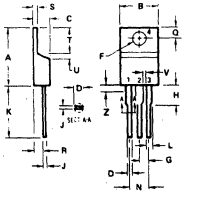
NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.
2. 001-02 OBSOLETE, NEW STANDARD 011-01.
3. 001-01 OBSOLETE, NEW STANDARD 001-03.
4. DIAMETER V AND SURFACE W ARE DATUMS.
5. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ ∅ 0.25 (0.010) Ⓜ W V Ⓜ
6. POSITIONAL TOLERANCE FOR LEADS:
⌖ ∅ 0.30 (0.012) Ⓜ W V Ⓜ Q Ⓜ

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	38.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	39.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.16	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA
(TO-3 TYPE)

MTP10N12
MTP10N15

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3 ONLY.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.85	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
R	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.78	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM10N12 MTP10N12	MTM10N15 MTP10N15	Unit
Drain-Source Voltage	V_{DSS}	120	150	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 10 28		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA) MTM10N12/MTP10N12	$V_{(BR)DSS}$	120	—	Vdc
MTM10N15/MTP10N15		150	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	0.25	mAdc
T_J = 100°C		—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})	V_{GS}	2.0	4.5	Vdc
T_J = 100°C		1.5	4.0	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5.0 Adc)	$V_{DS(on)}$	—	1.5	Vdc
(I_D = 10 Adc)		—	3.0	
(I_D = 5.0 Adc, T_J = 100°C)		—	2.5	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)	$r_{DS(on)}$	—	0.3	Ohms
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	2.5	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz	C_{iss}	—	1200	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz	C_{oss}	—	500	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz	C_{rss}	—	120	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time (V_{DS} = 25 V, I_D = 5.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time (V_{DS} = 25 V, I_D = 5.0 A, R_{gen} = 50 ohms)	t_r	—	180	ns
Turn-Off Delay Time (V_{DS} = 25 V, I_D = 5.0 A, R_{gen} = 50 ohms)	$t_{d(off)}$	—	200	ns
Fall Time (V_{DS} = 25V, I_D = 5.0 A, R_{gen} = 50 ohms)	t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 10 A	V_{SD}	1.3	Vdc
Forward Turn-On Time	V_{GS} = 0, di/dt = 25 A/μs	t_{on}	250	ns
Reverse Recovery Time		t_{rr}	325	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

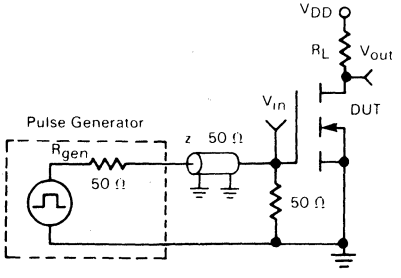
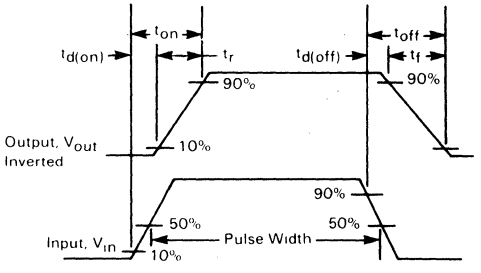


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

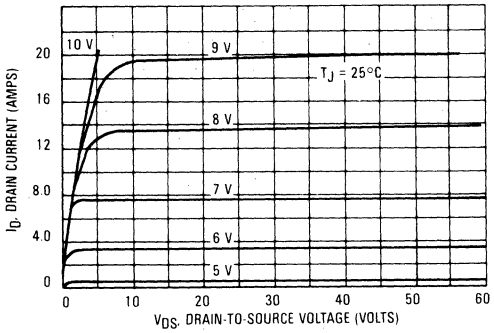


FIGURE 4 — ON-REGION CHARACTERISTICS

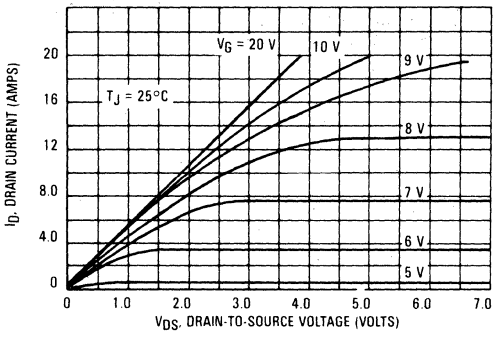


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

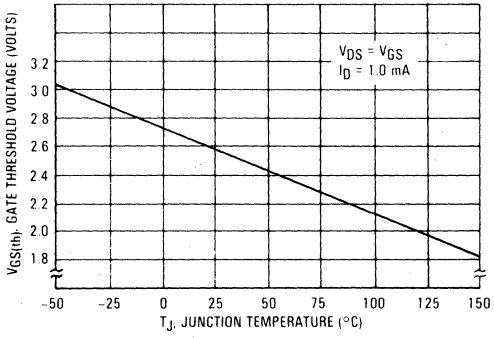


FIGURE 6 — TRANSFER CHARACTERISTICS

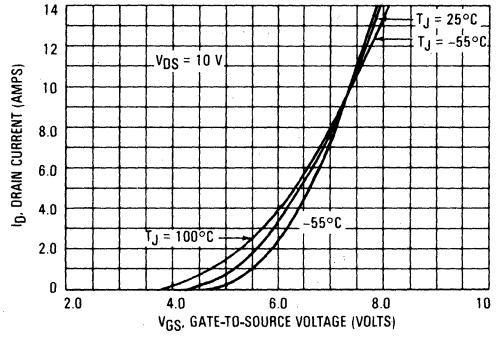


FIGURE 7 — ON-VOLTAGE VARIATION versus TEMPERATURE

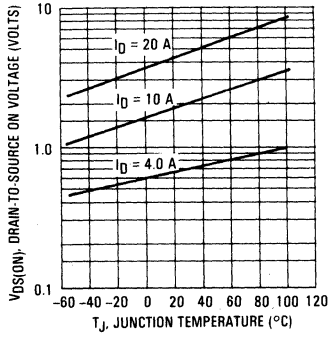
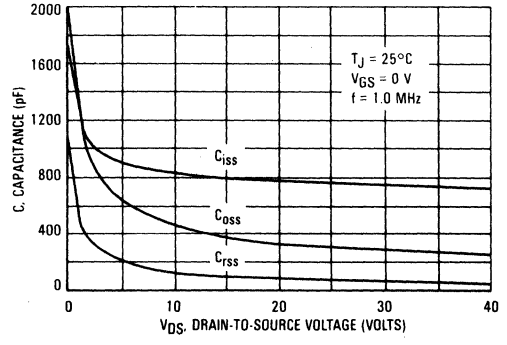


FIGURE 8 — CAPACITANCE VARIATION



TYPICAL CHARACTERISTICS

FIGURE 9 — ON-RESISTANCE versus DRAIN CURRENT

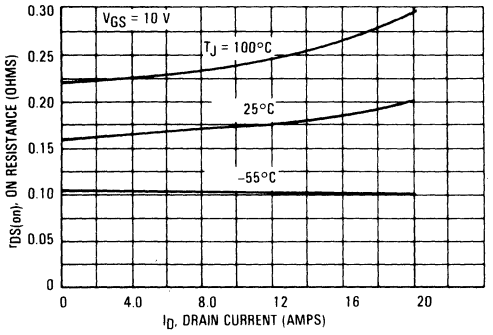
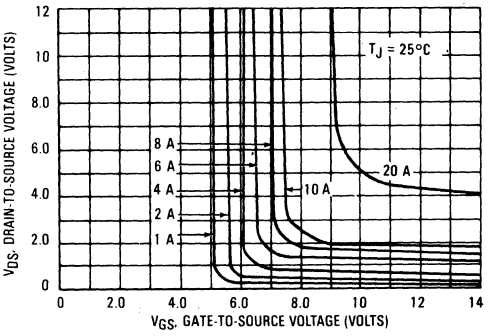


FIGURE 10 — ON-VOLTAGE VARIATION



C

THERMAL RESPONSE

FIGURE 11 — MTM10N12/MTM10N15

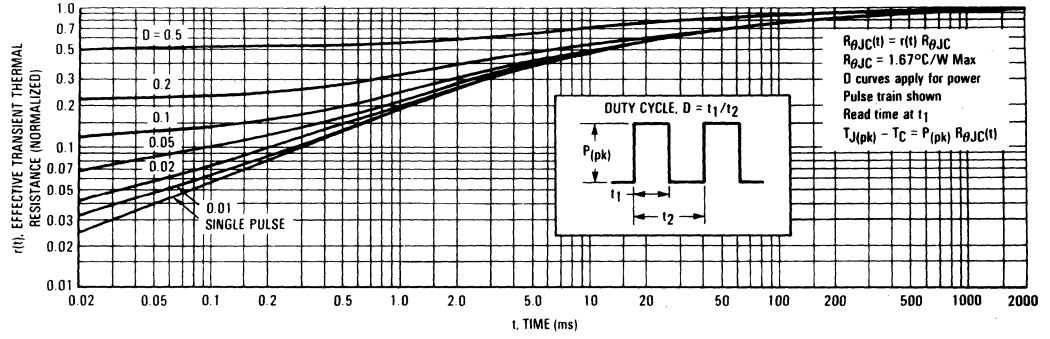
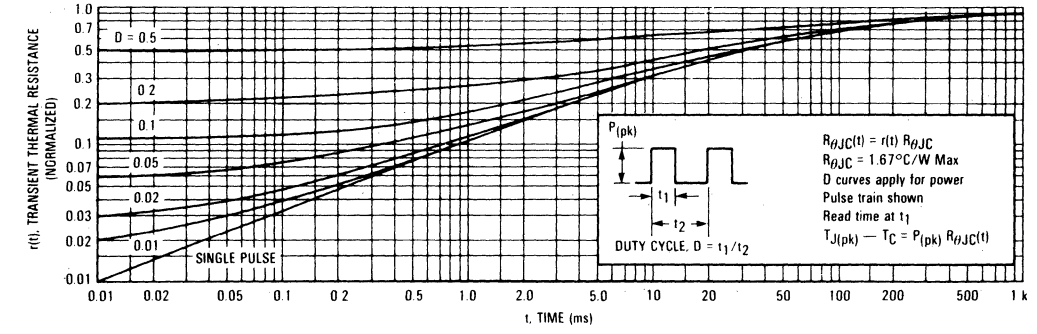


FIGURE 12 — MTP10N12/MTP10N15



SAFE OPERATING AREA INFORMATION

FIGURE 13 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

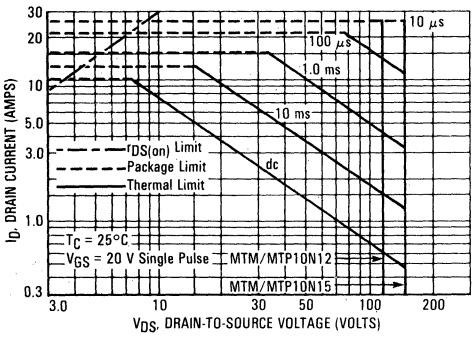
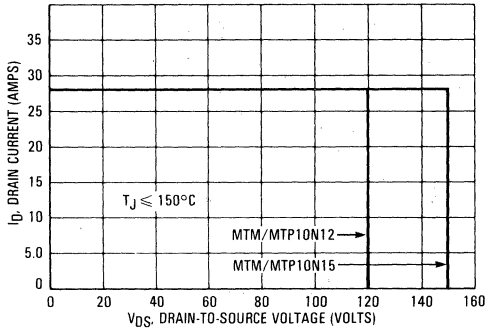


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 13.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figures 11 or 12.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14 is the boundary that the load line may traverse without incurring damage to the MOSFET. The Fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

MOTOROLA

MTM10N25
MTP10N25

Designer's Data Sheet

10 AMPERE

N-CHANNEL TMOS POWER FET

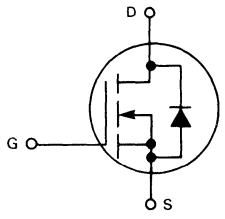
$r_{DS(on)}$ = 0.45 OHM
250 VOLTS

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

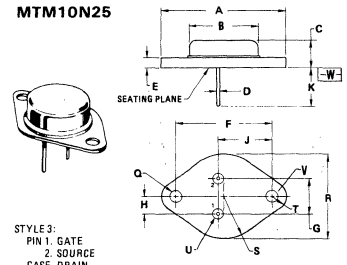
These TMOS Power FETs are designed for 120 V line operated high speed power switching applications such as motor controls, switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



MTM10N25



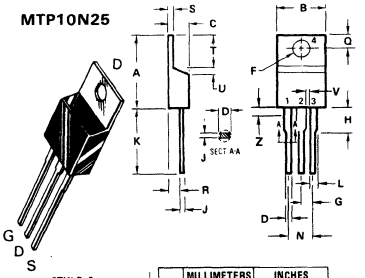
STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA
(TO-3 TYPE)

MTP10N25



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM10N25 MTP10N25	Unit
Drain-Source Voltage	V_{DSS}	250	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	250	Vdc
Gate – Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 10 30	Adc
Gate Current — Pulsed	I_{GM}	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 100 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM10N25/MTP10N25	$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_J = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 5.0 Adc)			—	2.25	
(I_D = 10 Adc)			—	5.60	
(I_D = 5.0 Adc, T_J = 100°C)			—	4.50	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)		$r_{DS(on)}$	—	0.45	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 5.0 A)		g_{fs}	3.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	600	pF
Reverse Transfer Capacitance		C_{rss}	—	150	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 5.0 A, R_{gen} = 50 ohms) See Figures 1 and 2.	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	250	ns
Turn-Off Delay Time		$t_{d(off)}$	—	100	ns
Fall Time		t_f	—	120	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 10 A, V_{GS} = 0	V_{SD}	1.5	Vdc
Forward Turn-On Time		t_{on}	50	ns
Reverse Recovery Time		t_{rr}	300	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

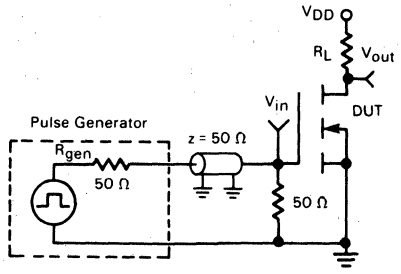
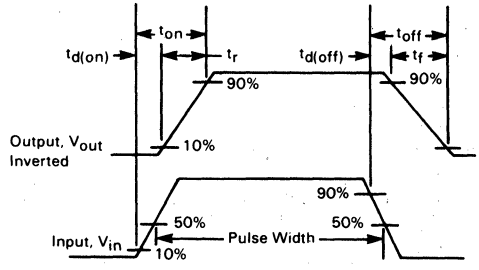


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

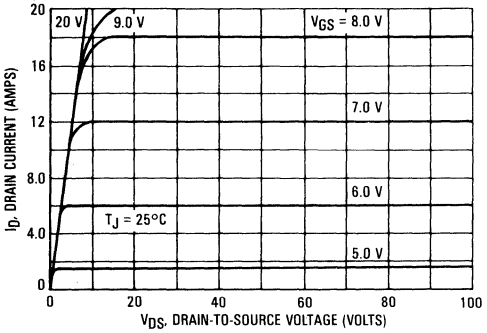


FIGURE 4 — ON-REGION CHARACTERISTICS

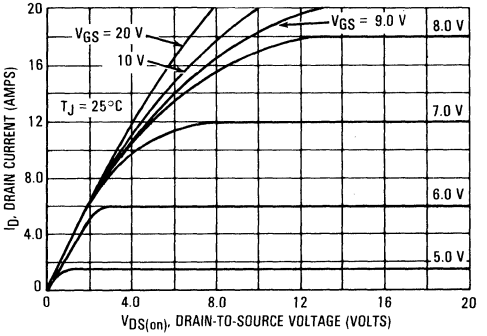


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

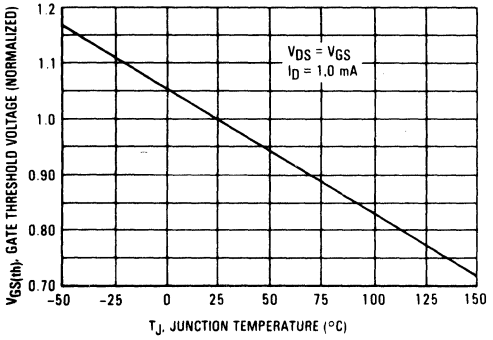


FIGURE 6 — TRANSFER CHARACTERISTICS

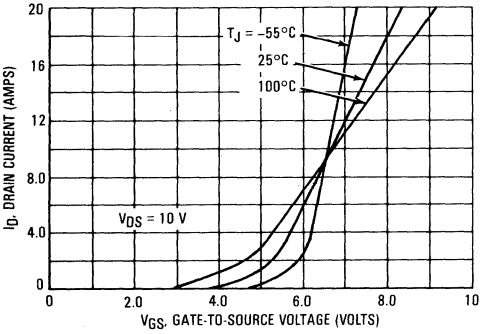


FIGURE 7 — ON RESISTANCE versus DRAIN CURRENT

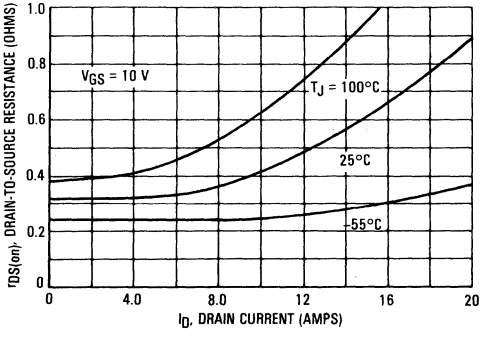
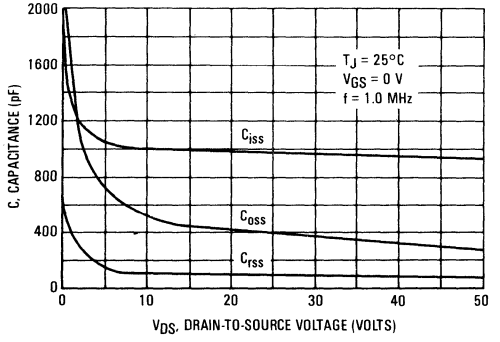


FIGURE 8 — CAPACITANCE VARIATION



C

SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

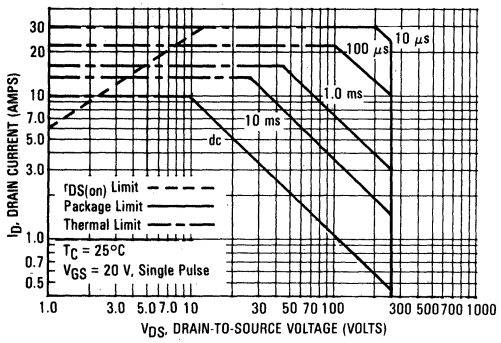
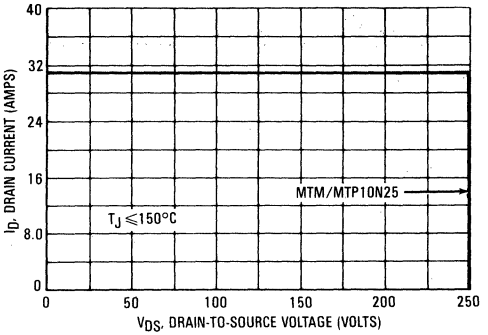


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figures 11 and 12

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

THERMAL RESPONSE

FIGURE 11 — MTM10N25

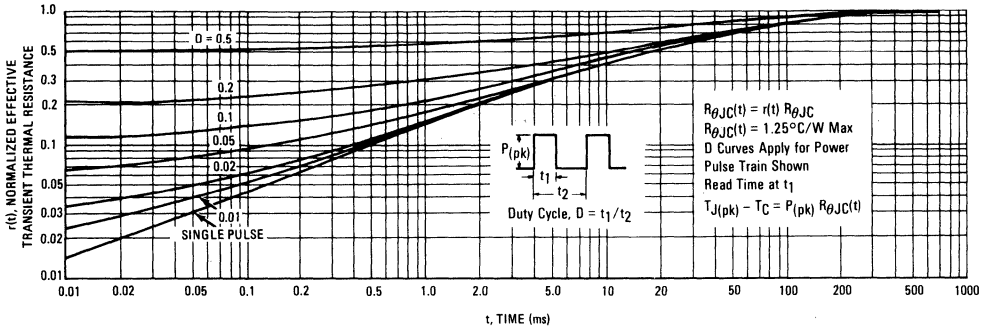
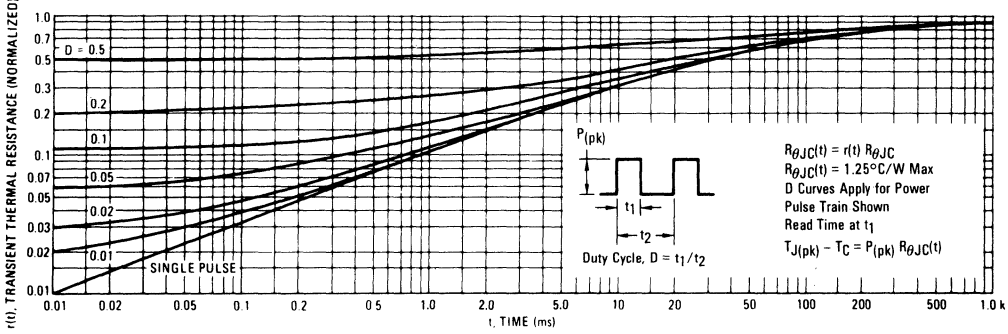


FIGURE 12 — MTP10N25



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 2.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

MTM12N05, MTM12N06
MTP12N05, MTP12N06

MOTOROLA

C

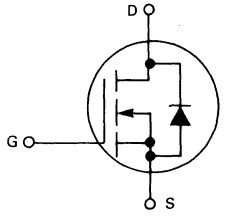
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

TMOS™

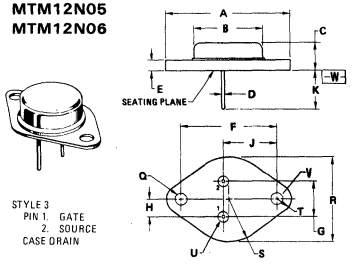


12 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.2 OHM
50 and 60 VOLTS

MTM12N05
MTM12N06

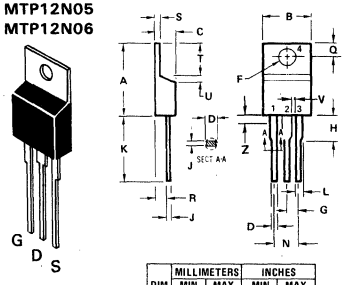


STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA
(TO-3 TYPE)

MTP12N05
MTP12N06



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM12N05 MTP12N05	MTM12N06 MTP12N06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 12 30		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM12N05/MTP12N05 MTM12N06/MTP12N06	$V_{(BR)DSS}$	50 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = 0) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6.0 Adc) (I_D = 12 Adc) (I_D = 6.0 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	1.2 3.2 2.4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$r_{DS(on)}$	—	0.2	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 6.0 A)		g_{fs}	3.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	800	pF
Output Capacitance		C_{oss}	—	700	pF
Reverse Transfer Capacitance		C_{rss}	—	160	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 6.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	160	ns
Turn-Off Delay Time		$t_{d(off)}$	—	80	ns
Fall Time		t_f	—	110	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 12 A V_{GS} = 0	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	80	ns
Reverse Recovery Time		t_{rr}	700	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

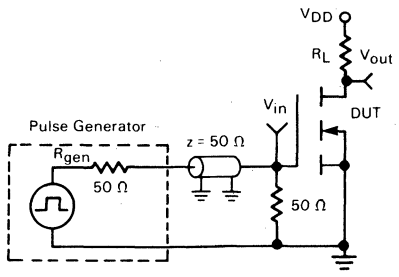
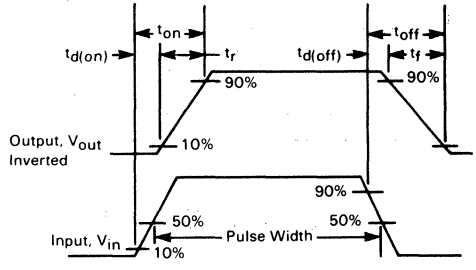


FIGURE 2 — SWITCHING WAVEFORMS



C

FIGURE 3 — OUTPUT CHARACTERISTICS

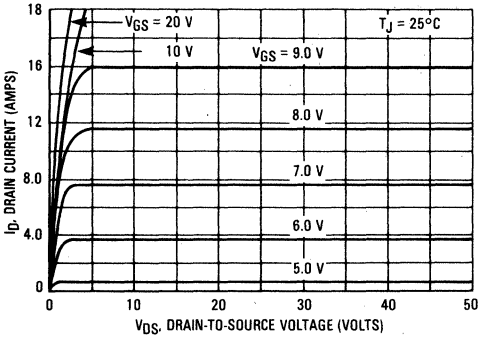


FIGURE 4 — ON-REGION CHARACTERISTICS

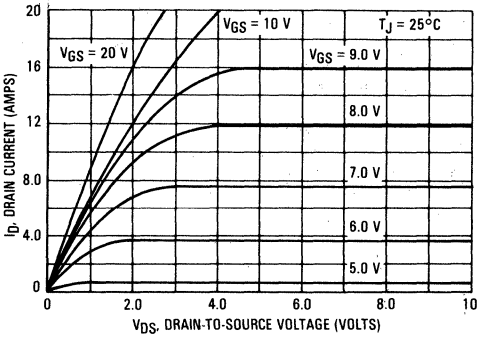


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

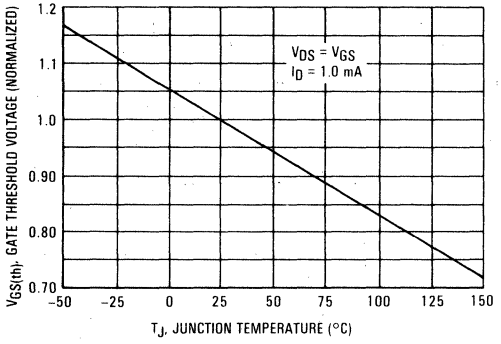


FIGURE 6 — TRANSFER CHARACTERISTICS

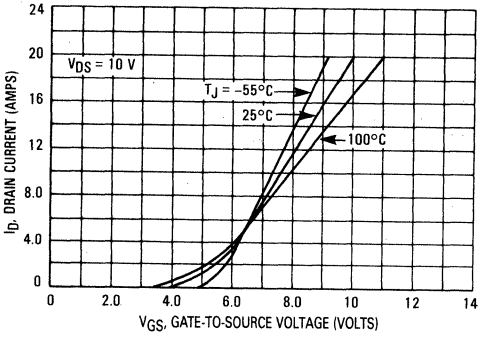


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

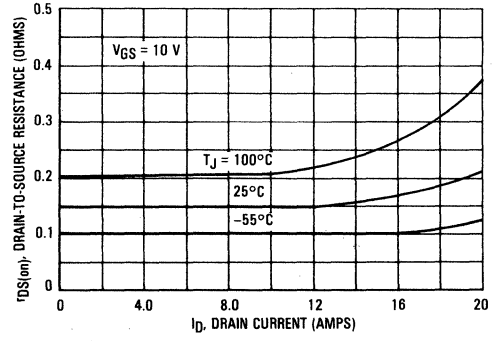
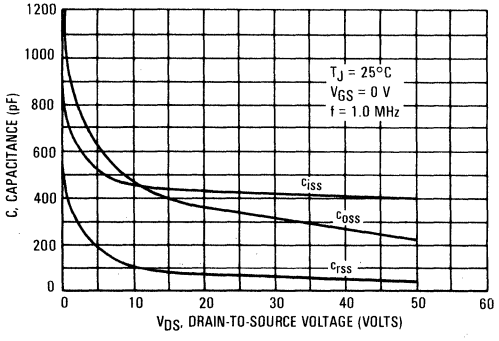


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SWITCHING SAFE OPERATING AREA

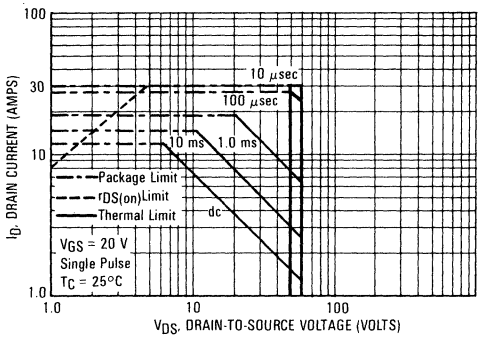
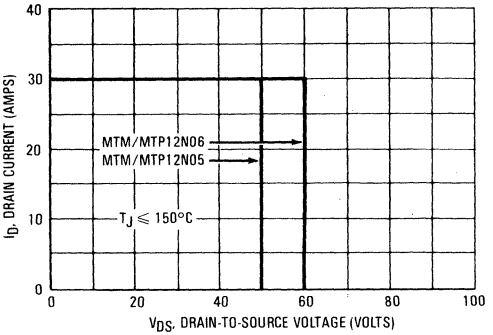


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figures 11 or 12.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

C

THERMAL RESPONSE

FIGURE 11 — MTM12N05/MTM12N06

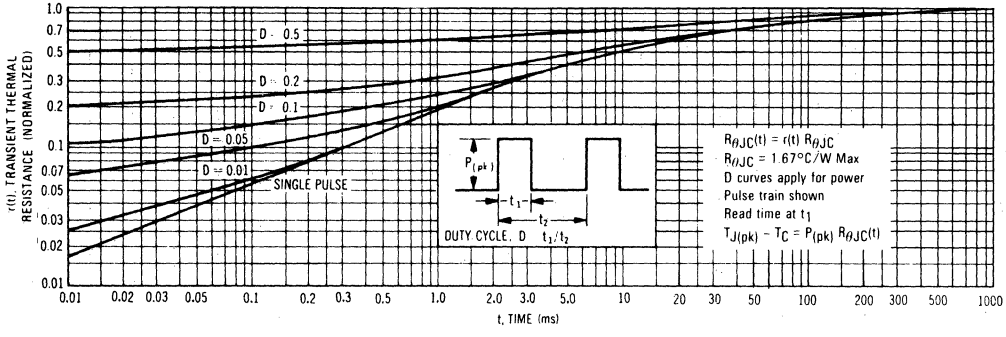
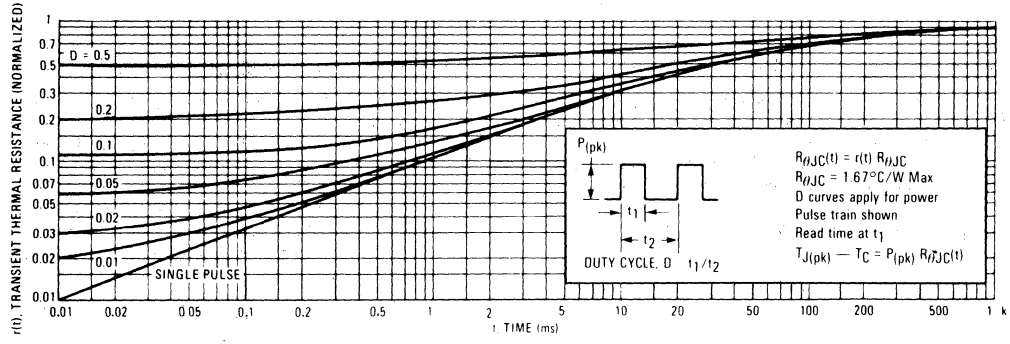


FIGURE 12 — MTP12N05/MTP12N06



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 3.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

MOTOROLA

MTM12N08 MTP12N08
MTM12N10 MTP12N10
MTM15N05 MTP15N05
MTM15N06 MTP15N06

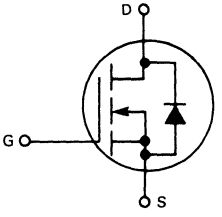
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

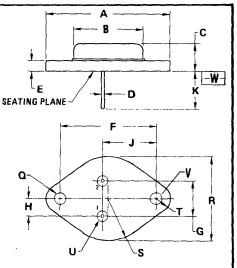


12 and 15 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.18 OHM
80 and 100 VOLTS
$r_{DS(on)}$ = 0.16 OHM
50 and 60 VOLTS

MTM15N05
MTM15N06
MTM12N08
MTM12N10



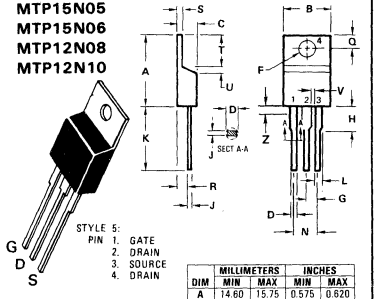
NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ ⌀ 0.25 (0.010) Ⓜ W V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ ⌀ 0.30 (0.012) Ⓜ W V Ⓜ Q Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

CASE 1-04
TO-204AA
(Formerly TO-3)

MTP15N05
MTP15N06
MTP12N08
MTP12N10



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 15N05	15N06	12N08	12N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous	I_D	15		12		Adc
Drain Current Pulsed	I_{DM}	40		30		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C	P_D	75				Watts
Derate above 25°C		0.6				W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM15N05/MTP15N05	$V_{(BR)DSS}$	50	—	Vdc
	MTM15N06/MTP15N06		60	—	
	MTM12N08/MTP12N08		80		
	MTM12N10/MTP12N10		100		
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_C = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)	MTM15N05/MTP15N05	$r_{DS(on)}$	—	0.16	Vdc
	MTM15N06/MTP15N06				
(V_{GS} = 10 Vdc, I_D = 6.0 Adc)	MTM12N08/MTP12N08		—	0.18	
	MTM12N10/MTP12N10				
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 15 Adc)	MTM15N05/MTP15N05		—	2.9	
	MTM15N06/MTP15N06				
(I_D = 7.5 Adc, T_J = 100°C)	MTM15N05/MTP15N05		—	2.4	
	MTM15N06/MTP15N06				
(I_D = 12 Adc)	MTM12N08/MTP12N08		—	2.6	
	MTM12N10/MTP12N10				
(I_D = 6.0 Adc, T_C = 100°C)	MTM12N08/MTP12N08		—	2.16	
	MTM12N10/MTP12N10				
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)	MTM15N05/MTP15N05	g_{fs}	3.5	—	mhos
	MTM15N06/MTP15N06				
(V_{DS} = 10 V, I_D = 6.0 A)	MTM12N08/MTP12N08		3.0	—	
	MTM12N10/MTP12N10				
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	1200	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	MTM15N05/MTP15N05	C_{oss}	—	700	pF
	MTM15N06/MTP15N06				
	MTM12N08/MTP12N08		—	500	
	MTM12N10/MTP12N10				
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	MTM15N05/MTP15N05	C_{rss}	—	250	pF
	MTM15N06/MTP15N06				
	MTM12N08/MTP12N08		—	250	
	MTM12N10/MTP12N10				

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D) R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	

SOURCE DRAIN DIODE CHARACTERISTICS*

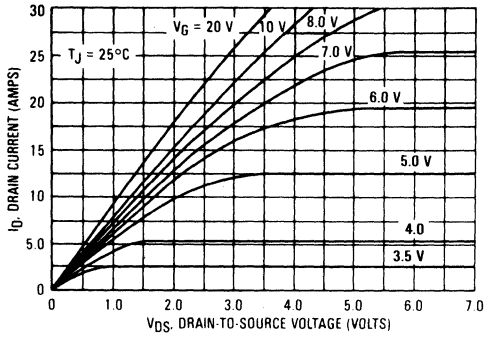
Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = Rated I_D	V_{SD}	1.4	Vdc
Forward Turn-On Time	V_{GS} = 0	t_{on}	250	ns
Reverse Recovery Time		t_{rr}	325	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

TYPICAL CHARACTERISTICS

MTM12N08, MTM12N10, MTP12N08, MTP12N10

FIGURE 1 — ON-REGION CHARACTERISTICS



MTM15N05, MTM15N06, MTP15N05, MTP15N06

FIGURE 2 — ON-REGION CHARACTERISTICS

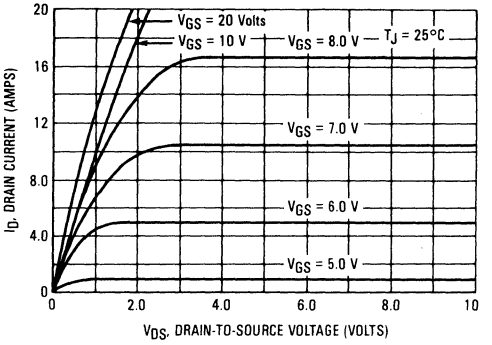


FIGURE 3 — TRANSFER CHARACTERISTICS

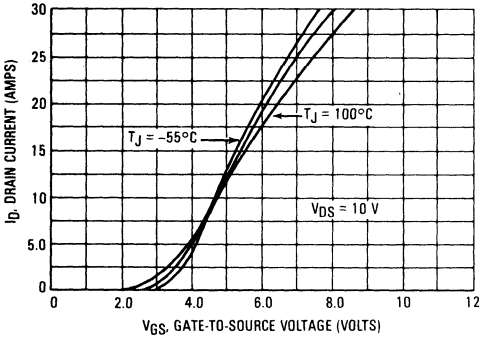


FIGURE 4 — TRANSFER CHARACTERISTICS

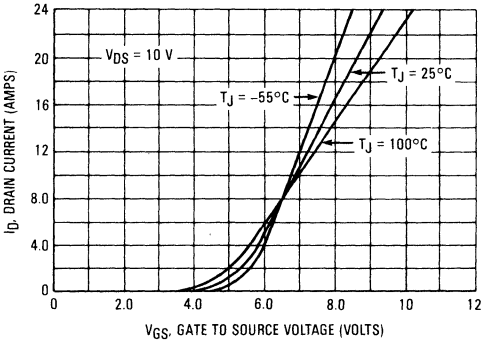


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT

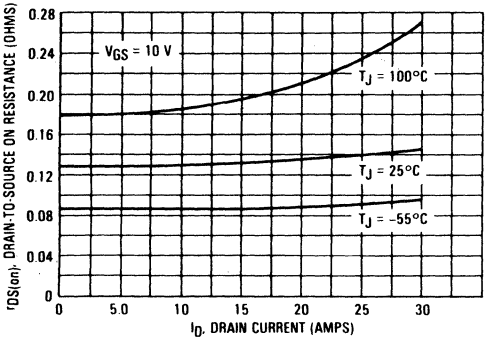
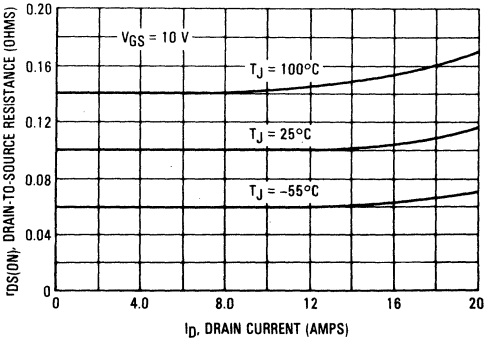


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT



C

TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

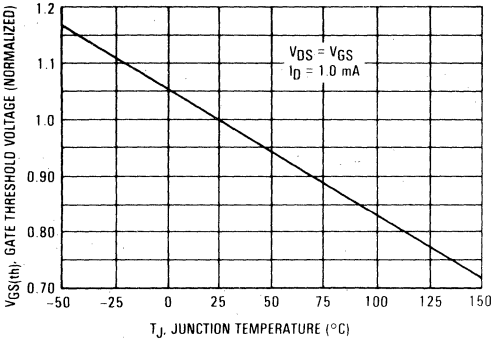
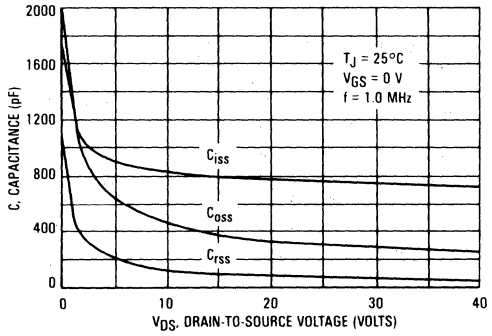


FIGURE 8 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 9 — MTM12N08/MTM12N10
MTM15N05/MTM15N06

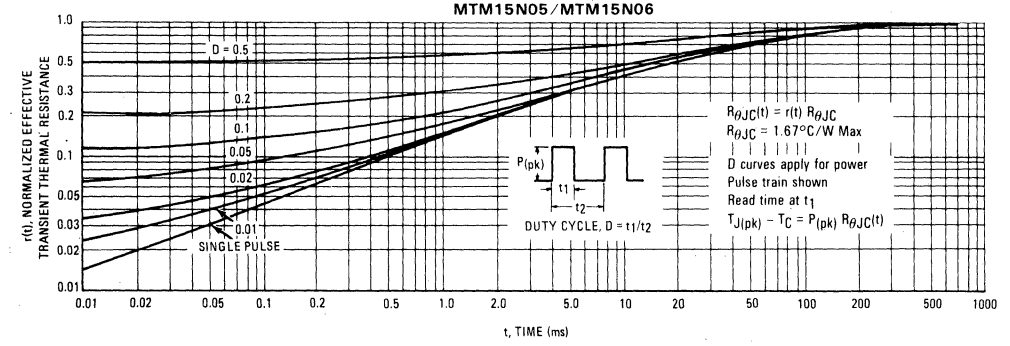
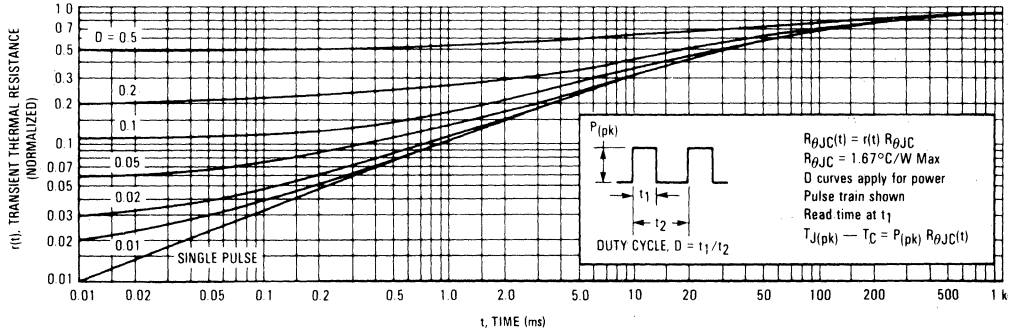


FIGURE 10 — MTP12N08/MTP12N10
MTP15N05/MTP15N06



OPERATING AREA INFORMATION

FIGURE 11 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

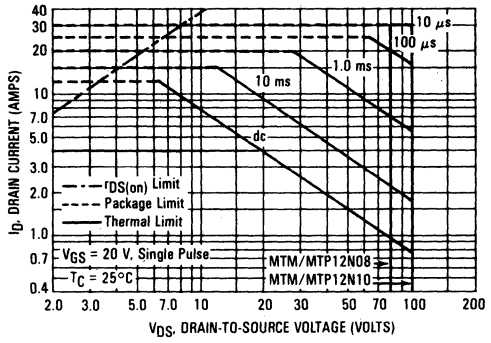


FIGURE 12 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

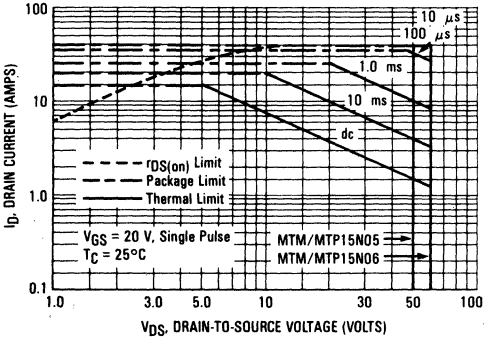
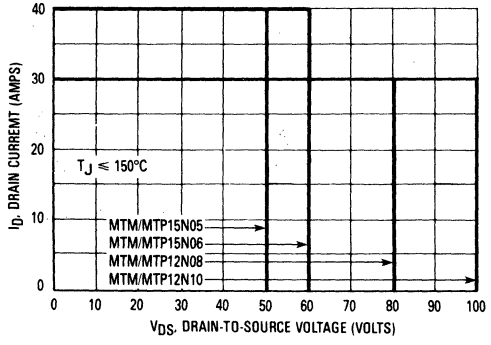


FIGURE 13 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 11 and 12 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figure 11 or 12
T_{Jmax} = Rated maximum junction temperature
T_C = Device case temperature
P_D = Rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = Rated steady state thermal resistance
r(t) = Normalized thermal response from Figures 9 and 10.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 13, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

MTM12N18, MTP12N18
MTM12N20, MTP12N20
MTM15N12, MTP15N12
MTM15N15, MTP15N15

MOTOROLA

C

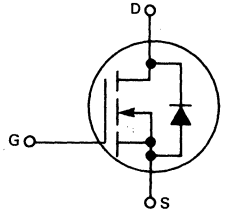
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high-speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

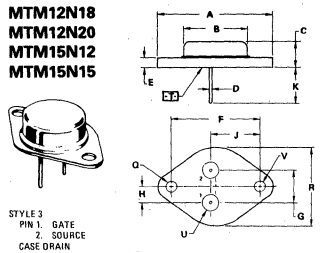
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



12 and 15 AMPERE
N-CHANNEL TMOS POWER FET
$r_{DS(on)}$ = 0.35 OHM
180 and 200 VOLTS
$r_{DS(on)}$ = 0.25 OHM
120 and 150 VOLTS

MTM12N18
MTM12N20
MTM15N12
MTM15N15



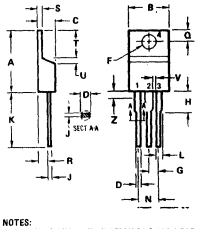
STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

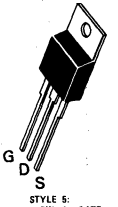
CASE 1-05
TO-204AA
(TO-3 TYPE)

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ ϕ.13 (0.005) M | T | V M
   FOR LEADS:
   ⌖ ϕ.13 (0.005) M T | V M | Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

MTP12N18
MTP12N20
MTP15N12
MTP15N15





STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

NOTES:
1. DIMENSIONS L AND H APPLIES TO ALL LEADS.
2. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.
4. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 15N12	15N15	12N18	12N20	Unit
Drain-Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous	I_D	15		12		Adc
Pulsed	I_{DM}	48		40		Apk
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C	P_D	100				Watts
Derate above 25°C		0.8				W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM15N12/MTP15N12	$V_{(BR)DSS}$	120	—	Vdc
	MTM15N15/MTP15N15		150	—	
	MTM12N18/MTP12N18		180	—	
	MTM12N20/MTP12N20		200	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)	MTM15N12/MTM15N15 MTP15N12/MTP15N15	$r_{DS(on)}$	—	0.25	Ohms
(V_{GS} = 10 Vdc, I_D = 6.0 Adc)	MTM12N18/MTM12N20 MTP12N18/MTP12N20		—	0.35	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 15 Adc)	MTM15N12/MTM15N15 MTP15N12/MTP15N15		—	4.5	
(I_D = 7.5 Adc, T_J = 100°C)	MTM15N12, MTM15N15 MTP15N12/MTP15N15		—	3.75	
(I_D = 12 Adc)	MTM12N18/MTM12N20 MTP12N18/MTP12N20		—	5.0	
(I_D = 6.0 Adc, T_J = 100°C)	MTM12N18/MTM12N20 MTP12N18/MTP12N20		—	4.2	
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)	MTM15N12/MTM15N15 MTP15N12/MTP15N15	g_{fs}	5.5	—	mhos
(V_{DS} = 15 V, I_D = 6.0 A)	MTM12N18/MTM12N20 MTP12N18/MTP12N20		4.5	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	600	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms, See Figures 1 and 2)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	250	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	120	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0,	V_{SD}	1.5	Vdc
Forward Turn-On Time		t_{on}	50	ns
Reverse Recovery Time		t_{rr}	300	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 1 — SWITCHING TEST CIRCUIT

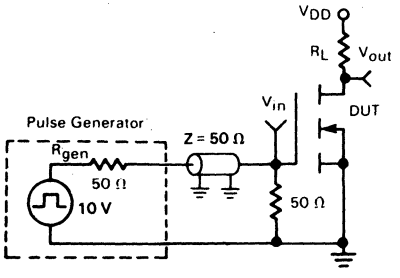
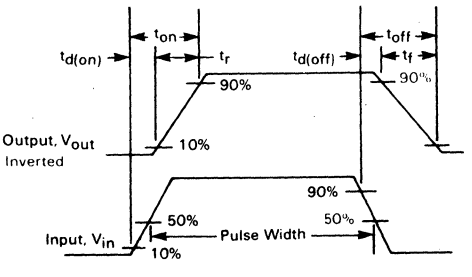


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTM15N12, MTM15N15
MTP15N12, MTP15N15

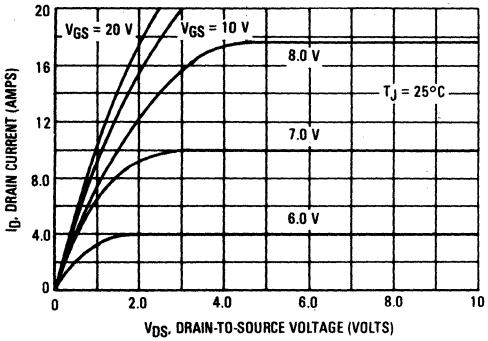
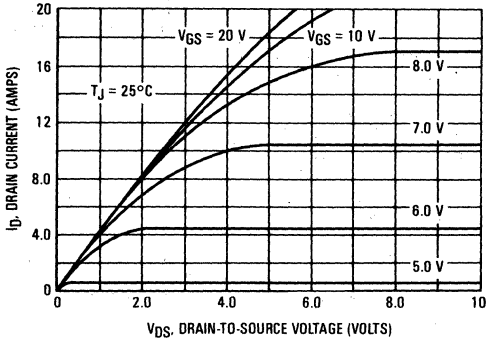


FIGURE 4 — MTM12N18, MTM12N20
MTP12N18, MTP12N20



TRANSFER CHARACTERISTICS

FIGURE 5 — MTM15N12, MTM15N15
MTP15N12, MTP15N15

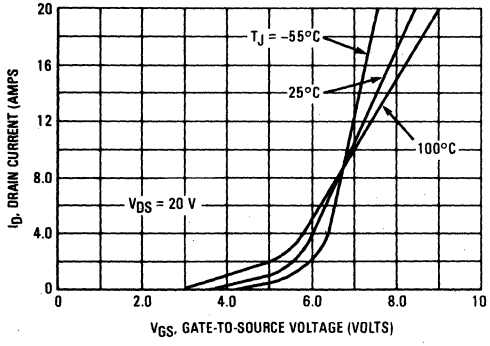
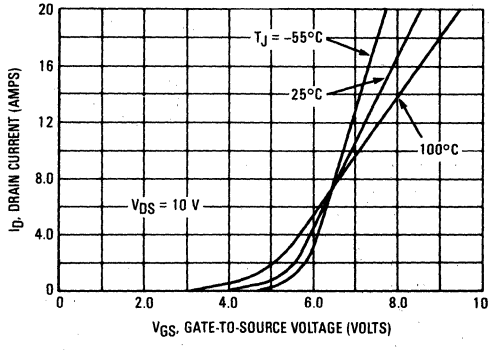


FIGURE 6 — MTM12N18, MTM12N20
MTP12N18, MTP12N20



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTM15N12, MTM15N15
MTP15N12, MTP15N15

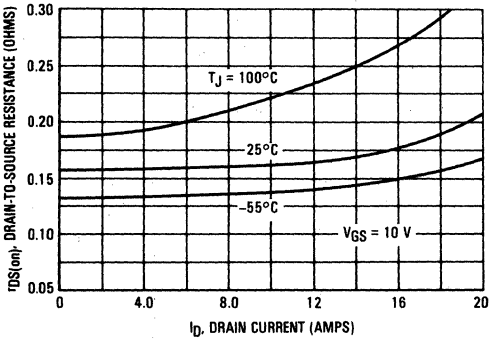
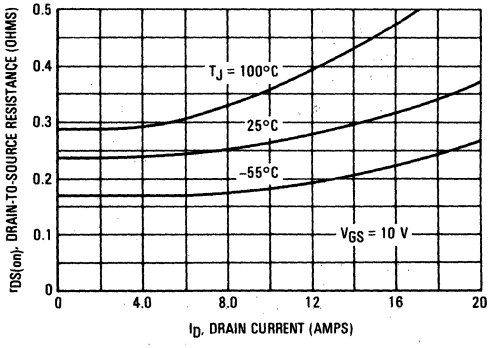


FIGURE 8 — MTM12N18, MTM12N20
MTP12N18, MTP12N20



TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

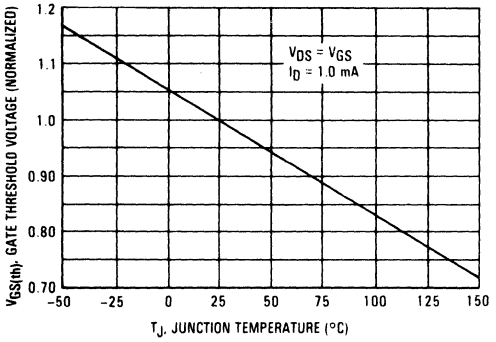
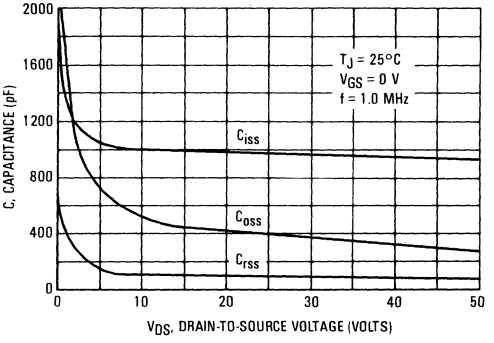


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM12N18, MTM12N20, MTM15N12 AND MTM15N15

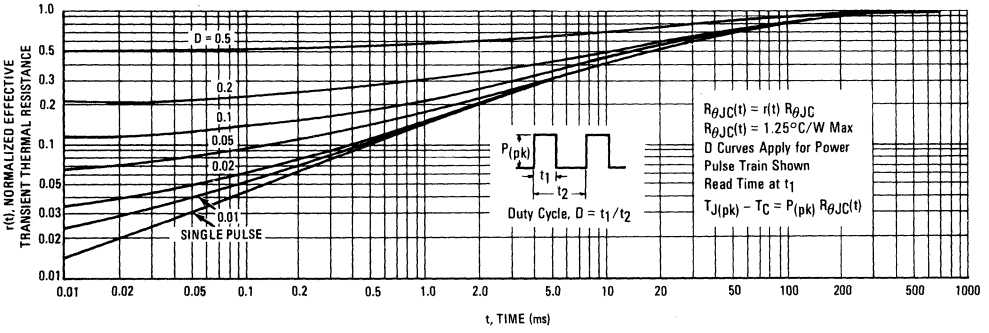
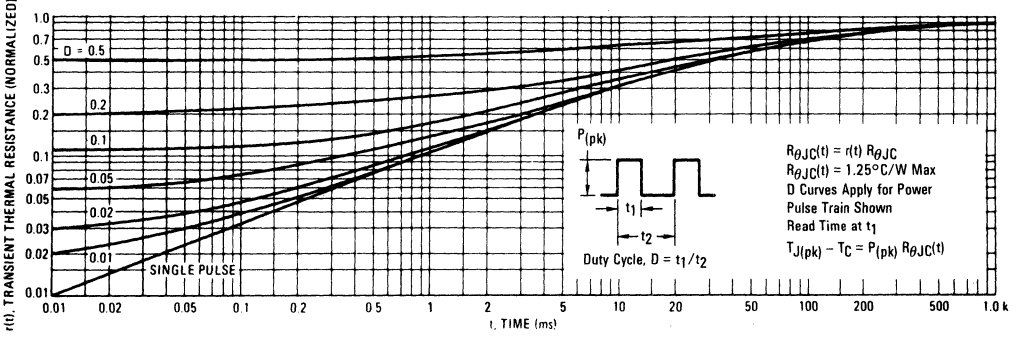


FIGURE 12 — MTP12N18, MTP12N20, MTP15N12 AND MTP15N15



C

RATED SAFE OPERATING AREA INFORMATION

FIGURE 13 — MTM15N12, MTM15N15
MTP15N12, MTP15N15

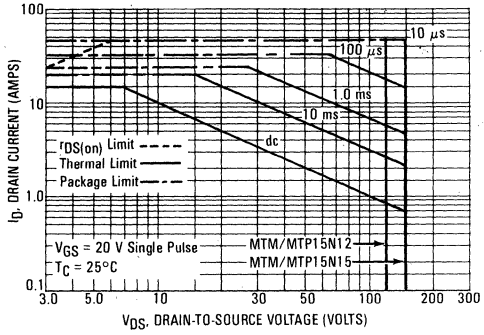


FIGURE 14 — MTM12N18, MTM12N20
MTP12N18, MTP12N20

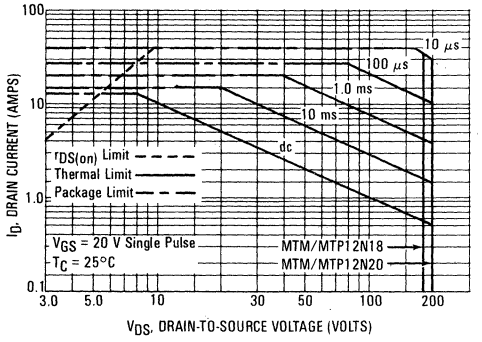
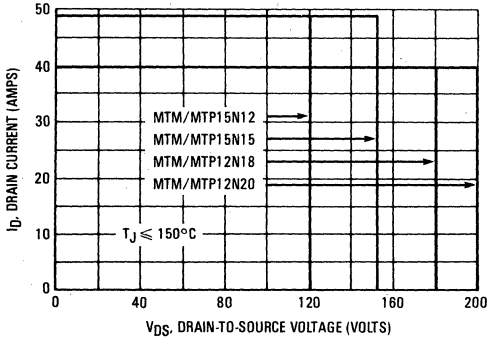


FIGURE 15 — MAXIMUM RATED SWITCHING
SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 13 and 14 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 13 and 14
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figures 11 and 12

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 15, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MOTOROLA

MTM15N18
MTM15N20
MTM20N12
MTM20N15

Designer's Data Sheet

15 and 20 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.16 OHM
180 and 200 VOLTS

$r_{DS(on)}$ = 0.12 OHM
120 and 150 VOLTS

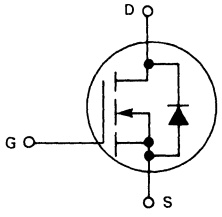
C

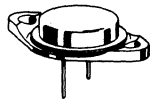
N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTORS

These TMOS Power FETs are designed for high-speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

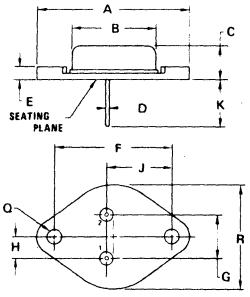
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™





MTM15N18
MTM15N20
MTM20N12
MTM20N15



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE Type
(TO-3 TYPE)

MAXIMUM RATINGS

Rating	Symbol	MTM 20N12	MTM 20N15	MTM 15N18	MTM 15N20	Unit
Drain-Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	I_D I_{DM}	20 100		15 80		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM20N12	$V_{(BR)DSS}$	120	—	Vdc
	MTM20N15		150	—	
	MTM15N18		180	—	
	MTM15N20		200	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)	MTM20N12/MTM20N15	$r_{DS(on)}$	—	0.12	Ohms
(V_{GS} = 10 Vdc, I_D = 7.5 Adc)	MTM15N18/MTM15N20		—	0.16	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 20 Adc)	MTM20N12/MTM20N15		—	3.0	
(I_D = 10 Adc, T_J = 100°C)	MTM20N12/MTM20N15		—	2.4	
(I_D = 15 Adc)	MTM15N18, MTM15N20		—	3.0	
(I_D = 7.5 Adc, T_J = 100°C)	MTM15N18/MTM15N20		—	2.4	
Forward Transconductance (V_{DS} = 15 V, I_D = 10 A)	MTM20N12/MTM20N15	g_{fs}	8.0	—	mhos
(V_{DS} = 15 V, I_D = 7.5 A)	MTM15N18/MTM15N20		4.0	—	

DYNAMIC CHARACTERISTICS

Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	700	pF
Reverse Transfer Capacitance		C_{rss}	—	200	pF

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms, See Figures 1 and 2)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	220	
Fall Time		t_f	—	250	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0,	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	50	ns
Reverse Recovery Time		t_{rr}	450	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

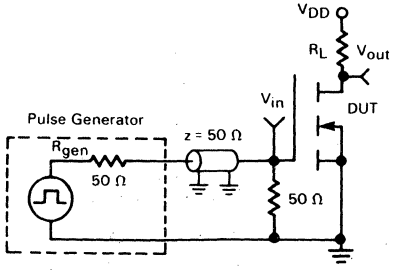
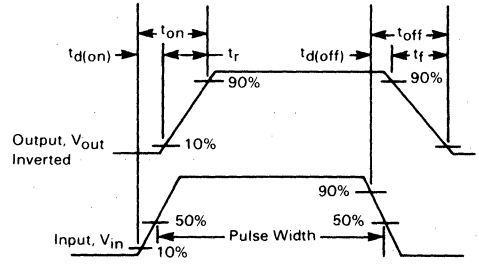


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTM20N12, MTM20N15

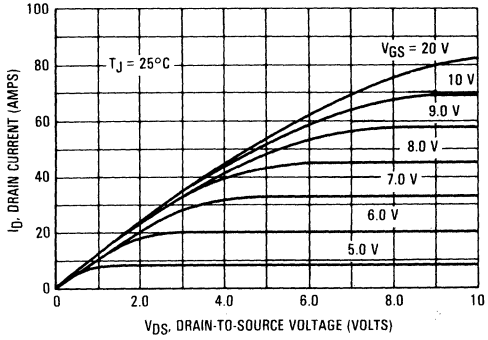
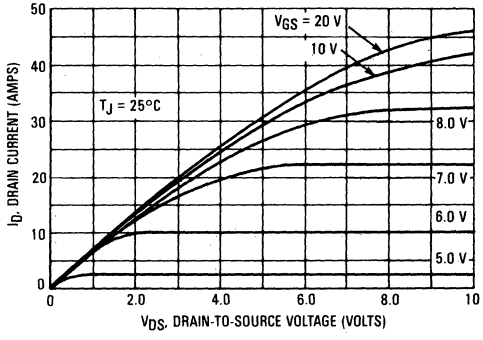


FIGURE 4 — MTM15N18, MTM15N20



TRANSFER CHARACTERISTICS

FIGURE 5 — MTM20N12, MTM20N15

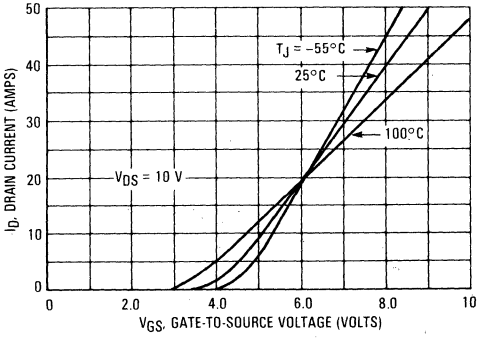
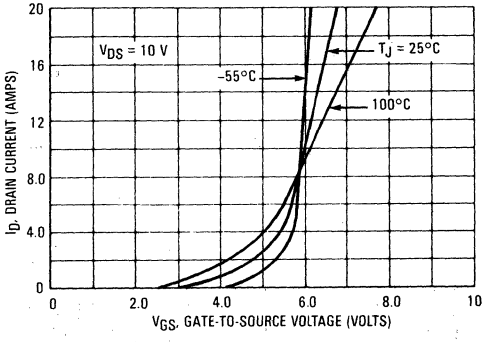


FIGURE 6 — MTM15N18, MTM15N20



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTM20N12, MTM20N15

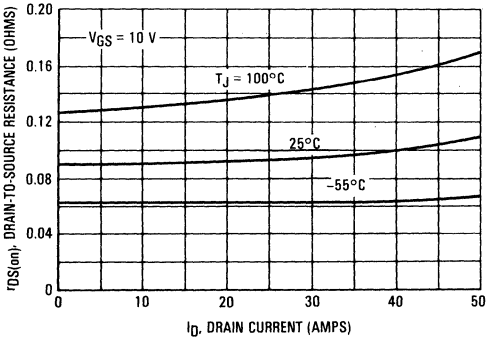
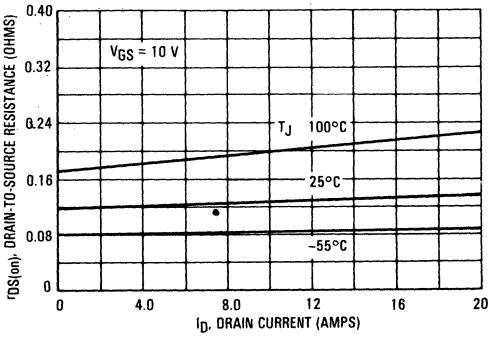


FIGURE 8 — MTM15N18, MTM15N20



C

TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

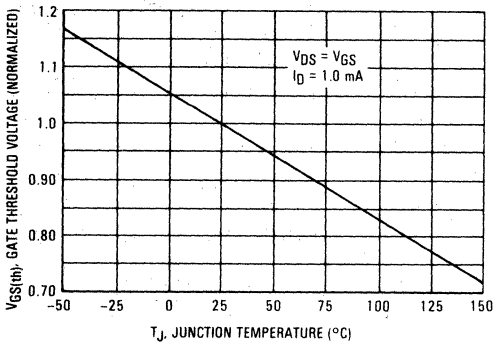
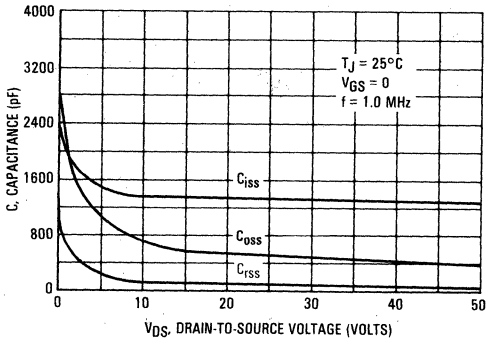
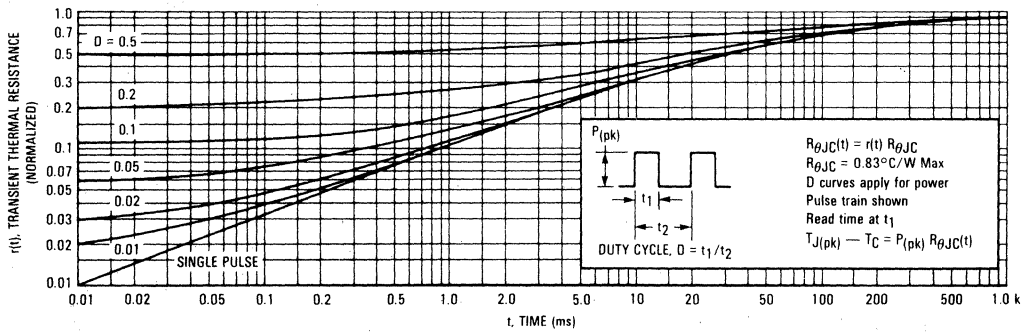


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM15N18, MTM15N20, MTM20N12 AND MTM20N15



RATED SAFE OPERATING AREA INFORMATION

FIGURE 12 — MTM20N12, MTM20N15

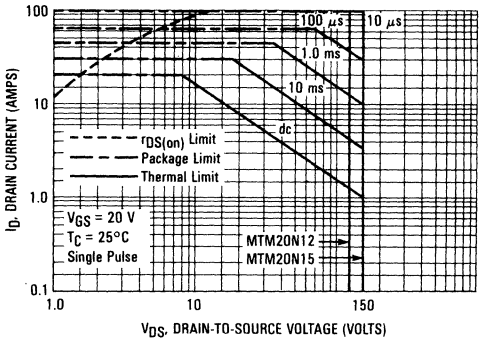


FIGURE 13 — MTM15N18, MTM15N20

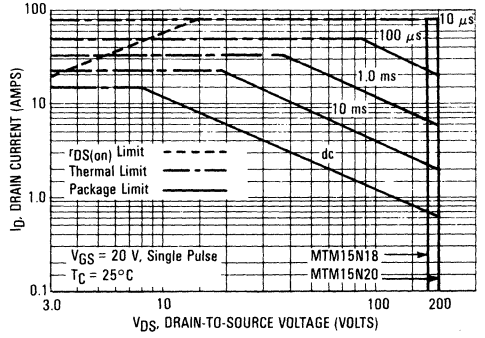
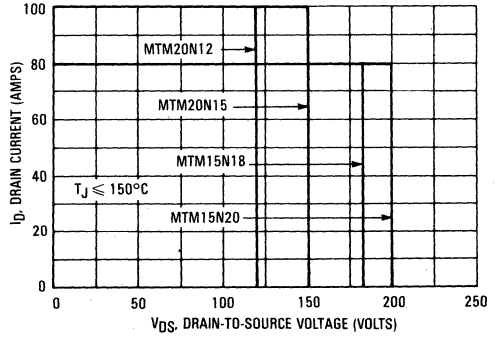


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 12 and 13.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MTM15N35
MTM15N40

MOTOROLA

C

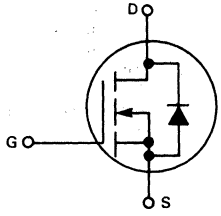
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

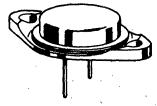
TMOS™



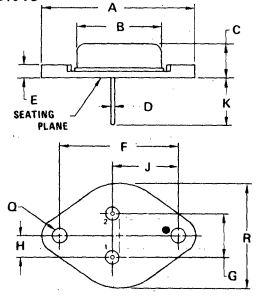
15 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.3 OHMS
350 and 400 VOLTS



MTM15N35
MTM15N40



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE (TYPE)
(TO-3 TYPE)

MAXIMUM RATINGS

Rating	Symbol	MTM15N35	MTM15N40	Unit
Drain-Source Voltage	V_{DSS}	350	400	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	350	400	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 15 70		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 2.0		Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM15N35 MTM15N40	$V_{(BR)DSS}$	350 400	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 7.5 Adc) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	**2.25** **6.0** **4.5**	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	**0.3**	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{fs}	6.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3600	pF
Output Capacitance		C_{oss}	—	700	pF
Reverse Transfer Capacitance		C_{rss}	—	300	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 7.5 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	120	ns
Rise Time		t_r	—	300	ns
Turn-Off Delay Time		$t_{d(off)}$	—	400	ns
Fall Time		t_f	—	240	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 15 A V_{GS} = 0	V_{SD}	1.0	Vdc
Forward Turn-On Time		t_{on}	175	ns
Reverse Recovery Time		t_{rr}	600	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

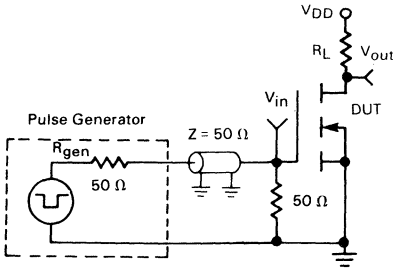
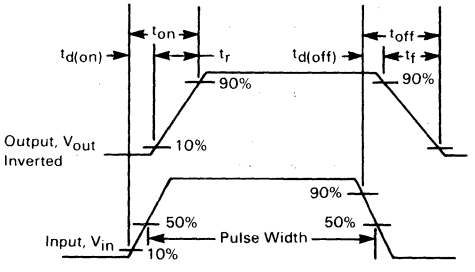


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

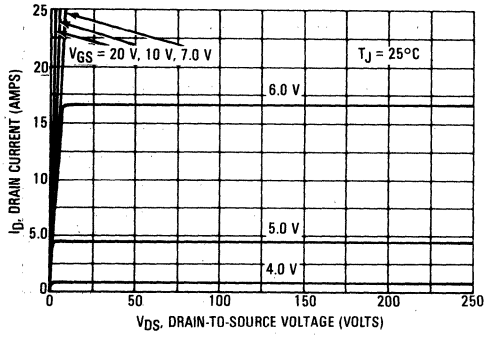


FIGURE 4 — ON CHARACTERISTICS

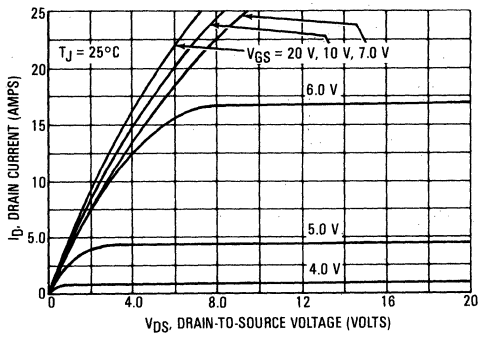


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

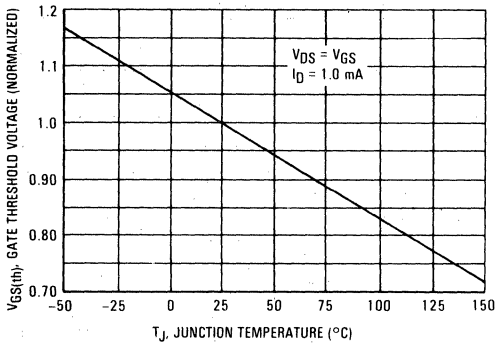


FIGURE 6 — TRANSFER CHARACTERISTICS

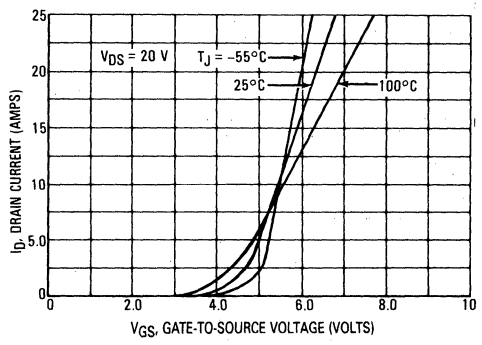


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

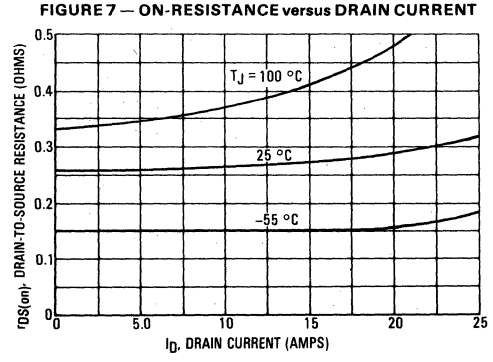
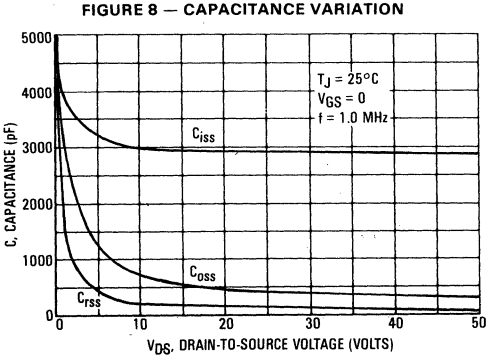


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

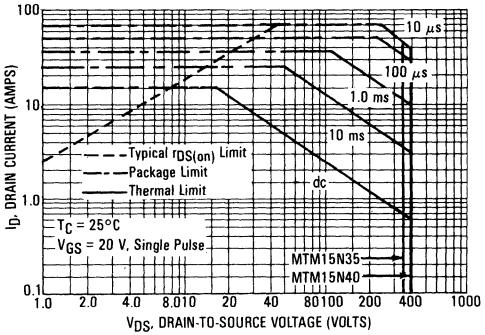
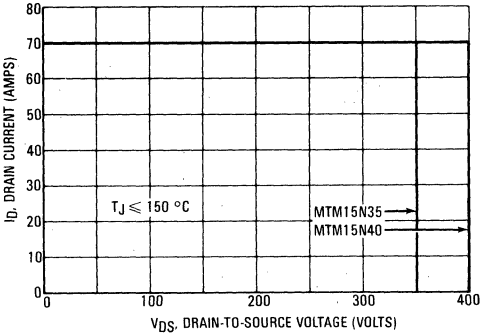


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figure 11.

SWITCHING SAFE OPERATING AREA

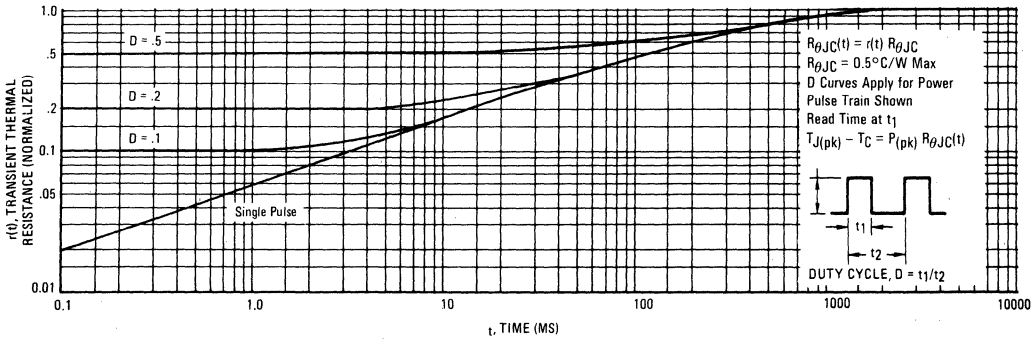
The switching safe operating area (SOA) of Figure 10 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

THERMAL RESPONSE

FIGURE 11 — MTM15N35/MTM15N40



MTM15N45
MTM15N50

MOTOROLA

C

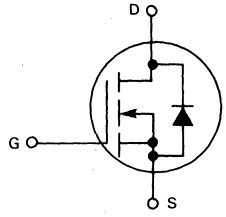
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, and motor controls.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

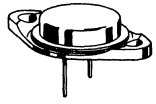
TMOS™



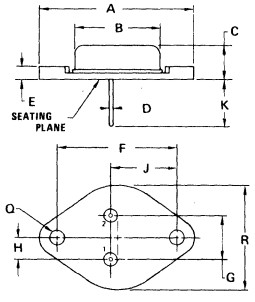
15 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.4 OHM
450 and 500 VOLTS



MTM15N45
MTM15N50



STYLE 1:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE (TYPE)
(TO-3 TYPE)

MAXIMUM RATINGS

Rating	Symbol	MTM15N45	MTM15N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGO}	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 15 65		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 2.0		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM15N45 MTM15N50	$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 7.5 Adc) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	3.0 7.5 6.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	0.4	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{fs}	4.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3600	pF
Output Capacitance		C_{oss}	—	700	pF
Reverse Transfer Capacitance		C_{rss}	—	300	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 7.5 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	120	ns
Rise Time		t_r	—	300	ns
Turn-Off Delay Time		$t_{d(off)}$	—	400	ns
Fall Time		t_f	—	240	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 15 A V_{GS} = 0	V_{SD}	1.5	Vdc
Forward Turn-On Time		t_{on}	175	ns
Reverse Recovery Time		t_{rr}	600	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

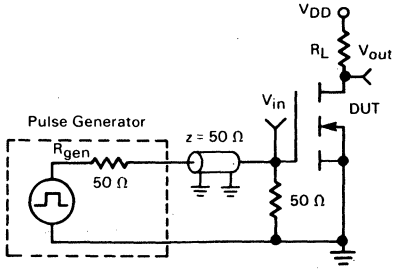
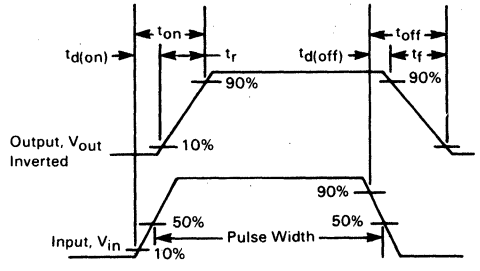


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

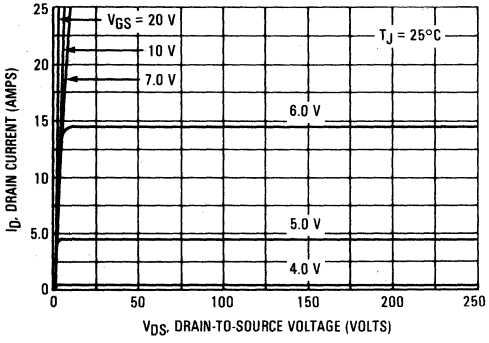


FIGURE 4 — ON-REGION CHARACTERISTICS

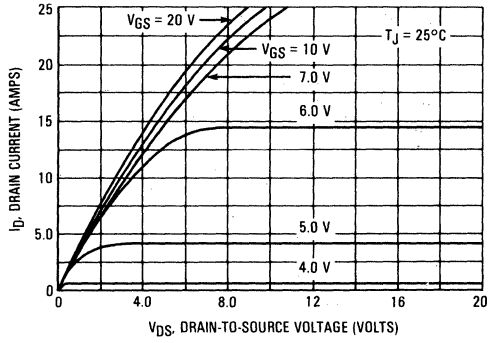


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

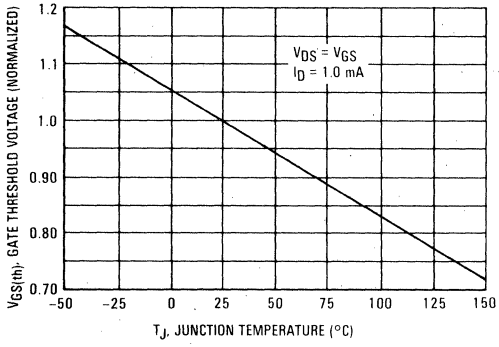


FIGURE 6 — TRANSFER CHARACTERISTICS

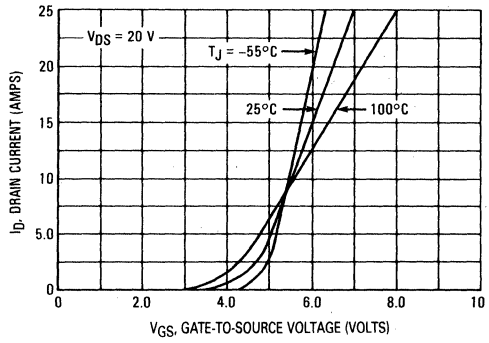


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

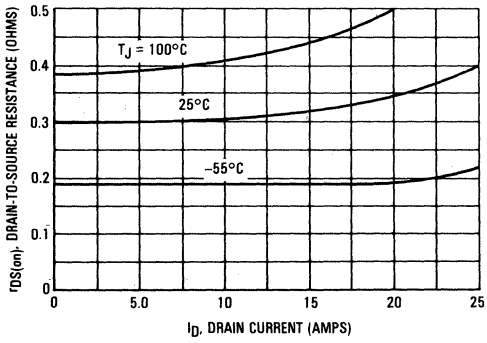
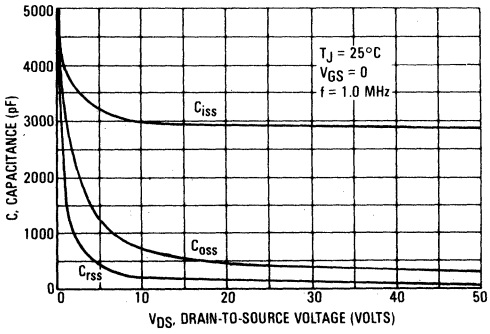


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

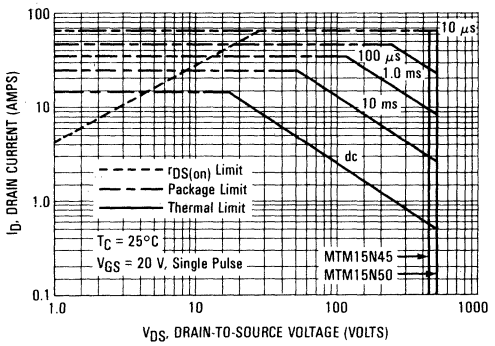
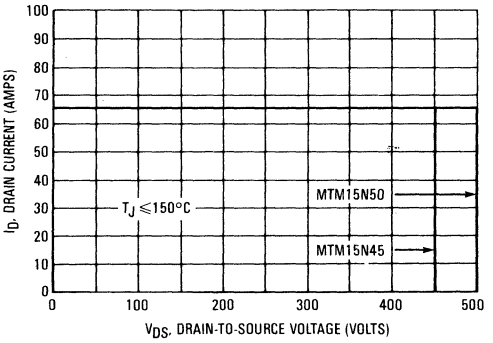


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
$r(t)$ = normalized thermal response from Figure 11.

SWITCHING SAFE OPERATING AREA

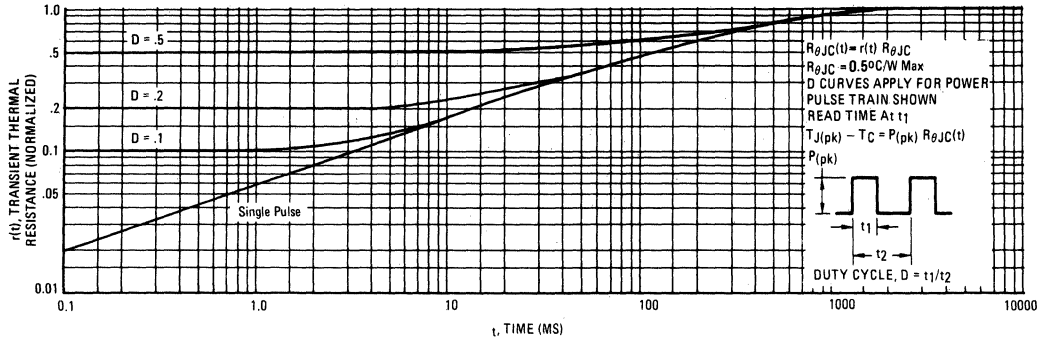
The switching safe operating area (SOA) of Figure 10 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

C

FIGURE 11 — MTM15N45/MTM15N50



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 2.5 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

MOTOROLA

MTM20N08 MTP20N08
MTM20N10 MTP20N10
MTM25N05 MTP25N05
MTM25N06 MTP25N06

Designer's Data Sheet

20 and 25 AMPERE

N-CHANNEL TMOS POWER FETs

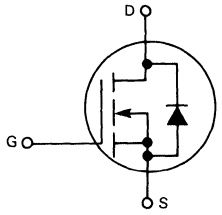
$r_{DS(on)}$ = 0.15 OHM
80 and 100 VOLTS
$r_{DS(on)}$ = 0.08 OHM
50 and 60 VOLTS

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

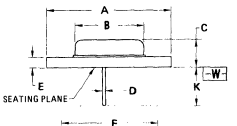
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

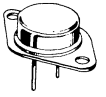
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

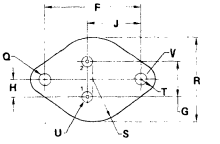
TMOS™



MTM25N05
MTM25N06
MTM20N08
MTM20N10





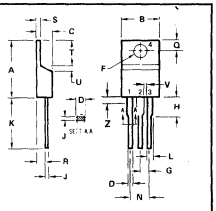


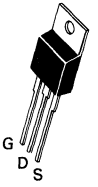
STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA
(TO-3 TYPE)

MTP25N05
MTP25N06
MTP20N08
MTP20N10





NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3 ONLY.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.
5. CONTROLLING DIMENSION: INCH.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 25N05	25N06	20N08	20N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 25 80		 20 60		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM25N05/MTP25N05	$V_{(BR)DSS}$	50	—	Vdc
	MTM25N06/MTP25N06		60	—	
	MTM20N08/MTP20N08		80	—	
	MTM20N10/MTP20N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_C = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 12.5 Adc)	MTM25N05/MTP25N05	$r_{DS(on)}$	—	0.08	Ohm
	MTM25N06/MTP25N06				
(V_{GS} = 10 Vdc, I_D = 10 Adc)	MTM20N08/MTP20N08		—	0.15	
	MTM20N10/MTP20N10				
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 25 Adc	MTM25N05/MTP25N05		—	2.4	
	MTM25N06/MTP25N06				
(I_D = 12.5 Adc, T_J = 100°C)	MTM25N05/MTP25N05		—	2.0	
	MTM25N06/MTP25N06				
(I_D = 20 Adc)	MTM20N08/MTP20N08		—	3.6	
	MTM20N10/MTP20N10				
(I_D = 10 Adc, T_C = 100°C)	MTM20N08/MTP20N08		—	3.0	
	MTM20N10/MTP20N10				
Forward Transconductance (V_{DS} = 15 V, I_D = 12.5 A)	MTM25N05/MTP25N05	g_{fs}	6.0	—	mhos
	MTM25N06/MTP25N06				
(V_{DS} = 10 V, I_D = 10 A)	MTM20N08/MTP20N08		6.0	—	
	MTM20N10/MTP20N10				

DYNAMIC CHARACTERISTICS

Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1400	pF
Output Capacitance		C_{oss}	—	1200	
Reverse Transfer Capacitance		C_{rss}	—	400	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D) R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	200	

SOURCE DRAIN DIODE CHARACTERISTICS*

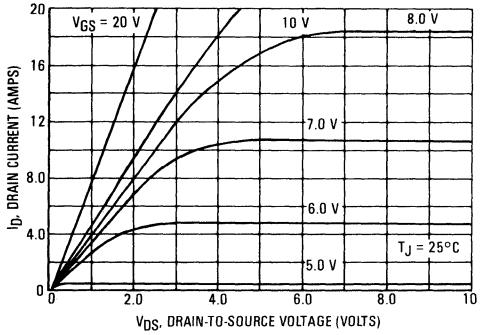
Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = Rated I_D	V_{SD}	2.0 (1)	Vdc
Forward Turn-On Time	V_{GS} = 0	t_{on}	50	ns
Reverse Recovery Time		t_{rr}	300	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.
(1) Add 0.5 V for MTM/MTP25N05 and MTM/MTP25N06.

TYPICAL CHARACTERISTICS

MTM20N08, MTM20N10, MTP20N08, MTP20N10

FIGURE 1 — ON-REGION CHARACTERISTICS



MTM25N05, MTM25N06, MTP25N05, MTP25N06

FIGURE 2 — ON-REGION CHARACTERISTICS

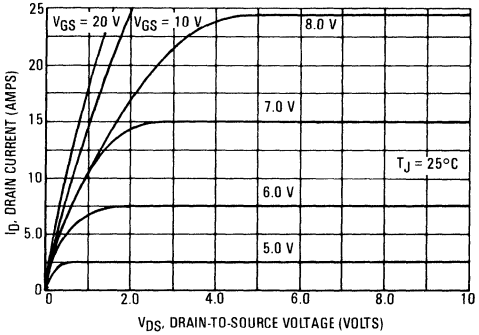


FIGURE 3 — TRANSFER CHARACTERISTICS

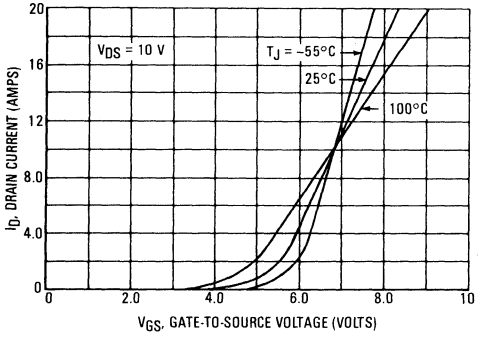


FIGURE 4 — TRANSFER CHARACTERISTICS

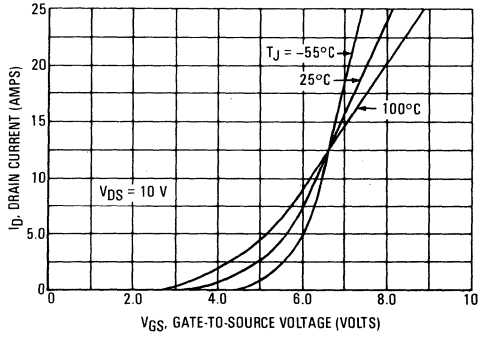


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT

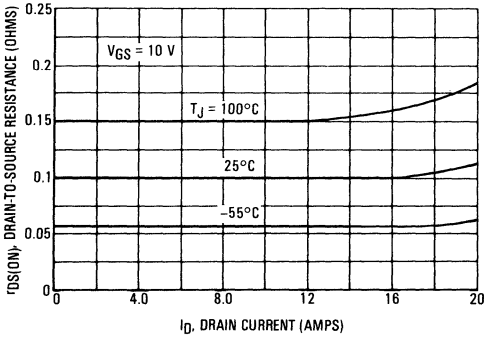
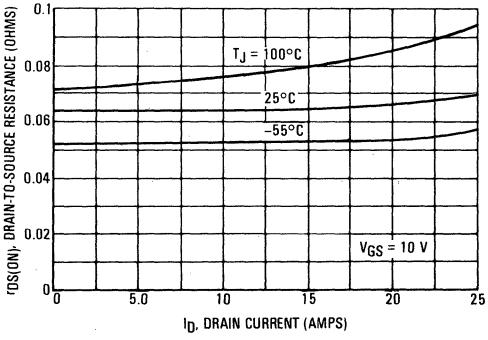


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT



C

C

TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

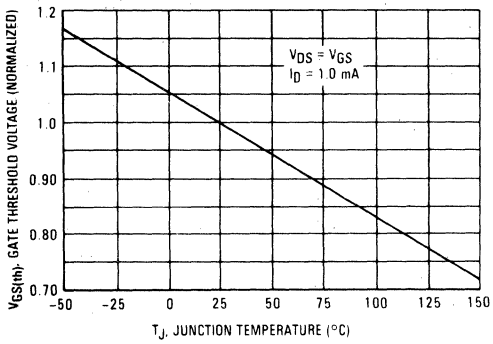
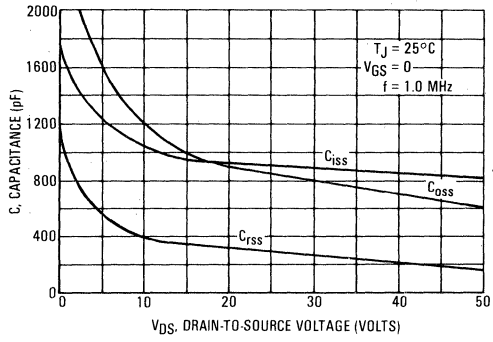


FIGURE 8 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 9 — MTM20N08/MTM20N10
MTM25N05/MTM25N06

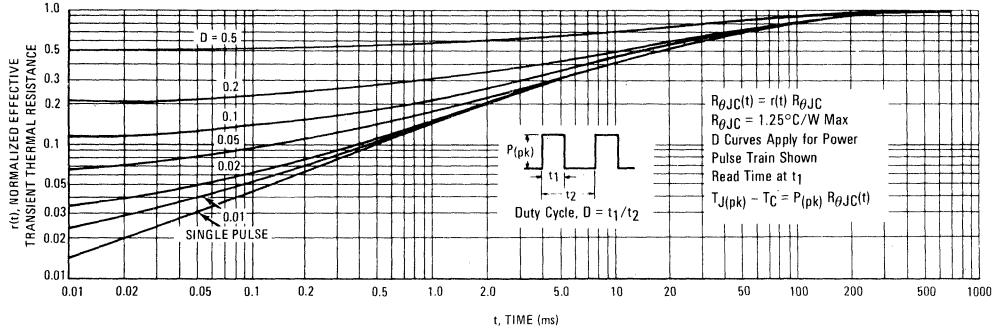
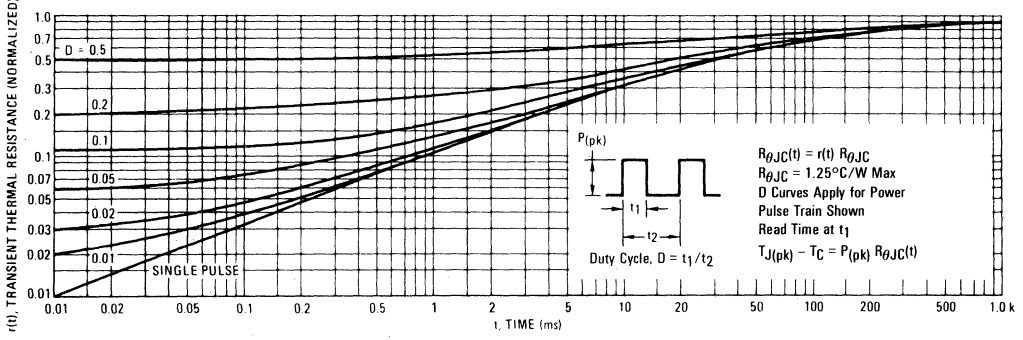


FIGURE 10 — MTP20N08/MTP20N10
MTP25N05/MTP25N06



OPERATING AREA INFORMATION

FIGURE 11 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

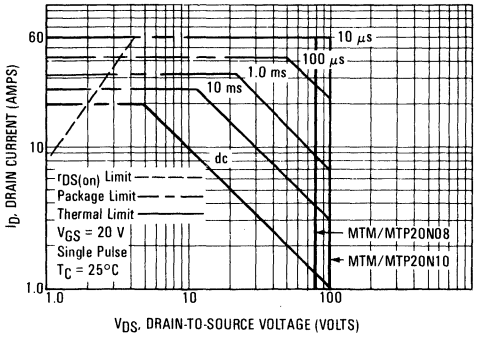


FIGURE 12 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

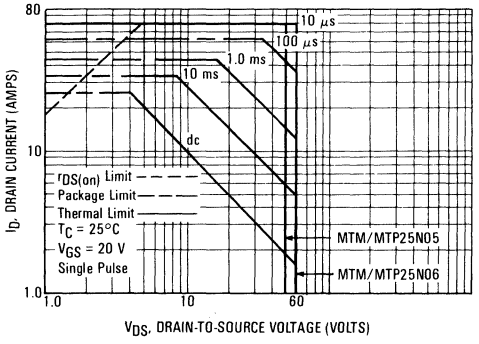
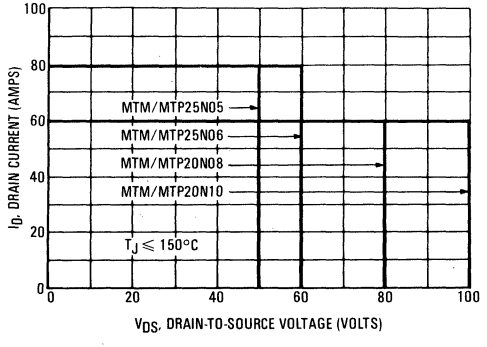


FIGURE 13 — MAXIMUM SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 11 and 12 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figures 11 or 12
T_{Jmax} = Rated maximum junction temperature
T_C = Device case temperature
P_D = Rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = Rated steady state thermal resistance
r(t) = Normalized thermal response from Figures 9 and 10.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 13, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

MTM25N08
MTM25N10
MTM35N05
MTM35N06

MOTOROLA

C

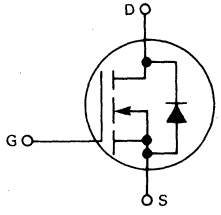
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



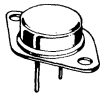
25 and 35 AMPERE

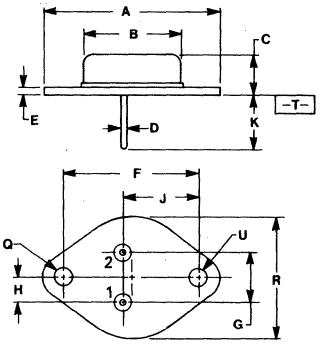
N-CHANNEL TMOS POWER FETs

$r_{DS(on)}$ = 0.075 OHM
80 and 100 VOLTS

$r_{DS(on)}$ = 0.055 OHM
50 and 60 VOLTS

MTM35N05
MTM35N06
MTM25N08
MTM25N10





STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

NOTES:
1. DIMENSIONS Q AND U ARE DATUMS AND -T- IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⌖ | ϕ 0.010 Ⓜ | T | U Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⌖ | ϕ 0.012 Ⓜ | T | Q Ⓜ | U Ⓜ
4. DIMENSIONING AND TOLERANCING PER Y14.5, 1982.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	1.52	1.77	0.060	0.070
F	30.14 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.08	0.151	0.161
R	25.15	26.67	0.990	1.050
U	3.84	4.08	0.151	0.161

CASE 197A-01
TO-204AE
(TO-3 TYPE)

MAXIMUM RATINGS

Rating	Symbol	MTM 35N05	MTM 35N06	MTM 25N08	MTM 25N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	I_D I_{DM}	35 150		25 125		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM35N05	$V_{(BR)DSS}$	50	—	Vdc
	MTM35N06		60	—	
	MTM25N08		80	—	
	MTM25N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_C = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 17.5 Adc)	MTM35N05/MTM35N06	$r_{DS(on)}$	—	0.055	Ohm
(V_{GS} = 10 Vdc, I_D = 12.5 Adc)	MTM25N08/MTM25N10		—	0.075	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 35 Adc)	MTM35N05/MTM35N06		—	2.3	
(I_D = 17.5 Adc, T_J = 100°C)	MTM35N05/MTM35N06		—	1.9	
(I_D = 25 Adc)	MTM25N08/MTM25N10		—	2.25	
(I_D = 12.5 Adc, T_C = 100°C)	MTM25N08/MTM25N10		—	1.8	
Forward Transconductance (V_{DS} = 15 V, I_D = 17.5 A)	MTM35N05/MTM35N06	g_{fs}	8.0	—	mhos
(V_{DS} = 10 V, I_D = 12.5 A)	MTM25N08/MTM25N10		5.0	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D) R_{gen} = 50 ohms)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	300	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = Rated I_D	V_{SD}	1.5	Vdc
Forward Turn-On Time	V_{GS} = 0	t_{on}	50	ns
Reverse Recovery Time		t_{rr}	450	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

C

TYPICAL CHARACTERISTICS

MTM25N08, MTM25N10

FIGURE 1 — ON-REGION CHARACTERISTICS

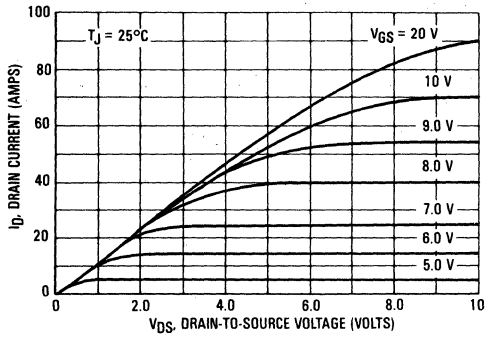


FIGURE 3 — TRANSFER CHARACTERISTICS

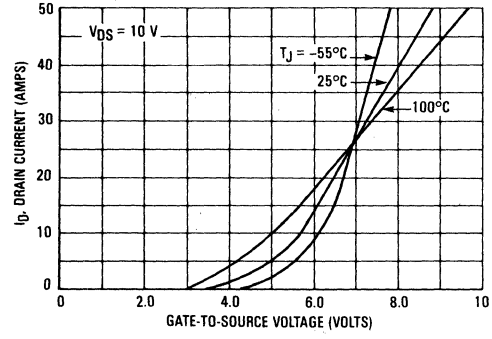
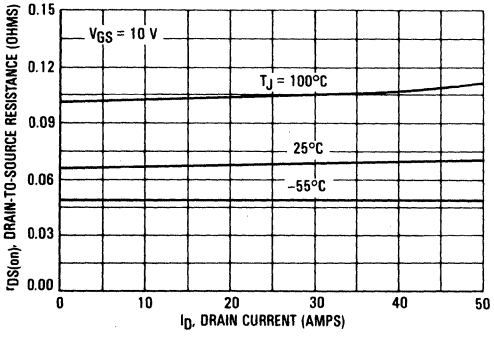


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT



MTM35N05, MTM35N06

FIGURE 2 — ON-REGION CHARACTERISTICS

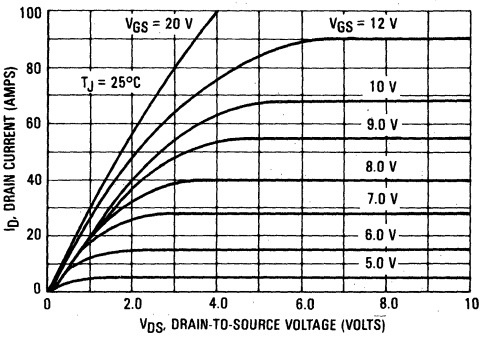


FIGURE 4 — TRANSFER CHARACTERISTICS

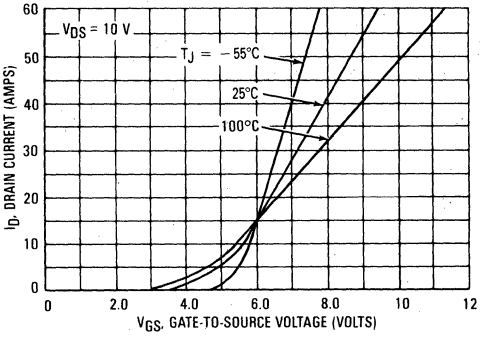
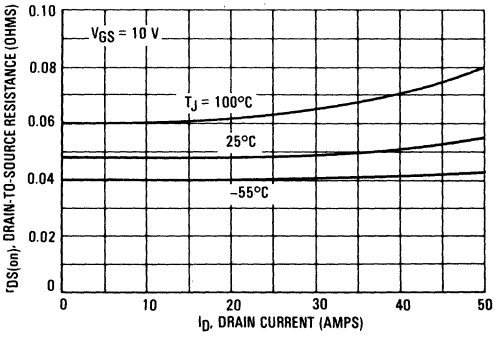


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

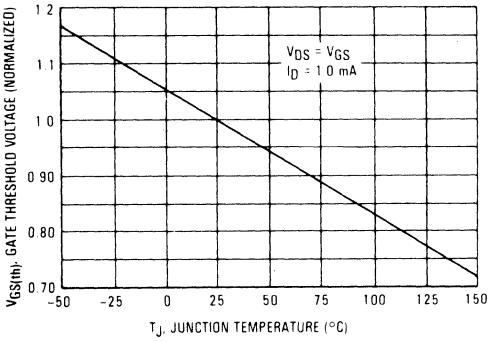
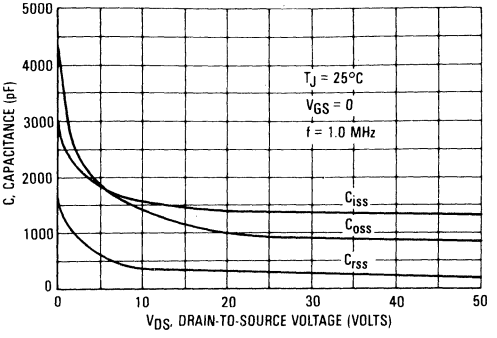
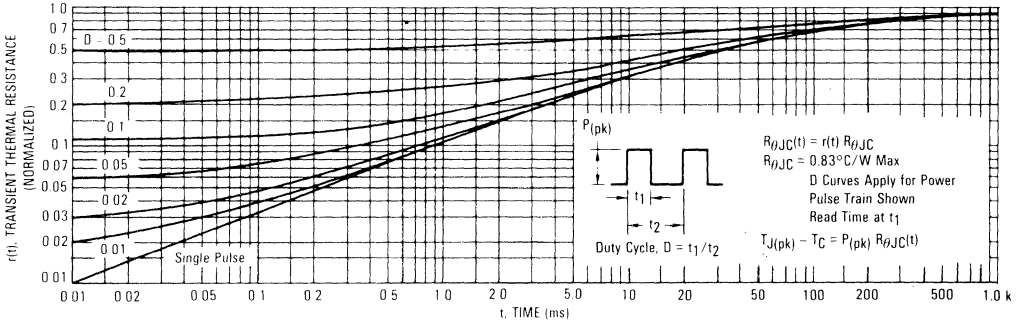


FIGURE 8 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 9 — MTM25N08/MTM25N10
MTM35N05/MTM35N06



C

OPERATING AREA INFORMATION

FIGURE 10 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

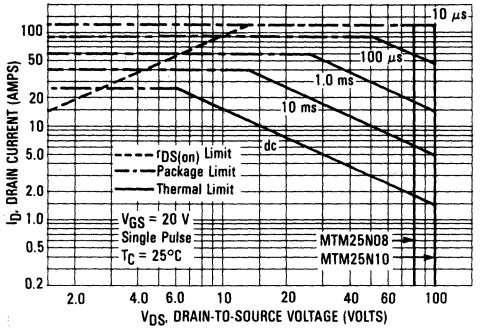


FIGURE 11 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

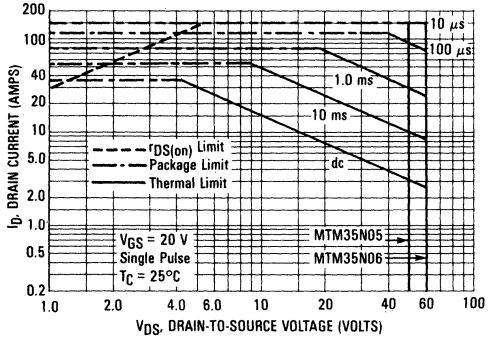
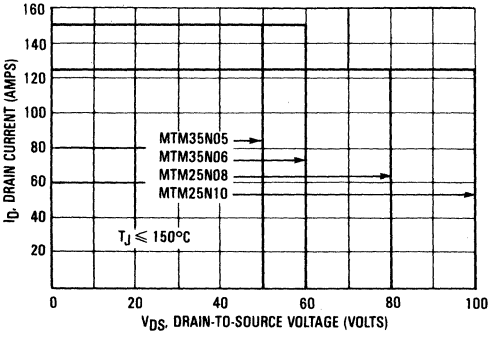


FIGURE 12 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 10 and 11 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_D(25°C)\left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

Where

I_D (25°C) = dc drain current at T_C = 25°C from Figures 10 or 11
T_{Jmax} = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 9

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 12, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MOTOROLA

MTM40N18
MTM40N20
MTM45N12
MTM45N15

C

Designer's Data Sheet

40 and 45 AMPERE

N-CHANNEL TMOS POWER FETs

$r_{DS(on)}$ = 0.08 OHM
180 and 200 VOLTS

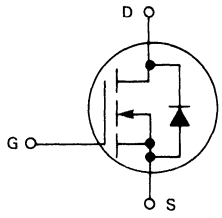
$r_{DS(on)}$ = 0.06 OHM
120 and 150 VOLTS

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

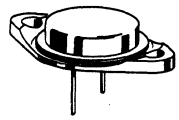
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



MTM40N18
MTM40N20
MTM45N12
MTM45N15



MAXIMUM RATINGS

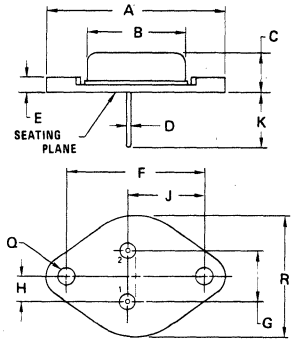
Rating	Symbol	MTM 45N12	MTM 45N15	MTM 40N18	MTM 40N20	Unit
Drain-Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	I_D I_{DM}	45 225		40 200		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 2:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE
(TO-3 TYPE)

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM45N12	$V_{BR(DSS)}$	120	—	Vdc
	MTM45N15		150	—	
	MTM40N18		180	—	
	MTM40N20		200	—	
Zero Gate Voltage Drain Current (V_{DSS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_C = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100 °C			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 22.5 Adc)	MTM45N12/MTM45N15	$r_{DS(on)}$	—	0.06	Ohm
(V_{GS} = 10 Vdc, I_D = 20 Adc)	MTM40N18/MTM40N20		—	0.08	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 45 Adc)	MTM45N12/MTM45N15		—	3.24	
(I_D = 22.5 Adc, T_J = 100°C)	MTM45N12/MTM45N15		—	2.70	
(I_D = 40 Adc)	MTM40N18/MTM40N20		—	3.80	
(I_D = 20 Adc, T_C = 100°C)	MTM40N18/MTM40N20		—	3.20	
Forward Transconductance (V_{DS} = 15 V, I_D = 12.5 A)	MTM45N12/MTM45N15	g_{fs}	10	—	mhos
(V_{DS} = 15 V, I_D = 10 A)	MTM40N18/MTM40N20		10	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	—	5500	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	500	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 1 and 2	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	150	

SOURCE-DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.0	Vdc
Forward Turn-On Time		t_{on}	150	ns
Reverse Recovery Time		t_{rr}	200	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

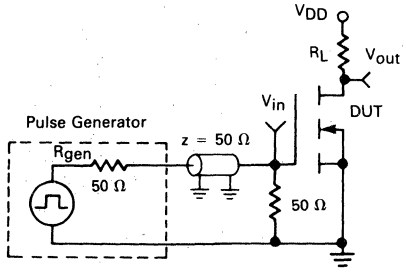
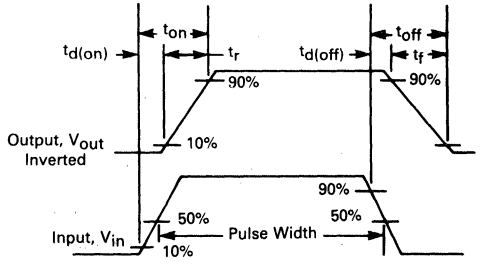


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

MTM45N12, MTM45N15

FIGURE 3 — ON-REGION CHARACTERISTICS

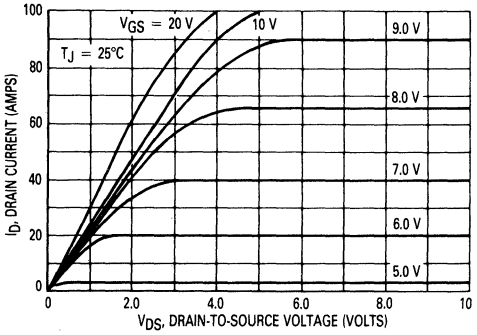


FIGURE 5 — TRANSFER CHARACTERISTICS

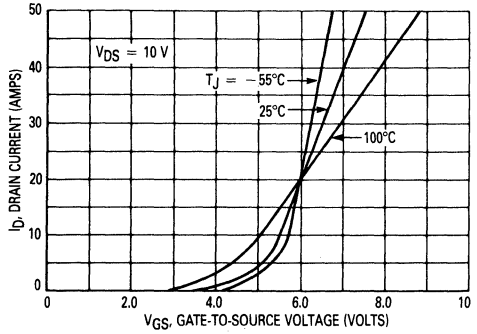
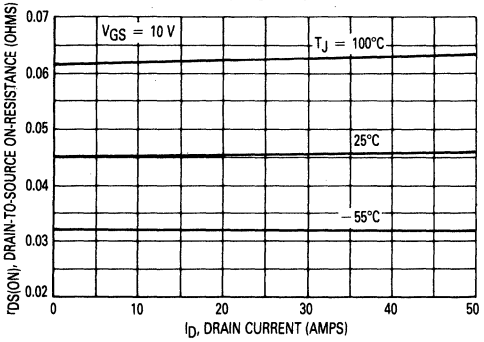


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT



MTM40N18, MTM40N20

FIGURE 4 — ON-REGION CHARACTERISTICS

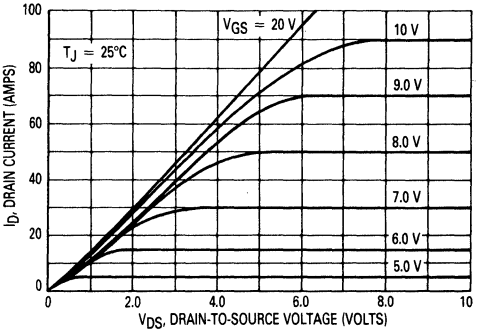


FIGURE 6 — TRANSFER CHARACTERISTICS

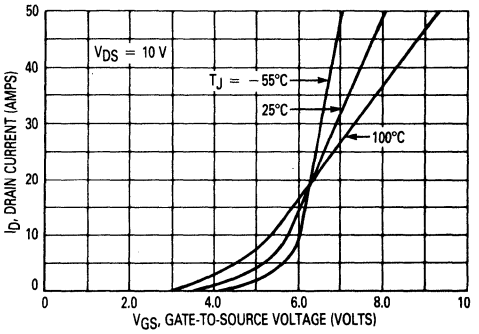
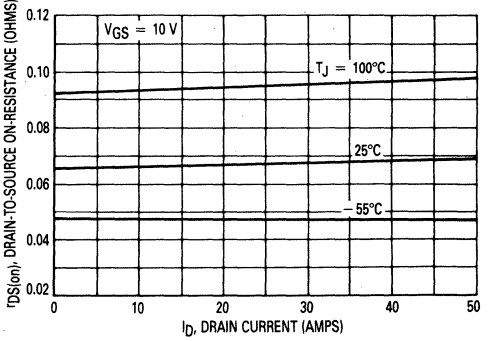


FIGURE 8 — ON-RESISTANCE versus DRAIN CURRENT



C

C

TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

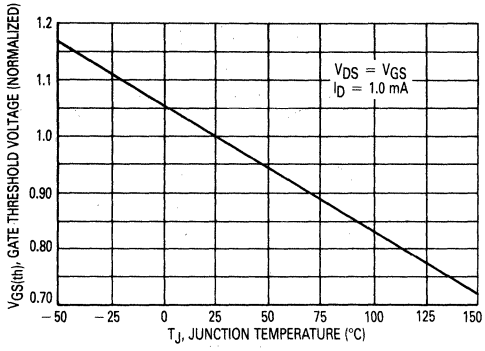
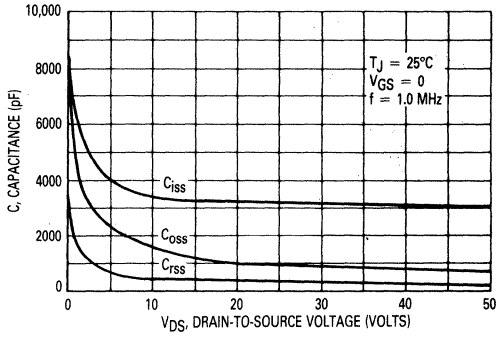
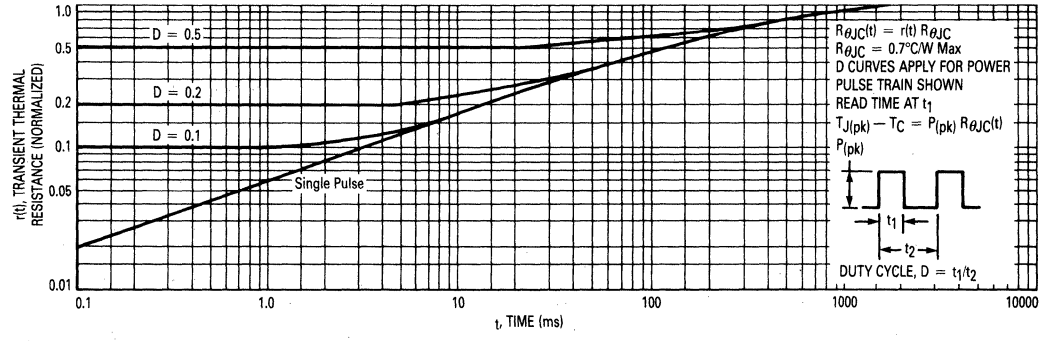


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM45N12, MTM45N15, MTM40N18, MTM40N20



SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTM45N12, MTM45N15

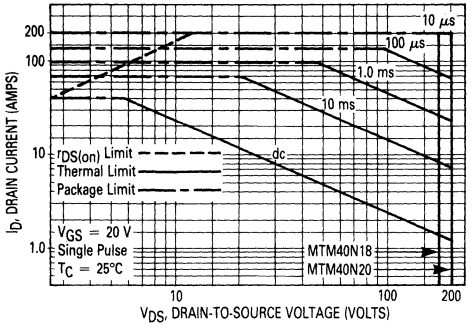


FIGURE 13 — MTM40N18, MTM40N20

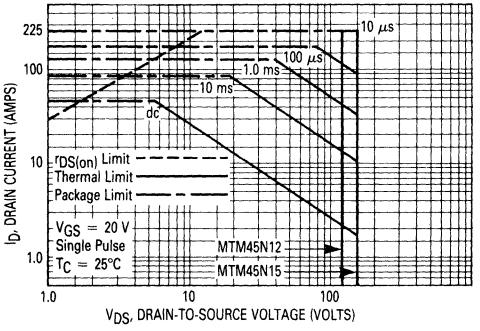
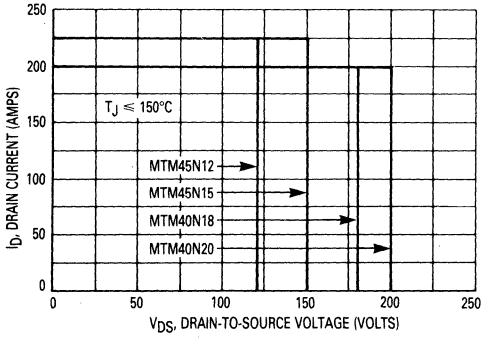


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 12 and 13
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MTM55N08
MTM55N10
MTM60N05
MTM60N06

MOTOROLA

C

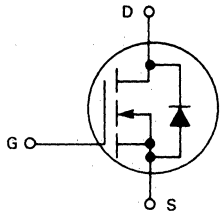
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



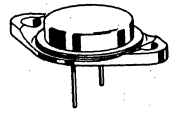
55 and 60 AMPERE

N-CHANNEL TMOS POWER FETs

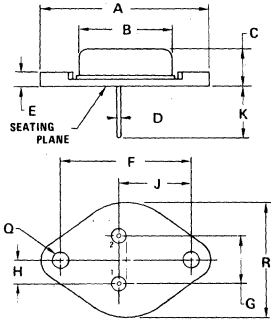
$r_{DS(on)}$ = 0.04 OHM
80 and 100 VOLTS

$r_{DS(on)}$ = 0.028 OHM
50 and 60 VOLTS

MTM55N08
MTM55N10
MTM60N05
MTM60N06



PIN 1: GATE
2: SOURCE
CASE: DRAIN



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE
(TO-3 TYPE)

MAXIMUM RATINGS

Rating	Symbol	MTM 60N05	MTM 60N06	MTM 55N08	MTM 55N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	I_D I_{DM}	60 300		55 275		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM60N05	$V_{BR(DSS)}$	50	—	Vdc
	MTM60N06		60	—	
	MTM55N08		80	—	
	MTM55N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_C = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100 °C			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 30 Adc)	MTM60N05/MTM60N06	$r_{DS(on)}$	—	0.028	Ohm
(V_{GS} = 10 Vdc, I_D = 27.5 Adc)	MTM55N08/MTM55N10		—	0.04	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 60 Adc)	MTM60N05/MTM60N06		—	1.98	
(I_D = 30 Adc, T_J = 100°C)	MTM60N05/MTM60N06		—	1.68	
(I_D = 55 Adc)	MTM55N08/MTM55N10		—	2.60	
(I_D = 27.5 Adc, T_C = 100°C)	MTM55N08/MTM55N10		—	2.20	
Forward Transconductance (V_{DS} = 15 V, I_D = 30 A)	MTM60N05/MTM60N06	g_{fs}	10	—	mhos
(V_{DS} = 15 V, I_D = 27.5 A)	MTM55N08/MTM55N10		10	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	5000	pF
Output Capacitance		C_{oss}	—	2500	
Reverse Transfer Capacitance		C_{rss}	—	1000	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 1 and 2	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	100	

SOURCE-DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.0	Vdc
Forward Turn-On Time		t_{on}	150	ns
Reverse Recovery Time		t_{rr}	200	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

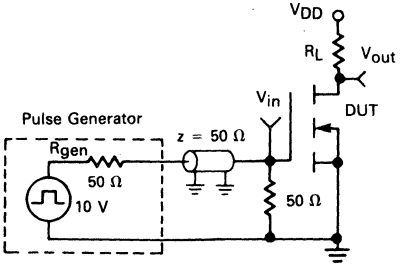
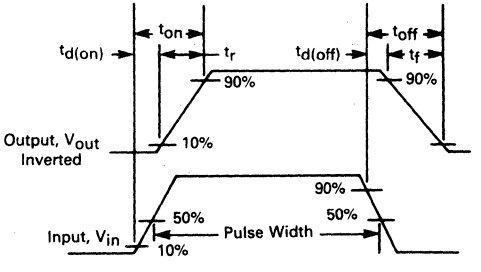


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

MTM60N05, MTM60N06

FIGURE 3 — ON-REGION CHARACTERISTICS

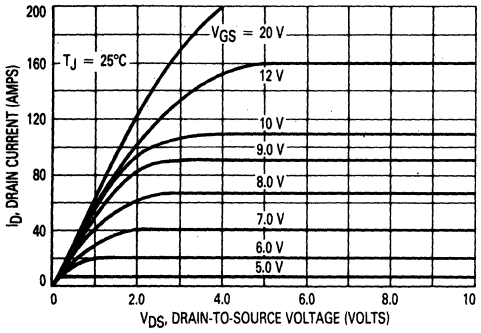


FIGURE 5 — TRANSFER CHARACTERISTICS

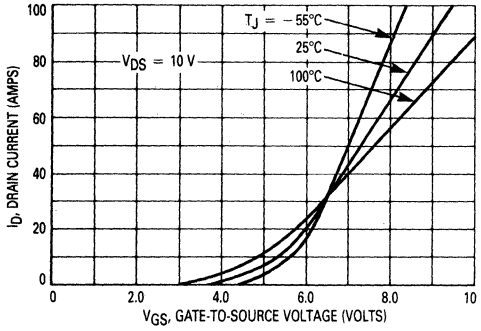
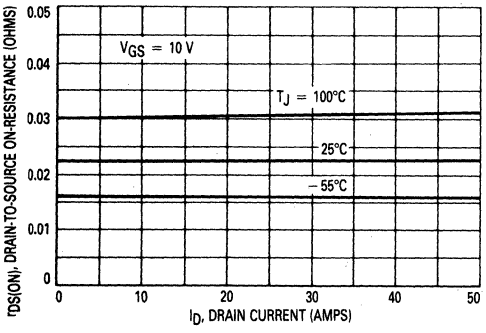


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT



MTM55N08, MTM55N10

FIGURE 4 — ON-REGION CHARACTERISTICS

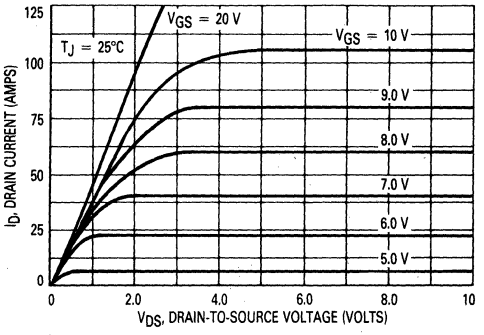


FIGURE 6 — TRANSFER CHARACTERISTICS

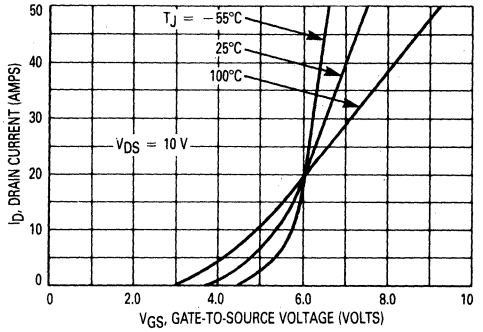
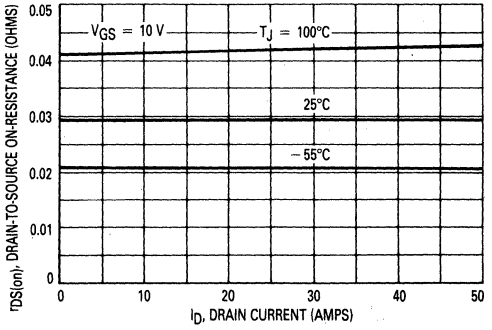


FIGURE 8 — ON-RESISTANCE versus DRAIN CURRENT



C

TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

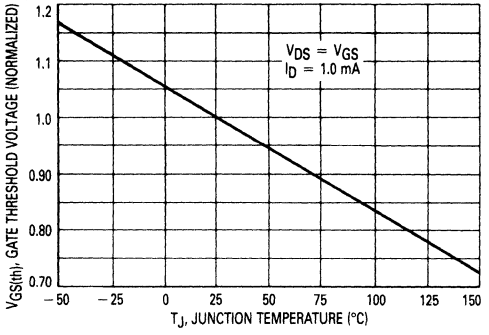
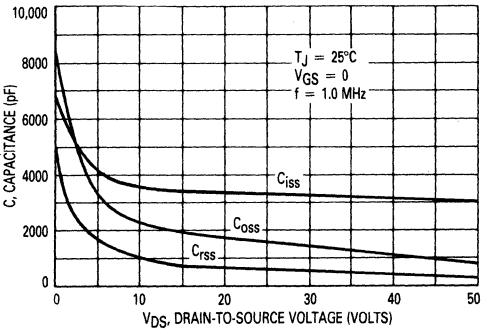
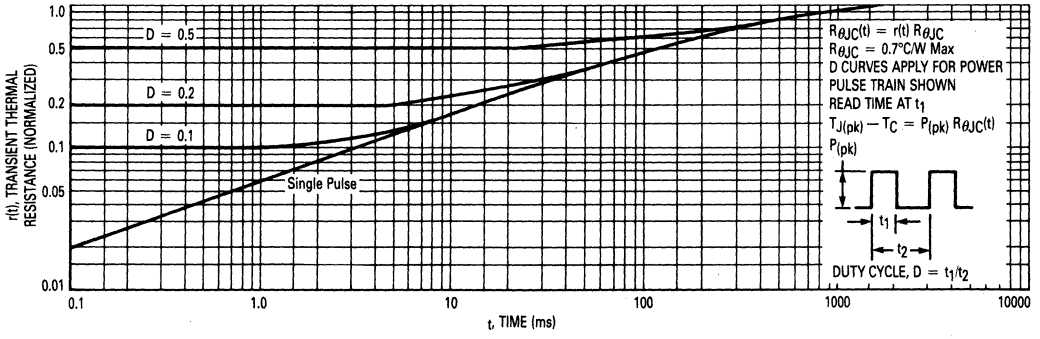


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM55N08, MTM55N10, MTM60N05, MTM60N06



C

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTM60N05, MTM60N06

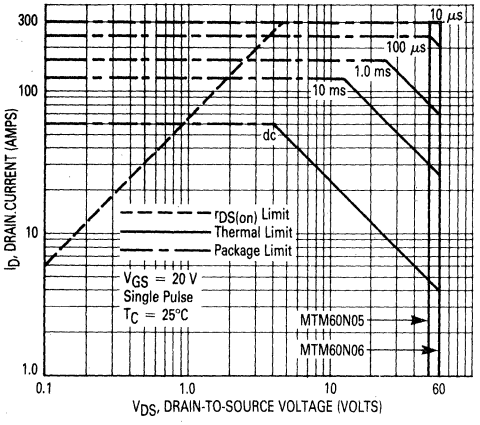
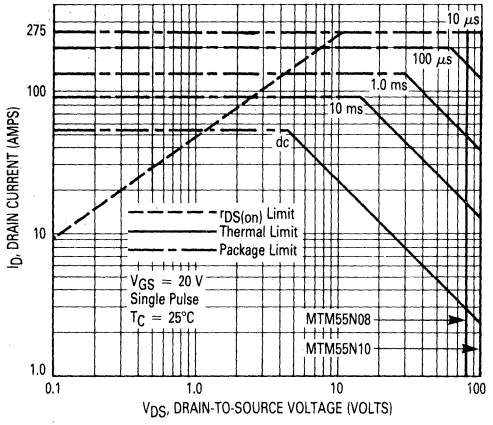


FIGURE 13 — MTM55N08, MTM55N10



FORWARD BIASED SAFE OPERATING AREA

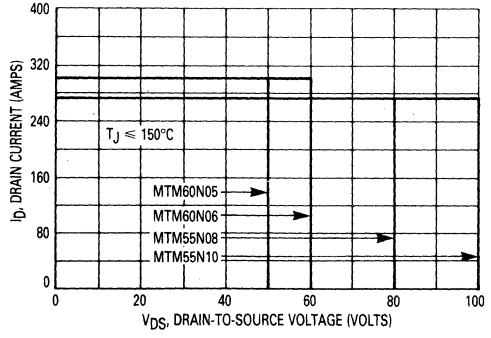
The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 12 and 13
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MOTOROLA

MTP1N45, MTP2N35
MTP1N50, MTP2N40

C

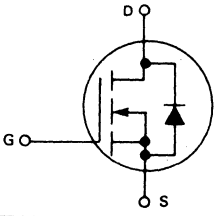
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

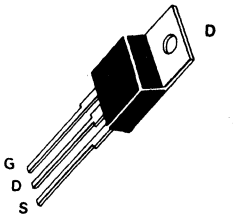


1.0 and 2.0 AMPERE

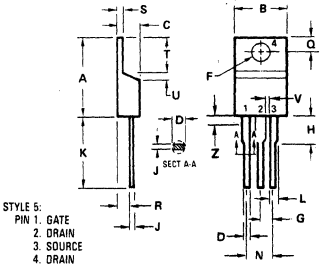
N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 8.0 OHMS
450 and 500 VOLTS

$r_{DS(on)}$ = 5.0 OHMS
350 and 400 VOLTS



MTP1N45 MTP2N35
MTP1N50 MTP2N40



NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
(TO-220AB)

MAXIMUM RATINGS

Rating	Symbol	MTP 2N35	MTP 2N40	MTP 1N45	MTP 1N50	Unit
Drain-Source Voltage	V_{DSS}	350	400	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	350	400	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous	I_D	2.0		1.0		Adc
Pulsed	I_{DM}	5.0		4.0		
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C	P_D	50				Watts
Derate above 25°C		0.4				W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	2.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTP2N35	$V_{(BR)DSS}$	350	—	Vdc
	MTP2N40		400	—	
	MTP1N45		450	—	
	MTP1N50		500	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = 0)		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	MTP2N35, MTP2N40	$r_{DS(on)}$	—	5.0	Ohms
(V_{GS} = 10 Vdc, I_D = 0.5 Adc)	MTP1N45, MTP1N50		—	8.0	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2.0 Adc)	MTP2N35, MTP2N40	$V_{DS(on)}$	—	13	Vdc
(I_D = 1.0 Adc, T_J = 100°C)			—	10	
(I_D = 1.0 Adc)	MTP1N45, MTP1N50		—	9.5	
(I_D = 0.5 Adc, T_J = 100°C)			—	8.0	
Forward Transconductance (V_{DS} = 15 V, I_D = 1.0 A)	MTP2N35, MTP2N40	g_{fs}	0.50	—	mhos
(V_{DS} = 15 V, I_D = 0.5 A)	MTP1N45, MTP1N50		0.50	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V,	C_{iss}	—	200	pF
Output Capacitance	V_{GS} = 0,	C_{oss}	—	30	pF
Reverse Transfer Capacitance	f = 1.0 MHz)	C_{rss}	—	10	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	15	ns
Turn-Off Delay Time		$t_{d(off)}$	—	35	ns
Fall Time		t_f	—	30	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0,	V_{SD}	1.0	Vdc
Forward Turn-On Time		t_{on}	30	ns
Reverse Recovery Time		t_{rr}	250	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 – SWITCHING TEST CIRCUIT

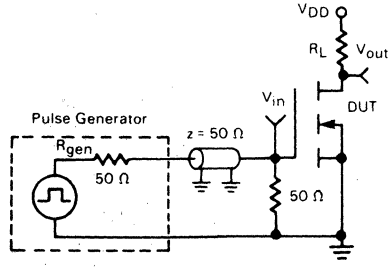
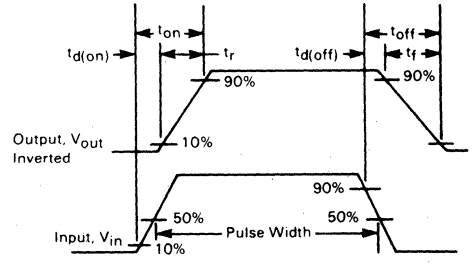


FIGURE 2 – SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTP1N45, MTP1N50

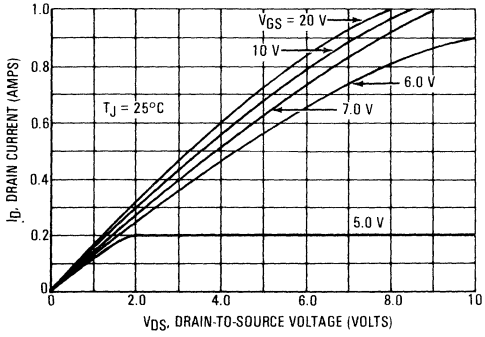
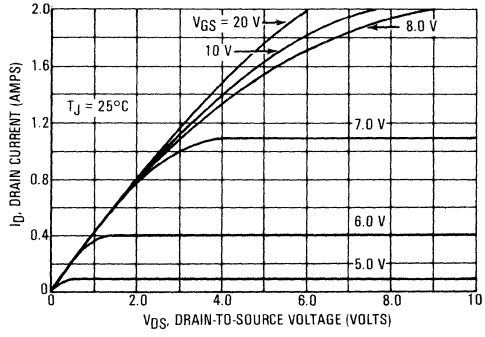


FIGURE 4 — MTP2N35, MTP2N40



TRANSFER CHARACTERISTICS

FIGURE 5 — MTP1N45, MTP1N50

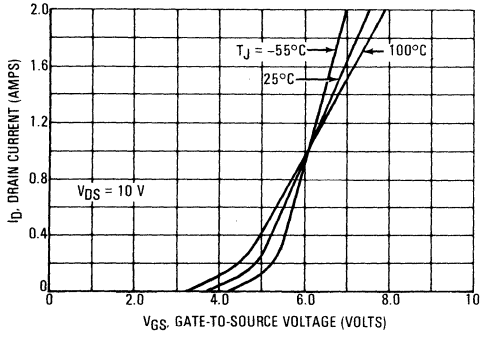
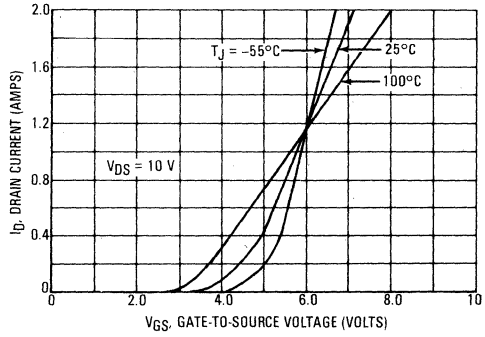


FIGURE 6 — MTP2N35, MTP2N40



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTP1N45, MTP1N50

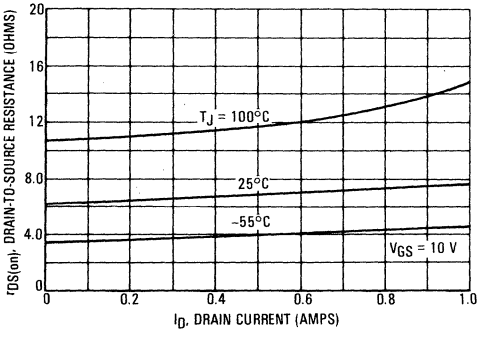
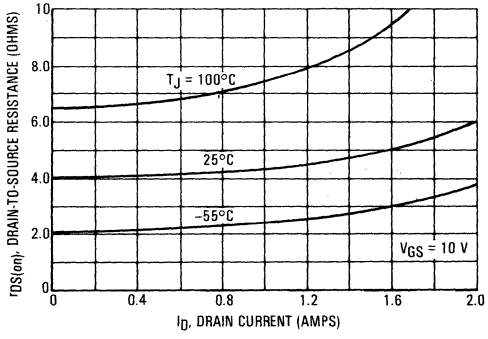


FIGURE 8 — MTP2N35, MTP2N40



C

TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

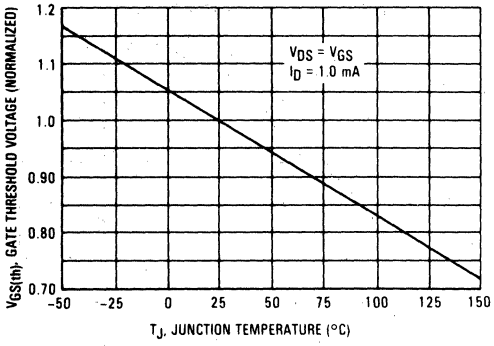


FIGURE 10 — CAPACITANCE VARIATION

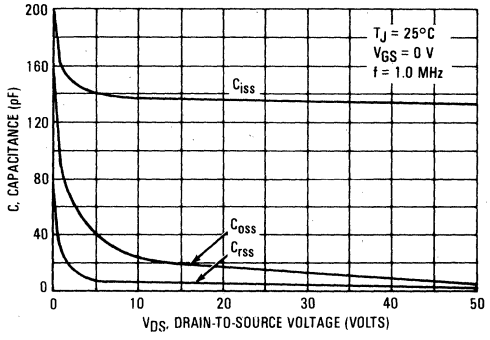
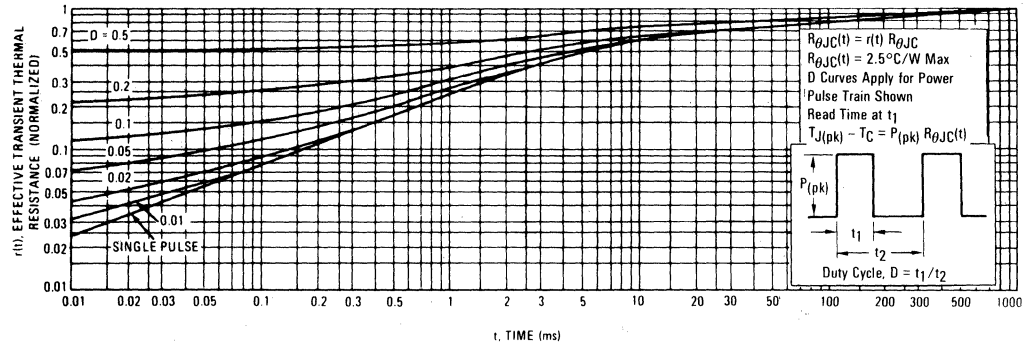


FIGURE 11 — THERMAL RESPONSE
MTP1N45, MTP1N50, MTP2N35 AND MTP2N40



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 0.5 Amp. (See Figures 5 and 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTP1N45, MTP1N50

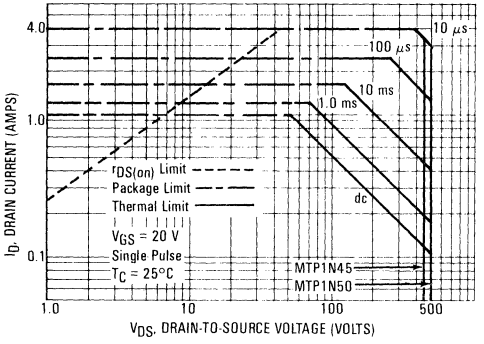
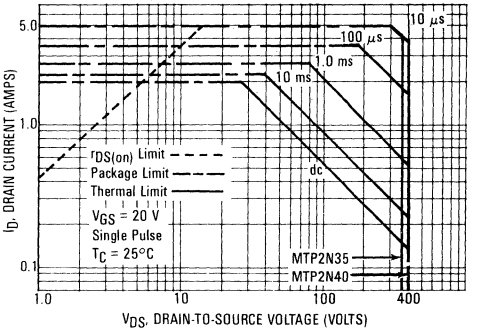


FIGURE 13 — MTP2N35, MTP2N40



FORWARD BIASED SAFE OPERATING AREA

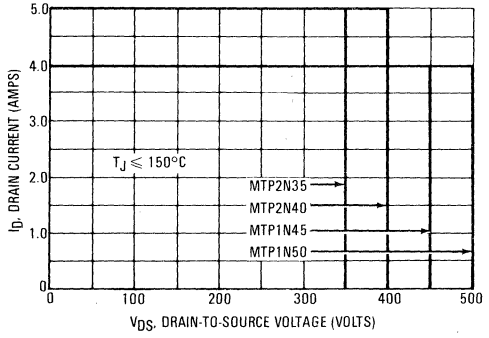
The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

Where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 12 and 13
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MTP1N55, MTP1N60

MOTOROLA

C

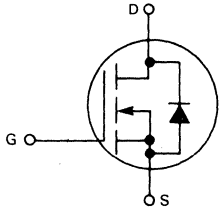
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$ $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

TMOS™

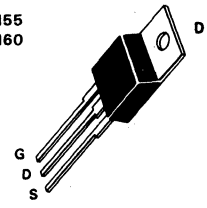


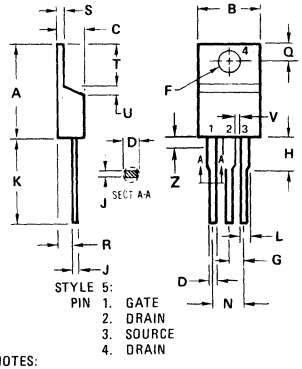
1.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 12 Ω
550 and 600 VOLTS

MTP1N55
MTP1N60





STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONS L AND H APPLIES TO ALL LEADS.
2. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-
Z	—	2.03	—	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP1N55	MTP1N60	Unit
Drain — Source Voltage	V_{DSS}	550	600	Vdc
Drain — Gate Voltage R_{GS} = 1 MΩ	V_{DGR}	550	600	Vdc
Gate — Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 1.0 3.0		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.4		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	2.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTP1N55 MTP1N60	$V_{(BR)DSS}$	550 600	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 0.5 Adc) (I_D = 1.0 Adc) (I_D = 0.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— — —	6.0 16 12	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$r_{DS(on)}$	—	12	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 0.5 A)		g_{fs}	0.5	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	200	pF
Output Capacitance		C_{oss}	—	30	
Reverse Transfer Capacitance		C_{rss}	—	10	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	35	
Fall Time		t_f	—	30	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 1.0 A V_{GS} = 0	V_{SD}	1.0	Vdc
Forward Turn-On Time		t_{on}	30	ns
Reverse Recovery Time		t_{rr}	250	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

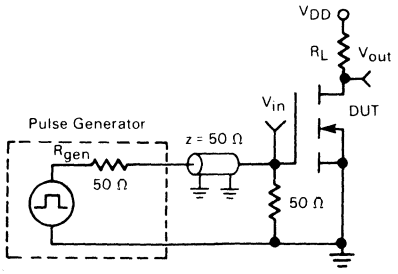
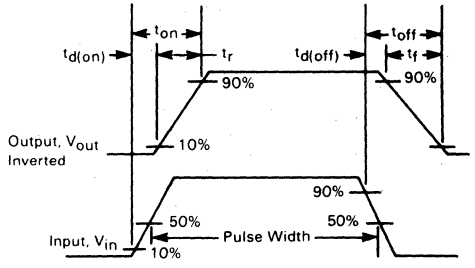


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

FIGURE 3 — ON-REGION CHARACTERISTICS

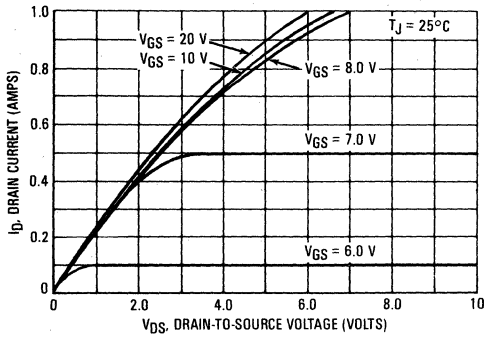


FIGURE 4 — TRANSFER CHARACTERISTICS

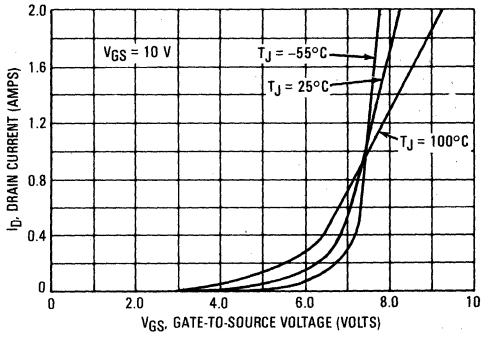


FIGURE 5 — ON-RESISTANCE VARIATION

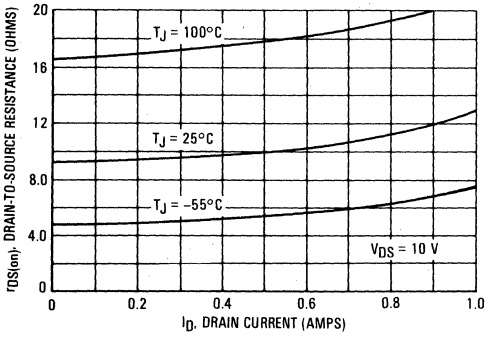


FIGURE 6 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

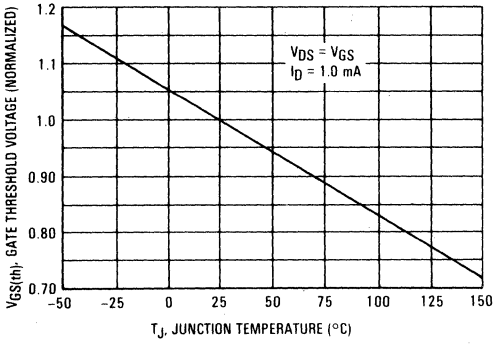


FIGURE 7 — ON-VOLTAGE VARIATION

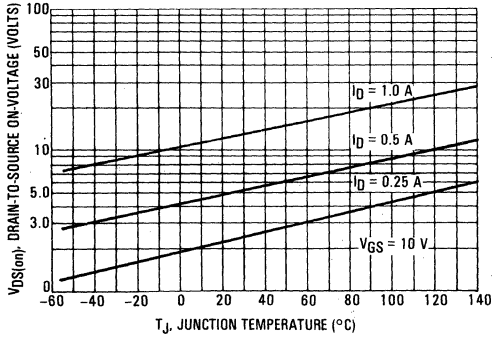
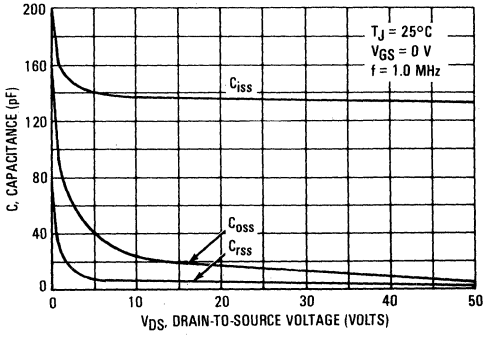


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

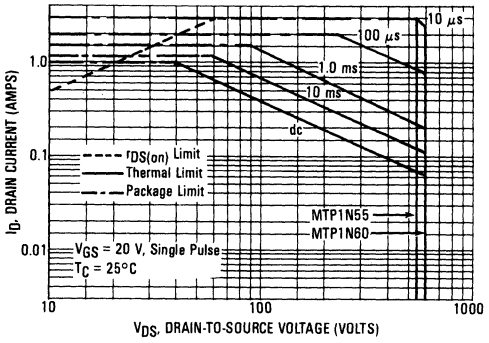
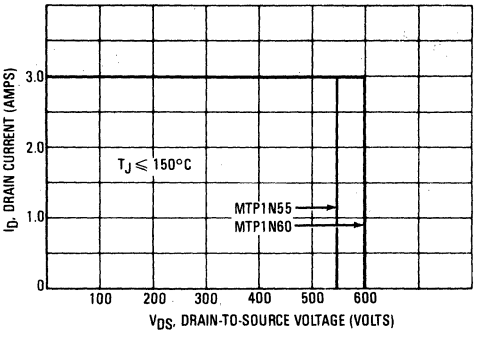


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}$$

Where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11.

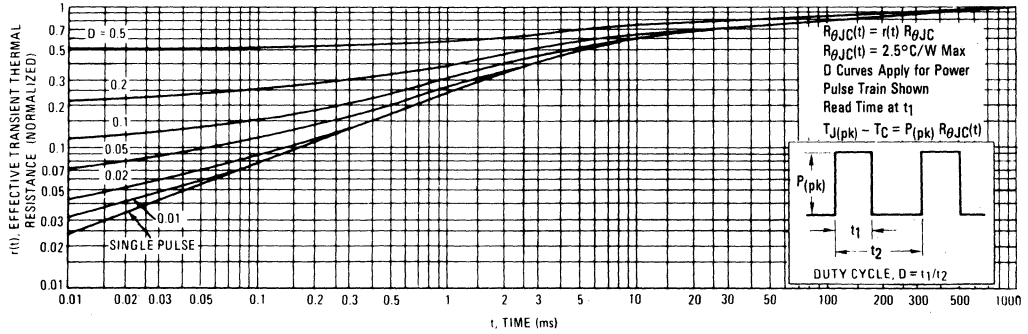
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

FIGURE 11 — THERMAL RESPONSE



MTP2N18, MTP2N20
MTP3N12, MTP3N15

MOTOROLA

C

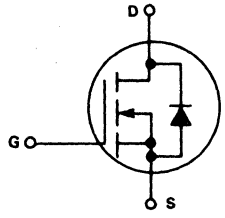
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

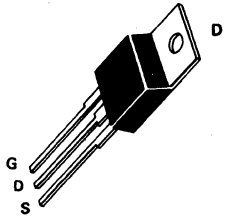
TMOS™



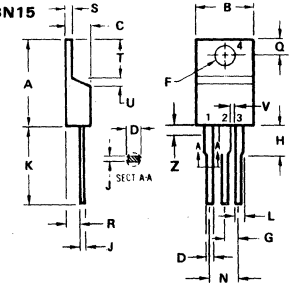
2.0 and 3.0 AMPERE
N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 1.8 OHMS
180 and 200 VOLTS

$r_{DS(on)}$ = 1.3 OHMS
120 and 150 VOLTS



MTP2N18
MTP2N20
MTP3N12
MTP3N15



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.75	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—
Z	—	2.03	—	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 3N12	MTP 3N15	MTP 2N18	MTP 2N20	Unit
Drain-Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 3.0 7.0		 2.0 6.0		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	2.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTP3N12	$V_{(BR)DSS}$	120	—	Vdc
	MTP3N15		150	—	
	MTP2N18		180	—	
	MTP2N20		200	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = 0)		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)	MTP3N12, MTP3N15	$r_{DS(on)}$	—	1.3	Ohms
(V_{GS} = 10 Vdc, I_D = 1.0 Adc)	MTP2N18, MTP2N20		—	1.8	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3.0 Adc)	MTP3N12, MTP3N15	$V_{DS(on)}$	—	5.1	Vdc
(I_D = 1.5 Adc, T_J = 100°C)			—	3.9	
(I_D = 2.0 Adc)	MTP2N18, MTP2N20		—	4.4	
(I_D = 1.0 Adc, T_J = 100°C)			—	3.6	
Forward Transconductance (V_{DS} = 15 V, I_D = 1.5 A)	MTP3N12, MTP3N15	g_{fs}	0.75	—	mhos
(V_{DS} = 15 V, I_D = 1.0 A)	MTP2N18, MTP2N20		0.50	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V,	C_{iss}	—	250	pF
Output Capacitance	V_{GS} = 0,	C_{oss}	—	150	pF
Reverse Transfer Capacitance	f = 1.0 MHz)	C_{rss}	—	25	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	30	ns
Turn-Off Delay Time		$t_{d(off)}$	—	30	ns
Fall Time		t_f	—	15	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0,	V_{SD}	2.5	Vdc
Forward Turn-On Time		t_{on}	150	ns
Reverse Recovery Time		t_{rr}	250	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

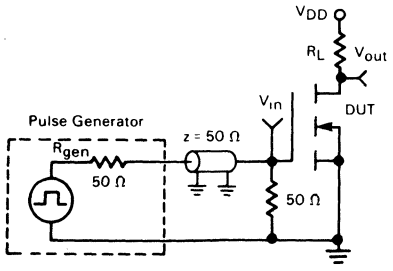
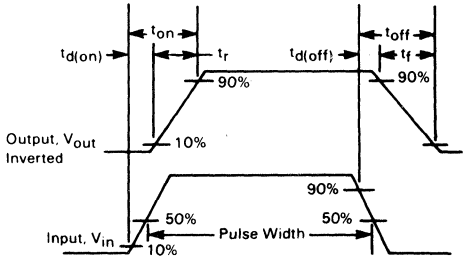


FIGURE 2 — SWITCHING WAVEFORMS



C

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTP2N18, MTP2N20

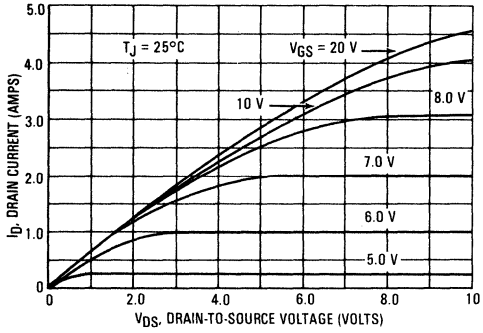
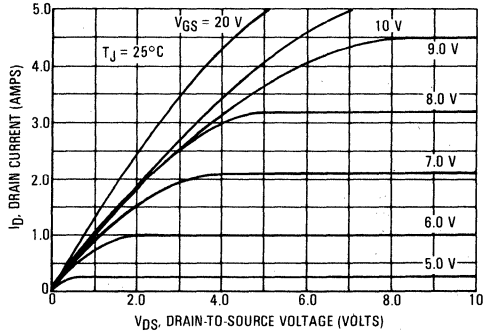


FIGURE 4 — MTP3N12, MTP3N15



TRANSFER CHARACTERISTICS

FIGURE 5 — MTP2N18, MTP2N20

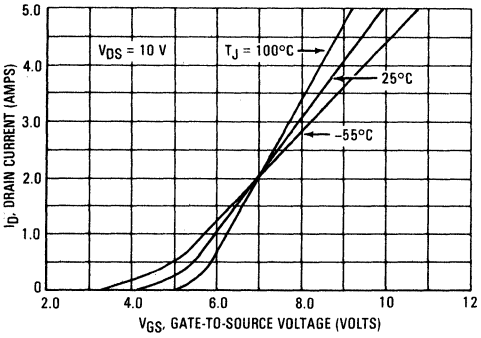
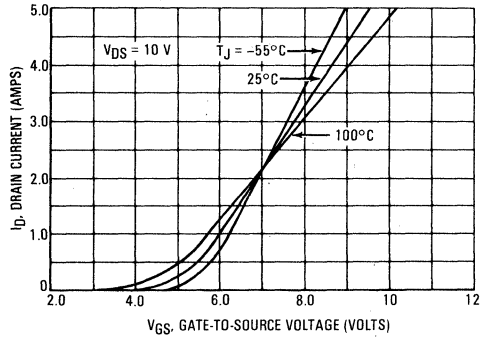


FIGURE 6 — MTP3N12, MTP3N15



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTP2N18, MTP2N20

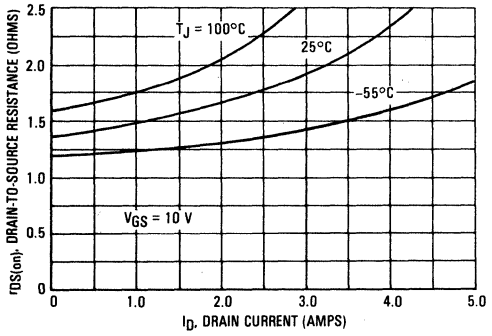
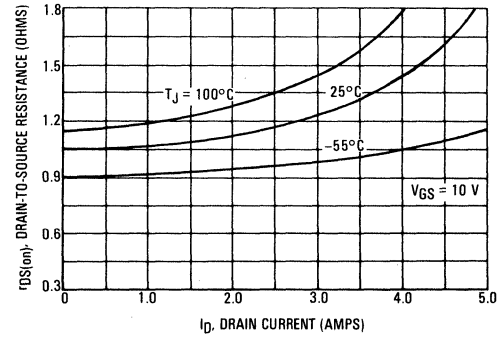


FIGURE 8 — MTP3N12, MTP3N15



TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

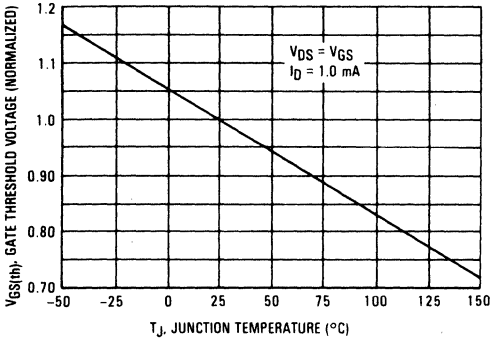


FIGURE 10 — CAPACITANCE VARIATION

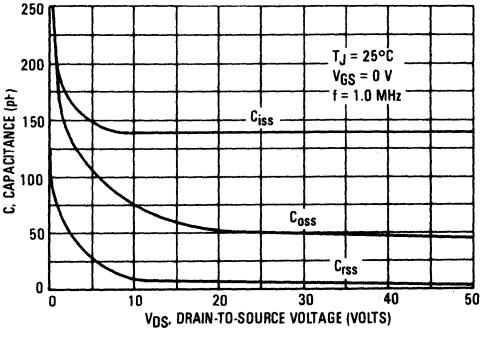
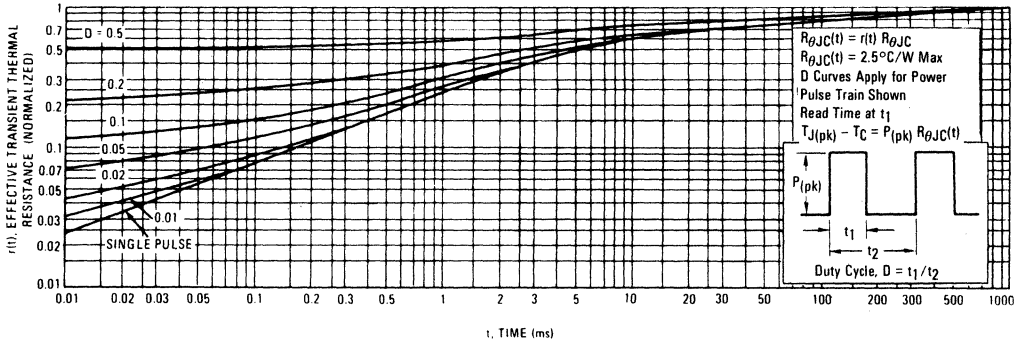


FIGURE 11 — THERMAL RESPONSE
MTP2N18, MTP2N20, MTP3N12 AND MTP3N15



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 0.5 Amp. (See Figures 5 and 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

C

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTP2N18, MTP2N20

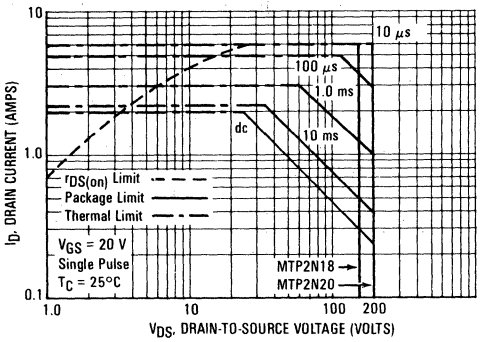
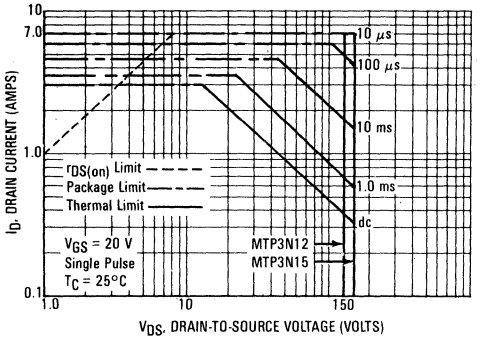


FIGURE 13 — MTP3N12, MTP3N15



FORWARD BIASED SAFE OPERATING AREA

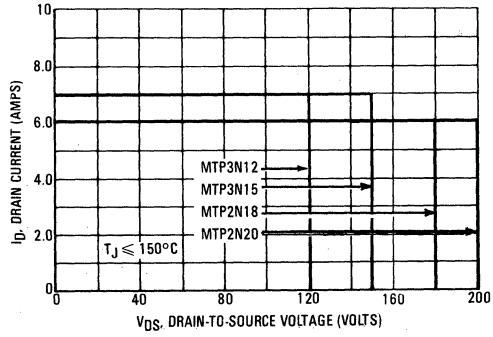
The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 12 and 13.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figure 11.

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14 is the boundary that the load line may traverse without incurring damage to the MOSFET. The Fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MOTOROLA

MTP4N08, MTP5N05
MTP4N10, MTP5N06

C

Designer's Data Sheet

4.0 and 5.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.8 OHM
80 and 100 VOLTS

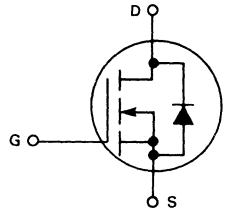
$r_{DS(on)}$ = 0.6 OHM
50 and 60 VOLTS

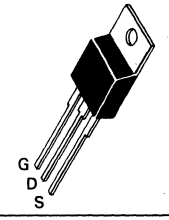
N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

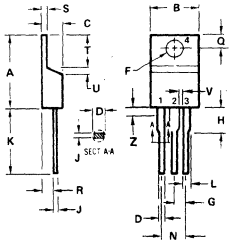
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™





MTP4N08
MTP4N10
MTP5N05
MTP5N06



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.78	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-
Z	—	2.03	—	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 5N05	MTP 5N06	MTP 4N08	MTP 4N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 5.0 10		 4.0 9.0		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	2.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTP5N05	$V_{(BR)DSS}$	50	—	Vdc
	MTP5N06		60	—	
	MTP4N08		80	—	
	MTP4N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	MTP5N05, MTP5N06	$r_{DS(on)}$	—	0.6	Ohms
(V_{GS} = 10 Vdc, I_D = 2.0 Adc)	MTP4N08/MTP4N10		—	0.8	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 5.0 Adc)	MTP5N05/MTP5N06		—	3.75	
(I_D = 2.5 Adc, T_J = 100°C)			—	3.0	
(I_D = 4.0 Adc)	MTP4N08, MTP4N10		—	4.8	
(I_D = 2.0 Adc, T_J = 100°C)			—	3.2	
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)	MTP5N05/MTP5N06	g_{fs}	0.75	—	mhos
(V_{DS} = 15 V, I_D = 2.0 A)	MTP4N08/MTP4N10		0.75	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	300	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	—	250	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	—	60	pF

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms, See Figures 1 and 2)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	80	
Turn-Off Delay Time		$t_{d(off)}$	—	30	
Fall Time		t_f	—	30	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0,	V_{SD}	2.5	Vdc
Forward Turn-On Time		t_{on}	150	ns
Reverse Recovery Time		t_{rr}	250	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 1 — SWITCHING TEST CIRCUIT

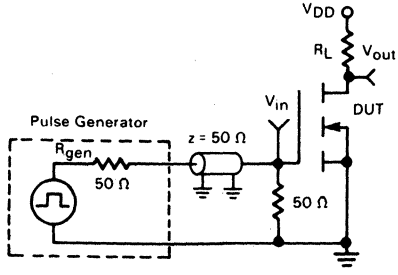
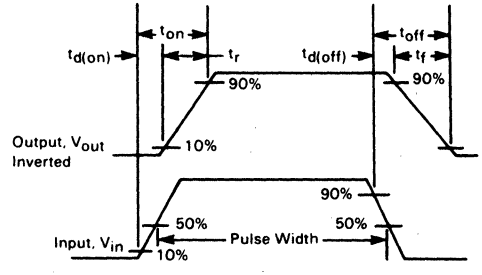


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTP4N08, MTP4N10

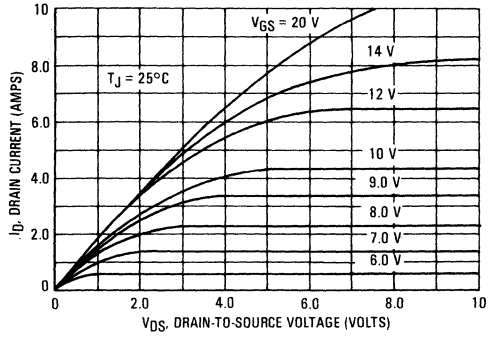
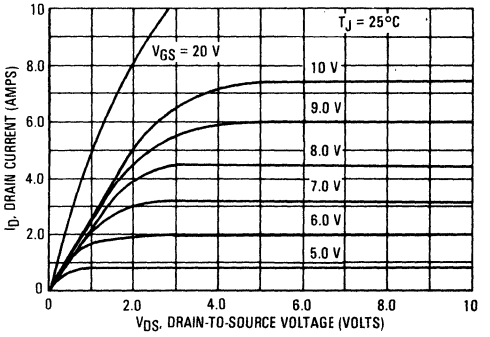


FIGURE 4 — MTP5N05, MTP5N06



TRANSFER CHARACTERISTICS

FIGURE 5 — MTP4N08, MTP4N10

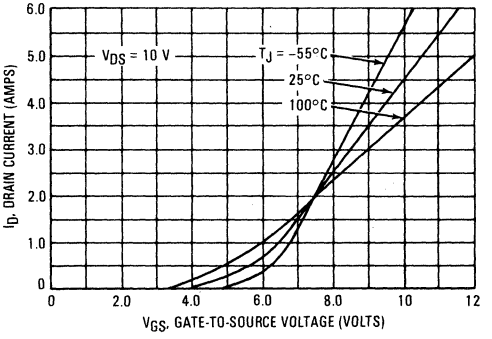
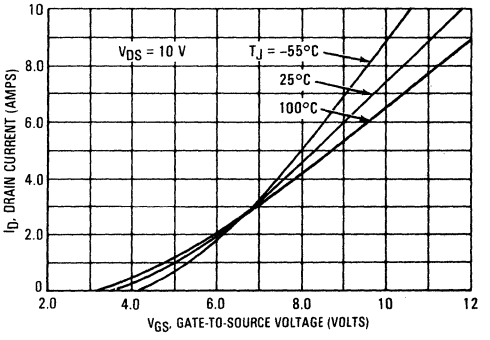


FIGURE 6 — MTP5N05, MTP5N06



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTP4N08, MTP4N10

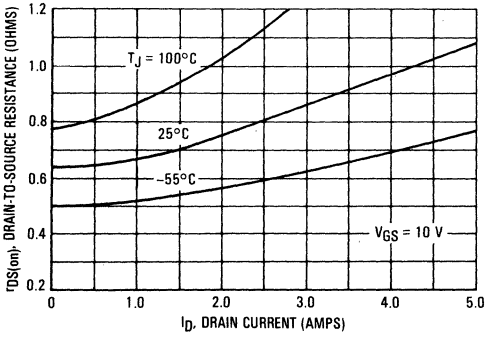
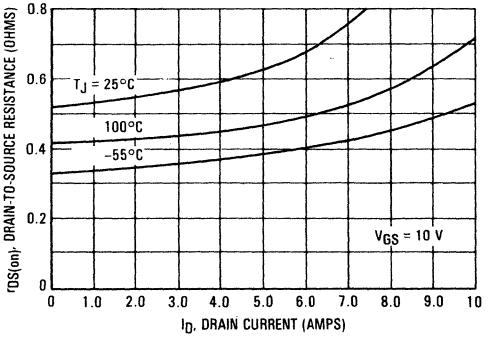


FIGURE 8 — MTP5N05, MTP5N06



C

TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

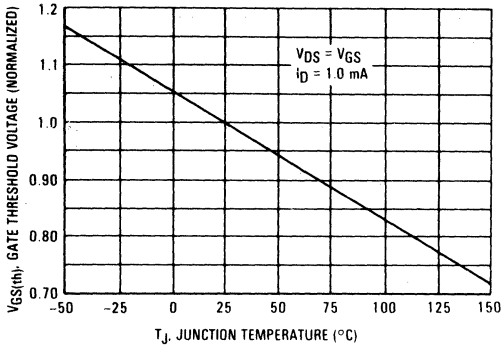


FIGURE 10 — CAPACITANCE VARIATION

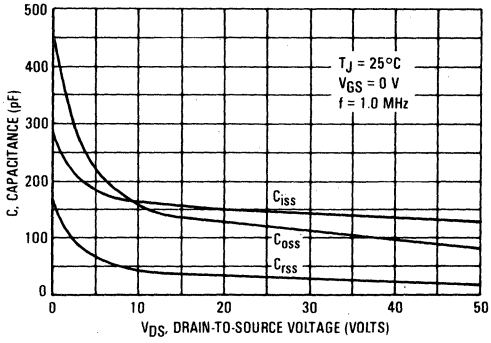
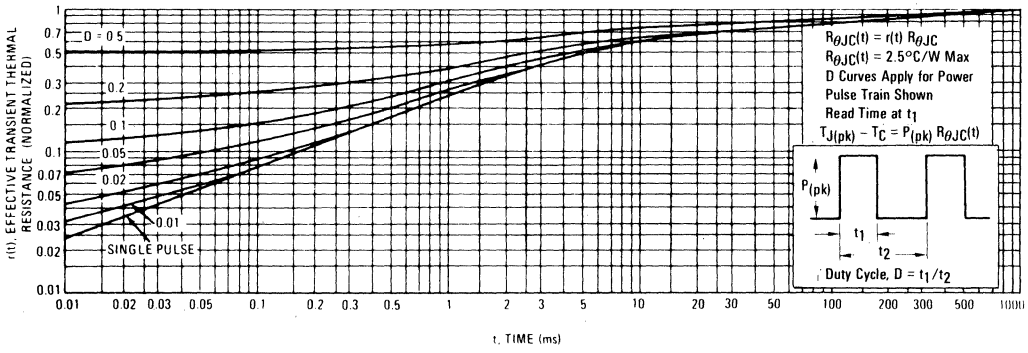


FIGURE 11 — THERMAL RESPONSE



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 0.5 Amp. (See Figures 5 and 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTP4N08, MTP4N10

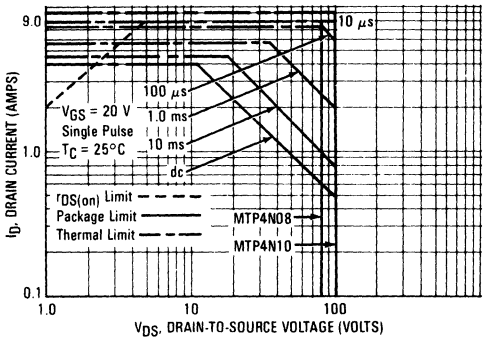
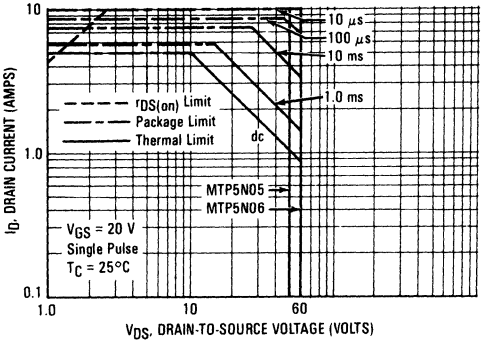


FIGURE 13 — MTP5N05, MTP5N06



FORWARD BIASED SAFE OPERATING AREA

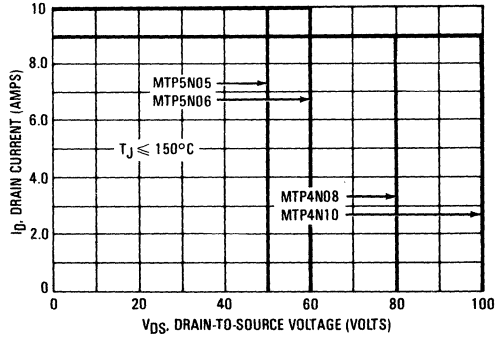
The dc data of Figures 12 and 13 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

Where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 12 and 13
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11

FIGURE 14 — MTP4N08, MTP4N10



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

C

Data sheets are arranged in alphanumeric sequence except when information applies to more than one device, e.g., MFE930, MFE960 and MFE990. Consult the table of contents for these part numbers.

Small-Signal Data Sheets

2N6660 MPF6660
2N6661 MPF6661

MOTOROLA

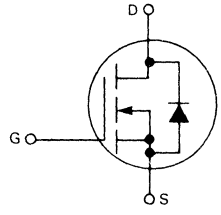
D

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

These TMOS FETs are designed for high-speed switching applications such as switching power supplies, CMOS logic, microprocessor or TTL-to-high current interface and line drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 5.0$ ns Max
- Low On-Resistance — 2.0 Ohm Typ — 2N6660/2N6661
  — MPF6660/MPF6661
- Low Drive Requirement, $V_{GS(th)} = 2.0$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

TMOS™

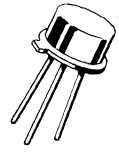


2.0 AMPERE

N-CHANNEL TMOS FET

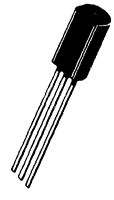
60, 90 VOLTS

2N6660
2N6661



CASE 79-02
TO-205AD
(TO-39)

MPF6660
MPF6661



CASE 29-03
TO-226AE

MAXIMUM RATINGS

Rating	Symbol	2N6660 MPF6660	2N6661 MPF6661	Unit
Drain-Source Voltage	V_{DSS}	60	90	Vdc
Drain-Gate Voltage	V_{DGO}	60	90	Vdc
Gate-Source Voltage	V_{GS}	± 30		Vdc
Drain Current — Continuous (1)	I_D	2.0		Adc
Pulsed (2)	I_{DM}	3.0		
		2N6660 2N6661	**MPF6660 MPF6661**	
Total Power Dissipation @ $T_C = 25°C$	P_D	6.25	2.5	Watts
Derate above 25°C		50	20	mW/°C
Total Power Dissipation @ $T_A = 25°C$	P_D	—	1.0	Watts
Derate above 25°C		—	8.0	mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150		°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs Duty Cycle ≤ 2.0%

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSS}$				Vdc
2N6660, MPF6660		60	—	—	
2N6661, MPF6661		90	—	—	
Zero Gate Voltage Drain Current (V_{DS} = Maximum Rating, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 V, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	0.8	1.4	2.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 1.0 A)	$V_{DS(on)}$				Vdc
2N6660, MPF6660		—	—	3.0	
2N6661, MPF6661		—	—	4.0	
(V_{GS} = 5.0 V, I_D = 0.3 A)					
2N6660, MPF6660		—	0.9	1.5	
2N6661, MPF6661		—	0.9	1.6	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$r_{DS(on)}$				Ohms
2N6660, MPF6660		—	—	3.0	
2N6661, MPF6661		—	—	4.0	
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	$I_{D(on)}$	1.0	2.0	—	Amps
Forward Transconductance (V_{DS} = 25 V, I_D = 0.5 A)	g_{fs}	170	—	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	30	50	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	20	40	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	3.6	10	pF
SWITCHING CHARACTERISTICS*					
Turn-On Time (See Figure 1)	t_{on}	—	—	5.0	ns
Turn-Off Time (See Figure 1)	t_{off}	—	—	5.0	ns
Rise Time	t_r	—	—	5.0	ns
Fall Time	t_f	—	—	5.0	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

D

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

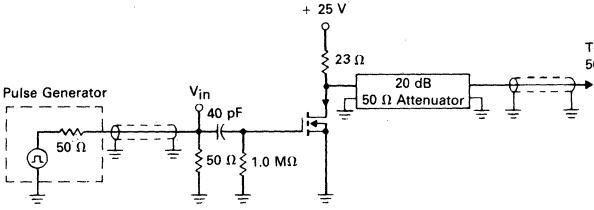
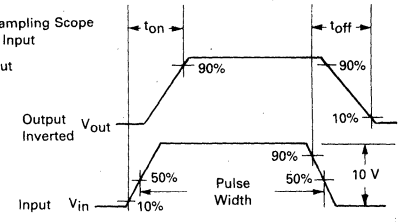


FIGURE 2 — SWITCHING WAVEFORMS



D

FIGURE 3 — $V_{GS(th)}$ NORMALIZED versus TEMPERATURE

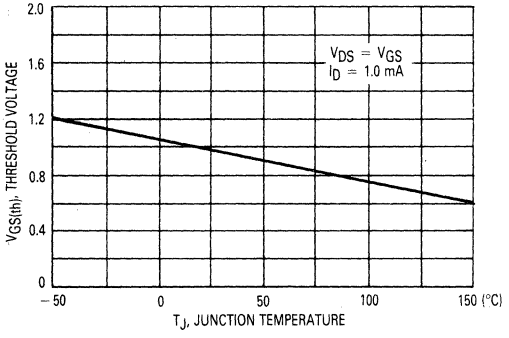


FIGURE 4 — ON-REGION CHARACTERISTICS

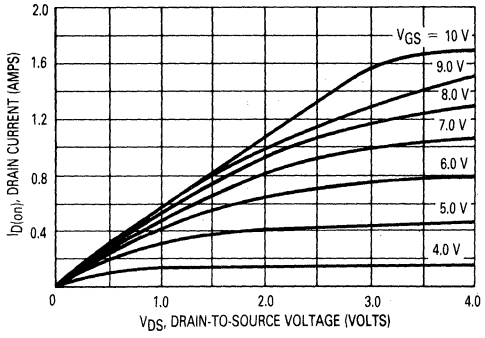


FIGURE 5 — OUTPUT CHARACTERISTICS

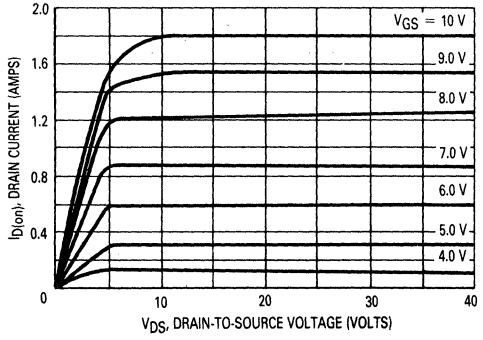


FIGURE 6 — CAPACITANCE versus DRAIN-TO-SOURCE VOLTAGE

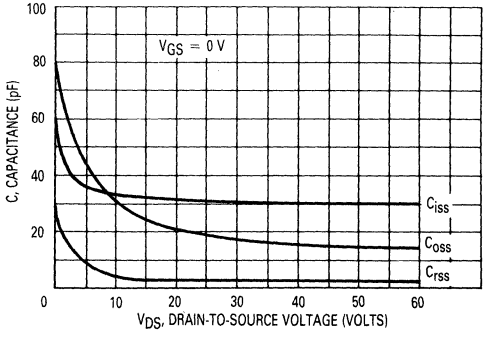
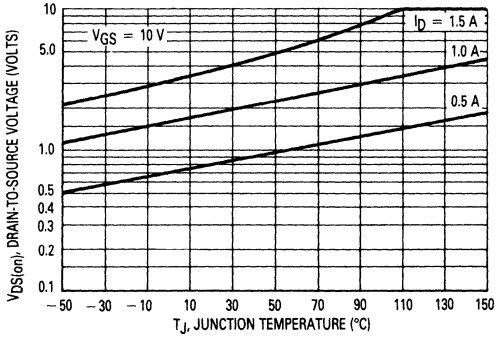
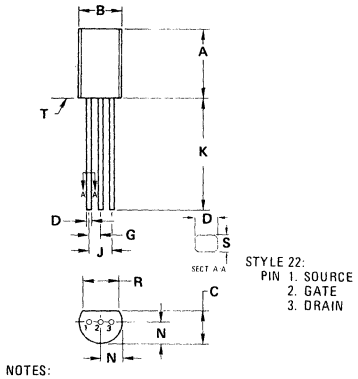


FIGURE 7 — ON-VOLTAGE versus TEMPERATURE



D

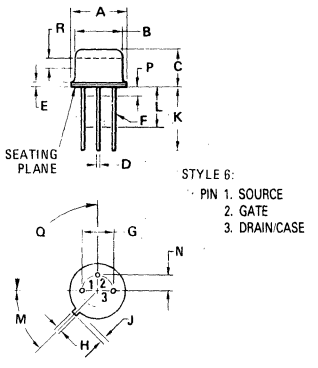
OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ Ø 0.10 (0.004) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.37	7.87	0.290	0.310
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.46	0.61	0.018	0.024
G	1.27 BSC		0.050 BSC	
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
N	2.03	2.92	0.080	0.115
R	3.43	–	0.135	–
S	0.46	0.61	0.018	0.024

CASE 29-03
TO-226AE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-205AD
(TO-39)

BS107
BS107A

MOTOROLA

Advance Information

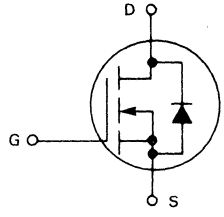
D

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS FIELD EFFECT TRANSISTOR

This TMOS FET is designed for high voltage, high speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL to high voltage interface and high voltage display drivers.

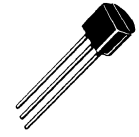
- Fast Switching Speed — $t_{on} = t_{off}$ 6 ns typ
- Low On-Resistance — 4.5 Ohms typ (BS107A)
- Low Drive Requirement, $V_{GS(th)}$ 3.0 V max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

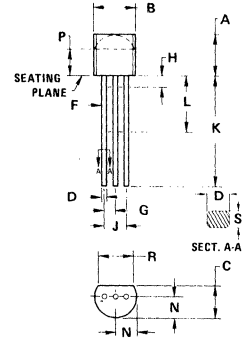
TMOS™



200 VOLTS

N-CHANNEL TMOS FET





STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.67	0.080	0.105
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
(TO-226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	200	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous(1) Pulsed(2)	 I_D I_{DM}	 250 500	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	0.6	Watts
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−55 to 150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero-Gate-Voltage Drain Current (V_{DS} = 130 V, V_{GS} = 0)	I_{DSS}	—	—	30	nAdc
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSX}$	200	—	—	Vdc
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0)	I_{GSS}	—	0.01	10	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})	$V_{GS(Th)}$	1.0	—	3.0	Vdc
Static Drain-Source On Resistance	$r_{DS(on)}$				Ohms
BS107					
(V_{GS} = 2.6 V, I_D = 20 mA)					
(V_{GS} = 10 V, I_D = 200 mA)		—	—	28	
BS107A		—	—	14	
(V_{GS} = 10 Vdc)					
(I_D = 100 mA)		—	4.5	6.0	
(I_D = 250 mA)		—	4.8	6.4	
SMALL-SIGNAL CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	72	90	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.8	3.5	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	15	20	pF
Forward Transconductance (V_{DS} = 25 V, I_D = 250 mA)	g_{fs}	200	400	—	mmhos
SWITCHING CHARACTERISTICS					
Turn-On Time	t_{on}	—	6.0	15	ns
Turn-Off Time	t_{off}	—	12	15	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

D

BS170

MOTOROLA

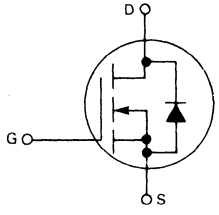
D

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL-to-high voltage interface and high voltage display drivers.

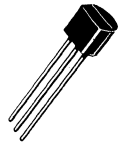
- Fast Switching Speed — $t_{on} = t_{off} = 6.0$ ns Typ
- Low On-Resistance — 5.0 Ohms Max
- Low Drive Requirement, $V_{GS(th)} = 3.0$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

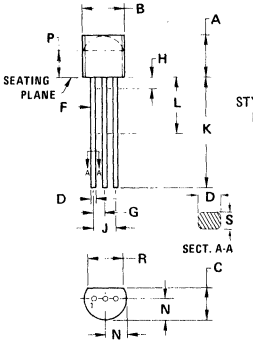
TMOS™



60 VOLTS

N-CHANNEL TMOS FET





NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70 mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70 mm (0.5") FROM SEATING PLANE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.67	0.080	0.105
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-226AA
(TO-92)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous (1)	I_D	0.5	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	0.83	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 μA)	$V_{(BR)DSS}$	60	90	—	Vdc
Gate-Body Leakage Current (V_{GS} = 15 V, V_{DS} = 0)	I_{GSS}	—	0.01	10	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	0.8	2.0	3.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 0 V)	$I_{D(off)}$	—	—	0.5	μA
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 200 mA)	$r_{DS(on)}$	—	1.8	5.0	Ohms
Forward Transconductance (V_{DS} = 10 V, I_D = 250 mA)	g_{fs}	—	200	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	60	—	pF
SWITCHING CHARACTERISTICS*					
Turn-On Time (I_D = 0.2 A) See Figure 1	t_{on}	—	4.0	10	ns
Turn-Off Time (I_D = 0.2 A) See Figure 1	t_{off}	—	4.0	10	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

D

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

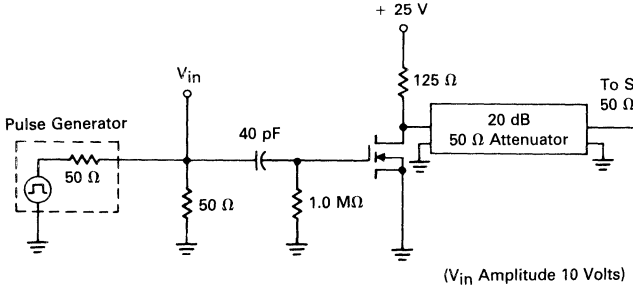
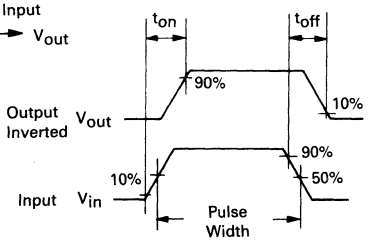


FIGURE 2 — SWITCHING WAVEFORMS



D

FIGURE 3 — $V_{GS(th)}$ NORMALIZED versus TEMPERATURE

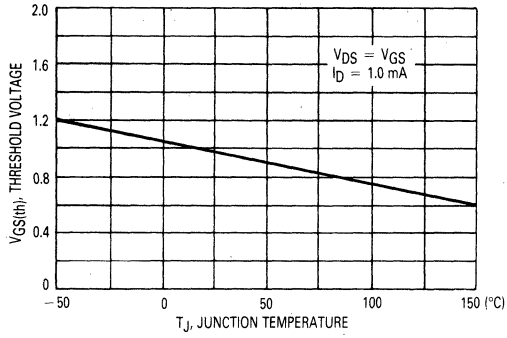


FIGURE 4 — ON-REGION CHARACTERISTICS

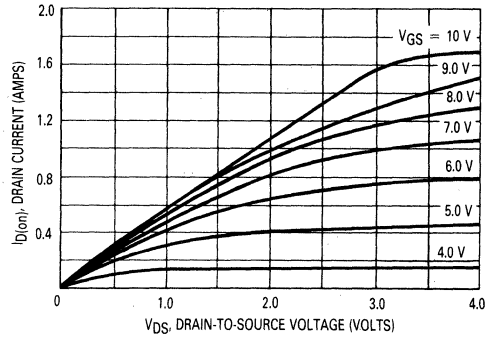


FIGURE 5 — OUTPUT CHARACTERISTICS

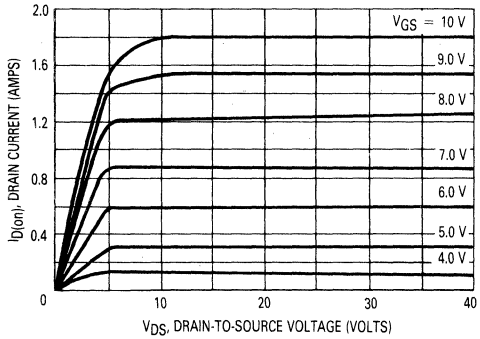
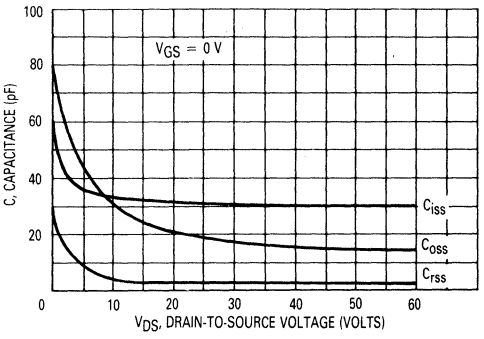


FIGURE 6 — CAPACITANCE versus DRAIN-TO-SOURCE VOLTAGE



MOTOROLA

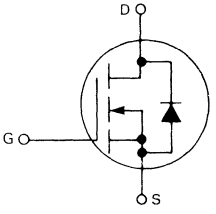
MFE910
MPF910

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor of TTL-to-high voltage interface and high voltage display drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 6.0$ ns Typ
- Low On-Resistance — 2.0 Ohms Typ
- Low Drive Requirement, $V_{GS(th)} = 2.5$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

TMOS™

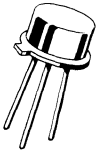


60 VOLTS

N-CHANNEL TMOS FET

D

MFE910



CASE 79-02
TO-205AD
(TO-39)

MPF910

CASE 29-03
TO-226AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Gate-Source Voltage	V_{GS}	±15	Vdc
Drain Current — Continuous (1) Pulsed (2)	I_D I_{DM}	0.5 1.0	Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C MFE910	P_D	6.25 50	Watts mW/°C
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C MPF910	P_D	1.0 8.0	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 μA)	$V_{(BR)DSS}$	60	90	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 40 V, V_{GS} = 0)	I_{DSS}	—	0.1	10	μAdc
Gate-Body Leakage Current (V_{GS} = 10 V, V_{DS} = 0)	I_{GSS}	—	0.01	10	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	0.3	1.5	2.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 500 mA)	$V_{DS(on)}$	—	—	2.5	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	$I_{D(on)}$	500	—	—	mA
Forward Transconductance (V_{DS} = 15 V, I_D = 500 mA)	g_{fs}	100	—	—	mmhos

D

FIGURE 1 — $V_{GS(th)}$ NORMALIZED versus TEMPERATURE

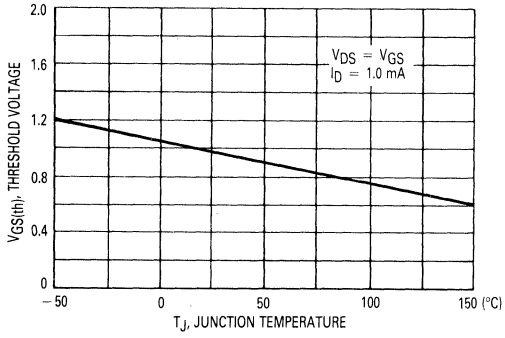


FIGURE 2 — ON-REGION CHARACTERISTICS

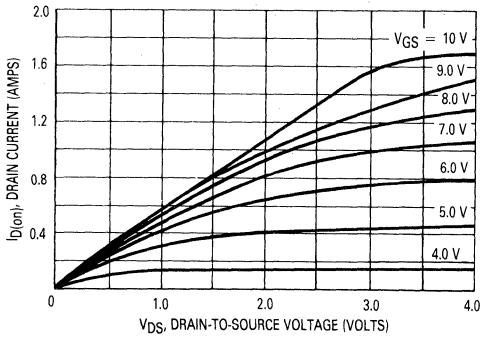


FIGURE 3 — OUTPUT CHARACTERISTICS

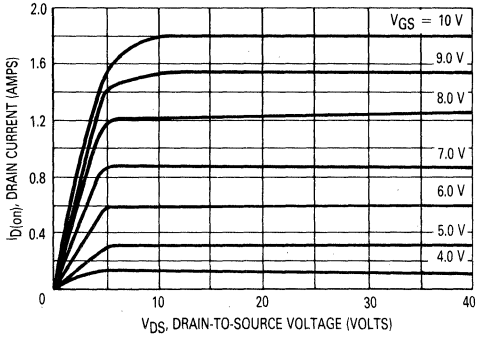
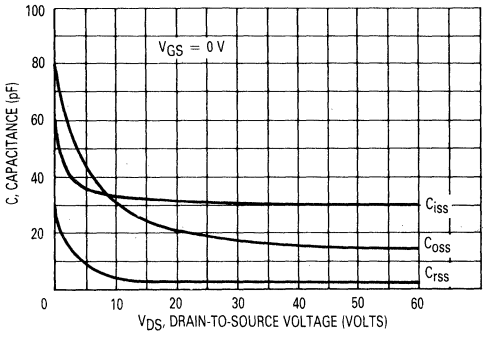
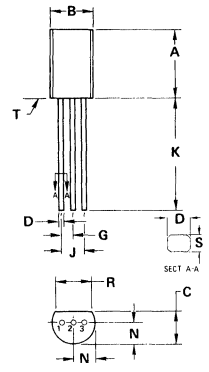


FIGURE 4 — CAPACITANCE versus DRAIN-TO-SOURCE VOLTAGE



OUTLINE DIMENSIONS

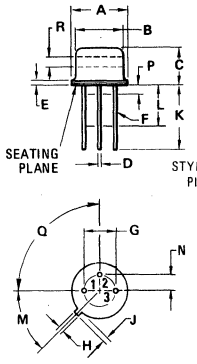


STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ Ø 0.10 (0.004) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.37	7.87	0.290	0.310
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.46	0.61	0.018	0.024
G	1.27 BSC		0.050 BSC	
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
N	2.03	2.92	0.080	0.115
R	3.43	–	0.135	–
S	0.46	0.61	0.018	0.024

CASE 29-03
TO-226AE



STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-205AD
(TO-39)

D

MFE930
MFE960
MFE990

MOTOROLA

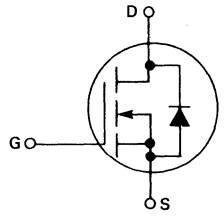
D

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

These TMOS FETs are designed for high-speed switching applications such as switching power supplies, CMOS logic, microprocessor or TTL-to-high current interface and line drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 7.0$ ns Typ
- Low On-Resistance — 0.9 Ohm Typ MFE930
  1.2 Ohm Typ MFE960 and MFE990
- Low Drive Requirement, $V_{GS(th)} = 3.5$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

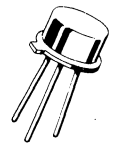
TMOS™

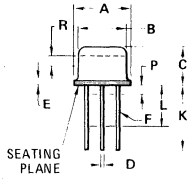


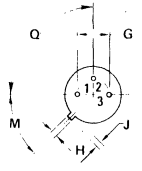
2.0 AMPERE

N-CHANNEL TMOS FET

30, 60, 90 VOLTS







STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-205AD
(TO-39)

MAXIMUM RATINGS

Rating	Symbol	MFE930	MFE960	MFE990	Unit
Drain-Source Voltage	V_{DSS}	35	60	90	Vdc
Drain-Gate Voltage	V_{DGO}	35	60	90	Vdc
Gate Source Voltage	V_{GS}	±30			Vdc
Drain Current Continuous (1) Pulsed (2)	 I_D I_{DM}	 2.0 3.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	6.25 50			Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	MFE930	$V_{(BR)DSS}$	35	—	—	Vdc
	MFE960		60	—	—	
	MFE990		90	—	—	
Zero Gate Voltage Drain Current (V_{DS} = Maximum Rating, V_{GS} = 0)		I_{DSS}	—	—	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	50	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)		$V_{GS(th)}$	1.0	—	3.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$				Vdc
(I_D = 0.5A)	MFE930		—	0.4	0.7	
	MFE960		—	0.6	0.8	
	MFE990		—	0.6	1.0	
(I_D = 1.0 A)	MFE930		—	0.9	1.4	
	MFE960		—	1.2	1.7	
	MFE990		—	1.2	2.0	
(I_D = 2.0 A)	MFE930		—	2.2	3.0	
	MFE960		—	2.8	3.5	
	MFE990		—	2.8	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	MFE930	$r_{DS(on)}$	—	0.9	1.4	Ohms
	MFE960		—	1.2	1.7	
	MFE990		—	1.2	2.0	
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)		$I_{D(on)}$	1.0	2.0	—	Amps
Forward Transconductance (V_{DS} = 25 V, I_D = 0.5 A)		g_{fs}	200	380	—	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	60	70	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	—	49	60	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	—	13	18	pF
SWITCHING CHARACTERISTICS*						
Turn-On Time See Figure 1		t_{on}	—	7.0	15	ns
Turn-Off Time See Figure 1		t_{off}	—	7.0	15	ns

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

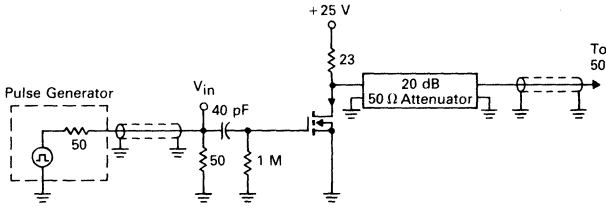
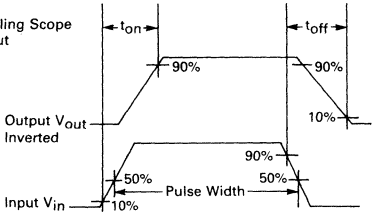


FIGURE 2 — SWITCHING WAVEFORMS



D

FIGURE 3 — ON VOLTAGE versus TEMPERATURE

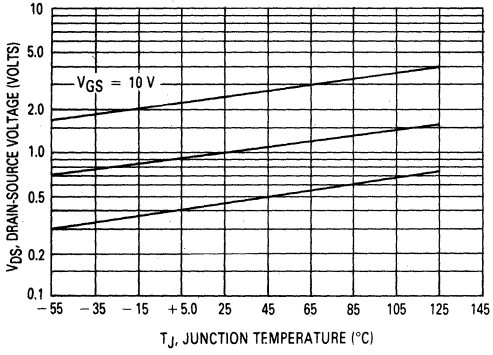


FIGURE 4 — CAPACITANCE VARIATION

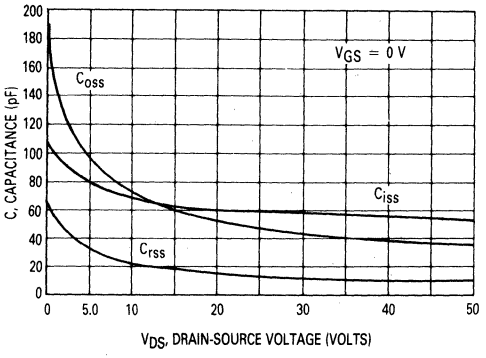


FIGURE 5 — TRANSFER CHARACTERISTIC

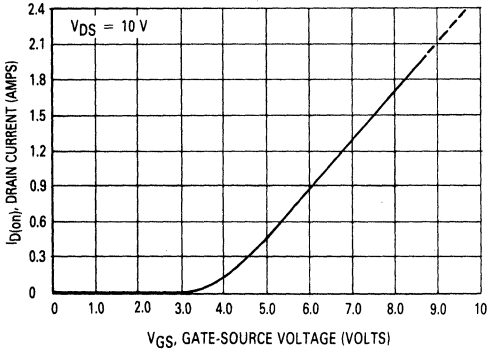


FIGURE 6 — OUTPUT CHARACTERISTIC

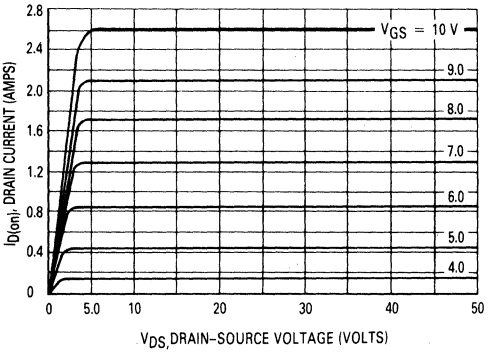
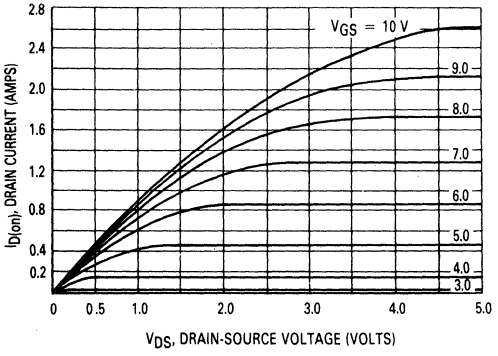


FIGURE 7 — SATURATION CHARACTERISTIC



MOTOROLA

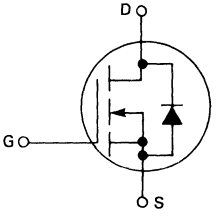
MFE9200

N-CHANNEL ENHANCEMENT MODE TMOS FIELD EFFECT TRANSISTOR

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL-to-high voltage interface and high-voltage display drivers.

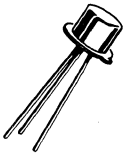
- Fast Switching Speed — $t_{on} = t_{off} = 6.0$ ns Typ
- Low On-Resistance — 4.5 Ohms Typ
- Low Drive Requirement, $V_{GS(th)} = 4.0$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

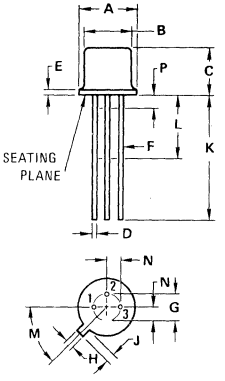
TMOS™



200 VOLTS

N-CHANNEL TMOS FET





STYLE 12:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC notes and dimensions apply.

CASE 22-03
TO-206AA
(TO-18)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous (1) Pulsed (2)	 I_D I_{DM}	 400 800	 mAdc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	 1.8 14.4	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSS}$	200	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 200 V, V_{GS} = 0)	I_{DSS}	—	0.1	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 Vdc, V_{DS} = 0)	I_{GSS}	—	0.01	50	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	1.0	—	4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$				Vdc
(I_D = 100 mA)		—	0.45	0.6	
(I_D = 250 mA)		—	1.20	1.60	
(I_D = 500 mA)		—	3.0	—	
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	$I_{D(on)}$	400	700	—	mA
State Drain-Source On-Resistance (V_{GS} = 10 Vdc)	$r_{DS(on)}$				Ohms
(I_D = 100 mA)		—	4.5	6.0	
(I_D = 250 mA)		—	4.8	6.4	
(I_D = 500 mA)		—	6.0	—	
Forward Transconductance (V_{DS} = 25 V, I_D = 250 mA)	g_{fs}	200	400	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	72	90	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	15	20	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.8	3.5	pF
SWITCHING CHARACTERISTICS*					
Turn-On Time See Figure 1	t_{on}	—	6.0	15	ns
Turn-Off Time See Figure 1	t_{off}	—	6.0	15	ns

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

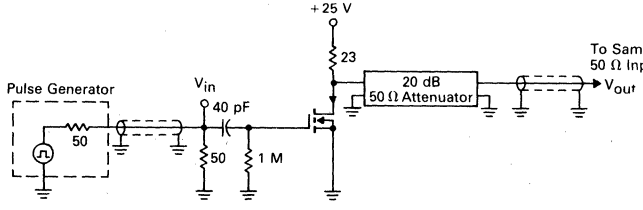


FIGURE 2 — SWITCHING WAVEFORMS

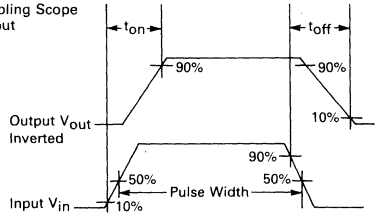


FIGURE 3 — ON VOLTAGE versus TEMPERATURE

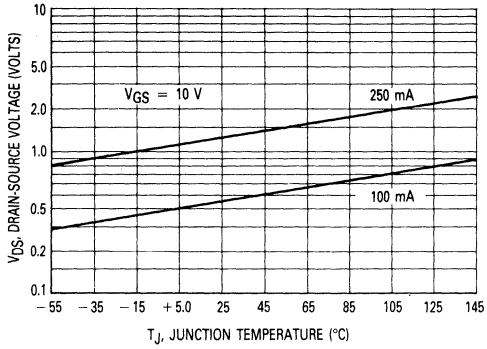
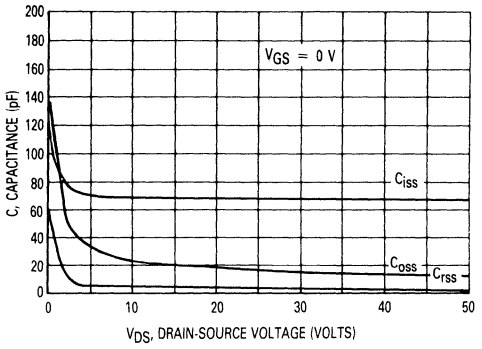


FIGURE 4 — CAPACITANCE VARIATION



D

FIGURE 5 — TRANSFER CHARACTERISTIC

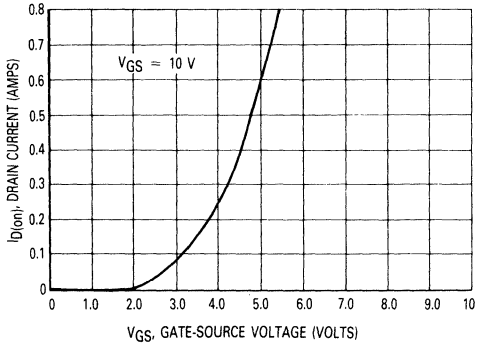


FIGURE 6 — OUTPUT CHARACTERISTIC

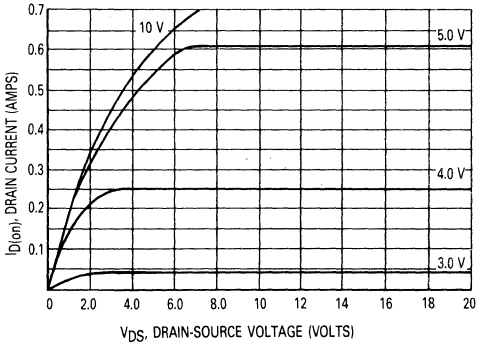
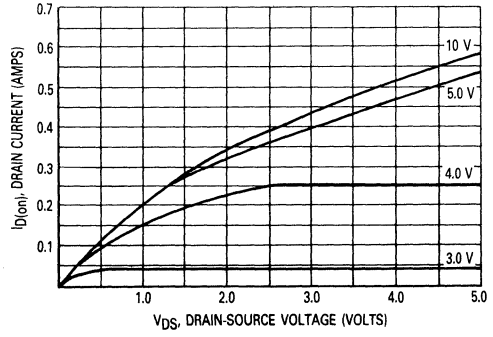


FIGURE 7 — SATURATION CHARACTERISTIC



MFQ930C
MFQ960C
MFQ990C

MOTOROLA

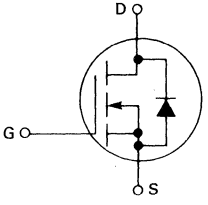
D

QUAD DUAL-IN-LINE N-CHANNEL EXHANCEMENT MODE SILICON GATE TMOS FIELD EFFECT TRANSISTORS

These TMOS FETs are designed for high speed switching applications such as switching power supplies, CMOS logic, microprocessor or TTL-to-high current interface and line drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 7.0$ nsTyp
- Low On-Resistance — 0.9 OhmTyp MFQ930C
  1.2 OhmTyp MFQ960C and MFQ990C
- Low Drive Requirement, $V_{GS(th)} = 3.5$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

TMOS™

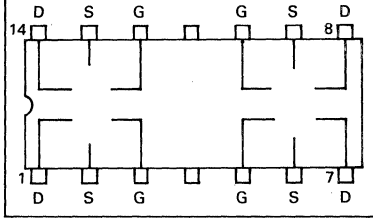


2.0 AMPERE

QUAD DUAL-IN-LINE N-CHANNEL TMOS FETS

35, 60, 90 VOLTS

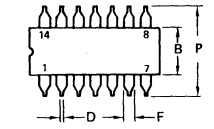
CONNECTION DIAGRAM

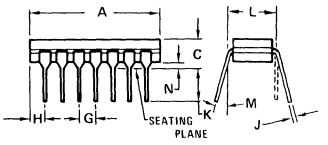


MAXIMUM RATINGS

Rating	Symbol	MFQ930C	MFQ960C	MFQ990C	Unit
Drain-Source Voltage	V_{DSS}	35	60	90	Vdc
Drain-Gate Voltage	V_{DGO}	35	60	90	Vdc
Gate Source Voltage	V_{GS}	±30			Vdc
Drain Current Continuous (1) Pulsed (2)	 I_D I_{DM}	 2.0 3.0			Adc
		Each Transistor	All Four Transistors		
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	 1.0 8.0	 2.0 16		Watts mW/°C
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	 2.0 16	 4.0 32		Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150			°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%





NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. LEADS WITHIN 0.25mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

CERAMIC
CASE 632-02
TO-116

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	MFQ930C	$V_{(BR)DSS}$	35	—	—	Vdc
	MFQ960C		60	—	—	
	MFQ990C		90	—	—	
Zero Gate Voltage Drain Current (V_{DS} = Maximum Rating, V_{GS} = 0)		I_{DSS}	—	—	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	50	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	1.0	—	3.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$				Vdc
(I_D = 0.5 A)	MFQ930C		—	0.4	0.7	
	MFQ960C		—	0.6	0.8	
	MFQ990C		—	0.6	1.0	
(I_D = 1.0 A)	MFQ930C		—	0.9	1.4	
	MFQ960C		—	1.2	1.7	
	MFQ990C		—	1.2	2.0	
(I_D = 2.0 A)	MFQ930C		—	2.2	3.0	
	MFQ960C		—	2.8	3.5	
	MFQ990C		—	2.8	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	MFQ930C	$r_{DS(on)}$	—	0.9	1.4	Ohms
	MFQ960C		—	1.2	1.7	
	MFQ990C		—	1.2	2.0	
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)		$I_{D(on)}$	1.0	2.0	—	Amps
Forward Transconductance (V_{DS} = 25 V, I_D = 0.5 A)		g_{fs}	200	380	—	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	60	70	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{oss}	—	49	60	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	13	18	pF
SWITCHING CHARACTERISTICS*						
Turn-On Time See Figure 1		t_{on}	—	7.0	15	ns
Turn-Off Time See Figure 1		t_{off}	—	7.0	15	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

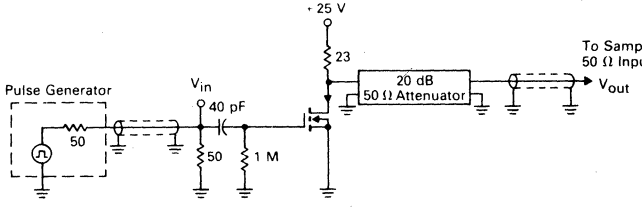
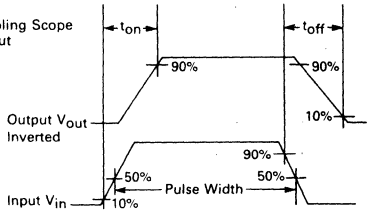


FIGURE 2 — SWITCHING WAVEFORMS



MPF930
MPF960
MPF990

MOTOROLA

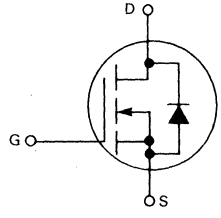
D

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

These TMOS FETs are designed for high-speed switching applications such as switching power supplies, CMOS logic, microprocessor or TTL to current interface and line drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 7.0$ ns typ
- Low On-Resistance — 0.9 Ohm typ MPF930
  1.2 Ohm typ MPF960 and MPF990
- Low Drive Requirement, $V_{GS(th)} = 3.5$ V max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

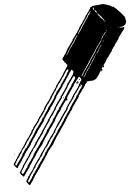
TMOS™



2.0 AMPERE

N-CHANNEL TMOS FET

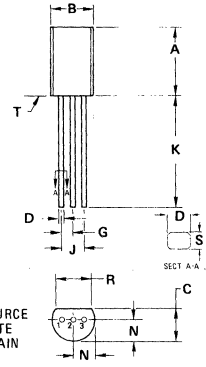
35, 60, 90 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MPF930	MPF960	MPF990	Unit
Drain-Source Voltage	V_{DSS}	35	60	90	Vdc
Drain-Gate Voltage	V_{DGO}	35	60	90	Vdc
Gate Source Voltage	V_{GS}	±30			Vdc
Drain Current Continuous (1) Pulsed (2)	 I_D I_{DM}	 2.0 3.0			Adc
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	1.0 8.0			Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150			°C
Thermal Resistance	θ_{JA}	125			°C/W

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ Ø 0.10 (0.004)Ⓜ T A Ⓜ B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.37	7.87	0.290	0.310
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.46	0.61	0.018	0.024
G	1.27 BSC		0.050 BSC	
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
N	2.03	2.92	0.080	0.115
R	3.43	–	0.135	–
S	0.46	0.61	0.018	0.024

CASE 29-03
TO-226AE

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	MPF930	$V_{(BR)DSS}$	35	—	—	Vdc
	MPF960		60	—	—	
	MPF990		90	—	—	
Zero Gate Voltage Drain Current (V_{DS} = Maximum Rating, V_{GS} = 0)		I_{DSS}	—	—	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	50	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	1.0	—	3.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$				Vdc
(I_D = 0.5 A)	MPF930		—	0.4	0.7	
	MPF960		—	0.6	0.8	
	MPF990		—	0.6	1.0	
(I_D = 1.0 A)	MPF930		—	0.9	1.4	
	MPF960		—	1.2	1.7	
	MPF990		—	1.2	2.0	
(I_D = 2.0 A)	MPF930		—	2.2	3.0	
	MPF960		—	2.8	3.5	
	MPF990		—	2.8	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	MPF930	$r_{DS(on)}$	—	0.9	1.4	Ohms
	MPF960		—	1.2	1.7	
	MPF990		—	1.2	2.0	
On State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V		$I_{D(on)}$	1.0	2.0	—	Amps
Forward Transconductance (V_{DS} = 25 V, I_D = 0.5 A)		g_{fs}	200	380	—	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	60	70	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{oss}	—	49	60	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	13	18	pF
SWITCHING CHARACTERISTICS*						
Turn-On Time See Figure 1		t_{on}	—	7.0	15	ns
Turn-Off Time See Figure 1		t_{off}	—	7.0	15	ns

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

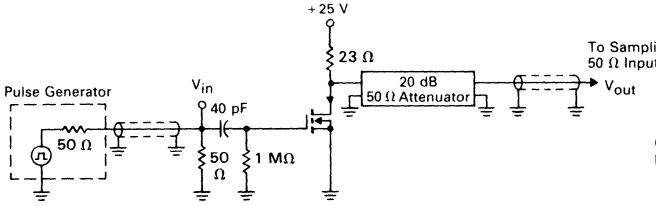


FIGURE 2 — SWITCHING WAVEFORMS

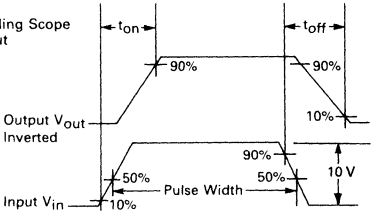


FIGURE 3 — ON VOLTAGE versus TEMPERATURE

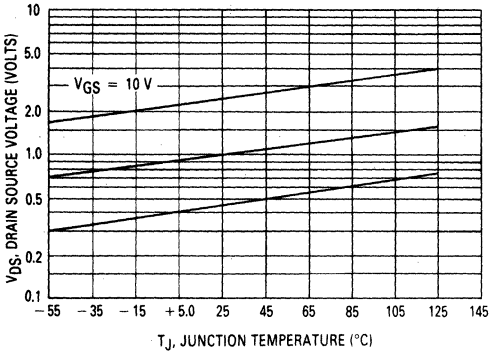


FIGURE 4 — CAPACITANCE VARIATION

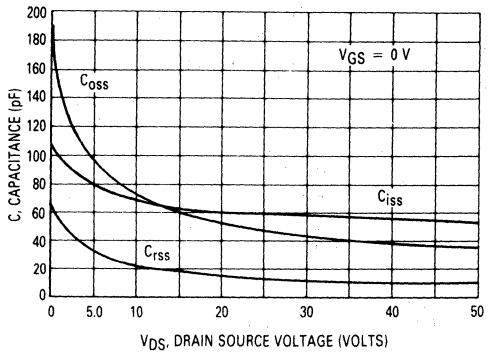


FIGURE 5 — TRANSFER CHARACTERISTIC

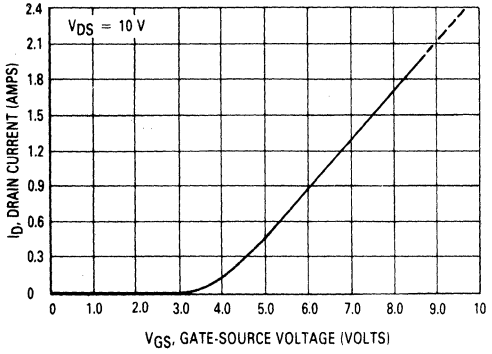


FIGURE 6 — OUTPUT CHARACTERISTIC

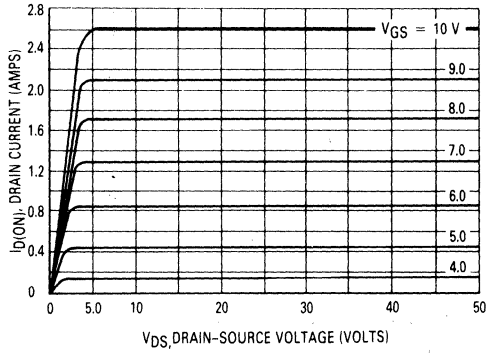
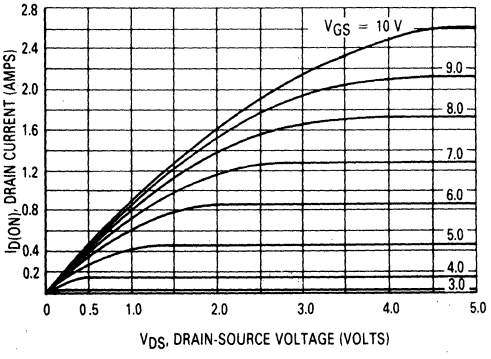


FIGURE 7 — SATURATION CHARACTERISTIC



MOTOROLA

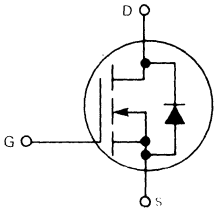
MPF9200

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

This TMOS FET is designed for high voltage, high speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL to high voltage interface and high voltage display drivers.

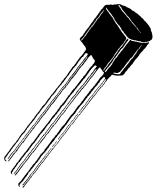
- Fast Switching Speed — $t_{on} = t_{off} = 6.0$ ns typ
- Low On-Resistance — 4.5 Ohms typ
- Low Drive Requirement, $V_{GS(th)} = 4.0$ V max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

TMOS™



200 VOLTS

N-CHANNEL TMOS FET

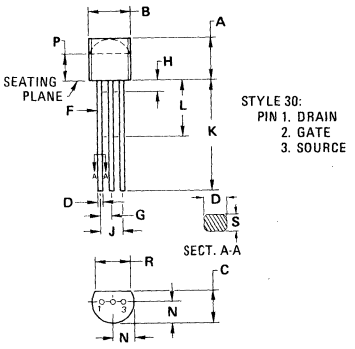


D

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous (1) Pulsed (2)	I_D I_{DM}	400 800	mAdc
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	0.6 4.8	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Thermal Resistance Junction to Ambient	θ_{JA}	208	°C/W

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70 mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70 mm (0.5") FROM SEATING PLANE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
(TO-92)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSS}$	200	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 200 V, V_{GS} = 0)	I_{DSS}	—	0.1	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 Vdc, V_{DS} = 0)	I_{GSS}	—	0.01	50	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})	$V_{GS(th)}$	1.0	—	4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$				Vdc
(I_D = 100 mA)		—	0.45	0.6	
(I_D = 250 mA)		—	1.20	1.60	
(I_D = 500 mA)		—	3.0	—	
On State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V	$I_{D(on)}$	400	700	—	mA
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc)	$r_{DS(on)}$				Ohms
(I_D = 100 mA)		—	4.5	6.0	
(I_D = 250 mA)		—	4.8	6.4	
(I_D = 500 mA)		—	6.0	—	
Forward Transconductance (V_{DS} = 25 V, I_D = 250 mA)	g_{fs}	200	400	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance OV_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	72	90	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	15	20	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.8	3.5	pF
SWITCHING CHARACTERISTICS*					
Turn-On Time See Figure 1	t_{on}	—	6.0	15	ns
Turn-Off Time See Figure 1	t_{off}	—	12	15	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

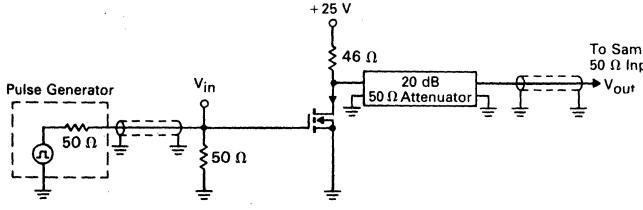


FIGURE 2 — SWITCHING WAVEFORMS

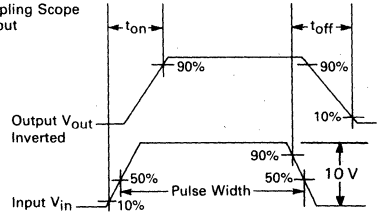


FIGURE 3 — ON VOLTAGE versus TEMPERATURE

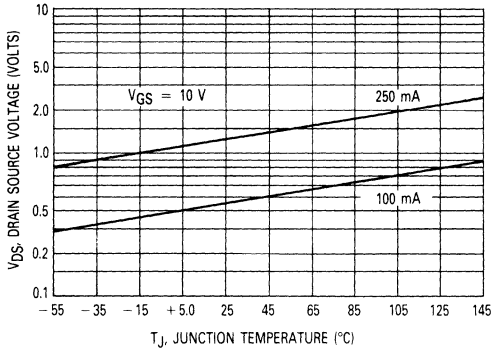


FIGURE 4 — CAPACITANCE VARIATION

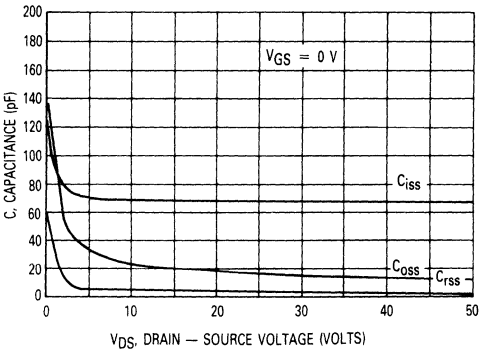


FIGURE 5 — TRANSFER CHARACTERISTIC

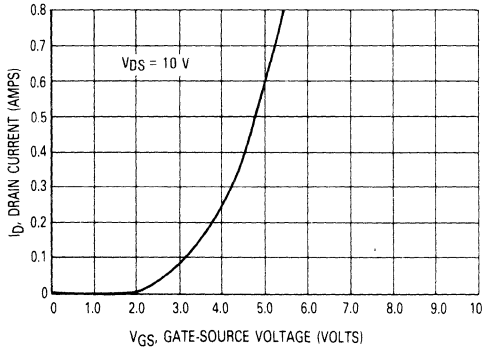


FIGURE 6 — OUTPUT CHARACTERISTIC

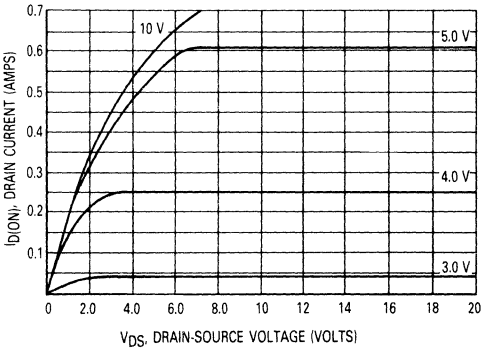
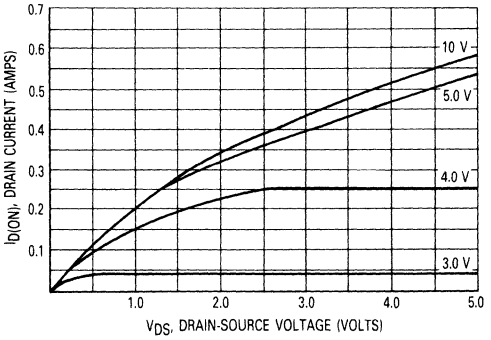


FIGURE 7 — SATURATION CHARACTERISTIC



D

D

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E

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2N6661	2N6661		D-2
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UNF26A2		MTP12N10	C-187
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VN0104N1	CF	CF	-
VN0104N2	CF	CF	-
VN0104N3	CF	CF	-
VN0104N4		MTP5N05	C-245
VN0104N5		MTP5N05	C-245
VN0104N6	-	-	-
VN0106N1	-	-	-
VN0106N2	-	-	-
VN0106N3	-	-	-
VN0106N4		MTP5N06	C-245
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VN0108N2	-	-	-
VN0108N3	-	-	-
VN0108N4		MTP4N08	C-245
VN0108N5		MTP4N08	C-245
VN0108N6	-	-	-
VN0109N1	-	-	-
VN0109N2	-	-	-
VN0109N3	-	-	-
VN0109N4		MTP4N10	C-245
VN0109N5		MTP4N10	C-245
VN0109N6	-	-	-
VN0204N1	-	-	-
VN0204N2	-	-	-
VN0204N3	-	-	-
VN0204N4		MTP5N05	C-245
VN0204N5		MTP5N05	C-245
VN0204N6	-	-	-
VN0206N1	-	-	-
VN0206N2	-	-	-
VN0206N5		MTP5N06	C-245
VN0206N6		MTP5N06	C-245
VN0208N1	-	-	-
VN0208N2	-	-	-
VN0208N5		MTP4N08	C-245
VN0208N6		MTP4N08	C-245
VN0209N1	-	-	-
VN0209N2	-	-	-
VN0209N5		MTP4N10	C-245
VN0209N6		MTP4N10	C-245
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VN0300M	-	-	-
VN0330N1		MTM3N35	C-112
VN0330N2	-	-	-
VN0330N5		MTP3N35	C-112
VN0335N1		MTM3N35	C-112
VN0335N2	-	-	-
VN0335N5		MTP3N35	C-112
VN0340N1		MTM3N40	C-112
VN0340N2	-	-	-
VN0340N5		MTP3N40	C-112
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VN0401A		MTM15N05	-
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VN0430N1		MTM5N35	C-127
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VN0440N1		MTM7N40	-
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VN0600D		MTP15N06	-
VN0601A		MTM15N06	-
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VN10KE	-	-	-
VN10KM	VN10LM		-
VN10LE	-	-	-
VN10LM		MPF10LM	-
VN35AA		MTM10N05	C-152
VN35AB	VN35AB		-
VN40AD	-	-	-
VN40AF		MPF6660	D-2
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VN46AF		MPF6660	D-2
VN64GA	-	-	-
VN66AB	VN66AB		-
VN66AD		MTP5N06	C-245
VN66AF		MPF6660	D-2
VN67AA	-	-	-
VN67AB	-	-	-
VN67AD		MTP5N06	C-245
VN67AF	-	-	-
VN80AF		MPF6660	D-2
VN88AD		MTP4N08	C-245
VN88AF		MPF6661	D-2
VN89AD		MTP4N08	C-245
VN89AF	-	-	-
VN90AA		MTP8N10	C-152
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VN99AA		MTP8N10	C-152
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VN300M		MPF930	D-22
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VN1206M	-	-	-
VN1206N1		MTM10N06	C-152
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VN1206N5		MTP10N06	C-152
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VN1208N2	-	-	-
VN1208N5		MTP10N08	C-167
VN1209N1		MTM10N10	C-167
VN1209N2	-	-	-
VN1209N5		MTP10N08	C-167
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VN1210M		BS107	D-6
VN1304N2	CF	CF	-
VN1304N3	CF	CF	-

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VN1306N2	CF	CF	-
VN1306N3	CF	CF	-
VN1306N6	CF	CF	-
VN1308N2	CF	CF	-
VN1308N3	CF	CF	-
VN1308N6	CF	CF	-
VN1309N2	CF	CF	-
VN1309N3	CF	CF	-
VN1309N6	CF	CF	-
VN1706B	-	-	-
VN1706D		MTP2N18	C-240
VN1706L	-	-	-
VN1706M	-	-	-
VN1710L	-	-	-
VN1710M		BS107	D-6
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VN2406D		MTP2N35	C-231
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VN2406M	-	-	-
VN2410L	-	-	-
VN2410M		BS107	D-6
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VP0104N2	-	-	-
VP0104N3	-	-	-
VP0104N5	-	-	-
VP0104N6	-	-	-
VP0106N1	-	-	-
VP0106N2	-	-	-
VP0106N3	-	-	-
VP0106N5	-	-	-
VP0106N6	-	-	-
VP0108N1	-	-	-
VP0108N2	-	-	-
VP0108N3	-	-	-
VP0108N5	-	-	-
VP0108N6	-	-	-

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VP0109N2	-	-	-
VP0109N3	-	-	-
VP0109N5	-	-	-
VP0109N6	-	-	-
VP0204N1	-	-	-
VP0204N2	-	-	-
VP0204N5	-	-	-
VP0204N6	-	-	-
VP0206N1	-	-	-
VP0206N2	-	-	-
VP0206N5	-	-	-
VP0206N6	-	-	-
VP0208N1	-	-	-
VP0208N2	-	-	-
VP0208N5	-	-	-
VP0208N6	-	-	-
VP0209N1	-	-	-
VP0209N2	-	-	-
VP0209N5	-	-	-
VP0209N6	-	-	-
VP0300B	-	-	-
VP0300M	-	-	-
VP0808B	-	-	-
VP0808L	-	-	-
VP0808M	-	-	-
VP1008B	-	-	-
VP1008L	-	-	-
VP1008M	-	-	-
VP1204N1		MTM8P08	C-162
VP1204N2	-	-	-
VP1204N5		MTP8P08	C-162
VP1206N1		MTM8P08	C-162
VP1206N2	-	-	-
VP1206N5	-	-	-
VP1208N1		MTM8P08	C-162
VP1208N2	-	-	-
VP1208N5		MTP8P08	C-162
VP1209N1		MTM8P10	C-162
VP1209N2	-	-	-
VP1209N5		MTP8P10	C-162
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