

MB81V4260S-60/-70

CMOS 256K X 16 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 262,144 x 16 bit Fast Page Mode Dynamic RAM

The Fujitsu MB81V4260S is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 16-bit increments. The MB81V4260S features a "fast page" mode of operation whereby high-speed access of up to 512x16-bits of data can be selected in the same row. The MB81V4260S-60/-70 DRAMs are ideally suited for memory applications such as embedded control, buffer, portable computers, and video imaging equipment where very low power dissipation and high bandwidth are basic requirements of the design.

The MB81V4260S is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes.

PRODUCT LINE & FEATURES

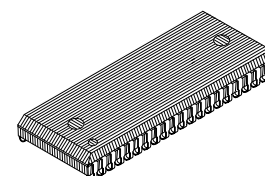
Parameter		MB81V4260S-60	MB81V4260S-70
RAS Access Time		60ns max.	70ns max.
CAS Access Time		20ns max.	20ns max.
Address Access Time		30ns max.	35ns max.
Random Cycle Time		110ns max.	125ns min.
Fast Page Mode Cycle Time		40ns min.	45ns min.
Low Power Dissipation	Operating current	378mW max.	335mW max.
	Standby current	7.2mW max. (LVTTTL level), 3.6mW max. (CMOS level)	

- Low VCC operating
- 262,144 words x 16 bit organization
- Silicon gate, CMOS, Advanced Stacked Capacitor Cell
- All input and output are LVTTTL compatible
- 512 refresh cycles every 8.2ms
- 9 rows x 9 columns, addressing scheme
- Self refresh function
- 1WE / 2CAS
- Early Write or OE controlled Write capability
- RAS only, CAS-before-RAS, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

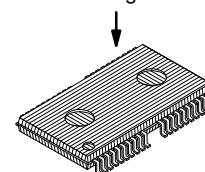
Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	-0.5 to +4.6	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C
Temperature under Bias	T_{BIAS}	0 to +70	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



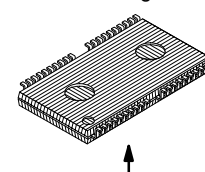
Plastic SOJ Package
LCC-40P-M01

Marking side



FPT-44P-M07
(Normal Bend)

Marking side



FPT-44P-M08
(Reverse Bend)

Plastic TSOP Packages

Package and Ordering Information

- 40-pin plastic (400mil) SOJ, order as MB81V4260S-xxPJ
- 44-pin plastic (400mil) TSOP-II with normal bend leads, order as MB81V4260S-xxPFTN
- 44-pin plastic (400mil) TSOP-II with reverse bend leads, order as MB81V4260S-xxPFTR

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

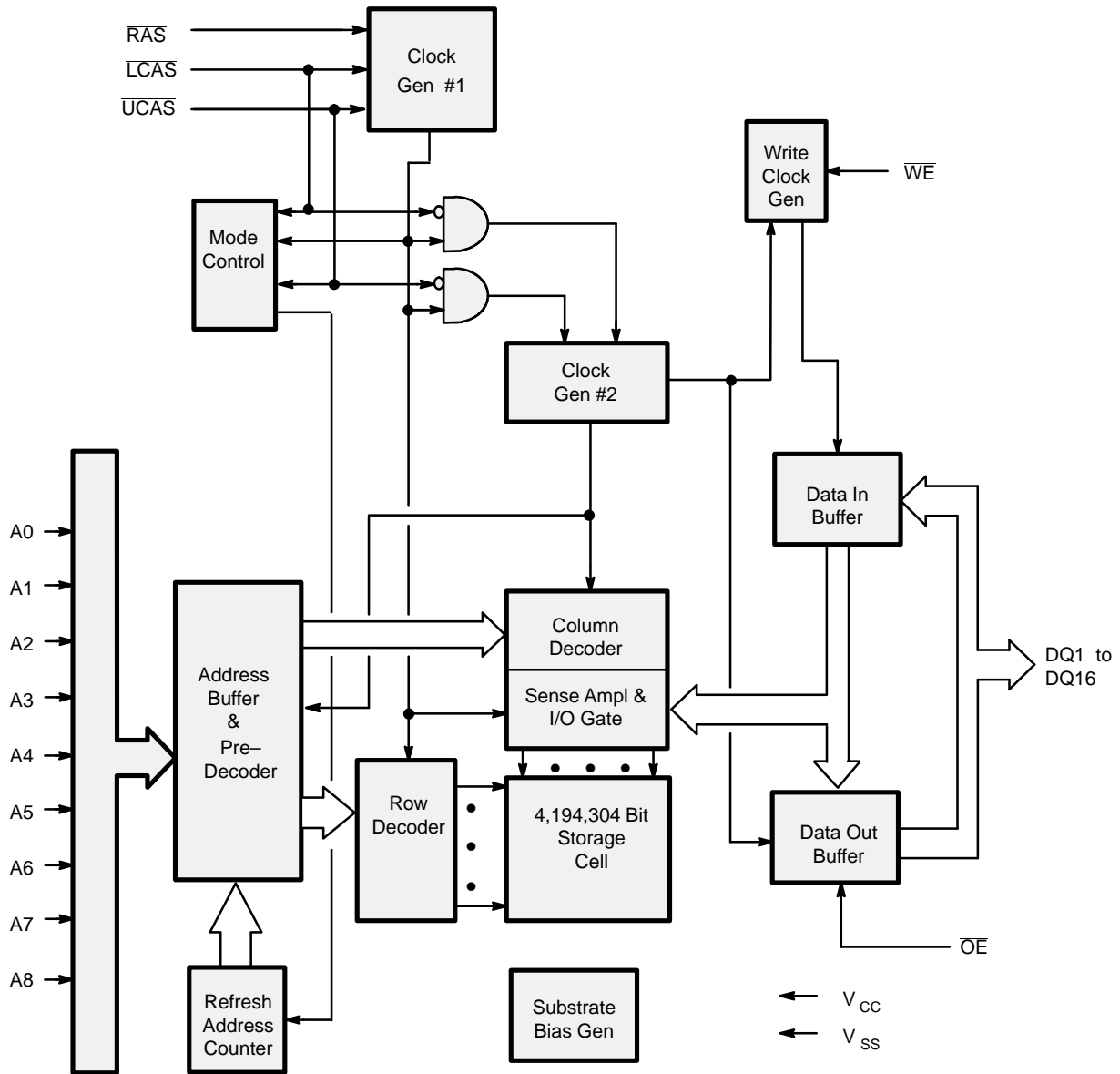
– PRELIMINARY –

Edition 2.0

MB81V4260S-60

MB81V4260S-70

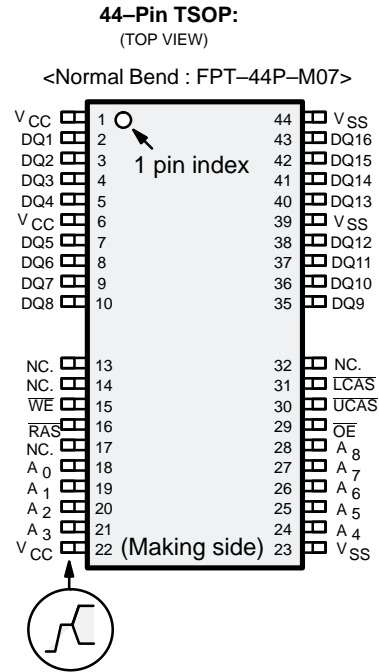
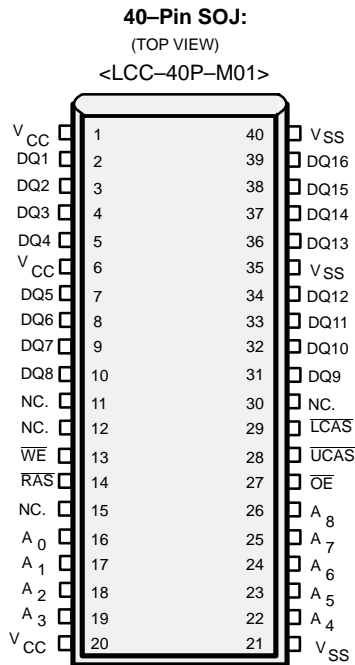
Fig. 1 – MB81V4260S DYNAMIC RAM – BLOCK DIAGRAM



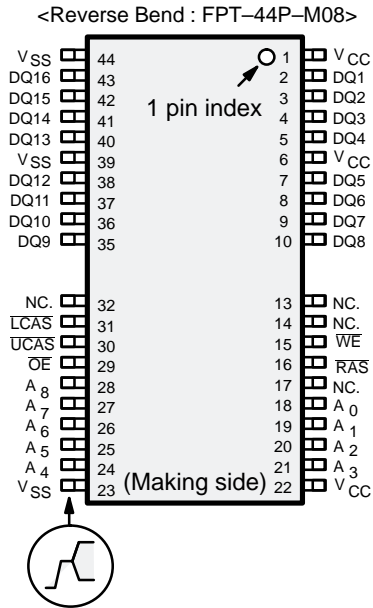
CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, RAS, LCAS, UCAS, WE, OE	C_{IN2}	—	7	pF
Input/Output Capacitance, DQ1 to DQ16	C_{DQ}	—	7	pF

PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
A0 to A8	Address inputs. row : A0 to A8 column : A0 to A8 refresh : A0 to A8
RAS	Row address strobe.
LCAS	Lower column address strobe
UCAS	Upper column address strobe
WE	Write enable
OE	Output enable.
DQ1 to DQ16	Data Input/ Output
VCC	+3.3 volt power supply.
VSS	Circuit ground.



– PRELIMINARY –

Edition 2.0

MB81V4260S-60

MB81V4260S-70

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	3.0	3.3	3.6	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	V_{IH}	2.0	—	$V_{CC}+0.3$	V	
Input Low Voltage, all inputs (*)	1	V_{IL}	−0.3	—	0.8	V	
Input Low Voltage, DQ (*)	1	V_{ILD}	−0.3	—	0.8	V	

* : Undershoots of up to −2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any sixteen of 4,194,304 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by \overline{LCAS} or \overline{UCAS} and \overline{RAS} as shown in Figure 5. First, nine row address bits are input on pins A0–through–A8 and latched with the row address strobe (\overline{RAS}) then, nine column address bits are input and latched with the column address strobe (\overline{LCAS} or \overline{UCAS}). Both row and column addresses must be stable on or before the falling edges of \overline{RAS} and \overline{LCAS} or \overline{UCAS} , respectively. The address latches are the flow-through type; thus, address information appearing after t_{RAH} (min)+ t_r is automatically treated as the column address to start select operation of the column decode. Therefore, to have correct data within t_{RAC} , the column address should be input within $t_{RAD}(\max.)$. If $t_{RAD} > t_{RAD}(\max.)$, the access time is the later one of either t_{AA} or t_{CAS} .

WRITE ENABLE

The read or write mode is determined by the logic state of \overline{WE} . When \overline{WE} is active Low, a write cycle is initiated; when \overline{WE} is High, a read cycle is selected. During the read mode, input data are ignored. When an early write cycle is executed, the output buffers stay in a high-impedance state during the cycle.

DATA INPUT

Input data are written into memory in either of three basic ways—the early write cycle, the \overline{OE} (delayed) write cycle, and the read-modify-write cycle. The falling edge of \overline{WE} or \overline{LCAS} / \overline{UCAS} , whichever is later, serves as the input data-latch strobe. In the early write cycle, the input data of DQ1–DQ8 are strobed by \overline{LCAS} and DQ9–DQ16 are strobed by \overline{UCAS} and the setup/hold times are referenced to each falling edge of \overline{LCAS} and \overline{UCAS} because \overline{WE} goes Low before \overline{LCAS} / \overline{UCAS} . In the delayed write or read-modify-write cycle, \overline{WE} goes Low after \overline{LCAS} / \overline{UCAS} ; thus, input data is strobed by \overline{WE} and all setup/hold times are referenced to the falling edge of \overline{WE} . Since this device is an I/O common type, when the delayed write or read-modified-write is executed, I/O data have to be controlled by \overline{OE} .

DATA OUTPUT

The three-state buffers are LVTTTL compatible with a fanout of one TTL load. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

t_{RAC} : from the falling edge of \overline{RAS} when t_{RCD} (max) is satisfied.

t_{CAC} : from the falling edge of \overline{LCAS} (for DQ1–DQ8) \overline{UCAS} (for DQ9–DQ16) when t_{RCD} is greater than t_{RCD} (max).

t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max).

t_{OEA} : from the falling edge of \overline{OE} when \overline{OE} is brought Low after t_{RAC} , t_{CAC} , or t_{AA} .

The data remains valid until either \overline{LCAS} / \overline{UCAS} or \overline{OE} returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, \overline{RAS} is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 512x16-bits can be accessed. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

– PRELIMINARY –

Edition 2.0

MB81V4260S-60

MB81V4260S-70

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Notes 3

Parameter	Notes	Symbol	Conditions	Value		Unit
				Min	Max	
Output high voltage	1	V_{OH}	$I_{OH} = -2.0 \text{ mA}$	2.4	—	V
Output low voltage	1	V_{OL}	$I_{OL} = +2.0 \text{ mA}$	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	$0V \leq V_{IN} \leq 3.6V$; $3.0V \leq V_{CC} \leq 3.6V$; $V_{SS} = 0V$; All other pins not under test = $0V$	-10	10	μA
Output leakage current		$I_{DQ(L)}$	$0V \leq V_{OUT} \leq 3.6V$; Data out disabled	-10	10	
Operating current (Average power supply current) 2	MB81V4260S-60	I_{CC1}	\overline{RAS} & \overline{LCAS} , \overline{UCAS} cycling; $t_{RC} = \text{min}$	—	105	mA
	MB81V4260S-70				93	
Standby current (Power supply current)	LV TTL level	I_{CC2}	$\overline{RAS} = \overline{LCAS}$, $\overline{UCAS} = V_{IH}$	—	2.0	mA
	CMOS level		$\overline{RAS} = \overline{LCAS}$, $\overline{UCAS} \geq V_{CC} - 0.2V$		1.0	
Refresh current #1 (Average power sup- ply current) 2	MB81V4260S-60	I_{CC3}	\overline{LCAS} , $\overline{UCAS} = V_{IH}$, \overline{RAS} cycling; $t_{RC} = \text{min}$	—	105	mA
	MB81V4260S-70				93	
Fast Page Mode current 2	MB81V4260S-60	I_{CC4}	$\overline{RAS} = V_{IL}$, \overline{LCAS} , \overline{UCAS} cycling; $t_{PC} = \text{min}$	—	105	mA
	MB81V4260S-70				93	
Refresh current #2 (Average power sup- ply current) 2	MB81V4260S-60	I_{CC5}	\overline{RAS} cycling; \overline{CAS} -before- \overline{RAS} ; $t_{RC} = \text{min}$	—	105	mA
	MB81V4260S-70				93	
Refresh current #3 (Average power supply current) 2		I_{CC9}	$\overline{RAS} = V_{IL}$, $\overline{CAS} = V_{IL}$ Self Refresh ; $t_{RASS} = \text{min}$	—	1000	μA

– PRELIMINARY –

Edition 2.0

MB81V4260S-60

MB81V4260S-70

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V4260S-60		MB81V4260S-70		Unit
				Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	125	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	150	—	170	—	ns
4	Access Time from \overline{RAS}	6,9	t_{RAC}	—	60	—	70	ns
5	Access Time from \overline{CAS}	7,9	t_{CAC}	—	20	—	20	ns
6	Column Address Access Time	8,9	t_{AA}	—	30	—	35	ns
7	Output Hold Time		t_{OH}	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	15	ns
10	Transition Time		t_T	2	50	2	50	ns
11	\overline{RAS} Precharge Time		t_{RP}	40	—	45	—	ns
12	\overline{RAS} Pulse Width		t_{RAS}	60	100000	70	100000	ns
13	\overline{RAS} Hold Time		t_{RSH}	20	—	20	—	ns
14	\overline{CAS} to \overline{RAS} Precharge Time		t_{CRP}	0	—	0	—	ns
15	\overline{RAS} to \overline{CAS} Delay Time	11,12	t_{RCD}	20	40	20	50	ns
16	\overline{CAS} Pulse Width		t_{CAS}	20	10000	20	10000	ns
17	\overline{CAS} Hold Time		t_{CSH}	60	—	70	—	ns
18	\overline{CAS} Precharge Time (Normal)	19	t_{CPN}	10	—	10	—	ns
19	Row Address Setup Time		t_{ASR}	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
21	Column Address Setup Time		t_{ASC}	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	ns
23	\overline{RAS} to Column Address Delay Time	13	t_{RAD}	15	30	15	35	ns
24	Column Address to \overline{RAS} Lead Time		t_{RAL}	30	—	35	—	ns
25	Column Address to \overline{CAS} Lead Time		t_{CAL}	30	—	35	—	ns
26	Read Command Setup Time		t_{RCS}	0	—	0	—	ns
27	Read Command Hold Time Referenced to \overline{RAS}	14	t_{RRH}	0	—	0	—	ns
28	Read Command Hold Time Referenced to \overline{CAS}	14	t_{RCH}	0	—	0	—	ns
29	Write Command Setup Time	15	t_{WCS}	0	—	0	—	ns
30	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
31	\overline{WE} Pulse Width		t_{WP}	10	—	10	—	ns
32	Write Command to \overline{RAS} Lead Time		t_{RWL}	15	—	20	—	ns
33	Write Command to \overline{CAS} Lead Time		t_{CWL}	15	—	18	—	ns
34	DIN Setup Time		t_{DS}	0	—	0	—	ns
35	DIN Hold Time		t_{DH}	10	—	10	—	ns
36	\overline{RAS} to \overline{WE} Delay Time		t_{RWD}	85	—	95	—	ns
37	\overline{CAS} to \overline{WE} Delay Time		t_{CWD}	40	—	40	—	ns
38	Column Address to \overline{WE} Delay Time		t_{AWD}	55	—	60	—	ns
39	\overline{RAS} Precharge Time to \overline{CAS} Active Time (Refresh cycles)		t_{RPC}	10	—	10	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V4260S-60		MB81V4260S-70		Unit
				Min	Max	Min	Max	
40	CAS Set Up Time for $\overline{\text{CAS}}$ -before-RAS Refresh		t_{CSR}	0	—	0	—	ns
41	CAS Hold Time for $\overline{\text{CAS}}$ -before-RAS Refresh		t_{CHR}	10	—	10	—	ns
42	Access Time from OE	9	t_{OEA}	—	20	—	20	ns
43	Output Buffer Turn Off Delay from OE	10	t_{OEZ}	—	15	—	15	ns
44	$\overline{\text{OE}}$ to RAS Lead Time for Valid Data		t_{OEL}	10	—	10	—	ns
45	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$	16	t_{OEH}	0	—	0	—	ns
46	$\overline{\text{OE}}$ to Data in Delay Time		t_{OED}	15	—	15	—	ns
47	DIN to $\overline{\text{CAS}}$ Delay Time	17	t_{DZC}	0	—	0	—	ns
48	DIN to $\overline{\text{OE}}$ Delay Time	17	t_{DZO}	0	—	0	—	ns
50	Column Address Hold Time from $\overline{\text{RAS}}$		t_{AR}	32	—	32	—	ns
51	Write Command Hold Time from RAS		t_{WCR}	30	—	30	—	ns
52	DIN Hold Time Referenced to RAS		t_{DHR}	30	—	30	—	ns
53	$\overline{\text{CAS}}$ to Data in Delay Time		t_{CDD}	15	—	15	—	ns
60	Fast Page Mode RAS Pulse width		t_{RASP}	60	200000	70	200000	ns
61	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	ns
62	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	80	—	90	—	ns
63	Access Time from $\overline{\text{CAS}}$ Precharge	9,18	t_{CPA}	—	35	—	40	ns
64	Fast Page Mode $\overline{\text{CAS}}$ Pulse width		t_{CP}	10	—	10	—	ns
65	Fast Page Mode RAS Hold Time from CAS Precharge		t_{RHCP}	35	—	40	—	ns
66	Fast Page Mode CAS Precharge to $\overline{\text{WE}}$ Delay Time		t_{CPWD}	55	—	60	—	ns

Notes:

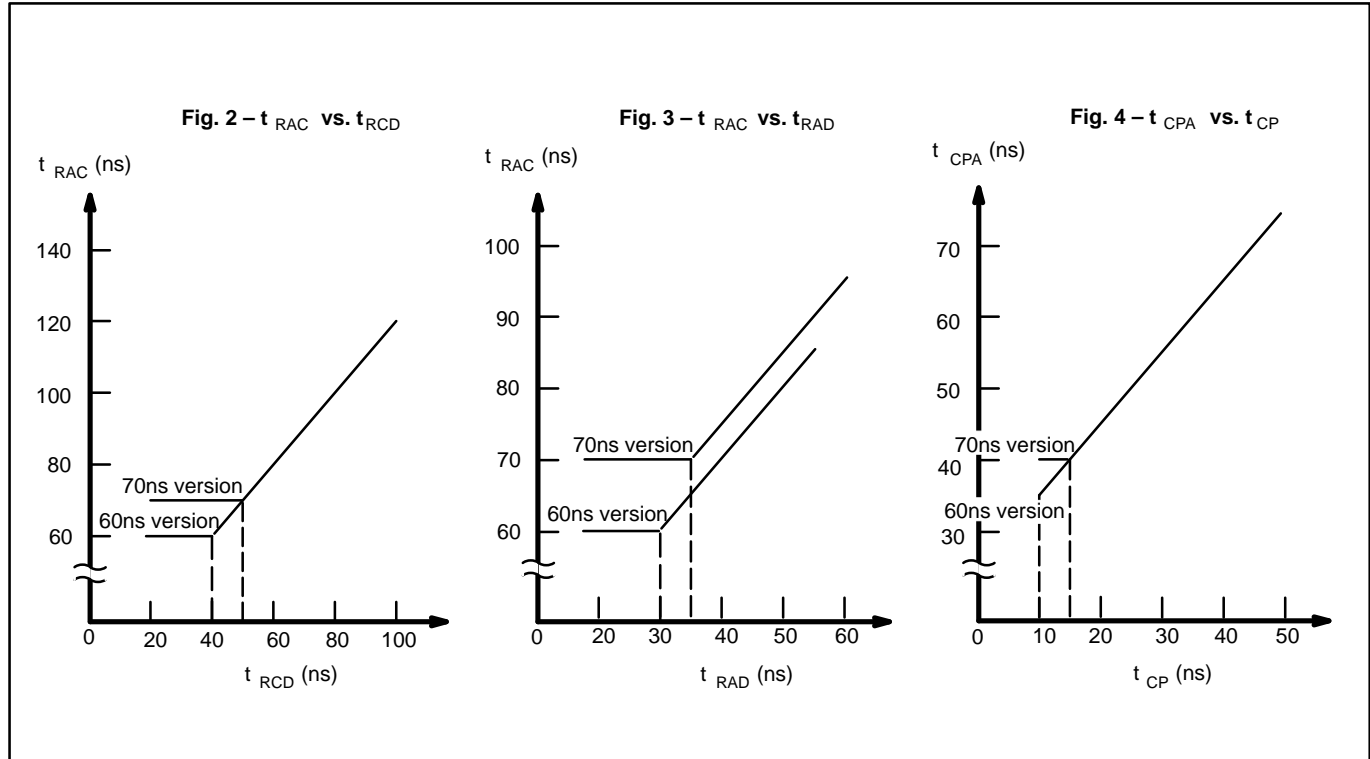
- Referenced to VSS. To all $V_{\text{CC}}(V_{\text{SS}})$ pins, the same supply voltage should be applied.
- ICC depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
ICC depends on the number of address change as $\overline{\text{RAS}} = V_{\text{IL}}$ and $\overline{\text{UCAS}} = V_{\text{IH}}$, $\overline{\text{LCAS}} = V_{\text{IH}}$, $V_{\text{IL}} > -0.3\text{V}$.
ICC1, ICC3 and ICC5 are specified at one time of address change during $\overline{\text{RAS}} = V_{\text{IL}}$ and $\overline{\text{UCAS}} = V_{\text{IH}}$, $\overline{\text{LCAS}} = V_{\text{IH}}$.
ICC4 is specified at one time of address change during one Page cycle.
- An initial pause ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{\text{IH}}$) of 200 μs is required after power-up followed by any eight $\overline{\text{RAS}}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
- AC characteristics assume $t_{\text{f}} = 5\text{ns}$.
- Input voltage levels are 0V and 3.0V, and input reference levels are $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ for measuring timing of input signals. Also, the transition time (t_{f}) is measured between $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$.
The output reference levels are $V_{\text{OH}}=2.0\text{V}$ and $V_{\text{OL}}=0.8\text{V}$.
- Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$, $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
- If $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$, $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$, and $t_{\text{ASC}} \geq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{T}}$, access time is t_{CAC} .
- If $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{ASC}} \leq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{T}}$, access time is t_{AA} .
- Measured with a load equivalent to one TTL loads and 100 pF.
- t_{OFF} and t_{OEZ} are specified that output buffer change to high impedance state.
- Operation within the $t_{\text{RCD}}(\text{max})$ limit ensures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
- $t_{\text{RCD}}(\text{min}) = t_{\text{RAH}}(\text{min}) + 2t_{\text{T}} + t_{\text{ASC}}(\text{min})$.
- Operation within the $t_{\text{RAD}}(\text{max})$ limit ensures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
- Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- t_{WCS} is specified as a reference point only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ the data output pin will remain High-Z state through entire cycle.
- Assumes that $t_{\text{WCS}} < t_{\text{WCS}}(\text{min})$.
- Either t_{DZC} or t_{DZO} must be satisfied.
- t_{CPA} is access time from the selection of a new column address (that is caused by changing both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than $t_{\text{CPA}}(\text{max})$.
- Assumes that $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh.

– PRELIMINARY –

Edition 2.0

MB81V4260S-60

MB81V4260S-70



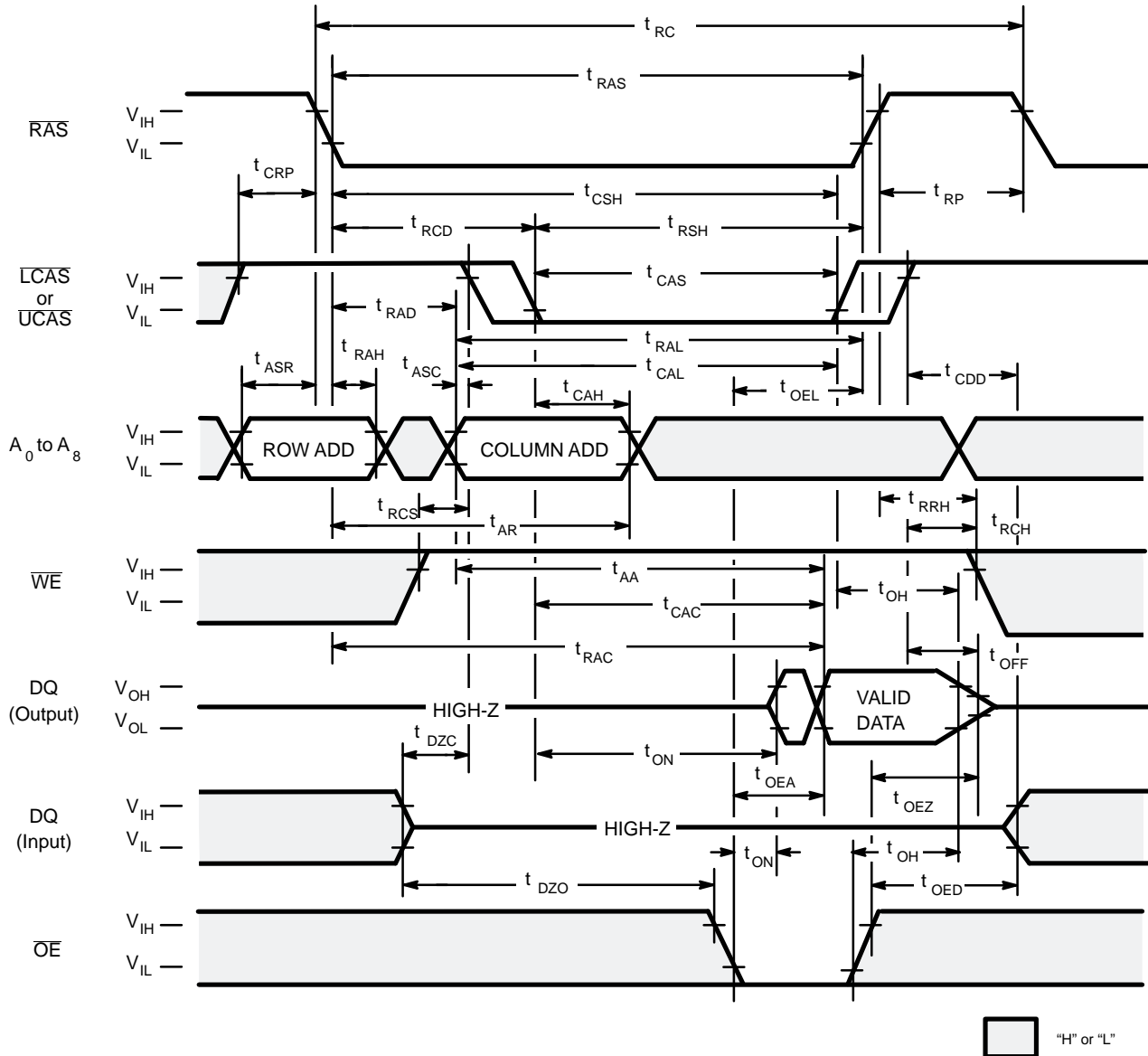
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input					Address		Input/Output Data				Refresh	Note
	RAS	LCAS	UCAS	WE	OE	Row	Column	DQ1 to DQ8		DQ9 to DQ16			
								Input	Output	Input	Output		
Standby	H	H	H	X	X	–	–	–	High-Z	–	High-Z	–	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	–	Valid High-Z Valid	–	High-Z Valid Valid	Yes. *	tRCS≥ tRCS (min.)
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid – Valid	High-Z	– Valid Valid	High-Z	Yes. *	tWCS≥ tWCS (min.)
Read-Modify- Write Cycle	L	L H L	H L L	H→L	L→H	Valid	Valid	Valid – Valid	Valid High-Z Valid	– Valid Valid	High-Z Valid Valid	Yes. *	
RAS-only Refresh Cycle	L	H	H	X	X	Valid	–	–	High-Z	–	High-Z	Yes.	
CAS-before-RAS Refresh Cycle	L	L	L	X	X	–	–	–	High-Z	–	High-Z	Yes.	tCSR≥ tCSR (min.)
Hidden Refresh Cycle	H→L	L H L	H L L	H	L	–	–	–	Valid High-Z Valid	–	High-Z Valid Valid	Yes.	Previous data is kept.

X; "H" or "L"

*; It is impossible in Fast Page Mode

Fig. 5 – READ CYCLE



DESCRIPTION

To implement a read operation, a valid address is latched in by the \overline{RAS} and \overline{LCAS} or \overline{UCAS} address strobes and with \overline{WE} set to a High level and \overline{OE} set to a low level, the output is valid once the memory access time has elapsed. \overline{LCAS} controls the input/output data on DQ1–DQ8 pins, \overline{UCAS} controls one on DQ8–DQ16 pins. The access time is determined by \overline{RAS} (t_{RAC}), $\overline{LCAS}/\overline{UCAS}$ (t_{CAC}), \overline{OE} (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

If $t_{RCD} > t_{RCD}(\text{max})$, access time = t_{CAC} .

If $t_{RAD} > t_{RAD}(\text{max})$, access time = t_{AA} .

If \overline{OE} is brought Low after t_{RAC} , t_{CAC} , or t_{AA} (whichever occurs later), access time = t_{OEA} .

However, if either $\overline{LCAS}/\overline{UCAS}$ or \overline{OE} goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

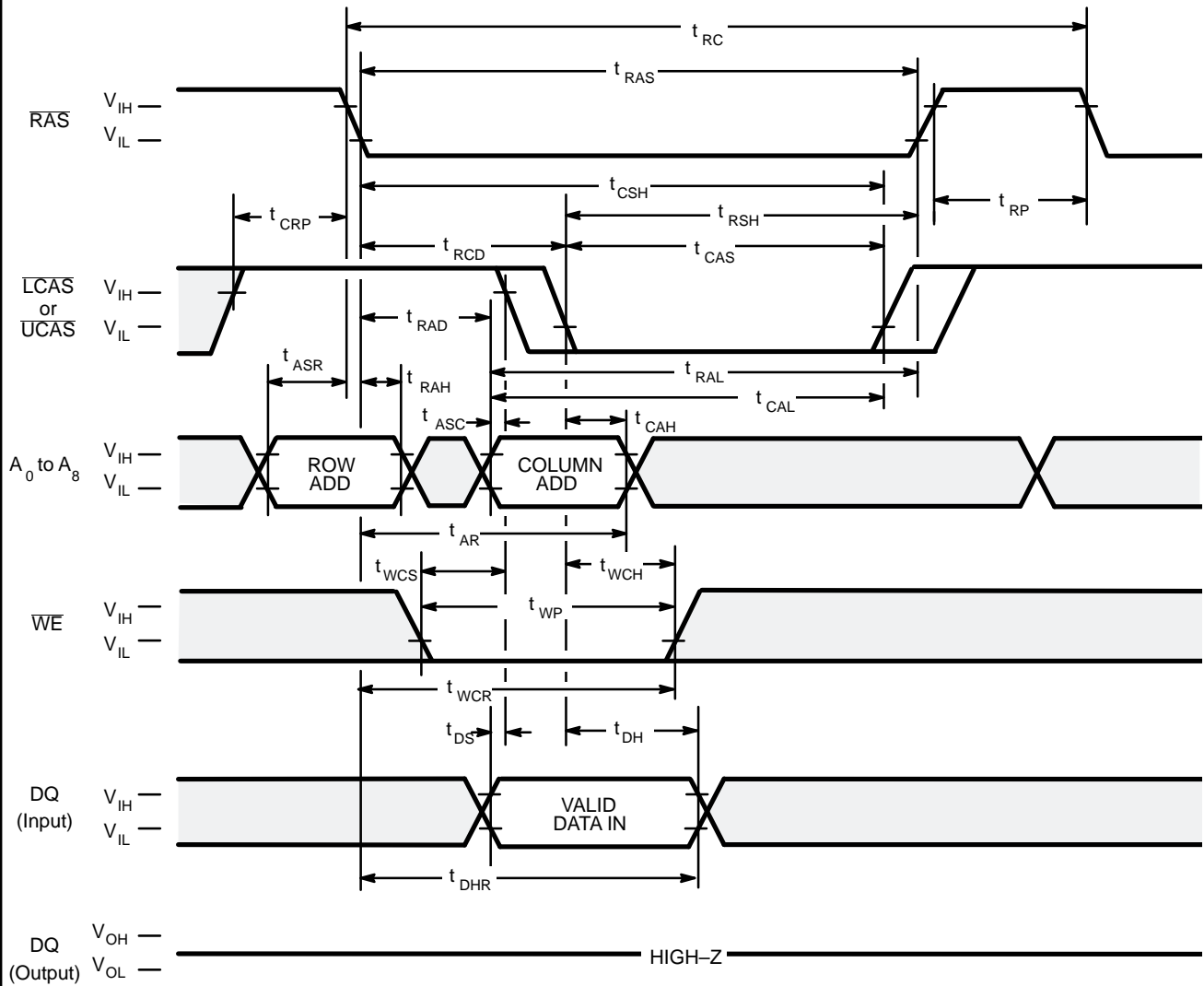
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MB81V4260S-60

MB81V4260S-70

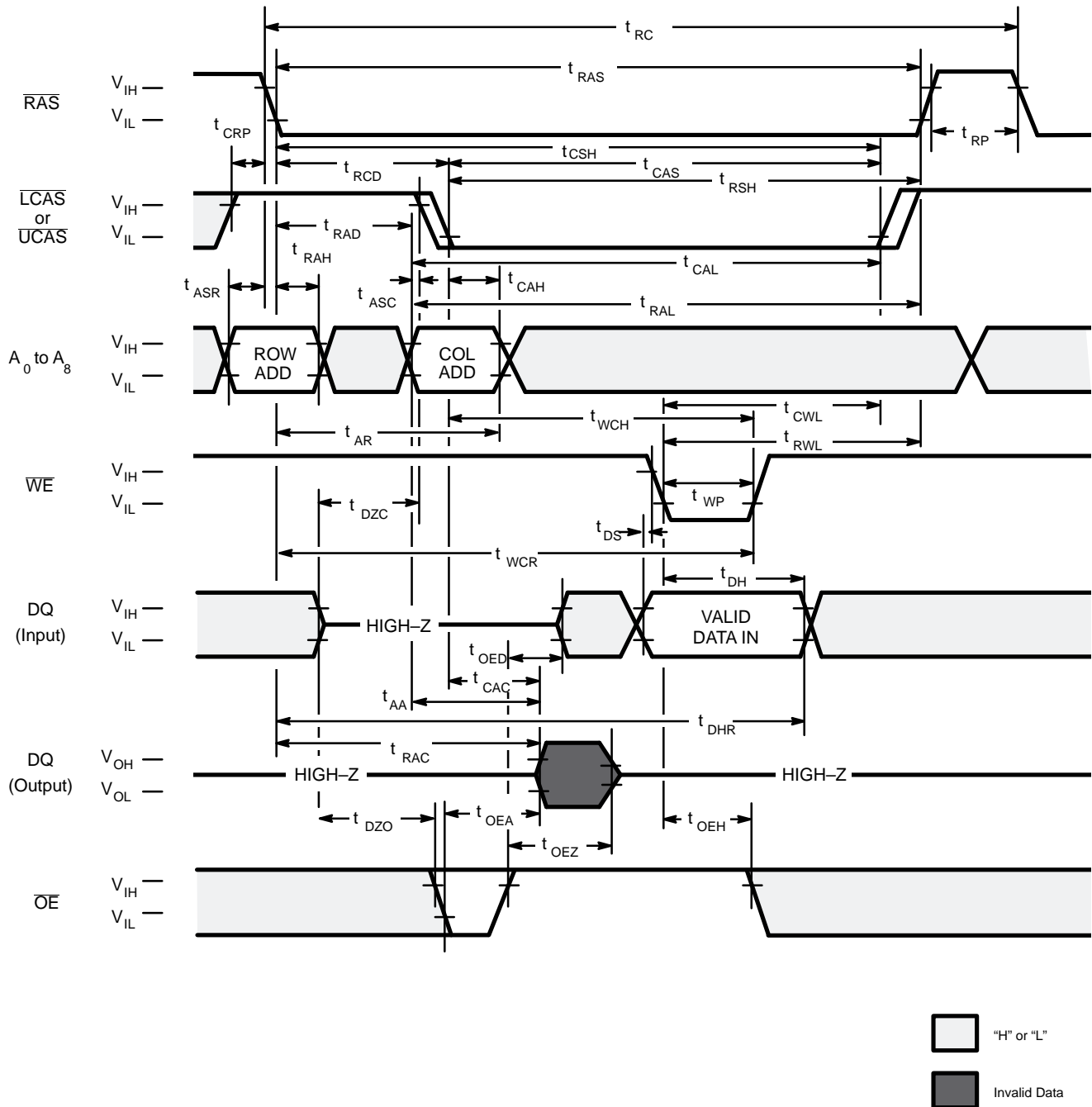
Fig. 6 – EARLY WRITE CYCLE (\overline{OE} ="H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except \overline{WE} is set to a Low state and \overline{OE} is an "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, \overline{OE} write (delayed write), or read-modify-write. During all write cycles, timing parameters t_{RWL} , t_{CWL} , t_{RAL} and t_{CAL} must be satisfied. In the early write cycle shown above t_{WCS} is satisfied, data on the DQ pins are latched with the falling edge of \overline{LCAS} or \overline{UCAS} and written into memory.

Fig. 7 – \overline{OE} (DELAYED WRITE) CYCLE



DESCRIPTION

In the \overline{OE} (delayed write) cycle, t_{WCS} is not satisfied ; thus, the data on the DQ pins is latched with the falling edge of \overline{WE} and written into memory. The Output Enable (\overline{OE}) signal must be changed from Low to High before \overline{WE} goes Low ($t_{OED} + t + t_{DS}$).

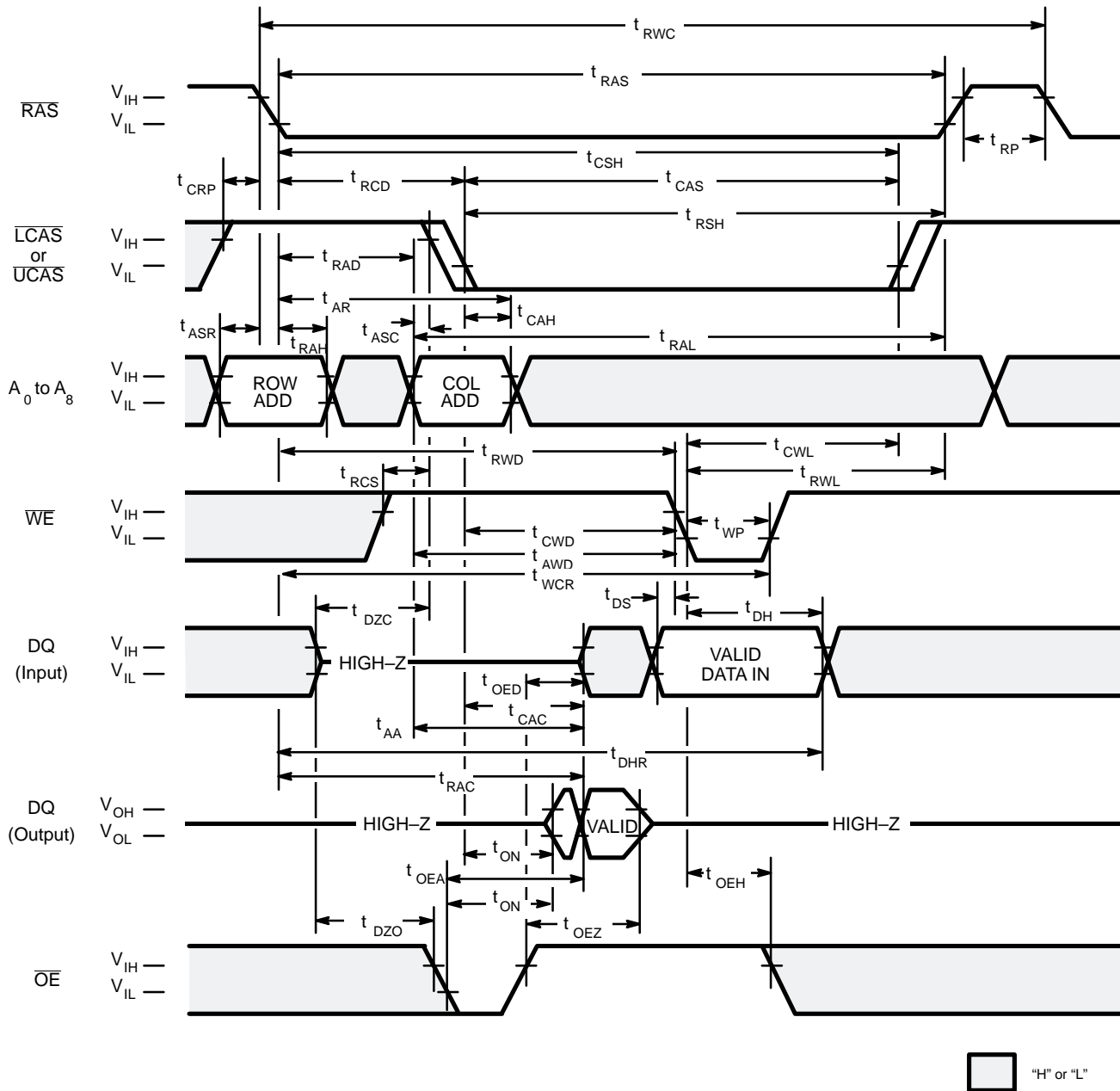
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MB81V4260S-60

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Fig. 8 – READ-MODIFY-WRITE-CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing \overline{WE} from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, \overline{OE} must be changed from Low to High after the memory access time.

MB81V4260S-70

The timing diagram illustrates the relationship between several control and data signals for the 16M1602 LCD module. The signals and their associated timing parameters are as follows:

- RAS:** Row Address Strobe. Timing parameters include t_{RCD} (Row Address Setup), t_{RAD} (Row Address Hold), t_{RASP} (Row Address Pulse Width), t_{RHCP} (Row Address Precharge), and t_{RP} (Row Address Return to High-Z).
- LCAS or UCAS:** Column Address Strobe or Update Command Strobe. Timing parameters include t_{CRP} (Column Address Setup), t_{PC} (Column Address Precharge), t_{CP} (Column Address Pulse Width), t_{CAS} (Column Address Setup), t_{RSH} (Column Address Return to High-Z), and t_{RP} (Column Address Return to High-Z).
- A_0 to A_8 :** Address bus. Timing parameters include t_{ASR} (Address Setup), t_{RAH} (Address Return to High-Z), t_{ASC} (Address Setup), t_{CAH} (Column Address Hold), t_{CDD} (Column Address Delay), t_{CAL} (Column Address Load), t_{ASC} (Address Setup), t_{RAL} (Row Address Load), t_{RRH} (Row Address Return to High-Z), t_{RCS} (Row Address Setup), t_{AR} (Address Return), t_{RCH} (Row Address Hold), and t_{RCH} (Row Address Hold).
- WE:** Write Enable. Timing parameters include t_{DZC} (Data ZC), t_{ON} (Write Enable On), t_{DZC} (Data ZC), t_{CPA} (Write Enable Precharge), t_{DZC} (Data ZC), t_{CDD} (Write Enable Delay), t_{DZC} (Data ZC), t_{OEL} (Write Enable Load), and t_{DZC} (Data ZC).
- DQ (Input):** Data bus input. Timing parameters include t_{DZO} (Data ZC), t_{OH} (Data Output Hold), t_{CAC} (Data Input Setup), t_{RAC} (Data Input Return to High-Z), t_{OFF} (Data Input Off), t_{ON} (Data Input On), t_{OFF} (Data Input Off), and t_{DZO} (Data ZC).
- DQ (Output):** Data bus output. Timing parameters include t_{AA} (Data Output Setup), t_{OEZ} (Data Output ZC), t_{OEA} (Data Output Setup), t_{OEZ} (Data Output ZC), t_{OH} (Data Output Hold), and t_{OED} (Data Output Delay).
- \overline{OE} :** Output Enable. Timing parameters include t_{ON} (Output Enable On), t_{OH} (Output Hold), and t_{OED} (Output Delay).

- "H" or "L"
- ▨ Valid Data

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{\text{RAS}}$ at a Low level and $\overline{\text{WE}}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by tCAC, tAA, tCPA, or tOEA, whichever one is the latest in occurring.

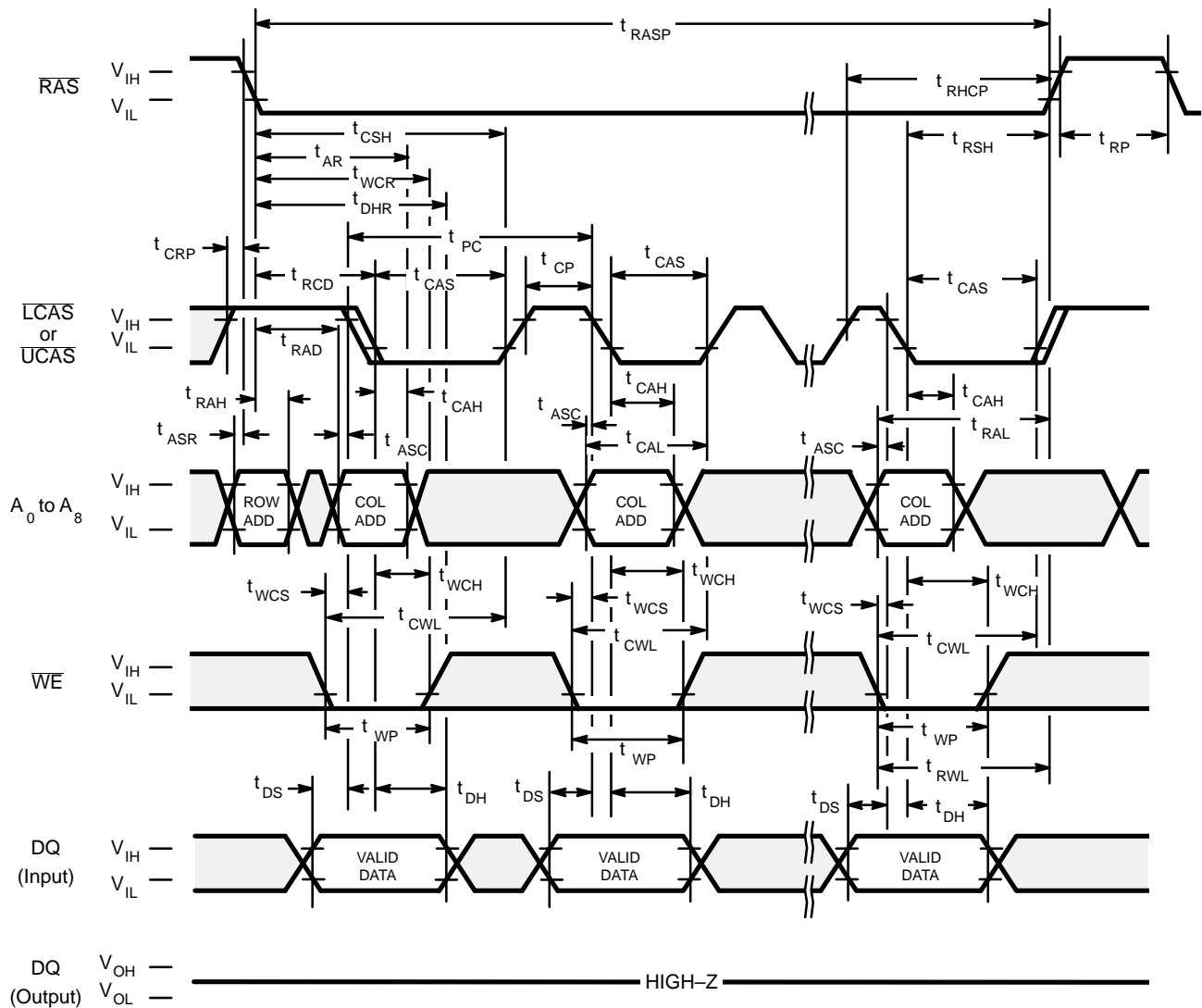
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MB81V4260S-70



Fig. 10 – FAST PAGE MODE WRITE CYCLE (\overline{OE} ="H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of \overline{WE} and \overline{OE} are reversed. Data appearing on the DQ1 to DQ8 is latched on the falling edge of LCAS and one appearing on the DQ9 to DQ16 is latched on the falling edge of UCAS and the data is written into the memory. During the fast page mode write cycle, including the delayed (\overline{OE}) write and read-modify-write cycles, t_{CWL} must be satisfied.

MB81V4260S-70

 "H" or "L"
 Invalid Data

The fast page mode $\overline{\text{OE}}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{\text{WE}}$ and $\overline{\text{OE}}$. Input data on the DQ pins are latched on the falling edge of $\overline{\text{WE}}$ and written into memory. In the fast page mode delayed write cycle, $\overline{\text{OE}}$ must be changed from Low to High before $\overline{\text{WE}}$ goes Low ($t_{\text{OED}} + t_{\text{T}} + t_{\text{DS}}$).

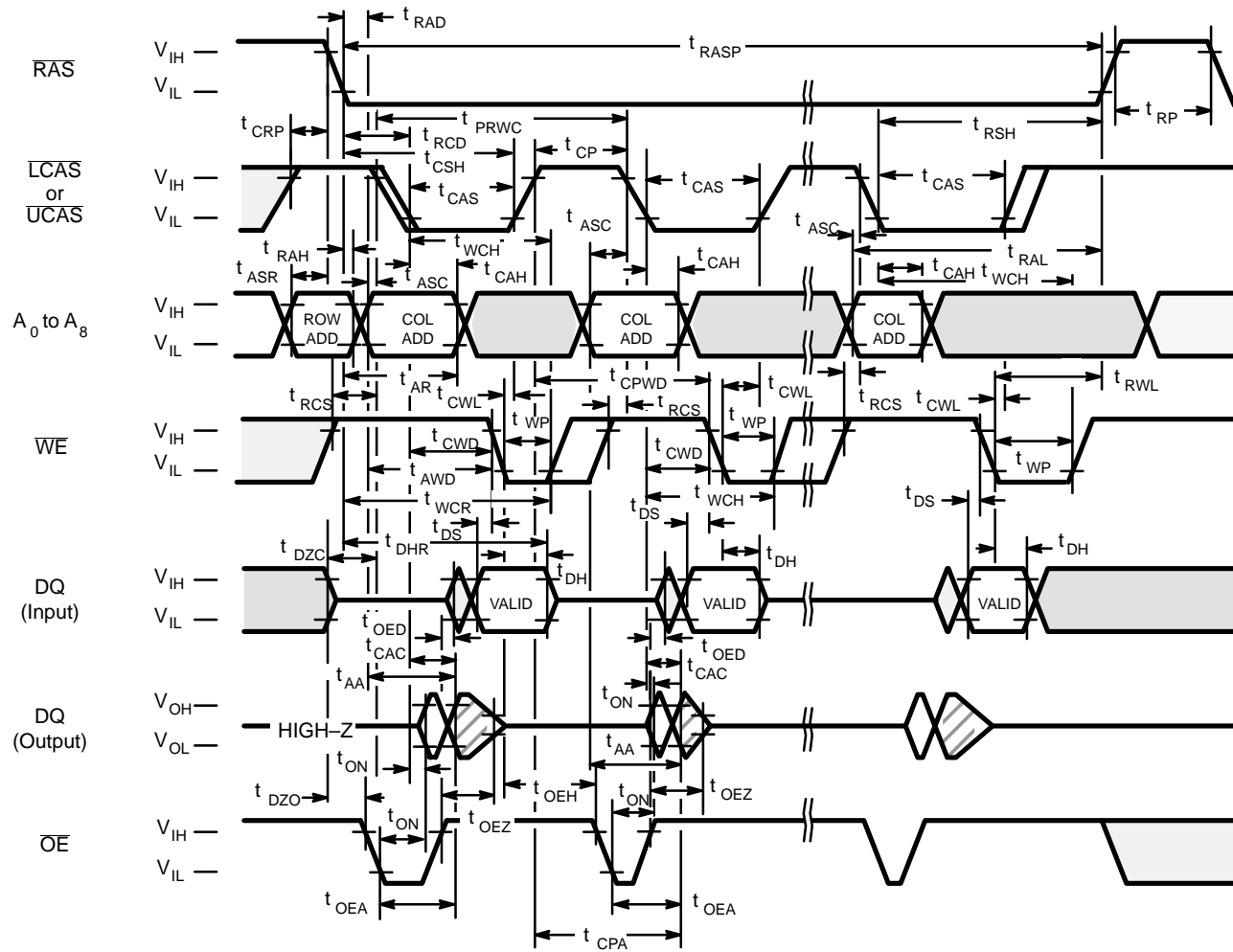
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MB81V4260S-70

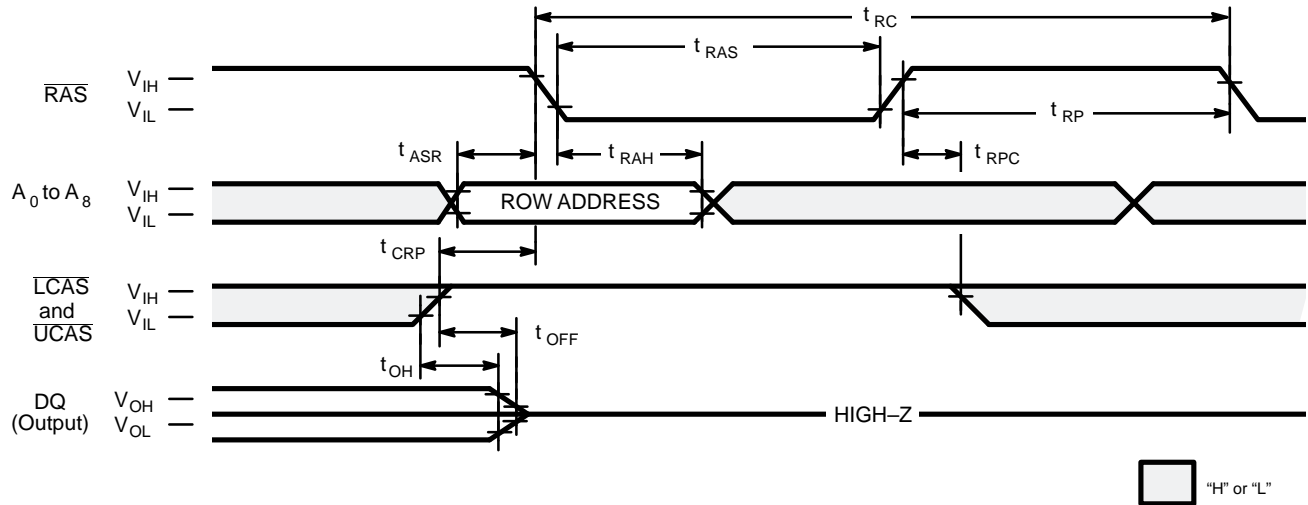
Fig. 12 – FAST PAGE MODE READ-MODIFY-WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read-modify-write cycle can be executed by switching $\overline{\text{WE}}$ from High to Low after input data appears at the DQ pins during a normal cycle.

Fig. 13 – $\overline{\text{RAS}}$ -ONLY REFRESH ($\overline{\text{WE}} = \overline{\text{OE}} = \text{"H"}$ or "L")

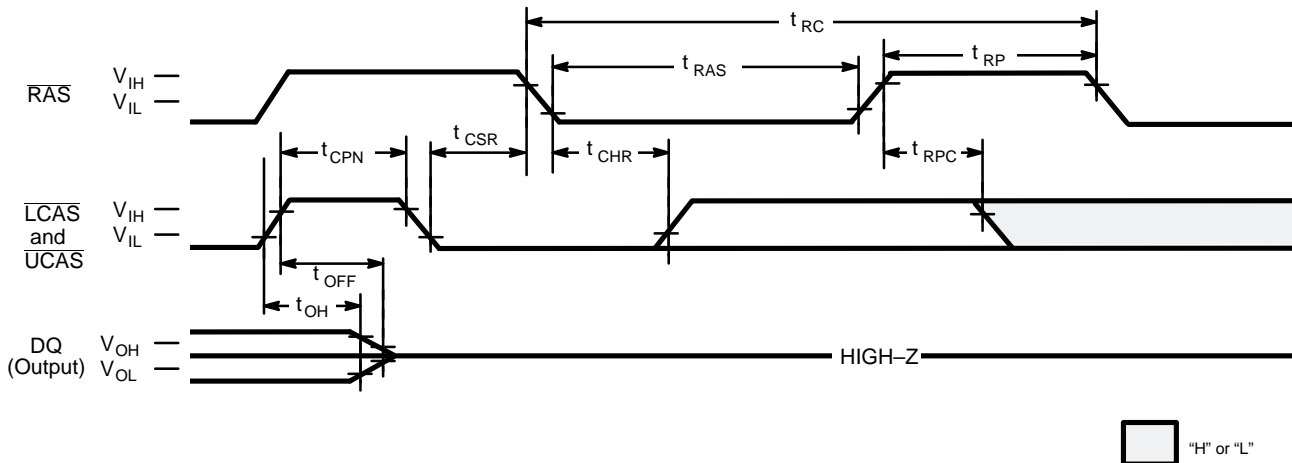


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available: $\overline{\text{RAS}}$ -only refresh, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, and hidden refresh.

$\overline{\text{RAS}}$ -only refresh is performed by keeping $\overline{\text{RAS}}$ Low and $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$ -only refresh, DQ pins are kept in a high-impedance state.

Fig. 14 – $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH (ADDRESSES = $\overline{\text{WE}} = \overline{\text{OE}} = \text{"H"}$ or "L")



DESCRIPTION

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ is held Low for the specified setup time (t_{CSR}) before $\overline{\text{RAS}}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh operation.

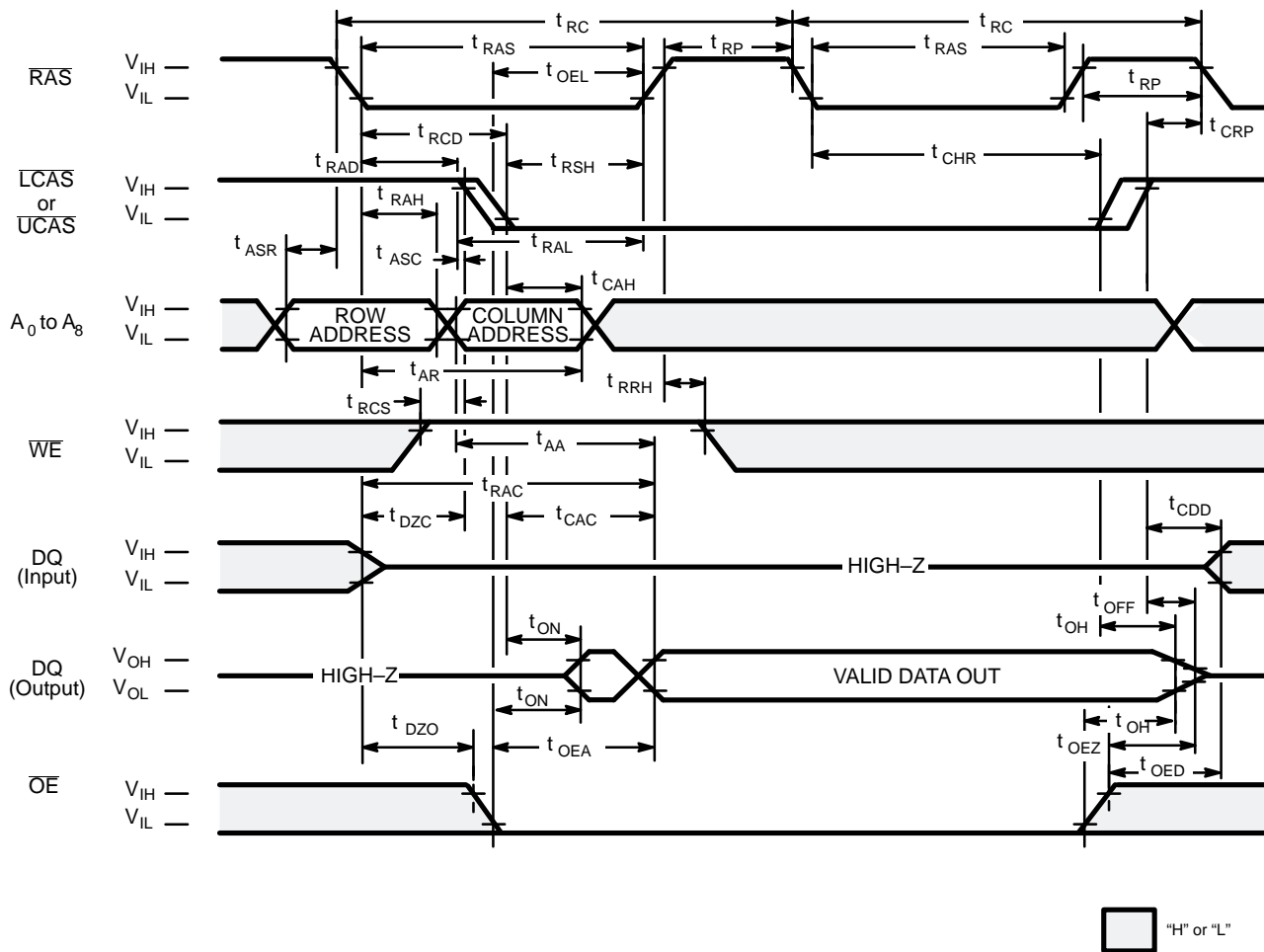
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Edition 2.0

MB81V4260S-60

MB81V4260S-70

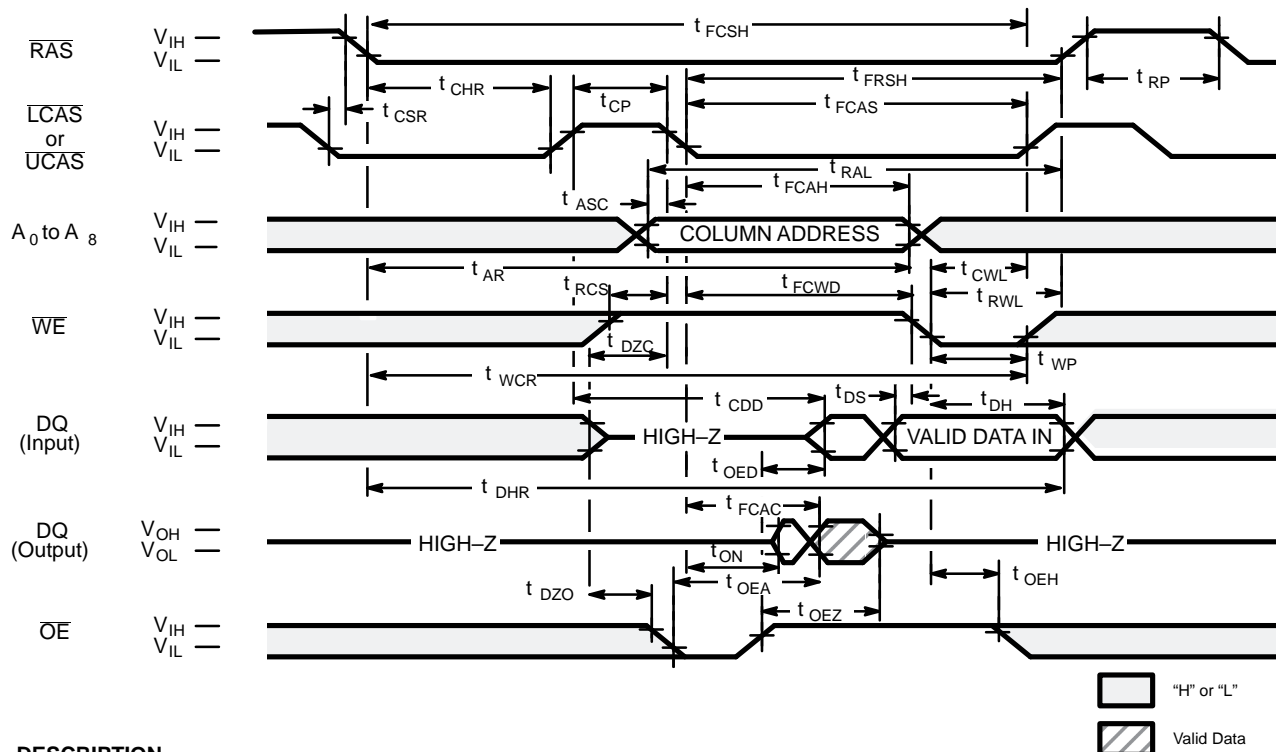
Fig. 15 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of LCAS or UCAS and cycling RAS. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have CAS-before-RAS refresh capability.

Fig. 16 – $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh circuitry. After a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle, if $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ makes a transition from High to Low while $\overline{\text{RAS}}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.

Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$.

The $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test procedure is as follows :

- 1) Normalize the internal refresh address counter by using 8 $\overline{\text{RAS}}$ only refresh cycles.
- 2) Use the same column address throughout the test.
- 3) Write "0" to all 512 row addresses at the same column address by using CBR refresh counter test cycles.
- 4) Read "0" written in procedure 3) by using normal read cycle and check; After reading "0" and check are completed (or simultaneously), write "1" to the same addresses by using normal write cycle (or read-modify-write cycle).
- 5) Read and check data "1" written in procedure 4) by using CBR refresh counter test cycle for all 512 memory locations.
- 6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V4260S-60		MB81V4260S-70		Unit
			Min	Max	Min	Max	
90	Access Time from $\overline{\text{CAS}}$	t_{FCAC}	—	55	—	55	ns
91	Column Address Hold Time	t_{FAH}	30	—	30	—	ns
92	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{FCWD}	80	—	80	—	ns
93	$\overline{\text{CAS}}$ Pulse width	t_{FCAS}	55	—	55	—	ns
94	$\overline{\text{RAS}}$ Hold Time	t_{FRSH}	55	—	55	—	ns
95	$\overline{\text{CAS}}$ Hold Time	t_{FCSH}	85	—	85	—	ns

Note. Assumes that $\overline{\text{CAS-before-RAS}}$ refresh counter test cycle only.

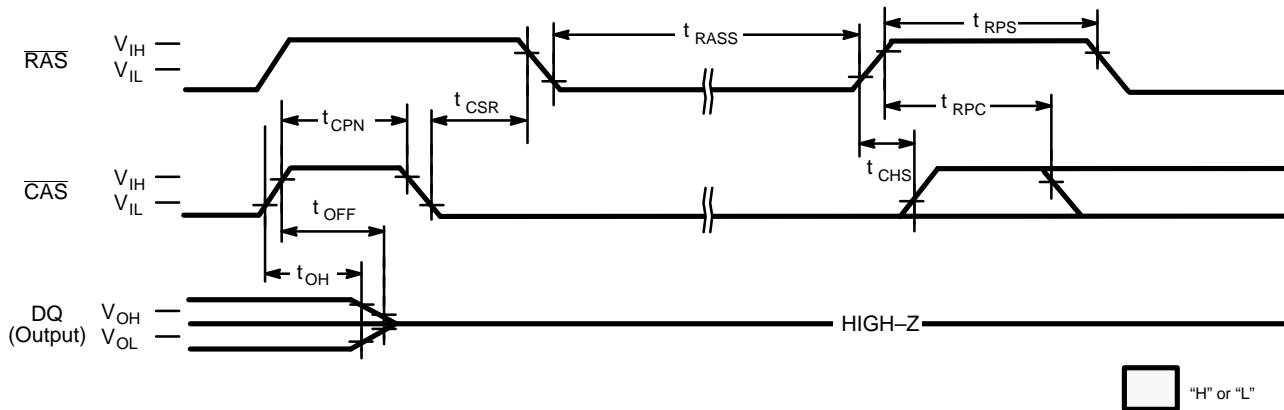
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Edition 2.0

MB81V4260S-60

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Fig. 17 – SELF REFRESH CYCLE ($A0-A9 = \overline{WE} = \overline{OE} = "H" \text{ or } "L"$)



(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V4260S-60		MB81V4260S-70		Unit
			Min	Max	Min	Max	
100	RAS Pulse Width	t_{RASS}	100	—	100	—	ns
101	RAS Precharge Time	t_{RPS}	110	—	125	—	ns
102	CAS Hold Time	t_{CHS}	-50	—	-50	—	ns

Note . Assumes that Self refresh cycles only.

DESCRIPTION

The self refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the self refresh cycle and refresh operation can be automatically executed using internal refresh address counter.

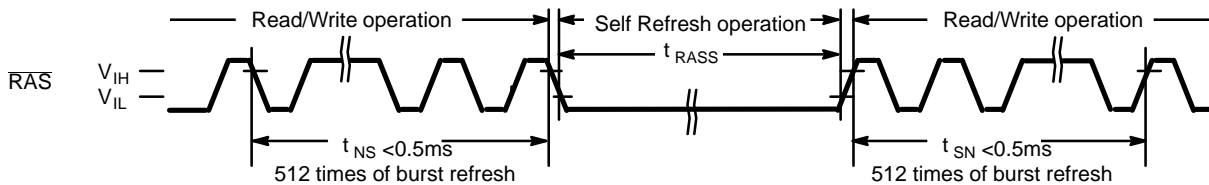
If /CAS goes to "L" before /RAS goes to "L" (CBR) and the condition of /CAS "L" and /RAS "L" is kept for term of t_{RASS} (more than 100 μ s), the device can be entered the self refresh cycle. And after that, refresh operation is automatically executed per fixed interval using internal refresh address counter during "/RAS=L" and "/CAS=L".

And exit from self refresh cycle is performed by toggling of /RAS and /CAS to "H" with specifying t_{CHS} min.

Restruction for Self refresh operation ;

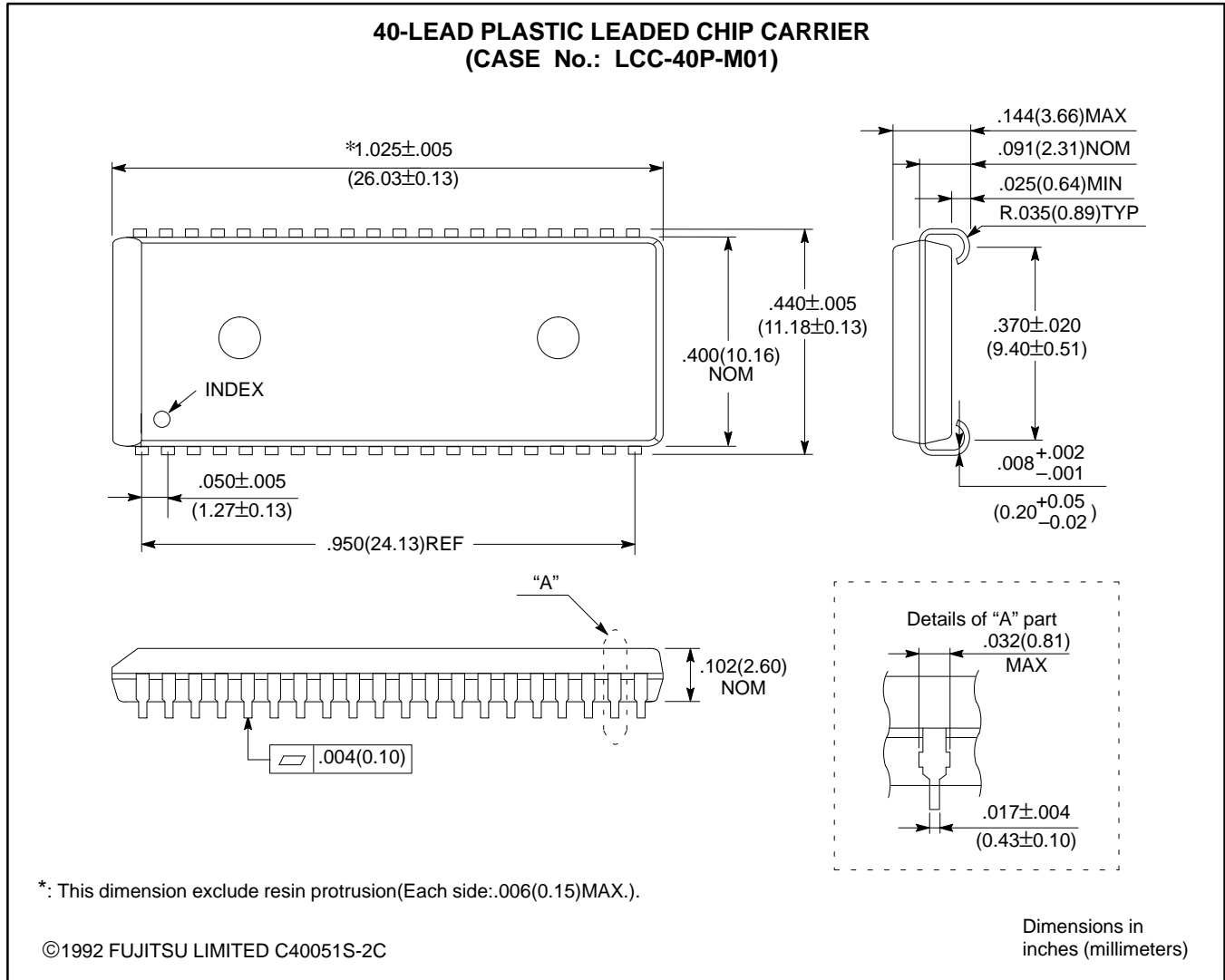
For self refresh operation, the notice below must be considered.

- 1) In the case that distribut CBR refresh are operated in read/write cycles
Self refresh cycles can be executed without special rule if 512 cycles of distribut CBR refresh are executed within t_{REF} max..
- 2) In the case that burst CBR refresh or /RAS only refresh are operated in read/write cycles
512 times of burst CBR refresh or 512 times of burst /RAS only refresh must be executed before and after Self refresh cycles.



PACKAGE DIMENSIONS

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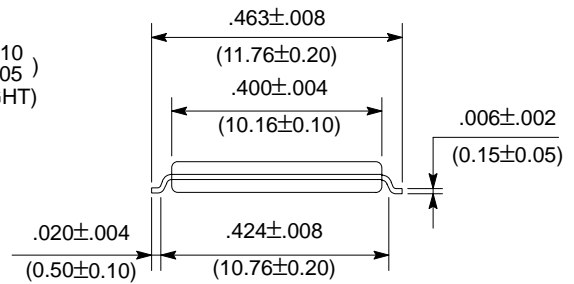
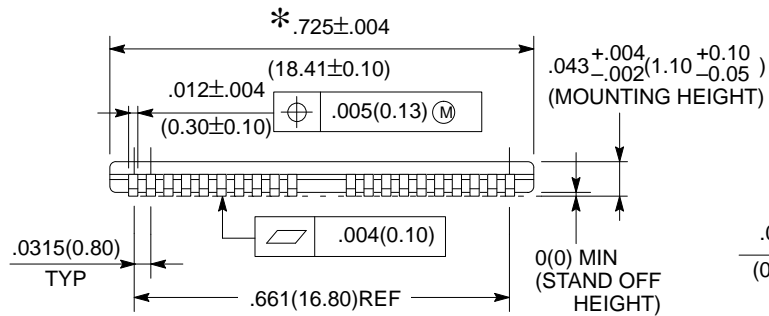
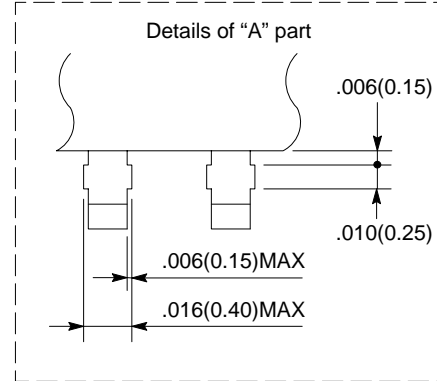
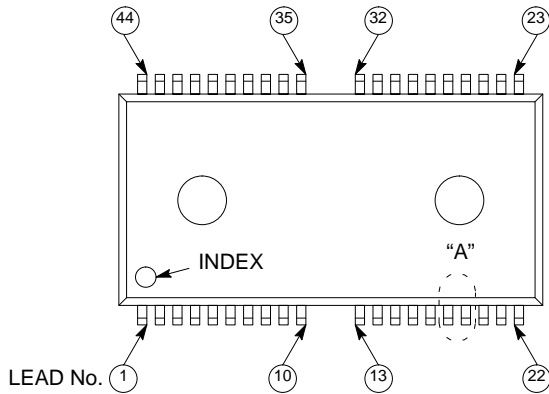
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Edition 2.0

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(Suffix : -PFTN)

44-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-44P-M07)



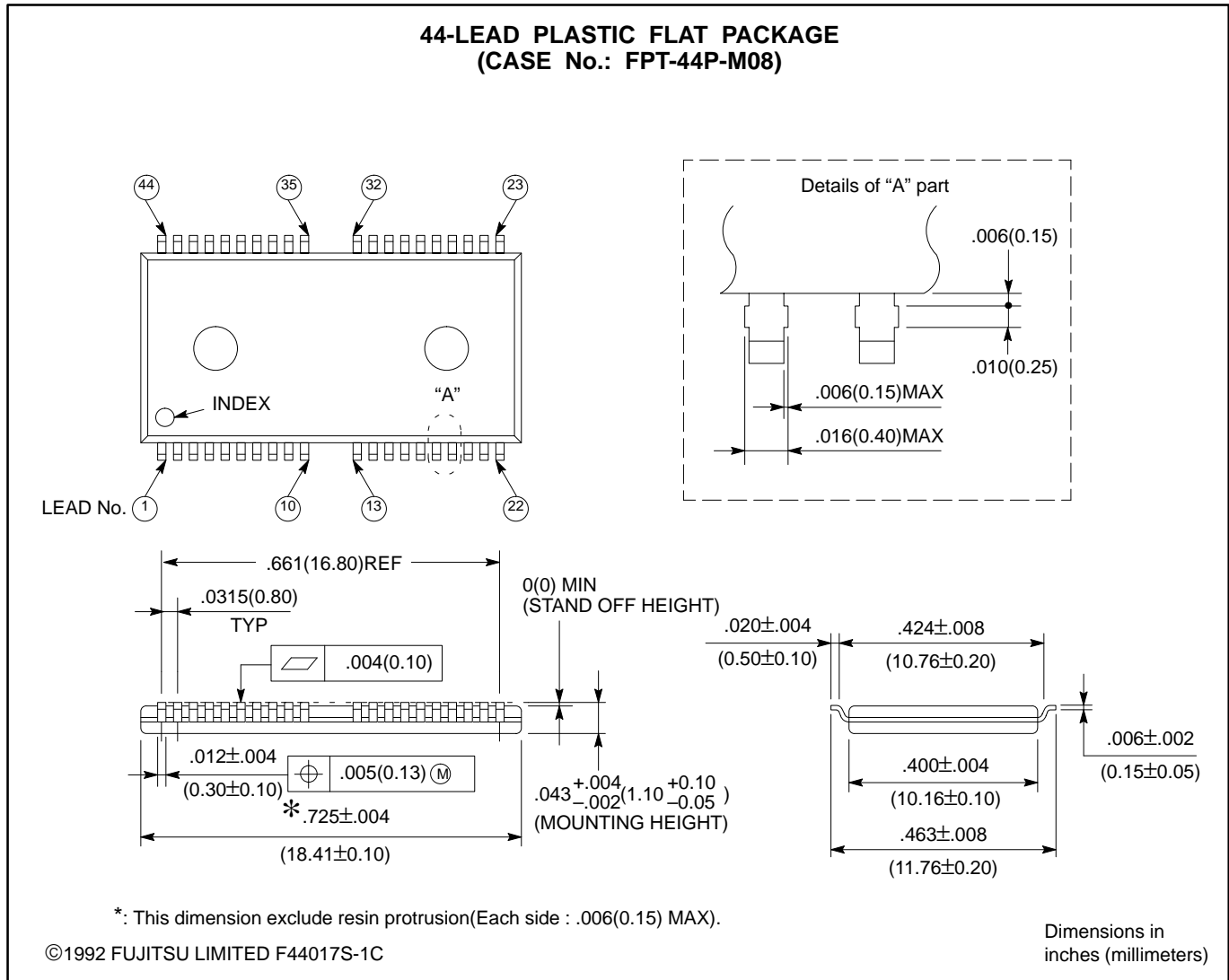
*: This dimension exclude resin protrusion(Each side : .006(0.15) MAX).

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Dimensions in
inches (millimeters)

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