

DORADO SCHEMATICS

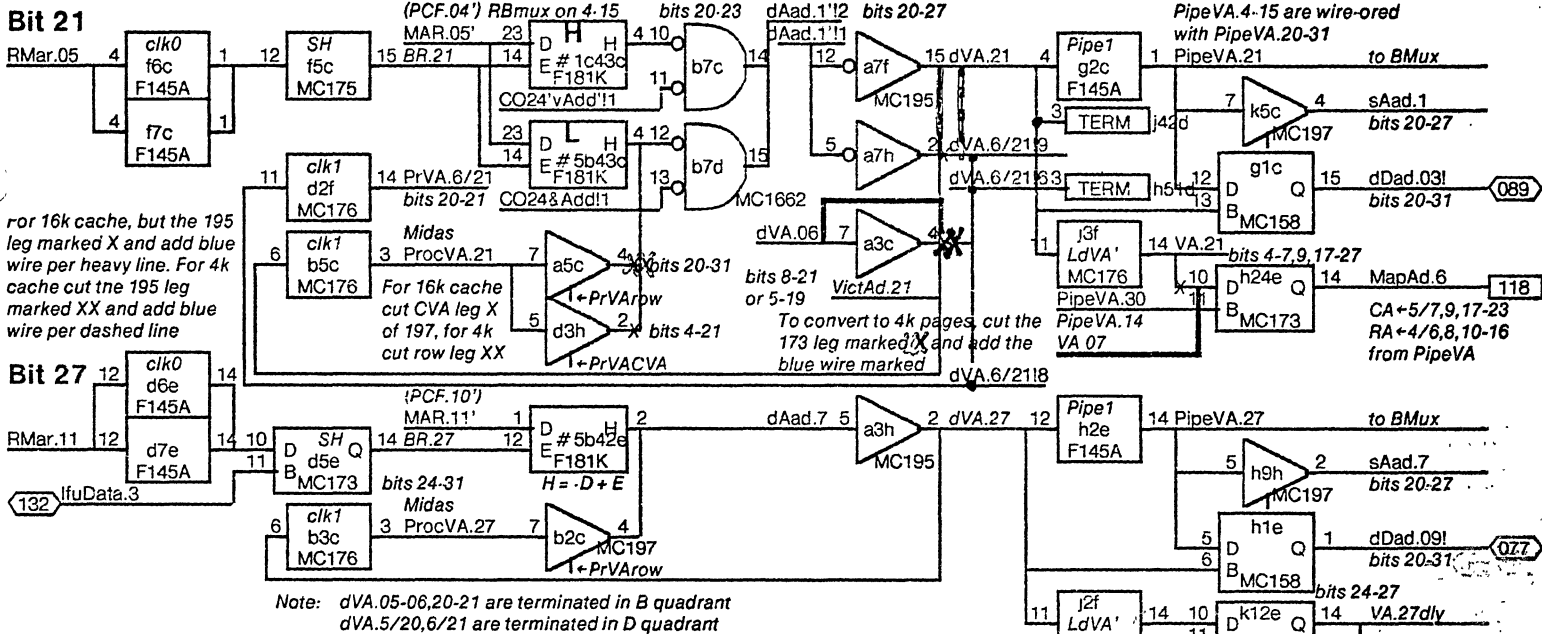
Memory Control

TESTING MEM C WITHOUT MEM X
 GROUND PINS 122 102 35 MDM TAG
 WITH NO IFU GND. 131
(130)

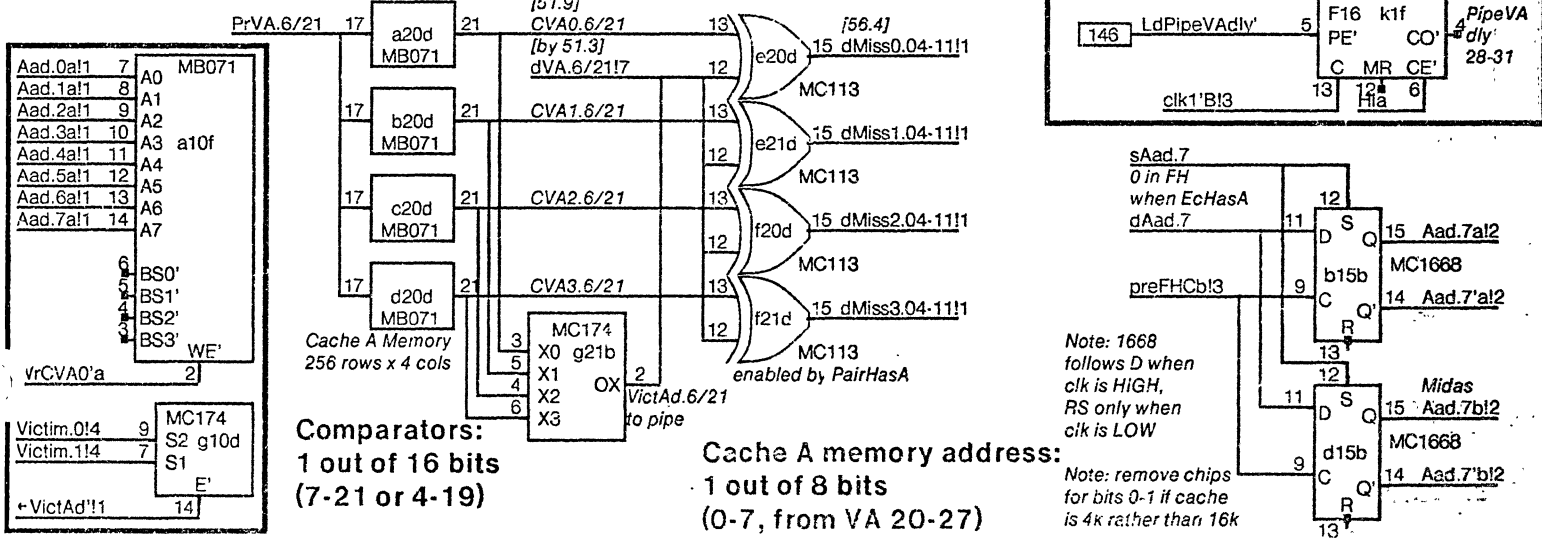
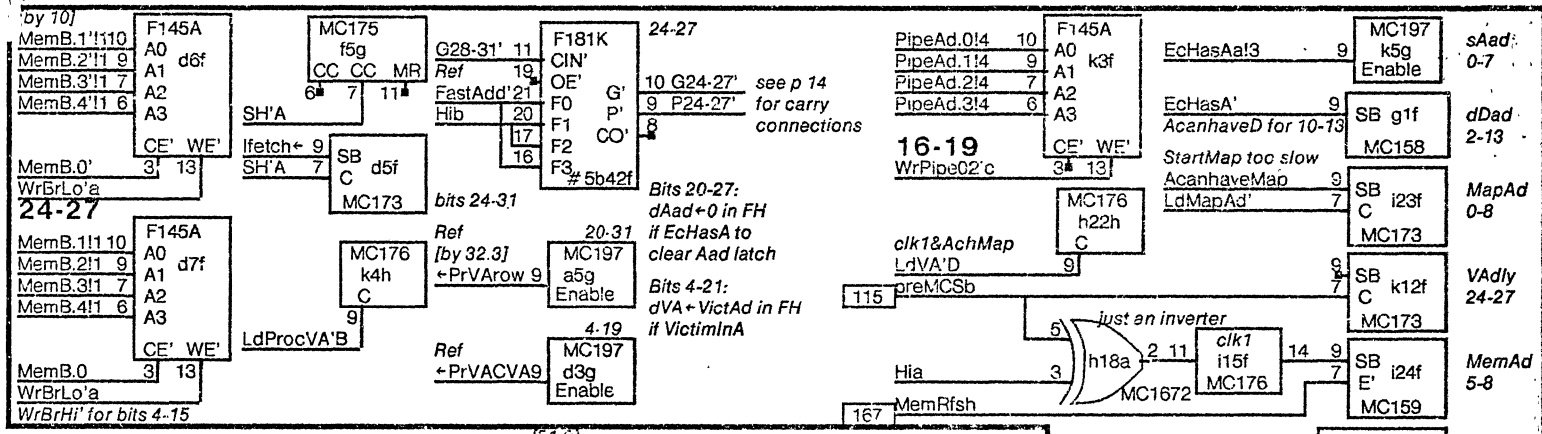
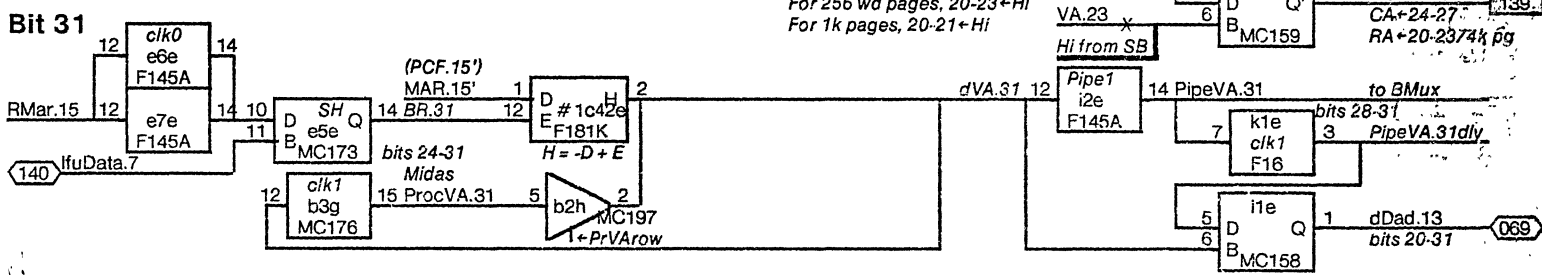
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SIMTEST WILL SHOW

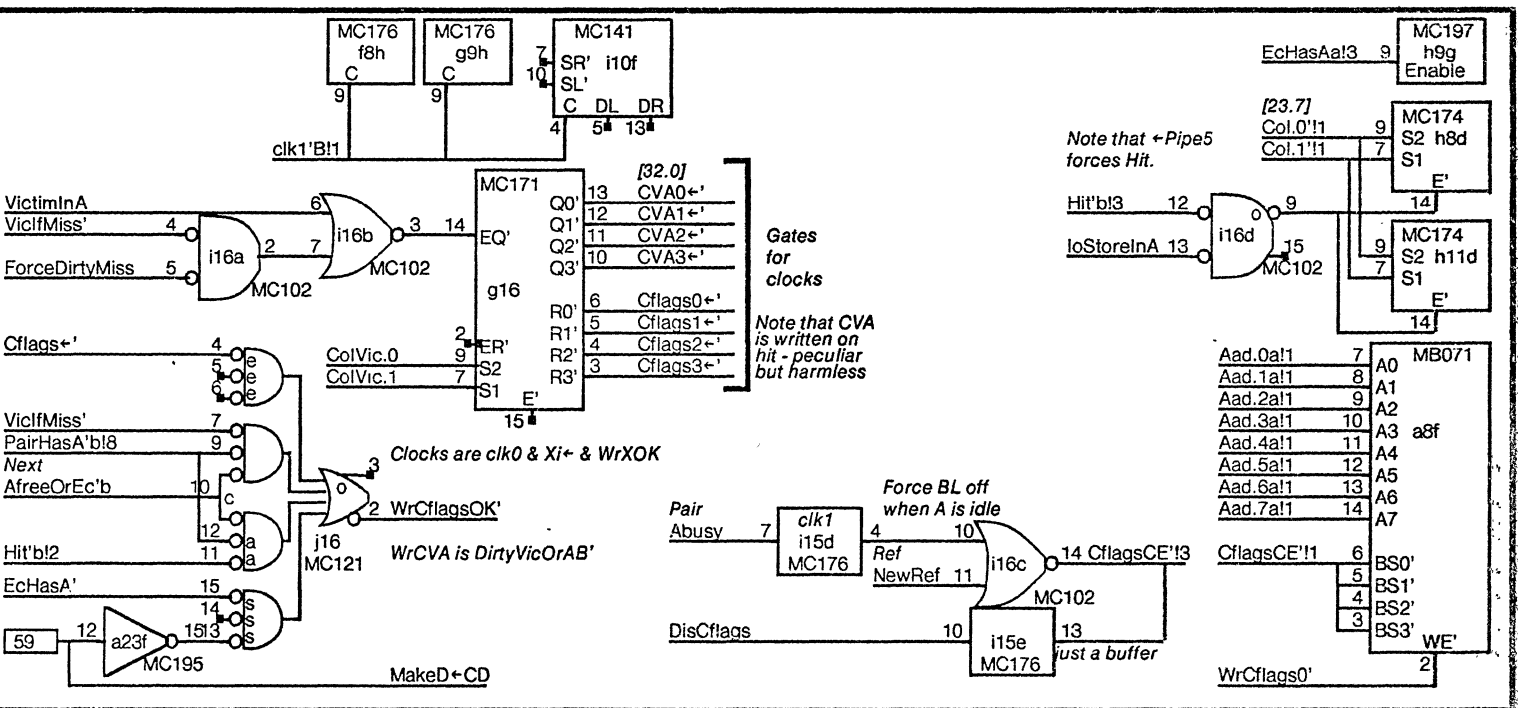
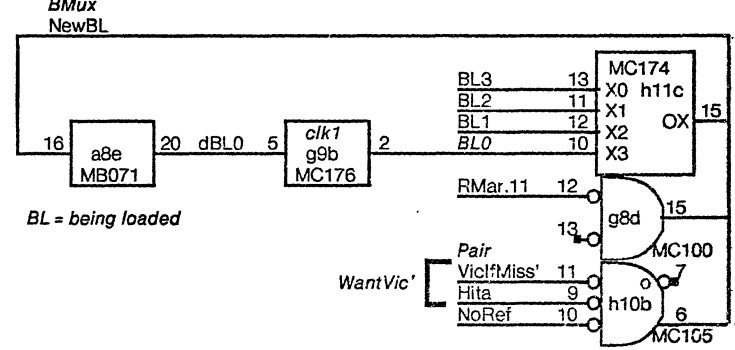
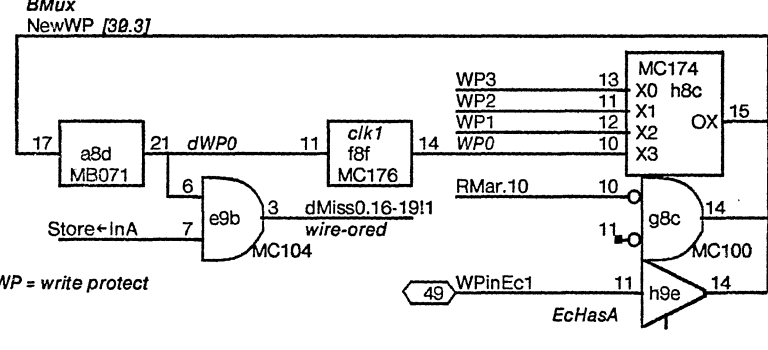
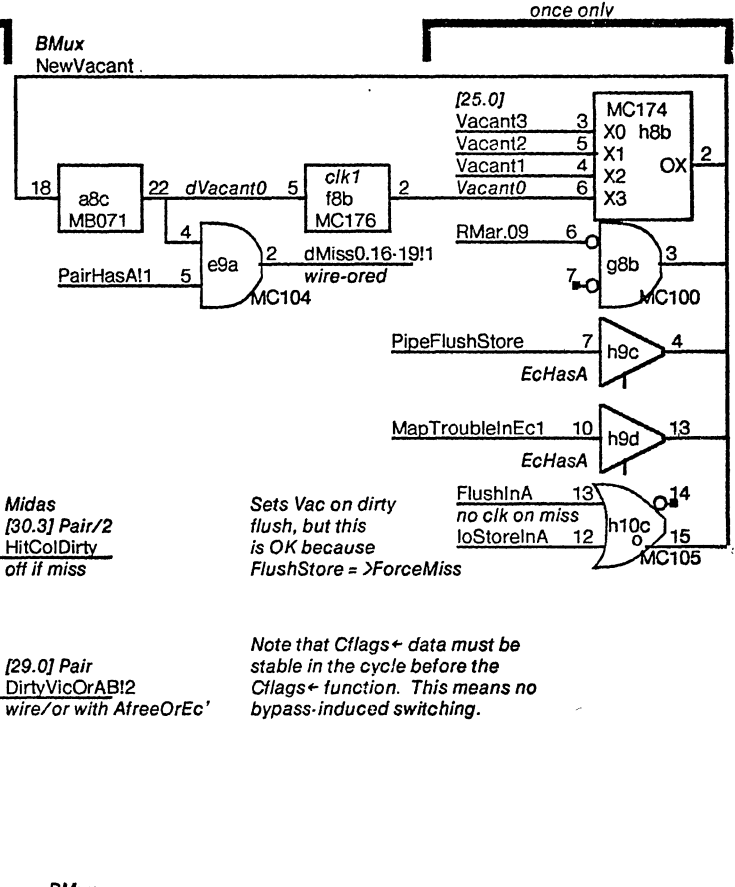
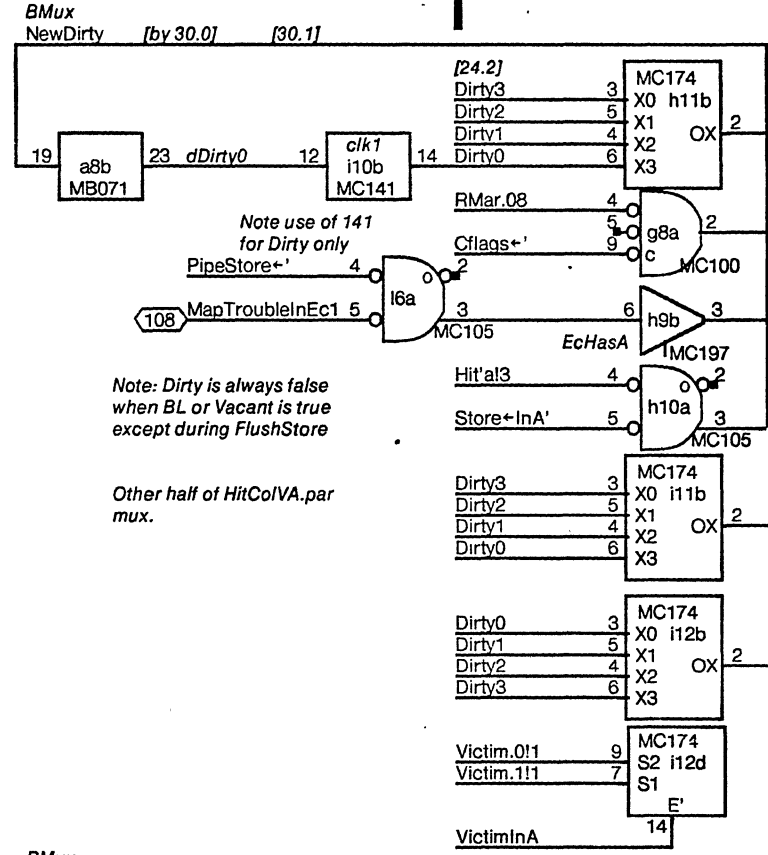
	<u>TITLE</u>	<u>Page</u>
Data paths <small>complete except for repetitions of address bits</small>	Main data path bits 21,27,31; A address bit 7; _____	01
	A memory and comparator bit 6	
	Cache flags, column 0 and common _____	02
	Cache flags, columns 1-3 _____	03
	Victim and next victim _____	04
	Cache A parity, control pipe, Mcr _____	05
	Mar and BMux drivers and receivers _____	06
Bit slices <small>for address bits</small>	Main data paths, bits 04-11 _____	07
	12-19 _____	08
	20-25 _____	09
	26-31 _____	10
	Cache A memory and comparators, bits 04-11 _____	11
	12-19 _____	12
	Cache A memory addressing _____	13
	Pipe and BR addressing; _____	14
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	Ref decoding _____	16
	Pair _____	17
	Next _____	18
	FF decoding _____	19
	Midas control and multiplexors _____	20
	Clock distribution _____	21
	Layout _____	22
	Loading Information _____	23
	Multiwire rev changes _____	24

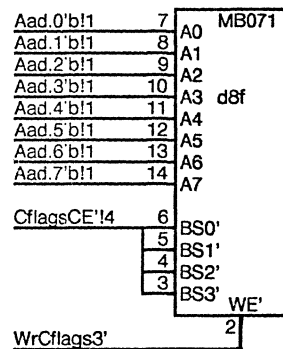
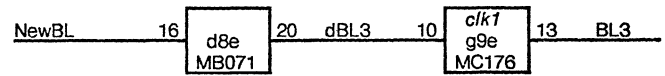
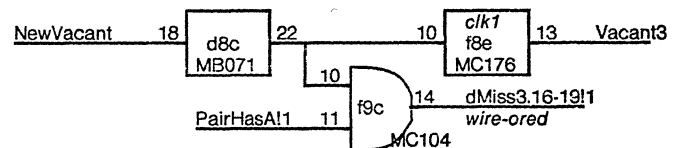
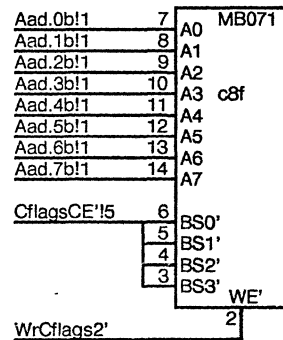
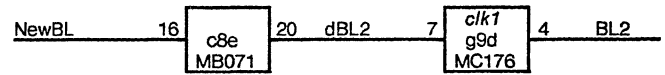
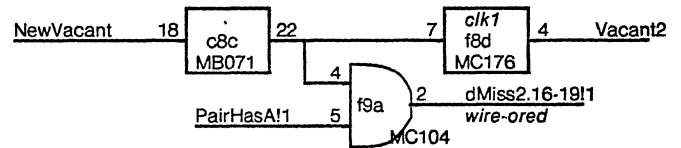
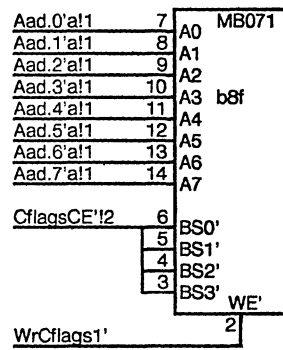
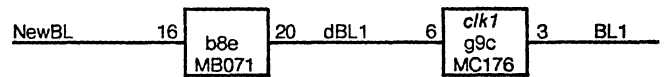
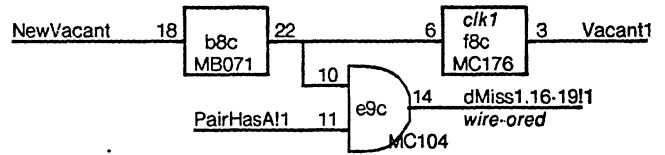
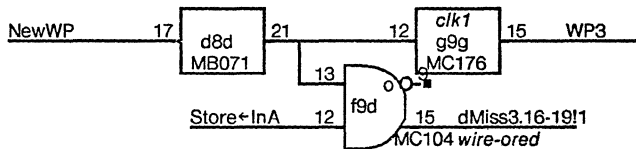
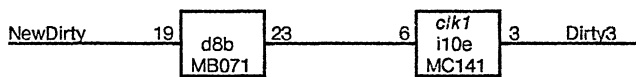
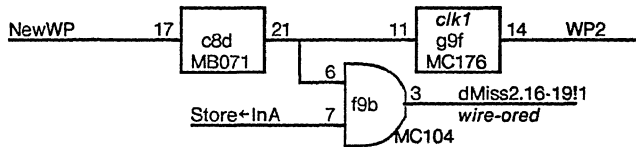
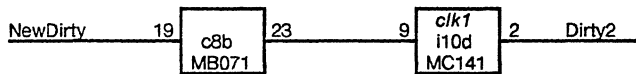
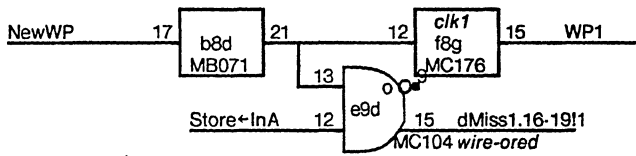
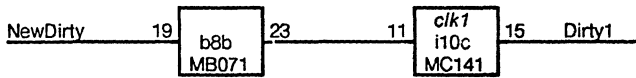


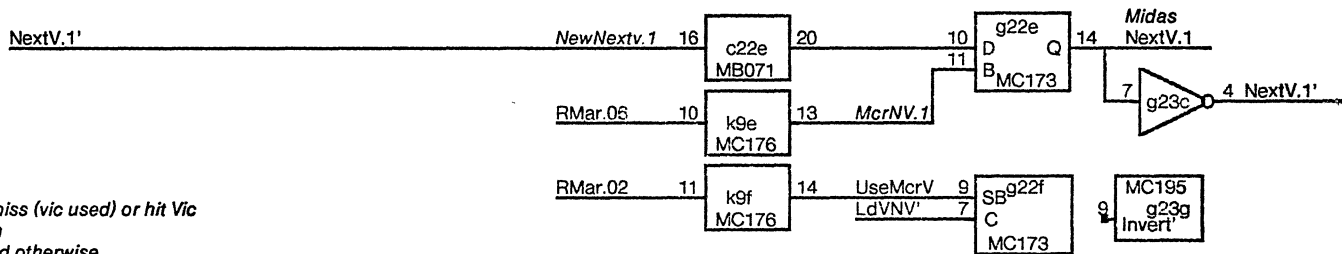
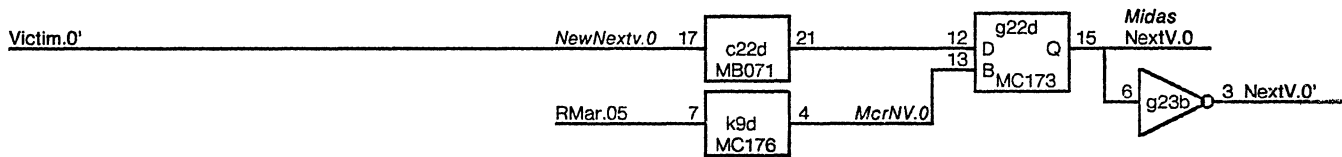
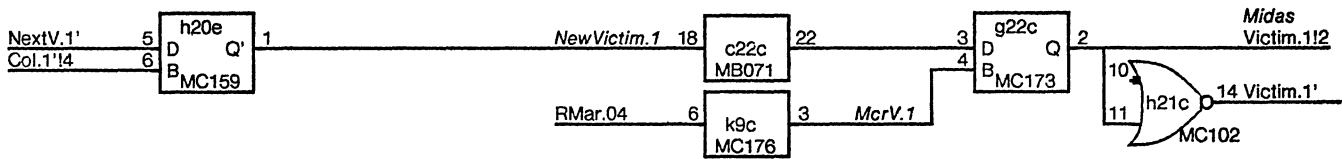
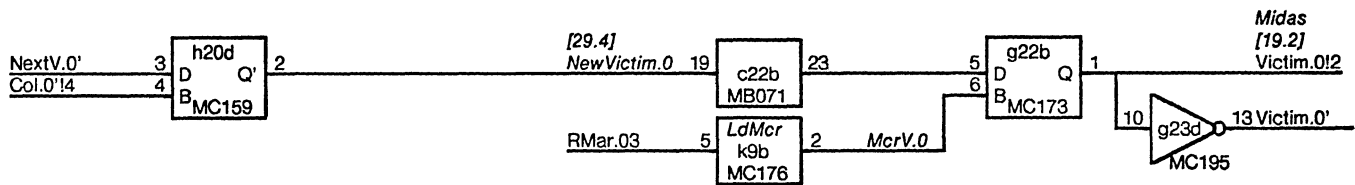
**Main data path:
3 out of 28 bits (4-31)**



Cols 0..3

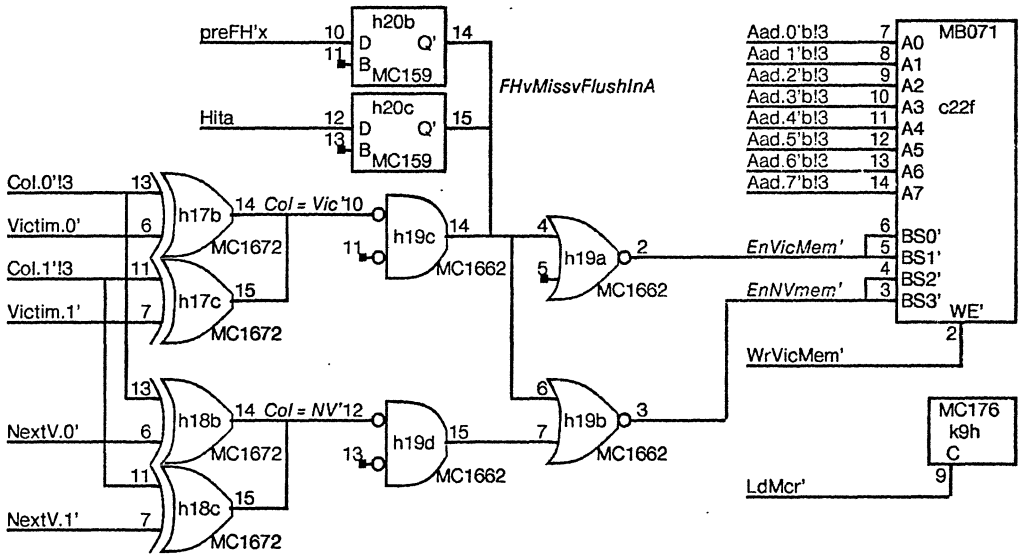






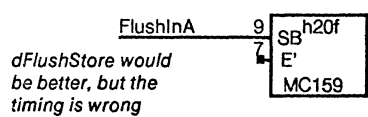
New Vic+ old NV if miss (vic used) or hit Vic
Col if flush
unchanged otherwise

New NV+ something not = old Vic or old NV if miss or hit Vic (NV used) or hit NV
unchanged otherwise (except for flush, which is an accident, not important)

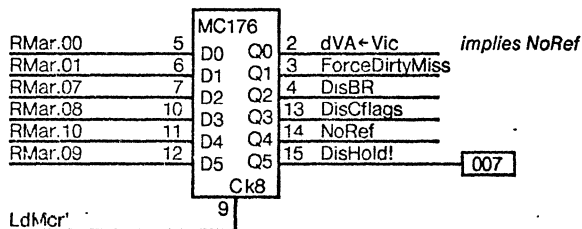
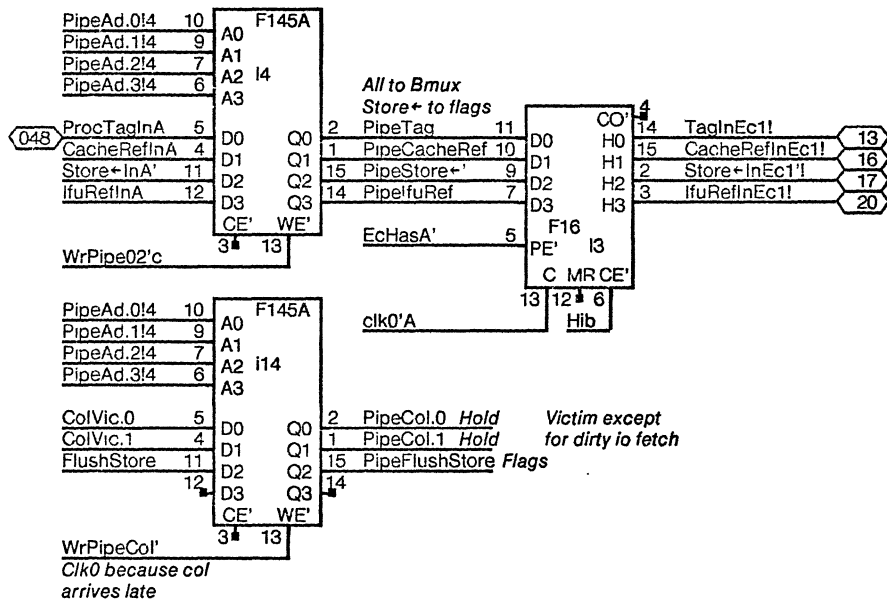
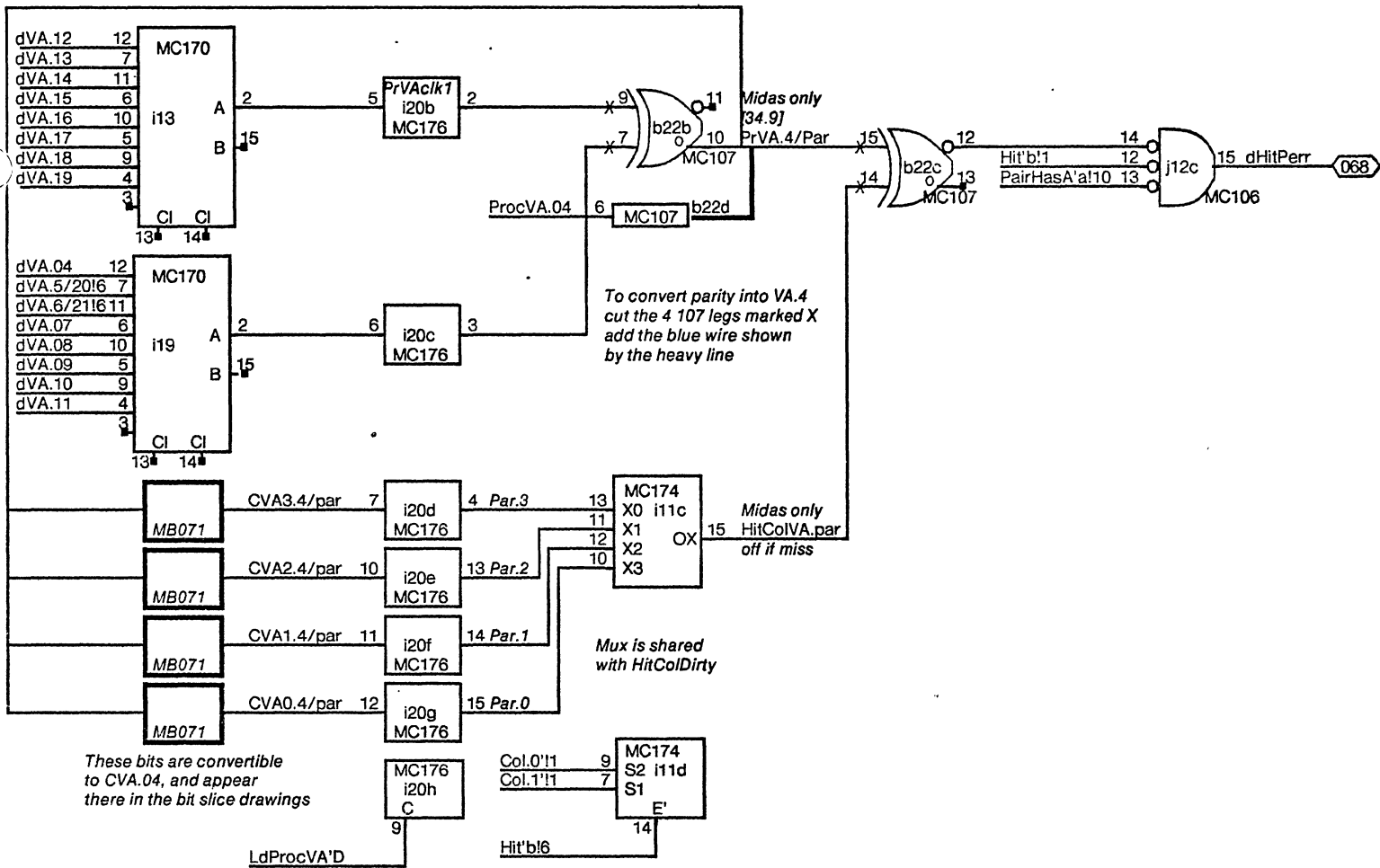


The Victim memory is written on a CacheRef, PreFetch or lfuRef that misses, and on any FlushStore or Flush+.

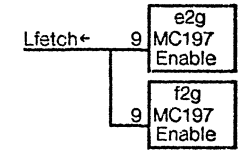
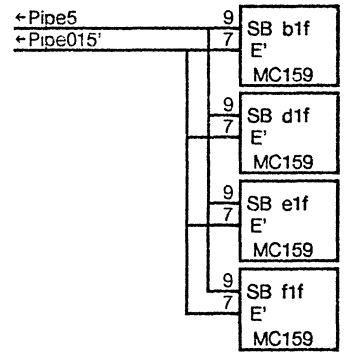
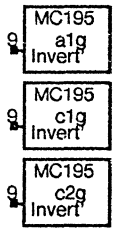
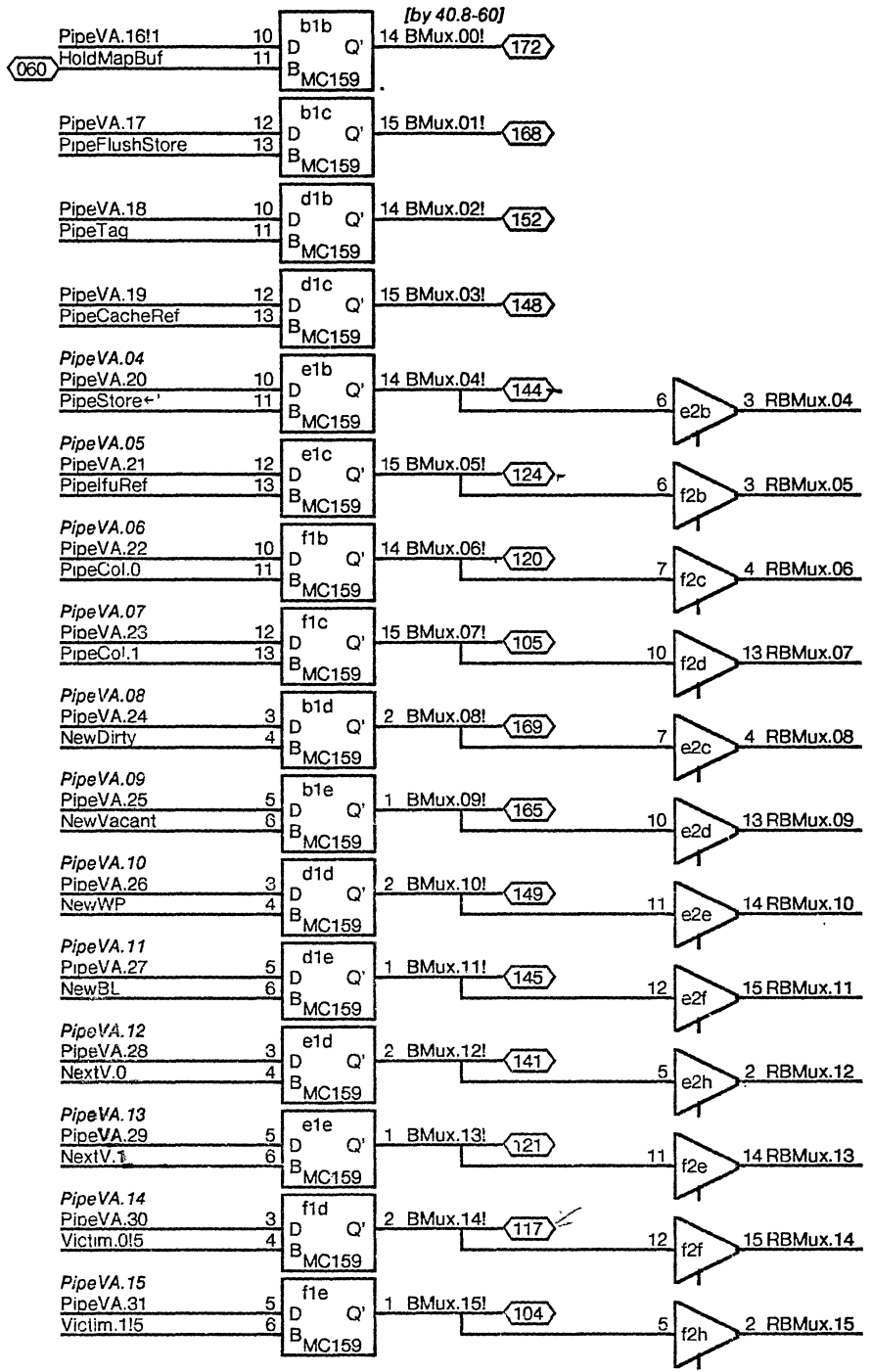
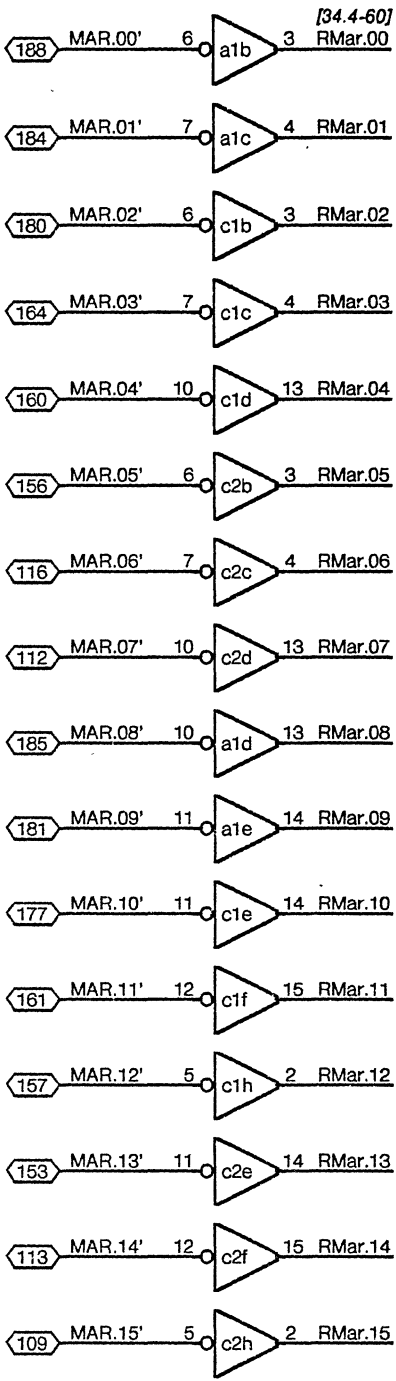
For a Flush+, Victim is first written with 0 on a miss or with the column of the hit. NextV is garbaged at the same time. On a dirty hit, a FlushStore follows, smashing Victim and NextV again.



dFlushStore would be better, but the timing is wrong

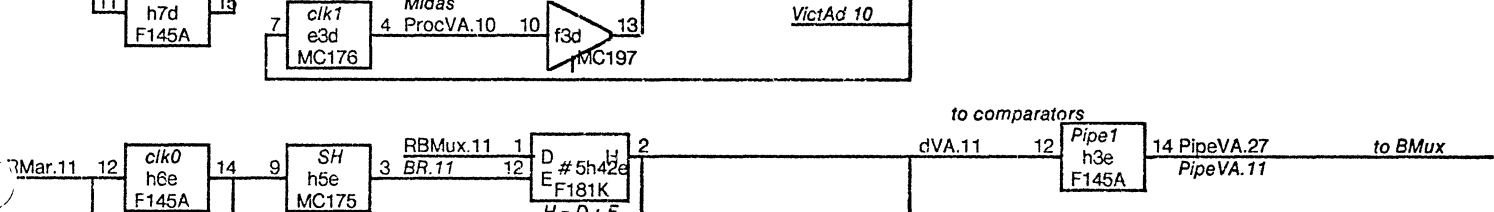
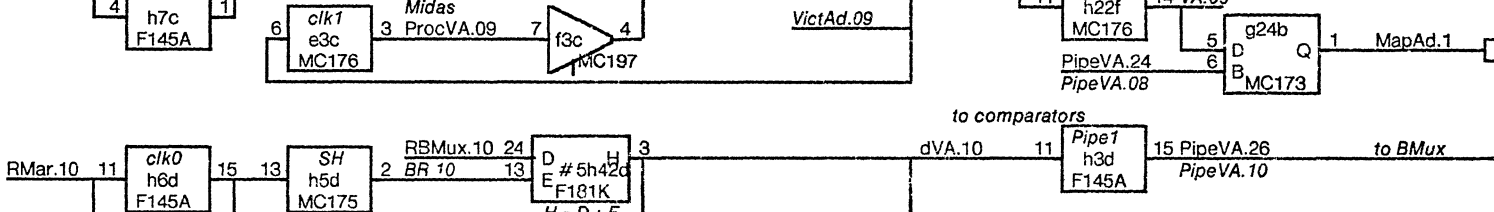
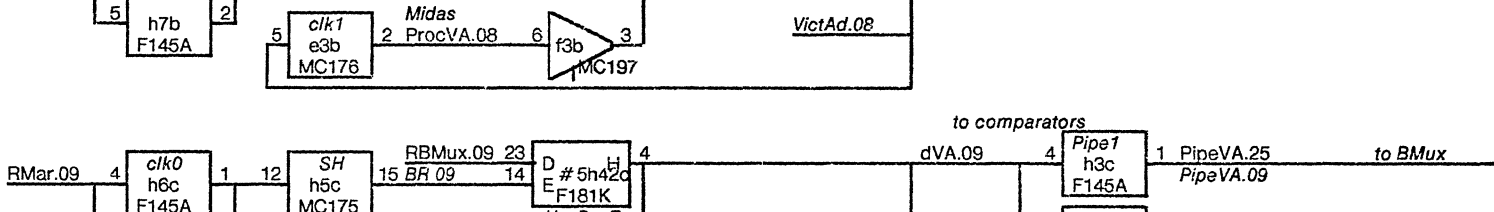
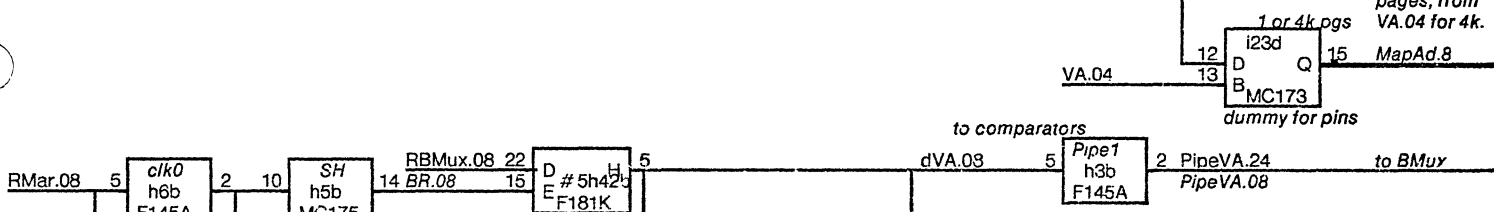
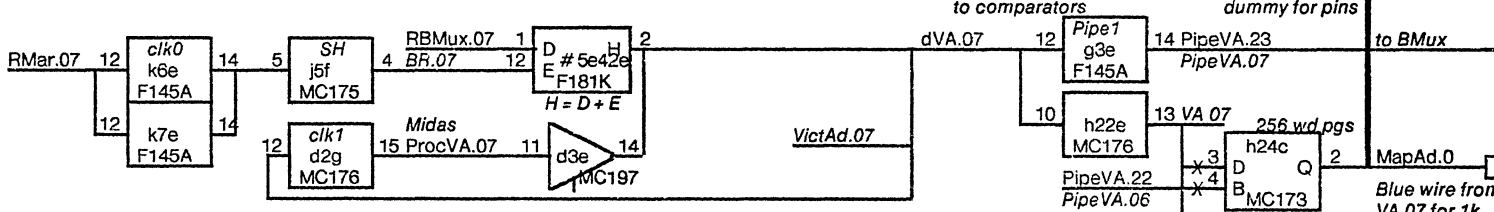
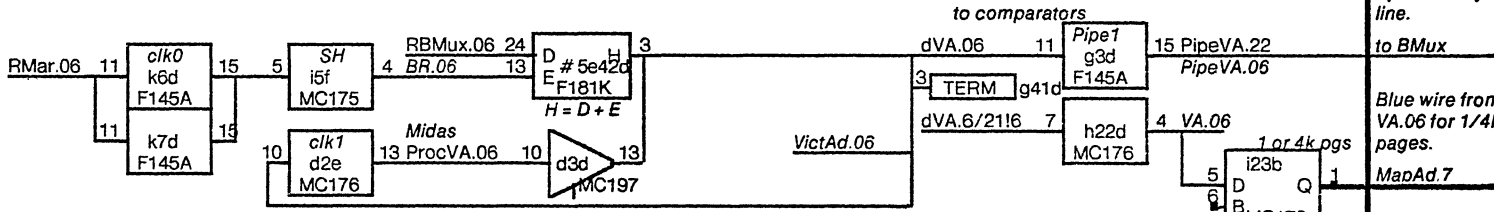
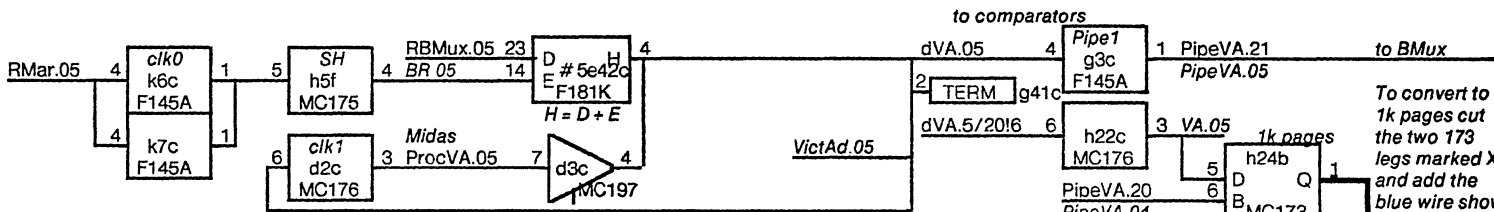
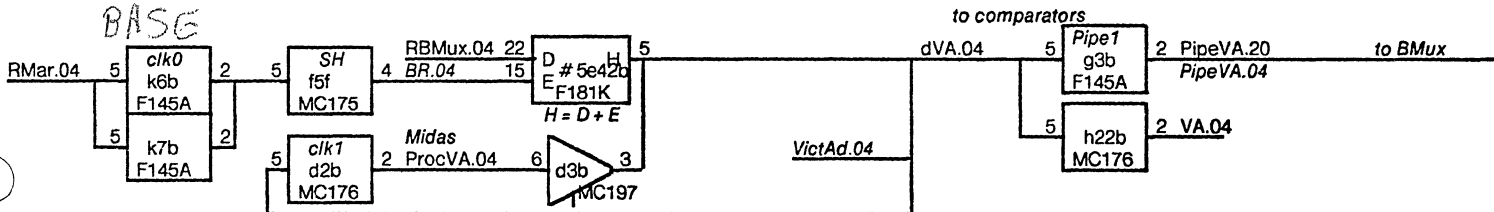


Mcr also includes 5 bits on Vic page



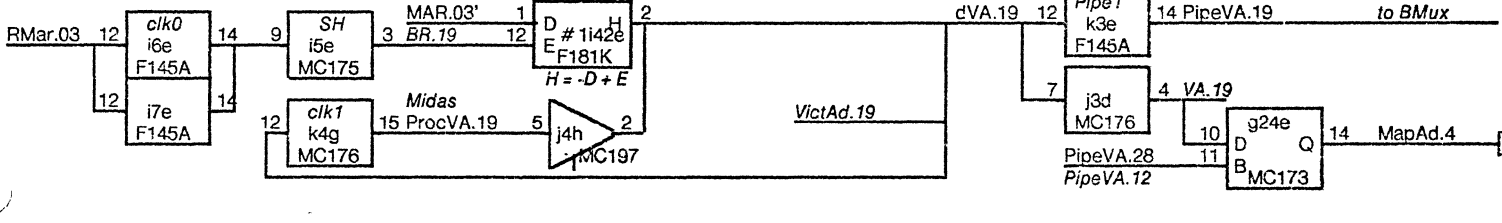
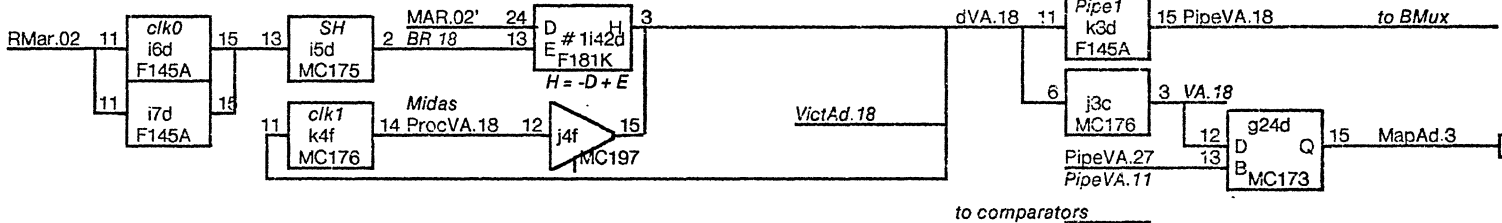
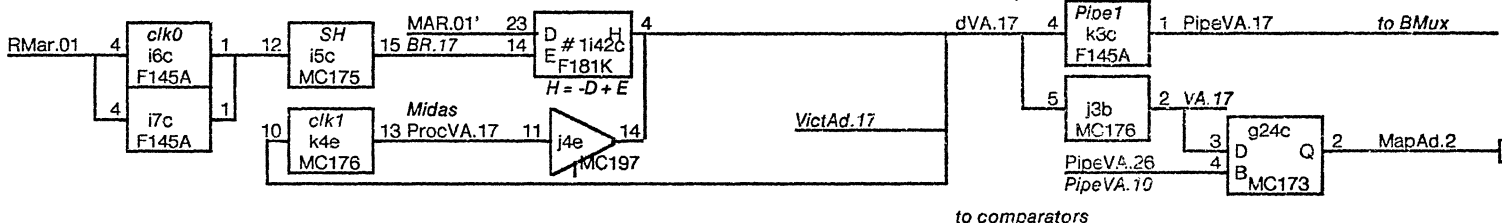
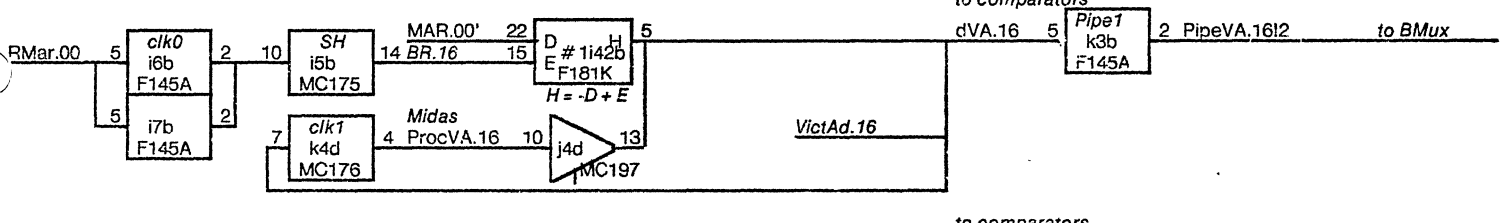
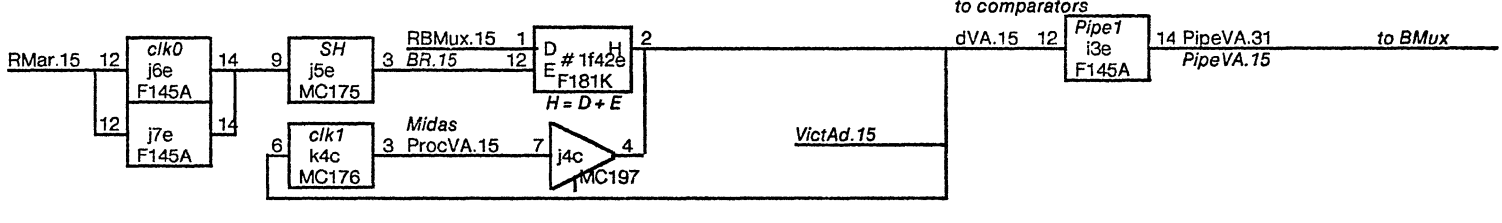
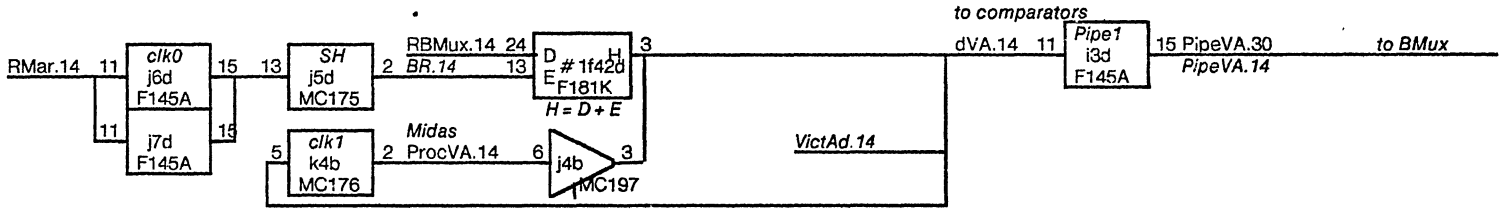
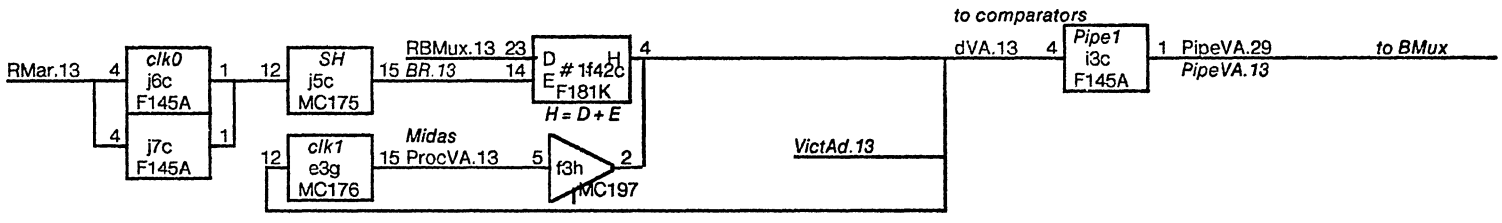
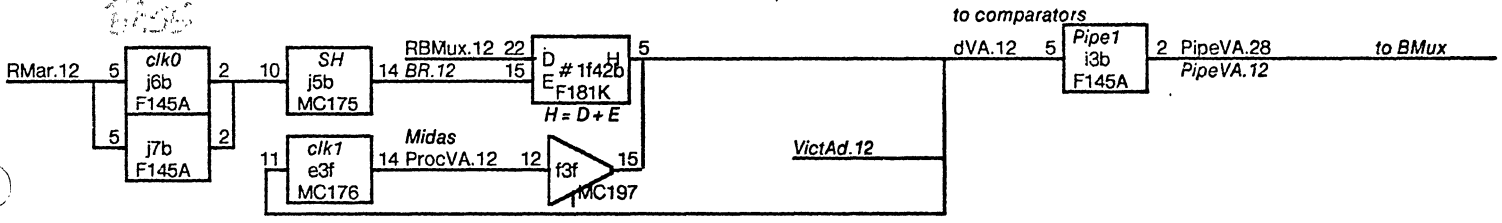
MEM
BASE

PIPE

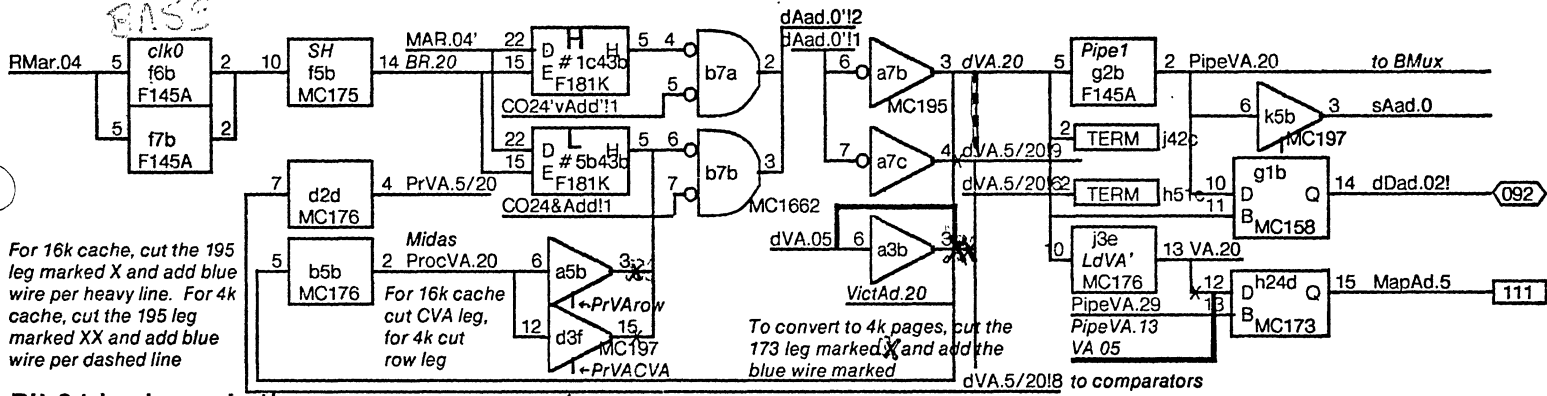


Hand
BASE

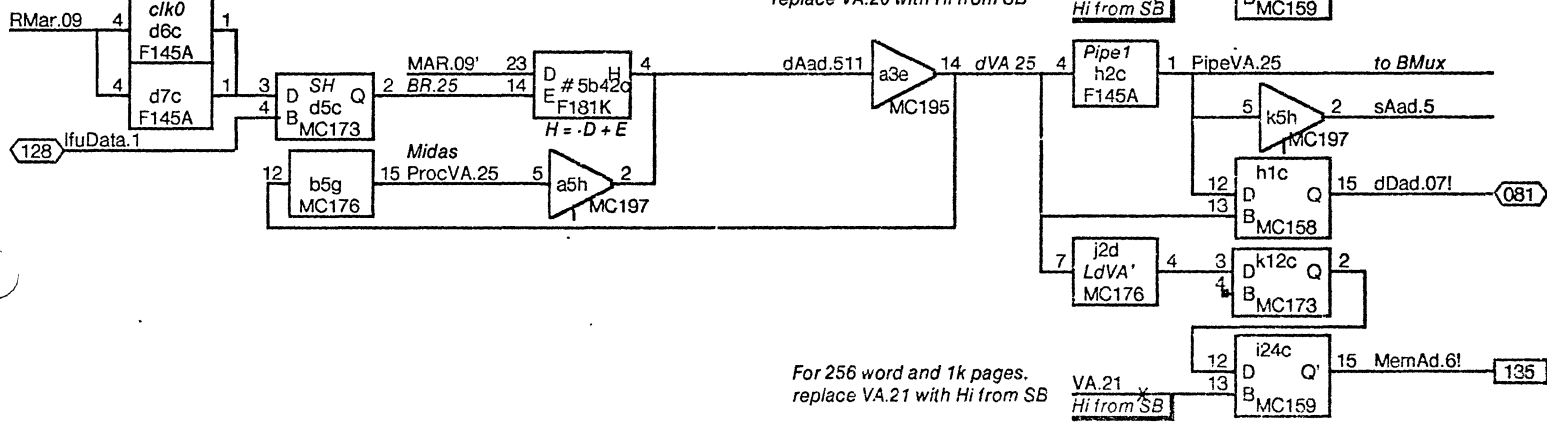
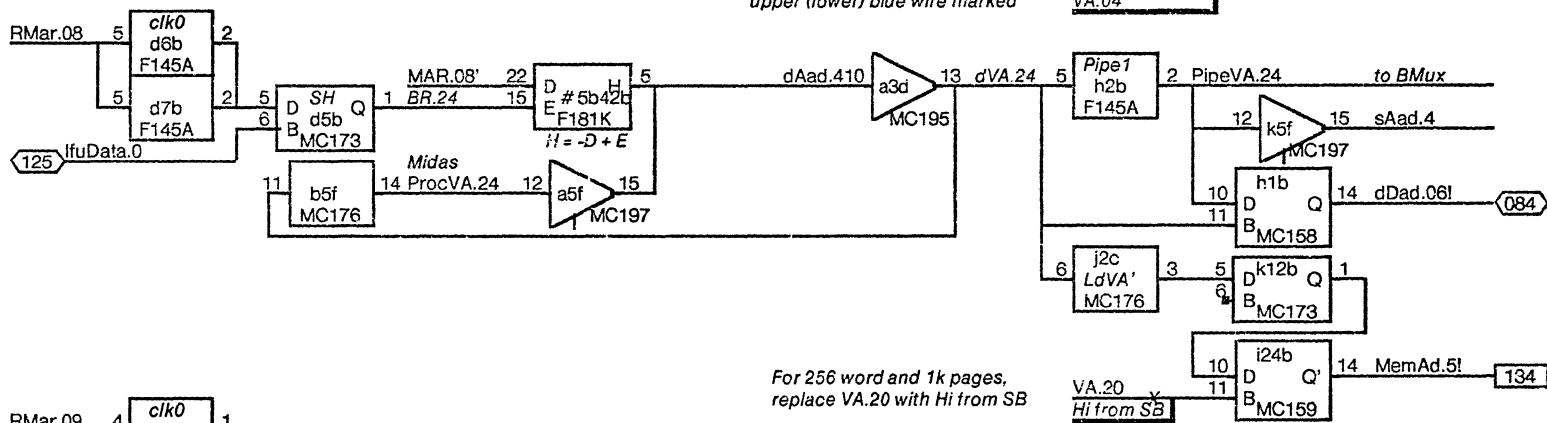
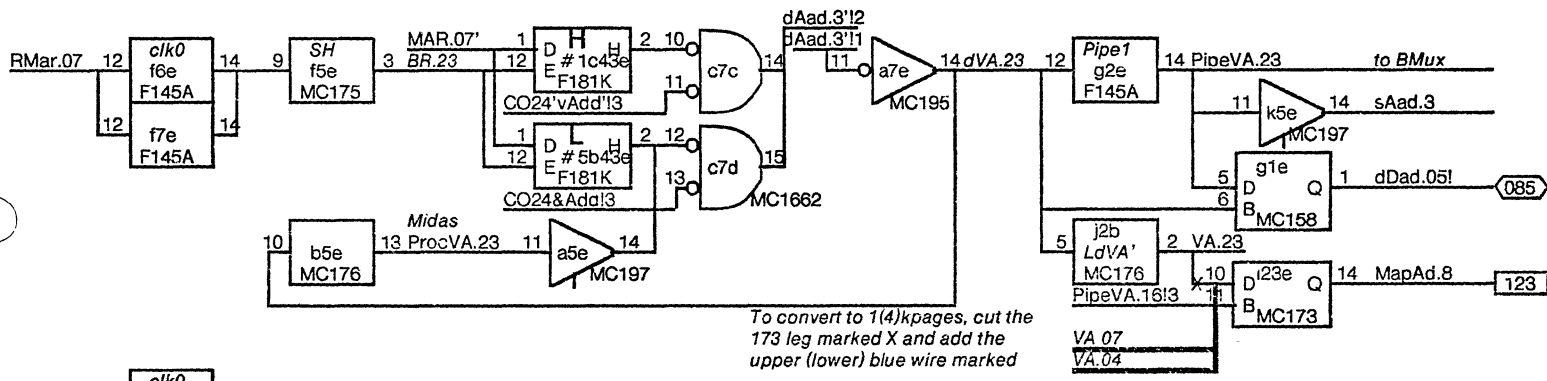
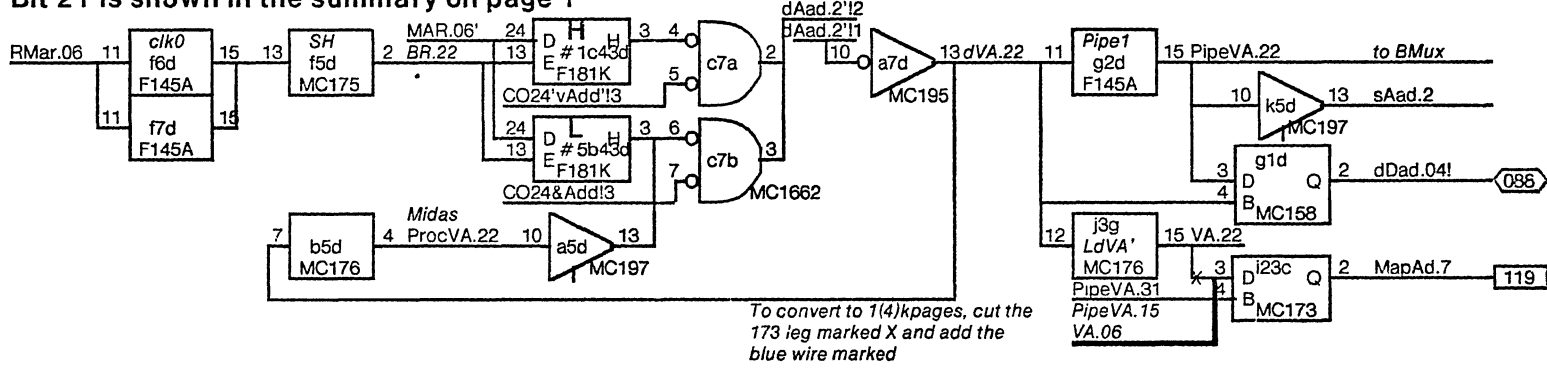
PIPE

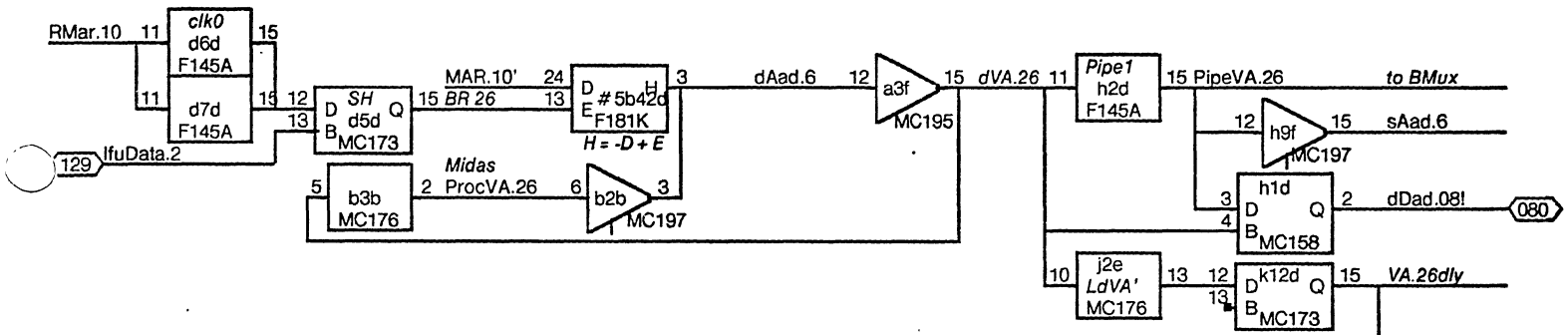


MEM
BASE

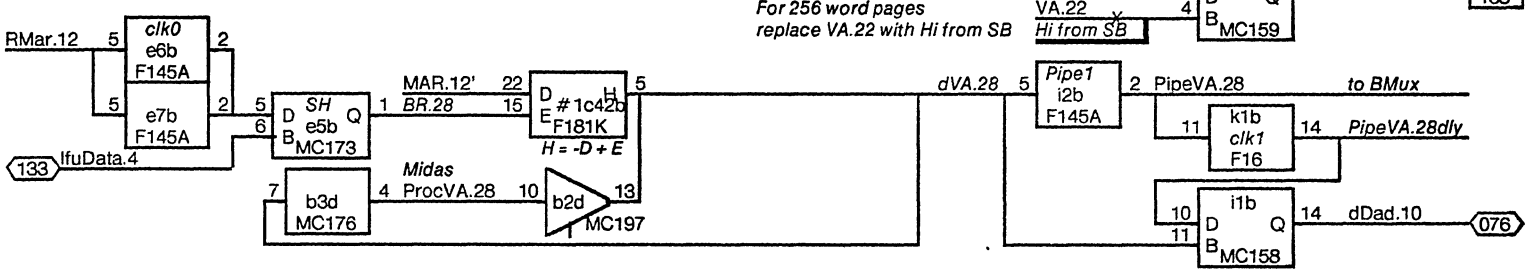


Bit 21 is shown in the summary on page 1

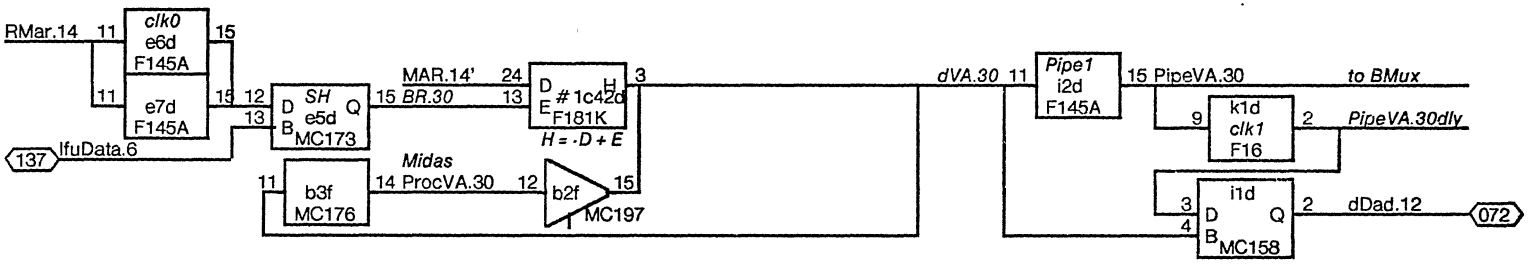
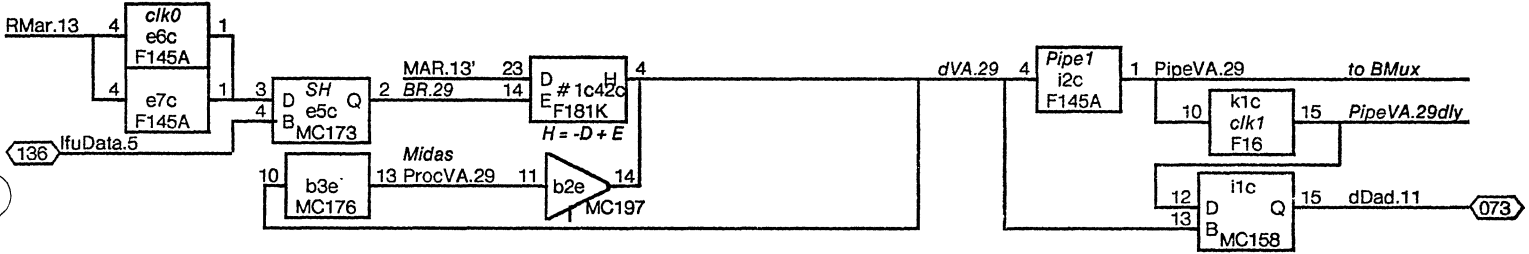




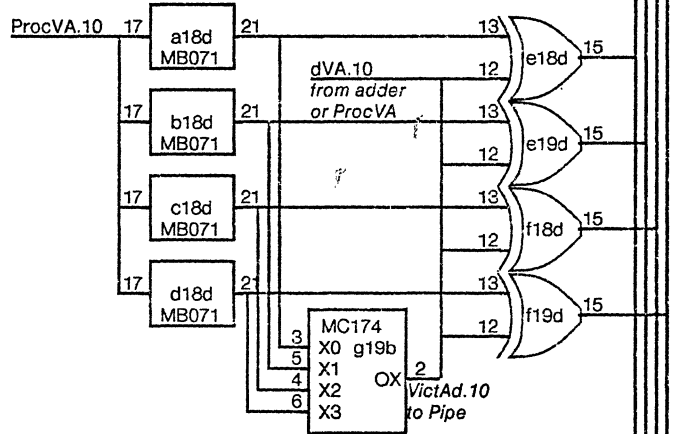
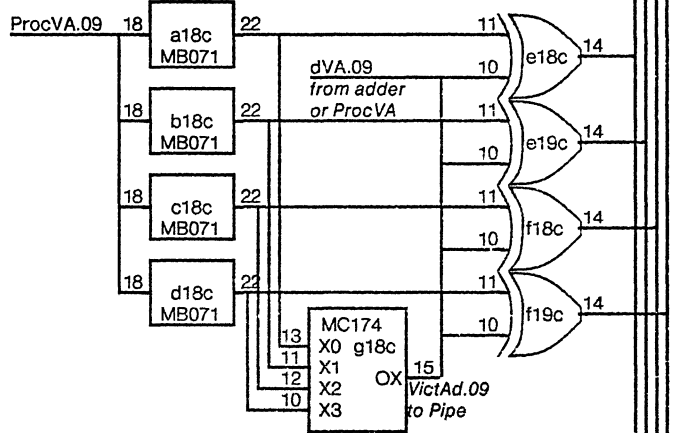
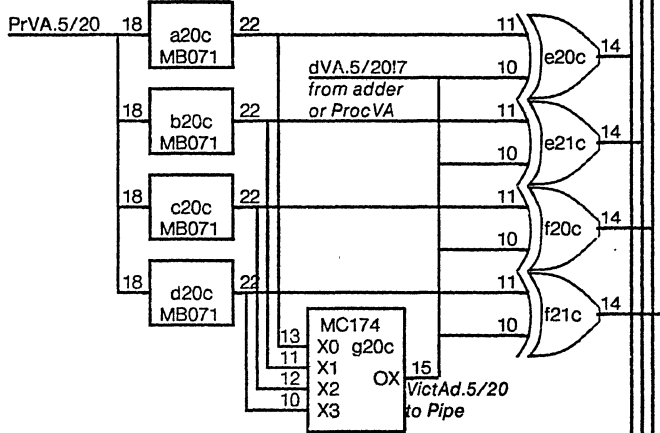
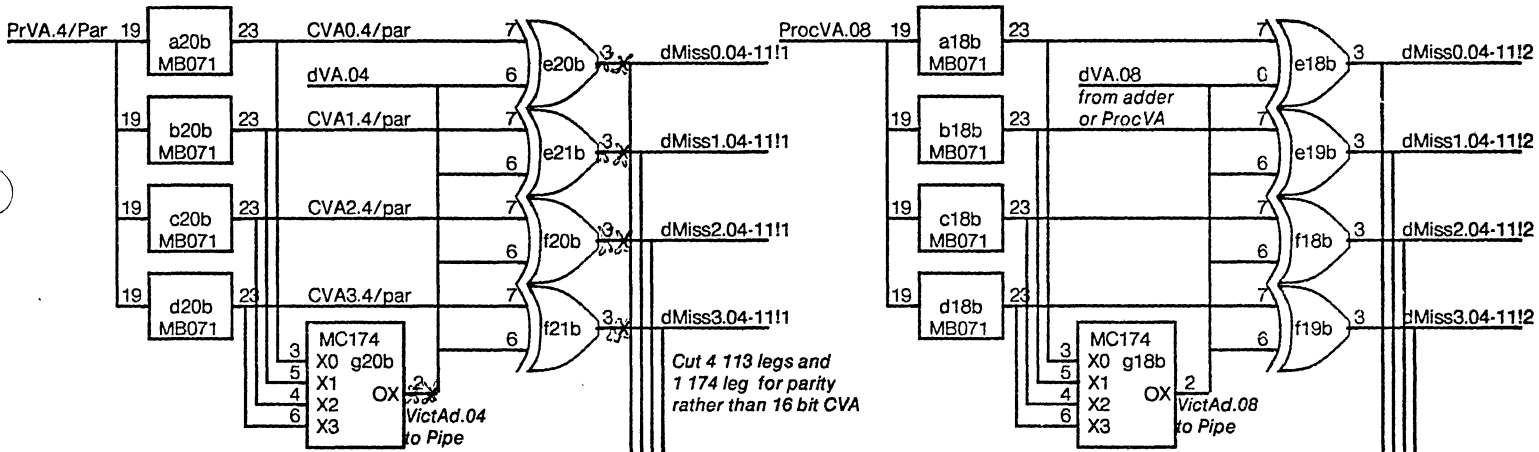
Bit 27 is shown in the summary on page 1



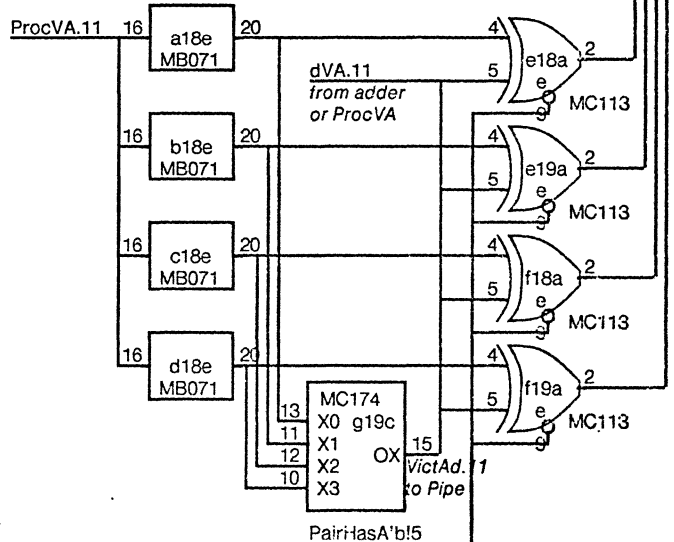
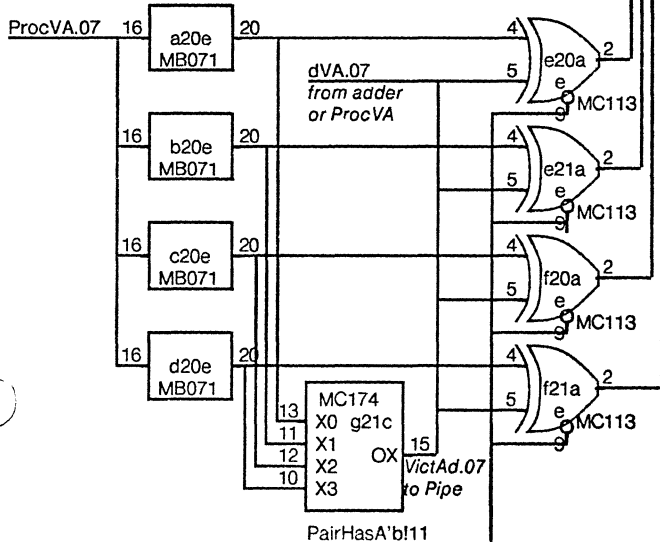
For 256 word pages
replace VA.22 with Hi from SB

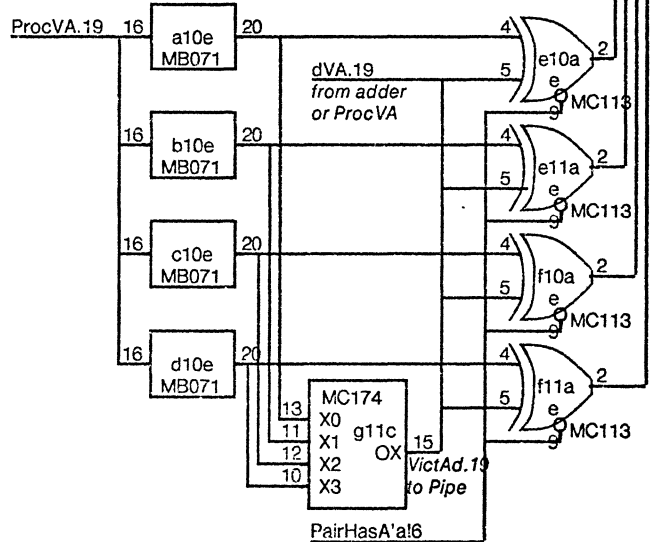
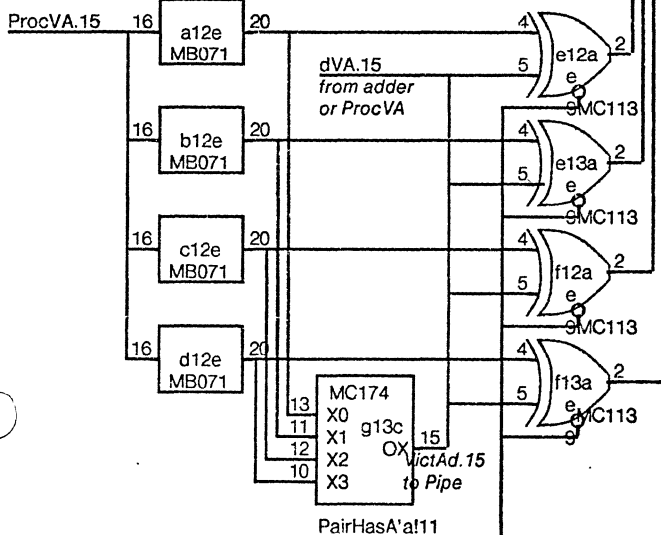
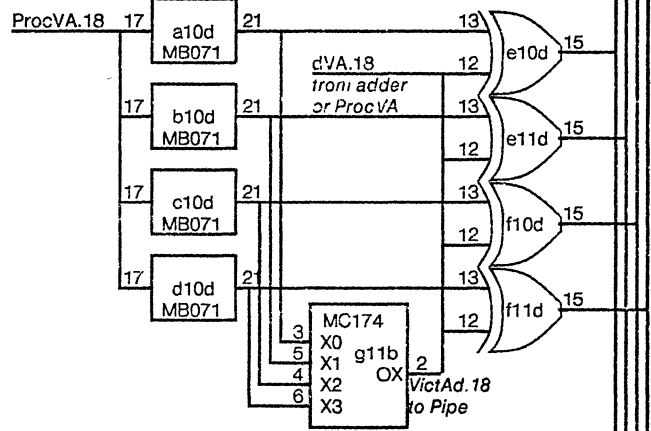
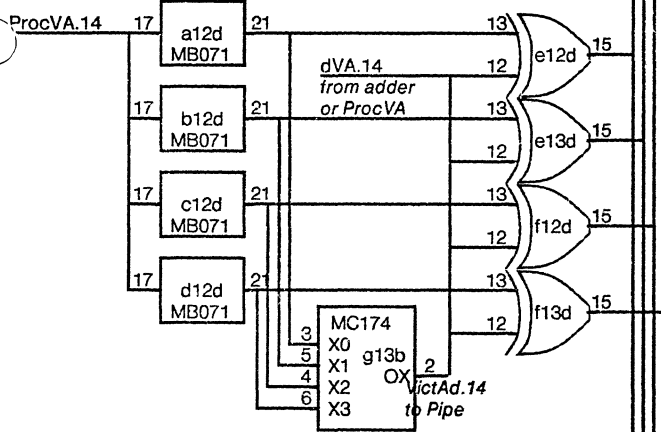
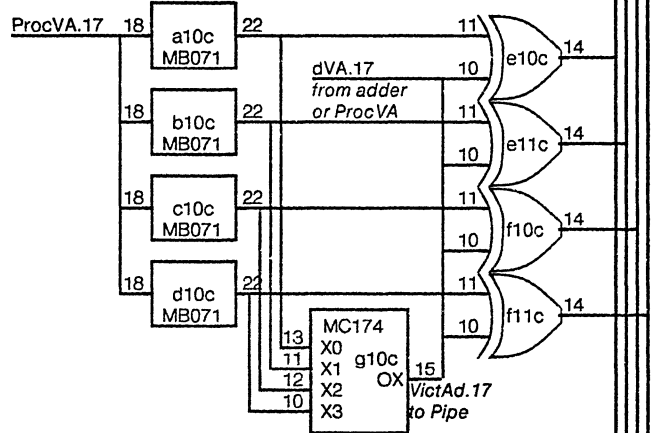
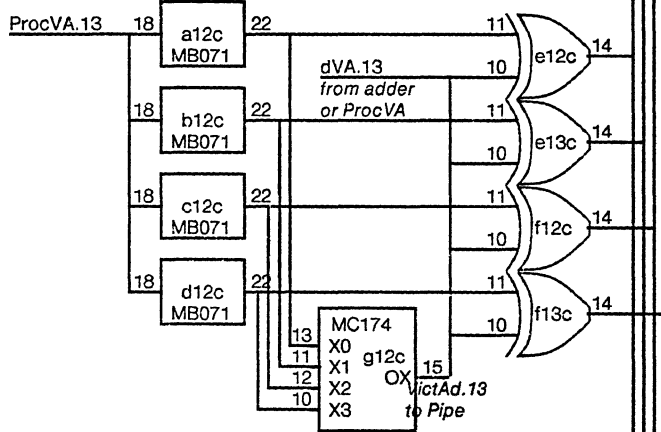
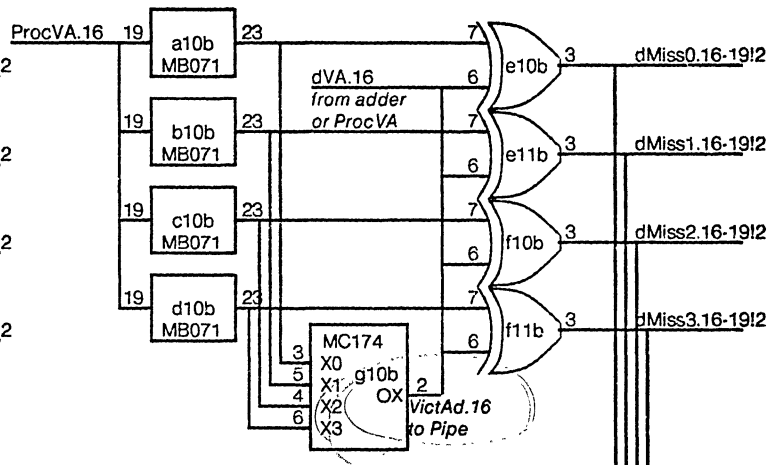
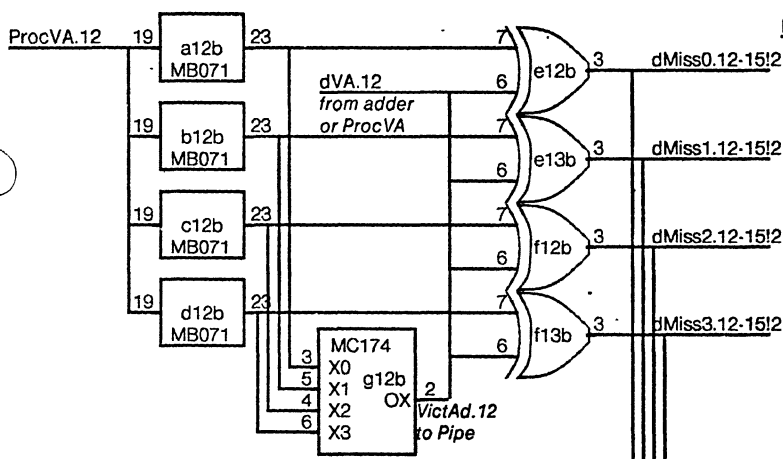


Bit 31 is shown in the summary on page 1



Bit 6 appears in the summary on page 1





This chip's addressing appears in the summary on page 1

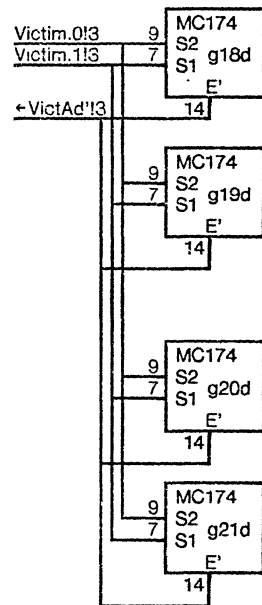
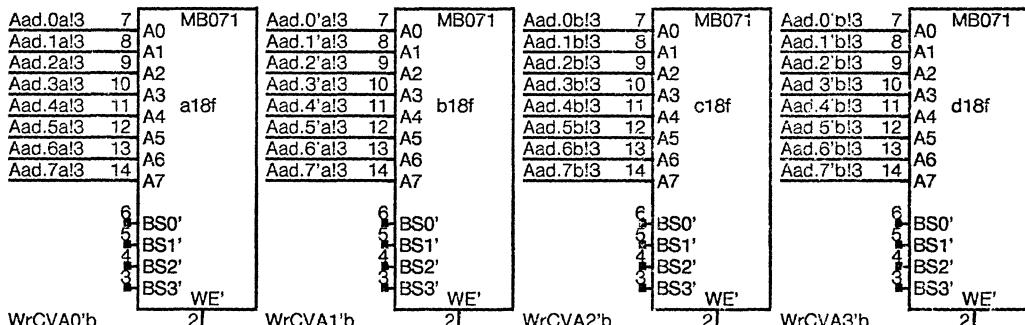
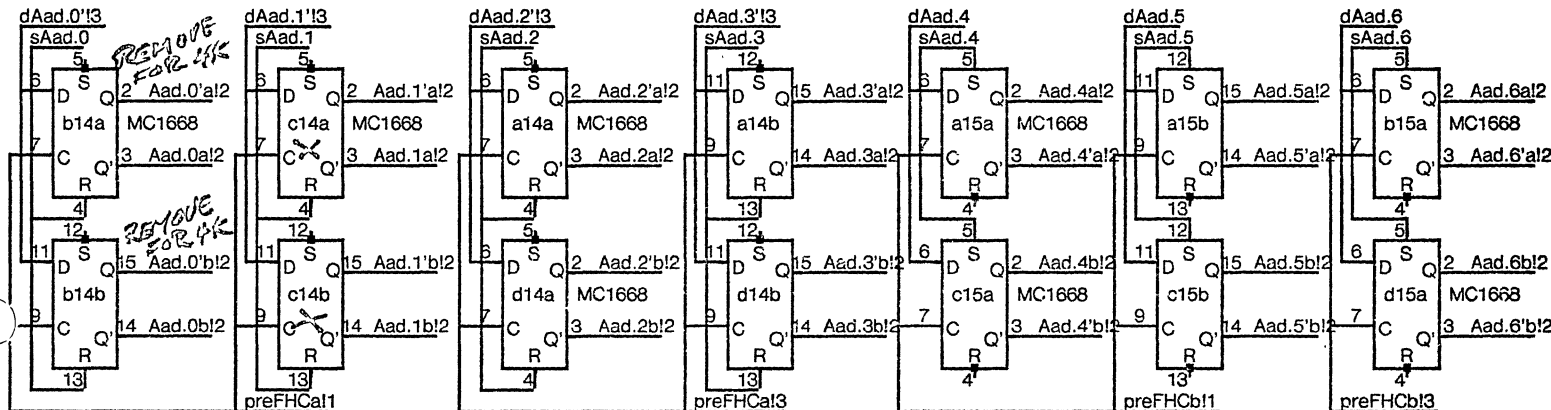
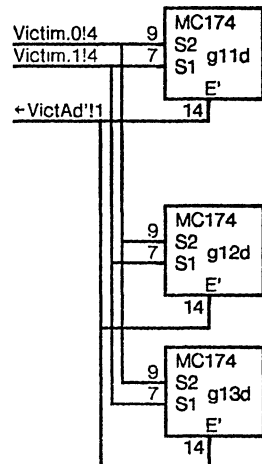
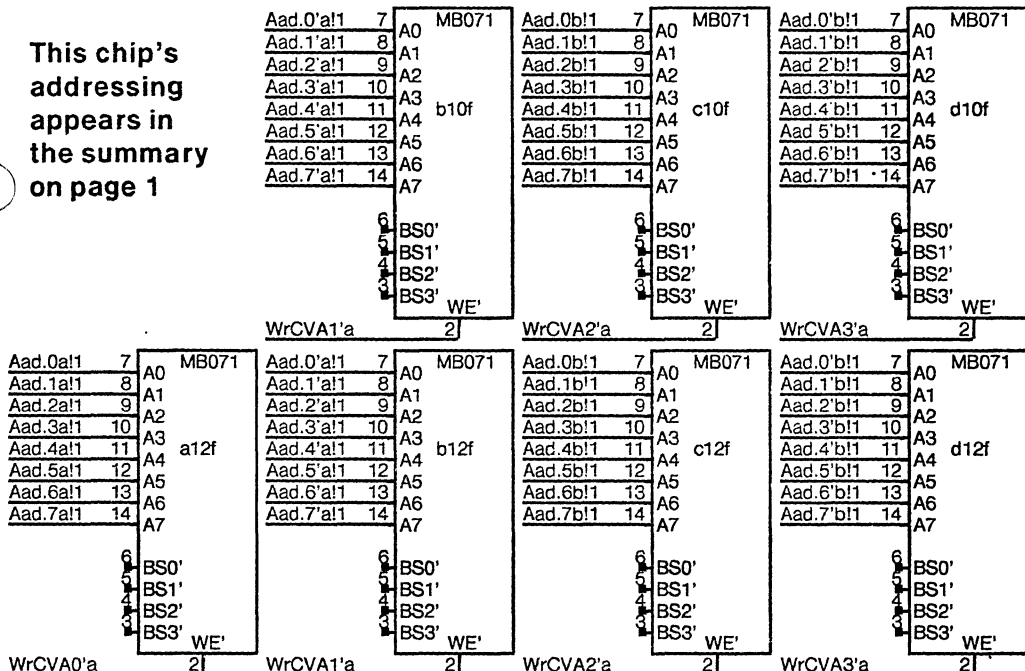
This VictAd mux control appears in the summary on page 1

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18-19

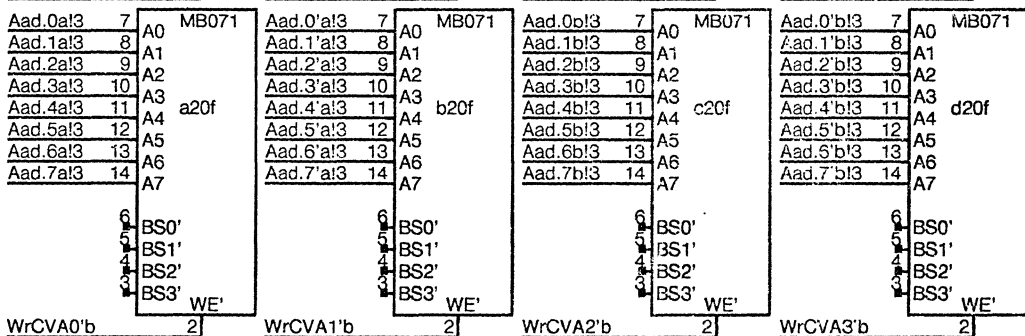
12-13

14-15



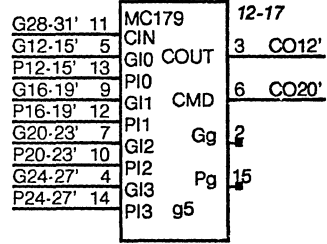
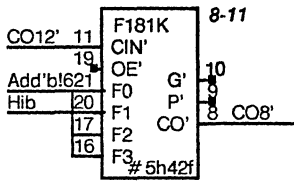
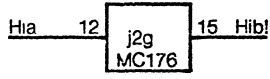
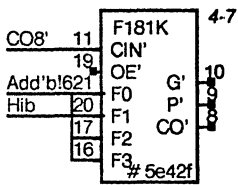
8-9

10-11



4/par-5-20

6/21-7

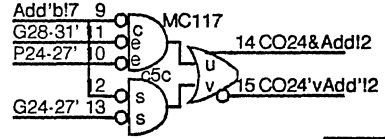
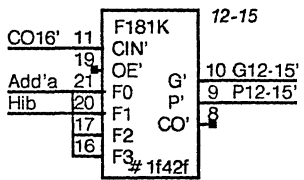


Timing:

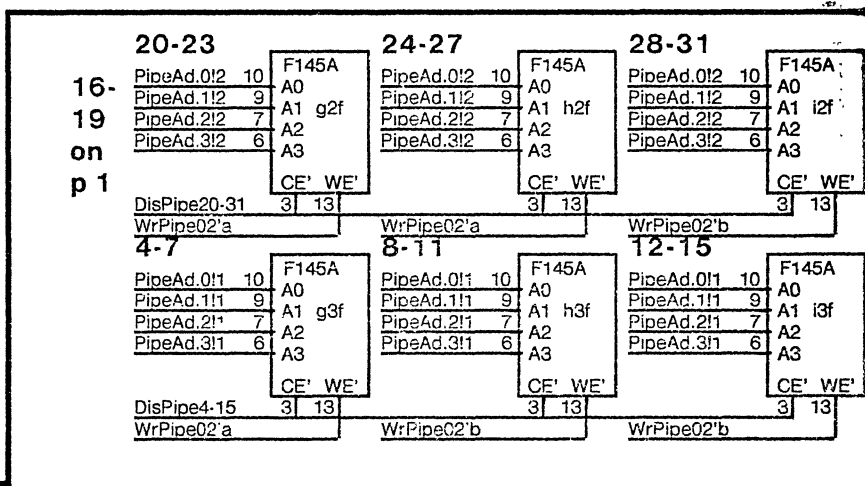
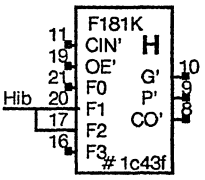
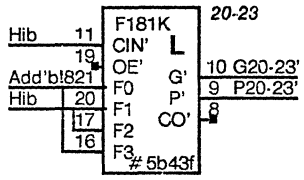
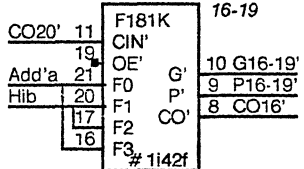
- 28-31 6.5
- 24-27 4.1 + 4.7 = 8.8
- 20-23 4.1 + 3.8 + 1.9 = 9.8
- 16-19 4.1 + 6.0 + 4.7 = 14.8
- 12-15 4.1 + 6.0 + 3.6 + 4.7 = 18.4
- 8-11 4.1 + 6.0 + 4.7 = 14.8
- 4-7 4.1 + 6.0 + 3.6 + 4.7 = 18.4

dAad. A RAM outputs are 2.8 + 10 = 12.8 later or at 22.6

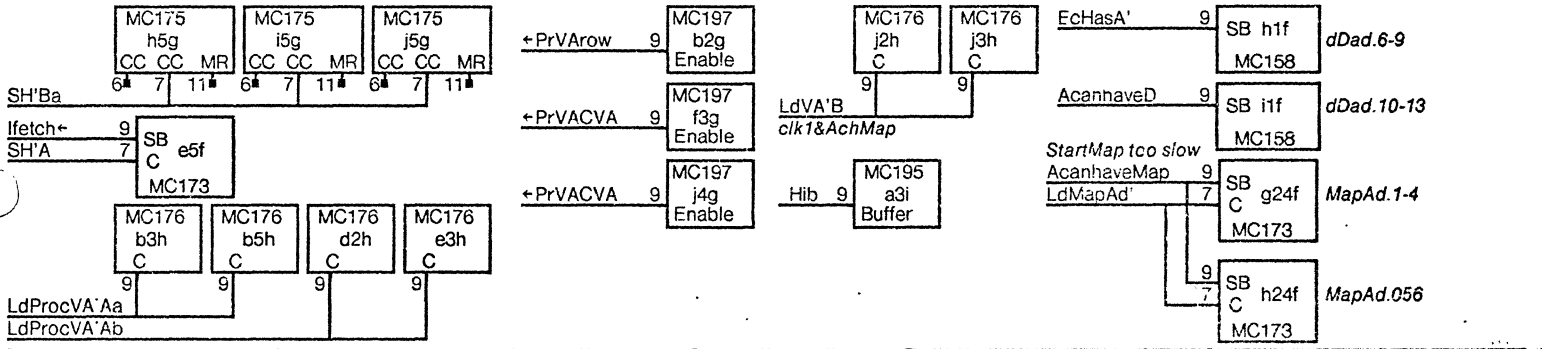
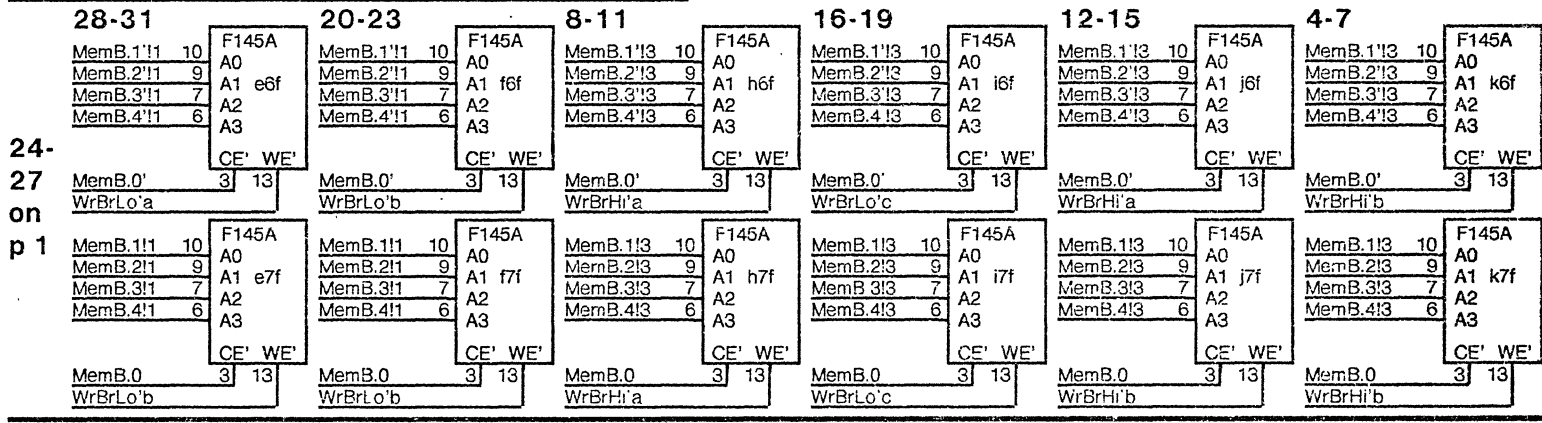
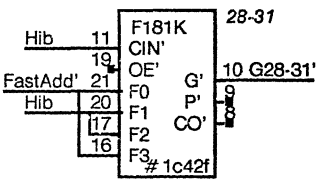
dVA, for comparators, must meet the RAM outputs

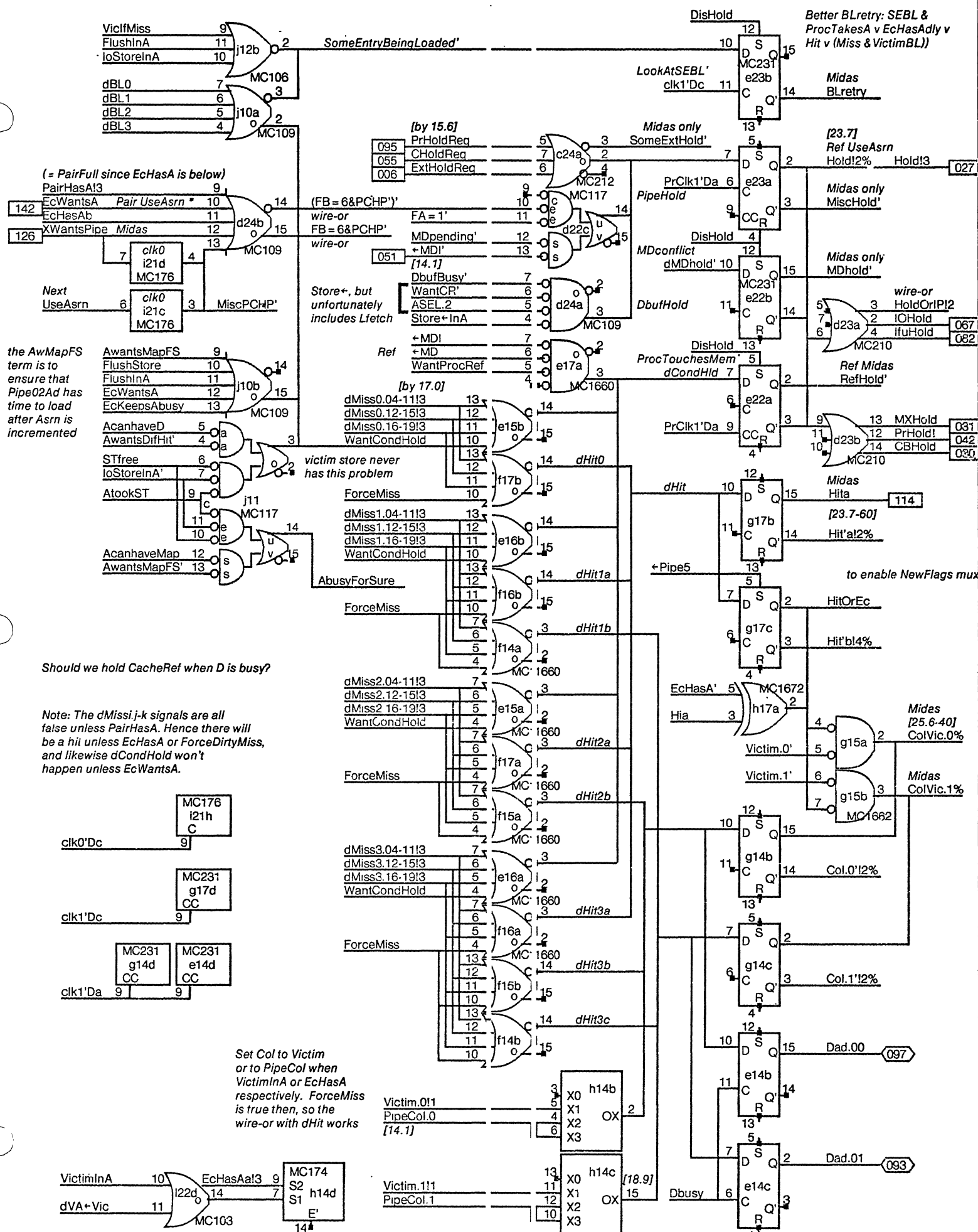


Control: D = RBMux/Mar' Add' = > 0 from 181K, or F = 1111
E = BR Add = > D + E, or F = 0100 on 4-15
-D + E, or F = 0110 on 16-31

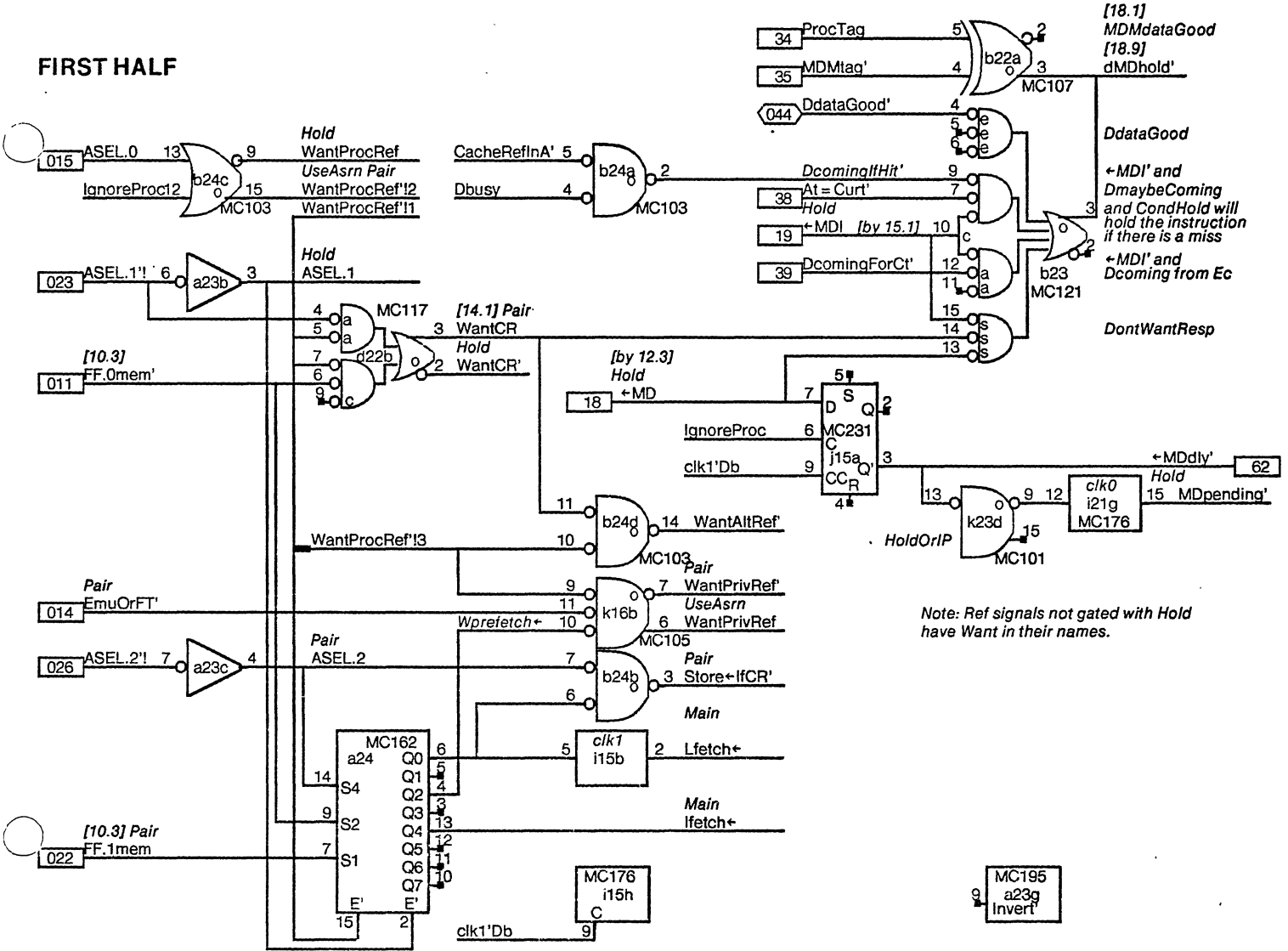


Bits 24-27 appear in the summary on page 1



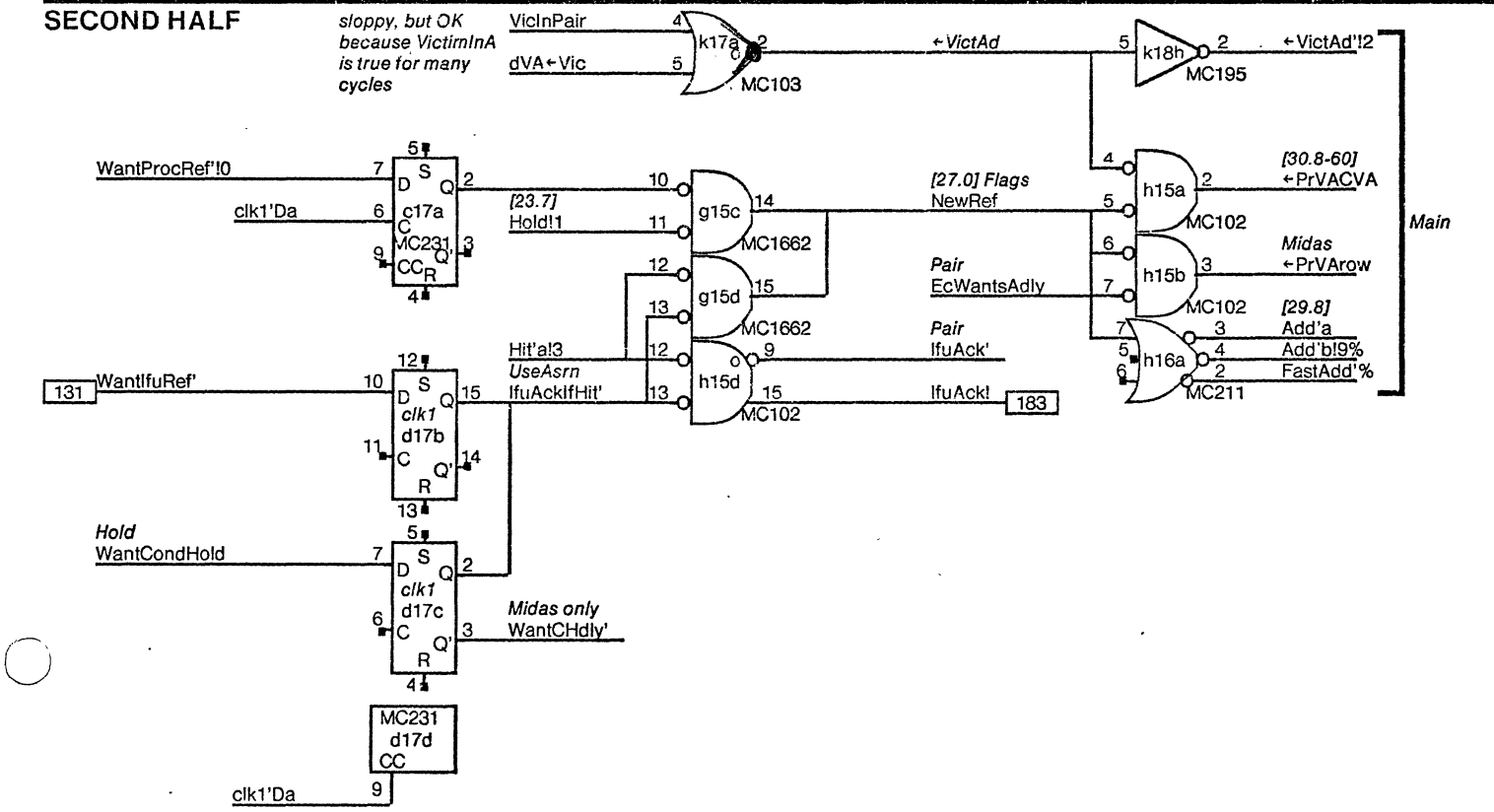


FIRST HALF

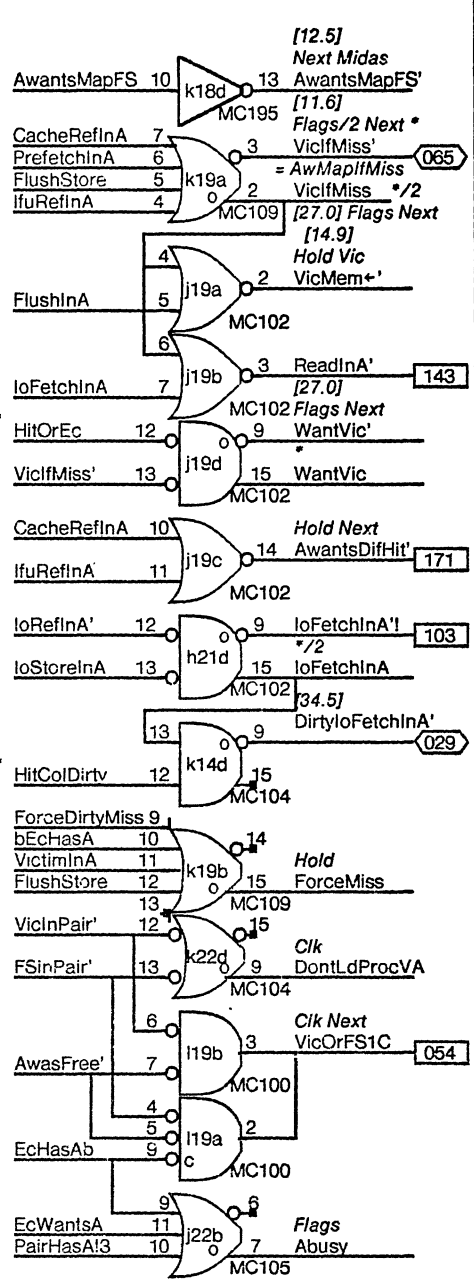
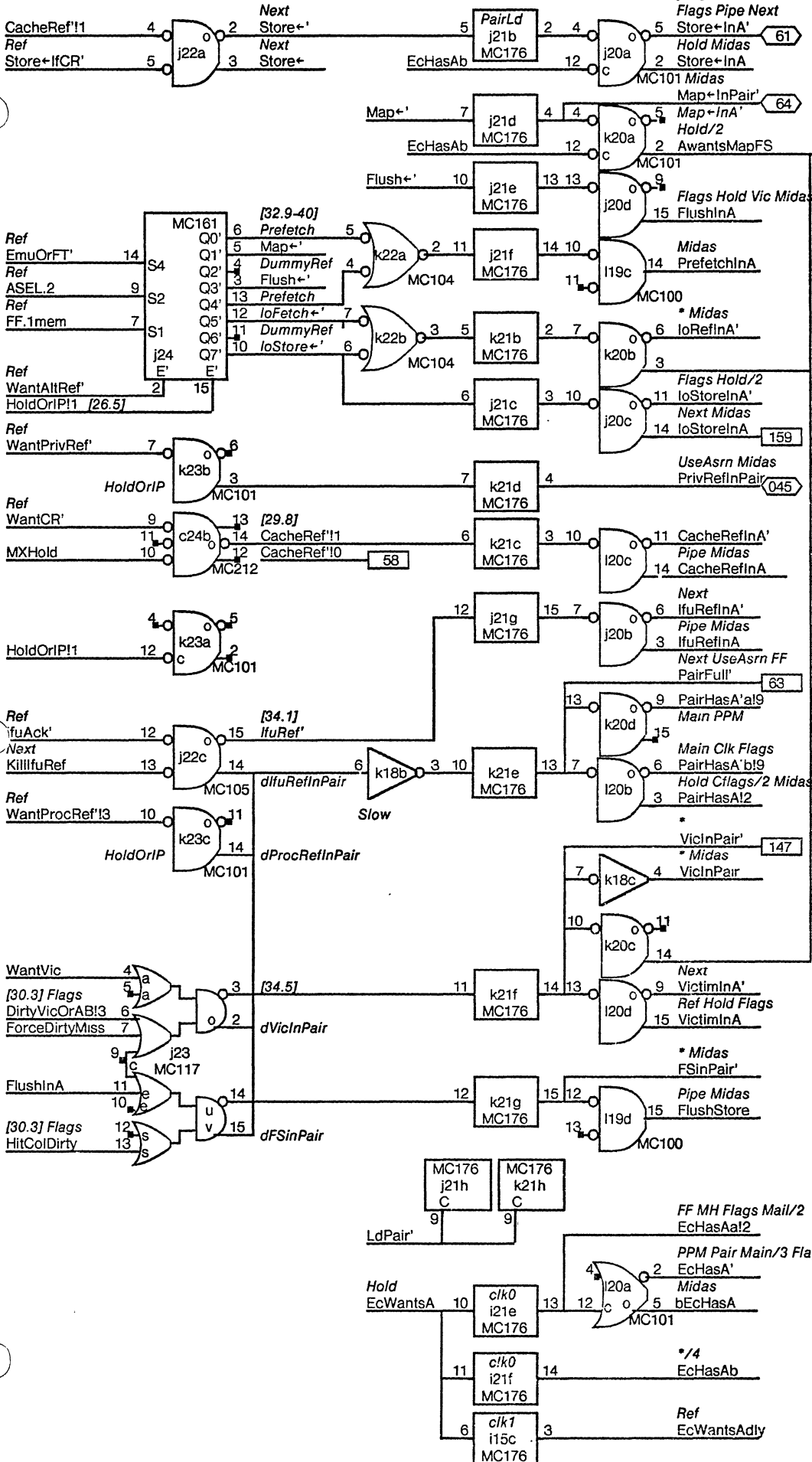


Note: Ref signals not gated with Hold have Want in their names.

SECOND HALF

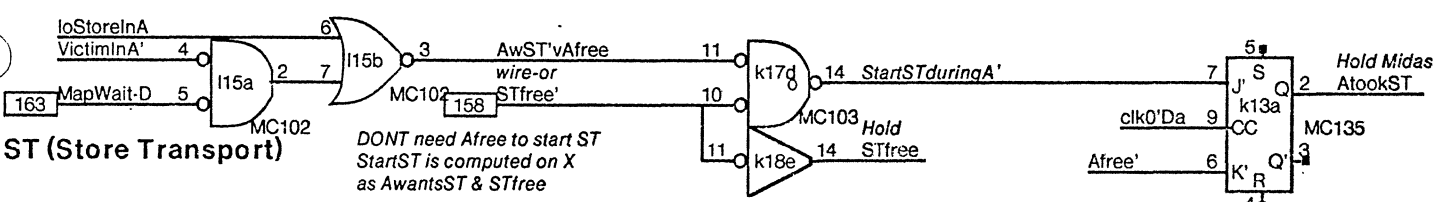
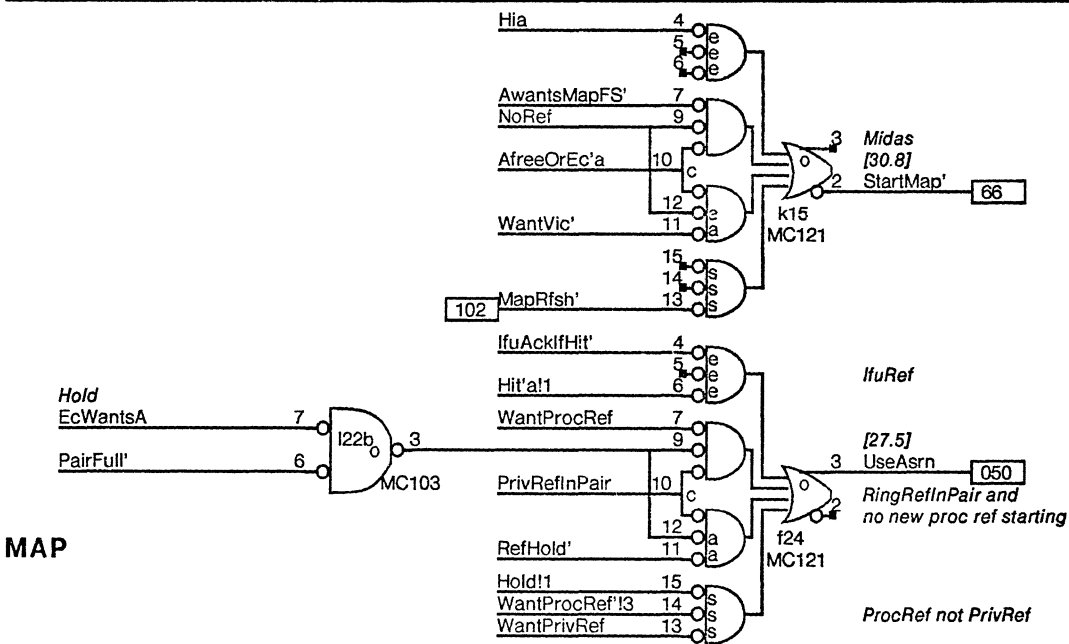
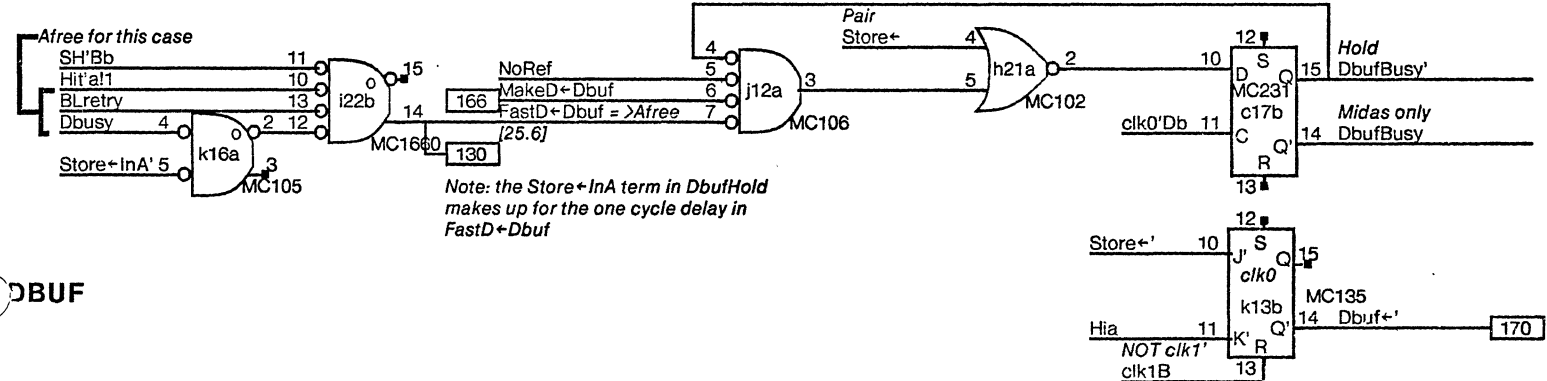
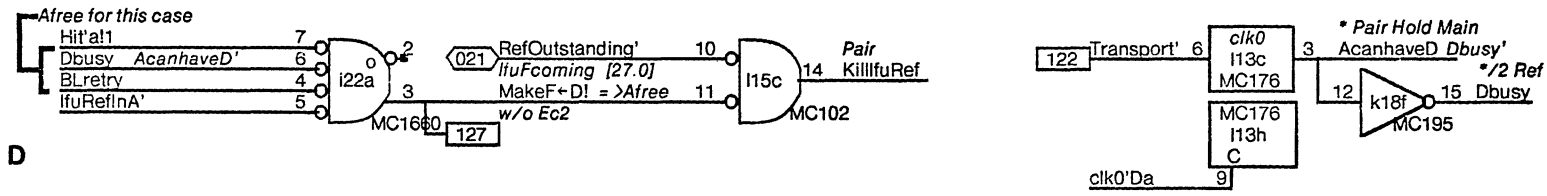
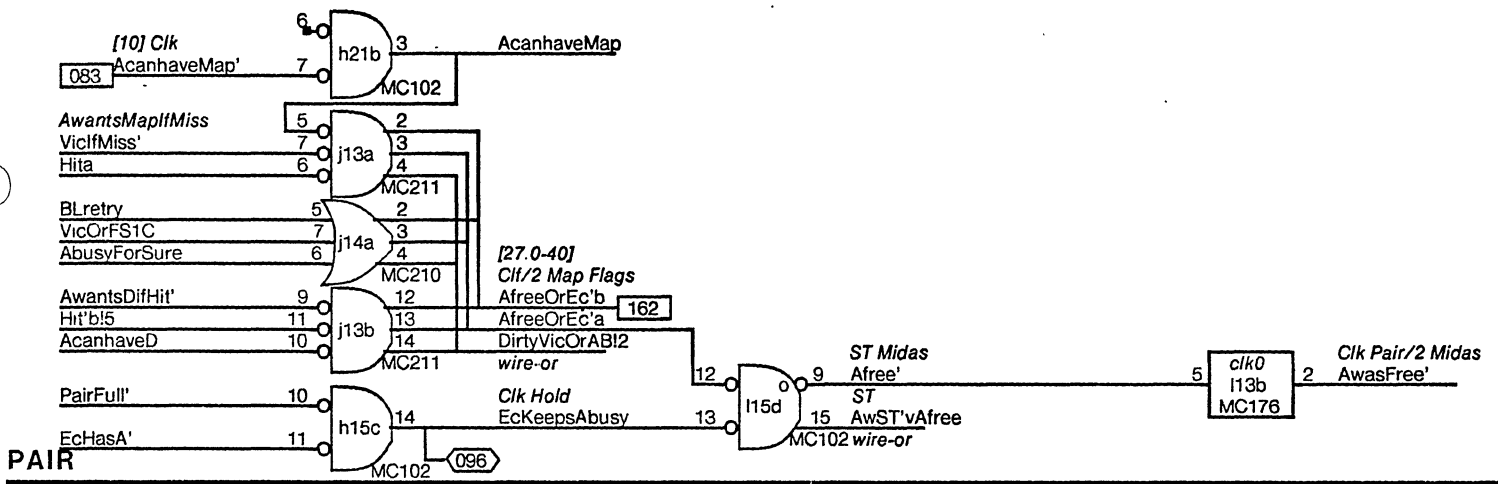


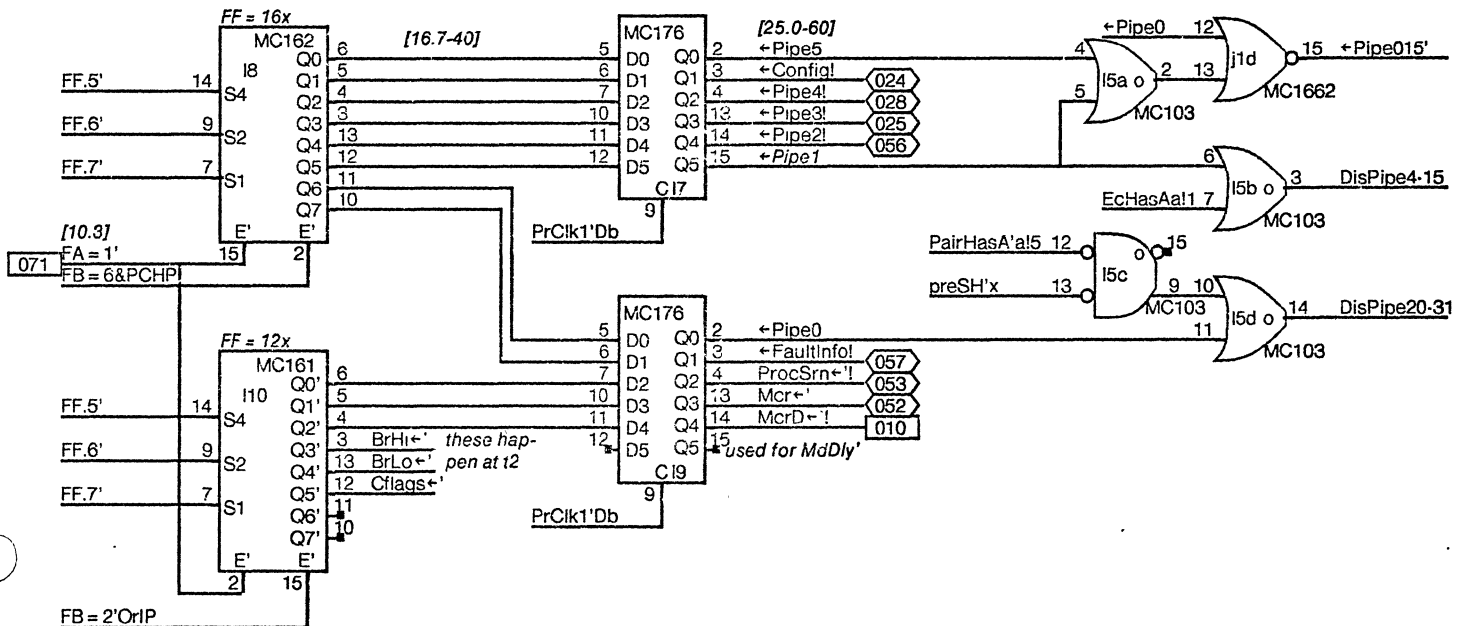
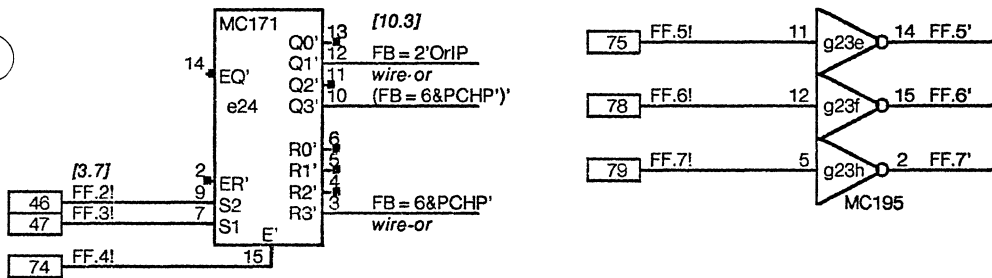
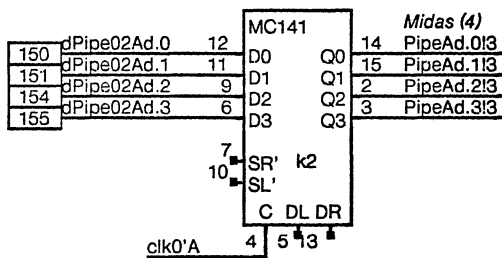
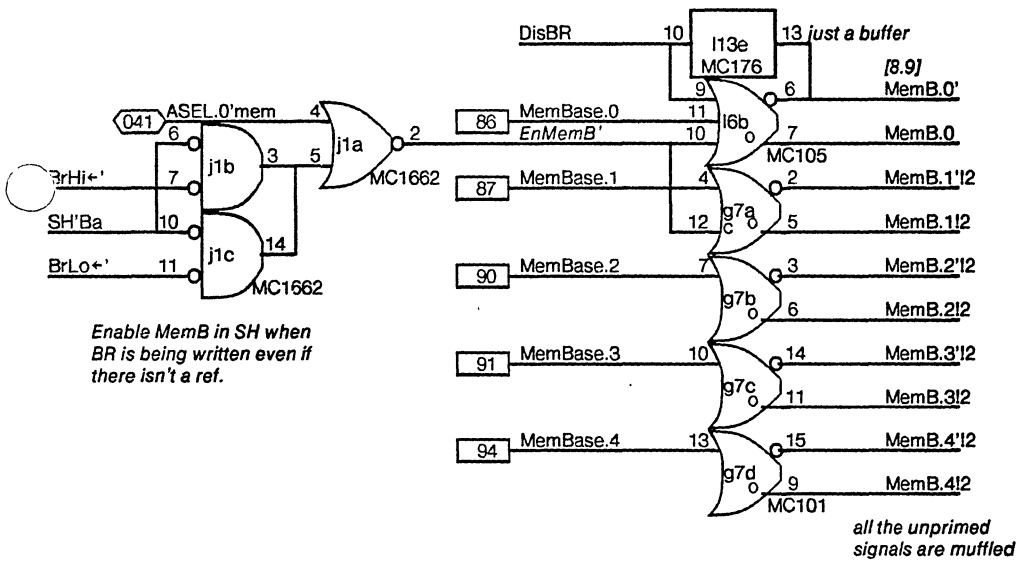
PAIR

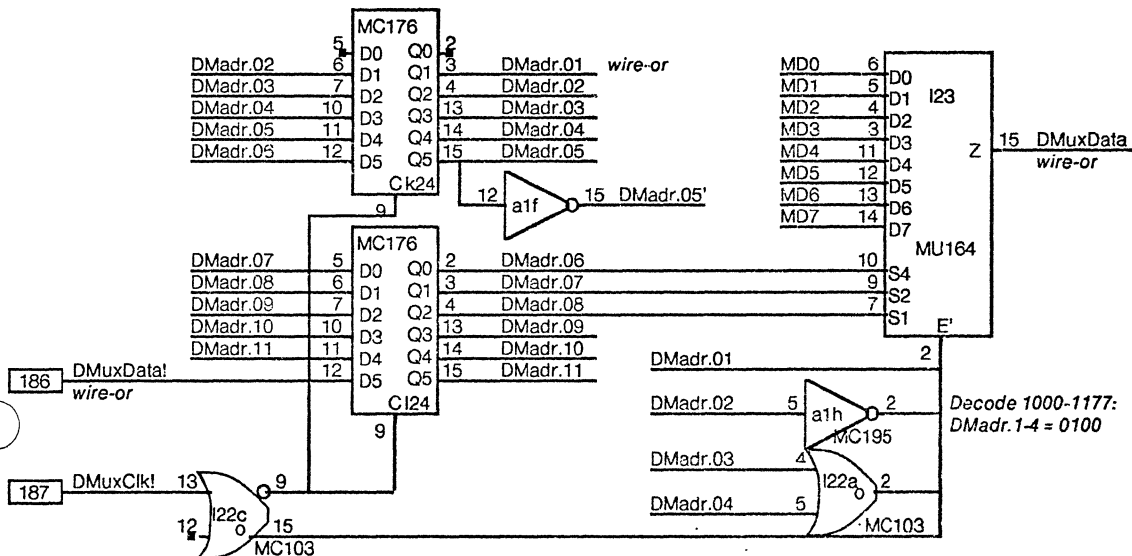
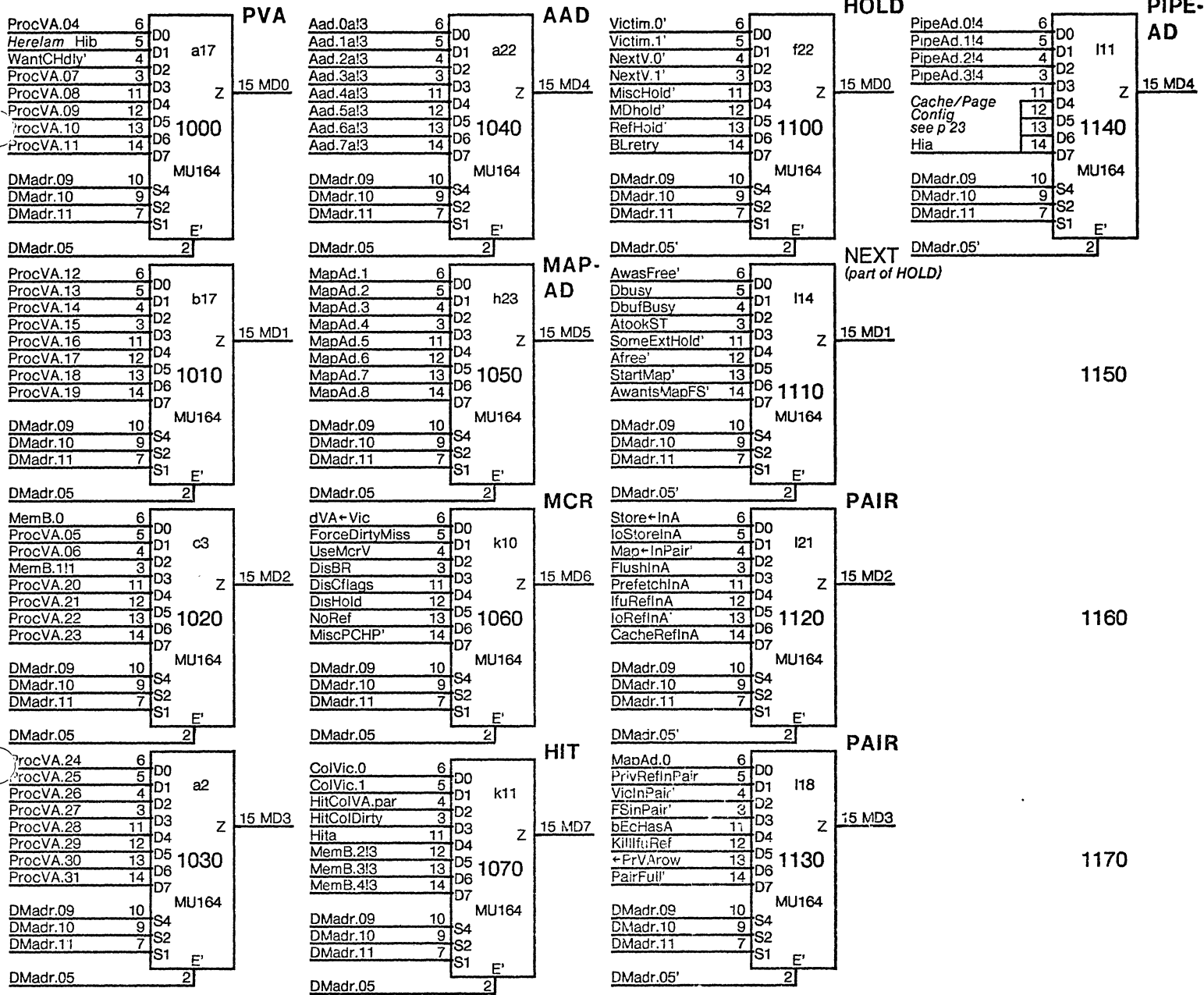


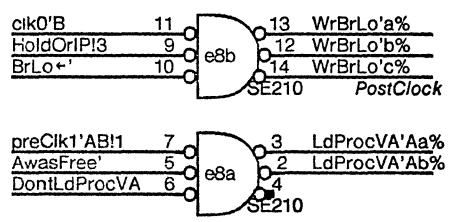
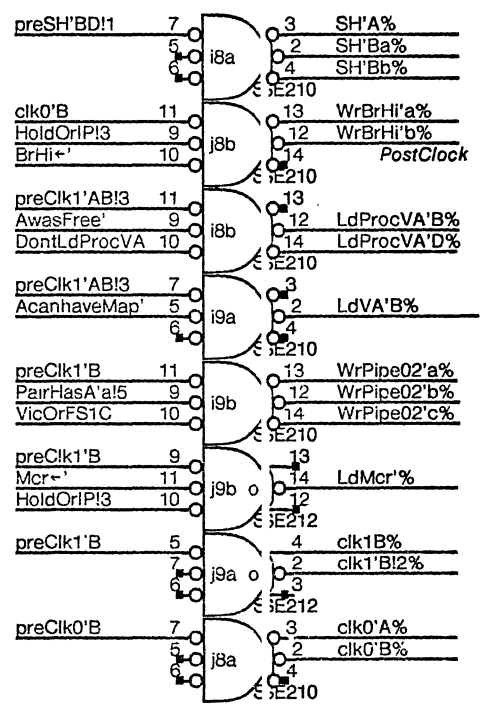
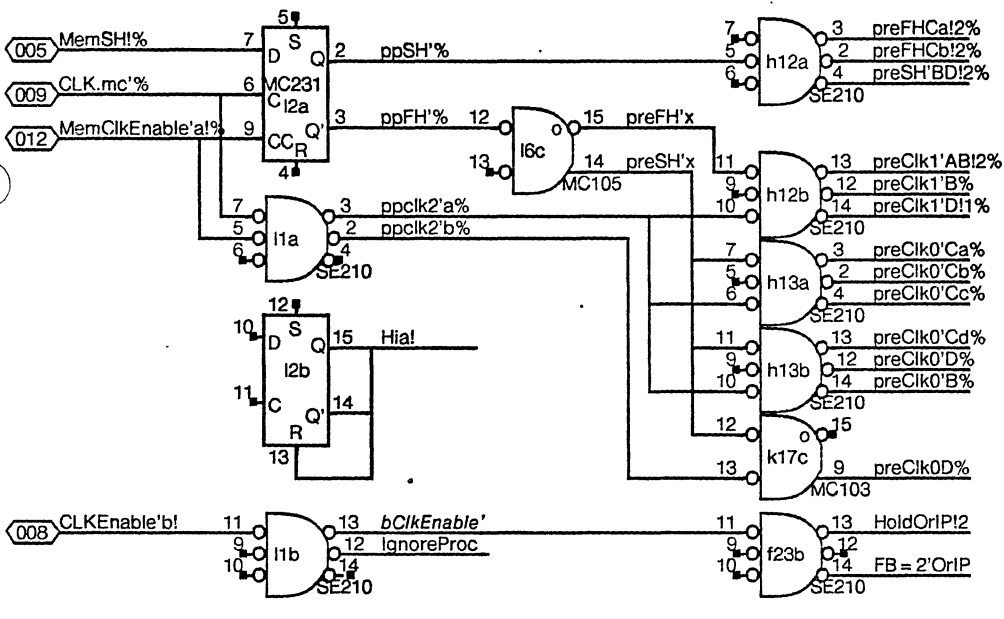
Possible states for Pair:
 PairFull and one of:
 CacheRef (Fetch or Store)
 Prefetch
 IfuRef
 loFetch
 loStore
 Map+
 Flush
 DummyRef (just PairFull)
 Victim
 FlushStore
 PairFull'

MC195
k18g
Invert

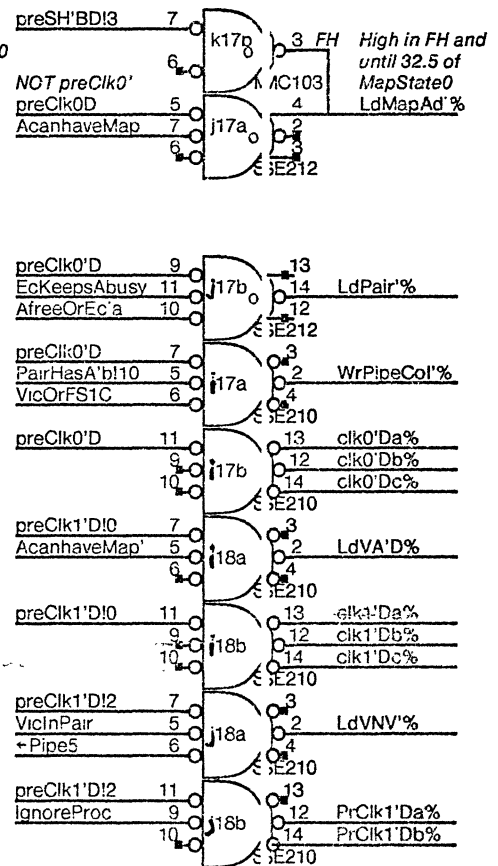
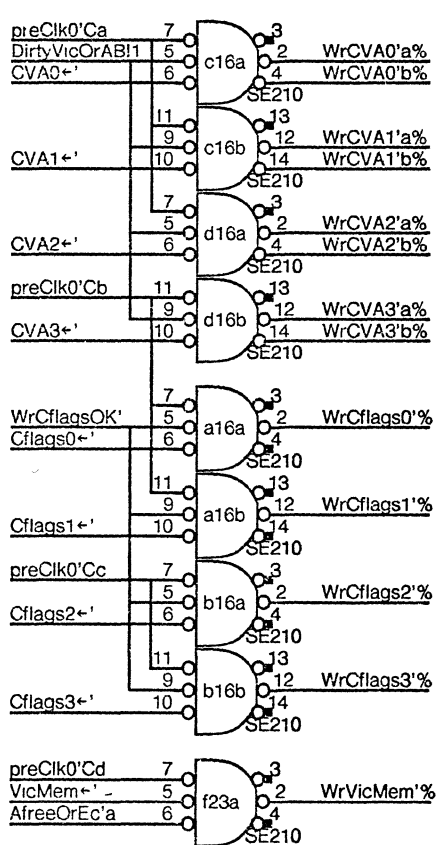








MapAd must be
 low by 12.8 before clk0 of StartMap
 to: let row MapAd through by 6 before clk0
 high from clk0 or StartMap to 27.5 after
 to: hold row MapAd
 low by 2.8 before clk0 after StartMap
 to: let col MapAd through by 4 after clk0



CLKE n	Clk Sync	CLK.mem	Rup	Rish																					
8	1	9	16																						
BMux 0/8	BMux 93	ifuData	Mar 7/15	dDad.02-10																					
A	a	181	b	168	c	153	d	137	e	124	f	109	15	g	80	h	64	i	48	j	33	k	20	l	B
1	RMar 0189 DMadr.2,5 195i	BD 0189	RMar 2-4,10-12 195i	BMux driver			231011	451213	671415	2-5 158	6-9 dDad 2-13 158	10-13 158	MemB+37 +Pipe015' 1662	PipeVAdly 28-31 F16	Clock 210	1									
2	MU ProcVA 24-31	Proc 197	5-7,13-15 195i	176	RBMux 4,8-12 197		5-7,13-15 197	Pipe 20-31 PipeAd!2			VA Hiib	PipeAd!3 141	ovh lia 231	2											
3	dVA buf 22-27 195	VA/dr 26-31 176	MU PrVA56,20-23 MemB.0-1	ProcVA & dr 197		4-13 8 5/20,6/21	197	Pipe 4-15 PipeAd!1			17-27 176	Pipe 16-19 PipeAd!4	PipeTag F16	3											
4	24-27 181k	Adder 181k	28-31 181k	4-7 181k	Adder 181k	12-15 181k	8-11 181k	Adder 181k	16-19 181k	ProcVA & dr 197 14 19 176			145	4											
5	ProcVA & dr 197 20 25 176		Cout.24' 117	ifuD/BR 24-31 173		BR latch 4,20-23 175	Cout12,20' 179	5,8-11 175	BR latch 6,16-19	7,12-15 175	sAad.0-5 197	disPipe/3 +Pipe15' 103	5												
6	20-23 181k	Adder 181k	20-23 181k	Base register RAMs			Base register RAMs			Base register RAMs			MemB.0! D+ec,pSHx 105	6											
7	dVAbuf.20-23 dVA.56/2021 195i	dAad.0-3 mux 1662		24-27 145	28-31 145	20-23 145	MemB.1-4 101	8-11 145	16-19 145	12-15 145	4-7 145	FF PRck1 176	7												
8	Aada	Aad'a	Aadb	Aad'b	LdProcVA' WrBrHi' 210	Cflags reg 176	Cf+RMar 100	New 174	Clocks			Mcr 176	decod- 162	8											
9	Cache flags				Miss←Cflags 104		Cflags reg BL + 176	sAad 6-7 197	176			ing PRck1 176	9												
10	A bits 16-19			Comparators			Victad	Cflags 105	Dirty 141	SEBL WantCH 109	Mcr 176	MU 161	10												
11	16-19			Comparators			Victad	16-19 174	HitColDirty Parity 174	AbusyFS WantCH 117	MemB.2-4 +5	MU PipeAd +4	11												
12	A bits 12-15			Comparators			Victad	Pre 210	DirtyVicOrAB dHitPerr SEBL 174	106	VAdly 173	+	12												
13	12-15			Comparators			Victad	12-15 210	clocks 210	dVA.12-19 parity 170	Afree 211	Dbuf+ AtookST 135	Next/2 MB.0 176.0	13											
14	2/3	0	1	2/3	Dad.0-1 231	Col 1660	Col.0-1 231	PipeCol 174	145	210	104	MU 104	14												
15	4/5 1668	6/7	4/5	6/7 1668	Hold 1660	1660	ColVic.0-1 NewR,HorEc 1662	ifuAck'1 +PrVA/2 EcKeepsAB 102	Lfatch EwAdly ABdly MCS 176.1	+MdDly' 231 1	StartMap 121	Afree! AwST/2 KillItuRef 102	15												
16	CVA/Cflags clocks				210	1660	Hit 171	Clk En 211	Add' 102	Cflags misc 121	WrCflagsOK 121	105	+	16											
17	MU PrVA 4,7-19 +2	WantPRdly DbufBusy 231	ifuAck!Hit 231	ProcTchMem 1660	1660	1660	Hit 231	HitOrEc' Col = Vic' 1672	Clocks			+preClk0 MapAdLd SIST,-VicA 103	+	17											
18	A bits 8-11			Comparators			Victad	Col = NV' preMCS New 1672	Pair/3 Next/2 +VictAd 195i	Pair 195i	MU 103	18													
19	8-11			Comparators			Victad	8-11 1662	VNV EnVNV 170	dVA.4-11 parity 170	WantVic! VicM-,RdInA AwDfHit 102	ForceMiss Vic!Miss 109	VicOrFSIC (EchAsA) 100	19											
20	A bits 7, 20-21, parity or bits 4-7				Comparators			Victad	stuff 159	Parity PrVAck1 176	101	PairInA (EchAsA) 101	20												
21	4,7,20-21 or 4-7			Comparators			Victad	4,7,20- or 4-7 102	Vic.1',IoFIA AchMap dDbufBusy 102	BPCHP.Pr/2 JsaAsrndly MdPend. 176.0	176	Pair 176	MU Pair	21											
22	MU Aad	dMdH,dPerr dVA.4/par 107	VNV	WantCR,CR dMdC,PipH 117	RefH, MdH 231	MU xHold/3 BLretry VNV	VNV 173	VA 4-7,9 176	FastD+Dbuf MakeF+D! 1660	St+ ,ifuRef Abusy 105	Pref,IoRef DntLdPrVA! 104	Midas/2! D+Dbuf Pcol+Vic 103	22												
23	ASEL12 mkD+CD 195i	dMDhold 121	RAM	xxHold dMiscH 210	MiscH, BLrty 231	WrVicMem IP buf 210	NextV' Vic.0' FF-5-7' 195i	MU 78 173	117	dVic/FS 101	Pair/3,MDd (HoldOrIP) 101	164	Midas 164	23											
24	WantRef decodes 162	WantPR! DcomingH St+icr,wAR 103	xxHold CacheRef' 212	dDbufHold PCHP 109	FB decode 171	UseAsrn 121	1-4 173	MapAd .056 173	MemAd 159	Ref decodes 161	overhead 176 176		24												

C a 11 b 26 c 39 d 55 e 70 f 86 g 99 h 114 i 129 j 143 k 159 l 174 D
 Exxx +MDI +MD Asel FF.0-3 PRhold FF.4-7 MemBase MemAd 5-8

CACHE CONFIGURATIONS

THIS ONE

4k CacheConfig = 3			16k CacheConfig = 2			16k without parity CacheConfig = 1		
Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)
a03	195	3x 4x cut 5-6 from 5/20-6/21	a03	195	3-6 4-7 connect 5-6 to 5/20-6/21	a03	195	3-6 4-7 connect 5-6 to 5/20-6/21
a07	195	2-15 3-4 connect 20-21 to 5/20-6/21	a07	195	2x 4x cut 20-21 from 5/20-6/21	a07	195	2x 4x cut 20-21 from 5/20-6/21
a05	197	3x 4x read ProcVA.20-21 for CVA	d03	197	2x 15x read ProcVA.20-21 for row	d03	197	2x 15x read ProcVA.20-21 for row
b14	1668	remove disconnect Aad.0						
c14	1668	remove disconnect Aad.1						
e20	113	3x	e20	113	3x	b22	107	7x 9x 14x 15x 6-10 connect 4 to 4/par disconnect Perr reporting
e21	113	3x	e21	113	3x			
f20	113	3x	f20	113	3x			
f21	113	3x keep parity from comparators	f21	113	3x			
g20	174	2x keep parity from CVA	g20	174	2x			
			i11	164	12x make CacheConfig = 2	i11	164	11x make CacheConfig = 1

PAGE SIZE CONFIGURATIONS

THIS ONE

256 words PageConfig = 3			1k words PageConfig = 2			4k words PageConfig = 1		
Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)
i24	159	4x 6x 11x 13x 4-6-11-13-9 MemRA+0000	i24	159	11x 13x 11-13-9 MemRA+00 22 23			MemRA+20 21 22 23
			h24	173	3x 4x 1-2 MapAd.0+4-5 for 6-7	h24	173	10x 12x 10-3 12-5 MapAd.5,6+5,7 for 20,21
			i23	173	3x 10x 3-5 10-12 MapAd.7,8+6,7 for 22,23	i23	173	3x 10x 3-5 10-13 MapAd.7,8+6,4 for 22,23
			i11	164	14x make PageConfig = 2	i11	164	13x make PageConfig = 1

Note: Muffler signals 1144-1147 specify the configuration as follows:

1144-1145 are CacheConfig

1146-1147 are PageConfig

and the meaning of their values is as listed in the tables above

Need information here about the two missing holes

CURRENTLY NONE

XEROX PARC	<i>Project</i> Dorado	<i>Reference</i> Multiwire rev changes	<i>File</i> MemC24.sil	<i>Designer</i> Lampson	<i>Rev</i> Be	<i>Date</i> 7/01/79	<i>Page</i> 24
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Page Numbers: Yes First Page: 1
 Columns: 2 Edge Margin: .8" Between Columns: .0"
 Heading:
 MemC-Rev-Be.ps
 COMPONENTS:

F145A:	1	5	7	8	9	10
	14					
F16:	1	5	10			
F181K:	1	7	8	9	10	14
MB071:	1	2	3	4	11	12
	13					
MC100:	2	17				
MC101:	16	17	19			
MC102:	2	4	16	17	18	
MC103:	15	16	18	19	20	21
MC104:	2	3	17			
MC105:	2	16	17	18	19	21
MC106:	5	15	18			
MC107:	5	16				
MC109:	15	17				
MC113:	1	11	12			
MC117:	14	15	16	17		
MC121:	2	16	18			
MC135:	18					
MC141:	2	3	19			
MC158:	1	9	10	14		
MC159:	1	4	6	9	10	
MC161:	17	19				
MC162:	16	19				
MC1660:	15	18				
MC1662:	1	4	9	15	16	19
MC1668:	1	13				
MC1672:	1	4	15			
MC170:	5					
MC171:	2	19				
MC173:	1	4	7	8	9	10
	14					
MC174:	1	2	5	11	12	13
	15					
MC175:	1	7	8	9	14	
MC176:	1	2	3	4	5	7
	8	9	10	14	15	16
	17	18	19	20		
MC179:	14					
MC195:	1	2	4	6	9	10
	14	16	17	18	19	20
MC197:	1	2	6	7	8	9
	10	14				
MC210:	15	18				
MC211:	16	18				
MC212:	15	17				
MC231:	15	16	18	21		
MU164:	20					
SE210:	21					
SE212:	21					
TERM:	1	7	9			

SIGNAL NAMES:

(FB=6&PCHP')':	15(1)	19(1)				
+	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)
	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
	19(1)	20(1)	21(1)			
Aad.0'a!1:	3(1)	13(2)				
Aad.0'a!2:	13(1)					
Aad.0'a!3:	13(2)					
Aad.0'b!1:	3(1)	13(2)				
Aad.0'b!2:	13(1)					
Aad.0'b!3:	4(1)	13(2)				
Aad.0a!1:	1(1)	2(1)	13(1)			
Aad.0a!2:	13(1)					
Aad.0a!3:	13(2)	20(1)				
Aad.0b!1:	3(1)	13(2)				

Aad.0b!2:	13(1)		
Aad.0b!3:	13(2)		
Aad.1'a!1:	3(1)	13(2)	
Aad.1'a!2:	13(1)		
Aad.1'a!3:	13(2)		
Aad.1'b!1:	3(1)	13(2)	
Aad.1'b!2:	13(1)		
Aad.1'b!3:	4(1)	13(2)	
Aad.1a!1:	1(1)	2(1)	13(1)
Aad.1a!2:	13(1)		
Aad.1a!3:	13(2)	20(1)	
Aad.1b!1:	3(1)	13(2)	
Aad.1b!2:	13(1)		
Aad.1b!3:	13(2)		
Aad.2'a!1:	3(1)	13(2)	
Aad.2'a!2:	13(1)		
Aad.2'a!3:	13(2)		
Aad.2'b!1:	3(1)	13(2)	
Aad.2'b!2:	13(1)		
Aad.2'b!3:	4(1)	13(2)	
Aad.2a!1:	1(1)	2(1)	13(1)
Aad.2a!2:	13(1)		
Aad.2a!3:	13(2)	20(1)	
Aad.2b!1:	3(1)	13(2)	
Aad.2b!2:	13(1)		
Aad.2b!3:	13(2)		
Aad.3'a!1:	3(1)	13(2)	
Aad.3'a!2:	13(1)		
Aad.3'a!3:	13(2)		
Aad.3'b!1:	3(1)	13(2)	
Aad.3'b!2:	13(1)		
Aad.3'b!3:	4(1)	13(2)	
Aad.3a!1:	1(1)	2(1)	13(1)
Aad.3a!2:	13(1)		
Aad.3a!3:	13(2)	20(1)	
Aad.3b!1:	3(1)	13(2)	
Aad.3b!2:	13(1)		
Aad.3b!3:	13(2)		
Aad.4'a!1:	3(1)	13(2)	
Aad.4'a!2:	13(1)		
Aad.4'a!3:	13(2)		
Aad.4'b!1:	3(1)	13(2)	
Aad.4'b!2:	13(1)		
Aad.4'b!3:	4(1)	13(2)	
Aad.4a!1:	1(1)	2(1)	13(1)
Aad.4a!2:	13(1)		
Aad.4a!3:	13(2)	20(1)	
Aad.4b!1:	3(1)	13(2)	
Aad.4b!2:	13(1)		
Aad.4b!3:	13(2)		
Aad.5'a!1:	3(1)	13(2)	
Aad.5'a!2:	13(1)		
Aad.5'a!3:	13(2)		
Aad.5'b!1:	3(1)	13(2)	
Aad.5'b!2:	13(1)		
Aad.5'b!3:	4(1)	13(2)	
Aad.5a!1:	1(1)	2(1)	13(1)
Aad.5a!2:	13(1)		
Aad.5a!3:	13(2)	20(1)	
Aad.5b!1:	3(1)	13(2)	
Aad.5b!2:	13(1)		
Aad.5b!3:	13(2)		
Aad.6'a!1:	3(1)	13(2)	
Aad.6'a!2:	13(1)		
Aad.6'a!3:	13(2)		
Aad.6'b!1:	3(1)	13(2)	
Aad.6'b!2:	13(1)		
Aad.6'b!3:	4(1)	13(2)	
Aad.6a!1:	1(1)	2(1)	13(1)
Aad.6a!2:	13(1)		
Aad.6a!3:	13(2)	20(1)	
Aad.6b!1:	3(1)	13(2)	
Aad.6b!2:	13(1)		
Aad.6b!3:	13(2)		
Aad.7'a!1:	3(1)	13(2)	
Aad.7'a!2:	1(1)		

Aad.7'a!3:	13(2)				
Aad.7'b!1:	3(1)	13(2)			
Aad.7'b!2:	1(1)				
Aad.7'b!3:	4(1)	13(2)			
Aad.7a!1:	1(1)	2(1)	13(1)		
Aad.7a!2:	1(1)				
Aad.7a!3:	13(2)	20(1)			
Aad.7b!1:	3(1)	13(2)			
Aad.7b!2:	1(1)				
Aad.7b!3:	13(2)				
Abusy:	2(1)	17(1)			
AbusyForSure:	15(1)	18(1)			
AcanhaveD:	14(1)	15(1)	18(2)		
AcanhaveMap:	1(1)	14(1)	15(1)	18(1)	21(1)
AcanhaveMap':	18(1)	21(2)			
Add'a:	14(2)	16(1)			
Add'b!6:	14(2)				
Add'b!7:	14(1)				
Add'b!8:	14(1)				
Add'b!9%:	16(1)				
Afree':	18(2)	20(1)			
AfreeOrEc'a:	18(2)	21(2)			
AfreeOrEc'b:	2(1)	18(1)			
ASEL.0:	16(1)				
ASEL.0'mem:	19(1)				
ASEL.1:	16(1)				
ASEL.1'!:	16(1)				
ASEL.2:	15(1)	16(1)	17(1)		
ASEL.2'!:	16(1)				
At=Curt':	16(1)				
AtookST:	15(1)	18(1)	20(1)		
AwantsDifHit':	15(1)	17(1)	18(1)		
AwantsMapFS:	15(1)	17(2)			
AwantsMapFS':	15(1)	17(1)	18(1)	20(1)	
AwasFree':	17(1)	18(1)	20(1)	21(2)	
AwST'vAfree:	18(2)				
bEcHasA:	17(2)	20(1)			
BL1:	2(1)	3(1)			
BL2:	2(1)	3(1)			
BL3:	2(1)	3(1)			
BLretry:	15(1)	18(3)	20(1)		
BMux.00!:	6(1)				
BMux.01!:	6(1)				
BMux.02!:	6(1)				
BMux.03!:	6(1)				
BMux.04!:	6(1)				
BMux.05!:	6(1)				
BMux.06!:	6(1)				
BMux.07!:	6(1)				
BMux.08!:	6(1)				
BMux.09!:	6(1)				
BMux.10!:	6(1)				
BMux.11!:	6(1)				
BMux.12!:	6(1)				
BMux.13!:	6(1)				
BMux.14!:	6(1)				
BMux.15!:	6(1)				
BrHi←':	19(2)	21(1)			
BrLo←':	19(2)	21(1)			
CacheRef'!0:	17(1)				
CacheRef'!1:	17(2)				
CacheRefInA:	5(1)	17(3)	20(1)		
CacheRefInA':	16(1)	17(1)			
CacheRefInEc1!:	5(1)				
CBHold:	15(1)				
Cflags0←':	2(1)	21(1)			
Cflags1←':	2(1)	21(1)			
Cflags2←':	2(1)	21(1)			
Cflags3←':	2(1)	21(1)			
CflagsCE'!1:	2(1)				
CflagsCE'!2:	3(1)				
CflagsCE'!3:	2(1)				
CflagsCE'!4:	3(1)				
CflagsCE'!5:	3(1)				
Cflags←':	2(2)	19(1)			
CHoldReq:	15(1)				

CLK.mc%:	21(1)		
clk0'A:	5(1)	19(1)	
clk0'A%:	21(1)		
clk0'B:	21(2)		
clk0'B%:	21(1)		
clk0'Da:	18(2)		
clk0'Da%:	21(1)		
clk0'Db:	18(1)		
clk0'Db%:	21(1)		
clk0'Dc:	15(1)		
clk0'Dc%:	21(1)		
clk1'B!1:	2(1)		
clk1'B!2%:	21(1)		
clk1'B!3:	1(1)		
clk1'Da:	15(1)	16(2)	
clk1'Da%:	21(1)		
clk1'Db:	16(2)		
clk1'Db%:	21(1)		
clk1'Dc:	15(2)		
clk1'Dc%:	21(1)		
clk1B:	18(1)		
clk1B%:	21(1)		
CLKEnable'b!:	21(1)		
C012':	14(2)		
C016':	14(2)		
C020':	14(2)		
C024&Add!1:	1(1)	9(1)	
C024&Add!2:	14(1)		
C024&Add!3:	9(2)		
C024'vAdd'!1:	1(1)	9(1)	
C024'vAdd'!2:	14(1)		
C024'vAdd'!3:	9(2)		
C08':	14(2)		
Co1.0'!1:	2(1)	5(1)	
Co1.0'!2%:	15(1)		
Co1.0'!3:	4(1)		
Co1.0'!4:	4(1)		
Co1.1'!1:	2(1)	5(1)	
Co1.1'!2%:	15(1)		
Co1.1'!3:	4(1)		
Co1.1'!4:	4(1)		
Co1Vic.0:	2(1)	5(1)	20(1)
Co1Vic.0%:	15(1)		
Co1Vic.1:	2(1)	5(1)	20(1)
Co1Vic.1%:	15(1)		
CVA0.4/par:	5(1)	11(1)	
CVA0←':	2(1)	21(1)	
CVA1.4/par:	5(1)	11(1)	
CVA1←':	2(1)	21(1)	
CVA2.4/par:	5(1)	11(1)	
CVA2←':	2(1)	21(1)	
CVA3.4/par:	5(1)	11(1)	
CVA3←':	2(1)	21(1)	
dAad.0'!1:	9(1)		
dAad.0'!2:	9(1)		
dAad.0'!3:	13(1)		
dAad.1'!1:	1(1)		
dAad.1'!2:	1(1)		
dAad.1'!3:	13(1)		
dAad.2'!1:	9(1)		
dAad.2'!2:	9(1)		
dAad.2'!3:	13(1)		
dAad.3'!1:	9(1)		
dAad.3'!2:	9(1)		
dAad.3'!3:	13(1)		
dAad.4:	9(1)	13(1)	
dAad.5:	9(1)	13(1)	
dAad.6:	10(1)	13(1)	
dAad.7:	1(2)		
Dad.00:	15(1)		
Dad.01:	15(1)		
dBLO:	2(1)	15(1)	
dBLL1:	3(1)	15(1)	
dBLL2:	3(1)	15(1)	
dBLL3:	3(1)	15(1)	
DbufBusy:	18(1)	20(1)	

DbufBusy':	15(1)	18(1)		
Dbuf←':	18(1)			
Dbusy:	15(1)	16(1)	18(3)	20(1)
DcomingForCt':	16(1)			
dDad.02!:	9(1)			
dDad.03!:	1(1)			
dDad.04!:	9(1)			
dDad.05!:	9(1)			
dDad.06!:	9(1)			
dDad.07!:	9(1)			
dDad.08!:	10(1)			
dDad.09!:	1(1)			
dDad.10:	10(1)			
dDad.11:	10(1)			
dDad.12:	10(1)			
dDad.13:	1(1)			
DdataGood':	16(1)			
dHitPerr:	5(1)			
Dirty0:	2(3)			
Dirty1:	2(3)	3(1)		
Dirty2:	2(3)	3(1)		
Dirty3:	2(3)	3(1)		
DirtyIoFetchInA':	17(1)			
DirtyVicOrAB!1:	21(1)			
DirtyVicOrAB!2:	2(1)	18(1)		
DirtyVicOrAB!3:	17(1)			
DisBR:	5(1)	19(1)	20(1)	
DisCFlags:	2(1)	5(1)	20(1)	
DisHold:	15(3)	20(1)		
DisHold!:	5(1)			
DisPipe20-31:	14(1)	19(1)		
DisPipe4-15:	14(1)	19(1)		
DMadr.01:	20(2)			
DMadr.02:	20(3)			
DMadr.03:	20(3)			
DMadr.04:	20(3)			
DMadr.05:	20(10)			
DMadr.05':	20(6)			
DMadr.06:	20(2)			
DMadr.07:	20(2)			
DMadr.08:	20(2)			
DMadr.09:	20(15)			
DMadr.10:	20(15)			
DMadr.11:	20(15)			
dMDhold':	15(1)	16(1)		
dMiss0.04-11!1:	1(1)	11(1)		
dMiss0.04-11!2:	11(1)			
dMiss0.04-11!3:	15(1)			
dMiss0.12-15!2:	12(1)			
dMiss0.12-15!3:	15(1)			
dMiss0.16-19!1:	2(2)			
dMiss0.16-19!2:	12(1)			
dMiss0.16-19!3:	15(1)			
dMiss1.04-11!1:	1(1)	11(1)		
dMiss1.04-11!2:	11(1)			
dMiss1.04-11!3:	15(1)			
dMiss1.12-15!2:	12(1)			
dMiss1.12-15!3:	15(1)			
dMiss1.16-19!1:	3(2)			
dMiss1.16-19!2:	12(1)			
dMiss1.16-19!3:	15(1)			
dMiss2.04-11!1:	1(1)	11(1)		
dMiss2.04-11!2:	11(1)			
dMiss2.04-11!3:	15(1)			
dMiss2.12-15!2:	12(1)			
dMiss2.12-15!3:	15(1)			
dMiss2.16-19!1:	3(2)			
dMiss2.16-19!2:	12(1)			
dMiss2.16-19!3:	15(1)			
dMiss3.04-11!1:	1(1)	11(1)		
dMiss3.04-11!2:	11(1)			
dMiss3.04-11!3:	15(1)			
dMiss3.12-15!2:	12(1)			
dMiss3.12-15!3:	15(1)			
dMiss3.16-19!1:	3(2)			
dMiss3.16-19!2:	12(1)			

dMiss3.16-19!3:	15(1)					
DMuxC1k!:	20(1)					
DMuxData:	20(1)					
DMuxData!:	20(1)					
DontLdProcVA:	17(1)	21(2)				
dPipe02Ad.0:	19(1)					
dPipe02Ad.1:	19(1)					
dPipe02Ad.2:	19(1)					
dPipe02Ad.3:	19(1)					
dVA.04:	5(1)	7(1)	11(1)			
dVA.05:	7(1)	9(1)				
dVA.06:	1(1)	7(1)				
dVA.07:	5(1)	7(1)	11(1)			
dVA.08:	5(1)	7(1)	11(1)			
dVA.09:	5(1)	7(1)	11(1)			
dVA.10:	5(1)	7(1)	11(1)			
dVA.11:	5(1)	7(1)	11(1)			
dVA.12:	5(1)	8(1)	12(1)			
dVA.13:	5(1)	8(1)	12(1)			
dVA.14:	5(1)	8(1)	12(1)			
dVA.15:	5(1)	8(1)	12(1)			
dVA.16:	5(1)	8(1)	12(1)			
dVA.17:	5(1)	8(1)	12(1)			
dVA.18:	5(1)	8(1)	12(1)			
dVA.19:	5(1)	8(1)	12(1)			
dVA.21:	1(1)					
dVA.5/20!6:	5(1)	7(1)	9(1)			
dVA.5/20!7:	11(1)					
dVA.5/20!8:	9(1)					
dVA.5/20!9:	9(1)					
dVA.6/21!6:	1(1)	5(1)	7(1)			
dVA.6/21!7:	1(1)					
dVA.6/21!8:	1(1)					
dVA.6/21!9:	1(1)					
dVA+Vic:	5(1)	15(1)	16(1)	20(1)		
EchAsA':	1(1)	2(1)	5(1)	14(1)	15(1)	17(1)
	18(1)					
EcHasAa!1:	19(1)					
EcHasAa!2:	17(1)					
EcHasAa!3:	1(1)	2(1)	15(1)			
EcHasAb:	15(1)	17(4)				
EcKeepsAbusy:	15(1)	18(1)	21(1)			
EcWantsA:	15(2)	17(2)	18(1)			
EcWantsAdly:	16(1)	17(1)				
EmuOrFT':	16(1)	17(1)				
ExtHoldReq:	15(1)					
FA=1':	15(1)	19(1)				
FastAdd':	1(1)	14(1)				
FastAdd'%:	16(1)					
FastD+Dbuf:	18(1)					
FB=2'OrIP:	19(2)	21(1)				
FB=6&PCHP':	15(1)	19(2)				
FF.0mem':	16(1)					
FF.1mem:	16(1)	17(1)				
FF.2!:	19(1)					
FF.3!:	19(1)					
FF.4!:	19(1)					
FF.5!:	19(1)					
FF.5':	19(3)					
FF.6!:	19(1)					
FF.6':	19(3)					
FF.7!:	19(1)					
FF.7':	19(3)					
FlushInA:	2(1)	4(1)	15(2)	17(3)	20(1)	
FlushStore:	5(1)	15(1)	17(3)			
Flush+':	17(2)					
ForceDirtyMiss:	2(1)	5(1)	17(2)	20(1)		
ForceMiss:	15(4)	17(1)				
FSinPair':	17(2)	20(1)				
G12-15':	14(2)					
G16-19':	14(2)					
G20-23':	14(2)					
G24-27':	1(1)	14(2)				
G28-31':	1(1)	14(3)				
Gnd:	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)

	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
	19(1)	20(1)	21(1)			
Hia:	1(2)	14(1)	15(1)	18(2)	20(1)	
Hia!:	21(1)					
Hib:	1(1)	5(1)	14(10)	20(1)		
Hib!:	14(1)					
Hit'a!1:	18(3)					
Hit'a!2%:	15(1)					
Hit'a!3:	2(1)	16(1)				
Hit'b!1:	5(1)					
Hit'b!2:	2(1)					
Hit'b!3:	2(1)					
Hit'b!4%:	15(1)					
Hit'b!5:	18(1)					
Hit'b!6:	5(1)					
Hita:	2(1)	4(1)	15(1)	18(1)	20(1)	
HitColDirty:	2(1)	17(2)	20(1)			
HitColVA.par:	5(1)	20(1)				
HitOrEc:	15(1)	17(1)				
Hold!1:	16(1)	18(1)				
Hold!2%:	15(1)					
Hold!3:	15(1)					
HoldMapBuf:	6(1)					
HoldOrIP!1:	17(2)					
HoldOrIP!2:	15(1)	21(1)				
HoldOrIP!3:	21(3)					
Ifetch←:	1(1)	14(1)	16(1)			
IfuAck!:	16(1)					
IfuAck':	16(1)	17(1)				
IfuAckIfHit':	16(1)	18(1)				
IfuData.0:	9(1)					
IfuData.1:	9(1)					
IfuData.2:	10(1)					
IfuData.3:	1(1)					
IfuData.4:	10(1)					
IfuData.5:	10(1)					
IfuData.6:	10(1)					
IfuData.7:	1(1)					
IfuHold:	15(1)					
IfuRefInA:	5(1)	17(3)	20(1)			
IfuRefInA':	17(1)	18(1)				
IfuRefInEc!:	5(1)					
IgnoreProc:	16(2)	21(2)				
IoFetchInA:	17(2)					
IoFetchInA'!:	17(1)					
IOHold:	15(1)					
IoRefInA':	17(2)	20(1)				
IoStoreInA:	2(2)	15(1)	17(2)	18(1)	20(1)	
IoStoreInA':	15(1)	17(1)				
KillIfuRef:	17(1)	18(1)	20(1)			
LdMapAd':	1(1)	14(1)				
LdMapAd'%:	21(1)					
LdMcr':	4(1)	5(1)				
LdMcr'%:	21(1)					
LdPair':	17(1)					
LdPair'%:	21(1)					
LdPipeVAdly':	1(1)					
LdProcVA'Aa:	14(1)					
LdProcVA'Aa%:	21(1)					
LdProcVA'Ab:	14(1)					
LdProcVA'Ab%:	21(1)					
LdProcVA'B:	1(1)					
LdProcVA'B%:	21(1)					
LdProcVA'D:	5(1)					
LdProcVA'D%:	21(1)					
LdVA'B:	14(1)					
LdVA'B%:	21(1)					
LdVA'D:	1(1)					
LdVA'D%:	21(1)					
LdVNV':	4(1)					
LdVNV'%:	21(1)					
Lfetch←:	6(1)	16(1)				
MakeD←CD:	2(1)					
MakeD←Dbuf:	18(1)					
MakeF←D!:	18(1)					
MapAd.0:	7(1)	20(1)				

MapAd.1:	7(1)	20(1)		
MapAd.2:	8(1)	20(1)		
MapAd.3:	8(1)	20(1)		
MapAd.4:	8(1)	20(1)		
MapAd.5:	9(1)	20(1)		
MapAd.6:	1(1)	20(1)		
MapAd.7:	9(1)	20(1)		
MapAd.8:	9(1)	20(1)		
MapRfsh':	18(1)			
MapTroubleInEc1:		2(2)		
MapWait-D:	18(1)			
Map←':	17(2)			
Map←InPair':	17(1)	20(1)		
MAR.00':	6(1)	8(1)		
MAR.01':	6(1)	8(1)		
MAR.02':	6(1)	8(1)		
MAR.03':	6(1)	8(1)		
MAR.04':	6(1)	9(1)		
MAR.05':	1(1)	6(1)		
MAR.06':	6(1)	9(1)		
MAR.07':	6(1)	9(1)		
MAR.08':	6(1)	9(1)		
MAR.09':	6(1)	9(1)		
MAR.10':	6(1)	10(1)		
MAR.11':	1(1)	6(1)		
MAR.12':	6(1)	10(1)		
MAR.13':	6(1)	10(1)		
MAR.14':	6(1)	10(1)		
MAR.15':	1(1)	6(1)		
McrD←'!:	19(1)			
Mcr←':	19(1)	21(1)		
MD0:	20(3)			
MD1:	20(3)			
MD2:	20(3)			
MD3:	20(3)			
MD4:	20(3)			
MD5:	20(2)			
MD6:	20(2)			
MD7:	20(2)			
MDhold':	15(1)	20(1)		
MDMtag':	16(1)			
MDpending':	15(1)	16(1)		
MemAd.5!:	9(1)			
MemAd.6!:	9(1)			
MemAd.7!:	10(1)			
MemAd.8!:	1(1)			
MemB.0:	1(1)	14(6)	19(1)	20(1)
MemB.0':	1(1)	14(6)	19(1)	
MemB.1!1:	1(1)	14(2)	20(1)	
MemB.1!2:	19(1)			
MemB.1!3:	14(4)			
MemB.1'11:	1(1)	14(2)		
MemB.1'12:	19(1)			
MemB.1'13:	14(4)			
MemB.2!1:	1(1)	14(2)		
MemB.2!2:	19(1)			
MemB.2!3:	14(4)	20(1)		
MemB.2'11:	1(1)	14(2)		
MemB.2'12:	19(1)			
MemB.2'13:	14(4)			
MemB.3!1:	1(1)	14(2)		
MemB.3!2:	19(1)			
MemB.3!3:	14(4)	20(1)		
MemB.3'11:	1(1)	14(2)		
MemB.3'12:	19(1)			
MemB.3'13:	14(4)			
MemB.4!1:	1(1)	14(2)		
MemB.4!2:	19(1)			
MemB.4!3:	14(4)	20(1)		
MemB.4'11:	1(1)	14(2)		
MemB.4'12:	19(1)			
MemB.4'13:	14(4)			
MemBase.0:	19(1)			
MemBase.1:	19(1)			
MemBase.2:	19(1)			
MemBase.3:	19(1)			

MemBase.4:	19(1)			
MemClkEnable'a!%:		21(1)		
MemRfsh:	1(1)			
MemSH!%:	21(1)			
MiscHold':	15(1)	20(1)		
MiscPCHP':	15(1)	20(1)		
MXHold:	15(1)	17(1)		
NewBL:	2(1)	3(3)	6(1)	
NewDirty:	2(1)	3(3)	6(1)	
NewRef:	2(1)	16(1)		
NewVacant:	2(1)	3(3)	6(1)	
NewWP:	2(1)	3(3)	6(1)	
NextV.0:	4(1)	6(1)		
NextV.0':	4(3)	20(1)		
NextV.1:	4(1)	6(1)		
NextV.1':	4(4)	20(1)		
NoRef:	2(1)	5(1)	18(2)	20(1)
P12-15':	14(2)			
P16-19':	14(2)			
P20-23':	14(2)			
P24-27':	1(1)	14(2)		
PairFull':	17(1)	18(2)	20(1)	
PairHasA!1:	2(1)	3(3)		
PairHasA!2:	17(1)			
PairHasA!3:	15(1)	17(1)		
PairHasA'a!10:	5(1)			
PairHasA'a!11:	12(1)			
PairHasA'a!5:	19(1)	21(1)		
PairHasA'a!6:	12(1)			
PairHasA'a!9:	17(1)			
PairHasA'b!10:	21(1)			
PairHasA'b!11:	11(1)			
PairHasA'b!5:	11(1)			
PairHasA'b!8:	2(1)			
PairHasA'b!9:	17(1)			
PipeAd.0!1:	14(3)			
PipeAd.0!2:	14(3)			
PipeAd.0!3:	19(1)			
PipeAd.0!4:	1(1)	5(2)	20(1)	
PipeAd.1!1:	14(3)			
PipeAd.1!2:	14(3)			
PipeAd.1!3:	19(1)			
PipeAd.1!4:	1(1)	5(2)	20(1)	
PipeAd.2!1:	14(3)			
PipeAd.2!2:	14(3)			
PipeAd.2!3:	19(1)			
PipeAd.2!4:	1(1)	5(2)	20(1)	
PipeAd.3!1:	14(3)			
PipeAd.3!2:	14(3)			
PipeAd.3!3:	19(1)			
PipeAd.3!4:	1(1)	5(2)	20(1)	
PipeCacheRef:	5(1)	6(1)		
PipeCol.0:	5(1)	6(1)	15(1)	
PipeCol.1:	5(1)	6(1)	15(1)	
PipeFlushStore:	2(1)	5(1)	6(1)	
PipeIfuRef:	5(1)	6(1)		
PipeStore+':	2(1)	5(1)	6(1)	
PipeTag:	5(1)	6(1)		
PipeVA.16!1:	6(1)			
PipeVA.16!2:	8(1)			
PipeVA.16!3:	9(1)			
PipeVA.17:	6(1)	8(1)		
PipeVA.18:	6(1)	8(1)		
PipeVA.19:	6(1)	8(1)		
PipeVA.20:	6(1)	7(2)	9(1)	
PipeVA.21:	1(1)	6(1)	7(1)	
PipeVA.22:	6(1)	7(2)	9(1)	
PipeVA.23:	6(1)	7(1)	9(1)	
PipeVA.24:	6(1)	7(2)	9(1)	
PipeVA.25:	6(1)	7(1)	9(1)	
PipeVA.26:	6(1)	7(1)	8(1)	10(1)
PipeVA.27:	1(1)	6(1)	7(1)	8(1)
PipeVA.28:	6(1)	8(2)	10(1)	
PipeVA.29:	6(1)	8(1)	9(1)	10(1)
PipeVA.30:	1(1)	6(1)	8(1)	10(1)
PipeVA.31:	1(1)	6(1)	8(1)	9(1)

ppc1k2'a%:	21(1)		
ppc1k2'b%:	21(1)		
ppFH'x%:	21(1)		
ppSH'x%:	21(1)		
PrC1k1'Da:	15(2)		
PrC1k1'Da%:	21(1)		
PrC1k1'Db:	19(2)		
PrC1k1'Db%:	21(1)		
preC1k0'B:	21(1)		
preC1k0'B%:	21(1)		
preC1k0'Ca:	21(1)		
preC1k0'Ca%:	21(1)		
preC1k0'Cb:	21(1)		
preC1k0'Cb%:	21(1)		
preC1k0'Cc:	21(1)		
preC1k0'Cc%:	21(1)		
preC1k0'Cd:	21(1)		
preC1k0'Cd%:	21(1)		
preC1k0'D:	21(3)		
preC1k0'D%:	21(1)		
preC1k0D:	21(1)		
preC1k0D%:	21(1)		
preC1k1'AB!1:	21(1)		
preC1k1'AB!2%:	21(1)		
preC1k1'AB!3:	21(2)		
preC1k1'B:	21(3)		
preC1k1'B%:	21(1)		
preC1k1'D!0:	21(2)		
preC1k1'D!1%:	21(1)		
preC1k1'D!2:	21(2)		
PrefetchInA:	17(2)	20(1)	
preFH'x:	4(1)	21(1)	
preFHCa!1:	13(1)		
preFHCa!2%:	21(1)		
preFHCa!3:	13(1)		
preFHCB!1:	13(1)		
preFHCB!2%:	21(1)		
preFHCB!3:	1(1)	13(1)	
preMCSb:	1(1)		
preSH'BD!1:	21(1)		
preSH'BD!2%:	21(1)		
preSH'BD!3:	21(1)		
preSH'x:	19(1)	21(1)	
PrHold!:	15(1)		
PrHoldReq:	15(1)		
PrivRefInPair:	17(1)	18(1)	20(1)
ProcSrn←'!:	19(1)		
ProcTag:	16(1)		
ProcTagInA:	5(1)		
ProcVA.04:	5(1)	7(1)	20(1)
ProcVA.05:	7(1)	20(1)	
ProcVA.06:	7(1)	20(1)	
ProcVA.07:	7(1)	11(1)	20(1)
ProcVA.08:	7(1)	11(1)	20(1)
ProcVA.09:	7(1)	11(1)	20(1)
ProcVA.10:	7(1)	11(1)	20(1)
ProcVA.11:	7(1)	11(1)	20(1)
ProcVA.12:	8(1)	12(1)	20(1)
ProcVA.13:	8(1)	12(1)	20(1)
ProcVA.14:	8(1)	12(1)	20(1)
ProcVA.15:	8(1)	12(1)	20(1)
ProcVA.16:	8(1)	12(1)	20(1)
ProcVA.17:	8(1)	12(1)	20(1)
ProcVA.18:	8(1)	12(1)	20(1)
ProcVA.19:	8(1)	12(1)	20(1)
ProcVA.20:	9(1)	20(1)	
ProcVA.21:	1(1)	20(1)	
ProcVA.22:	9(1)	20(1)	
ProcVA.23:	9(1)	20(1)	
ProcVA.24:	9(1)	20(1)	
ProcVA.25:	9(1)	20(1)	
ProcVA.26:	10(1)	20(1)	
ProcVA.27:	1(1)	20(1)	
ProcVA.28:	10(1)	20(1)	
ProcVA.29:	10(1)	20(1)	
ProcVA.30:	10(1)	20(1)	

ProcVA.31:	1(1)	20(1)			
PrVA.4/Par:	5(1)	11(1)			
PrVA.5/20:	9(1)	11(1)			
PrVA.6/21:	1(2)				
RBMux.04:	6(1)	7(1)			
RBMux.05:	6(1)	7(1)			
RBMux.06:	6(1)	7(1)			
RBMux.07:	6(1)	7(1)			
RBMux.08:	6(1)	7(1)			
RBMux.09:	6(1)	7(1)			
RBMux.10:	6(1)	7(1)			
RBMux.11:	6(1)	7(1)			
RBMux.12:	6(1)	8(1)			
RBMux.13:	6(1)	8(1)			
RBMux.14:	6(1)	8(1)			
RBMux.15:	6(1)	8(1)			
ReadInA':	17(1)				
RefHold':	15(1)	18(1)	20(1)		
RefOutstanding':		18(1)			
RMar.00:	5(1)	6(1)	8(1)		
RMar.01:	5(1)	6(1)	8(1)		
RMar.02:	4(1)	6(1)	8(1)		
RMar.03:	4(1)	6(1)	8(1)		
RMar.04:	4(1)	6(1)	7(1)	9(1)	
RMar.05:	1(1)	4(1)	6(1)	7(1)	
RMar.06:	4(1)	6(1)	7(1)	9(1)	
RMar.07:	5(1)	6(1)	7(1)	9(1)	
RMar.08:	2(1)	5(1)	6(1)	7(1)	9(1)
RMar.09:	2(1)	5(1)	6(1)	7(1)	9(1)
RMar.10:	2(1)	5(1)	6(1)	7(1)	10(1)
RMar.11:	1(1)	2(1)	6(1)	7(1)	
RMar.12:	6(1)	8(1)	10(1)		
RMar.13:	6(1)	8(1)	10(1)		
RMar.14:	6(1)	8(1)	10(1)		
RMar.15:	1(1)	6(1)	8(1)		
sAad.0:	9(1)	13(1)			
sAad.1:	1(1)	13(1)			
sAad.2:	9(1)	13(1)			
sAad.3:	9(1)	13(1)			
sAad.4:	9(1)	13(1)			
sAad.5:	9(1)	13(1)			
sAad.6:	10(1)	13(1)			
sAad.7:	1(2)				
SH'A:	1(2)	14(1)			
SH'A%:	21(1)				
SH'Ba:	14(1)	19(1)			
SH'Ba%:	21(1)				
SH'Bb:	18(1)				
SH'Bb%:	21(1)				
SomeExtHold':	15(1)	20(1)			
StartMap':	18(1)	20(1)			
STFree:	15(1)	18(1)			
STfree':	18(1)				
Store←:	17(1)	18(1)			
Store←':	17(1)	18(1)			
Store←IfCR':	16(1)	17(1)			
Store←InA:	2(1)	3(3)	15(1)	17(1)	20(1)
Store←InA':	2(1)	5(1)	17(1)	18(1)	
Store←InEc1!':	5(1)				
TagInEc1!:	5(1)				
Transport':	18(1)				
UseAsrn:	15(1)	18(1)			
UseMcrV:	4(1)	20(1)			
VA.04:	7(2)				
VA.20:	9(2)				
VA.21:	1(1)	9(1)			
VA.22:	9(1)	10(1)			
VA.23:	1(1)	9(1)			
Vacant1:	2(1)	3(1)			
Vacant2:	2(1)	3(1)			
Vacant3:	2(1)	3(1)			
VicIfMiss:	15(1)	17(1)			
VicIfMiss':	2(3)	17(2)	18(1)		
VicInPair:	16(1)	17(1)	21(1)		
VicInPair':	17(2)	20(1)			
VicMem←':	17(1)	21(1)			

VicOrFS1C:	17(1)	18(1)	21(2)
Victim.0!1:	2(1)	15(1)	
Victim.0!2:	4(1)		
Victim.0!3:	13(1)		
Victim.0!4:	1(1)	13(1)	
Victim.0!5:	6(1)		
Victim.0':	4(3)	15(1)	20(1)
Victim.1!1:	2(1)	15(1)	
Victim.1!2:	4(1)		
Victim.1!3:	13(1)		
Victim.1!4:	1(1)	13(1)	
Victim.1!5:	6(1)		
Victim.1':	4(2)	15(1)	20(1)
VictimInA:	2(2)	15(1)	17(2)
VictimInA':	17(1)	18(1)	
WantAltRef':	16(1)	17(1)	
WantCHdly':	16(1)	20(1)	
WantCondHold:	15(4)	16(1)	
WantCR:	16(1)		
WantCR':	15(1)	16(1)	17(1)
WantIfuRef':	16(1)		
WantPrivRef:	16(1)	18(1)	
WantPrivRef':	16(1)	17(1)	
WantProcRef:	15(1)	16(1)	18(1)
WantProcRef'!0:	16(1)		
WantProcRef'!1:	16(1)		
WantProcRef'!2:	16(1)		
WantProcRef'!3:	16(1)	17(1)	18(1)
WantVic:	17(2)		
WantVic':	17(1)	18(1)	
WP1:	2(1)	3(1)	
WP2:	2(1)	3(1)	
WP3:	2(1)	3(1)	
WPinEc1:	2(1)		
WrBrHi'a:	14(3)		
WrBrHi'a%:	21(1)		
WrBrHi'b:	14(3)		
WrBrHi'b%:	21(1)		
WrBrLo'a:	1(2)	14(1)	
WrBrLo'a%:	21(1)		
WrBrLo'b:	14(3)		
WrBrLo'b%:	21(1)		
WrBrLo'c:	14(2)		
WrBrLo'c%:	21(1)		
WrCflags0':	2(1)		
WrCflags0'%:	21(1)		
WrCflags1':	3(1)		
WrCflags1'%:	21(1)		
WrCflags2':	3(1)		
WrCflags2'%:	21(1)		
WrCflags3':	3(1)		
WrCflags3'%:	21(1)		
WrCflagsOK':	2(1)	21(1)	
WrCVA0'a:	1(1)	13(1)	
WrCVA0'a%:	21(1)		
WrCVA0'b:	13(2)		
WrCVA0'b%:	21(1)		
WrCVA1'a:	13(2)		
WrCVA1'a%:	21(1)		
WrCVA1'b:	13(2)		
WrCVA1'b%:	21(1)		
WrCVA2'a:	13(2)		
WrCVA2'a%:	21(1)		
WrCVA2'b:	13(2)		
WrCVA2'b%:	21(1)		
WrCVA3'a:	13(2)		
WrCVA3'a%:	21(1)		
WrCVA3'b:	13(2)		
WrCVA3'b%:	21(1)		
WrPipe02'a:	14(3)		
WrPipe02'a%:	21(1)		
WrPipe02'b:	14(3)		
WrPipe02'b%:	21(1)		
WrPipe02'c:	1(1)	5(1)	
WrPipe02'c%:	21(1)		
WrPipeCol':	5(1)		

WrPipeCol'%:	21(1)			
WrVicMem':	4(1)			
WrVicMem'%:	21(1)			
XWantsPipe:	15(1)			
←Config!:	19(1)			
←FaultInfo!:	19(1)			
←MD:	15(1)	16(1)		
←MDdly':	16(1)			
←MDI:	15(1)	16(1)		
←MDI':	15(1)			
←Pipe0:	19(2)			
←Pipe015':	6(1)	19(1)		
←Pipe2!:	19(1)			
←Pipe3!:	19(1)			
←Pipe4!:	19(1)			
←Pipe5:	6(1)	15(1)	19(1)	21(1)
←PrVACVA:	1(1)	14(2)	16(1)	
←PrVArOW:	1(1)	14(1)	16(1)	20(1)
←VictAd'!1:	1(1)	13(1)		
←VictAd'!2:	16(1)			
←VictAd'!3:	13(1)			