READ ONLY MEMORY

Capacitive Keyboard Encoder

FEATURES

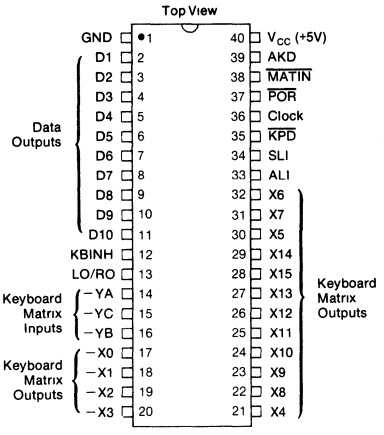
- 128 Key Keyboard Encoder: 112 Fully Decoded Keys, 16 Discrete Function Keys
- 112 Keys With 4 Modes, 10 Bit Output
- Key Validation Logic Protects Against Bounce
- N-Key Roll Over or 2-Key Roll Over
- Internal ROM Allows Any Keys to Control SHIFT CTRL, SHIFT LOCK and ALPHA LOCK
- ALPHA LOCK and SHIFT LOCK Indicator Lines
- Any Key Down (AKD) Strobe
- Single +5 Volt Power Supply
- Programable Coding of Standard and Special Function Keys
- Zener Diode Protection on All I/O Pins
- Low Power Consumption, Less Than 2 MW per Key
- Usable with Capacitive, Magnetic, Inductive, Hall Effect, or Mechanical Keyboard Switches
- Inputs and Outputs TTL and CMOS Compatible
- Internal Oscillator

DESCRIPTION

The General Instrument AY-3-4592 is a unique dual pulse scanning encoder and keyboard controller for 112 keys in four modes and 16 programable discrete function keys. ROM programing permits any keys to control the shift control and lock functions The AY-3-4592 can be used with capacitive, inductive (magnetic) or switch closure type switches since it works on pulse detection.

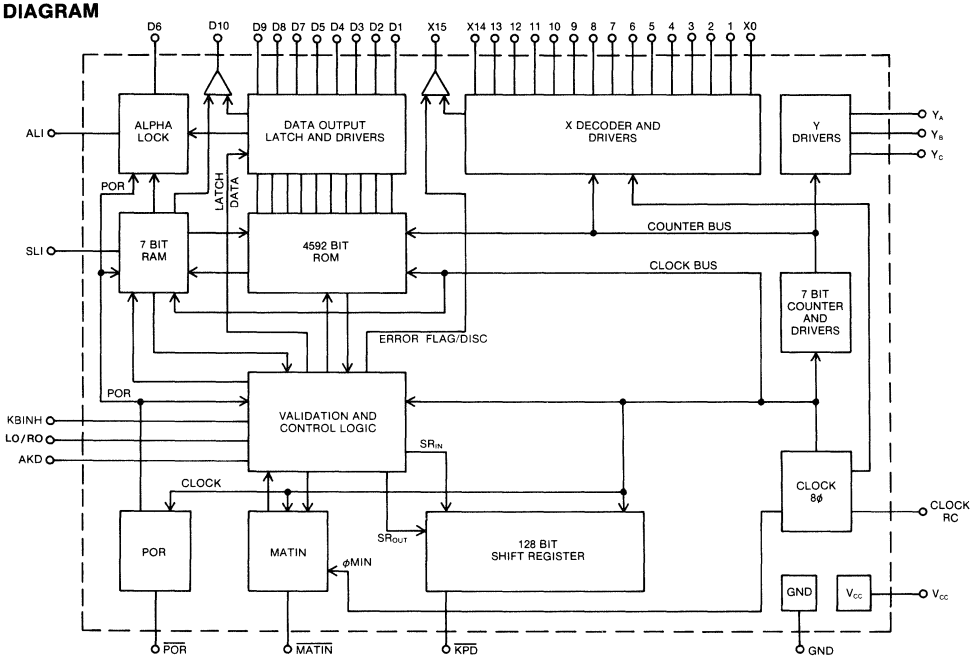
PIN CONFIGURATION

40 LEAD DUAL IN LINE



The AY-3-4592 is fabricated with General Instrument N-Channel MOS technology on a single chip containing a 4592 bit ROM, a 128 bit shift register and an internal oscillator.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	Ground	GND	Ground Pin
2-10	Data Out	D1-D9	Data Outputs, D1 through D9
11	Data Out	D10	Data Output D10. See AY-3-4592 options for complete description
12	Key Inhibit	KBINH	Logic "1" on KBINH will inhibit the processing of Key closures and prevent new output codes. See AY-3-4592 options for other custom options.
13	Lockout/rollover	LO/RO	High for 2 Key Rollover operation, low for N Key Rollover operation. This input is a high impedance Schmitt trigger with thresholds of approximately ¼ (low) and ¾ (high) of V_{CC}. This allows easy interfacing with very slow RC circuits for such functions as "repeat delay". LO/RO is internally "anded" with AKD/STB; if either is low, N Key rollover is automatically selected.
14-16	Y-Address	YA, YB, YC	Y Address lines select one of eight Y inputs through external multiplexer. Scan sequence is Y7 to Y0
17-27, 30-32	X Outputs	X0-X13, X5-X7	X output drivers for Matrix scanning. Scan sequence is X15 to X0. Each driver generates 8 pairs of pulses each scanning cycle.
28, 29	X15, 14	X15, X14	X15 is programed as a "discrete output" key in the standard part. Optionally it may be programed as an error flag or as a Matrix drive line. See AY-3-4592 options. Unlike X0-X13, neither X14 nor X15 have associated ROM output codes. These lines are used to enable separate discrete keys to be debounced using an addressable latch as illustrated in figure 2.
33	Alpha Lock Indicator	ALI	ALI will indicate if op code XX101 is selected. (See operation codes). In the standard device there is no other function. If alpha lock is selected as an option, op code XX101 will result in bit 6 being replaced by bit 9 when a key is depressed.
34	Shift Lock Indicator	SLI	SLI will indicate if op code XX011 is selected (see operation codes). In the standard device this op code will also select the shift lock function.
35	Key Pressed	$\overline{KPD}$	$\overline{KPD}$ is used to shift the threshold of the external sense amplifier in order to provide hysteresis to improve noise immunity. In addition $\overline{KPD}$ may be inverted to provide the data input to the 8 bit latches for decoding X14 and X15. When a key closure is detected $\overline{KPD}$ is generated causing the 8 bit latch output to go high. See figure 2.
36	CLOCK	CLK	Resistor/capacitor tie point for the internal oscillator. Nominal frequencies and scan times are shown below:
37	Reset	$\overline{POR}$	Reset clears all internal registers and flip flops. Suggested circuit for power on reset is illustrated in Figure 1.
38	Matrix Input	$\overline{MATIN}$	Input from external multiplexer. Senses signal from X-Y scan of depressed key.
39	Any Key Down Strobe	AKD	AKD is low when no key is depressed. When a key is depresed AKD goes high. If, while one key is held, a second key is depressed, AKD will go low for 2 clock cycles.
40	Power	V_{CC}	Power supply +5V input

	C = 150pf		C = 220pf		C = 500pf	
R	Freq	Scan time	Freq	Scan time	Freq	Scan time
5K	1 3 MHz	1 5 msec	1 2 MHz	1 7 msec	71 MHz	2 8 msec
10K	8 MHz	2 3 msec	.8 MHz	2 7 msec	45 MHz	4 3 msec
25K	4 MHz	4 8 msec	3 MHz	6 0 msec	20 MHz	10 0 msec

OPERATION

Keys are connected in a 16 x 8 matrix. Scanning of the matrix is performed by the encoder in conjunction with an external, multiplexer. The encoder provides a 3 bit binary address (YA, YB, YC) used to scan each of eight possible sense lines (Y-lines). The drive lines (X-lines) are each pulsed low by the encoder. If a key is closed, the pulse is coupled from the drive to the sense lines, amplified, and sent to the encoder. When used to encode reactive switches, a detection circuit is necessary between the output of the multiplexer and the $\overline{\text{MATIN}}$ input to the encoder. In this manner, each matrix cross-point is interrogated in turn. Each matrix cross-point is given a unique binary code that is determined by the internal scan counters. This code is used to address a ROM which generates the output codes (such as ASCII or other customer defined codes). The output of the ROM is entered into an output holding register when the key is determined to be a valid key closure. Only the cross-points on X0 through X13 can have output codes: X14 and X15 can be used for scanning discrete keys.

An internal oscillator controls the matrix scanning rate. The minimum scanning time is 1.7 ms, at a 1.2 MHz clock. This allows a burst typing speed equivalent to over 250 words/min. When a key is depressed, a matrix address from an X driver and Y input line representing that key is loaded into a 7 bit latch. On the second keyboard scan, the matrix address and the stored address are compared. If the two addresses match, the ROM 10 bit word at that address is loaded into the data holding register. This data remains valid until the next key is depressed. The internal error flag is set, if this option was utilized, whenever there is a mismatch between 7 bit addresses.

Two negative pulses must be detected during the $\overline{\text{MATIN}}$ timing window for the depression to be recognized.

Keyboard Selection

The AY-3-4592 keyboard encoder can be used with a wide variety of available keyboards. An external multiplexing circuit and one external sense amplifier can be tailored to the user's specific requirements. As shown in Figure 1, the sense amplifier detects changes in voltage caused by variations in the switch impedance as a key is depressed and released. Given the key switch impedances for depressed and released states, the values of Rx and Rh can be chosen to guarantee switch closure detection and noise margins. Rx is chosen to match the capacitor or reactor time constants. For example, given a variable capacitance keyboard switch with C1 = 100pf, and C2 = 10pf for depressed and released positions respectively, with a 1.5MHz oscillator and Rx = 10 Kohm, a depressed key would make a 4.7 volt pulse while a raised key would produce a 2.6 volt pulse. The potentiometer would then be set for best noise immunity with minimum pulse width, 90ns for all keys. The hysteresis resistor, Rh, is chosen at roughly ten times the value of Rx to provide increased noise immunity for detected key depressions.

Operation Codes

Depending on the internal programing of the AY-3-4592, keys may have one of three different functions. Keys on matrix line X0 through X13 have, in addition to the output code bits, a function flag bit (FFB). If the FFB is programed as a zero, the key produces a data output when depressed.

When FFB is a one, the key is a "function" key for which bits 1-5 determine the function. These bits are referred to as the op code and are used to provide special functions such as shift, shift lock, alpha lock, etc. Bits 6-10 are not used.

Op codes may be programed to provide data outputs as well as change the mode of operation Data when outputted is not latched as are normal coded outputs.

Bits 1-3 indicate what operation the key will perform; per table 1.

Bit 4 programed as one indicates a down-coded key, for which the 10 data bits programed in the shift mode level of ROM are outputted when the key is depressed.

Bit 5 programed as one indicates an up-coded key for which the 10 data bits programed in the control mode level of ROM are outputted when the key is released.

Neither bit 4 nor 5 will have any effect on the operational control of bits 10-3.

Table 1

Op-Code 5	4	3	2	1	Function
X	X	0	0	0	Function key (with up/down codes)*
X	X	0	0	1	Right Shift Key
X	X	0	1	0	Left Shift Key
X	X	0	1	1	Shift Lock Key or Discrete Key (output SLI)
X	X	1	0	0	Control Key
X	X	1	0	1	Alpha Lock Key or Discrete Key (output ALI)
X	0	1	1	0	Error Reset Key or discrete key (output X15)
X	X	1	1	1	Discrete Key (output D10)

*If the op-code is 00000 the key has no internal function but $\overline{\text{KPD}}$ will go low when it is processed.

OPTIONS

Pin or Function	Option
X15	X15 may be programed as 1) an X-output to provide a second set of 8 discrete lines 2) a discrete output which indicates when a function key with op code XX110 is depressed 3) an Error Flag Indicator (EFI). See Error Flag In the AY-3-4592 STD X15 is a discrete output
Error Flag	When this option is selected, the AY-3-4592 has the capability of detecting multiple key depressions during the same scan cycle. When selected, the error flag may be programed to generate KBINH and or appear at the X15 output. The error flag may be reset by three methods. If the automatic reset is selected/the flag will be reset when the error causing Key is released. Op-code XX110 may be programed on a function key to reset the error flag. If pin 12 is programed for KBINH error flag will be reset by pulsing pin 12 high. The reset will occur on the negative edge of the KBINH signal; the pulse must be at least 16 clock cycles. Error flag causes KBINH and is automatically reset.
Alpha Lock	When programed for Alpha lock, the function key with op-code XX101 will cause the bit 6 output to be replaced by bit 9. Bit 9 is not altered. Alpha lock is normally used to force printing of upper case characters irrespective of the shift function. Op Code XX101 will also cause an output on ALI (pin 33). When Alpha lock is not programed, op code XX101 will result in an output on ALI (pin 33). Op code XX101 may be programed for momentary action, or latched push-on, push-off alternating action. ALI may be programed for normally low or high output. Op code XX101 is momentary action. ALI is normally low. The AY-3-4592 STD is not programed for Alpha lock, although there will be an output on ALI.
Shift Lock	When programed for shift lock, the function key with op-code XX011 will cause normal electronic shift action. Op code XX011 will also cause an output on SLI (pin 34). If shift lock is not programed, op code XX011 will simply cause an output on SLI. SLI may be programed for normally low or high output. The AY-3-4592 STD is programed for shift lock operation with SLI normally low.
KBINH	KBINH, Keyboard Inhibit, may be programed to be caused by Pin 12 high, by the error flag, or both. In addition, function keys with up or down codes may be programed, as a group, to be inhibited by KBINH. This is the KCI Out option. When pin 12 is programed to cause KBINH, a high input on pin 12 will inhibit processing of common keys. If a key is depressed while the KBINH signal is present, output and output strobe will be generated when KBINH is released. The AY-3-4592 STD has KBINH actuated by pin 12 high, and by the error flag. The KCI In option is used, that is, the function key operation is independent of KBINH.
D10	D10, pin 11, may be programed as the output for the memory bit 10 or as a discrete output. As a discrete output, pin 10 is switched from its normal state (programable as high or low) by the function key with op-code XX111. The AY-3-4592 STD is programed for D10 as a discrete key, normally low.
Key Type	Keys may be either normally open or normally closed. The AY-3-4592 STD is designed for normally open keys.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} ..... -0.3 Volts to +7.0 Volts
Maximum voltage with respect to V_{CC} ..... +0.3 Volts
Storage Temperature ..... 65°C to +150°C
Operating Temperature ..... 0 to 70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

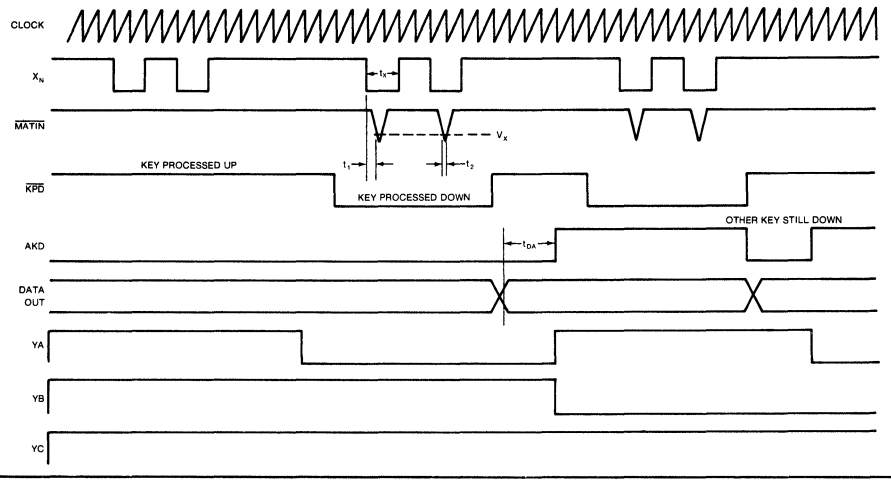
Standard Conditions (unless otherwise noted)

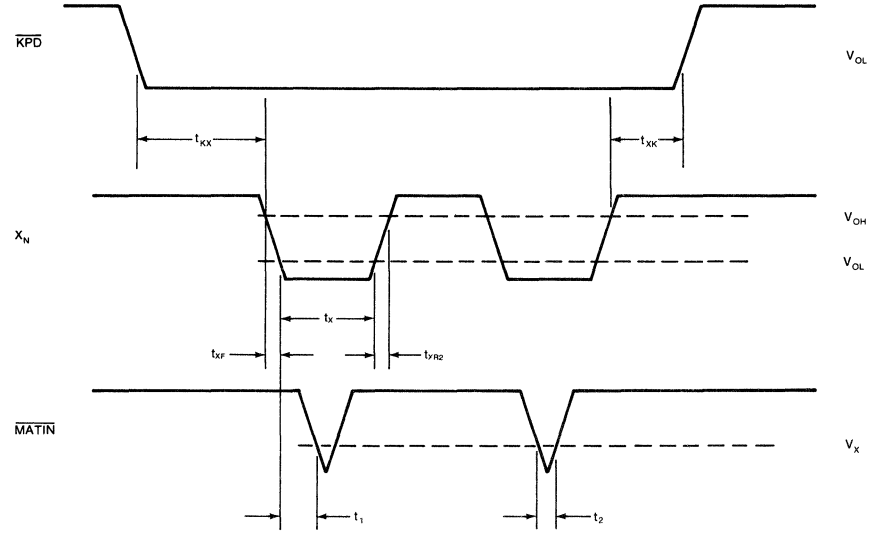
V_{CC} = 5.0V ±5%
T_A = 0° to 70°C

Characteristic	Symbol	Min.	Typ.**	Max.	Unit	Condition
Data Output "1" Voltage	V_{OH}	3.5	-	-	V	I_{OH} = 50μA, 25pf
Data Output "0" Voltage	V_{OL}	-	-	0.5	V	I_{OL} = 1.6mA
All Inputs "1" Voltage	V_{IH}	2.2	-	-	V	except $\overline{POR}$, 2KRO
All Inputs "0" Voltage	V_{IL}	-	-	0.8	V	except $\overline{POR}$, 2KRO
All Inputs Leakage	I_{IH}	-	-	10	μA	V_{in} = 5V
X Output "1" Voltage	X_{OH}	3.5	-	-	V	I_{OH} = 50μA, 100pf
X Output "0" Voltage	X_{OL}	-	-	0.5	V	I_{OL} = 1.6mA
AKd Output Voltage	V_A	-	-	0.6	V	I_{OL} = 3.2mA
$\overline{MATIN}$ Input Voltage	V_X	-	-	0.4	V	
$\overline{POR}$, 2KRO high threshold	V_{SH}	-	1.3	-	V	Schmitt trigger
$\overline{POR}$, 2KRO low threshold	V_{SL}	-	3.7	-	V	Schmitt trigger
Power Supply Current	I_{CC}	-	35	60	mA	Vcc = 5.3V
Clock Frequency	ϕ	200	-	1200	kHz	
Matrix Delay	t_1	-	-	250	ns	
Input pulse width	t_2	90	-	-	ns	
X Output pulse width	t_x	1.7	-	-	μs	
X Output fall time	t_{XF}	-	-	150	ns	V_{OH} = 4.3V, V_{OL} = 0.4V
X Output rise time	t_{XR1}	-	-	150	ns	V_{OH} = 2.4V, V_{OL} = 0.4V
X Output rise time	t_{XR2}	-	-	500	ns	V_{OH} = 3.5V, V_{OL} = 0.4V
X Output rise time	t_{XR3}	-	-	1500	ns	V_{OH} = 4.3V, V_{OL} = 0.4V
$\overline{KPD}$-X Output set time	T_{KX}	500	-	-	ns	
X Output-$\overline{KPD}$ hold time	t_{XK}	100	-	-	ns	
Data out to AKD time	t_{OA}	1.7	-	-	μs	

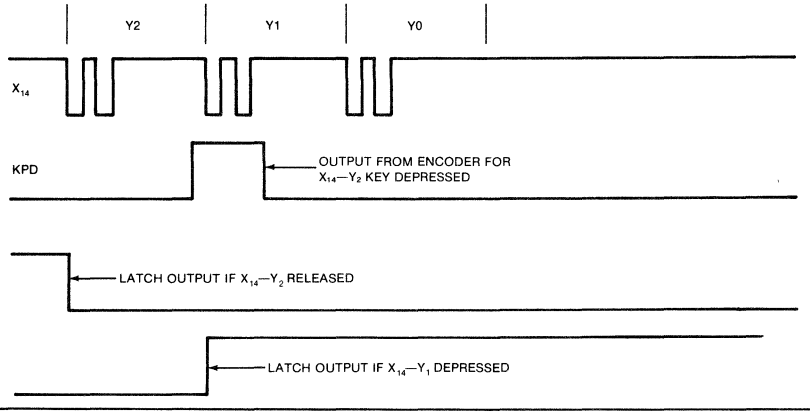
**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS





Discrete Function Key



CODE CHART / AY-3-4592-STD

XXY	F	NORMAL			SHIFT			CONTROL			SHIFT/CONTROL		
	B	HEX	BINARY		HEX	BINARY		HEX	BINARY		HEX	BINARY	
000	1	001	0000000001	Right Shift	3FF	1111111111		3FF	1111111111		3FF	1111111111	
001	1	002	0000000010	Left Shift	3FF	1111111111		3FF	1111111111		3FF	1111111111	
002	1	003	0000000011	Shift Lock	3FF	1111111111		3FF	1111111111		3FF	1111111111	
003	1	004	0000000100	Control	3FF	1111111111		3FF	1111111111		3FF	1111111111	
004	1	005	0000000101	ALI	3FF	1111111111		3FF	1111111111		3FF	1111111111	
005	1	006	0000000110	X15	3FF	1111111111		3FF	1111111111		3FF	1111111111	
006	1	007	0000000111	D10	3FF	1111111111		3FF	1111111111		3FF	1111111111	
007	0	0CE	0011001110	1	0DE	0011011110	!	0CE	0011001110	!	0DE	0011011110	!
010	0	1E4	0111100100	ESC	1E4	0111100100	ESC	1E4	0111100100	ESC	1E4	0111100100	ES
011	0	0CD	0011001101	2	1BF	0110111111	@	0CD	0011001101	2	1FF	0111111111	NUL
012	0	0CD	0011001101	2	0DD	0011011101	"	0CD	0011001101	2	0DD	0011011101	"
013	0	1B8	0110001000	W	1A8	0110101000	W	1E8	0111101000	ETB	1E8	0111101000	ETB
014	0	1BE	0110001110	9	1AE	0110101110	Q	1EE	0111101110	DC1	1EE	0111101110	DC1
015	0	1BC	0110001100	S	1AC	0110101100	S	1EC	0111101100	DC3	1EC	0111101100	DC3
016	0	19E	0110011110	a	1BE	0110111110	A	1FE	0111111110	SOH	1FE	0111111110	SOH
017	0	185	0110000101	Z	1A5	0110100101	Z	1E5	0111100101	SUB	1E5	0111100101	SUB
020	0	17F	0101111111	NUL	17F	0101111111	NUL	17F	0101111111	NUL	17F	0101111111	NUL
021	0	0CB	0011001011	4	0DB	0011011011	$	0CB	0011001011	4	0DB	0011011011	$
022	0	0CC	0011001100	3	0DC	0011011100	#	0CC	0011001100	3	0DC	0011011100	#
023	0	1BD	0110001101	r	1AD	0110101101	R	1ED	0111101101	DC2	1ED	0111101101	DC2
024	0	19A	0110011010	e	1BA	0110111010	E	1FA	0111111010	ENQ	1FA	0111111010	ENQ
025	0	19B	0110011011	d	1BB	0110111011	D	1FB	0111111011	EOT	1FB	0111111011	EOT
026	0	187	0110000111	x	1A7	0110100111	X	1E7	0111100111	ETB	1E7	0111100111	ETB
027	0	19C	0110011100	c	1BC	0110111100	C	1FC	0111111100	ETX	1FC	0111111100	ETX
030	0	17E	0101111110	SOH	17E	0101111110	SOH	17E	0101111110	SOH	17E	0101111110	SOH
031	0	17D	0101111101	STX	17D	0101111101	STX	17D	0101111101	STX	17D	0101111101	STX
032	0	0CA	0011001010	5	0DA	0011011010	%	0CA	0011001010	5	0DA	0011011010	%
033	0	18B	0110001011	t	1A8	0110101011	T	1E8	0111101011	DC4	1E8	0111101011	DC4
034	0	199	0110011001	f	1B9	0110111001	F	1F9	0111111001	ACK	1F9	0111111001	ACK
035	0	198	0110011000	g	1B8	0110111000	G	1F8	0111111000	BEL	1F8	0111111000	BEL
036	0	189	0110001001	v	1A9	0110101001	V	1E9	0111101001	SYN	1E9	0111101001	SYN
037	0	19D	0110011101	b	1BD	0110111101	B	1FD	0111111101	STX	1FD	0111111101	STX
040	0	17C	0101111100	ETX	17C	0101111100	ETX	17C	0101111100	ETX	17C	0101111100	ETX
041	0	0C8	0011001000	7	0D9	0011011001	¿	0C8	0011001000	7	0D9	0011011001	¿
042	0	0C9	0011001001	6	0D9	0011011001	¿	0C9	0011001001	6	0D9	0011011001	¿
043	0	186	0110000110	y	1A6	0110100110	Y	1E6	0111100110	EM	1E6	0111100110	EM
044	0	197	0110010111	h	1B7	0110110111	H	1F7	0111110111	BS	1F7	0111110111	BS
045	0	191	0110010001	n	1B1	0110110001	N	1F1	0111110001	SO	1F1	0111110001	SO
046	0	0C9	0011001001	6	0C3	0011000011	<	0C9	0011001001	6	0C3	0011000011	<
047	0	0DF	0011011111	SP	0DF	0011011111	SP	0DF	0011011111	SP	0DF	0011011111	SP
050	0	17B	0101111011	EOT	17B	0101111011	EOT	17B	0101111011	EOT	17B	0101111011	EOT
051	0	0C7	0011000111	8	0D5	0011010101	*	0C7	0011000111	8	0D5	0011010101	*
052	0	0C8	0011001000	7	0D8	0011011000	'	0C8	0011001000	7	0D8	0011011000	
053	0	18A	0110001010	u	1AA	0110101010	u	1EA	0111101010	NAK	1EA	0111101010	NAK
054	0	195	0110010101	J	1B5	0110110101	J	1F5	0111110101	ENQ	1F5	0111110101	ENQ
055	0	194	0110010100	k	1B4	0110110100	K	1F4	0111110100	VT	1F4	0111110100	VT
056	0	192	0110010010	m	1B2	0110110010	M	1F2	0111110010	CR	1F2	0111110010	CR
057	0	0D3	0011010011	,	0C3	0011000011	<	0D3	0011010011		0C3	0011000011	<
060	0	17A	0101111010	ENQ	17A	0101111010	ENQ	17A	0101111010	ENQ	17A	0101111010	ENQ
061	0	0C6	0011000110	9	0D7	0011010111	(	0C6	0011000110	9	0D7	0011010111	(
062	0	0C7	0011000111	8	0D7	0011010111	(	0C7	0011000111	8	0D7	0011010111	(
063	0	196	0110010110	i	1B6	0110110110	I	1F6	0111110110	HT	1F6	0111110110	HT
064	0	190	0110010000	o	1B0	0110110000	O	1F0	0111110000	SI	1F0	0111110000	SI
065	0	194	0110010100	K	1A4	0110100100	[	1F4	0111110100	VT	1E4	0111100100	ESC
066	0	193	0110010011	l	1B3	0110110011	L	1F3	0111110011	FF	1F3	0111110011	FF
067	0	192	0110010010	m	1A2	0110100010	]	1F2	0111110010	CR	1E2	0111100010	GS
070	0	179	0101111001	ACK	179	0101111001	ACK	179	0101111001	ACK	179	0101111001	ACK
071	0	0CF	0011001111	ø	0D6	0011010110	)	0CF	0011001111	ø	0D6	0011010110	)
072	0	0C6	0011000110	9	0D6	0011010110	)	0C6	0011000110	9	0D6	0011010110	)
073	0	178	0101111000	BEL	178	0101111000	BEL	178	0101111000	BEL	178	0101111000	BEL

CODE CHART / AY-3-4592-STD

XXY	F B	NORMAL HEX	NORMAL BINARY		SHIFT HEX	SHIFT BINARY		CONTROL HEX	CONTROL BINARY		SHIFT/CONTROL HEX	SHIFT/CONTROL BINARY	
074	0	18F	01100011111	P	1AF	01101011111	P	1EF	01111101111	DLE	1EF	01111101111	DLE
075	0	0C4	00110001100	;	0C5	00110001101	·	0C4	00110001100	;	0C5	00110001101	:
076	0	193	01100100011	L	1A3	01101000011	\	1F3	01111100011	FF	1E3	01111000011	FS
077	0	0D1	00110100001	.	0C1	00110000001	>	0D1	00110100001	.	0C1	00110000001	>
080	0	0D2	00110100010	–	1A0	01101000000	–	0D2	00110100010	–	1A0	01101000000	–
081	0	191	01100100001	n	1A1	01101000001	^	1F1	01111100001	SI	1E1	01111000001	RS
082	0	18F	01100011111	P	1BF	01101111111	@	1EF	01111101111	DLE	1FF	01111111111	NUL
083	0	1A4	01101000100	[	1A2	01101000010	]	1E4	01111001000	ESC	1E2	01111000010	GS
084	0	0D8	00110110000	'	0DD	00110111101	"	0D8	00110110000	'	0DD	00110111101	"
085	0	0C4	00110001100	,	0D4	00110101100	+	0C4	00110001100	;	0D4	00110101100	+
086	0	0D0	00110100000	/	0C0	00110000000	?	0D0	00110100000	/	0C0	00110000000	?
087	0	177	01011110111	BS	177	01011110111	BS	177	01011110111	BS	177	01011110111	BS
090	0	0C2	00110000010	=	0D4	00110101100	+	0C2	00110000010	=	0D4	00110101100	+
091	0	0C5	00110001101		0D5	00110101101	*	0C5	00110001101		0D5	00110101101	*
092	0	176	01011110110	HT	176	01011110110	HT	176	01011110110	HT	176	01011110110	HT
093	0	1A3	01101000011	\	0B3	00101000011	'	1E3	01111100011	FS	1E3	01111000011	FS
094	0	175	01011110101	LF	175	01011110101	LF	175	01011110101	LF	175	01011110101	LF
095	0	1A4	01101000100	[	0B4	00101000100	{	1E4	01111001000	ESC	1E4	01111000100	ESC
096	0	1F2	01111100010	CR	1F2	01111100010	CR	1F2	01111100010	CR	1F2	01111100010	CR
097	0	1A2	01101000010	]	0B2	00101000010	}	1E2	01111000010	GS	1E2	01111000010	GS
100	0	080	00100000000	DEL	080	00100000000	DEL	080	00100000000	DEL	080	00100000000	DEL
101	0	174	01011101000	VT	174	01011101000	VT	174	01011101000	VT	174	01011101000	VT
102	0	0D2	00110100010	–	1A0	01101000000	—	1E0	01111000000	US	1E0	01111000000	US
103	0	173	01011100011	FS	173	01011100011	FS	173	01011100011	FS	173	01011100011	FS
104	0	1F5	01111101101	LF	1F5	01111101101	LF	1F5	01111101101	LF	1F5	01111101101	LF
105	0	1BF	01101111111	@	1A3	01101000011	\	1FF	01111111111	NUL	1FF	01111111111	NUL
106	0	1A1	01101000001	^	0B1	00101000001	~	1E1	01111000001	RS	1E1	01111000001	RS
107	0	1A0	01101000000	—	0^2	00110000010	=	1A0	01101000000	—	0C2	00110000010	=
110	0	172	01011100010	CR	172	01011100010	CR	172	01011100010	CR	172	01011100010	CR
111	0	1F6	01111101110	HT	1F6	01111101110	HT	1F6	01111101110	HT	1F6	01111101110	HT
112	0	0D2	00110100010	-	0C2	00110000010	=	0D2	00110100010	–	0C2	00110000010	=
113	0	171	01011100001	SO	171	01011100001	SO	171	01011100001	SO	171	01011100001	SO
114	0	190	01100100000	o	1A0	01101000000	–	1F0	01111100000	SI	1E0	01111000000	US
115	0	1A4	01101000100	[	1A2	01101000010	]	1A4	01101001000	[	1A2	01101000010	]
116	0	1F7	01111101111	BS	1F7	01111101111	BS	1F7	01111101111	BS	1F7	01111101111	BS
117	0	160	01011000000	US	160	01011000000	US	160	01011000000	US	160	01011000000	US
120	0	170	01011100000	SI	170	01011100000	SI	170	01011100000	SI	170	01011100000	SI
121	0	0C8	00110010000	7	0C8	00110010000	7	0C8	00110010000	7	0C8	00110010000	7
122	0	1F4	01111101100	VT	1F4	01111101100	VT	1F4	01111101100	VT	1F4	01111101100	VT
123	0	16F	01011101111	DLE	16F	01011101111	DLE	16F	01011101111	DLE	16F	01011101111	DLE
124	0	0CB	00110010011	4	0CB	00110010011	4	0CB	00110010011	4	0CB	00110010011	4
125	0	0D3	00110100011	,	0D3	00110100011	,	0D8	00110110000	,	0D3	00110100011	,
126	0	0CE	00110011110	1	0CE	00110011110	1	0CE	00110011110	1	0CE	00110011110	1
127	0	0CF	00110011111	ø	0CF	00110011111	ø	0CF	00110011111	ø	0CF	00110011111	0
130	0	16E	01011101110	DC1	16E	01011101110	DC1	16E	01011101110	DC1	16E	01011101110	DC1
131	0	0C6	00110001110	9	0C6	00110001110	9	0C6	00110001110	9	0C6	00110001110	9
132	0	0C7	00110001111	8	0C7	00110001111	8	0C7	00110001111	8	0C7	00110001111	8
133	0	0CA	00110101010	5	0CA	00110101010	5	0CA	00110101010	5	0CA	00110101010	5
134	0	0C9	00110101001	6	0C9	00110101001	6	0C9	00110101001	6	0C9	00110101001	6
135	0	0CD	00110101101	2	0CD	00110101101	2	0CD	00110101101	2	0CD	00110101101	2
136	0	0CC	00110101100	3	0CC	00110101100	3	0CC	00110101100	3	0CC	00110101100	3
137	0	0D1	00110100001		0D1	00110100001		0D1	00110100001		0D1	00110100001	

OPTIONS ARE Error Flag — Programmed
X15 — Discrete output, normally low
KBINH — Set by high on pin 12 or error flag Function keys not inhibited by KBINH
Error Flag — Reset by releasing error-causing key
Shift Lock — Operational SLI normally low
Alpha Lock — Inhibited ALI normally low, set by OP code XX101
D10 — Discrete output, normally low
Key Type — Normally open

NOTE Bit 9 — Programmed to allow alpha lock implementation using external logic
Bit 8 — Programmed low for "mono mode" keys, for which the output is the same in all modes
Bits 1-7 — "Inverted" ASCII data bits

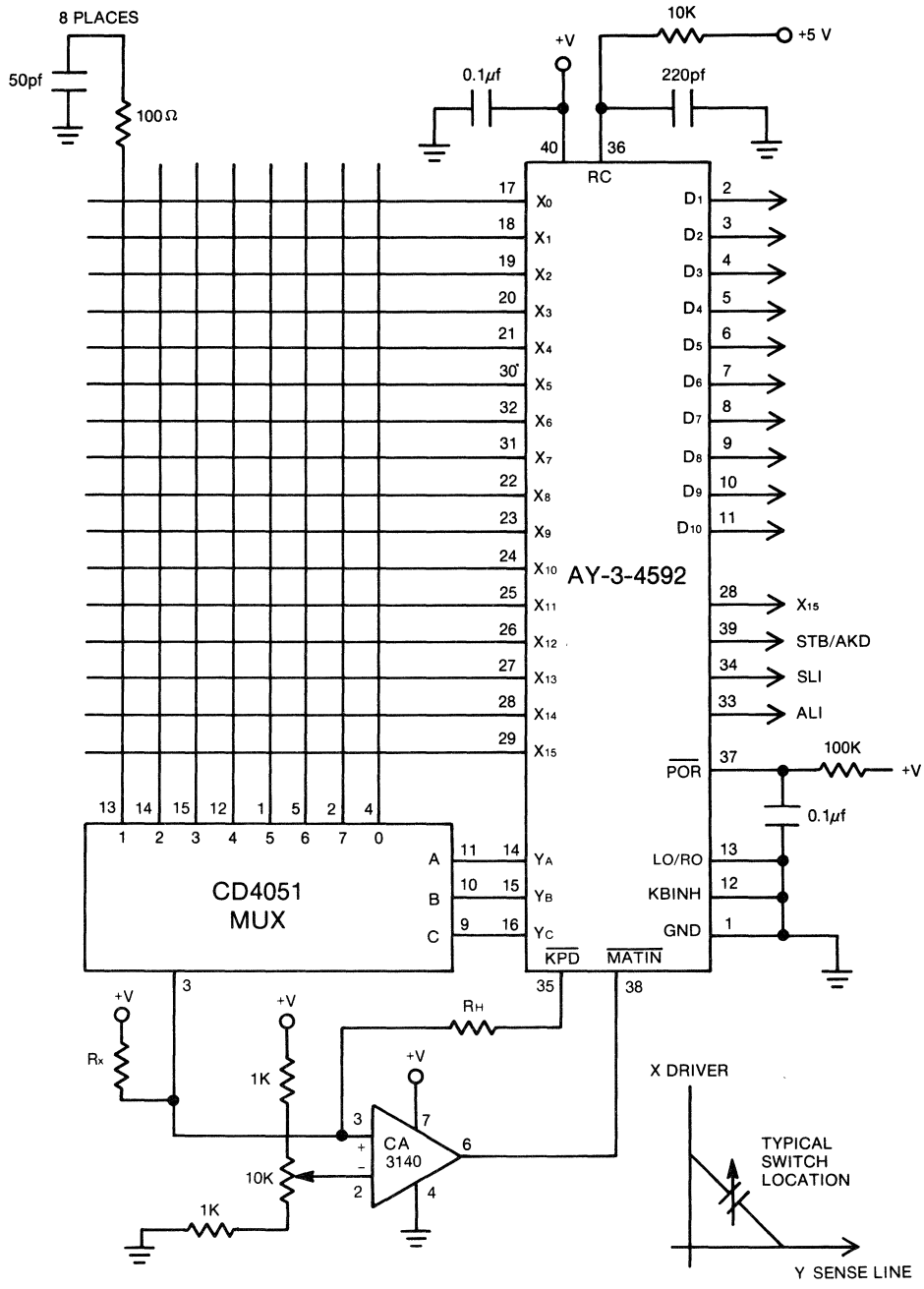


Fig. 1 SAMPLE KEYBOARD DESIGN ROM CODED KEYS

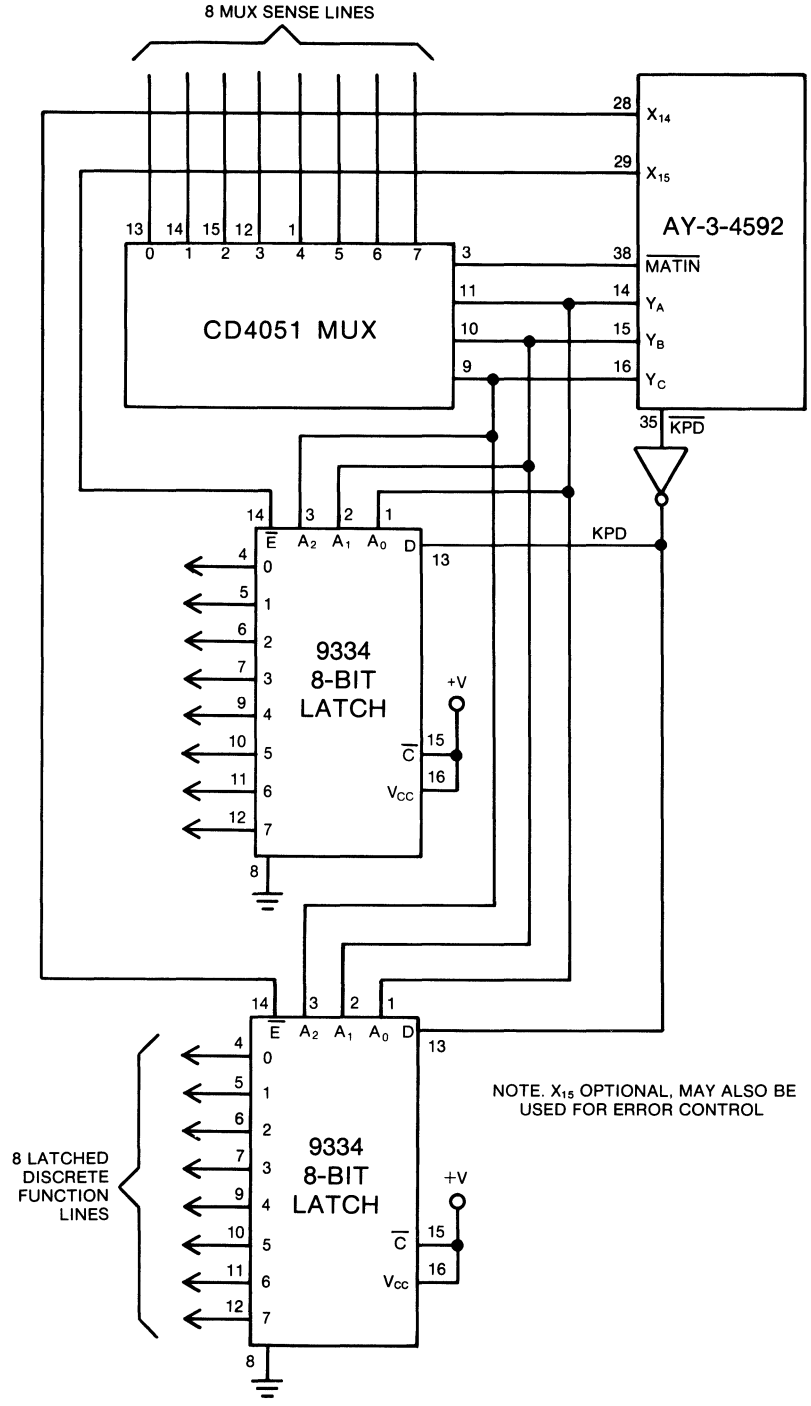


Fig. 2 SAMPLE KEYBOARD DESIGN DISCRETE FUNCTION KEYS