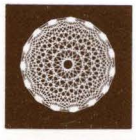
MEGATEK 7000
GRAPHICS DISPLAY SYSTEM
INTERFACE DESCRIPTION

DECEMBER 22, 1977



MEGATEK
CORPORATION
GRAPHIC SYSTEMS

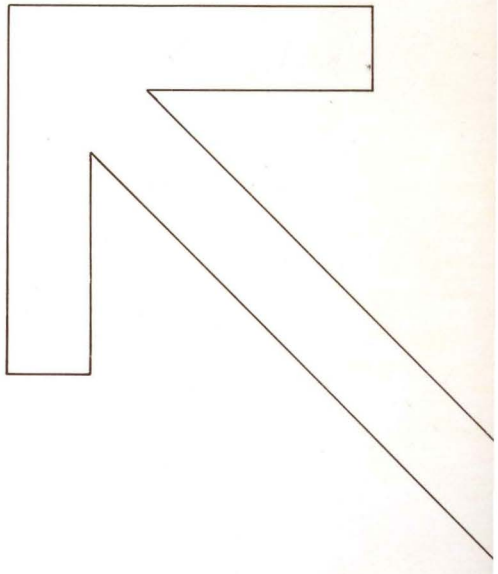


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TABLE OF CONTENTS

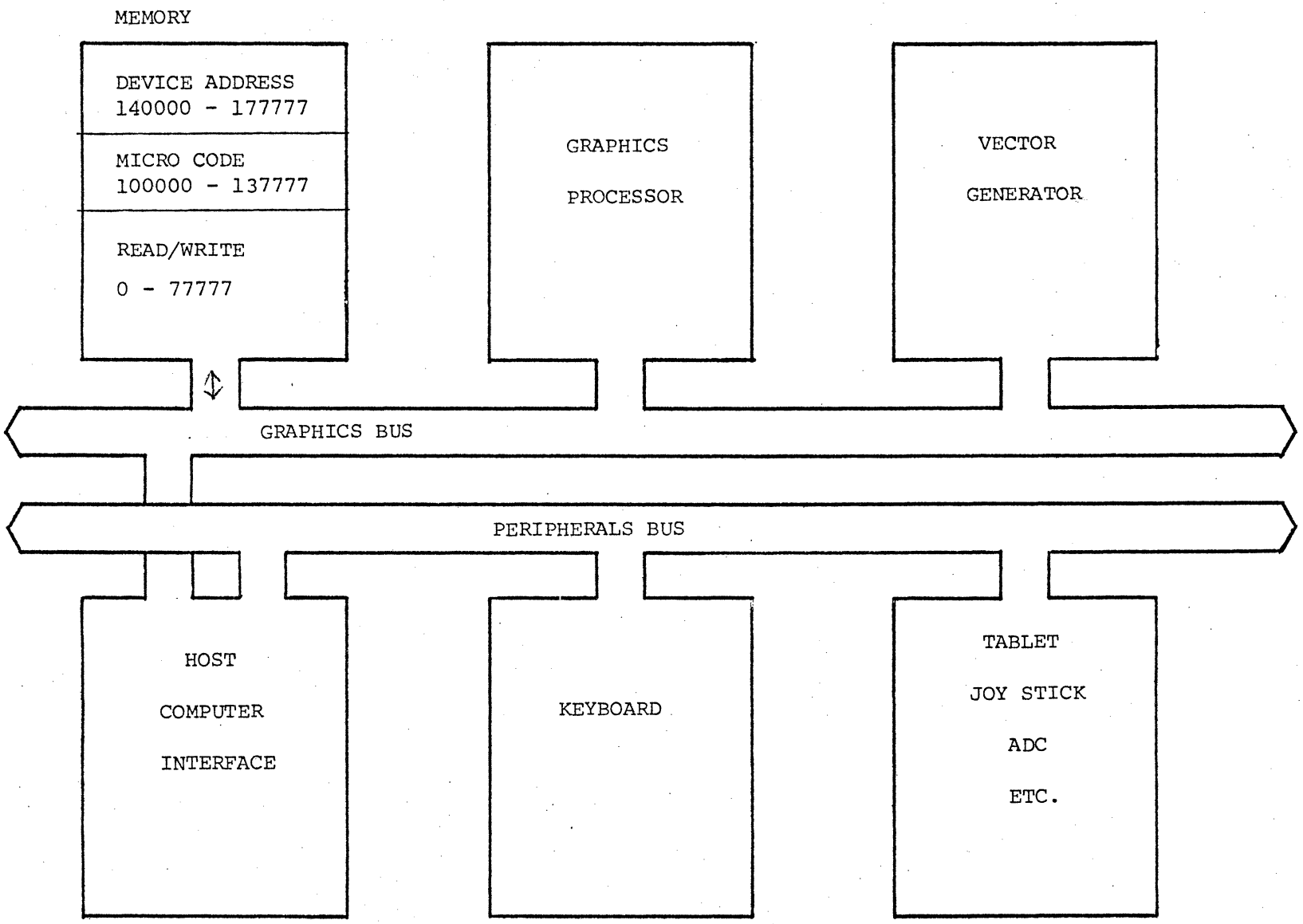
1. INTRODUCTION

The MEGRAPHIC 7000 Graphics Display System is a stand-alone system containing its own refresh memory and graphics display processor. The 7000 is a bus-oriented system and is therefore easily interfaced to a wide variety of host processors should the user desire. This document presents a detailed description of the operation of the bus and requirements for a user-designed bus interface.

Figure 1-1 shows the organization of the MEGRAPHIC 7000 Graphics Display System. The graphics bus ties together the graphics display processor, the vector generator, and memory. Note that the graphics bus is a memory-mapped system and that addresses OCTAL: 140000 through OCTAL: 177777 are reserved for up to four host processor interfaces, up to four graphic display processors, and up to four vector generators.

The peripherals bus ties together the low speed devices in a system. The peripherals bus is addressed by a six-bit address field and does not include provision for a memory.

The data transfer sequence and priority determination sequence of each bus is different due to the widely differing requirements of each bus. In order to assist the user in designing a host computer interface, a detailed description of both the priority determination and data transfer sequences are presented. A pin-signal list is also presented along with a signal glossary.



MEGRAPHIC 7000 SYSTEM ORGANIZATION

FIGURE 1 - 1

2. GRAPHICS BUS

2.1 OVERVIEW

The M7000^{tm} GRAPHIC BUS (GBUS) is a high speed parallel data bus operating in a MASTER-SLAVE style. That is, any device on the bus is allowed to assume the MASTER function and communicate with any other device (SLAVE) on the bus. All devices are functionally similar except the HOST COMPUTER INTERFACE which has additional circuitry to generate GSYNC.

The bus consists of 32 data lines, 16 address lines, and several control signals. The lower 32K addresses are reserved for READ/WRITE memory while the upper 32K are device addresses. Hence, devices on the bus are accessed as if they were memory locations.

2.2 PRIORITY ARBITRATION

All device requests are synchronized with the leading (positive) edge of GSYNC. Those devices requesting access at that time assert $\overline{\text{GREQ}}$ to force GSYNC to remain low after it finishes its following function. During the next 100 nanoseconds, while GSYNC is high, priority is determined via a daisy-chain priority network. All interested parties (those that made requests prior to the rising edge of GSYNC) break the daisy-chain. When GSYNC returns low, the device seeing an unbroken chain is "granted" the bus. This device would be the one "closest" to the host interface (of those requesting service).

When the "granted" device completes its transfer, it simply releases $\overline{\text{GREQ}}$ and reconnects the daisy-chain. If no other device had synchronized a request earlier, GSYNC re-starts. If another device(s) had made a simultaneous request, its continuing assertion of $\overline{\text{GREQ}}$ prevents further GSYNC's. Instead, the next device to see an unbroken daisy-chain is "granted" the bus. This process continues until all those devices which had made requests prior to the last GSYNC are serviced.

This scheme guarantees that even the lowest priority device cannot be blocked out by higher devices for more than one GSYNC period. That is, if every device wanted access at once, the lowest device would be granted the bus before any other device was allowed a second transfer.

See Figure 2-1 for a typical situation where two devices compete for the bus.

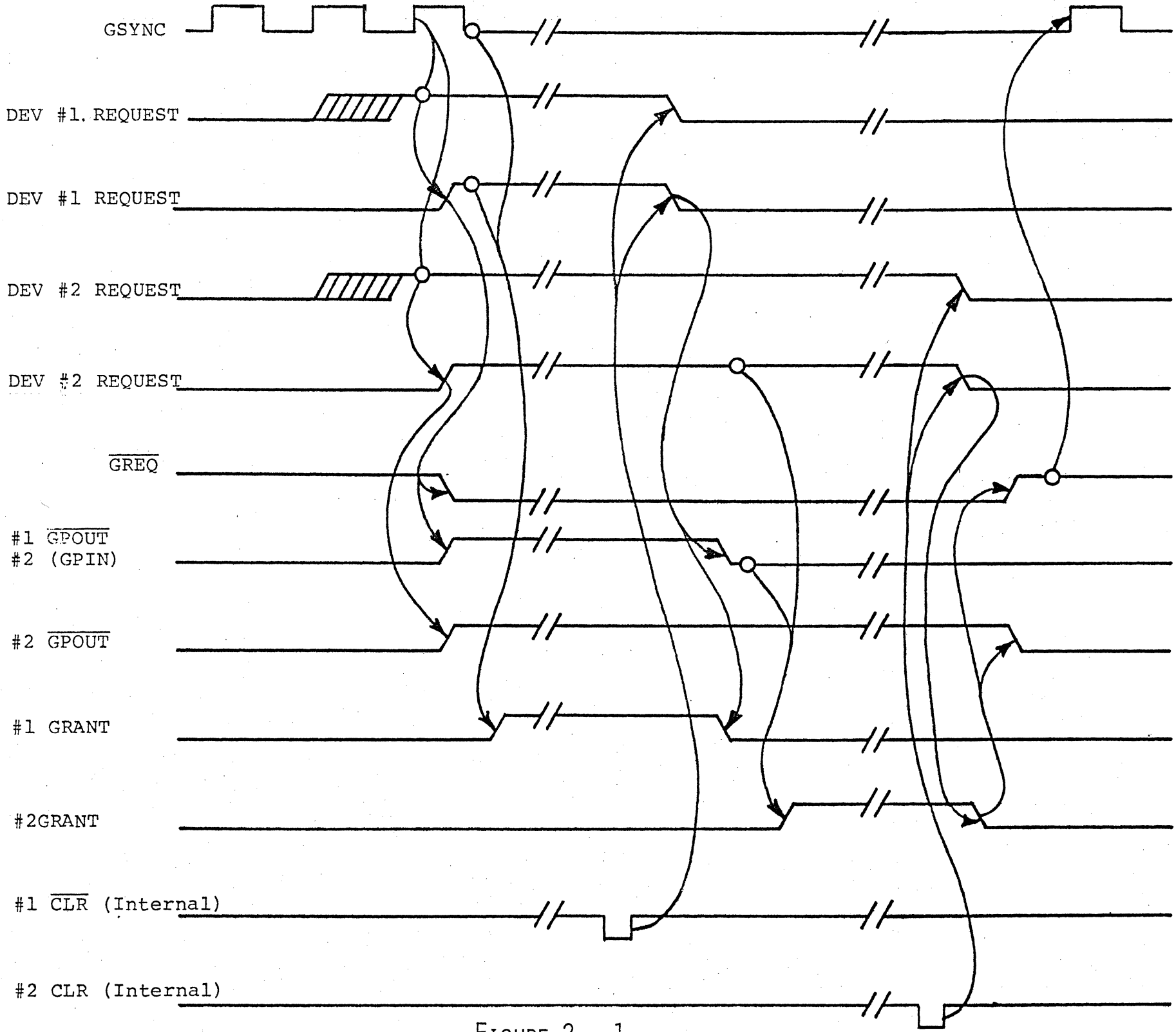

GSYNC
DEV #1. REQUEST
DEV #1 REQUEST
DEV #2 REQUEST
DEV #2 REQUEST
GREQ
#1 GPOUT
#2 (GPIN)
#2 GPOUT
#1 GRANT
#2GRANT
#1 CLR (Internal)
#2 CLR (Internal)

FIGURE 2 - 1

2.3 DATA TRANSFERS

See Figure 2-2 for an idealized bus circuit. Note that the drawing has been simplified for this discussion. See Section 4 for recommended circuits.

The basic timing of a transfer is independent of whether the transfer is a READ or a WRITE. There are several simple differences however, so they will be discussed separately.

2.3.1 READ OPERATION

The transfer is initiated by a device raising its REQUEST signal. The next rising edge of GSYNC sets REQSYNC. REQSYNC forces $\overline{\text{GREQ}}$ active and $\overline{\text{GPOUT}}$ false, thus inhibiting further GSYNCS and disabling lower priority devices. When GSYNC returns low, if $\overline{\text{GPIN}}$ is true, GRANT is raised. GRANT causes the device to assert the SLAVE address onto the bus and after a delay (to allow propagation and setup of the SLAVE address decoder), $\overline{\text{GARDY}}$ is asserted. When the SLAVE recognizes its address and $\overline{\text{GARDY}}$, it will gate its data onto the bus. When this data is valid, the SLAVE asserts $\overline{\text{GDRDY}}$. When the MASTER sees $\overline{\text{GDRDY}}$, it strobes the data into its internal register, and then clears REQSYNC which removes $\overline{\text{GARDY}}$. When the SLAVE sees $\overline{\text{GARDY}}$ lapse, it in turn releases $\overline{\text{GDRDY}}$. The MASTER then removes its bus addresses, releases $\overline{\text{GREQ}}$, and asserts $\overline{\text{GPOUT}}$, completing the transfer.

2.3.2 WRITE OPERATION

All timing follows the READ description with several differences. GRANT causes the MASTER to assert GRD/$\overline{\text{WR}}$ and GDATA0 thru GDATA31 in addition to $\overline{\text{GADDR0}}$ thru GADDR15 (as during READ). When the SLAVE sees $\overline{\text{GARDY}}$, it strobes the data into its internal register. When it has captured the data, it asserts $\overline{\text{GDRDY}}$ (it actually indicates DATA ACCEPTED, not DATA READY). When the MASTER sees $\overline{\text{GDRDY}}$, it clears BUSREQ and the transaction copies a READ cycle.

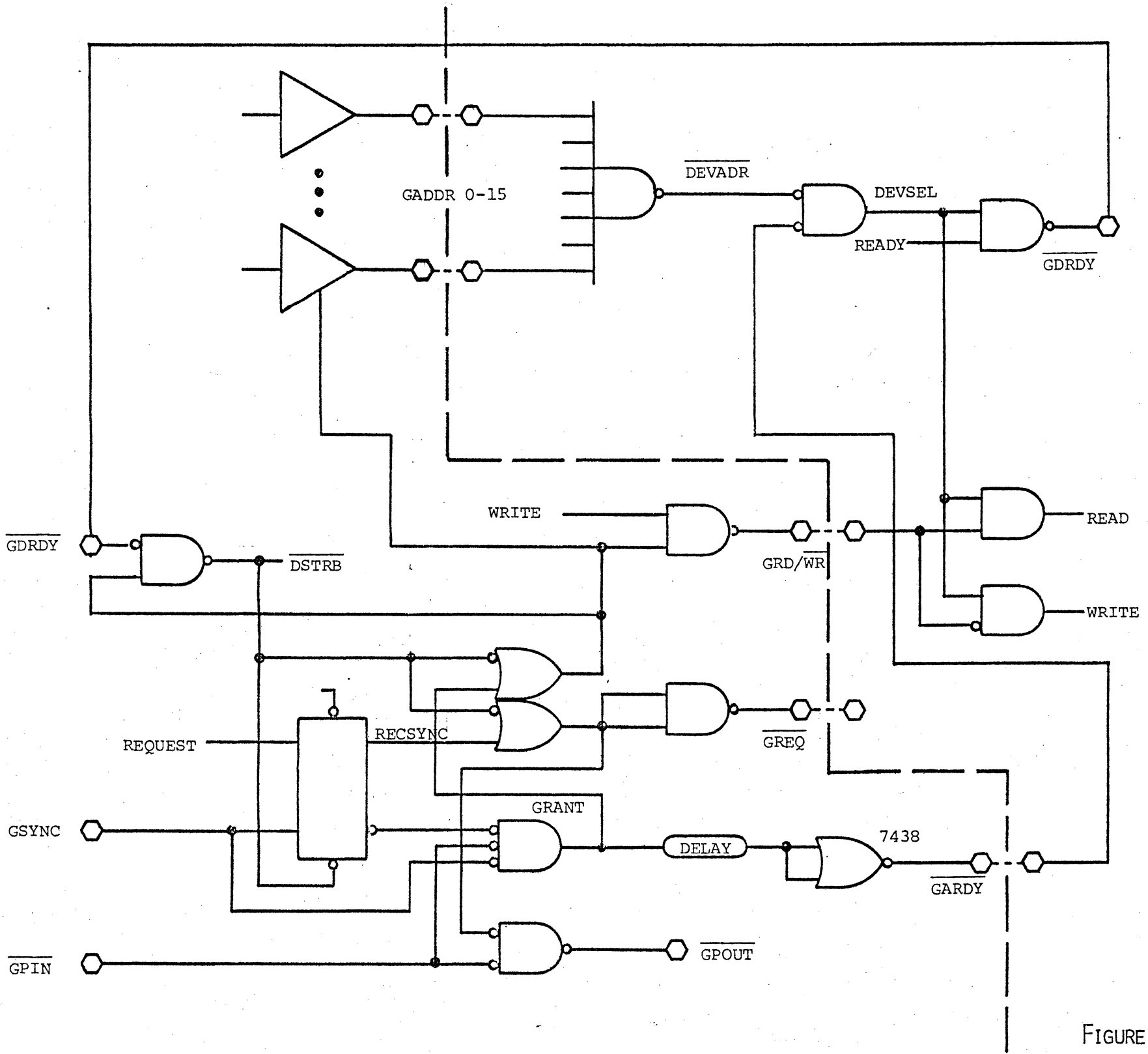

GADDR 0-15
DEVADR
DEVSEL
READY
GDRDY
WRITE
READ
GDRDY
DSTRB
GRD/WR
WRITE
REQUEST
RECSYNC
GREQ
GRANT
GSYNC
DELAY
7438
GARDY
GPIN
GPOUT

FIGURE 2 - 2

3. PERIPHERAL BUS

3.1 OVERVIEW

The PERIPHERAL BUS (PBUS) differs from the GRAPHIC BUS in several significant ways.

1. The PBUS is not MASTER/SLAVE. The HOST INTERFACE circuit controls all bus action.

2. The PBUS is not memory mapped. IE devices are not memory locations, but rather selected by a six bit device select code.

3. The PBUS has an interrupt scheme to allow a device to attract the HOST INTERFACE's attention.

3.2 INTERRUPT AND PRIORITY DETERMINATION

Figure 3-1 shows the timing for the peripherals bus priority determination. When some device on the bus lowers $\overline{\text{PREQ}}$, it is the signal for the bus interface to lower $\overline{\text{PPIN}}$. When $\overline{\text{PPIN}}$ is drawn LOW, the interrupting device of the highest priority will place its device select address on the data bus within 100 ns. The bus interface must then accept the device select address before allowing $\overline{\text{PPIN}}$ to go HIGH.

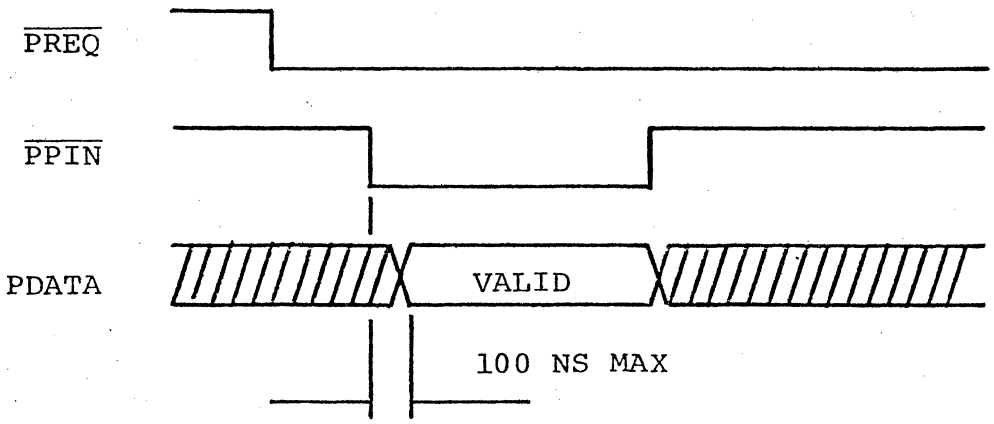
The device select address is placed on the lines $\overline{\text{PDATA10}}$ through $\overline{\text{PDATA15}}$. Bit 0 of the device select appears on $\overline{\text{PDATA10}}$ and bit 5 of the device select appears on $\overline{\text{PDATA15}}$. Both are, of course, in inverted form. In addition, $\overline{\text{PDATA9}}$ informs the processor whether the interrupting device is an input device or an output device. During the $\overline{\text{PPIN}}$ process, $\overline{\text{PDATA0}}$ and $\overline{\text{PDATA1}}$ indicate the status of the device addressed by the PSELx lines.

The line $\overline{\text{PREQ}}$ will return HIGH if both the interrupting device is serviced and no further requests are pending. If additional requests are pending, $\overline{\text{PREQ}}$ will remain LOW until all requests are satisfied.

3.3 PERIPHERAL DATA TRANSFERS

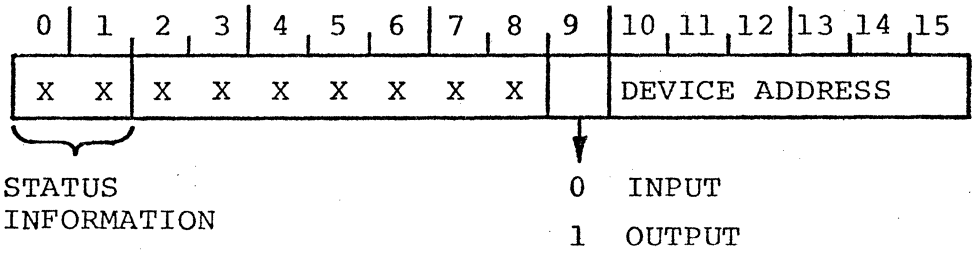
3.3.1 READ SEQUENCE

The timing for a read operation on the peripherals bus is shown in Figure 3-3. Within 100 ns. after the peripheral select lines (PSEL0 through PSEL5) and the PRSTB line have been



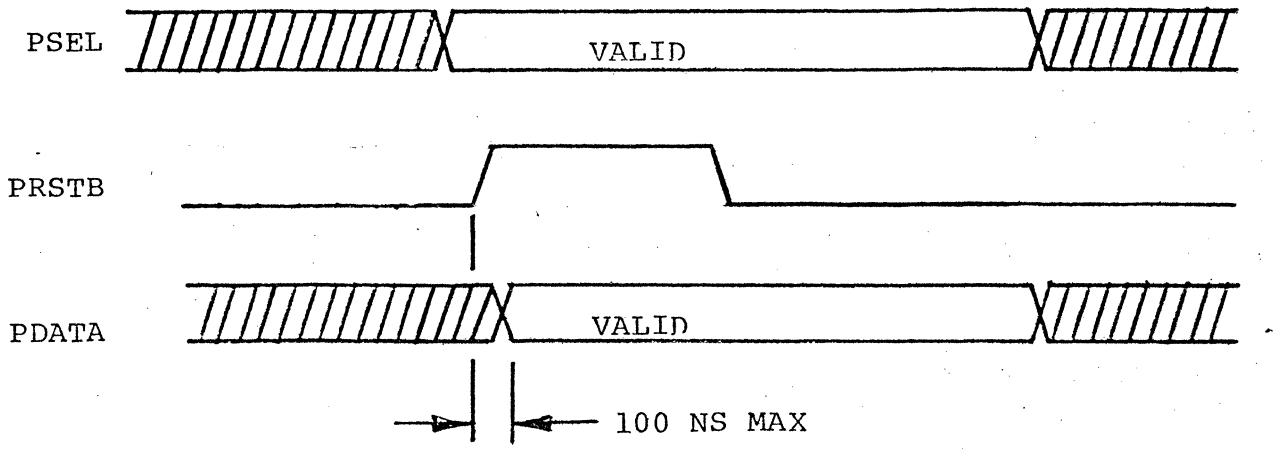
PERIPHERALS BUS PRIORITY TIMING

FIGURE 3 - 1



PERIPHERALS BUS PRIORITY FORMAT

FIGURE 3 - 2



PERIPHERALS BUS READ TIMING

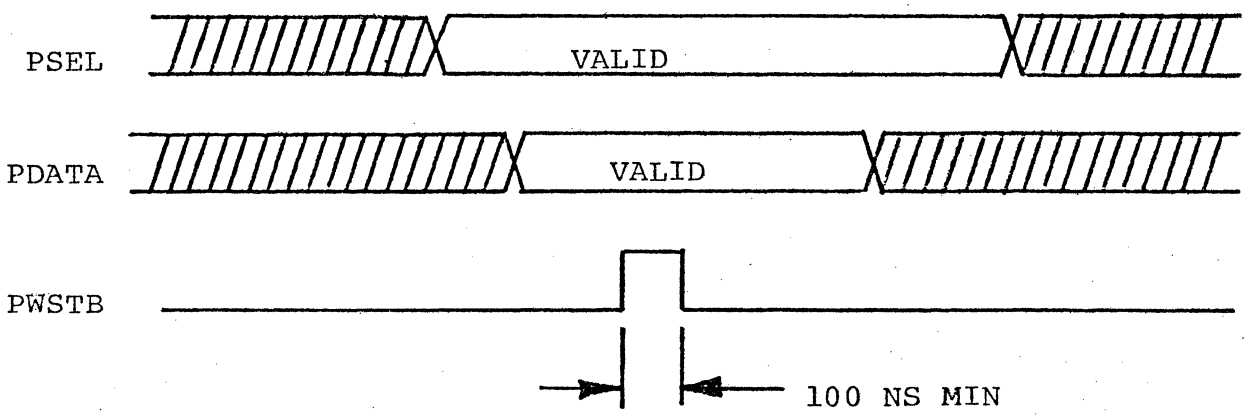
FIGURE 3 - 3

3.3.1 READ SEQUENCE (Cont'd)

set by the bus interface, the peripheral data bus will present data from the selected device. The bus interface must then accept the data before lowering PRSTB and before changing any of the select lines. Note that data is transferred from the bus into the bus interface during a read.

3.3.2 WRITE SEQUENCE

The timing for a write operation on the peripherals bus is shown in Figure 3-4. Operation is similar to a READ except that the bus interface must supply a strobe pulse (PWSTB) in order to cause the peripheral device to accept the data.



PERIPHERALS BUS WRITE TIMING

FIGURE 3 - 4

4. INTERFACE DESIGN

The logical design of a bus interface to the MEGRAPHIC 7000 Graphics Display System should follow the guidelines set forth in Sections 2 and 3. Because of the high speed nature of the bus, certain precautions must be taken in the actual circuit design of bus interfaces.

In order to reduce the possibility of spurious transients interfering with the operation of the bus, line filters should be placed on critical lines. A typical filter is shown in Figure 4-1. Lines to which this type of filter should be applied are presented in Table 4-1.

Table 4-1

Signal Lines Requiring Filters

$\overline{\text{GARDY}}$	PRSTB
$\overline{\text{GDRDY}}$	PWSTB
$\overline{\text{GSNS}}$	PPLS
GYSNC	

The graphics bus data lines (GDATA0 thru GDATA31) and graphics bus address lines (GADDR0 thru GADDR15) are equipped with tri-state drivers. Recommended loading for these lines is one low power Schottky load.

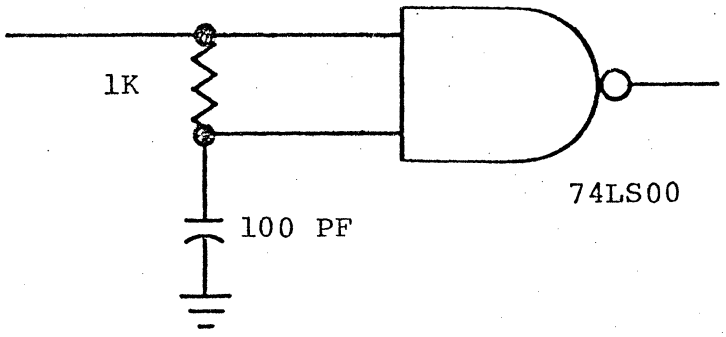
The host computer bus interface should supply all necessary pull-up resistors for open collector outputs. These lines are presented in Table 4-2.

Table 4-2

Signal Lines Requiring 330/390

Pull-Up Resistors

$\overline{\text{PREQ}}$		$\overline{\text{GREQ}}$
$\overline{\text{PDATA0}}$	through	$\overline{\text{GARDY}}$
$\overline{\text{PDATA15}}$		$\overline{\text{GDRDY}}$
		$\overline{\text{GSNS}}$
		GRD/$\overline{\text{WR}}$
		RESET

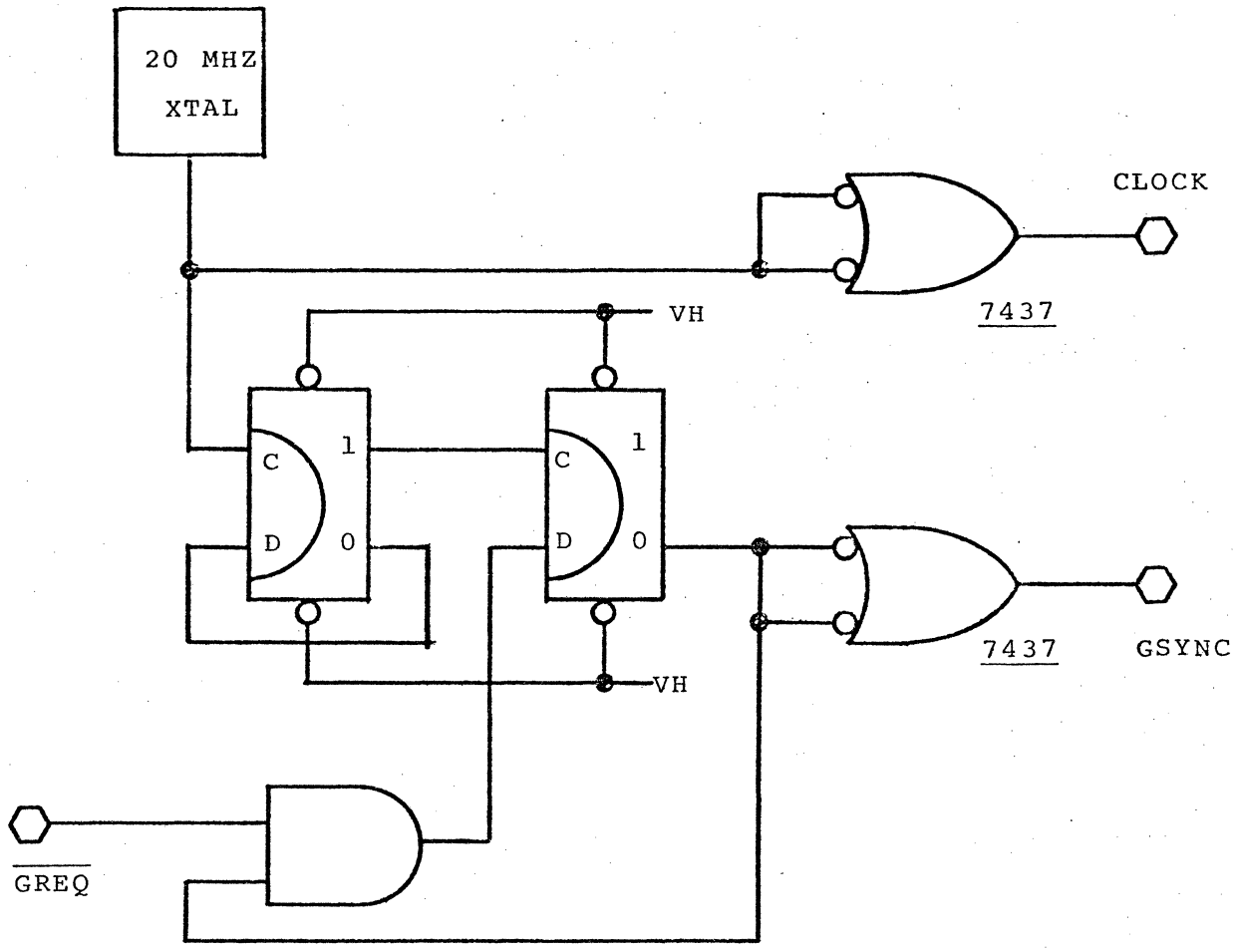


TYPICAL LINE FILTER

FIGURE 4 - 1

4. INTERFACE DESIGN (Cont'd)

The host computer interface must also supply the GSYNC and 20MHz clock signals. A recommended circuit is presented in Figure 4-2. Note that the 20 MHz clock must be crystal controlled in order to insure proper operation of the graphics processor and that high current drivers (7437) are provided for the CLOCK and GSYNC lines.



TYPICAL CLOCK CIRCUIT

FIGURE 4 - 2

APPENDIX A - PIN LIST

(100 Pin Winchester Connector) *Use Filter on Line

PIN	SIGNAL	PIN	SIGNAL
1	GND	50	GADDR 7
2	GND	51	GADDR 8
3	+5	52	GADDR 9
4	+5	53	GADDR 10
5	$\overline{\text{PPOUT}}$	54	GADDR 11
6	$\overline{\text{PPIN}}$	55	GADDR 12
7	$\overline{\text{GPOUT}}$	56	GADDR 13
8	$\overline{\text{GPIN}}$	57	GADDR 14
9	$\overline{\text{PREQ}}$	58	GADDR 15
10	$\overline{\text{GREQ}}$	59	$\overline{\text{GRD/WR}}$
11	GDATA 0	60	*$\overline{\text{GARDY}}$
12	GDATA 1	61	*$\overline{\text{GDRDY}}$
13	GDATA 2	62	*$\overline{\text{GSNS}}$
14	GDATA 3	63	GSYNC
15	GDATA 4	64	60 Hz
16	GDATA 5	65	$\overline{\text{CLOCK}}$ (20 MHZ)
17	GDATA 6	66	*$\overline{\text{RESET}}$
18	GDATA 7	67	*PWSTB
19	GDATA 8	68	*PPLS
20	GDATA 9	69	RESERVED
21	GDATA 10	70	PSEL 0
22	GDATA 11	71	PSEL 1
23	GDATA 12	72	PSEL 2
24	GDATA 13	73	PSEL 3
25	GDATA 14	74	PSEL 4
26	GDATA 15	75	PSEL 5
27	GDATA 16	76	*PRSTB
28	GDATA 17	77	$\overline{\text{PDATA 0}}$
29	GDATA 18	78	$\overline{\text{PDATA 1}}$
30	GDATA 19	79	$\overline{\text{PDATA 2}}$
31	GDATA 20	80	$\overline{\text{PDATA 3}}$
32	GDATA 21	81	$\overline{\text{PDATA 4}}$
33	GDATA 22	82	$\overline{\text{PDATA 5}}$
34	GDATA 23	83	$\overline{\text{PDATA 6}}$
35	GDATA 24	84	$\overline{\text{PDATA 7}}$
36	GDATA 25	85	$\overline{\text{PDATA 8}}$
37	GDATA 26	86	$\overline{\text{PDATA 9}}$
38	GDATA 27	87	$\overline{\text{PDATA 10}}$
39	GDATA 28	88	$\overline{\text{PDATA 11}}$
40	GDATA 29	89	$\overline{\text{PDATA 12}}$
41	GDATA 30	90	$\overline{\text{PDATA 13}}$
42	GDATA 31	91	$\overline{\text{PDATA 14}}$
43	GADDR 0	92	$\overline{\text{PDATA 15}}$
44	GADDR 1	93	-15
45	GADDR 2	94	-15
46	GADDR 3	95	+15
47	GADDR 4	96	+15
48	GADDR 5	97	+5
49	GADDR 6	98	+5
		99	GND
		100	GND

APPENDIX B - GLOSSARY OF SIGNAL TERMS

CLOCK	20 MHz continuous clock signal.
GADDR0 through GADDR15	Graphics bus address lines. These lines are tri-state and switched to the high impedance when the $\overline{\text{GARDY}}$ line is HIGH. These lines present a single low power Schottky load, and data are true when HIGH. Bit 0 is the most significant bit.
$\overline{\text{GARDY}}$	Graphics bus address ready. This line should be driven by an open collector gate. $\overline{\text{GARDY}}$ is driven LOW when the graphics address bus has a valid address presented to it. Line is bidirectional and also should be filtered as described in Section 4.
GDATA0 through GDATA31	Graphics bus data lines. These lines are tri-state and are switched to the high impedance state when the $\overline{\text{GDRDY}}$ line is HIGH. These lines present a single low power Schottky load, and data are true when HIGH. Bit 0 is the most significant bit.
$\overline{\text{GDRDY}}$	Graphics bus data ready. This line should be driven by an open collector gate. $\overline{\text{GDRDY}}$ is driven LOW when the graphics data bus has valid data presented to it. Line is bidirectional and also should be filtered as described in Section 4.
GND	Ground.
$\overline{\text{GPIN}}$	Graphics bus priority in. This signal is used in a daisy-chain fashion to establish priority for bus requests. When $\overline{\text{GPIN}}$ is LOW it indicates that no other devices on the bus of higher priority are requesting the bus.

$\overline{\text{GPOUT}}$	Graphics bus priority out. This signal is used in a daisy-chain fashion to establish priority for bus requests. When $\overline{\text{GPOUT}}$ is driven HIGH by the bus interface, it inhibits all devices of lower priority from requesting the bus.
$\overline{\text{GREQ}}$	Graphics bus request line. This line should be driven by an open collector gate. When $\overline{\text{GREQ}}$ is LOW the bus timing signal GSYNC is inhibited.
GRD/$\overline{\text{WR}}$	Graphics bus read signal. This line should be driven by an open collector gate. GRD/$\overline{\text{WR}}$ is LOW when data are transferred from the bus interface to the bus (WRITE).
$\overline{\text{GSNS}}$	Graphics bus sense signal. This line is held LOW when the vector generator is unable to accept data due to a full input buffer. When such an overflow occurs, $\overline{\text{GSNS}}$ will go LOW and $\overline{\text{GDRDY}}$ will remain HIGH. This line is not normally used by a host computer bus interface.
GSYNC	Graphics bus synchronization signal. This signal is a clocking signal used to synchronize bus requests. When the graphics bus is busy, the GSYNC signal is inhibited and held LOW.
PPLS	Peripherals bus signal. Performs device dependent functions. Line should be filtered as described Section 4.
$\overline{\text{PDATA0}}$ through $\overline{\text{PDATA15}}$	Peripherals bus data lines. These lines are open collector data lines and should be terminated with 230 to 390 ohm resistances. Data are true when LOW and bit 0 is the most significant bit.

PRSTB	Peripherals bus read strobe signal. PRSTB is HIGH when data are to be transferred from the peripheral device to the bus.
$\overline{\text{PPIN}}$	Peripherals bus priority in. This signal is used in a daisy-chain fashion to establish priority for bus requests. When $\overline{\text{PPIN}}$ is LOW, it causes the requesting device to place its device select address on the data bus.
$\overline{\text{PPOUT}}$	Peripherals bus priority out. This signal is used in a daisy-chain fashion to establish priority for bus requests. When $\overline{\text{PPOUT}}$ is driven HIGH by the bus interface, it inhibits all devices of lower priority from requesting the bus.
$\overline{\text{PREQ}}$	Peripherals bus request line. This line should be driven by an open collector gate. When $\overline{\text{PREQ}}$ is LOW, it indicates some device on the peripheral bus is requesting service. Typical response is to lower $\overline{\text{PPIN}}$.
PWSTB	Peripherals bus write strobe signal. This line should be terminated by a line filter as described in Section 4. PWSTB is driven HIGH when the peripherals data bus has valid data presented to it.
PSEL0 through PSEL5	Peripherals bus select lines. These lines select the desired device on the peripheral bus and hence perform a function similar to the address lines on the graphics bus. Data are true when HIGH, and bit 0 is the most significant bit.

APPENDIX C - MEMORY MAPPED IO ADDRESSES
(Graphics Bus Only)

OCTAL

177761	Graphics Processor 0
177762	Graphics Processor 1
177764	Graphics Processor 2
177770	Graphics Processor 3
177600	Vector Generator 0
177601	Vector Generator 1
177602	Vector Generator 2
177603	Vector Generator 3