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32 KB CORE MEMORY (750 ns)
MAINTENANCE MANUAL

Consists of:

Information Specification	29-493A12
Schematic (Electronics)	35-607R05D08
Component Locator (Electronics)	35-607R05E03
Schematic (Stack)	35-475R01D08
Component Locator (Stack)	35-517R02D03
Schematic (Electronics)	35-607M01R06D08
Component Locator (Electronics)	35-607M01R06E03

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Briefly, the changes are as follows:

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35-607M01R06E03 Sheet 1 of 1

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New Title Sheet

Foreword

35-607R05D08 Sheets 1 thru 20

35-607R05E03 Sheet 1 of 1

35-607M01R04D08 Sheets 1 thru 20

35-607M01R04E03 Sheet 1 of 1

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This Instruction Sheet

New Title Page

Foreword

35-607R05D08 Sheets 1 thru 20

35-607R05E03 Sheet 1 of 1

35-607M01R01D08 Sheets 1 thru 20

35-607M01E03 Sheet 1 of 1

FOREWORD

This Manual contains the information necessary to maintain the 1 microsecond, 32KB core memory. Both M00 and M01 versions are covered.

32 KB CORE MEMORY INFORMATION SPECIFICATION

INTRODUCTION

The 32KB Core Memory Module consists of one 15 inch mother board which contains a plug-on core stack of 16K X 17 bits (32K bytes with parity – INTERDATA Part Number 02-409F01) or 16K X 16 bits (32K bytes without parity – INTERDATA Part Number 02-409F02). The Memory Module is pluggable into standard INTERDATA chassis with 0.75 inch center to center spacings. Table 1 provides the part number and cycle times for the 32KB core Memories.

TABLE 1. 32KB CORE MEMORY

PART NUMBER	PRODUCT NUMBER	SPEED	SIZE	CONFIGURATION
32-206F01		0.75 microseconds	32KB	16K X 17*
32-206F02		0.75 microseconds	32KB	16K X 16

*The seventeenth bit is a Parity bit.

SCOPE

This specification describes the operation of the 32KB Core Memory, the inputs necessary to operate the memory, and the resultant outputs provided by the Memory.

Sections on Block Diagram Analysis, Timing Information, Troubleshooting, Maintenance, and Mnemonics are also provided.

MEMORY CONFIGURATION

The Memory is wired in a 3D, 3 wire, coincident current configuration. Figure 1 illustrates the x and y wiring for the 16K X 17 bit core array, arranged in a 128 by 128 line matrix. Each bit has two sense-inhibit windings designated as Sense Inhibit Section A and Sense Inhibit Section B.

PHYSICAL DESCRIPTION

The 32KB Core Memory assembly, part number 32-206, consists of two subassemblies:

1. 35-607-Electronics (Mother Board)
2. 35-517 F01 Core Stack

The mother board (approximately 15 inches by 15 inches) contains all memory drive, timing, and memory bus interface circuits.

The 35-517 Core Stack, which plugs directly into the 35-607 Mother Board, contains the core and diode arrays.

Figure 2 illustrates the physical location, on the mother board, of the major circuit blocks. The 35-607E03 Component Factor shows address and parity strapping in addition to test and adjustment points.

A back panel map is shown on Sheet 2 of Functional Schematic 35-607D08.

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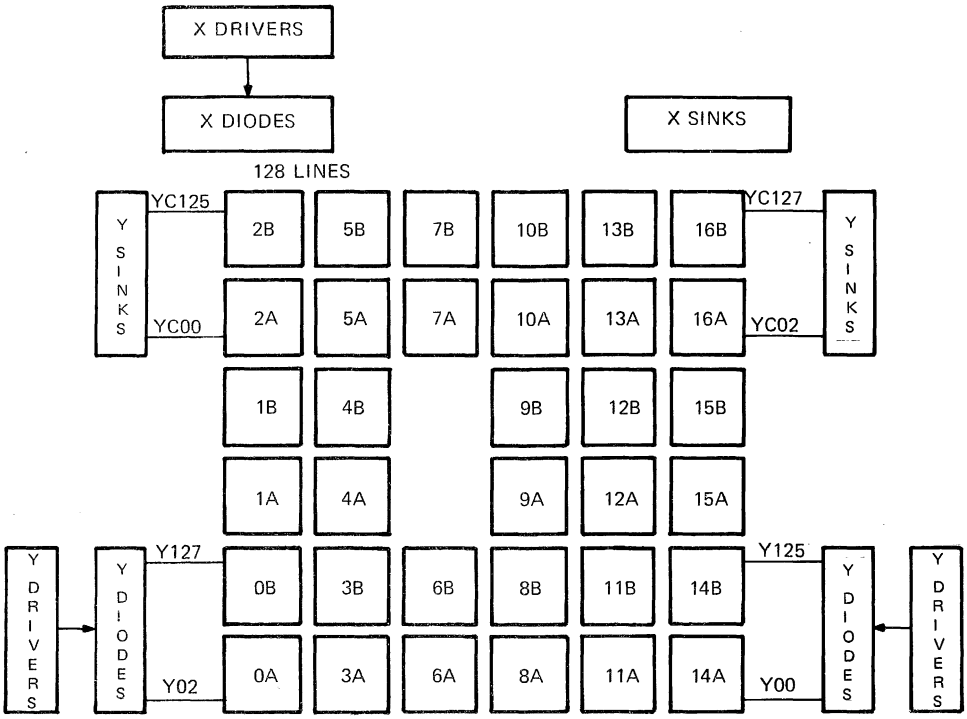

Figure 1. X and Y Core Array

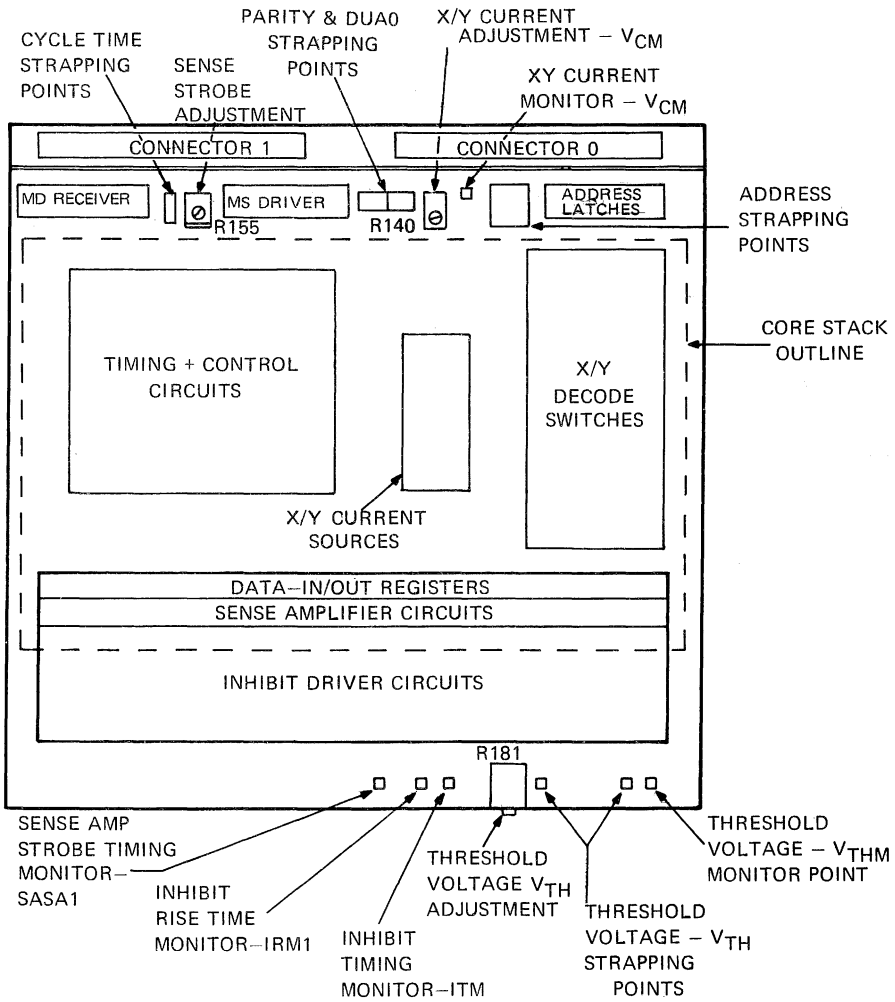

Figure 2. 32KB Core Memory Major Circuit Locations

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BLOCK DIAGRAM ANALYSIS

A block diagram, illustrating the major functions of the Core Memory, is shown on Sheet 1 of Functional Schematic 35-607D08. Descriptions of the individual sections of the memory are given in the following paragraphs.

Interface

System Initialization and Power Up/Power Down

The Power Up, Power Down, or System Initialize conditions are guaranteed by the Memory Shut-Down circuit. This circuit, controlled by the SCLR0 signal, provides complete transitional and long term storage protection.

Memory Access

Access to the Memory Module is obtained through a binary (1 of 8) wired code of the three address bits; XMA150, XMA140, and MA000. Wiring of the code is implemented with on-board wire wrap terminals. Refer to Sheet 11 of the Functional Schematic 35-607D08.

The ER0 latch, when set, enables the initialization of the memory cycle and, with the WRT0 signal, provides Read-Restore or Clear-Write mode control.

A memory cycle starts when one of eight valid address codes enables the low Board Select signal (BS0), and when Shift Register Clock high (SRC1) is generated by the memory start command Early Read (ER0). Refer to Sheet 11 of Functional Schematic 35-607D08.

Timing and Control

The negative going edge of the ER0 signal enables a 25 MHZ delay line oscillator, which in turn advances the shift register. The Timing and Control block contains a 24 stage, two phase shift register time base. All the functional timing pulses associated with internal and interface operations are derived from the Timing and Control Section. Refer to Sheet 11.

The Module Address line MA010 is used to select the sense strobe and inhibit timing pulses for the first and second 8K bit respectively and to control the selection of the first 64 Y lines and the last 64 Y lines respectively.

Word Access (X and Y - Decode and Drivers)

In addition to the Module Address bits MA150, MA140, and MA000, there are 14 additional address lines MA010: 140 which are loaded into the address latches by Memory Busy (internal) (MB0). The latch outputs (A01:14) are decoded by the X and Y axis current steering switches which determine the memory address location to be selected. The latch outputs (A01:14), with the RXDTA/B0 and RYDTA/B0 for Read, and XWDTA/B0 and YWDTA/B0 for Write, determine the polarity of the X and Y currents. One of eight decoders, in turn, drives the X and Y current steering transformer coupled switches. The signals XRT0 and YRT0 for Read, and XWT0 and YWT0 for Write determine the time of the X and Y currents. A total of 3 switches are selected during Read and again during Write to provide a closed circuit through one X and one Y line back to their respective current sources. Refer to Sheet 12.

The functions of the drive line selection lie in a 128(Y) x 128(X) matrix with the first 64 links designated as the A Section and the second group of 64 lines designated as the B Section of each bit. Refer to Sheets 13 through 17.

Sense Section

The Sense Section contains 17 dual sense amplifiers. Each dual amplifier senses one bit. The Sense Strobe signals SASA1 or SASB1, as determined by MA010 to select the appropriate amplifier of each bit. Refer to Sheet 12.

Inhibit

Write control for each bit is provided through two separate inhibit windings; one for each 8K bit section (A or B). Selection of the required Sense Inhibit line is determined by the address MA010. A ZERO is written when the state of the Memory Data Register is Zero during Inhibit timings. Refer to Sheets 2 through 12.

Data Input/Output

The Data Register circuit block provides for temporary storage of Data Input (MD) and Data Output (MS). Refer to Sheets 2 through 10.

The 17 Memory Data (MD) lines, through the internal Data Register, determine whether a ONE or a ZERO is written into each bit.

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Additional Memory Outputs

Three additional output functions provided by the memory are:

1. Memory Busy (MBS0) signal.
2. Parity bit indicator (PAR0).
3. Data Unavailability (DUA0) signal.

MEMORY INTERFACE SIGNALS

Inputs

Signals on the memory interface are TTL levels and considered positive true (e.g., Logical 1 = High>+2.7 Volts and Logical 0 = Low <+0.5 Volts). In addition, the input loading is equal to one TTL input per each signal (low level sink current I_{IL}<2 Milliamperes). All timing is referenced to the ER0 negative going edge at +1.5 Volt levels. Refer to Sheet 18 (32KB Core Memory Timing Diagram).

Early Read Signal (ER0)

The negative going edge of the ER0 signal starts the memory cycle. This time is defined as T_0. The ER0 signal must remain low for a minimum of 50 nanoseconds (T_0+50). This signal is internally latched and therefore has no further effect on the memory operation until the next cycle.

Address Signals

The address signals MAX000:160 and the Extended Memory Address Lines (XMA120:150) must be valid at least 15 nanoseconds prior to ER0 (T_0-15) and remain stable at least 50 nanoseconds after the ER0 negative going edge (T_0 + 50).

To enable access to a particular 64KB Core Memory Module, the module must be coded through the use of wire wrap connections. Refer to Sheet 11.

Write Mode (WRT0)

The Write mode (WRT0) signal defines one of the two operation modes of the memory cycle:

WRT0
Low = Clear-Write mode cycle
High = Read-Restore mode cycle

The WRT0 signal must be valid at T_0 + 150 nanoseconds maximum and remain valid for a period of 100 nanoseconds minimum. Refer to Sheet 11.

Memory Data (MDXX0)

The 17 Memory Data (MD) input lines carry the information to be stored into the memory location determined by the state of address lines MA150:000. The MD Bus must be valid for a Clear-Write cycle from T_0+250 nanoseconds maximum and remain stable for a period of 100 nanoseconds minimum. The high TTL level on the bus indicates that a ZERO is to be stored in the memory location.

System Clear (SCLR0)

The System Clear (SCLR0) line is activated during power-up and power-down periods. The SCLR0 line provides a data retention function as well as a restart of the memory control circuits. Refer to Sheet 17.

Outputs

All output signals are open collector circuits. The fan-out capability is limited to 20 TTL inputs (low level sink current I_{OL}<40 Milliamperes).

Memory Sense (MSXX0)

The 17 Memory Sense (MS) lines carry the information read from the memory location during the Read-Restore mode cycle. The MS Bus is valid at T_0 + 275 nanoseconds maximum and remains valid for a period of 200 nanoseconds ± 50 nanoseconds.

Memory Busy (MBZ0)

A low Memory Busy (MBZ0) line indicates the active state of the memory cycle. Refer to Sheet 11. The MBZ0 signal is valid at T_0 + 50 nanoseconds maximum and remains valid for T_0 + 660 nanoseconds minimum.

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Parity Line (PAR0)

A low Parity (PAR0) line indicates the presence of a parity bit within the addressed 64KB Memory Module. Refer to Sheet 12 for strapping information. The PAR0 signal is valid at T_0+50 nanoseconds maximum and remains valid for T_0+660 nanoseconds minimum.

Data Unavailable (DUA0)

A low Data Unavailable (DUA0) line indicates unavailability of the Read data on the MS Bus. The DUA0 signal is valid for both operation modes at T_0 + 80 nanoseconds maximum and remains valid for T_0 + 350 nanoseconds minimum.

ADDRESS DECODE

Address signals MA010 : 140 provide the X and Y decode and other functions associated with 128 X 128 line matrix as shown in Tables 2 and 3. Refer to Sheet 12 for further information.

TABLE 2. X DRIVE LINE TABLE AND SELECTION SCHEME

32 KB CORE MEMORY X LINE DECODE

XSTA0 - MA030=1
XSTB0 - MA030=0
RXDTB0+WXDTB0 - MA100=0
RXDTA0+WXDTA0 - MA100=1

				MA020	0	0	0	0	1	1	1	1
				MA030	0	0	1	1	0	0	1	1
				MA140	0	1	0	1	0	1	0	1
MA070	MA080	MA090	MA100	XWC / XRA	XS4	XS5	XS0	XS1	XS6	XS7	XS2	XS3
1	1	1	1	15	119	117	126	124	115	113	122	120
1	1	1	0	7	55	53	62	60	51	49	58	56
1	1	0	1	11	87	85	94	92	83	81	90	88
1	1	0	0	3	23	21	30	28	19	17	26	24
1	0	1	1	13	104	106	97	99	108	110	101	103
1	0	1	0	5	40	42	33	35	44	46	37	39
1	0	0	1	9	72	74	65	67	76	78	69	71
1	0	0	1	1	8	10	1	3	12	14	5	7
0	1	1	1	14	118	116	127	125	114	112	123	121
0	1	1	0	6	54	52	63	61	50	48	59	57
0	1	0	1	10	86	84	95	93	82	80	91	89
0	1	0	0	2	22	20	31	29	18	16	27	25
0	0	1	1	12	105	107	96	98	109	111	100	102
0	0	1	0	4	41	43	32	34	45	47	36	38
0	0	0	1	8	73	75	64	66	77	79	68	70
0	0	0	0	0	9	11	0	2	13	15	4	6

TABLE 3. Y DRIVE LINE TABLE AND SELECTION SCHEME

32KB CORE MEMORY Y LINE DECODE

YSTA0 - MA060=1
YSTB0 - MA060=0
RYDTB0+WYDTB0 - MA010=1
RYDTA0+WYDTA0 - MA010=0

				MA040	0	0	0	0	1	1	1	1
				MA050	0	0	1	1	0	0	1	1
				MA060	0	1	0	1	0	1	0	1
MA010	MA110	MA120	MA130	YWA / YRC	YS0	YS4	YS2	YS6	YS1	YS5	YS3	YS7
1	1	1	1	15	126	111	118	103	122	107	114	99
1	1	1	0	11	67	32	75	90	71	86	79	94
1	1	0	1	13	124	109	116	101	120	105	112	97
1	1	0	0	9	65	80	73	88	69	84	77	92
1	0	1	1	14	127	110	119	102	123	106	115	98
1	0	1	0	10	66	83	74	91	70	87	78	95
1	0	0	1	12	125	108	117	100	121	104	113	96
1	0	0	0	8	64	81	72	89	68	85	76	93
0	1	1	1	7	62	47	54	39	58	43	50	35
0	1	1	0	3	3	18	11	26	7	22	15	30
0	1	0	1	5	60	45	52	37	56	41	48	33
0	1	0	0	1	1	16	9	24	5	20	13	28
0	0	1	1	6	63	46	55	38	59	42	51	34
0	0	1	0	2	2	19	10	27	6	23	14	31
0	0	0	1	4	61	44	53	36	57	40	49	32
0	0	0	0	0	0	17	8	25	4	21	12	29

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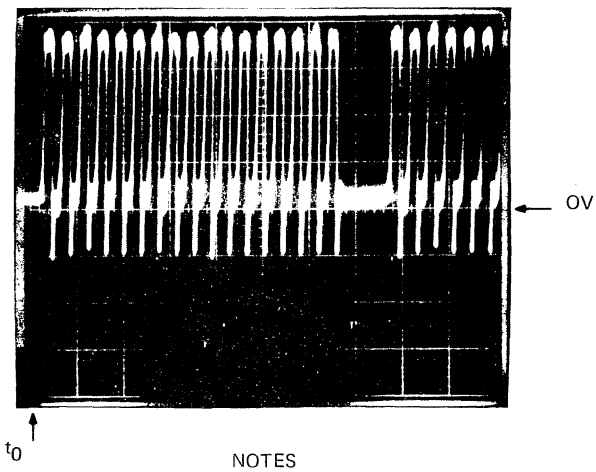
CIRCUIT BLOCK DESCRIPTION

Timing and Control

Memory Timing and Control is derived from a time base comprising a 24 stage two phase shift register (Johnson Counter).

The clock is provided by a delay line oscillator. The frequency of oscillation is set at the factory. Typical wave forms and timing are shown on Figure 3.

The control part of the circuit is associated with address decode and generation of auxiliary functions. Refer to Sheet 11 and 12.



NOTES

1. V = VOLTS
   CM = CENTIMETER
   NS = NANOSECOND

2. ALL TIMING IS REFERENCED TO ERO SIGNAL AND POSITIONED AT THE BEGINNING OF THE TIME SCALE.

Figure 3. SRC1 Location: A89-08

Data Loop

The Data Loop circuit is controlled by a D-type flip-flop which is able to store input (Clear-Write mode) and output (Read-Restore mode) data.

A simplified circuit is shown in Figure 4. The MD Bus receiver contains a tri-state inverter.

In the Clear-Write mode, the register is controlled by the DS1 pulse whose negative going edge enables the TTL level on the tri-state receiver output. The positive going edge of the DS1 pulse transfers the input information into the register. If ZEROs are to be stored, the inhibit source is activated at the write portion of the cycle.

The loop is closed in the Read-Restore mode when the sense amplifier sets the register when reading ONEs and restores such information back in the same memory location at the write portion of the cycle. For further information, refer to Sheets 2 through 10.

X/Y Current Source

The 128 X 128 line matrix is arranged in 16 drives X 8 sinks for the X dimension and 16 drives X 8 sinks for the Y dimension.

The shared drive switch scheme requires the opposite polarities to be activated for a given operation. The X Sink is negative for Read Half Cycle and positive for Write Half Cycle. The Y Sink is positive for Read Half Cycle and negative for Write Half Cycle.

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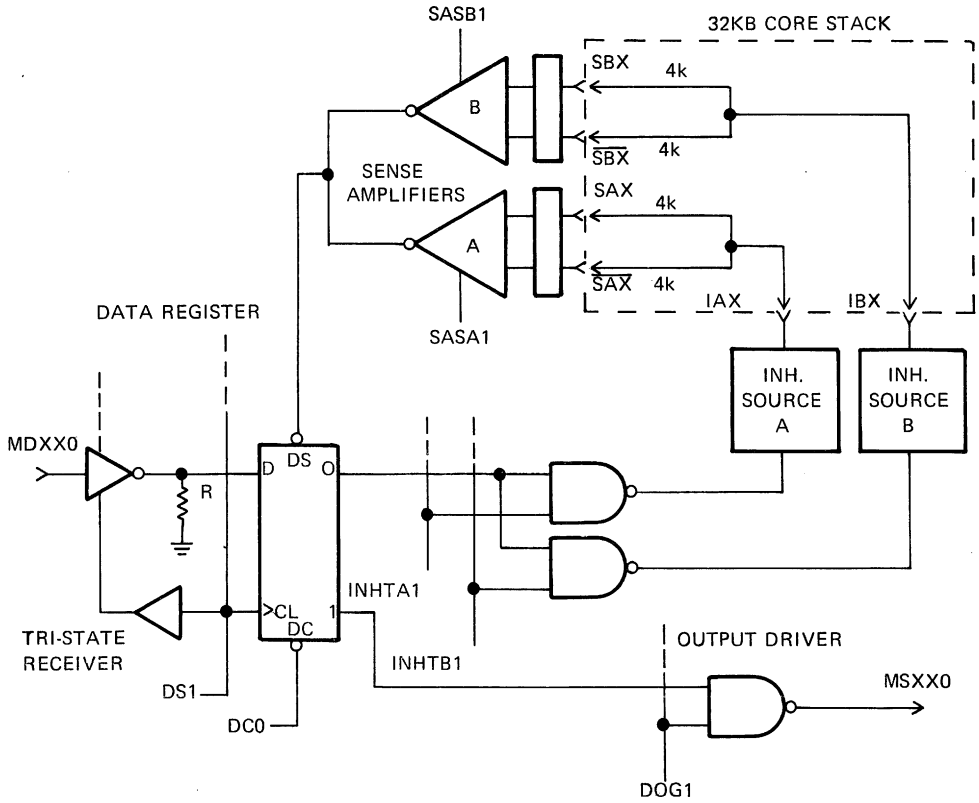

Figure 4. Simplified Data Loop Circuit

TEST POINTS

The Memory Module is equipped with test points to facilitate factory and field adjustments. Table 4 lists the test points with their corresponding location on Functional Schematic 35-607DO8, as well as the appropriate test equipment.

TABLE 4. TEST POINTS

TEST POINT	FUNCTION	LOCATION	TEST EQUIPMENT
SASAI	Sense Amp. Timing Monitor	12N5	>150 MHZ Oscilloscope
IRM1	Inhibit Rise Time Monitor	12N7	>150 MHZ Oscilloscope
ITM1	Inhibit Timing Monitor	12N8	>150 MHZ Oscilloscope
VTHM	Threshold Voltage Monitor	10J3	0-4V,<±1% DVM
VCM	X/Y Current Source Monitor	17K6	0-2V,<±1% DVM

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TESTS AND ADJUSTMENTS

The timing of the Sense Amplifier Strobe (SAS), setting of the sense threshold (V_{TH}), and the X/Y current source bias are adjustable, and are all set to the exact standard at the factory. These settings do not change except with a circuit malfunction. Therefore, readjustment should not be attempted unless the appropriate test equipment listed in Table 4 is available.

A memory suspected of being marginal may be checked by two methods (A and B) whenever they apply:

A. Verifies factory nominal settings.

B. Verifies memory operation margins (while running memory tests or exercises).

A1. Verify that P5, P15, and N15 are within limits, including the temperature tracking, if applicable.

A2. Verify that V_{CM} monitor point reads 1.80 Volts + .020 Volts maximum.

If the reading is out of range, adjust Potentiometer R140 located at the Connector Section of the board until the reading is within the prescribed tolerance.

A3. Verify that the V_{THM} monitor reads 1.900 Volts ± .050 Volts maximum.

If the reading is out of range, adjust Potentiometer R181 located at the edge of the board until the reading is within the prescribed tolerance.

B1. Verify the memory operation margins by varying the sense amplifier threshold voltage (V_{THM}). Monitor Test Point V_{THM} on the front edge of the board and vary Potentiometer R181 over the range of 1.3 to 2.5 Volts. If the memory passes this test, the problem is not in the sense circuit. If memory fails the test, troubleshoot the device circuit. Refer to the Troubleshooting Chart (Table 5) for further information.

A4. Verify that the timing of the Sense Strobe Timing (SASA1) monitor (Read-Restore mode only) is within the specified range as follows:

While running the memory test, monitor the voltage waveform on T48, Pin 16 (XRCS1 + YWCS1) and Sense Strobe Timing test point (SASA1) located at the edge of the board. The leading edge of the Sense Strobe Timing (SAS1) at +1.5 Volts level should be found at 105 nanoseconds ±3 nanoseconds maximum from -8 Volts level on the X Read Voltage Waveform on T48, Pin 16 as shown in Figure 5.

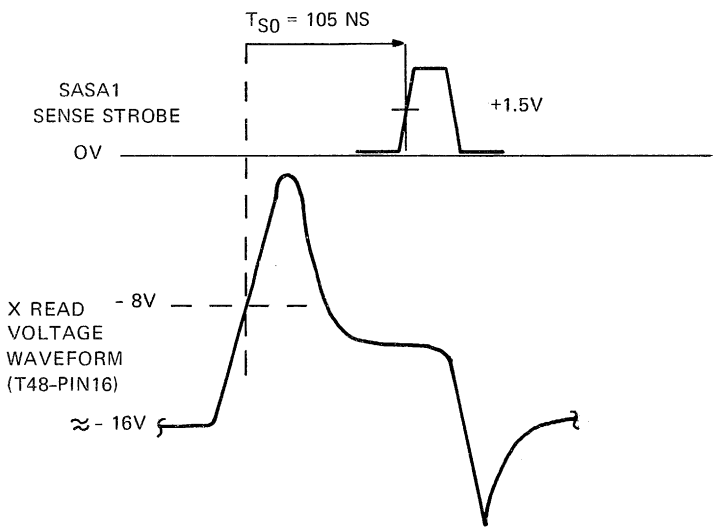

Figure 5. Sense Strobe Timing Reference

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B2. Verify that the memory operates successfully by varying the sense amplifier strobe timing. Monitor as described previously and vary Potentiometer R155 so that strobe timing varies between 99 to 111 nanoseconds without error.

If the memory passes this test, the problem is not of the operational margins character. If the strobe timing interval is found to be out of range, readjustment is possible with the use of the extender board. Adjust Potentiometer R155 accordingly.

NOTES

1. Clockwise adjustments on all potentiometers result in an increase of the adjusted parameter.

2. Under any circumstances, return all the variable parameters to their nominal settings within the maximum tolerances indicated.

TROUBLESHOOTING

CAUTION

UNDER NO CIRCUMSTANCES UNCOVER THE CORE ARRAY. DAMAGE MAY RESULT.

To expose the component side of the electronics board for repairs, the core stack assembly may be separated (unplugged) from the electronics board by removing eight screws from the solder side of the electronics board.

The troubleshooting sequence is contained in Table 5.

TABLE 5. TROUBLESHOOTING CHART

SYMPTOM	POSSIBLE TROUBLE	WHAT TO CHECK
Fails to read or write all bits and all addresses	1. P5, P15, N15 not present	Check P5 on Pins 100-0,-1, 141-0-1 Check P15 on Pins 102-0, 139-1, 239-1 Check N15 on Pins 202-0, 138-1, 238-1
	2. Memory module not selected	Select memory module and determine that A88-Pin 06 (BS0) is low from T_0 +10 to T_0 +60 minimum. If not, refer to Sheet 11 or 32KB Core Memory Maintenance Manual Publication Number 29-493.
	3. Internal clock not running	Check waveform A89-Pin 8 (SRC1) as per Figure 3. If no pulses appear, check that A87 Pin 6 (MB1) is at a logic ONE. If not, determine if ER0 is being generated. Refer to Sheet 11.

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TABLE 5. TROUBLESHOOTING CHART (Continued)

SYMPTOM	POSSIBLE TROUBLE	WHAT TO CHECK
	4. X and Y currents improper	Monitor X or Y Sink Bus Connector B pins and compare the voltage waveforms on Figures 6 and 7. If the current probe is available, monitor the current waveforms on the core stack's test loops. Compare the waveforms to Figures 8 and 9. Check the X and Y bias current source and its monitor point V_{CM} = 1.80 Volts + .020 Volts. Refer to Tests and Adjustments Section. If an individual current pulse appears abnormal, check the appropriate drive and sink address switches. Check that CHT0 Connector C Pins 0:3 are per Figure 10 and refer to Functional Schematic 35-607D08 Sheets 11 and 17.
	5. Improper sense Amplifier operation	Check the sense amplifier outputs available on Pins 10 and 4 of A37-A45 on Sheets 2 through 10. If the waveform is incorrect: 1. Check that the V_{THM} is correct (1.9 Volts ± .050 Volts maximum). 2. Check that the sense strobe timing is within tolerance, refer to Test Point Section for the test and adjustment information. 3. Check the inhibit current presence, comparing the voltage waveforms on Figures 12 and 13. If current probe is available, compare with the current waveform on Figure 14. **NOTE** Inhibit current loop is provided for Bit 16 only.
	6. Data Loop	If sense amplifier output is correct: 1. Check that DOG1 is being generated at A64-Pin 8 (Sheet 11). 2. Check that DS1 is being generated at A64-Pin 6 (Sheet 11).
Fails to read ZEROES on all bits at all addresses	1. Inhibit circuit failing	Check that inhibit timing A61-Pin 6 and A61-Pin 8 (Sheet 12) is per timing diagram on Sheet 18. Check with current probe (if available) the amplitude of the inhibit current for Bit-16 as per Figure 14.
	2. V_{TH} very low	Determine that the V_{THM} is 1.9 Volts +.050 Volts maximum.
	3. Sense strobe out of adjustments	Determine that sense strobe timing is within tolerance, refer to Test and Adjustments Section.

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TABLE 5. TROUBLESHOOTING CHART (Continued)

SYMPTOM	POSSIBLE TROUBLE	WHAT TO CHECK
Fails to read ONES on all bits at some addresses	1. Malfunction of address switches	Check sink and drive voltages on Connector B as per Figures 6, 7, 15 and 16. 1. If individual lines appear abnormal, check the address decoder (A47-A57) outputs associated with that line. 2. If waveform in preceding step is correct, check the transistors and diodes associated with that line. 3. If waveform in preceding step is incorrect, check the input of that decoder. 4. If waveform is incorrect, check address latches associated with the appropriate bit.
	2. Sense strobe malfunction	Check that both Sense Strobe A and B are being generated at A63-Pin 6 and A63-Pin 8 (Sheet 12) when appropriately addressed.
Fails to read ONES on some bits at all addresses	1. Sense Amplifier failure	Check sense amp. output of appropriate bits. If incorrect: 1. Check V_{TH} at T.P. V_{THM} (1.9 Volts ± .050 Volts maximum). 2. Check sense strobe timing as per Test and Adjustment Section. 3. Check that associated inhibit drivers are not turning ON when writing a ONE.
	2. Data loop failure	If correct: 1. Check the associated bit register for proper operation. 2. Check the associated data output buffer for proper operation.
Fails to read ZEROES on some bits at all addresses	1. Inhibit failure	Check appropriate inhibit driver and gates for proper operation when writing zeroes. If correct: 1. Check inhibit waveform as per Figures 12 and 13. 2. Check for shorted diodes in this recovery circuit. If incorrect: Check the associated data bit register output.

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TABLE 5. TROUBLESHOOTING CHART (Continued)

SYMPTOM	POSSIBLE TROUBLE	WHAT TO CHECK
Fails to read ZEROES on all bits at some addresses	1. Inhibit timing failure	Check that INHTA1 and INHTB1 signals are being generated at A61 Pins 6 and 8 when properly addressed. Refer to functional schematic 35-607DO8, Sheet 12. Check the inhibit waveform as per Figures 12 and 13.
Fails to read ZEROES on some bits at some addresses	1. Inhibit driver failure	Check the drive transistor associated with the failing bits when properly addressed.
Memory fails to write data on all bits at all addresses	1. Input WRT0	Check that WRT0 is entering the module at Pin 127-1 on the backplane at the proper time. Refer to Functional Schematic 35-607D08, Sheets 11 and 18. If correct, ensure that CWM1 A77 Pin 9 is a logic ONE in the Clear-Write mode. Ensure that DS1 A64 Pin 6 is being generated in the Clear-Write mode.

NOTES

1. V = VOLTS
   CM = CENTIMETER
   NS = NANOSECOND

2. All timing is referenced to ER0 signal and positioned at the beginning of the time scale.

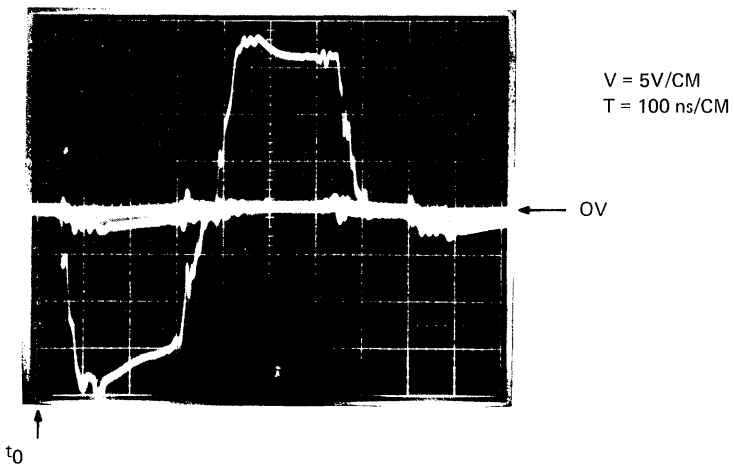

Figure 6. X Sink Voltage Waveform

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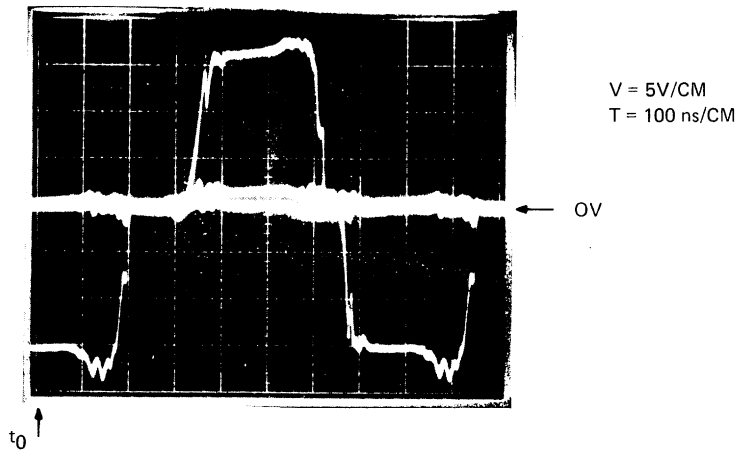

Figure 7. Y Sink Voltage Waveform

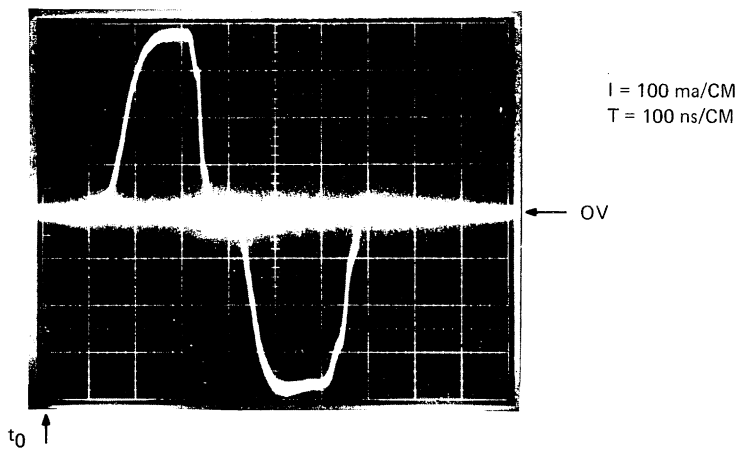

Figure 8. X0 – Line Current Waveform

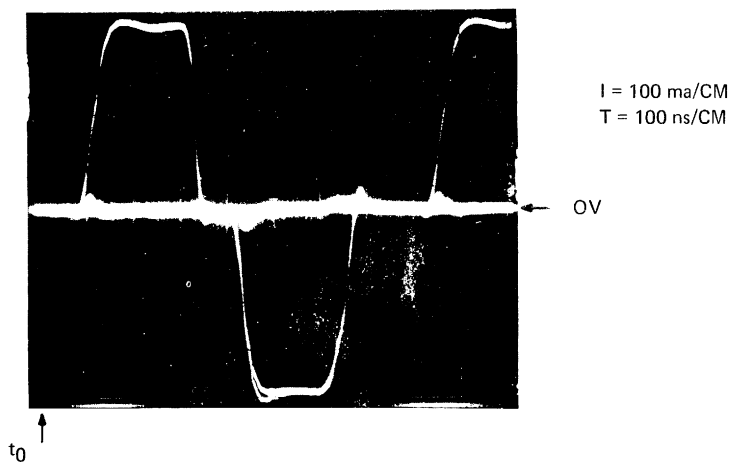

Figure 9. Y0 – Line Current Waveform

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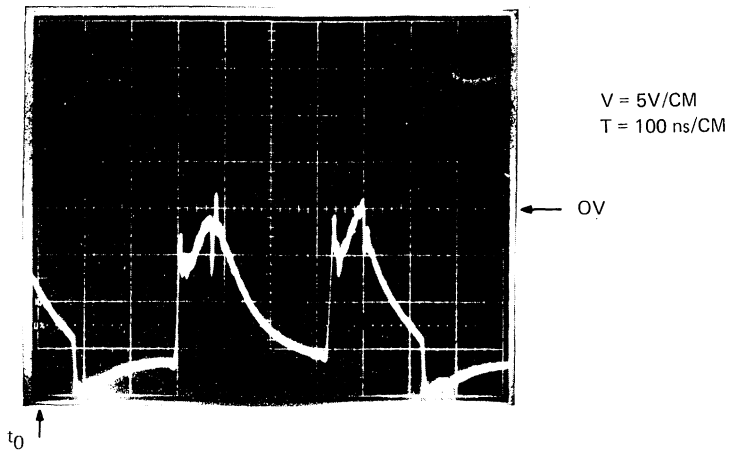

Figure 10. X – Discharge (Anode) Pin 01

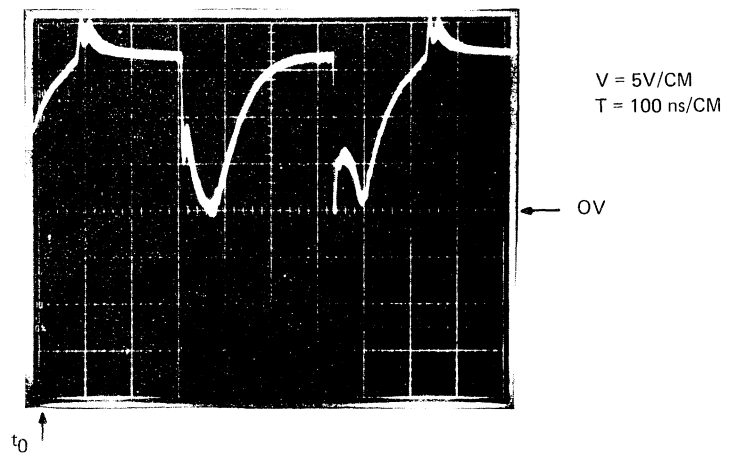

Figure 11. Y – Discharge (Cathode) Pin 02

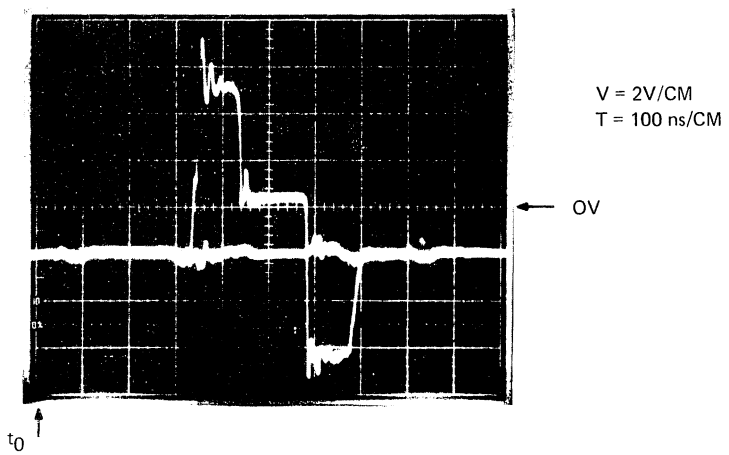

Figure 12. Inhibit Source Voltage Waveform (Pin 118, Conn. A)

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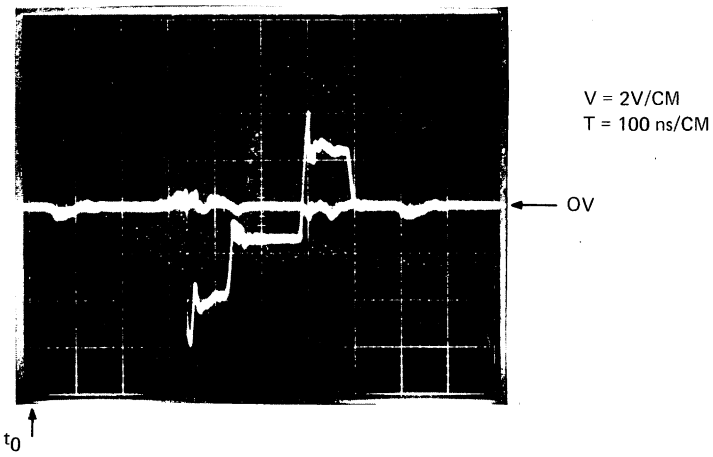

Figure 13. Inhibit Return Voltage Waveform (Pin 117, Conn. A)

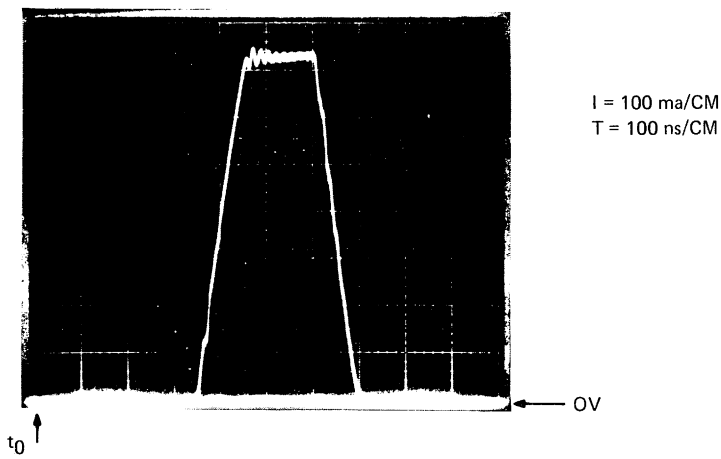

Figure 14. Inhibit Current Waveform

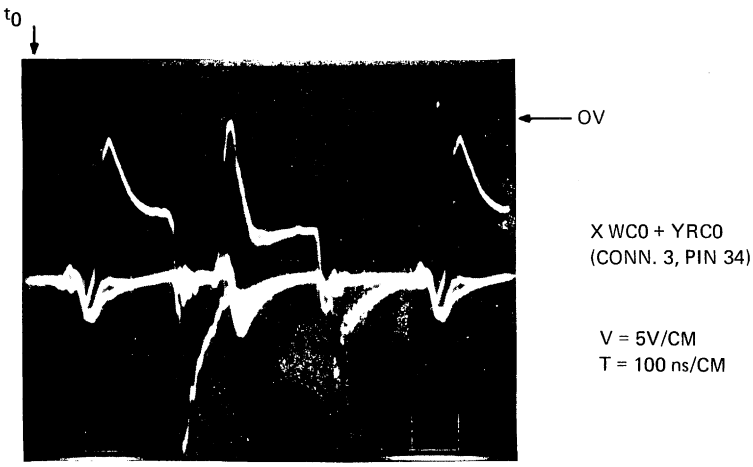

Figure 15. Drive Voltage Waveform

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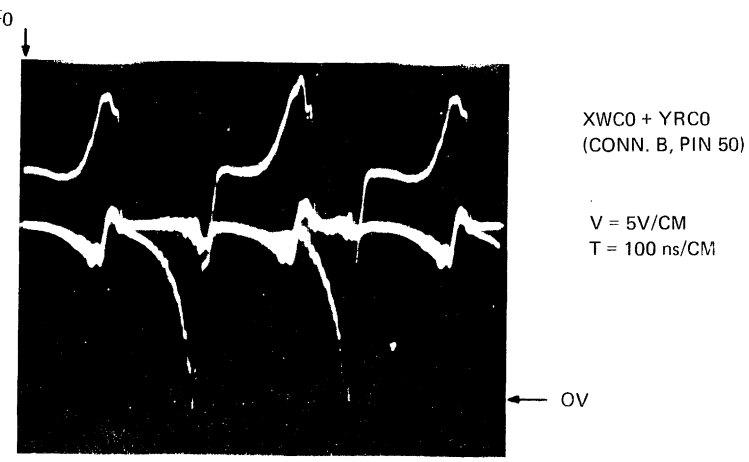

Figure 16. Drive Voltage Waveform

MNEMONICS LIST

The following list provides a brief description of each mnemonic found in the 32K Core Memory. The source and location of each signal on Functional Schematic 35-607DO8 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
A1:14	Latched Address Lines	12D1
BS0	Board Select	11C2
CHT0	Sink Discharge Timing	11C7
CWM1	Clear-Write Mode	11D8
DC0	Data Register-Clear	11R8
DOG1	Data Output Gate	11L8
DS1	Data-In Strobe	llL8
DSA0	Data-In Enable Tri-State	2L8
DSB0	Data-In Enable Tri-State	4L4
DSC0	Data-In Enable Tri-State	5L8
DSD0	Data-In Enable Tri-State	7L3
DSE0	Data-In Enable Tri-State	8L8
DSFO	Data-In Enable Tri-State	9L8
DUA0	Data Unavailable	11K7
ERO	Early Read (Memory Start)	11A3
INHTA1	Inhibit Timing-Section A	12N8

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MNEMONIC	MEANING	SCHEMATIC LOCATION
INHTB1	Inhibit Timing-Section B	12N9
INRT1	Inhibit Rise Timing	12N7
IRM1	Inhibit Rise Monitor	2N7
ITM1	Inhibit Timing Monitor	12N8
MA000:140	Memory Address Lines	11A2 & 12A1
MB0	Memory Busy (internal)	11C2
MB1	Memory Busy (internal)	11C2
MBS0	Memory Busy Bus	11F1
MC0	Master Clear	11N7
MD000:160	Memory Data-In Bus	2K3
MS000:160	Memory Data-Out Bus	2N3
N5A	-5 Volts Source (Bits 0:8)	10R4
N5B	-5 Volts Source (Bits 9:16)	10R5
PARO	Parity Preserve Bus	11F1
READ0	Read-Half Cycle	11F7
RRM1	Read-Restore Mode	11D8
RT0	Read Timing	11D4
RT1	Read Timing	11D4
RXDTA0	X-Read Drive Timing-Section A	12H4
RXDTB0	X-Read Drive Timing-Section B	12H4
SASA1	Sense Amplifier Strobe-Section A	12N5
SASB1	Sense Amplifier Strobe-Section B	12N6
SAT1	Sense Amplifier Timing	12N3
SCC0	System-Clear (internal)	17A1
SCLR0	System-Clear Bus	17A3
+SKV	Positive Sink Voltage	17G1
-SKV	Negative Sink Voltage	17N1
SRC1	Shift Register Clock	11G2
T_1, T_3, T_5 T_{23}	Odd Timing Taps	11G3
T_2, T_4, T_6, T_{24}	Even Timing Taps	11G4
TEMPA	Tracking Thermistor (P/N 15)	10A1
TEMPB	Tracking Thermistor (P/N 15)	10A1
V_{CM}	X/Y Current Bias Monitor	17K7

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MNEMONIC	MEANING	SCHEMATIC LOCATION
V_{TH}	Sense Amplifier Threshold Source	10H4
V_{THM}	Sense Amplifier Threshold Monitor	10J3
WRITE0	Write-Half Cycle	11E8
WRT0	Mode Control Bus	11A8
WT0	Write Timing	11E6
XCHA	X-Sink Discharge Common Anode	17J8
XCHC	X-Sink Discharge Common Cathode	17L7
XRCS1 + YWCS1	X-Read or Y-Write Bus	17 M1
XRA0 + YWA0:15	X-Read or Y-Write Drive	15K2
XRT0	X-Read Current Timing	12K9
XS0:7	X-Sink	14F2
XSTA0	X-Sink Timing-Section A	12H1
XSTBO	X-Sink Timing-Section B	12H2
YCHA	Y-Sink Discharge Common Anode	17L8
YCHC	Y-Sink Discharge Common Cathode	17L7
YRCS0 + XWCS0	Y-Read + X-Write Bus	17E1
YRT0	Y-Read Current Timing	12H9
YS0:7	Y-Sink Bus	13F2
YSTA0	Y-Sink Timing-Section A	12H2
YSTB0	Y-Sink Timing-Section B	12H3

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INTERDATA

BACK PANEL MAP

CONN	CONN. POSITION MOTHER BOARD VERTICAL POS.	32KB MEMORY HORIZONTAL POSITION 1	2
/	41	P5	GND
	40	GND	GND
	39	P15	P15
	38	N15	N15
	37	MD150	MD160
	36	MD130	MD140
	35	MD110	MD120
	34	MD090	MD100
	33	MD070	MD080
	32	MD050	MD060
	31	MD030	MD040
	30	MD010	MD020
	29		MD000
	28	TEMPA	
	27	WRTO	TEMP B
	26		
	25		
	24		
	23		
	22		
	21		
	20		
	19		
	18		
	17		
	16		
	15		
	14		
	13		
	12		
	11		
	10		MS000
	09	MS010	MS020
	08	MS030	MS040
	07	MS050	MS060
	06	MS070	MS080
	05	MS090	MS100
	04	MS110	MS120
	03	MS130	MS140
	02	MS150	MS160
	01	GND	GND
	00	P5	GND
O	41	P5	GND
	40	GND	GND
	39		
	38		
	37		
	36		
	35	DUAO	MB20
	34		
	33	MA130	MA140
	32	MA110	MA120
	31	MA090	MA100
	30	MA070	MA080
	29	MA050	MA060
	28		
	27		
	26	SCLRO	
	25		
	24		
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	22		
	21		
	20		
	19		
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	16		
	15		
	14		
	13		
	12		
	11		
	10	MA030	MA040
	09	MA020	
	08	XMA150	XMA140
	07	MA010	
	06	MA000	
	05	PARO	
	04		ERO
	03		
	02	P15	N15
	01	GND	GND
	00	P5	GND

0	XCHC
1	XCHA
2	YCHC
3	YCHA

CONN C

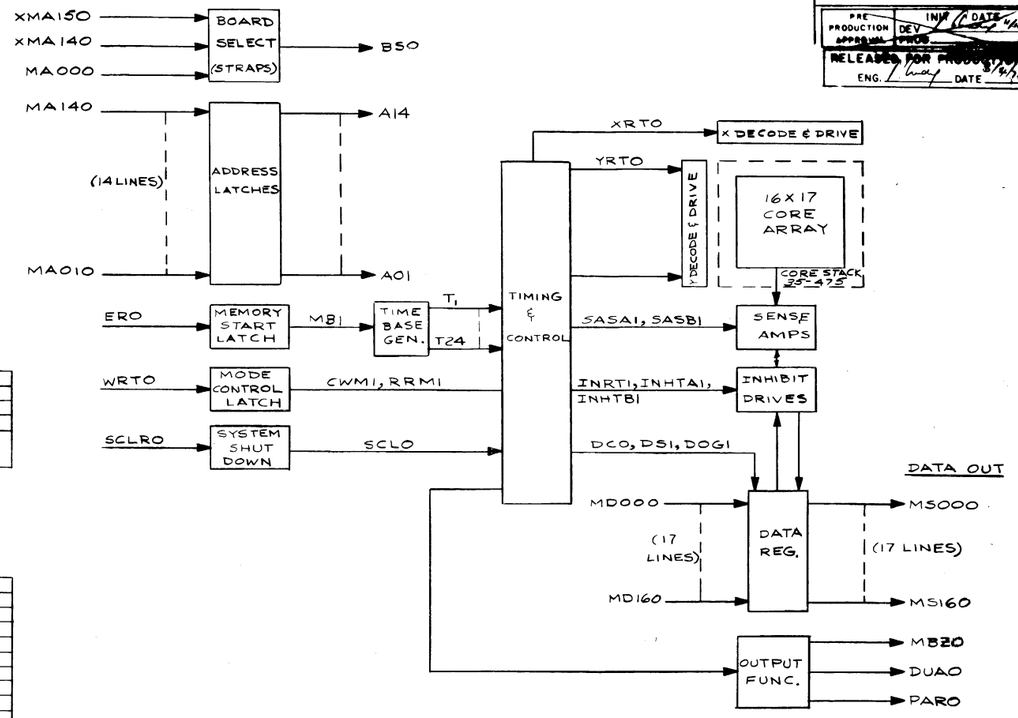
118	IB16
117	SB16
116	SB16
115	GND
114	SA16
113	SA16
112	IA16

13	IB1
12	SB1
11	SB1
10	GND
09	SA1
08	SA1
07	IA1
06	IB0
05	SB0
04	SB0
03	GND
02	SA0
01	SA0
00	IA0

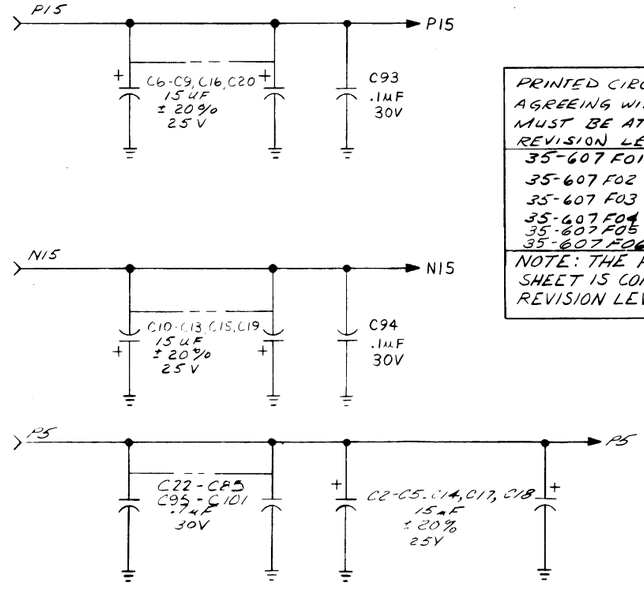
CONN A

00	GND	
01	GND	
02	XS7	
03	XS6	
04	XS5	
05	XS4	
06	XS3	
07	XS2	
08	XS1	
09	XS0	
10	YS7	
11	YS6	
12	YS5	
13	YS4	
14	YS3	
15	YS2	
16	YS1	
17	YS0	
18	N15	
19	XRA14 + YWA14	
20	15	15
21	13	13
22	12	12
23	10	10
24	11	11
25	9	9
26	8	8
27	6	6
28	7	7
29	5	5
30	4	4
31	2	2
32	3	3
33	1	1
34	XRA0 + YWA0	
35	XWC14 + YRC14	
36	15	15
37	13	13
38	12	12
39	10	10
40	11	11
41	9	9
42	8	8
43	6	6
44	7	7
45	5	5
46	4	4
47	2	2
48	3	3
49	1	1
50	XWC0 + YRC0	
51	P15	

CONN B



32 KB CORE MEMORY BLOCK DIAGRAM



PRINTED CIRCUIT BOARD ASSEMBLIES AGREEING WITH THIS SCHEMATIC, MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-607 F01 R05	.75 μSEC W/AAR
35-607 F02 R05	.75 μSEC W/O PAR
35-607 F03 R05	1.0 μSEC W/AAR
35-607 F04 R05	1.0 μSEC W/O PAR
35-607 F05	1.0 μSEC W/PAR R.M.W
35-607 F06	1.0 μSEC W/O PA R.M.W

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

REVISIONS

PRE PRODUCTION	DEV	INIT	DATE
RELEASED FOR PRODUCTION ENG.			DATE

REVISIONS

REVISED SHTS 17 & 20			
WS	2801	- 5-19-76	R01
SHT 1 ADDED C95-C101 TO P5. REVISED SHTS 19 & 20.			
JC	2936	- 7-30-76	R02
REVISED SHTS 1, 18 & 20 35-607 F01-4 REV LEVELS WERE R03. ADDED F05 & F06 VARIATIONS			
WS	2937	- 9/16/76	R03

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REVISIONS (CONT'D)

SUPERCEDED PER ECN #3066

WS	3066	- 8-13-77	R04

REVISED SHTS 1, 4

WS	3092	- 8-16-77	R05

SHEET INDEX	REV	5								2						1	1	1	3
	SHT. NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

NOTES

NAME	TITLE	DATE
B. GRAY	DRAFT	9-12-74
H. MATTER	CHK	1-19-76
P. OBROA	ENGR	1-19-76
[illegible]	TEST	1-19-76
[illegible]	DIR ENG	1-19-76

TITLE SCHEMATIC ELECTRONICS BOARD (32KB MEMORY)

TASK NO. 03141 SIZE 35-607 SCALE NONE SHEET 1 OF 20

BRUNING 44-231 16042

REVISIONS

BIT 16

BIT 15

A20 * 19-099 SENSE AMP

A21 19-099 SENSE AMP

* - WITHOUT PARITY (F02 & F04 VARIATIONS)

NOTES:
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CAGE NO. 03141 SHEET OF 2 — 20

DRAWING NO. 35-607 ROD 008

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

12N8 INHTAI

T2 30-028 P15 Q27 — T17 30-027 — D104 23-018 — D16 23-034 — D17 — D18 23-034

R9 56 P5 1/2 W

ITMI

A1 19-057 56 — A1 19-057 56

T2 30-028 P15 Q26 — T17 30-027 — D15 23-034 — D14 — D13 23-034

A6 19-100 D

289 IRTTA

T10 30-026 Q7

BIT 14

SA14 100-A IA14 98-A SA14 99-A D119 D120

R38 4.7K

101-A

RM 3 100 120 120 120 100 120 120 120

R69 2.15K 1%

21-083

SB14 103-A IB14 104-A SB14 102-A D118 D117

R37 4.7K

A22 19-099 SENSE AMP

N5B J9

R173 1K

236-1 MD140 — A105 19-134 TTL — 2K7 DSA0

A38 19-063 SDP

A98 19-125 580 — MS140 — 203-1

DOG1 11L8

T2 30-028 P16 Q29 — T18 30-027 — D22 23-034 — D23 — D24 23-034

A7 19-100 D

10J4 VTM

BIT 13

SA13 93-A IA13 91-A SA13 92-A D123 D124

R40 4.7K

R8 56 P5 1/2 W

T2 30-028 P16 Q28 — T18 30-027 — D21 23-034 — D20 — D19 23-034

12N8 INNTBI — 4C3 N32

T10 30-026 Q8 — N15

SB13 96-A IB13 97-A SB13 95-A D122 D121

R39 4.7K

SA5B1 12N5

SA5B1 12N6

A23 19-099 SENSE AMP

N5B J5, 10J5

R174 1K

136-1 MD130 — A105 19-134 TTL — 4K3 DS80

A38 19-063 SDP

A98 19-125 580 — MS130 — 103-1

DCO 11R8

DS1 11L8

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ASSY NO 03141 — DWG NO 35-607 — 008 — SHEET 3 OF 20

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

BIT 12

BIT 11

A24
19-099
SENSE AMP

A25
19-099
SENSE AMP

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		CHK	
		MGR	

TITLE SCHEMATIC
ELECTRONICS BRD
(32KB MEMORY)

03141
35-607 008

SHEET OF 4-20

REVISIONS

12N8 INHTAI
A10 19-100 D
T4 30-028 Q35 P15
T21 30-027
D40 23-034
D41
D42 23-034
R15 56 P5 1/2W
R46 4.7K
BIT 10
SA10 72-A
IA10 70-A
SA10 71-A
D135
D136
73-A
RM 7
100 120 120 2K
R73 2.15K 1/%
21-053
75-A SB10
IB10 76-A SB10
74-A
D134
D133
R45 4.7K
T11 30-026 Q11
489 IRTTB
D37 23-034
D38
T4 30-028 Q34 P15
T21 30-027
D39 23-034
A10 19-100 D
A26 19-099 SENSE AMP
N58 J9
R163 1K
234-1 MD100
A104 19-134 TTL
K7 DSCO
A40 19-063 SDF
A99 19-125 SBO
MS100 205-1
D0G1 11L8
SASAI 12N5
SASBI 12N6
10J4 VTH
A11 19-100 D
T4 30-028 Q37 P15
T22 30-027
D46 23-034
D47
D48 23-034
R14 56 P5 1/2W
R48 4.7K
BIT 9
SA9 65-A
IA9 63-A SA9
64-A
D139
D140
66-A
RM 8
100 120 120 2K
R74 2.16K 1/%
21-053
68-A SB9
IB9 69-A SB9
67-A
D138
D137
R47 4.7K
T11 30-026 Q12
N15
D43 23-034
D44
T4 30-028 Q36 P15
T22 30-027
D45 23-034
A11 19-100 D
12N8 INHTBI
4C8 N23
A27 19-099 SENSE AMP
N58 J5, 1055
R164 1K
134-1 MD090
A104 19-134 TTL
K3,6K3, 7K7 DSCO
A40 19-063 SDF
A99 19-125 SBO
MS090 105-1
DCO 11R8
DSI 11L8

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a) DIODES ARE 23-001.
b) TRANSISTORS ARE 20-020.

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

SCALE	NAME	TITLE	DATE
		DRAFT	
		MFR	
		ENGR	

TITLE SCHEMATIC ELECTRONICS BRD (32KB MEMORY)
ASY 03141
35-607 008
SHEET 5 OF 20

DRAWING 44 231 R4639

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

BIT 8

BIT 7

A28 19-099 SENSE AMP

A29 19-099 SENSE AMP

12N8 INRTI 01 — A2 19-057 56 — 02 — Q3 20-025 — R19 330 — R18 33 PS — R32 2.2K N15

Q13 — D53 23-034 — T23 30-027 — D52 — D54 23-034 — T12 30-026 — 15 02

12N7 INHTAI — A12 19-100 D — T5 30-028 — Q39 — N15

D49 23-034 — D50 — T23 30-027 — D51 23-034 — R17 56 1/2W PS — T5 30-028 — Q38 — N15 — A13 19-100 D

D106 23-018 — P21 7C2

T12 30-026 — Q14 — D59 23-034 — T24 30-027 — D58 — D60 23-034 — 7B1 IRTTC — T5 30-028 — Q41 — N16 — A13 19-100 D

D55 23-034 — D56 — D57 23-034 — R16 56 1/2W P5 — T5 30-028 — Q40 — N15 — 12N8 INHTBI — A13 19-100 D

10J4 VTH

R50 4.7K — 58-A 5A8 IA8 56-A 5A8 57-A — D143 D144

R52 4.7K — 49-A 5A7 IA7 51-A 5A7 50-A — D147 D148

R49 4.7K — 59-A 5B8 IB8 61-A 5B8 62-A — D142 D141

R51 4.7K — 52-A 5B7 IB7 54-A 5B7 55-A — D146 D145

RM9 — RM10 — 21-053 — 100 120 120 — R75 2.15K ±1% — R76 2.15K ±1%

5A5A1 12N5 — 5A5B1 12N6

N5A J9 — N5A J5, 10S4

R165 1K — 233-1 MD080 06 — A104 19-134 TTL — 07 — 5K7 DSC0

A441 19-063 SDF — DS 0 1 — DC — 10 09 11 08 13

A100 19-125 SBC — 12 09 12 — 11 MS080 <206-1

D061 11L8

R166 1K — 133-1 MD070 14 — A104 19-134 TTL — 13 — 7K3 DSD0

04 02 05 09 03 06 01

A100 19-125 SBC — 10 — 08 MS070 <106-1

DC0 11R8

DS1 11L8

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a) DIODES ARE 23-001.
b) TRANSISTORS ARE 2C 001.

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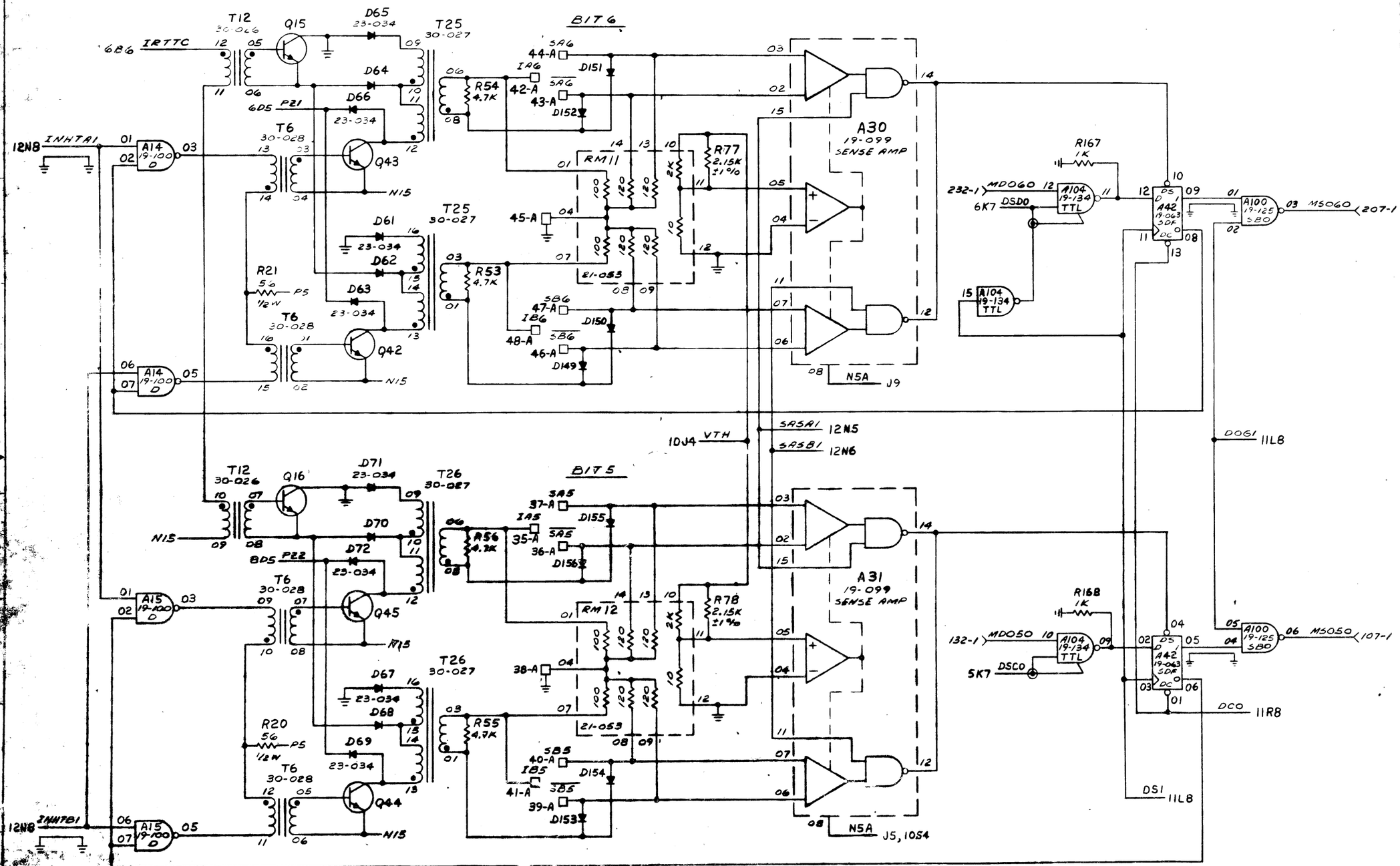
SCALE–	NAME	TITLE	DATE	TITLE SCHEMATIC ELECTRONICS BRD. (32KB MEMORY)
		DRAFT		03141
				35-607 D08

SHEET 20 OF 6

DRAWING 44231 24538

INTERDATA
Place, Oceanport, New Jersey 07757

REVISIONS



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) DIODES ARE 23-001.
   b) TRANSISTORS ARE 20-020.

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SCALE –	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC ELECTRONICS BRD. (32KB MEMORY)

DWG 03141 SHEET 7 OF 20
REV 32-607 008

BIT 4

BIT 3

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) DIODES ARE 23-001.
   b) TRANSISTORS ARE 20-020.

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SCALE –	NAME	TITLE	DATE
		DRAFT	

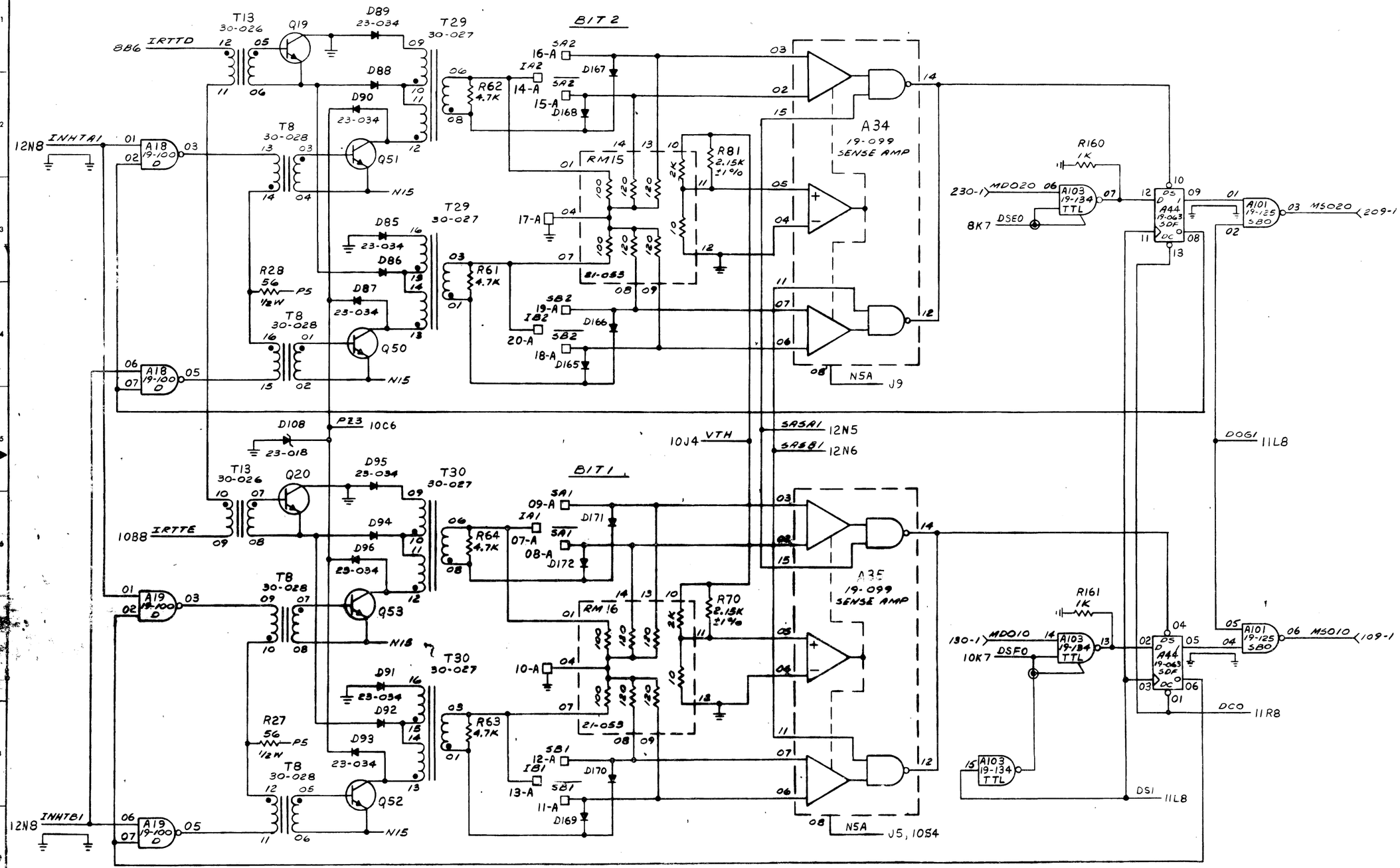
TITLE SCHEMATIC
ELECTRONICS BRD.
(32KB MEMORY)

03141
35-607 008

SHEET 8 OF 20

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) DIODES ARE 23-001.
   b) TRANSISTORS ARE 20-020.

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SCALE –	NAME	TITLE / DATE
		DRAFT
		CHK
		ENGR

TITLE SCHEMATIC ELECTRONICS BRD. (32KB MEMORY)

93141
35-607 008

SHEET 9 – 20

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

128-1 TEMP A
227-1 TEMP B
R157 330
R156 2.2K
RT2 23-012

C21 0.1UF
C1 15 UF
T. P. VTHM
TP5 TP4
P5 03 02 01
R181 500
GND T. P. 6
VTH 2G5, 3G5, 4G5, 5G5, 6G5, 7G5, 8G5, 9G5

P5
R107 39 1/2 W
04
13
14
Q61
T52 30-028
N15
R108 50 2W
R109 50 2W
D183 23-002 5.1V
D184 23-002 5.1V
N5A J9, 6J9, 7J9, 8J9, 9J9
N5B 2J9, 3J9, 4J9, 5J9

11G3 TI
11F7 READO
01
02
A70 19-137 D
03
03

SASA1 12N5
SASB1 12N6

N5 REGULATOR

A36 19-099 SENSE AMP
14
15
03
02
05
04
11
07
06
08 N5A S4

R162 1K
229-1 MD000
9K7 DSF0
12
A103 19-134 TTL
11
A45 19-063 SDF
OS
D
Q
DC
10
12
09
11
08
13
R102 19-125 S80
10
09
08 MS000 210-1
DOG1 11L8
DCO 11R8
DS1 11L8

BIT 0

SA0 02-A
IA0 00-A
SA0 01-A
D175
D176
SB0 05-A
IB0 06-A
SB0 04-A
D173
D174
R66 4.7K
R65 4.7K
06
08
03
01
RM17
01
14 13 10 11 12
100 120 120 2K
100 120 120 10
04
03-A
07
21-053
08 09
R83 2.15K ±1%

12N8 INHTAI
12N8 INHTBI
A3 19-100 D
01
02
03
07
06
05
T9 30-028
13 03 14 04
16 01 15 02
N15 Q55
N15 Q54
T31 30-027
12 11 10 09
13 03 14 15 01
PZ3 9D5
D102 23-034
D100
D101 23-034
R29 56 P5 1/2 W
23-034
D98
D97 23-034
T14 30-026
16 01 15 02
986 IRTTE
N15
Q21

NOTES:
1. UNLESS OTHERWISE SPEC:
a) DIODES ARE 23-001.
b) TRANSISTORS ARE 20-020.

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SCALE –	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC ELECTRONICS BRD (32KB MEMORY)
PART NO. 03141
DWG NO. 35-607 D08
SHEET OF 10 — 20

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

FOR PREVIOUS REV. INFO SEE VOIDED MICRO-FILM COPY 35-607 DOB SHT 11, REV			
25	E937	11-4-76	1
AREA C2: A87-05,-06 PIN NUMBERS WERE REVERSED.			
31	3072	9-8-77	

W/O PARITY (F02, F04, & F06)
W/ PARITY (F01, F03, & F05)
R138 470 P5
PAR0 < 105-0
MB20 < 235-0
XMA15 0 108-0
XMA14 0 208-0
MA000 106-0
ERO 204-0
MCO
SRC1
SELECT JUMPER AT TEST
TYPICAL CONNECTION
R146 180
R147 270
A90 30-041 DELAY LINE
.75 u SEC (F01 & F02)
1.0 u SEC (F03 & F04)
T18 (T22) NOTE 2
M4
J4
L7
SCL1
12A1
M80
RTO 12E1
RT1 12F4
R145 470
A80 19-131 SDF
A79 19-131 SDF
A78 19-131 SDF
A75 19-131 SDF
A74 19-131 SDF
A73 19-131 SDF
CLK
CLR
(F00-F04) J8
(F00-F04) H9
F05 & F06
WTO 12E1
WT1 12F5
CHTO 17F8
READO 10K5, 13A4, 17C4
WRITEO 12K5, 14A4 17C4
WRTO 127-1
CWMI
RRMI 12K5
FO5 & F06 ONLY
R128 470
35-607 FO5 & F06 K4 (T16)
35-607 F01-4 N4
DCO N8
DUAO < 135-0
DISABLE DUAO
DS1 2M9, 3M9, 4M9, 5M9, 6M9, 7M9, 8M9, 9M9, 10M9
DOG1 2N5, 3N5, 4N5, 5N5, 6N5, 7N5, 8N5, 9N5, 10N6
R98 150
R125 150
R127 470
R126 470
A4
C8
DCO 2N8, 3N8, 4N8, 5N8, 6N8, 7N8, 8N8, 9N8, 10N8, G7

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) DIODES ARE 23-001.
   b) TRANSISTORS ARE 20-020.
2. TIMING TAP REFERENCES IN BRACKETS APPLY TO 35-607 FO5 & F06 ONLY.

MEMORY TIMING

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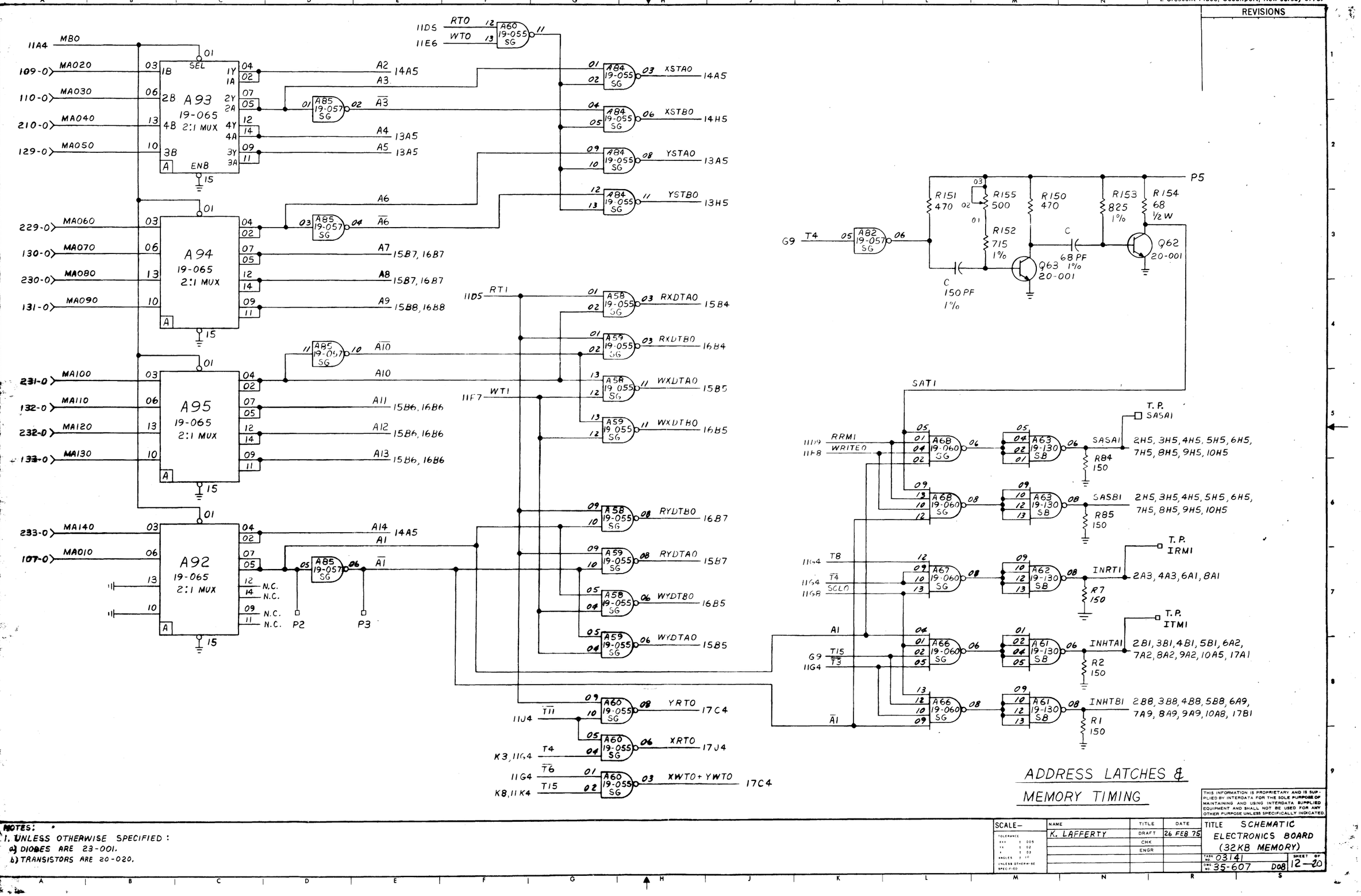
SCALE –	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1/2°, UNLESS OTHERWISE SPECIFIED	K. LAFFERTY	DRAFT	27 FEB 75
		CHK	
		ENGR	

TITLE SCHEMATIC ELECTRONICS BOARD (32K8 MEMORY)
TASK NO. 03141
DWG NO. 35-607 REV D08
SHEET OF 11 — 20

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



ADDRESS LATCHES & MEMORY TIMING

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
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SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	K. LAFFERTY	DRAFT	26 FEB 75
		CHK	
		ENGR	

TITLE SCHEMATIC ELECTRONICS BOARD (32KB MEMORY)
DASH NO. 03141
DWG NO. 35-607 D08
SHEET 12 OF 20

INTERDATA

REVISIONS

1761 +5KV

P5

R94 39 1/2 W

T40 30-028

QM9 20-026

A54 19-136

INPUTS

OUTPUTS

H4, 11F7 READ 15 A

H5, 12E2 A5 13 C

12H2 YSTB0 12 D

1 OF 10 DECODER

0 1 2 3 4 5 6 7 8 9

01 02 03 04 05 06 07 09 10 NC 11 NC

YS0 □ 17-B

YS1 □ 16-B

YS2 □ 15-B

YS3 □ 14-B

T41 30-028

QM10 20-026

17N1 -5KV

P5

R95 39 1/2 W

T42 30-028

QM11 20-026

A55 19-136

A4 READ 15 A

A4 A4 14 B

A4 A5 13 C

12H3 YSTB0 12 D

1 OF 10 DECODER

YS4 □ 13-B

YS5 □ 12-B

YS6 □ 11-B

YS7 □ 10-B

T43 30-028

QM12 20-026

Y SINK

NOTES

NAME	TITLE	DATE	TITLE FUNCT. SCHEMATIC ELECTRONICS BOARD (32 KB MEMORY)
	DRAFT		
	CHK		
	ENGR		
			TABC NO. 03141 SHEET OF 13-20
	DIR ENG		DWG NO. 35-607 DATE

INTERDATA®

REVISIONS

17G1 +5KV

17N1 −5KV

P5

R96 39 12 W

R97 39 112 W

T44 30-028 · T45 30-028 · T46 30-028 · T47 30-028

QM13 20-026 · QM14 20-026 · QM15 20-026 · QM16 20-026

A56 19-136 — 1 OF 10 DECODER

A57 19-136 — 1 OF 10 DECODER

H4, 11F8 WRITE0 15 A

H5, 12E6 A14 14 B

H5, 12E1 A2 13 C

12H1 XSTA0 12 D

A4 WRITE0 15 A

A5 A14 14 B

A5 A2 13 C

12H2 XSTB0 12 D

01 02 03 04 05 06 07 09 10 NC 11 NC

X50 □ 09-B

X51 □ 08-B

X52 □ 07-B

X53 □ 06-B

X54 □ 05-B

X55 □ 04-B

X56 □ 03-B

X57 □ 02-B

X SINK

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NOTES

DRAWING 44-231 16042

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE FUNCT. SCHEMATIC ELECTRONICS BOARD (32 KB MEMORY)

03141 35-607 DOB

SHEET 14 OF 20

INTERDATA

P5

R88 56 1/2W
R89 56 1/2W
R86 56 1/2W
R87 56 1/2W

A48 19-136 1 OF 10 DECODER
A49 19-136 1 OF 10 DECODER
A47 19-136 1 OF 10 DECODER
A46 19-136 1 OF 10 DECODER

12H4 RXDTA0
12H3 WYDTA0
12E5 A11
12E5 A12
12E5 A13
12H7 RYDTA0
12E3 A7
12E3 A8
12E4 A9
12H5 WXDTA0

QM3 20-026
T34 30-028
T35 30-028
QM4 20-026

XRA0+YWA0 → 34-B
XRA1+YWA1 → 33-B
XRA2+YWA2 → 31-B
XRA3+YWA3 → 32-B
XRA4+YWA4 → 30-B
XRA5+YWA5 → 29-B
XRA6+YWA6 → 27-B
XRA7+YWA7 → 28-B
XRA5'1+YWC5' → 17L1

QM1 20-026
T32 30-028
T33 30-028
QM2 20-026

XWC0+YRC0 → 50-B
XWC1+YRC1 → 49-B
XWC2+YRC2 → 47-B
XW'C3+YRC3 → 48-B
XWC4+YRC4 → 46-B
XWC5+YRC5 → 45-B
XWC6+YRC6 → 43-B
XWC7+YRC7 → 44-B
YRC5'0+XWC5'0 → 17E1

X/Y DRIVE

NOTES

NAME	TITLE	DATE	TITLE FUNCT. SCHEMATIC ELECTRONICS BRD. (32 KB MEMORY)
G. MELTON	DRAFT		
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03191 DWG NO. 35-607 DOC SHEET OF 15-20

P5

R93 56 1/2W

R91 56 1/2W

R92 56 1/2W

R90 56 1/2W

A52 19-136 1 OF 10 DECODER

A53 19-136 1 OF 10 DECODER

A51 19-136 1 OF 10 DECODER

A50 19-136 1 OF 10 DECODER

12I14 RXDTB0

12I17 WYDTB0

12E5 A11

12E5 A12

12E5 A13

12H6 RYDTB0

12E3 A7

12E3 A8

12E4 A9

12H5 WXDTB0

T38 30-028

QM7 20-026

XRA8+YWA8 — 26-B

XRA9+YWA9 — 25-B

XRA10+YWA10 — 23-B

XRA11+YWA11 — 24-B

XRA12+YWA12 — 22-B

XRA13+YWA13 — 21-B

XRA14+YWA14 — 19-B

XRCS1+YWCS1 — 17L1

XRA15+YWA15 — 20-B

T36 30-028

QM5 20-026

XWC8+YRC8 — 42-B

XWC9+YRC9 — 41-B

XWC10+YRC10 — 39-B

XWC11+YRC11 — 40-B

T37 30-028

QM6 20-026

XWC12+YRC12 — 38-B

XWC13+YRC13 — 37-B

XWC14+YRC14 — 35-B

XWC15+YRC15 — 36-B

YRCS0+XWCS0 — 17E1

X/Y DRIVE

...ARY AND STOR... ...E PURPOSE OF... ...ING ... IS APPLIED... ...NEXT HIGHER... ...SETS UP ... INDICATE...

NAME: MELTON	DRAFT / CHK / ENGR / DRFTG	DATE	TITLE: FUNCT. SCHEMATIC ELECTRONICS BRD. (32KB MEMORY)
			SIZE: D 53141 — 35-607 — DOS — SHEET 16 OF 20

2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

AREA L4: A183 WAS NOT SPEC'D. AREA L4: A182 WAS NOT SPEC'D			
W/S	M	2801	5-72

SYSTEM CLEAR

X-Y CURRENT SOURCE

BIAS SOURCE

CHARGE CIRCUIT REQ'D FOR 35-607 F01 & F02 ONLY

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) DIODES ARE 23-001.
   b) TRANSISTORS ARE 20-020.

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SCALE—

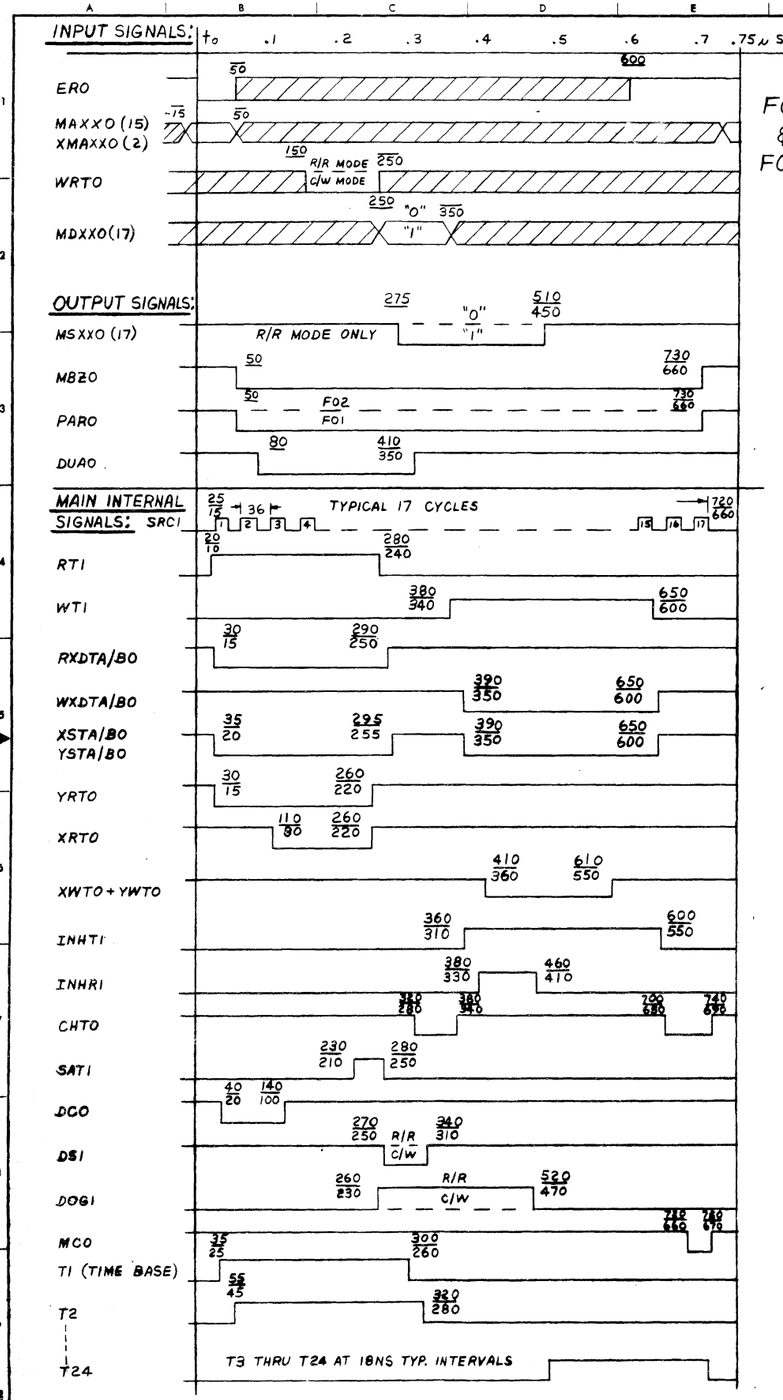
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

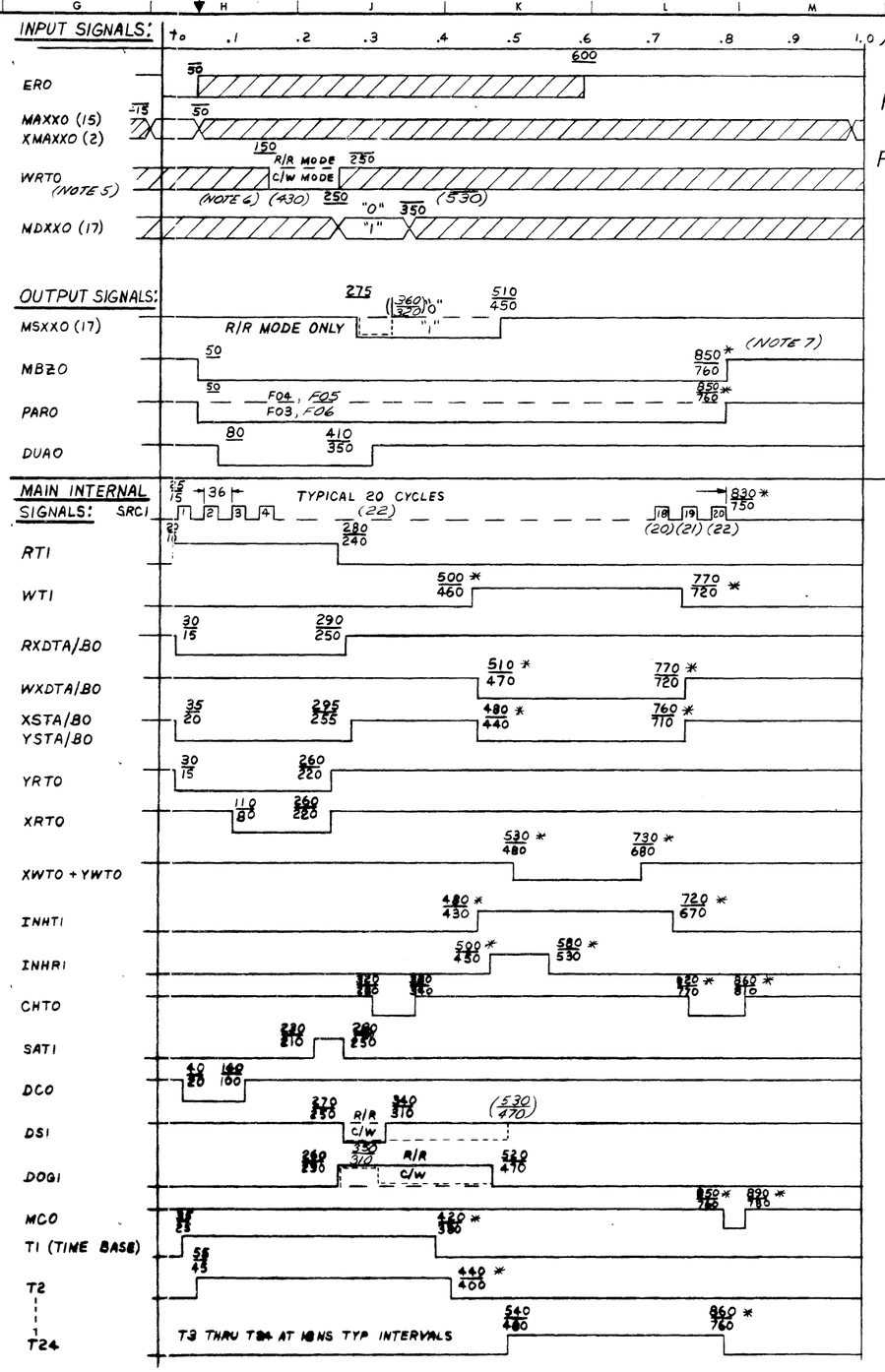
SCHEMATIC
ELECTRONICS BOARD
(32 K MEMORY)

DWG NO. 03141 SHEET 08
REV NO. 35-607 R01 D08 17

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
F05, F06 & RELATED INFO. WAS NOT SPECD. ADDED NOTES 5, 6 & 7.
WSJ 2932 - 1446-76 RM





NOTES:
1. SHADED AREA (////) INDICATES "CAN CHANGE" OR "DO NOT CARE" INTERVAL.
2. UNLESS OTHERWISE INDICATED TIME IS IN NANOSECONDS.
3. THE NUMBER ABOVE THE LINE INDICATES MAXIMUM TIME; BELOW THE LINE IS MINIMUM.
4. ALL SIGNALS ARE OF STANDARD TTL LEVELS & TIMING IS REFERENCED TO 1.5V.
5) NOT APPLICABLE TO F05 & F06
6) REFERENCES IN BRACKETS ARE APPLICABLE TO F05 & F06 ONLY.
7) REFERENCES DESIGNATED WITH (*) ADD 80 NANO SECONDS FOR F05 & F06 ONLY.

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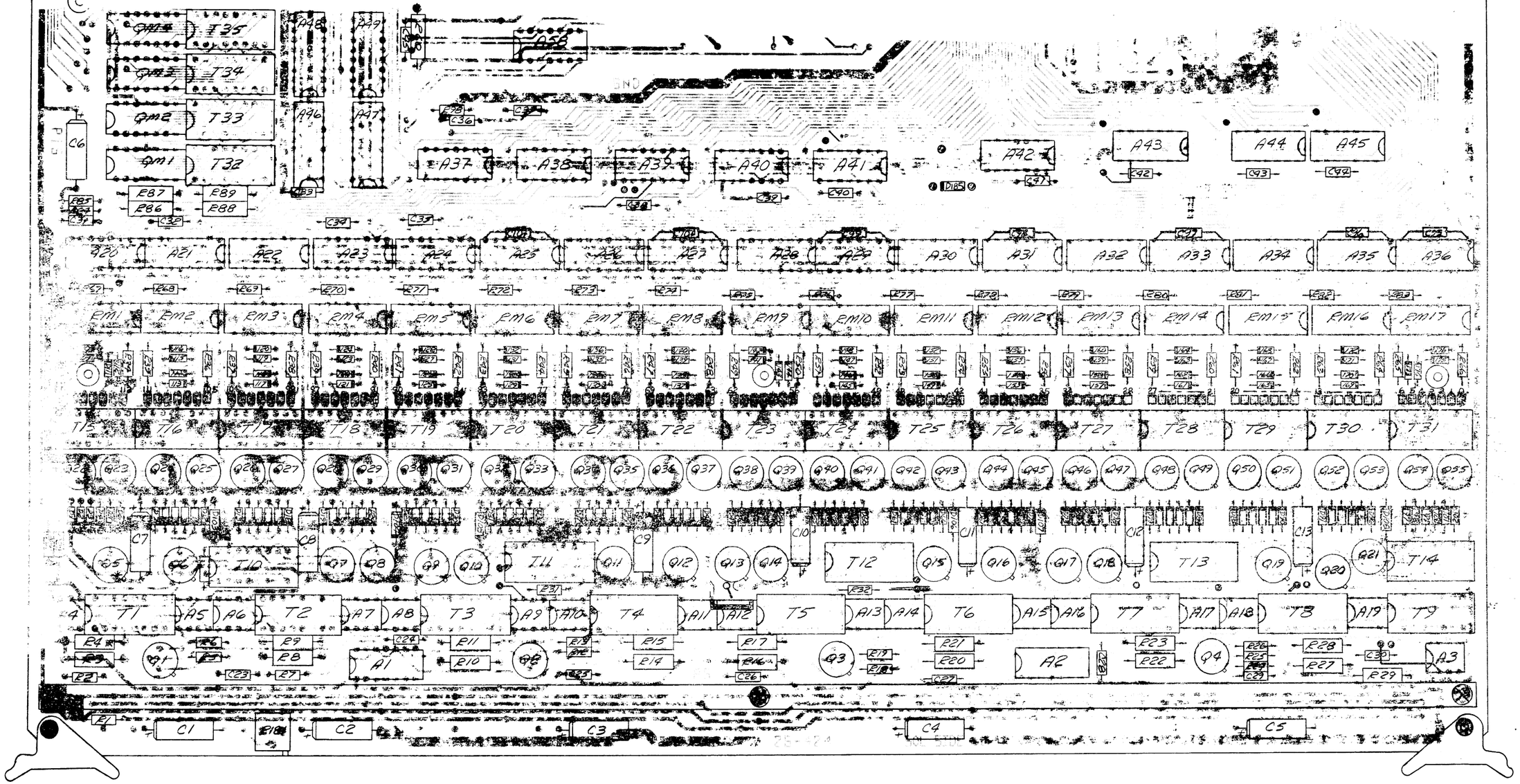
SCALE—
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
ELECTRONICS BOARD
(32KB MEMORY)

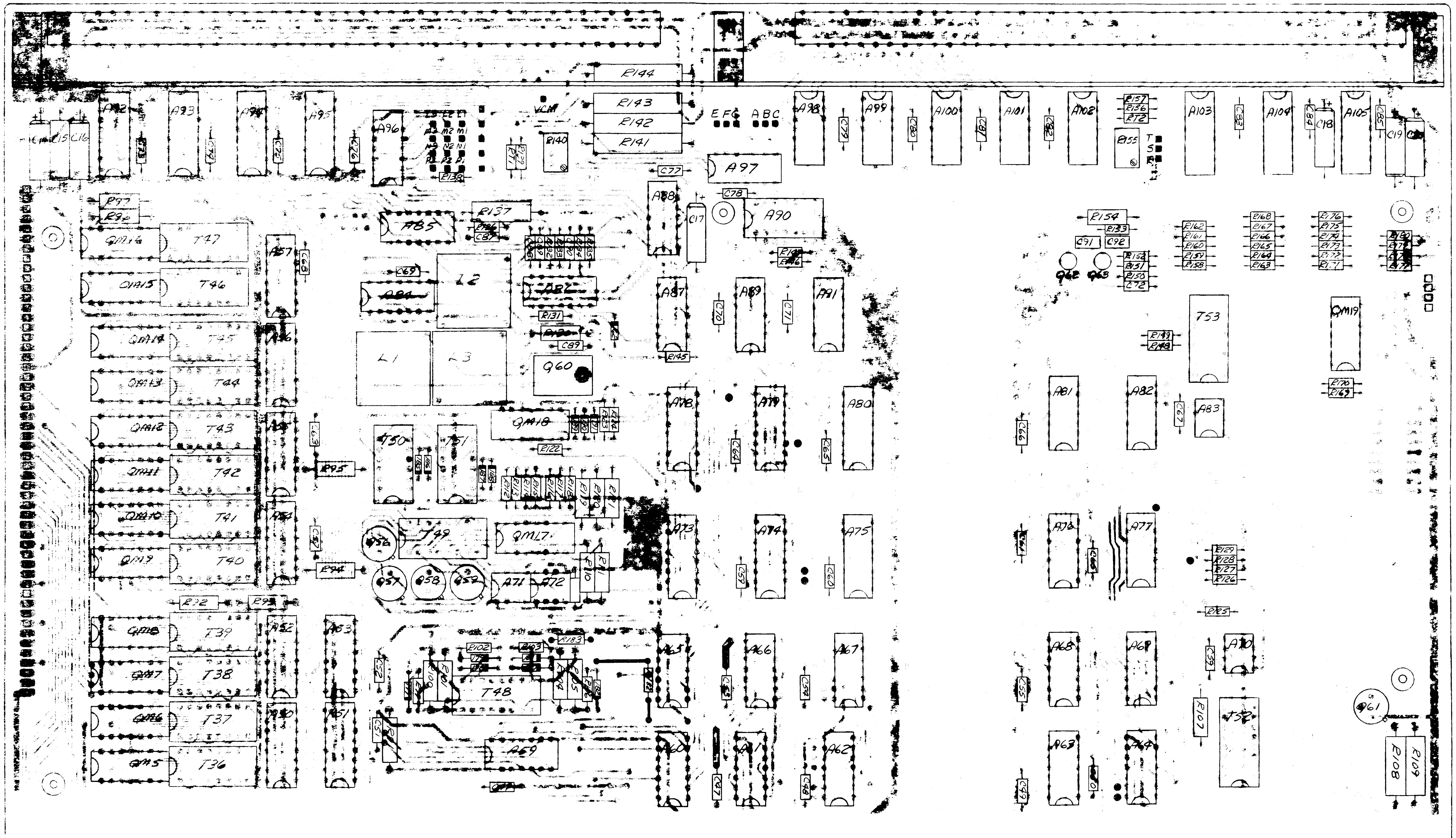
TASK NO. 03141
DWG NO. 35-607 R01 D08
SHEET OF 18 — 20

BRUNING 44-239 3858



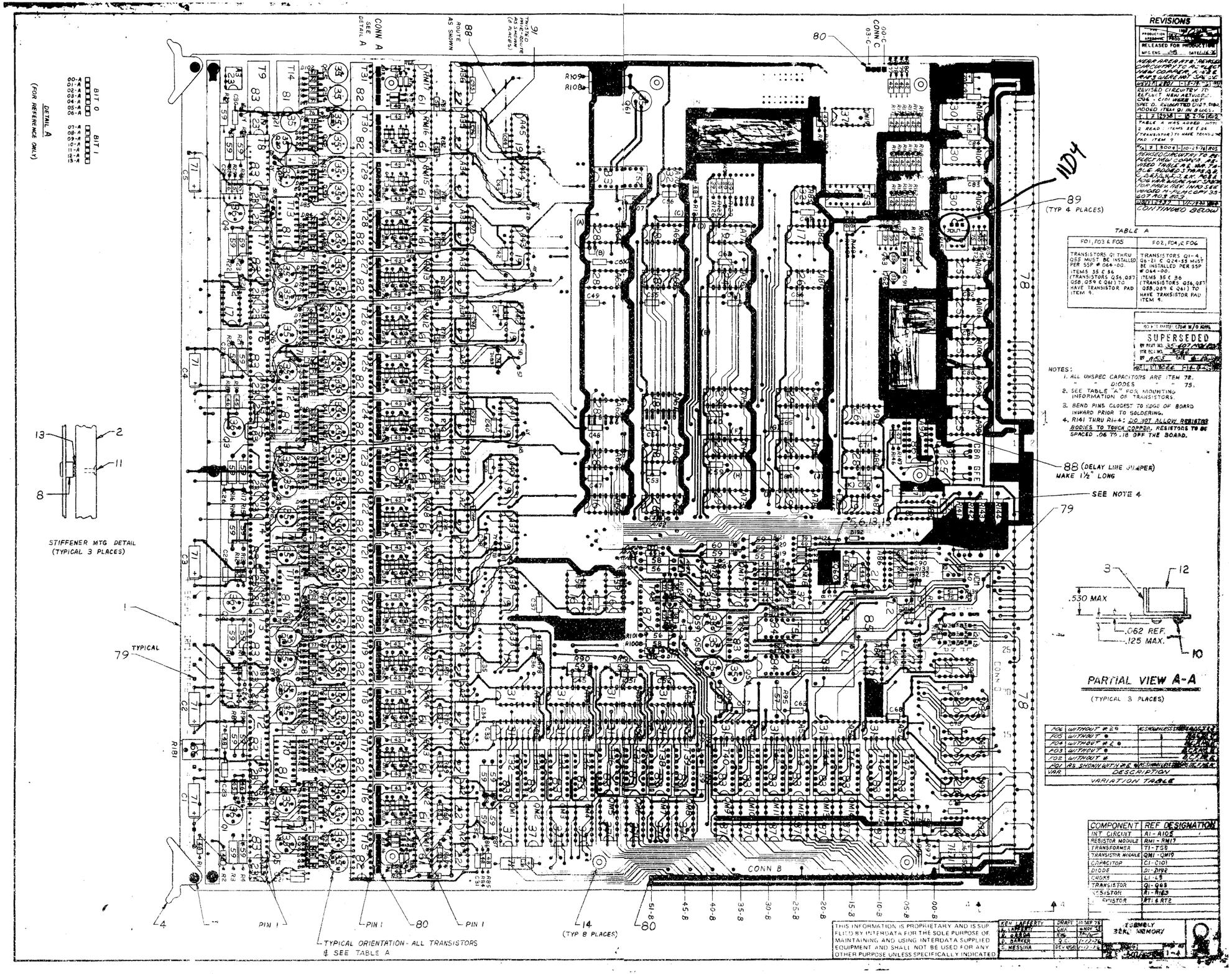
VIEWED FROM SOLDER SIDE
FOR COMPONENT REFERENCE ONLY

REVISIONS				J. HELVATY	DRAFT	10-22-75	SCHEMATIC ELECTRONICS BOARD (32 KB MEMORY	
ADDED COMPONENTS C95-C101								
RELOCATED COMPS C71-84 & D195								
CHANGED CIRCUITRY ID # ETC.								
NEW ART WORK.								
JC		2958	-	7-30-76	R01		03141	SHEET 19-20
							35-607 R01 D08	



VIEWED FROM SOLDER SIDE
FOR COMPONENT REFERENCE ONLY

C47 & C53 WERE NOT GROUNDED	REVISIONS	J. HELVATY	DRAFT	10-23-75	SCHEMATIC ELECTRONICS BOARD (32KB MEMORY)
JC 2938 - 7-30-76 R02	R182 & R183 PLUS RELATED CIRCUITRY WAS NOT SPEC'D				
REVISED CIRCUITRY TO REFLECT NEW C.O.P.					03141
WS 2951 - VI-16-76 R03	WS 2801 - 5-19-76 R01				35-607 R02 D08 · SHEET 20-20


REVISIONS
RELEASED FOR PRODUCTION
CONTINUED BELOW
SUPERSEDED
NOTES:
1. ALL UNSPEC CAPACITORS ARE ITEM 78.
" " DIODES " 75.
2. SEE TABLE "A" FOR MOUNTING INFORMATION OF TRANSISTORS.
3. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING.
4. R141 THRU R144: DO NOT ALLOW RESISTOR BODIES TO TOUCH COPPER. RESISTORS TO BE SPACED .06 TO .18 OFF THE BOARD.
TABLE A
FO1, FO3 & FO5
FO2, FO4, & FO6
TRANSISTORS Q1 THRU Q55 MUST BE INSTALLED PER SSP # 064-00. ITEMS 35 & 36 (TRANSISTORS Q56, Q57 Q58, Q59 & Q61) TO HAVE TRANSISTOR PAD ITEM 9.
TRANSISTORS Q1-4, Q6-21 & Q24-55 MUST BE INSTALLED PER SSP # 064-00. ITEMS 35 & 36 (TRANSISTORS Q56, Q57 Q58, Q59 & Q61) TO HAVE TRANSISTOR PAD ITEM 9.
VARIATION TABLE
COMPONENT
REF DESIGNATION
INT CIRCUIT A1 - A105
RESISTOR MODULE RM1 - RM17
TRANSFORMER T1 - T59
TRANSISTOR MODULE QM1 - QM10
CAPACITOR C1 - C101
DIODE D1 - D192
CHOKE L1 - L9
TRANSISTOR Q1 - Q68
RESISTOR R1 - R183
POTENTIOMETER RT1 & RT2
ASSEMBLY 32K MEMORY
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.
DETAIL A
(FOR REFERENCE ONLY)
BIT 0
BIT 1
STIFFENER MTG DETAIL
(TYPICAL 3 PLACES)
PARTIAL VIEW A-A
(TYPICAL 3 PLACES)
TYPICAL ORIENTATION - ALL TRANSISTORS & SEE TABLE A
(TYP 8 PLACES)
(TYP 4 PLACES)
CONN A
CONN B
CONN C
PIN 1
80
79
78
89
88 (DELAY LINE JUMPER) MAKE 1½" LONG
SEE NOTE 4

BACK PANEL MAP

CONN	CONN. POSITION MOTHER BOARD VERTICAL POS.	32KB MEMORY HORIZONTAL POSITION 1	2
/	41	P5	GND
	40	GND	GND
	39	P15	P15
	38	N15	N15
	37	MD150	MD160
	36	MD130	MD140
	35	MD110	MD120
	34	MD090	MD100
	33	MD070	MD080
	32	MD050	MD060
	31	MD030	MD040
	30	MD010	MD020
	29		MD000
	28	TEMP A	
	27	WRTO	TEMP B
	26		
	25		
	24		
	23		
	22		
	21		
	20		
	19		
	18		
	17		
	16		
	15		
	14		
	13		
	12		
	11		
	10		MS000
	09	MS010	MS020
	08	MS030	MS040
	07	MS050	MS060
	06	MS070	MS080
	05	MS090	MS100
	04	MS110	MS120
	03	MS130	MS140
	02	MS150	MS160
	01	GND	GND
	00	P5	GND
O	41	P5	GND
	40	GND	GND
	39		
	38		
	37		
	36		
	35	DUAO	MB20
	34		
	33	MA130	MA140
	32	MA110	MA120
	31	MA090	MA100
	30	MA070	MA080
	29	MA050	MA060
	28		
	27		
	26	SCLRO	
	25		
	24		
	23		
	22		
	21		
	20		
	19		
	18		
	17		
	16		
	15		
	14		
	13		
	12		
	11		
	10	MA030	MA040
	09	MA020	
	08	XMA150	XMA140
	07	MA010	
	06	MA000	
	05	PARO	
	04		ERO
	03		
	02	P15	N15
	01	GND	GND
	00	P5	GND

118	IB16
117	SB16
116	$\overline{SB16}$
115	GND
114	SA16
113	$\overline{SA16}$
112	IA16

13	IB1
12	SB1
11	$\overline{SB1}$
10	GND
09	SA1
08	$\overline{SA1}$
07	IA1
06	IB0
05	SB0
04	$\overline{SB0}$
03	GND
02	SA0
01	$\overline{SA0}$
00	IA0

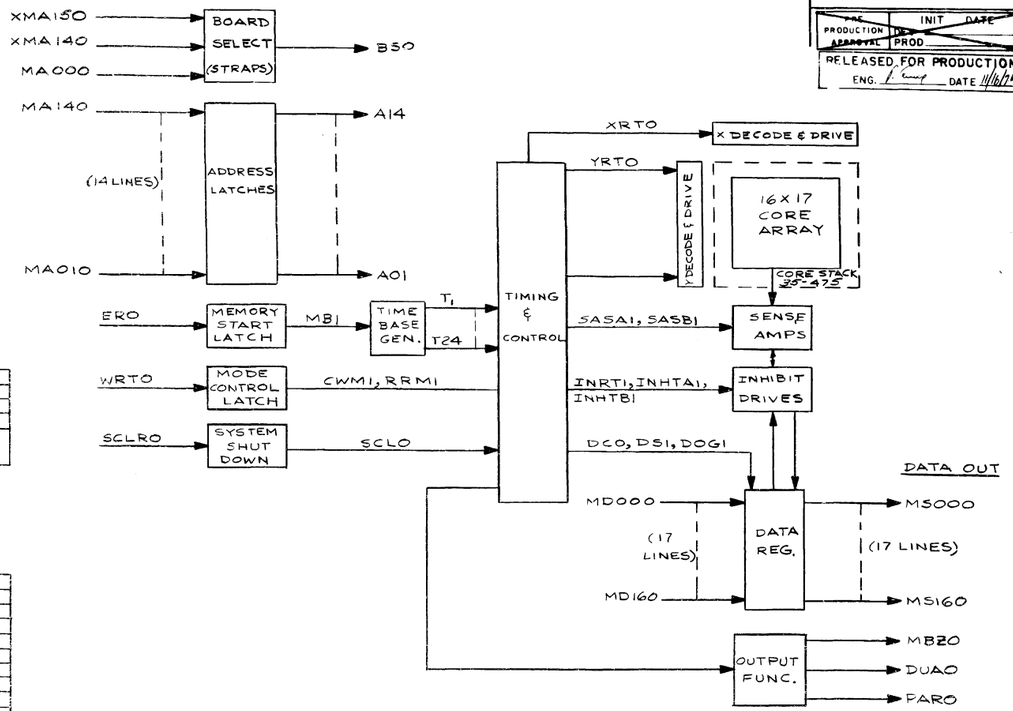
CONN A

0	XCHC
1	XCHA
2	YCHC
3	YCHA

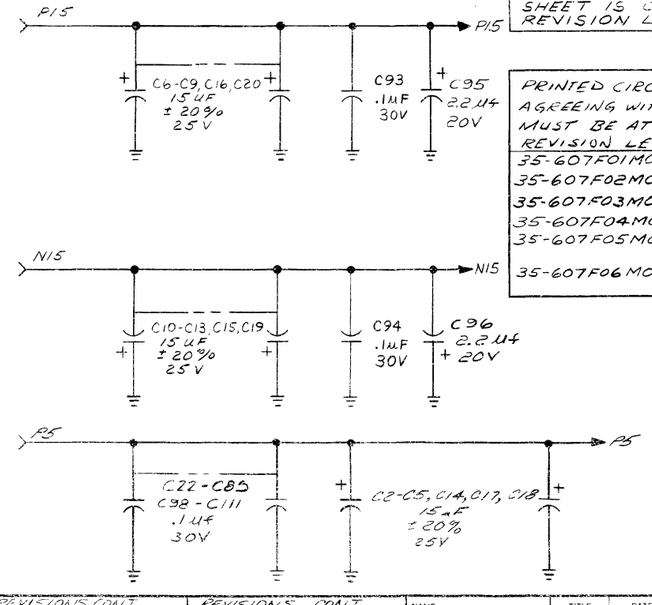
CONN C

00	GND	
01	GND	
02	XS7	
03	XS6	
04	XS5	
05	XS4	
06	XS3	
07	XS2	
08	XS1	
09	XS0	
10	YS7	
11	YS6	
12	YS5	
13	YS4	
14	YS3	
15	YS2	
16	YS1	
17	YS0	
18	N15	
19	XRA14 + YWA14	
20	15	15
21	13	13
22	12	12
23	10	10
24	11	11
25	9	9
26	8	8
27	6	6
28	7	7
29	5	5
30	4	4
31	2	2
32	3	3
33	1	1
34	XRA0 + YWA0	
35	XWC14 + YRC14	
36	15	15
37	13	13
38	12	12
39	10	10
40	11	11
41	9	9
42	8	8
43	6	6
44	7	7
45	5	5
46	4	4
47	2	2
48	3	3
49	1	1
50	XWC0 + YRC0	
51	P15	

CONN B



32 KB CORE MEMORY BLOCK DIAGRAM



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PRINTED CIRCUIT BOARD ASSEMBLIES AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-607F01M01R06	.75 μSec W/PAR
35-607F02M01R06	.75 μSec W/O PAR
35-607F03M01R06	1.0 μSec W/PAR
35-607F04M01R06	1.0 μSec W/O PAR
35-607F05M01R06	1.0 μSEC W/PAR READ MODIFY WRITE
35-607F06M01R06	1.0 μSEC W/O PAR READ MODIFY WRITE

REVISIONS

REVISED SHT 11

WS	JV	3072	9-16-77	R01

REVISED SHT'S 11 & 18 AREA N7 35-607F01M01 THRU 35-607F06M01 WERE R00.

PM	JV	3188	6-19-77	R02

REVISED SHT'S 10 & 11 & 18 AREA N7 35-607F01M01 THRU 35-607F06M01 WERE R02.

PM	JV	3148	6-21-77	R03

REVISED SHTS 2 & 17 35-607F01M01 — F06 M01 WAS R02

PM	JV	3227	7-5-77	R04

CONT. BELOW

SHEET INDEX	REV	6	1							1	4	1				2	3	1
	SHT. NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

NOTES

REVISIONS CONT
35-607F01M01 - F06 M01 WERE R04
GP JV 3407 12-8-77 R06

REVISIONS CONT.
REVISED SHTS 17 & 20
35-607F01M01 - F06 M01 WERE R03.
GP JV 3366 11-15-77 R05
REVISED SHTS. 11, 12, 18

NAME	TITLE	DATE
W. LIMPERT	DRAFT	3/15/76
H. MATTER	CHK	9/15/76
P. OBRDA	ENGR	11-17-76
B. MULLER	TEST	11-17-76
S. MESSINA	MGR.	11-17-76

TITLE SCHEMATIC
ELECTRONICS BOARD (32KB MEMORY)
TASK NO. 03017
DWG NO. 35-607M01RD6008
SHEET OF 1-20

INTERDATA®

REVISIONS

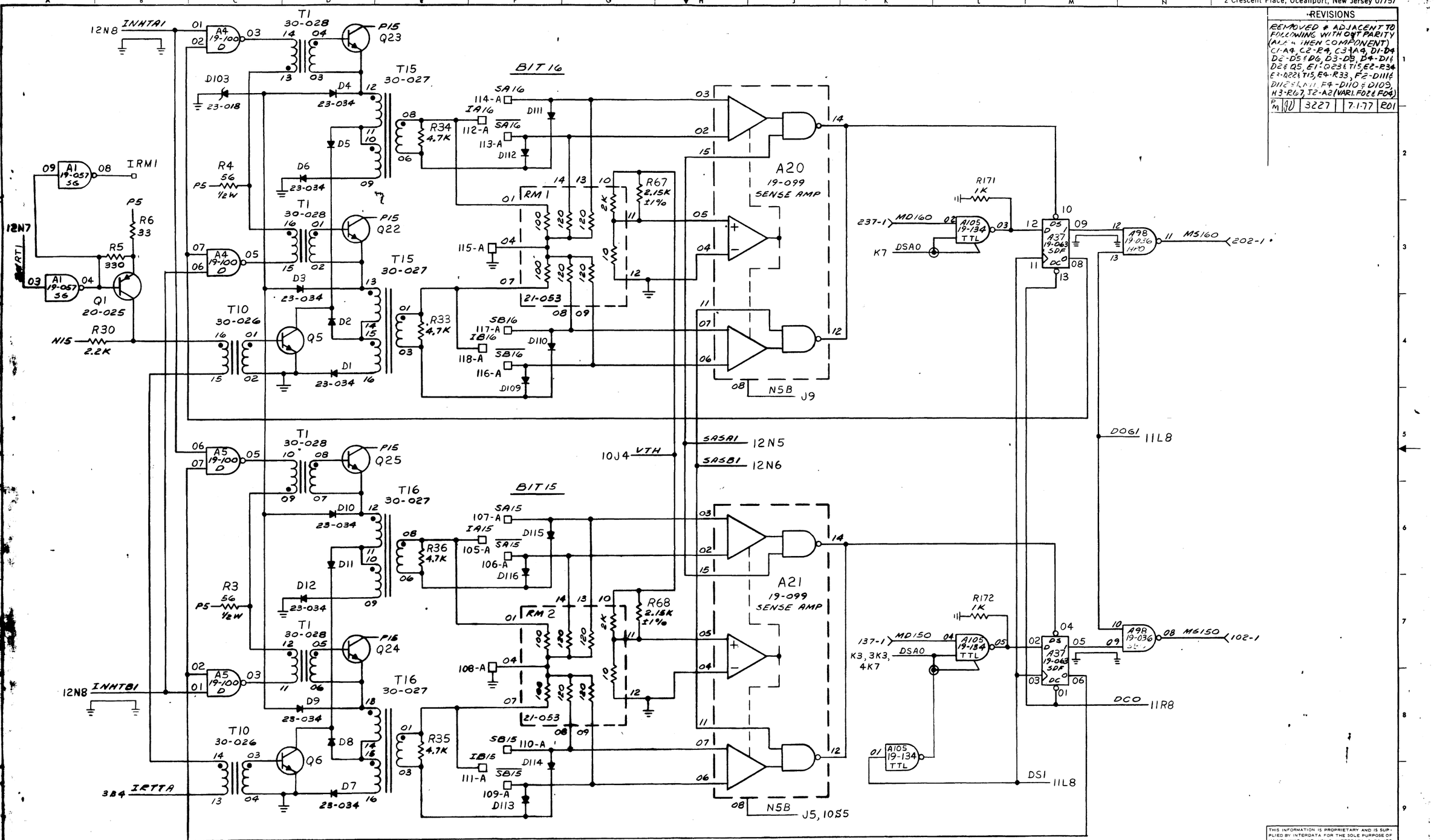
LTR	INIT	DATE
PRODUCTION APPROVAL	DR PROD	

RELEASED FOR PRODUCTION
ENG. _____ DATE 11/16/76

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

REMOVED # ADJACENT TO FOLLOWING WITH OUT PARITY (ALSO WHEN COMPONENT) C1-A4, C2-R4, C3-A4, D1-D4 D2-D5 & D6, D3-D9, D4-D16 D2 & Q5, E1-Q23 & T15, E2-R34 E3-R22 & T15, E4-R33, F2-D111 & D112 & R171, F4-D110 & D109, H3-R67, T2-A2 (VARI. FOR F04)				
P M	JJ	3227	7.1.77	R01



NOTES:
UNLESS OTHERWISE SPECIFIED:
A) DIODES ARE 23-001.
B) TRANSISTORS ARE 20-020.

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SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005 XX ± .02 X ± .03 ANGLES ± 1°		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC ELECTRONICS BRD (32KB MEMORY)
TASK NO. 03017
DWG NO. 35-607MNR01008
SHEET 2 OF 20

INTERDATA®

BACK PANEL MAP

CONN	CONN. POSITION MOTHER BOARD VERTICAL POS.	32KB MEMORY HORIZONTAL POSITION 1	2
/	41	P5	GND
	40	GND	GND
	39	P15	P15
	38	N15	N15
	37	MD150	MD160
	36	MD130	MD140
	35	MD110	MD120
	34	MD090	MD100
	33	MD070	MD080
	32	MD050	MD060
	31	MD030	MD040
	30	MD010	MD020
	29		MD000
	28	TEMPA	
	27	WRTO	TEMP B
	26		
	25		
	24		
	23		
	22		
	21		
	20		
	19		
	18		
	17		
	16		
	15		
	14		
	13		
	12		
	11		
	10		MS000
	09	MS010	MS020
	08	MS030	MS040
	07	MS050	MS060
	06	MS070	MS080
	05	MS090	MS100
	04	MS110	MS120
	03	MS130	MS140
	02	MS150	MS160
	01	GND	GND
	00	P5	GND
0	41	P5	GND
	40	GND	GND
	39		
	38		
	37		
	36		
	35	DUAO	MBZO
	34		
	33	MA130	MA140
	32	MA110	MA120
	31	MA090	MA100
	30	MA070	MA080
	29	MA050	MA060
	28		
	27		
	26	SCLRO	
	25		
	24		
	23		
	22		
	21		
	20		
	19		
	18		
	17		
	16		
	15		
	14		
	13		
	12		
	11		
	10	MA030	MA040
	09	MA020	
	08	XMA150	XMA140
	07	MA010	
	06	MA000	
	05	PARO	
	04		ERO
	03		
	02	P15	N15
	01	GND	GND
	00	P5	GND

118	IB16
117	SB16
116	$\overline{SB16}$
115	GND
114	SA16
113	$\overline{SA16}$
112	IA16

13	IB1
12	SB1
11	$\overline{SB1}$
10	GND
09	SA1
08	$\overline{SA1}$
07	IA1
06	IB0
05	SB0
04	$\overline{SB0}$
03	GND
02	SA0
01	$\overline{SA0}$
00	IA0

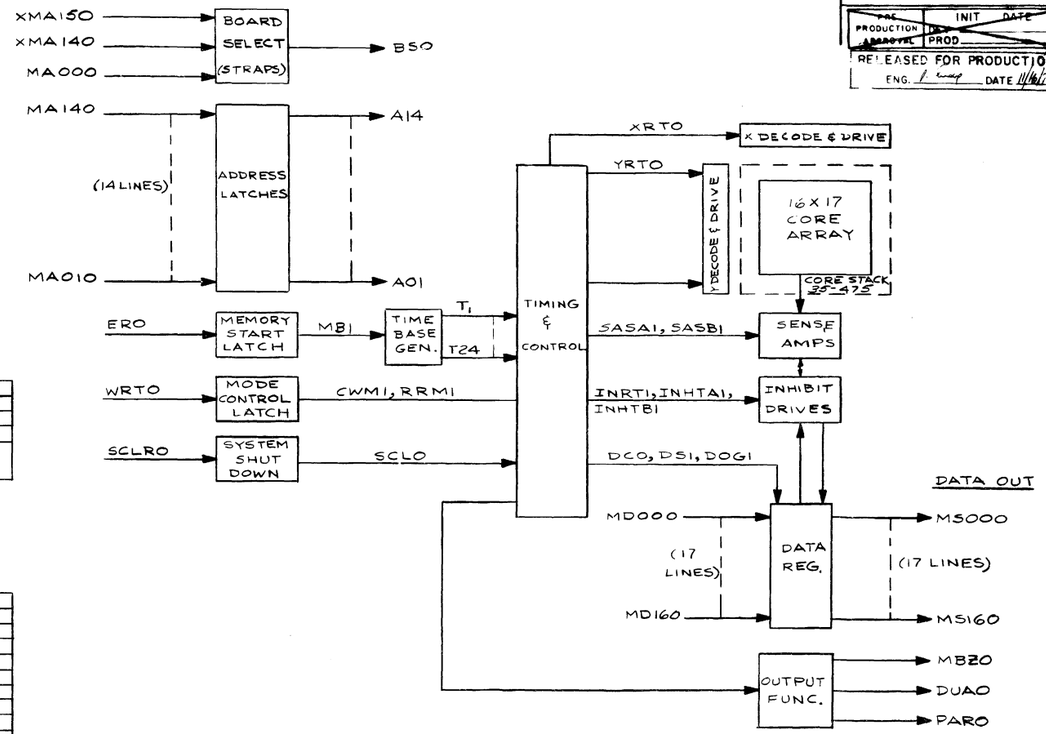
CONN A

0	XCHC
1	XCHA
2	YCHC
3	YCHA

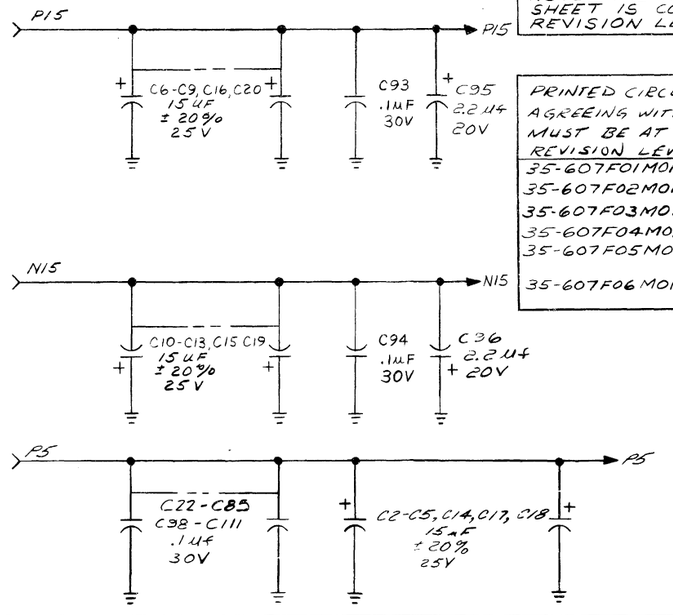
CONN C

00	GND	
01	GND	
02	XS7	
03	XS6	
04	XS5	
05	XS4	
06	XS3	
07	XS2	
08	XS1	
09	XS0	
10	YS7	
11	YS6	
12	YS5	
13	YS4	
14	YS3	
15	YS2	
16	YS1	
17	YS0	
18	N15	
19	XRA14 + YWA14	
20	15	15
21	13	13
22	12	12
23	10	10
24	11	11
25	9	9
26	8	8
27	6	6
28	7	7
29	5	5
30	4	4
31	2	2
32	3	3
33	1	1
34	XRA0 + YWA0	
35	XWC14 + YRC14	
36	15	15
37	13	13
38	12	12
39	10	10
40	11	11
41	9	9
42	8	8
43	6	6
44	7	7
45	5	5
46	4	4
47	2	2
48	3	3
49	1	1
50	XWC0 + YRC0	
51	P15	

CONN B



32 KB CORE MEMORY BLOCK DIAGRAM



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PRINTED CIRCUIT BOARD ASSEMBLIES AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-607F01M01R02	.75 μSEC W/PAR
35-607F02M01R01	.75 μSEC W/O PAR
35-607F03M01R03	1.0 μSEC W/PAR
35-607F04M01R03	1.0 μSEC W/O PAR
35-607F05M01R03	1.0 μSEC W/PAR READ MODIFY WRITE
35-607F06M01R03	1.0 μSEC W/O PAR READ MODIFY WRITE

REVISIONS

PRE PRODUCTION / PROTOTYPE	INIT	DATE
	PROD	

RELEASED FOR PRODUCTION
ENG. [illegible] DATE 11/16/76

REVISIONS

REVISED SHT. 11				
WS	WV	3072	8-16-77	R01
REVISED SHT'S 11 & 18 AREA N7 35-607F01M01 THRU 35-607F06M01 WERE R00.				
PM	WV	3188	6-19-77	R02
REVISED SHT'S 10 & 11 & 18 AREA N7 35-607F01M01 THRU 35-607F06M01 WERE R02.				
PM	WV	3148	6-21-77	R03
REVISED SHTS 2 & 17				
35-607F01M01 — F06 M01 WAS R02				
PM	WV	3227	7-5-77	R04

SHEET INDEX

REV	4	1									1	3					1	2		
SHT. NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

NOTES

NAME	TITLE	DATE
W. LIMPERT	DRAFT	9/15/76
H. MATTER	CHK	9/15/76
P. OBRDA	ENGR	11-17-76
B. MULLER	TEST	11-17-76
S. MESSINA	MGR.	11-17-76

TITLE SCHEMATIC: ELECTRONICS BOARD (32KB MEMORY)

TASK NO. 03017
DWG NO. 35-607M01R04
SHEET OF 1-20

BRUNING 44-233 16042

REVISIONS

M	90	3627	7177	E01

BIT 16

BIT 15

A20 19-099 SENSE AMP

A21 19-099 SENSE AMP

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a) DIODES ARE 23-[illegible].
b) TRANSISTORS ARE [illegible].

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SCALE- | DRAWN | CHK'D | APP'D | DATE

TITLE SCHEMATIC ELECTRONICS BRD (32KB MEMORY)

SIZE 03017 | DWG NO 35-607 MINI01208 | REV 2 | SHEET 4 OF 20

REVISIONS

12N8 INHTA1

T2 30-028 Q27 P15

T17 30-027

D104 23-018

D16 23-034

D17

D18 23-034

R9 56 P5 1/2W

T.P ITMI

A1 19-057 5G

A6 19-100 D

T2 30-028 Q26 P15

T17 30-027

D15 23-034

T10 30-026 Q7

289 IRTTA

D14

D13 23-034

R38 4.7K

R37 4.7K

BIT 14

SA14 100-A IA14 98-A

SA14 99-A

D119

D120

RM 3 21-053

101-A

SB14 103-A IB14 104-A

SB14 102-A

D118

D117

R69 2.15K 1%

2K

A22 19-099 SENSE AMP

N5B J9

R173 1K

236-1 MD140

A105 19-134 TTL

2K7 DSA0

A38 19-063 SDF

A98 19-026 HPC

03 MS140 (203-1

DO61 11L8

T2 30-028 Q29 P15

T18 30-027

D22 23-034

D23

D24 23-034

R8 56 P5 1/2W

T2 30-028 Q28 P15

12N8 INHTB1

4C3 N22

D21 23-034

T10 30-026 Q8

N15

D20

D19 23-034

R40 4.7K

R39 4.7K

BIT 13

SA13 93-A IA13 91-A

SA13 92-A

D123

D124

RM 4 21-053

94-A

SB13 96-A IB13 97-A

SB13 95-A

D122

D121

R70 2.15K 1%

2K

A23 19-099 SENSE AMP

N5B J5, 10B5

10J4 VTH

SASA1 12N5

SASB1 12N6

R174 1K

136-1 MD130

A105 19-134 TTL

4K3 DSB0

A38 19-063 SDF

A98 19-026 HPC

06 MS130 (103-1

DCO 11R8

DS1 11L8

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a.) DIODES ARE 23-[illegible].
b.) TRANSISTORS ARE [illegible]-0-0.

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SCALE—

	NAME	TITLE	DATE
DRAWN			
CHK			

TITLE SCHEMATIC ELECTRONICS BRD (32KB MEMORY)

SIZE C 03017

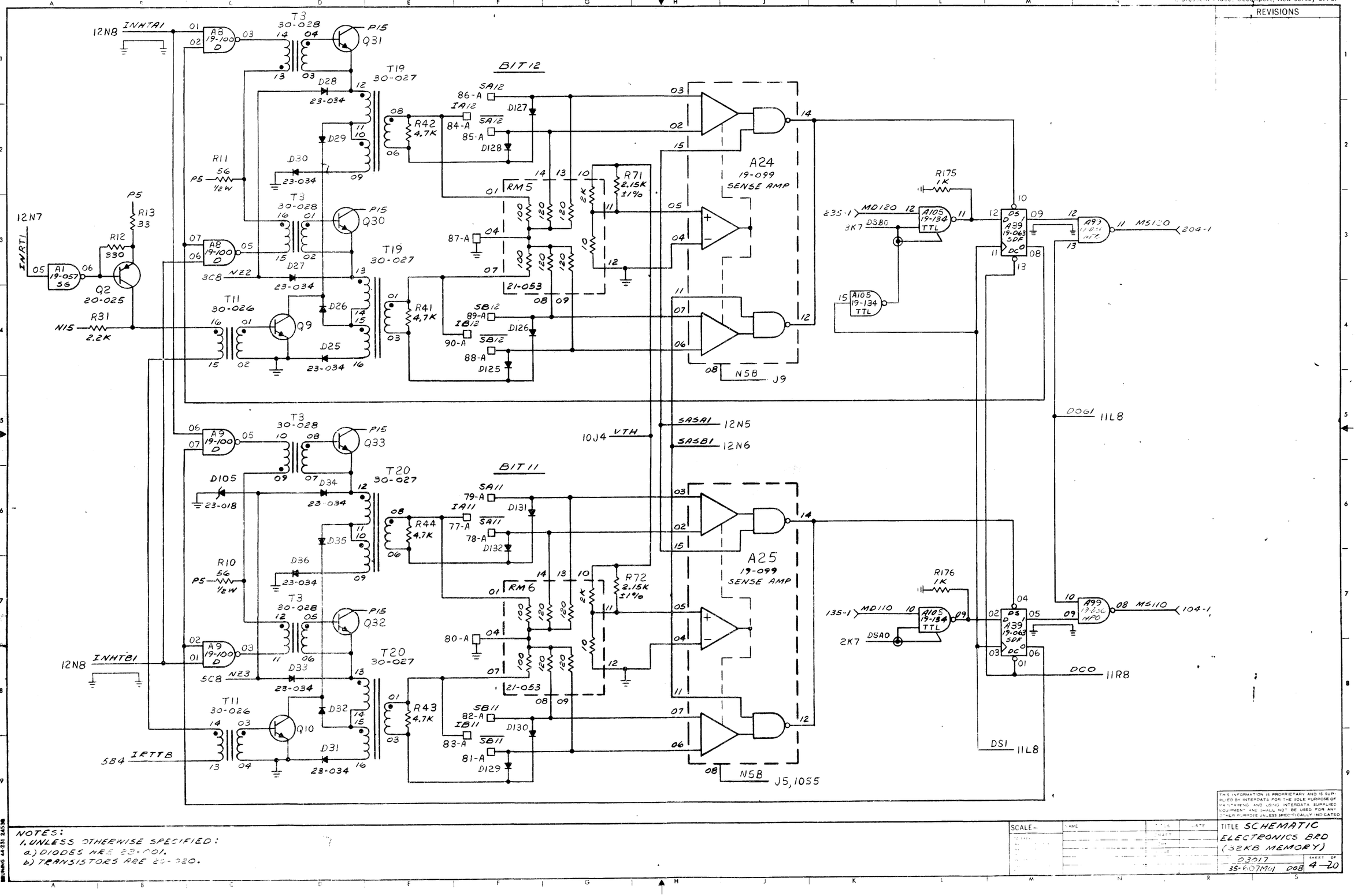
35-607M01 D08

SHEET 3 OF 20

BRUNING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) DIODES ARE 23-001.
   b) TRANSISTORS ARE 23-020.

BRUNING 44-231 24530

SCALE –

NAME	DATE
DRAWN	
CHECKED	
ENGR	
MFG	
QA	

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TITLE SCHEMATIC
ELECTRONICS BRD
(32KB MEMORY)

03017
35-607M01 008

SHEET OF 4 — 20

BIT 10

BIT 9

12N8 IA14 — A10 19-100 C — T4 30-028 — P15 Q35 — T21 30-027 — D40 23-034 — D41 — D42 23-034 — R15 56 1/2W P5

T4 30-028 — P15 Q34 — T21 30-027 — D39 23-034 — D38 — T11 30-026 — Q11 — D37 23-034 — 489 IRTTB

A10 19-100 D — 07 06 05

R46 4.7K — R45 4.7K

SA10 72-A — IA10 70-A — SA10 71-A — D135 — D136

SB10 75-A — IB10 76-A — SB10 74-A — D134 — D133

RM 7 — 21-053 — 100 — 120 — 2K — R73 2.15K 1%

73-A

A26 19-099 SENSE AMP

SASA1 12N5 — SASB1 12N6

N58 J9

R163 1K — 234-1 MD100 — A104 19-134 TTL — K7 DSCO

A440 19-063 SDF — A99 — MS100 205-1

DOG1 11L8

T4 30-028 — P16 Q37 — T22 30-027 — D46 23-034 — D47 — D48 23-034 — R14 56 1/2W P5

T4 30-028 — P15 Q36 — T22 30-027 — D45 23-034 — D44 — T11 30-026 — Q12 — D43 23-034 — N15

A11 19-100 D — 12N8 INHTB1 — 4C8 N23

10J4 VTH

R48 4.7K — R47 4.7K

SA9 65-A — IA9 63-A — SA9 64-A — D139 — D140

SB9 68-A — IB9 69-A — SB9 67-A — D138 — D137

RM 8 — 21-053 — 100 — 120 — 2K — R74 2.15K 1%

66-A

A27 19-099 SENSE AMP

N5B J5, 1055

R164 1K — 134-1 MD090 — A104 19-134 TTL — K3, 6K3, 7K7 DSCO

A440 19-063 SDF — A99 — MS090 105-1

OCO 11R8

DS1 11L8

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a) DIODES ARE 23-001.
b) TRANSISTORS ARE 20-020.

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SCALE — | NAME | TITLE | DATE | DRAFT | CHK | ENGR

TITLE SCHEMATIC ELECTRONICS BRD (32KB MEMORY)

DWG NO 03017 — SHEET 5 OF 20

SIZE — DWG NO 35-607M01 008

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

BIT 8

BIT 7

A28
19-099
SENSE AMP

A29
19-099
SENSE AMP

12N8 INRT1 01 A2 19-057 56 02 Q3 20-025 R19 330 R18 33 P5 R32 N15 2.2K Q13 D53 23-034 T23 30-027 D52 D54 23-034 T12 30-026 T5 30-028 Q39 N15 D49 23-034 D50 D51 23-034 T5 30-028 Q38 N15 R17 56 1/2W P5 R50 4.7K R49 4.7K R75 2.15K ±1% R76 2.15K ±1% RM9 RM10 21-053 21-063 58-A 56-A 57-A 59-A 61-A 62-A 60-A D143 D144 D142 D141 5A8 IA8 5B8 IB8 N5A J9

12N7 INHT1 01 A12 19-100 D 02 03 06 07 A13 19-100 D 05

D106 23-018 P21 7C2 T12 30-026 Q14 D59 23-034 T24 30-027 7B1 IRTTC D58 D60 23-034 T5 30-028 Q41 N18 D55 23-034 D56 D57 23-034 T5 30-028 Q40 N18 R16 56 1/2W P5 R52 4.7K R51 4.7K RM10 21-063 51-A 49-A 50-A 52-A 55-A 53-A D147 D148 D146 D145 5A7 IA7 5B7 IB7 N5A J5, 10J4

10J4 VTH 5A5A1 12N5 5A5B1 12N6

R165 1K 233-1 MD080 06 A104 19-134 TTL 07 5K7 DSC0 A41 19-063 SDF DS 10 09 DC 08 11 13 12 A100 11 MS080 206-1 D061 11L8

R166 1K 133-1 MD070 14 A104 19-134 TTL 13 7K3 DSD0 A41 19-063 SDF DS 04 05 DC 06 01 10 A100 08 MS070 106-1 D00 11R8 DS1 11L8

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a) DIODES ARE 23-001.
b) TRANSISTORS ARE 20-020.

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY

SCALE–

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

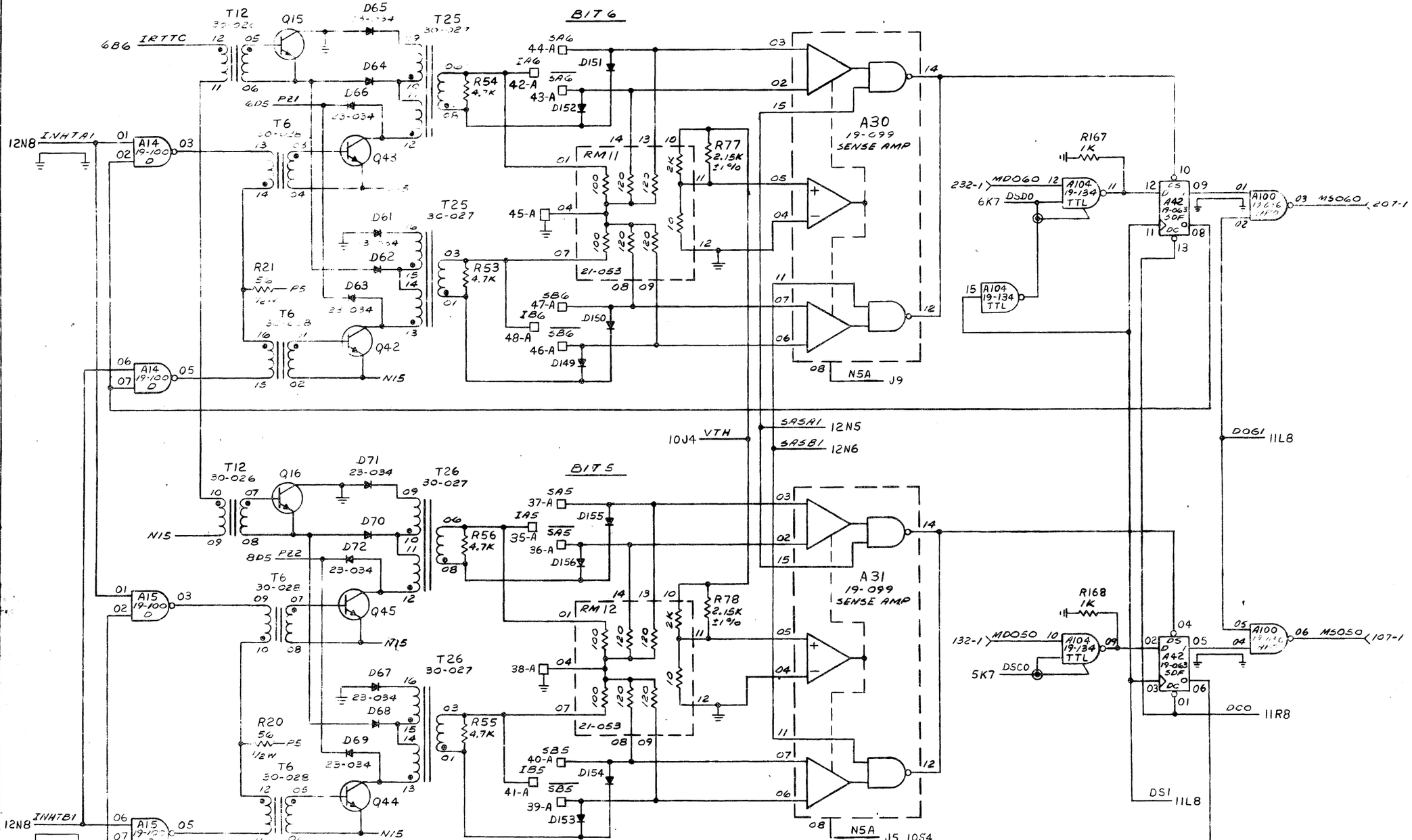
TITLE SCHEMATIC ELECTRONICS (32KB MEMORY)

TASK NO. 03017
DWG NO. 35-607

INTERDATA

Port Washington, New Jersey 07757

REVISIONS



NOTES:
1. UNLESS OTHERWISE [illegible]
a.) DIODES ARE [illegible]
c.) TRANS. STD. [illegible]

INFORMATION IS PROPRIETARY AND IS SUPPLIED FOR USE BY THE SOLE PURPOSE OF INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

SCALE –	DRAWN	DATE	TITLE SCHEMATIC, ELECTRONICS BRD. (32KB MEMORY)
			C3-17
			33-607M01 P08
			SHEET 20 7-20

BRUNING 44231 24538

BIT 4

BIT 3

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
2. DIODES ARE 3-[illegible]
3. TRANSISTORS ARE [illegible]

THIS INFORMATION PROPRIETARY AND IS SUPPLIED SOLELY INTERDATA FOR THE SOLE PURPOSE OF MAINTENANCE AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

SCALE— | NAME | SIZE | DATE

TITLE SCHEMATIC
ELECTRONICS BRD.
(32KB MEMORY)

SHEET 8 OF 20

DRAWING 44-231 24538

BIT 2

T13 30-026 Q19 — D89 23-034 — T29 30-027
8B6 IRTTD — 12 05 — 09 — D88 — 10 11 — 06 11 — 08
D90 23-034 — T8 30-028 — Q51 — N15
12N8 INHTA1 — A18 19-100 D — 01 02 03 — 13 03 — 14 04
D85 23-034 — D86 — T29 30-027 — 16 — 08
R28 56 PS 1/2W — D87 23-034 — T8 30-028 — Q50 — N15
06 07 A18 19-100 D 05 — 16 01 — 15 02
D108 23-018 — PZ3 10C6

T13 30-026 Q20 — D95 23-034 — T30 30-027
10B8 IRTTE — 10 07 — 09 08 — D94 — D96 23-034 — 06 — R64 4.7K — 08
01 A19 19-100 D 03 — T8 30-028 — 09 07 — 10 08 — Q53 — N15
D91 23-034 — D92 — T30 30-027 — 16 — 03
R27 56 PS 1/2W — D93 23-034 — T8 30-028 — Q52 — N15
12N8 INHTB1 — 06 07 A19 19-100 D 05 — 12 05 — 11 06
R63 4.7K — 01

IA2 14-A — 5A2 15-A — D167 D168
IB2 20-A — 5B2 18-A — D166 D165 — 5B2 19-A
IA1 07-A — 5A1 08-A — D171 D172
IB1 13-A — 5B1 11-A — D170 D169 — 5B1 12-A
17-A — 5A2 16-A — 10-A — 5A1 09-A

RM15 — 01 — 14 13 10 — 100 120 120 — 21-053 — 08 09 — 07 04
RM16 — 01 — 14 13 10 — 100 120 120 — 21-053 — 08 09 — 07 04
R81 2.15K ±1% — R82 2.15K ±1% — 2K 10 — 11 12

A34 19-099 SENSE AMP — 03 02 15 — 05 04 — 11 07 06 — 14 12 — 08 N5A J9
A35 19-099 SENSE AMP — 03 02 15 — 05 04 — 11 07 06 — 14 12 — 08 N5A J5, 10S4

10J4 VTH
5A5A1 12N5
5A5B1 12N6

R160 1K — 230-1 MD020 — A103 19-134 TTL — 06 07 — 8K7 DSE0
R161 1K — 130-1 MD010 — A103 19-134 TTL — 14 13 — 10K7 DSF0
A103 19-134 TTL — 15 — DSI 11L8

A44 19-063 SDF — D0 D1 D2 D3 DC — 10 09 08 13 — 04 05 06 01
A101 19-036 NPO — 12 01 02 — 03 M5020 — 209-1
A101 19-036 NPO — 05 04 — 06 M5010 — 109-1
D0G1 11L8
DCO 11R8

NOTES:
1. UNLESS OTHERWISE SPECIFIED.
2) DIODES ARE 23-001.
3) TRANSISTORS ARE 21-001.

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SCALE — | TOLERANCE | TIME | TITLE | DATE
TITLE SCHEMATIC ELECTRONICS BRD. (32KB MEMORY)
SIZE D | 35-601M01 008 | SHEET OF 9-20

BRUNING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
AREA L5 A70 PIN1, 13 WAS 17.			
P4	37	3148	6-21-77

128-1 TEMP A — R157 330 — R156 2.2K — RT2 23-012 — TEMP B 227-1

C97 0.10UF, C21 0.1UF, + C1 15 UF

T. P. VTHM

P5 03 02 R181 500 01 — TP5 TP4 — GND T.P. 6

VTH — 2G5, 3G5, 4G5, 5G5, 6G5, 7G5, 8G5, 9G5

P5 R107 39 1/2W 04 — T52 30-028 — 13 14 — Q61 — N15

11G3 T3 01 READO 02 — A70 19-137 D — 03 03

R108 50 2W — D183 23-002 5.1V — N5A J9, 6J9, 7J9, 8J9, 9J9

R109 50 2W — D184 23-002 5.1V — N5B 2J9, 3J9, 4J9, 5J9

N5 REGULATOR

12N8 INHTAI — A3 19-100 D — T9 30-028 — N15 Q55 — T31 30-027

9D5 PZ3 — D102 23-034 — D100 — D101 23-034 — R29 56 P5 1/2W

BIT 0

SA0 02-A — IA0 00-A — SA0 01-A — DI75 — DI76

R66 4.7K — R65 4.7K

SB0 05-A — IB0 06-A — SB0 04-A — DI73 — DI74

RM17 01 — 100 120 120 2K R83 2.15K ±1% 10 — 03-A 04 — 07 — 21-053 08 09

SASA1 12N5 — SASB1 12N6

A36 19-099 SENSE AMP — 03 02 15 05 04 11 07 06 — 14 12 — 08 N5A 54

12N8 INHTBI — A3 19-100 D — T9 30-028 — N15 Q54 — T31 30-027

23-034 — D98 — D97 23-034 — T14 30-026 — 9B6 IRTTE — N15 — Q21

R162 1K — 229-1 MD000 — 9K7 DSF0 — A103 19-134 TTL — A45 19-063 SDF — DS D DC

DOG1 11L8 — A102 19-036 HPO — MS000 210-1

DCO 11R8

DSI 11L8

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NOTES:
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   b) TRANSISTORS ARE 20-020.

SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC ELECTRONICS BRD (32KB MEMORY)
TASK NO 03017
DWG NO 35-607M01R/D08
SHEET 10 OF 20

BRUNING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
AREA D2: A87-05,06 PIN NUMBERS WERE REVERSED. WS WJ 3072 8-16-77 R01
AREA A7, T15 K4 WAS T14 N.C. AREA K4, T14 N.C. WAS A7 ALSO, ADDED A7 TO T15. FM JV 3188 6-19-77 R02
AREA N8, T7 WAS T5. AREA G8 & H4, T1 N.C. WAS T1 10K5, ADDED 10K5 TO T3, T5 N.C. WAS T3 M8, T3 M8 WAS T7 N.C. FM JV 3148 6-21-77 R03
AREA G3, 12K8 WAS REMOVED FROM A80-06 GP JV 3407 12-8-77 R04

W/O PARITY (F02, F04 & F06)
W/ PARITY (F01, F03 & F05)
R138 470 P5
PAR0 105-0
MB20 235-0
MCO
SRCI
XMA15 0 108-0 L2 L1 L3
XMA14 0 208-0 M2 M1 M3
MA000 106-0 N2 N1 N3
A96 19-127 XORS
A88 19-060 SG
A89 19-130 SB
A87 19-063 SDF
BS0 MB1
SELECT JUMPER AT TEST
TYPICAL CONNECTION
R146 180
R147 270
A90 30-041 DELAY LINE
ER0 204-0
12A1 MB0
T12 .75 u SEC (F01 & F02)
1.0 u SEC (F03 & F04)
T18
1.0 u SEC (F05 & F06)
T22
A91 19-126
J4 T12
L7 SCL1
M4 T22
RT0 12E1
RT1 12F4
R145 470 P5
A80 A79 A78 A75 A74 A73
19-131 SDF
CLK ID CLR
T1 T3 T5 T7 T9 T11 T13 T15 T17 T19 T21 T23
M8 N.C. N.C.O C6, 10K5 N.C.O N.C. N.C.O M8,0 C9 N.C.O H8 12G8 N.C.O N.C. N.C.O A7, 12G9 G9 C6 A7 N.C.O A8 N.C.O L6 N.C.O G8
T2 T4 T6 T8 T10 T12 T14 T16 T18 T20 T22 T24
N.C. 12G9 12K7 N.C. 12G9 12K7 N.C. A4, J8, D4 N.C. N.C. G7 G8 D4 N.C. N.C. A8, D4 N.C. G9
WT0 12E1
G4 T3 T17 A69 19-060 SG
L4 WT1 12F5
A82 19-057 SG
K4 T17 T15 A81 19-126 CHT0 17F8
M4 T19 T22
A76 19-124 SB
READ0 10K5, 13A4, 17C4
WRITE0 12K5, 14A4 17C4
N7 MCO
R129 470 P5
A102 19-036 HPO
127-1 WRT0
J4 T9
R128 470 P5
CWM1
RRM1
R185 470 P5
R184 470 P5
12K5
SEE NOTE 2
E2 E1
E4 E3
R8 DCO
R127 470 P5
R126 470 P5
SCL1 A4
M4 T21
A65 19-126 MCO C8
K5 T16 N.C.
A97 19-036 HPO DUA0 135-0
DISABLE DUA0
12K7, 17A1 SCL0
K4 T16 N4 T23 J4 T11 M4 T24 K4 T15
A64 19-130 SB
A69 19-060 SG
DS1 2M9, 3M9, 4M9, 5M9, 6M9, 7M9, 8M9, 9M9, 10M9
R98 150
DOG1 2N5, 3N5, 4N5, 5N5, 6N5, 7N5, 8N5, 9N5, 10N6
R125 150
H4 T7 G4 T1
DC0 G7, 2N8, 3N8, 4N8, 5N8, 6N8, 7N8, 8N8, 9N8, 10N8

MEMORY TIMING

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) DIODES ARE 23-001.
   b) TRANSISTORS ARE 20-020.
2. FOR F05 & F06 CUT PATHS E1-E2, E3-E4, E5-E6, E7-E8 & ADD JUMPER WIRES "Z TO V" & "Y TO W"

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SCALE— | NAME | TITLE | DATE
DRAFT | CHK | ENGR

TITLE SCHEMATIC ELECTRONICS BOARD (32KB MEMORY)
TASK NO. 03017
DWG NO. 3-607M01P04D08
SHEET OF 11 —20

REVISIONS

AREA K7, A66-05 WAS CONNECTED TO 11G4 T3.			
GP	AV	3407	12-8-77 R01

11A4 MB0

109-0 MA020 — A93 19-065 2:1 MUX (SEL, ENB) — 110-0 MA030, 210-0 MA040, 129-0 MA050

A93: 1B→1Y, 2B→2Y, 4B→4Y, 3B→3Y; 1A→A2, 2A→A3, 4A→A4, 3A→A5

11D5 RT0, 11E6 WT0 → A60 19-055 SG → 11

11 → A84 19-055 SG → XSTA0 14A5

A2 14A5; A3 → A85 19-057 SG → $\overline{A3}$

$\overline{A3}$ → A84 19-055 SG → XSTB0 14H5

A4 13A5; A5 13A5

A5 → A84 19-055 SG → YSTA0 13A5

A6 → A84 19-055 SG → YSTB0 13H5

229-0 MA060 — A94 19-065 2:1 MUX (SEL, ENB) — 130-0 MA070, 230-0 MA080, 131-0 MA090

A94: 1B→1Y, 2B→2Y, 4B→4Y, 3B→3Y; A6 → A85 19-057 SG → $\overline{A6}$

A7 15B7, 16B7; A8 15B7, 16B7; A9 15B8, 16B8

11D5 RT1 → A58 19-055 SG → RXDTA0 15B4

A59 19-055 SG → RXDTB0 16B4

11F7 WT1 → A58 19-055 SG → WXDTA0 15B5

A59 19-055 SG → WXDTB0 16B5

231-0 MA100 — A95 19-065 2:1 MUX (SEL, ENB) — 132-0 MA110, 232-0 MA120, 133-0 MA130

A95: 1B→1Y, 2B→2Y, 4B→4Y, 3B→3Y; A10 → A85 19-057 SG → $\overline{A10}$

A10; A11 15B6, 16B6; A12 15B6, 16B6; A13 15B6, 16B6

233-0 MA140 — A92 19-065 2:1 MUX (SEL, ENB) — 107-0 MA010

A92: 1B→1Y, 2B→2Y, 4B→4Y, 3B→3Y; A14 → A85 19-057 SG → $\overline{A1}$

A14 14A5; A1

12 N.C., 14 N.C., 09 N.C., 11 N.C.

$\overline{A1}$ → P3; A1 → P2

A59 19-055 SG → RYDTB0 16B7

A58 19-055 SG → RYDTA0 15B7

A58 19-055 SG → WYDTB0 16B5

A59 19-055 SG → WYDTA0 15B5

11J4 $\overline{T11}$ → A60 19-055 SG → YRTO 17C4

K3, 11G4 T4 → XRTO 17J4

11G4 $\overline{T6}$, K8, 11K4 T15 → A60 19-055 SG → XWTO+YWTO 17C4

G9 T4 → A82 19-057 SG → R151 470, R155 500, R152 825 1%, R150 470, C91 68 PF 1%, R153 825 1%, R154 68 ½ W, P5

C92 150 PF 1%; Q63 20-001; Q62 20-001

SAT1

11F9 RRM1, 11F8 WRITE0 → A68 19-060 SG → A63 19-130 SB → SASA1 2H5, 3H5, 4H5, 5H5, 6H5, 7H5, 8H5, 9H5, 10H5; T.P. SASA1; R84 150

A68 19-060 SG → A63 19-130 SB → SASB1 2H5, 3H5, 4H5, 5H5, 6H5, 7H5, 8H5, 9H5, 10H5; R85 150

11G4 T8, 11G4 $\overline{T4}$ SCL0, 11G8 → A67 19-060 SG → A62 19-130 SB → INRT1 2A3, 4A3, 6A1, 8A1; R7 150

A1, G9 T15, $\overline{A1}$ → A66 19-060 SG → A61 19-130 SB → INHTA1 2B1, 3B1, 4B1, 5B1, 6A2, 7A2, 8A2, 9A2, 10A5, 17A1; R2 150

A66 19-060 SG → A61 19-130 SB → INHTB1 2B8, 3B8, 4B8, 5B8, 6A9, 7A9, 8A9, 9A9, 10A8, 17B1; R1 150

ADDRESS LATCHES & MEMORY TIMING

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   b) TRANSISTORS ARE 20-0[illegible]

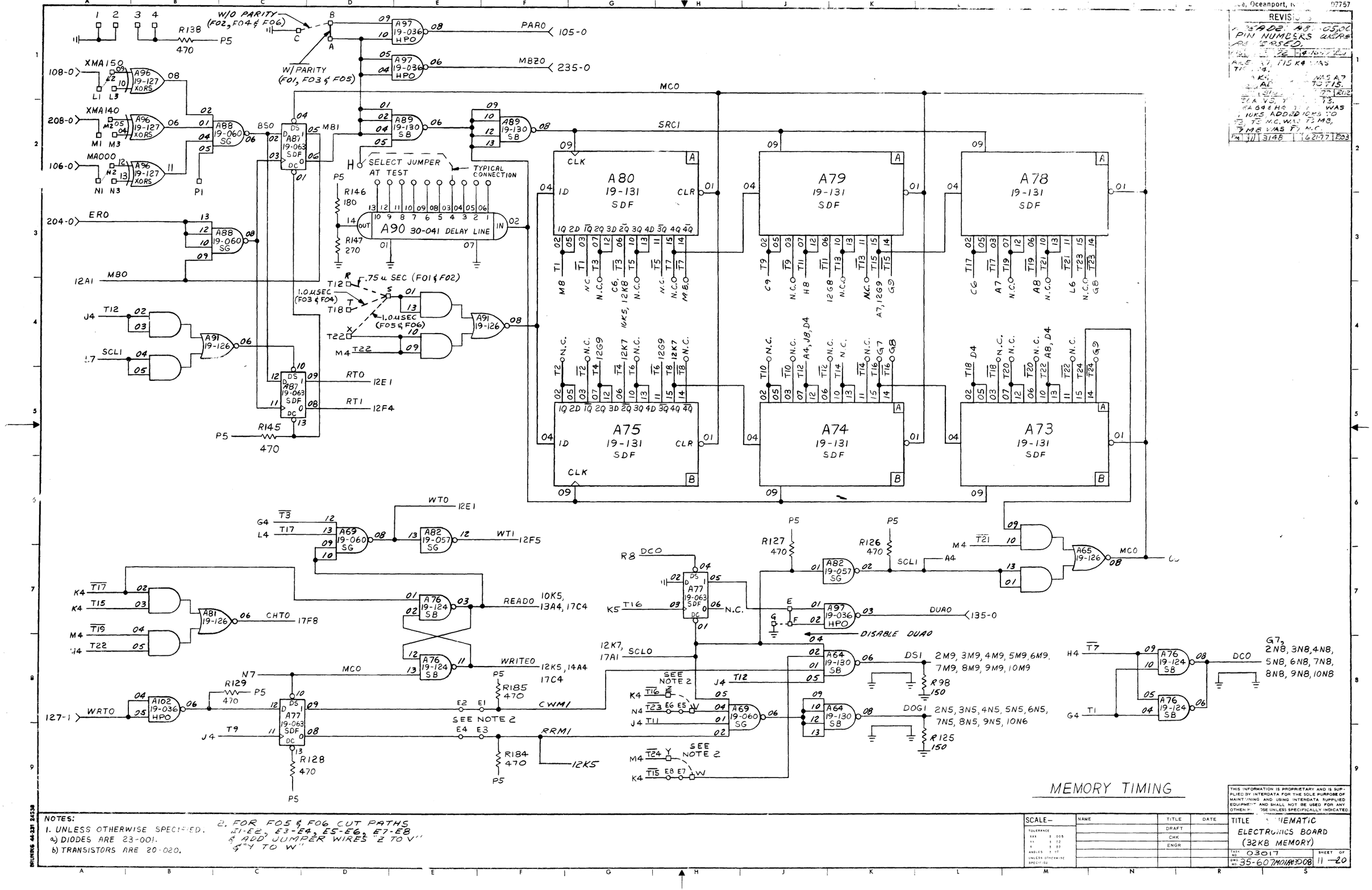
SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC ELECTRONICS BOARD (32KB MEMORY)

TASK NO. 03017 — SHEET OF 12—20

DWG NO. 35-607M01R01 D08

BRUNING 44-231 24538



MEMORY TIMING

NOTES:
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   b) TRANSISTORS ARE 20-020.
2. FOR F05 & F06 CUT PATHS E1-E2, E3-E4, E5-E6, E7-E8 & ADD JUMPER WIRES "Z TO V" & "Y TO W"

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	NAME	TITLE	DATE
SCALE–		DRAFT	
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		CHK	
		ENGR	

TITLE SCHEMATIC ELECTRONICS BOARD (32K8 MEMORY)
TASK NO. 03017
DWG NO. 35-607MOMAB008
SHEET OF 11 – 20

BRUNING 44-237 24238

REVISIONS

A93 19-065 2:1 MUX — MA020 (109-0), MA030 (110-0), MA040 (210-0), MA050 (129-0), MBO (11A4) → A2, A3, A4, A5

A94 19-065 2:1 MUX — MA060 (229-0), MA070 (130-0), MA080 (230-0), MA090 (131-0) → A6, A7, A8, A9

A95 19-065 2:1 MUX — MA100 (231-0), MA110 (132-0), MA120 (232-0), MA130 (133-0) → A10, A11, A12, A13

A92 19-065 2:1 MUX — MA140 (233-0), MA010 (107-0) → A14, A1

A85 19-057 SG: A2 → A2; A3 → A3; A5 → A5; A6 → A6; A10 → A10; A1 → A1

A84 19-055 SG: A2 + A5 → XSTA0 (14A5); A3 + A5 → XSTB0 (14H5); A4 + A5 → YSTA0 (13A5); A6 + A5 → YSTB0 (13H5)

A85 19-057 SG: A7 → A7 (15B7, 16B7); A11 → A11 (15B6, 16B6); A12 → A12 (15B6, 16B6); A13 → A13 (15B6, 16B6)

A85 19-057 SG: A14 → A14 (14A5); A1 → A1; N.C.; N.C.; P2; P3

RTO (11D5) + WTO (11E6) → A60 19-055 SG

RTI (11D5) + WTI (11F7) → A58 19-055 SG: RXDTA0 (15B4); A59 19-055 SG: RXDTB0 (16B4); A58 19-055 SG: WXDTA0 (15B5); A59 19-055 SG: WXDTB0 (16B5)

A58 19-055 SG: RYDTB0 (16B7); A59 19-055 SG: RYDTA0 (15B7); A58 19-055 SG: WYDTB0 (16B5); A59 19-055 SG: WYDTA0 (15B5)

T11 (11J4) + T4 (K3, 11G4) + T6 (11G4) + T15 (K8, 11K4) → A60 19-055 SG: YRT0 (17C4); A60 19-055 SG: XRT0 (17J4); A60 19-055 SG: XWT0 + YWT0 (17C4)

G9 T4 → A82 19-057 SG

P5: R151 470; R155 500; R150 470; R153 825 1%; R154 68 1/2 W; R152 825 1%; C91 68 PF 1%; C92 150 PF 1%; Q63 20-001; Q62 20-001

SAT1

RRMI (11F9) + WRITE0 (11F8) → A68 19-060 SG → A63 19-130 SB → SASA1 (T.P.) (2H5, 3H5, 4H5, 5H5, 6H5, 7H5, 8H5, 9H5, 10H5); R84 150

A68 19-060 SG → A63 19-130 SB → SASB1 (2H5, 3H5, 4H5, 5H5, 6H5, 7H5, 8H5, 9H5, 10H5); R85 150

T8 (11G4) + T4 (11G4) + SCL0 (11G8) → A67 19-060 SG → A62 19-130 SB → INRT1 (2A3, 4A3, 6A1, 8A1); R7 150

A1 + G9 + T15 (11G4) + T3 (11G4) → A66 19-060 SG → A61 19-130 SB → INHTA1 (2B1, 3B1, 4B1, 5B1, 6A2, 7A2, 8A2, 9A2, 10A5, 17A1); R2 150

A1 → A66 19-060 SG → A61 19-130 SB → INHTB1 (2B8, 3B8, 4B8, 5B8, 6A9, 7A9, 8A9, 9A9, 10A8, 17B1); R1 150

ADDRESS LATCHES & MEMORY TIMING

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SCALE—

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

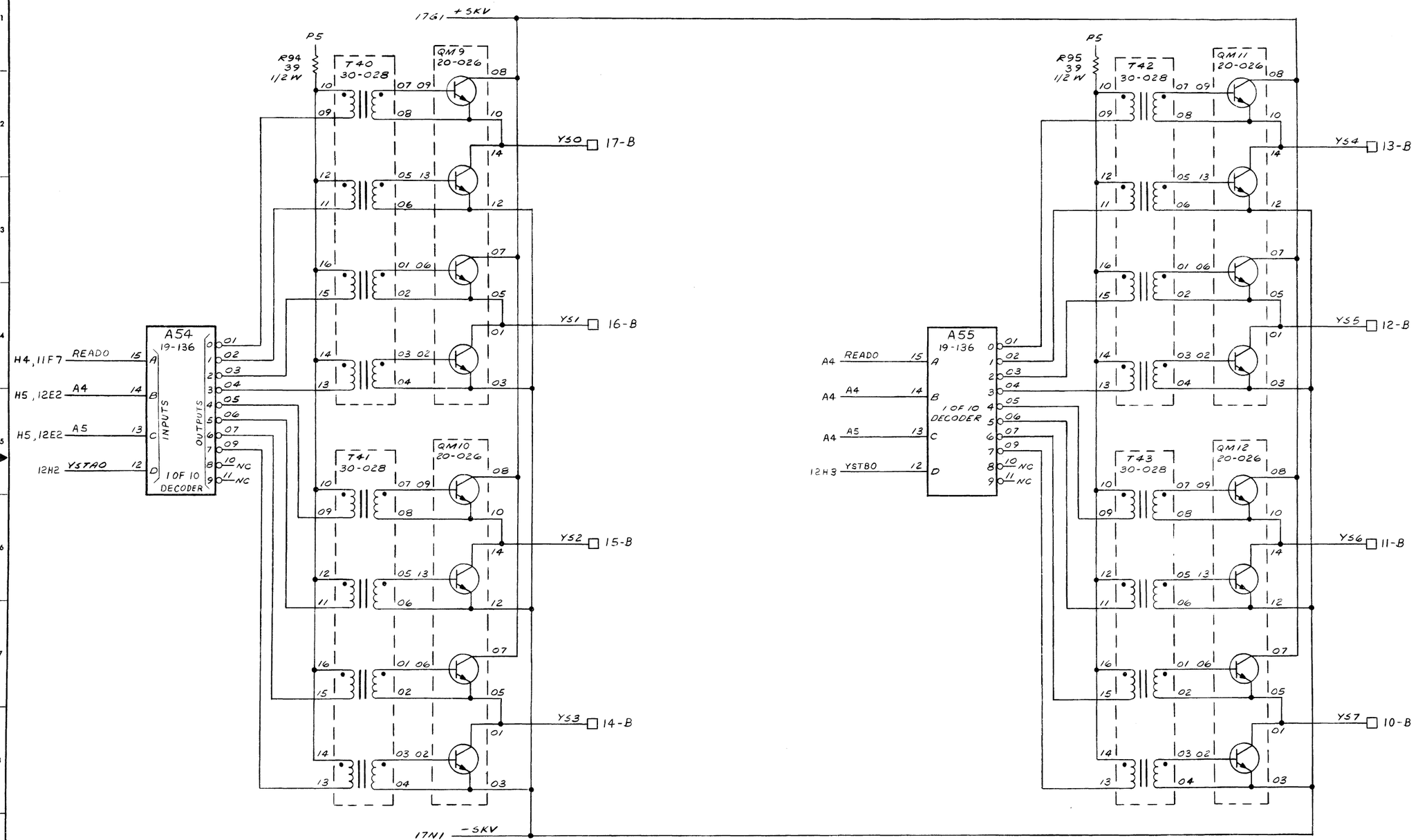
TITLE SCHEMATIC
ELECTRONICS BOARD
(32KB MEMORY)

TASK NO. 03017
DWG NO. 35-607M01 D08
SHEET OF 12—20

BRUNING 44-231 24538

INTERDATA®

REVISIONS



Y SINK

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCT. SCHEMATIC
ELECTRONICS BOARD
(32 KB MEMORY)

TASK NO. C 3017
DWG NO. 35-607M01 D08
SHEET OF 13-20

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

BRUNING 44-231 16042

INTERDATA®

REVISIONS

17G1 +5KV

P5

R96 39 1/2 W

T44 30-028

QM13 20-026

T45 30-028

QM14 20-026

R97 39 1/2 W

T46 30-028

QM15 20-026

T47 30-028

QM16 20-026

A56 19-136

A57 19-136

1 OF 10 DECODER

H4, 11F8 WRITEO 15 A

H5, 12E6 A14 14 B

H5, 12E1 A2 13 C

12H1 XSTA0 12 D

A4 WRITEO 15 A

A5 A14 14 B

A5 A2 13 C

12H2 XSTB0 12 D

0 1 2 3 4 5 6 7 8 9

01 02 03 04 05 06 07 09 10 NC 11 NC

X50 09-B

X51 08-B

X52 07-B

X53 06-B

X54 05-B

X55 04-B

X56 03-B

X57 02-B

17N1 −5KV

X SINK

NOTES

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF USE BY INTERDATA EMPLOYEES EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

NAME | DATE | TITLE FUNCT. SCHEMATIC ELECTRONICS BOARD (32 KB MEMORY)

DRAWN | CHK | ENG | MFG

SIZE D 70177 | SHEET OF 14-20

35-607M01 008

(DRUMING 64-33-16842)

INTERDATA®

P5

R88 56 1/2W

R89 56 1/2W

R86 56 1/2W

R87 56 1/2W

12H4 RXDTA0

12H8 WYDTA0

12E5 A11

12E5 A12

12E5 A13

12H7 RYDTA0

12E3 A7

12E3 A8

12E4 A9

12H5 WXDTA0

A48 19-136 1 OF 10 DECODER

A49 19-136 1 OF 10 DECODER

A47 19-136 1 OF 10 DECODER

A46 19-136 1 OF 10 DECODER

T34 30-028

T35 30-028

T32 30-028

T33 30-028

QM3 20-026

QM4 20-026

QM1 20-026

QM2 20-026

XRA0+YWA0 → 34-B

XRA1+YWA1 → 33-B

XRA2+YWA2 → 31-B

XRA3+YWA3 → 32-B

XRA4+YWA4 → 30-B

XRA5+YWA5 → 29-B

XRA6+YWA6 → 27-B

XRCS1+YWCS1 → 17L1

XRA7+YWA7 → 28-B

XWC0+YRC0 → 50-B

XWC1+YRC1 → 49-B

XWC2+YRC2 → 47-B

XWC3+YRC3 → 48-B

XWC4+YRC4 → 46-B

XWC5+YRC5 → 45-B

XWC6+YRC6 → 43-B

XWC7+YRC7 → 44-B

YRCS0+XWCS0 → 17E1

X/Y DRIVE

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NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCT. SCHEMATIC ELECTRONICS BRD. (32KB MEMORY)

TASK NO. 03017

DWG NO. 35-607M01 D08

SHEET 15 OF 20

DRAWING 44-231 18042

INTERDATA®

P5

R93 56 1/2W

R91 56 1/2W

R92 56 1/2W

R90 56 1/2W

A52 19-136 1 OF 10 DECODER

A53 19-136 1 OF 10 DECODER

A51 19-136 1 OF 10 DECODER

A50 19-136 1 OF 10 DECODER

12H4 RXDTB0

12H7 WYDTB0

12E5 A11

12E5 A12

12E5 A13

12116 RYDTB0

12E3 A7

12C3 A8

12E4 A9

12H5 WXDTB0

QM7 20-026 — T38 30-028

QM8 20-026 — T35 30-028

QM5 — T36

QM6 20-026 — T37 30-028

xEA8+YWA8 — 26-B

xEA9+YWA9 — 25-B

xEA10+YWA10 — 23-B

xEA11+YWA11 — 24-B

xEA12+YWA12 — 22-B

xEA13+YWA13 — 21-B

xEA14+YWA14 — 19-B

xEC31+YWC31 — 17L1

xEA15+YWA15 — 20-B

xWC8+YEC8 — 42-B

xWC9+YEC9 — 41-B

xWC10+YEC10 — 39-B

xWC11+YEC11 — 40-B

xWC12+YEC12 — 38-B

xWC13+YEC13 — 37-B

xWC14+YEC14 — 35-B

xWC15+YEC15 — 36-B

YEC50+XWC50 — 17E1

X/Y DRIVE

NOTES

TITLE FUNCT. SCHEMATIC ELECTRONICS BRD. (2KB MEMORY)

03017
35-607M01 D08

SHEET 16 OF 20

DRAWING 44 231 16042

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
ADDED KB CHARGE CIRCUIT WAS CHARGE CIRCUIT L.O.D FOR 35-607 F01 AND F02 ONLY				
C.F.	3227	7-1-77	R01
ADDED NOTE 2			
C.F.	3366	11-15-77	R02

SYSTEM CLEAR

BIAS SOURCE

X-Y CURRENT SOURCE

CHARGE CIRCUIT

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) DIODES ARE 23-001.
   b) TRANSISTORS ARE 20-020.
2. THERMISTOR "RT1" (23-012) IS REQUIRED WITH 35-517 F01 CORE STACK ONLY.

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SCALE—
TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

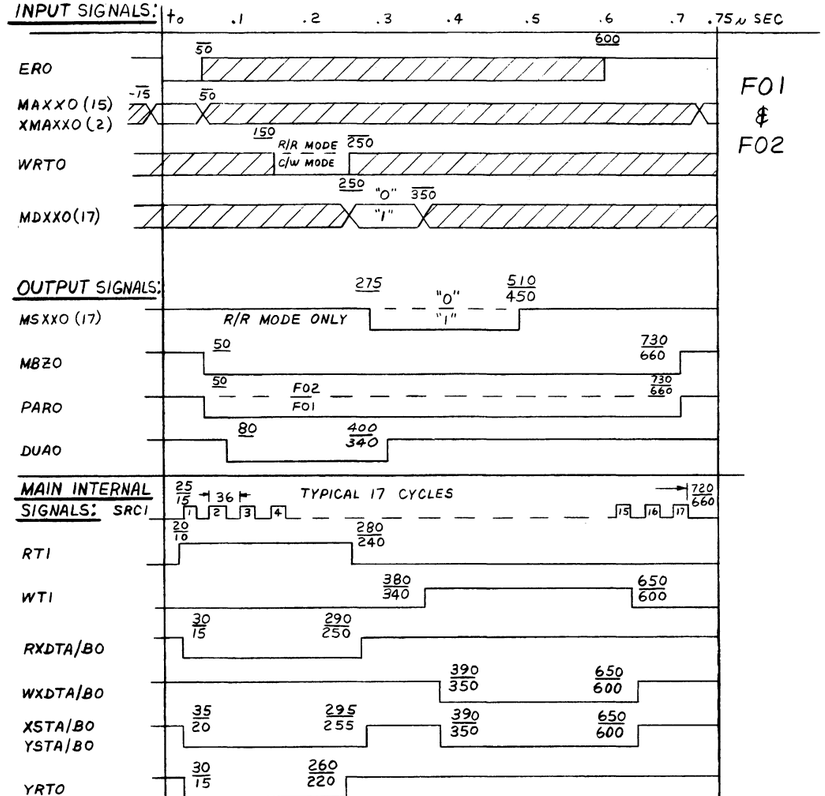
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE SCHEMATIC
ELECTRONICS BOARD
(32 KB MEMORY)

TASK NO. 03017 | SHEET OF 17—20
DWG NO. 35-607 MOI F02 D08

DRAWING 44-237 2553B

INPUT SIGNALS:

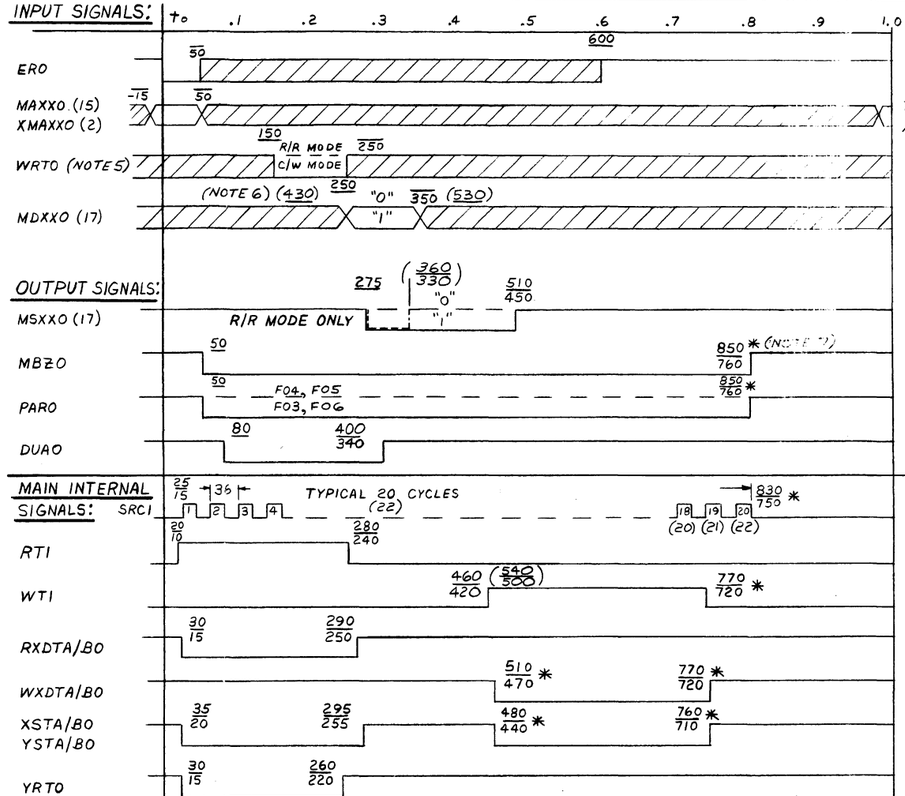


F01 & F02

OUTPUT SIGNALS:

MAIN INTERNAL SIGNALS: SRCI

INPUT SIGNALS:



F03 THRU F06

OUTPUT SIGNALS:

MAIN INTERNAL SIGNALS: SRCI

REVISIONS			
AREA J7, 340/300 WAS 320/280			
PM	JH	3188	6-19-77 R01
AREA H8, 180/140 WAS 140/100			
PM	JH	3148	6-22-77 R02
AT AREA G6 SIGNAL INHTI WAS 480-720 430-670			
AREA G6 SIGNAL INHTI WAS 360-600 310-550			
GP	JH	3407	12-8-77 R03

NOTES:
1. SHADED AREA (////) INDICATES "CAN CHANGE" OR "DO NOT CARE" INTERVAL.
2. UNLESS OTHERWISE INDICATED TIME IS IN NANOSECONDS.
3. THE NUMBER ABOVE THE LINE INDICATES MAXIMUM TIME; BELOW THE LINE IS MINIMUM.
4. ALL SIGNALS ARE OF STANDARD TTL LEVELS & TIMING IS REFERENCED TO 1.5V.
5. NOT APPLICABLE TO F05 & F06.
6. REFERENCES IN BRACKETS ARE APPLICABLE TO F05 & F06 ONLY.
7. REFERENCES DESIGNATED WITH * ADD 80 NANOSECONDS FOR F05 & F06 ONLY.

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SCALE–

TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE SCHEMATIC
ELECTRONICS BOARD
(32KB MEMORY)

TASK NO 03017
SYS NO 35-607M01R03D08
SHEET 18 OF 20

BRUNNING 44-239 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
AREA K3 CHARGE CIRCUIT WAS CHARGE CIRCUIT REQ'D FOR 35:607 FCN AND FOR ONLY				
	JJV	3227	7-1-77	R01

11G8 SCLO
12N8 INHTAI
12N9 INHTBI
QM1B 20-026
R114 820
R115 150
R116 150
P5
R124 470
SCLRO
126-0
D191
D190
D189
R123 680
R122 4.7K
R119 100 ½W
R112 180
R110 56 ½W
T49 30-028
QM17 20-026
Q57
R113 180
R120 56 ½W
T49 30-028
QM17 20-026
Q56
R118 180
R111 68 ½W
T49 30-028
QM17 20-026
Q59
R117 180
R121 56 ½W
T49 30-028
QM17 20-026
Q58
SYSTEM CLEAR
12H8 YRTO
11F7 READO
12J9 XWTO + YWTO
11F8 WRITEO
A71 19-137 D
A72 19-137 D
15R7, 16R7 YRCSO + XWCSO
R104 1K ½W
R105 220 ½W
D182 23-034
R106 10
T48 30-042
D181 23-034
R103 47
D180 23-034
+SKV
13E1, 14E1
P15
C95 2.2UF 20V
C93 .1MF 30V
15K7, 16K7 XRCS1 + YWCS1
R101 1K ½W
R100 220 ½W
D177 23-034
R99 10
T48 30-042
D179 23-034
R102 47
D178 23-034
-SKV
13E9, 14E9
N15
C96 2.2UF 20V
C94 .1MF 30V
12H9 XRTO
R183 150Ω
YWTO
R182 150Ω
T50 30-039
T51 30-039
D185 23-034
R144 40 5W
D186 23-034
R143 40 5W
D188 23-034
R141 33 5W
D187 23-034
R142 40 5W
L3 30-040
L1 30-040
L2 30-040
D192
T.P.
T.P. VCM
R136 1K
C87 1000 PF
X-Y CURRENT SOURCE
P5
P15
R131 180
R130 39 ½W
Q60 20-008
C86 1000PF
A86 19-094 VOLTAGE REG.
V+
Vcc
VREF
VOUT
C.S. N.C.
C.L. N.C.
COMP
N.I.
INV IN
V-
R134 1.65K 1%
R140 500
RT1
R139 340 1%
R135 825 1%
C90 .1μF
C88 .1μF
C89 .1μF
R133 1.65K 1%
R132 340 1%
R137 4 2W ¼%
BIAS SOURCE
T53 30-026
R148 47
R177 1K 02-C
YCHC
R178 1K 00-C
XCHC
R149 47
R170 10
R179 1K 01-C
XCHA
R180 1K 03-C
YCHA
R169 10
11C7 CHTO
A83 19-137 D
CHARGE CIRCUIT

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a) DIODES ARE 23-001.
b) TRANSISTORS ARE 20-020.

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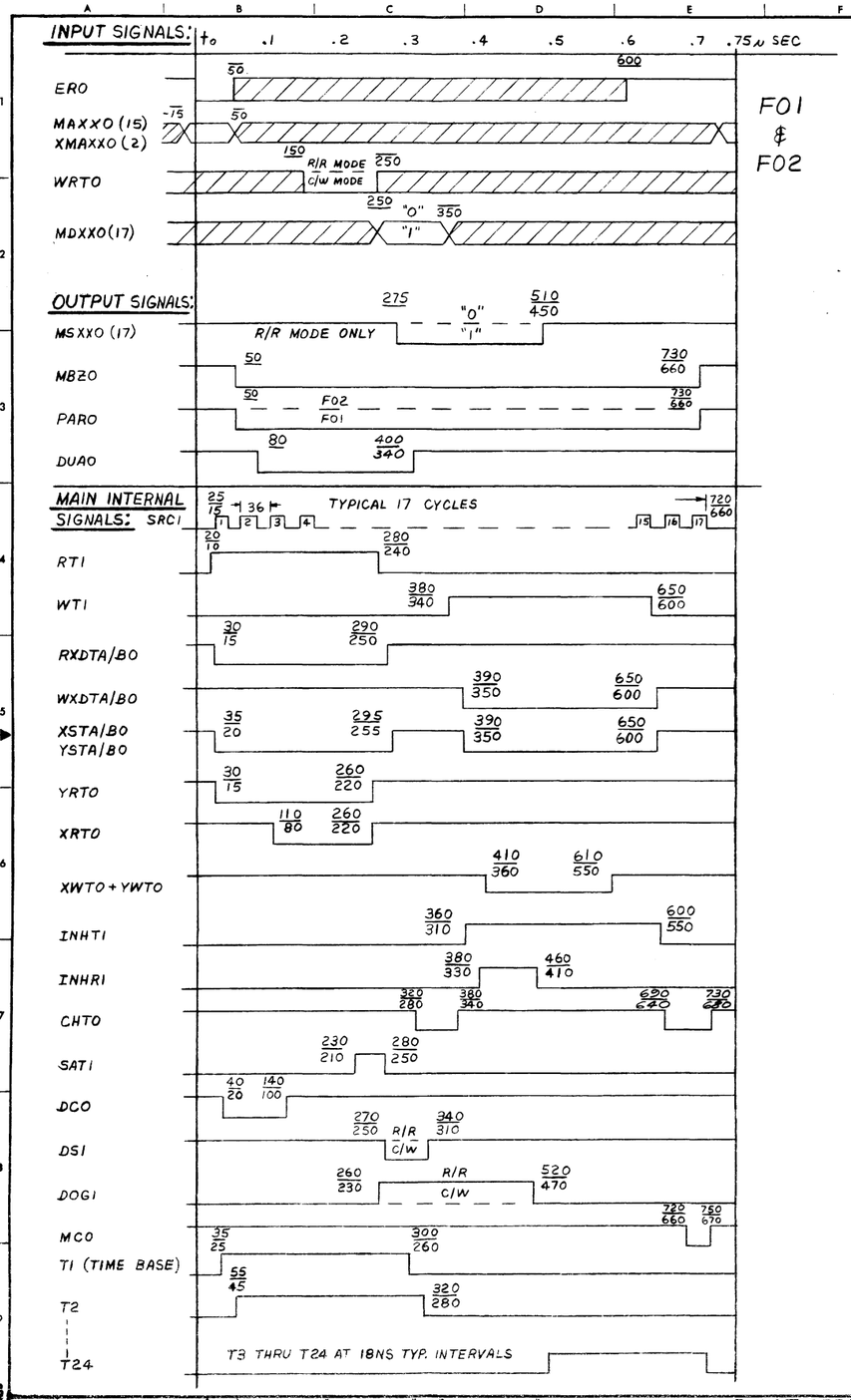
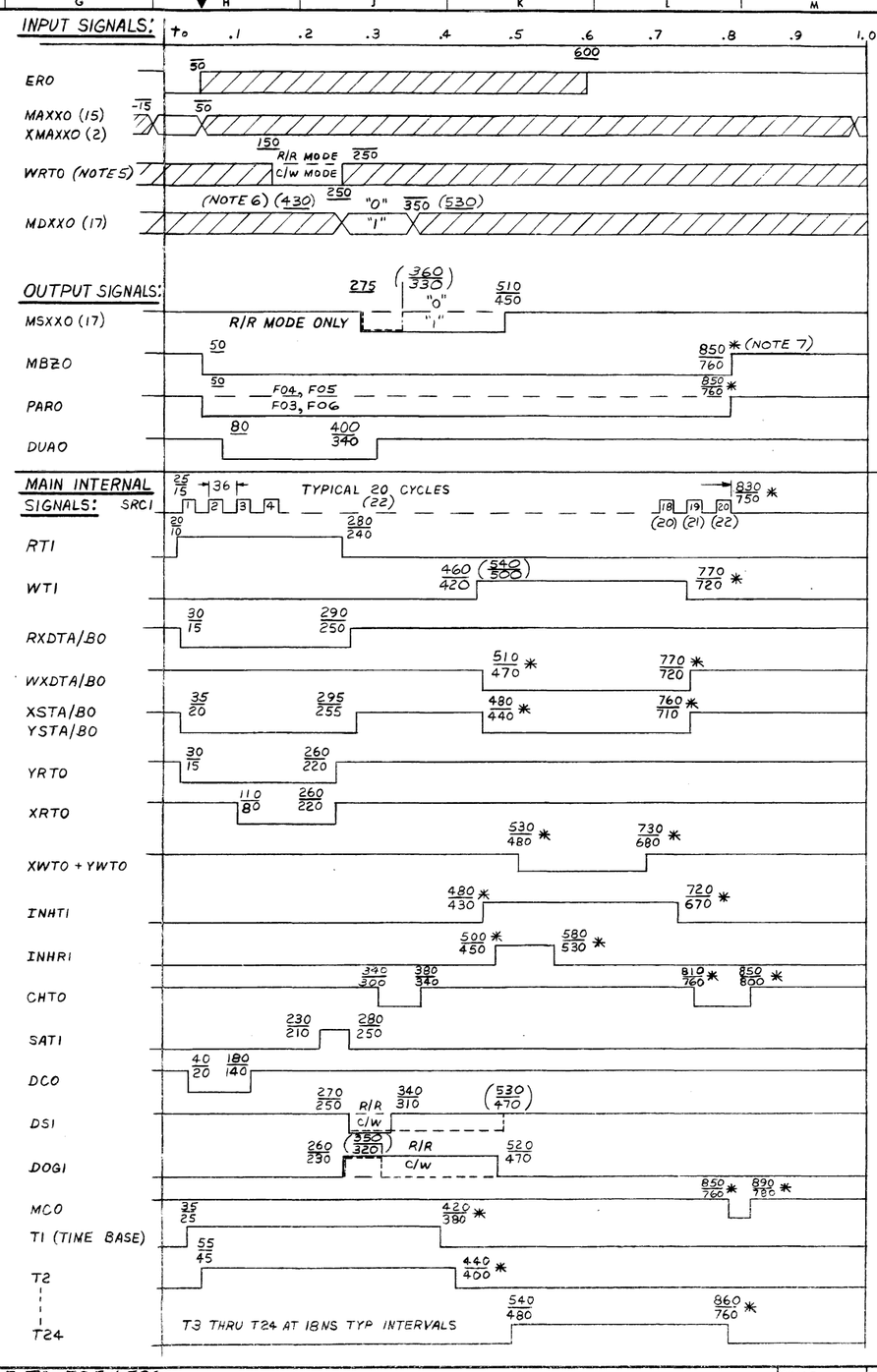
SCALE–	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
ELECTRONICS BOARD
(32KB MEMORY)
TASK NO. 03017
DWG NO. 35-607MO1R01D08
SHEET 17 OF 20

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
AREA J7, 330/300 WAS 320/280			
FM 01	3188	6-19-72	R01
AREA H8, 180/140 WAS 140/100			
FM 01	3198	6-22-72	R02





NOTES:
1. SHADED AREA (////) INDICATES "CAN CHANGE" OR "DO NOT CARE" INTERVAL.
2. UNLESS OTHERWISE INDICATED TIME IS IN NANOSECONDS.
3. THE NUMBER ABOVE THE LINE INDICATES MAXIMUM TIME; BELOW THE LINE IS MINIMUM.
4. ALL SIGNALS ARE OF STANDARD TTL LEVELS & TIMING IS REFERENCED TO 1.5V.
5. NOT APPLICABLE TO F05 & F06.
6. REFERENCES IN BRACKETS ARE APPLICABLE TO F05 & F06 ONLY.
7. REFERENCES DESIGNATED WITH * ADD 80 NANOSECONDS FOR F05 & F06 ONLY.

DRAWING 44-SIZE B/W/D

SCALE–
TOLERANCE
XXX ± .005
XX ± .02
X ± .09
ANGLES ± 10
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

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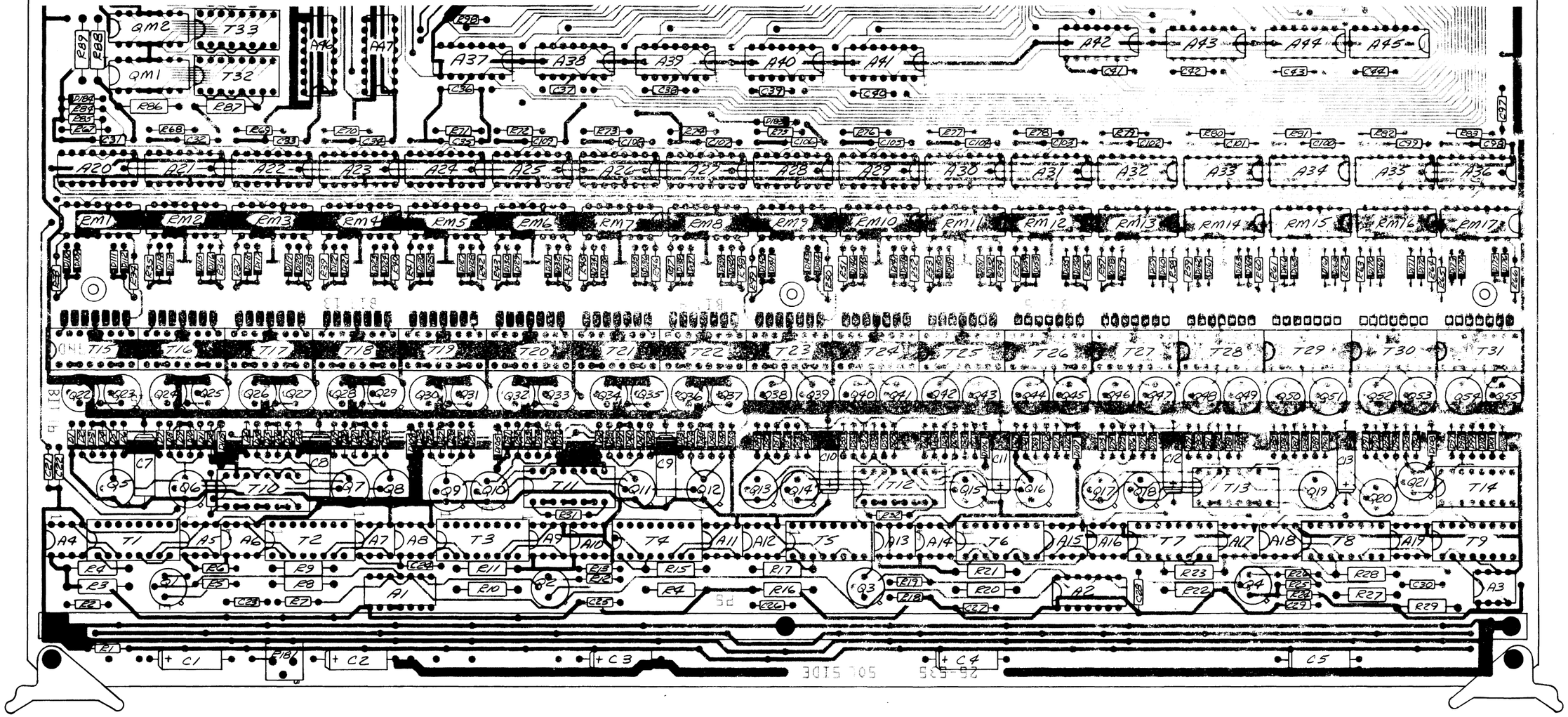
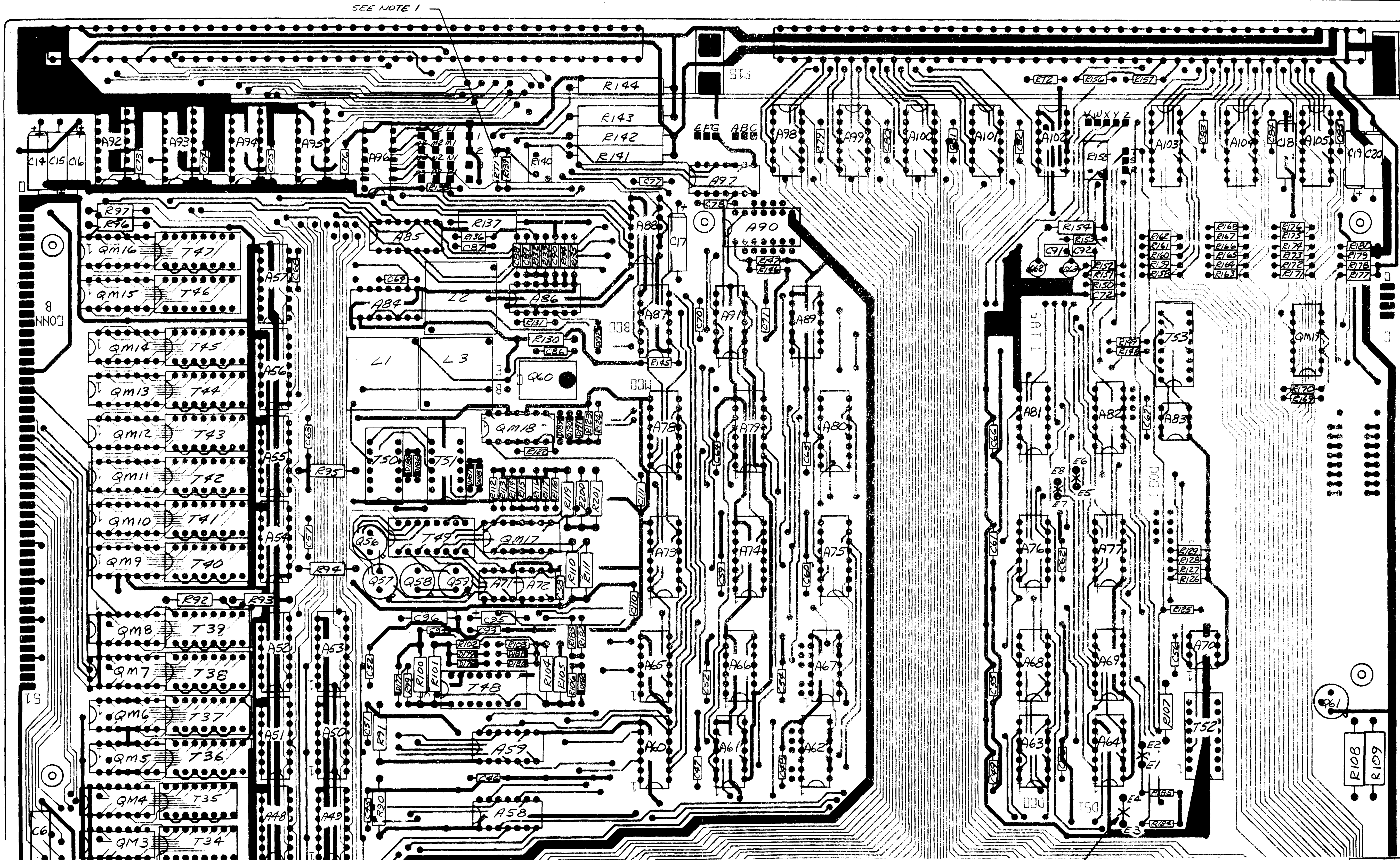
TITLE SCHEMATIC
ELECTRONICS BOARD
(32KB MEMORY)

TASK NO. 03017
DWG NO. 35-607MOIR02D08
SHEET 18 OF 20



VIEWED FROM SOLDER SIDE
FOR COMPONENT REFERENCE ONLY

J. HELVATY	DRAFT	10-12-76	SCHEMATIC ELECTRONICS BOARD (32KB MEMORY)
			03017 SHT OF 19-20
			35-607 M01 D08



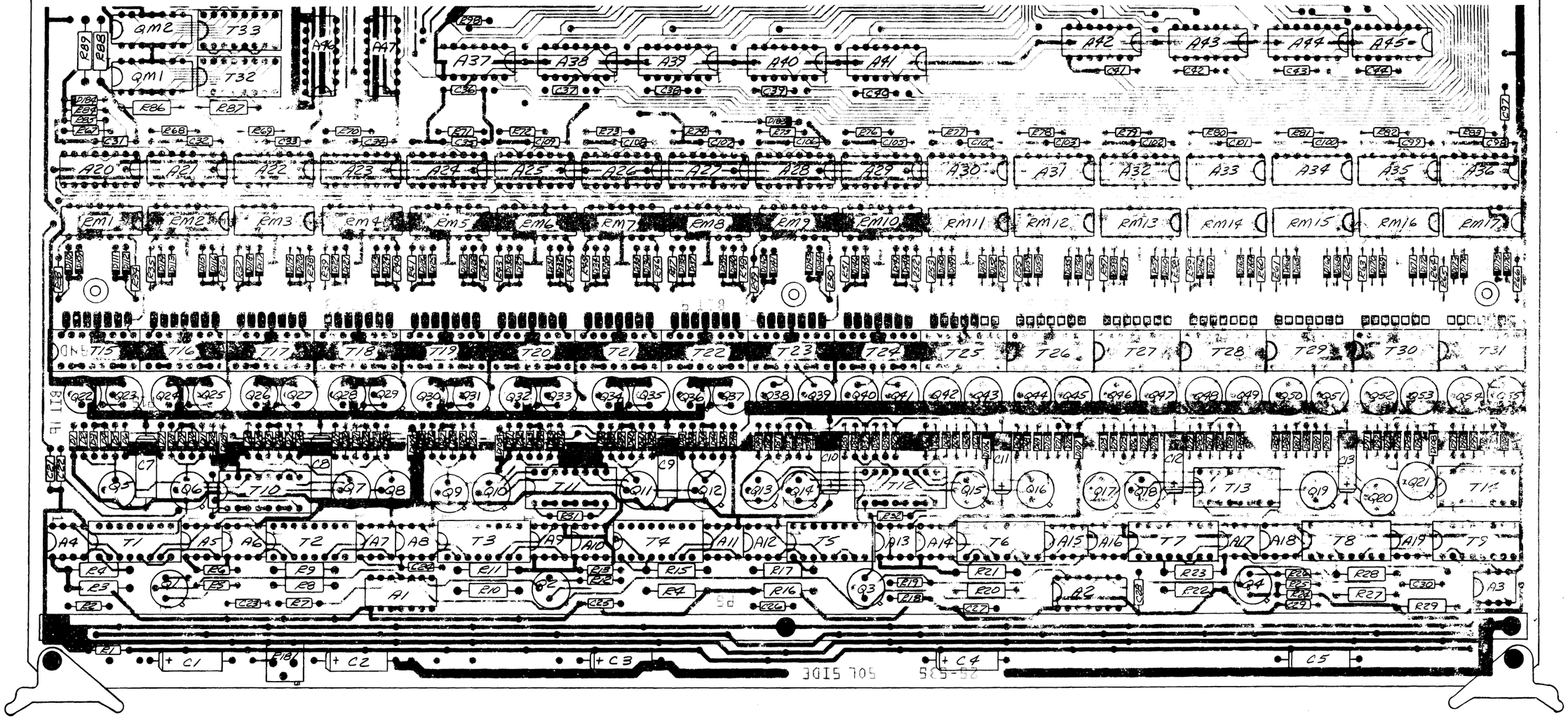
VIEWED FROM SOLDER SIDE
FOR COMPONENT REFERENCE ONLY

COPPER CUT FOR
F05 & F06
TYP 4 PLACES

NOTES:
1. THERMISTOR "RT1" (23-012) IS REQUIRED WITH 35-517F01 CORE STACK ONLY.

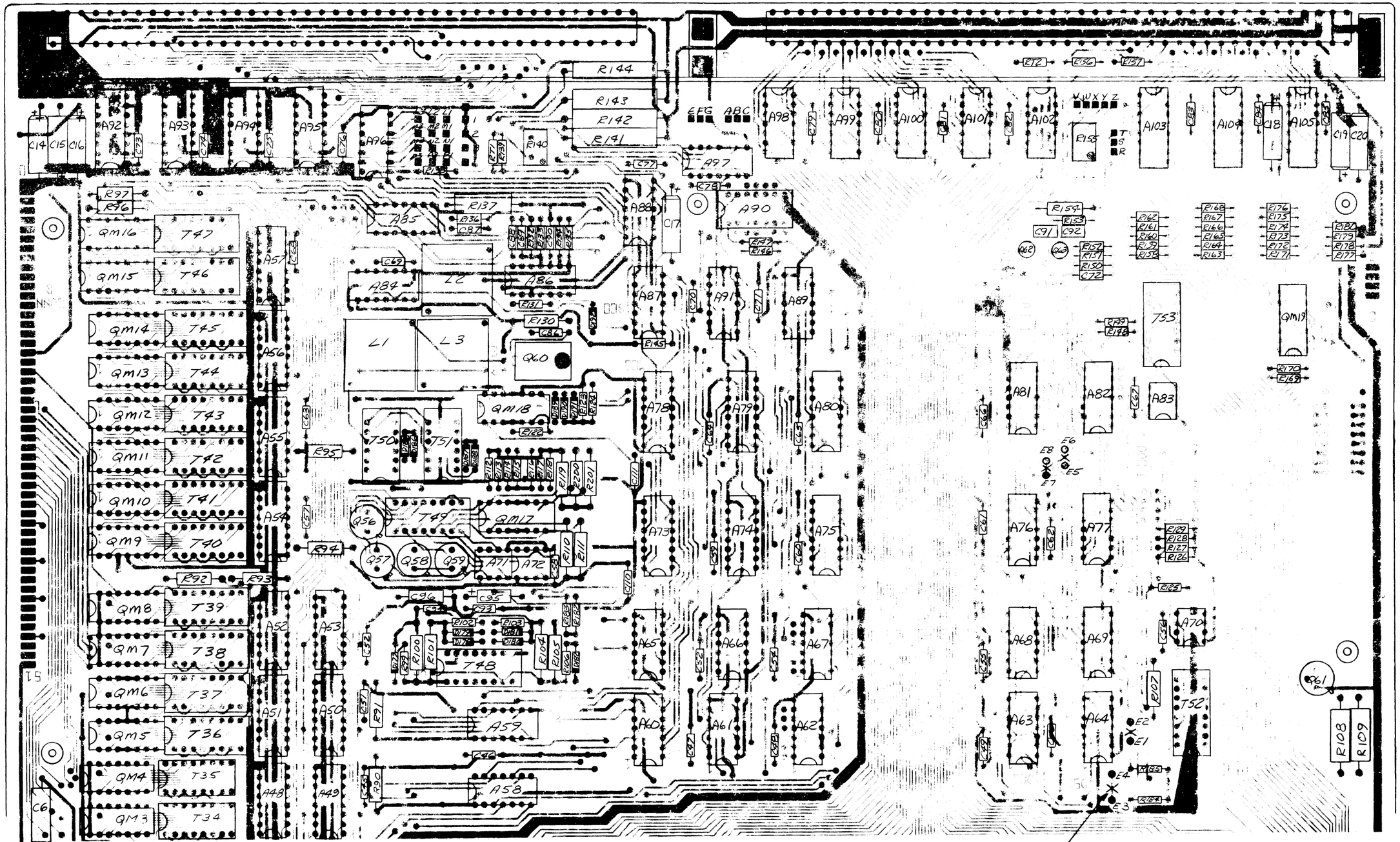
REVISIONS				
ADDED NOTE 1, & CALLOUT TO RT1				
GP	JD	3566	11-15-77	R01

J. HELVATY	DRAFT	10-13-76	SCHEMATIC ELECTRONICS BOARD (32 KB MEMORY)
			03017
			35-607M01R01 D08
			SHT. OF 20 - 20



VIEWED FROM SOLDER SIDE
FOR COMPONENT REFERENCE ONLY

J. HELVATY	DRAFT	10-12-76	SCHEMATIC ELECTRONICS BOARD (32KB MEMORY)
			03017 SHT 0F 19-20
			35-607 M01 D08



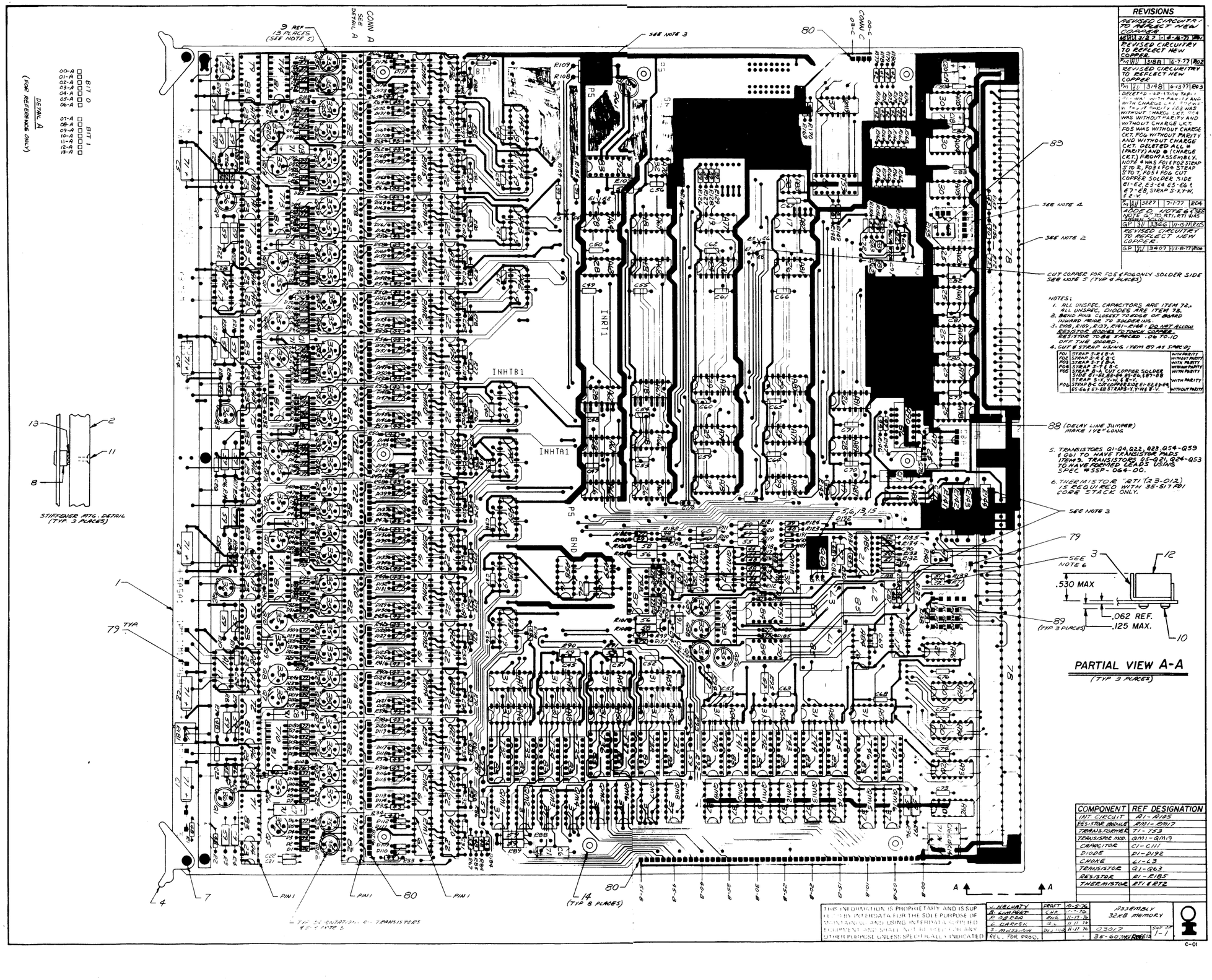
VIEWED FROM SOLDER SIDE
FOR COMPONENT REFERENCE ONLY

COPPER CUT FOR
FO5 & FO6
TYP 4 PLACES

J. HELVATY	DRAFT	10-13-76	SCHEMATIC ELECTRONICS BOARD (32 KB MEMORY)
			03017
			35-607 M01 D08

SHT. 01 OF 20-20

I



NOTES:

1. ALL UNSPEC. CAPACITORS ARE ITEM 72. ALL UNSPEC. DIODES ARE ITEM 73.
2. BEND PINS CLOSEST TO EDGE OF BOARD INWARD AT AN 15° ANGLE MAX.
3. R108, R109, R137, R141-R168 : DO NOT ALLOW RESISTOR BODIES TO TOUCH SOLDER SIDE OF THE BOARD.
4. CUT & STRAP USING ITEM 89 AS SPACER:

FOI	STRAP 5-8 & A	WITH PARITY
FOI	STRAP 5-7 & A	WITHOUT PARITY
FOS	STRAP 5-7 & C	WITH PARITY
FOS	STRAP 5-8 & C	WITHOUT PARITY
FOG	STRAP B-C, CUT COPPER SOLDER SIDE 61-62, 63-64, 65-66, 167-68	WITH PARITY
	STRAP 5-7 & C	
FOG	STRAP B-C, CUT COPPER SIDE 61-62, 63-64, 65-66, 167-68 STRAPS 1-7 & 5-7.	WITHOUT PARITY

5. TRANSISTORS Q1-Q4, Q22, Q23, Q54-Q59 & Q61 TO HAVE TRANSISTOR SPACE ITEM 93. TRANSISTORS Q5-Q21, Q24-Q53 TO HAVE FORMED LEADS USING SPEC #55P-064-00.
6. THERMISTOR RT1 (A3-0(2) IS REQUIRED WITH 35-517.R01 CORE STACK ONLY.

REVISIONS				
REVISED CIRCUITRY TO REFLECT NEW COMPAR				
GP	JU	3188	6-7-77	B02
REVISED CIRCUITRY TO REFLECT NEW COMPAR				
PM	JU	3198	6-13-77	B03
DELETED CAPACITOR TAP... WAS WITH PARITY AND WITH CHARGE CKT. THIS WAS W/ PARITY BUT NO CHARGE CKT. B03 WAS WITHOUT PARITY AND WITHOUT CHARGE CKT. B04 WAS WITHOUT PARITY AND WITHOUT CHARGE CKT. FOS WAS WITHOUT CHARGE CKT. FOG WITHOUT PARITY AND WITHOUT CHARGE CKT. DELETED ALL ● (PARITY) AND ● (CHARGE CKT.) FROM ASSEMBLY. NOTE 4 WAS FOI, FOS STRAP 5 TO 7, FOS & FOG CUT COPPER SOLDER SIDE 61-62, 63-64, 65-66, 167-68, STRAP 5-7 W. 67-68, STRAP 5-7 W. 68-V				
PM	JU	3227	7-1-77	B04
ADDED SCOTCH #850 TAPE SEE NOTE 5. TO RT1. RT1 WAS SHIELDED				
GP	JU	3366	11-15-77	B05
REVISED CIRCUITRY TO REFLECT NEW COPPER.				
GP	JU	3407	12-8-77	B06

COMPONENT	REF DESIGNATION
INT. CIRCUIT	A1 - A105
RESISTOR MODULE	RM1 - RM17
TRANSFORMER	T1 - T53
TRANSISTOR MOD.	QM1 - QM19
CAPACITOR	C1 - C111
DIODE	D1 - D132
CHOKE	L1 - L3
TRANSISTOR	Q1 - Q63
RESISTOR	R1 - R185
THERMISTOR	RT1 & RT2

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J. HELVATY	DRAFT	10-5-76
R. HUBBERT	ENG.	11-17-76
P. O'BRIEN	ENG.	11-17-76
C. WARREN	QA	11-17-76
S. MADISON	DES. MGR.	11-17-76
REL. FOR PROD.		

ASSEMBLY 32KB MEMORY

030177

35-607.M01 REV B

SHT 1 OF 1

C-01

REVISIONS			
REVISED CIRCUITRY TO REFLECT NEW COPPER			
P.R.	1	3148	11/3/77
REVISED CIRCUITRY TO REFLECT NEW COPPER			
P.R.	1	3148	11/3/77
DELETED LEAD WIRE TAG 1, CUT W1 TO MAKE WITH CHARGE (PART NO. 1), W2 TO MAKE WITHOUT CHARGE (PART NO. 2), W3 TO MAKE WITHOUT CHARGE (PART NO. 3), W4 TO MAKE WITHOUT CHARGE (PART NO. 4), ADDED W5 TO MAKE WITH CHARGE (PART NO. 5), ADDED W6 TO MAKE WITHOUT CHARGE (PART NO. 6), ADDED MJ-1 SELECTED MJ-1 (PART NO. 01 CHARGE (LAT.) FROM ASSEMBLY. NOTE 4 WAS FOR E7 STRAP E7 TO E8 FOR STRAP E7 TO E9 CUT FOR COPPER. NOW FOR E1-E4, E2-E3, E5-E6, E7-E8, STRAP E2 TO E4.			
P.R.	1	3223	1/11/77

NOTES:
1. ALL UNSPEC. CAPACITORS ARE ITEM 78.
   ALL UNSPEC. DIODES ARE ITEM 78.
2. BEND RIVE CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING.
3. R101, R107, R107, R01-R140 : DO NOT ALLOW RESISTOR LEADS TO TOUCH COPPER. RESISTOR TO BE SPACED .06 TO .10 OFF THE BOARD.
4. CUT & STRAP USING ITEM 89 AS SPEC'D:

FO1	STRAP S1-E1-A	WITH PARITY
FO2	STRAP S2-E2-B	WITHOUT PARITY
FO3	STRAP S1-E1-C	WITH PARITY
FO4	STRAP B-A CUT COPPER SOLDER SIDE E1-E2 & E5-E6 E7-E8 STRAP S1-Y W/ 1 W.	WITHOUT PARITY
FO5	STRAP B-C CUT COPPER SIDE E1-E2 & E5-E6 E7-E8 STRAPS-Y W/ 1 W.	WITH PARITY
FO6	STRAP B-C CUT COPPER SIDE E1-E2 & E5-E6 E7-E8 STRAPS-Y W/ 2 W.	WITHOUT PARITY

COMPONENT	REF DESIGNATION
INT. CIRCUIT	Q1 - Q185
RESISTOR MODULE	RM1 - RM17
TRANSFORMER	T1 - T3
TRANSISTOR MOD.	QM1 - QM19
CAPACITOR	C1 - C111
DIODE	D1 - D132
CHOKE	L1 - L3
TRANSISTOR	Q1 - Q63
RESISTOR	R1 - R185
THERMISTOR	RT1 & RT2

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K. HELVATY	DRFT	10-8-76
R. WILBERT	CKD.	10-76
D. OBRIEN	ENG.	11-17-76
R. BASSER	M.C.	11-17-76
S. MESSINA	QA	11-17-76
REL. FOR PROD.	MFG	11/17/76

ASSEMBLY 32K8 MEMORY

03017 REV 04

36-603 01 A 603

SHT 1 OF 1

C-01

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