Test Aid schematic 35-612 is in this Document After "Display Panel" Section.

QUICK REFERENCE INDEX

To aid in quickly locating a particular section, the index marks on the edge of this page are aligned with similar marks on the first page of each section.

MANUAL UPDATE PACKAGE COVER SHEET

MANUAL TITLE: M83 SERIES MODEL 8/32, 8/32C, AND 8/32D PROCESSORS Maintenance Manual

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This package updates the old pages of the subject manual with the new pages. Please discard old pages.

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35-535 R23D08, Sheets 1, 4	35-535 R24D08, Sheets 1, 4
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35-555 R10D08, Sheets 1, 3, 5, 8	35-555 R12D08, Sheets 1, 3, 5, 8
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PERKIN-ELMER

M83 SERIES MODEL 8/32, 8/32C AND 8/32D PROCESSORS

Maintenance Manual

Consists of:

29-394R85

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PREFACE

This manual provides information to operate, install and maintain the M83 Series Model 8/32 Processors.

Revision 85 includes revisions 82 through 85 and reflects changes to assembly and schematic drawings.

For information on the contents of all Perkin-Elmer 32-bit manuals, see the 32-Bit Systems User Documentation Summary.

GENERAL DESCRIPTION

29-394R03A12
May 1978

METRIC

M83 SERIES
MODELS 8/32, 8/32C, AND 8/32D
PROCESSORS
GENERAL DESCRIPTION

1. INTRODUCTION

The M83-Series 8/32 Processors are 32 bit micro-programmed minicomputers. By combining advanced circuits, packaging, and micro-programming, Interdata gives the user price/performance optimized machines. The Model 8/32 was developed because of the need for a high-speed 32 bit minicomputer. Because of Perkin-Elmer's experience with 16 bit minicomputers and a user instruction format that is readily suited for a 32 bit machine, Perkin-Elmer is able to provide a 32 bit machine. The Model 8/32 is upward compatible with other current Perkin-Elmer Processors. Through micro-programming, the Model 8/32 Processor is able to provide present and future owners of Perkin-Elmer's 16 bit minicomputers the ability to grow into a 32 bit Model 8/32 without having to regenerate all the programs that were created on their 16 bit Processors.

The M83-Series consists of three models: the 8/32, the 8/32C, and the 8/32D. The basic Model 8/32 introduced the M83-Series modular processor architecture. In addition to the Control and Input/Output modules whose operations are similar in all models of the series, the basic 8/32 contained a combined ALU/FAU module which performed either fixed point arithmetic or single precision floating point arithmetic. The basic 8/32 backpanel wiring is shown on Back Panel Map 01-078D08. The basic Model 8/32 (M83-023) is no longer a current Perkin-Elmer product.

The Model 8/32C Processor (M83-025) includes provisions for a High Speed Data Handling option (HSDH) which upgrades the operations of the processor Auto Driver channel, and provisions for a High Performance Floating Point option (DFU) which performs both single and double precision floating point operations. In the Model 8/32C and the Model 8/32D, the existing single-precision floating point ability of the ALU module is only available through the facilities of a Writable Control Store option (WCS). The Model 8/32C is configured with 32KB 750 nanosecond core memory modules expandable through two expansion chassis to one megabyte. The Model 8/32C backpanel wiring is shown on Back Panel Map 01-098D08.

The Model 8/32D Processor (M83-030) is identical to the 8/32C except that it is configured with 64KB 750 nanosecond core memory modules expandable through one expansion chassis to one megabyte, and the boards have different chassis slot positions (see chart on page 4). The Model 8/32D backpanel wiring is shown on Back Panel Map 01-103D08.

The Model 8/32 Processors have 148 instructions defined which include arithmetic and logical, operational, list processing, floating point, cyclic redundancy checking, and bit and byte manipulation instructions. Double indexing is also allowed, along with a multitude of branch instructions. There are 40 extended branch instructions (Mnemonics) defined which brings the total instructions to 180. Through these instructions and direct addressing, coding and debugging time is reduced to a minimum.

The 8/32 Processors offer 32 General Registers, each 32 bits wide, in two sets of 16 (optionally expandable to 8 sets). Register set selection is controlled by bits in the Program Status Word. The multi-set organization offers fast and simple context switching without the necessity of storing and restoring register sets. See 32 Bit Series Reference Manual, Publication Number 29-365.

The 8/32 Processors contain 1,280 words of micro-programmed Control Store in the Control Module. The Control Store may be optionally expanded through a 512 word and/or a 2,048 (2K) word Writable Control Store (WCS).

The 8/32 Processors are capable of directly addressing up to 1,048,576 bytes of memory, through the Local Memory Bus. Memory is constructed of 32KB or 64KB memory modules. Memory is addressable to the eight-bit byte level. No paging or indirect addressing is required by the user instruction sets. A Multiport Memory option is available which allows multiple processors to share memory. In addition, a Processor/Memory Parity Generation and Checking Hardware option is available. The processors contain a Memory Access Controller (MAC) and a Memory Bus Controller (MBC). The MAC contains its own sixteen 32 bit hardware registers to allow segmentation, relocation, and memory protection of user programs. The MBC provides access to both the Local Memory Bus (LMB) and the Extended Direct Memory Access Bus (EDMA). The EDMA Bus is a high quality, high-speed bus that may have up to seven EDMA devices attached. These optional devices include the Extended Selector Channel (ESELCH) which provides direct memory access to high speed peripherals at a transfer rate of 2 million bytes per second; the Buffered Selector Channel (BSELCH) with a EDMA transfer rate of up to 6 million bytes per second; the Memory Access Multiplexor (MAM), a direct memory access port which provides interleaved block transfers of data between multiple low and medium speed peripheral devices and memory; the EMAM, an enhanced version of the MAM; and the EDMA Bus Universal Interface used in designing custom controllers. The ESELCH or BSELCH may have up to 16 devices attached, and may be extended for additional devices through the use of the I/O Switch.

The 8/32 Processors provide a flexible automatic input/output system through the processor Multiplexor Bus in addition to the conventional means of programmed I/O. The Processors can have up to 1,023 auto driver channels, implemented through the microcode instructions. These provide fast automatic character input/output operations including automatic conversion from one character to another. Each character is transferred into or out of memory without any effect on a running program except for a small amount of stolen time. The auto driver channel operations may be optionally enhanced through the High-Speed Data Handling option. The Multiplexor Bus can have up to 16 peripheral controllers attached directly, but may be optionally extended through the use of the I/O Switch.

2. RELATED PUBLICATIONS

Table 1 contains a list of related Perkin-Elmer publications which may be useful in the programming or trouble shooting of the M83-Series 8/32 Processors.

TABLE 1. RELATED PUBLICATIONS

Title	Publication Number
32 Bit Series Reference Manual	29-365
Series 32 Pocket Guide	29-445
Models 8/32, 8/32C, 8/32D Processors User's Manual	29-428
Installation Planning Guide	29-583
Model 8/32 Customer Installation Manual	29-526
Model 8/32 Installation Manual (for Perkin-Elmer Internal use only)	29-449
Models 8/32C and 8/32D Customer Installation Manual	29-537
Models 8/32, 8/32C, and 8/32D Processors Micro Instruction Reference Manual	29-438
Perkin-Elmer Model 8/32 Writable Control Store (WCS) User's Guide	29-479
Models 8/32C and 8/32D Communication Instruction Package Maintenance Manual	29-520
8/32 DFU Instruction Manual	29-538
32KB (750 ns) Core Memory Maintenance Manual	29-493
64KB (750 ns) Core Memory Maintenance Manual	29-593
Multiport Memory Instruction Manual	29-539
Shared Local Memory Interface (SLMI) Maintenance Manual	29-611
EDMA Bus Universal Interface Instruction Manual	29-423
Extended Selector Channel (ESELCH) Programming Manual	29-529
Buffered Selector Channel (BSELCH) Maintenance Manual	29-572
Buffered Selector Channel (MOI) Maintenance Manual	29-590
Memory Access Multiplexor (MAM) Maintenance Manual	29-422
Memory Access Multiplexor (MAM) Programming Manual	29-474
EMAM Maintenance Manual	29-609
EMAM Programming Manual	29-610
Input/Output Switch Maintenance Manual	29-616
Input/Output Switch Programming Manual	29-617
Universal Clock Instruction Manual	29-427
Digital Multiplexor System Instruction Manual	29-209
High-Speed Paper Tape Reader/Punch Technical Manual	29-334
Paper Tape Reader Manual	29-549
Teletype Interface Instruction Manual	29-288
Current Loop Interface Maintenance Manual	29-444
Model 1100 Terminal User/Maintenance Manual	29-605
Model 1200 Terminal User/Maintenance Manual	29-612
Card Reader Manual	29-510
Intertape Cassette System Instruction Manual	29-297
N.S. Line Printer Maintenance Manual	29-313
Fully Buffered Line Printer 300 LPM Manual	29-511
Read After Write Magnetic Tape System Instruction Manual	29-295
1600 BPI Magnetic Tape System Instruction Manual	29-309
Dual Density Tape System Maintenance Manual	29-559
2-5 MD Disc Perkin-Elmer Maintenance Manual	29-487
10 MB Disc Maintenance Manual	29-486
Removable Media Mass Storage Module (MSM) Maintenance Manual	29-644
Mini I/O System Instruction Manual	29-443
Micro I/O Bus Adaptor Instruction Manual	29-597
Analog Input Controller System Programming Manual	29-475
Analog Output Controller System Programming Manual	29-476
Digital I/O (DIO) Programming Manual	29-477
8/32 Test Display Instruction Manual	29-525

3. BLOCK DIAGRAM

A simplified block diagram of the Model 8/32 system is shown in Figure 1. The Processor logic is contained on three circuit boards. The Memory Bus Controller (MBC), Local Memory Interface (LMI) and memory are contained on separate boards. The Arithmetic/Logic Unit (ALU) and Input/Output Unit (IOU) are also separate boards. The 8/32 Processors are contained in a standard 16 slot Perkin-Elmer Twin Chassis which is divided into an Upper (U) 8 slots (numbered 0-7) and a Lower (L) 8 slots (numbered 0-7). Shown below are the chassis slots associated with specific processor boards.

Part Number	Description	Chassis Slot		
		8/32	8/32C	8/32D
35-534	Local Memory Interface (LMI)	3U,6U	3U,6U	2U,5U
35-535	Memory Bus Controller (MBC)	1U	1U	1U
35-536	Control Processor A (CPA)	0U	0U	0U
35-537	Control Processor B (CPB)	7L	7L	7L
35-555 or 36-663	Control Processor C (CPC)	6L	6L	6L
35-538	Arithmetic Logic Unit (ALU)	4L	3L	3L
35-539	Input/Output Unit (IOU)	3L	0L	0L
	Floating Point* (DFA)	---	5L	5L
	Floating Point (DFB)	---	4L	4L
	Memory	2U,4U,5U,7U	2U,4U,5U,7U	3U,4U,6U,7U

*Optional

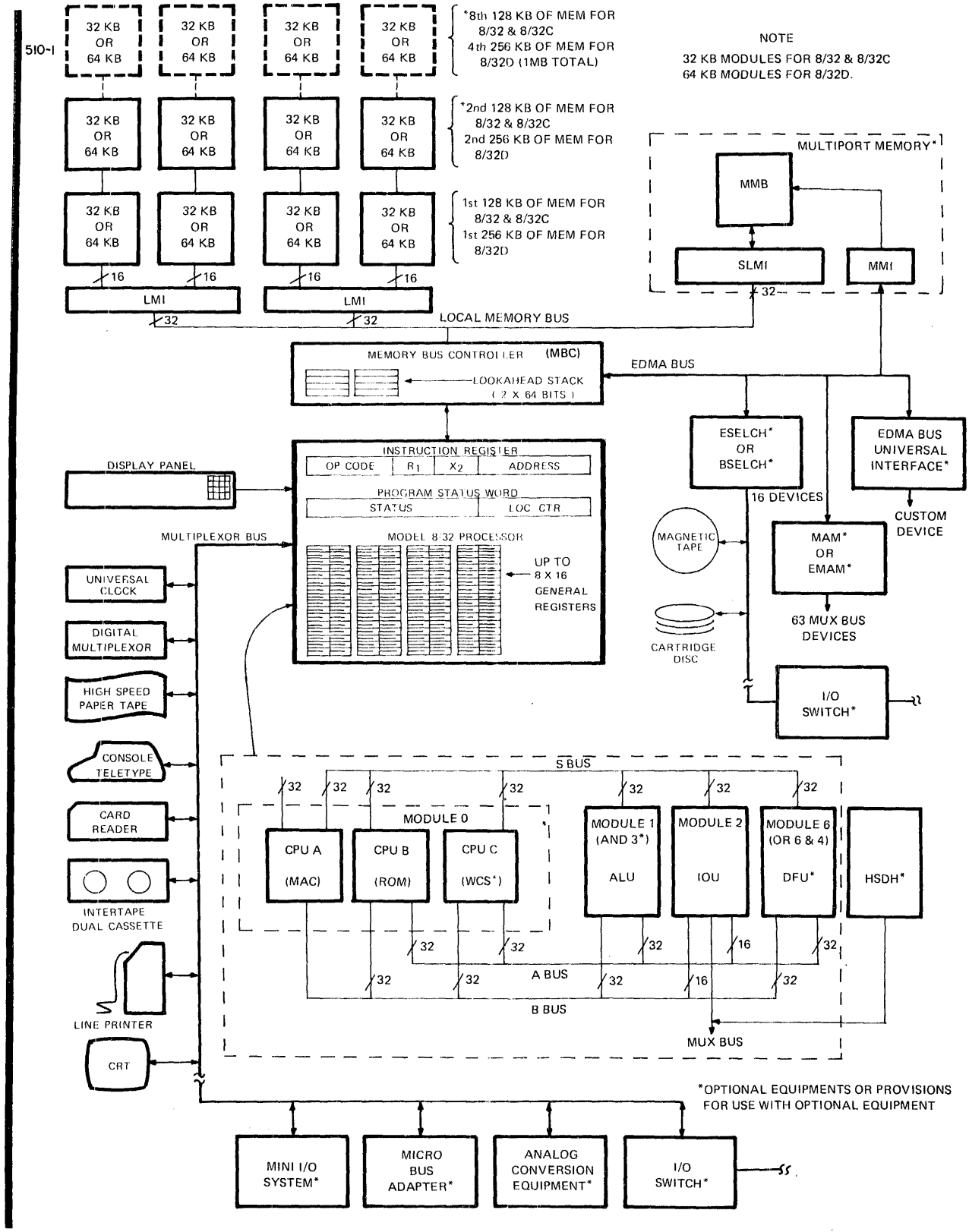


Figure 1. 8/32 Processor Block Diagram

4. DOCUMENTATION

This section describes the style and conventions used with Perkin-Elmer documentation.

4.1 Number Notation

The most common form of number notation used in Perkin-Elmer documentation is hexadecimal notation. In this system, groups of four binary digits are represented by a single hexadecimal digit. Table 2 lists the hexadecimal characters employed.

TABLE 2. HEXADECIMAL NOTATION DATA

Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	10	A			
0101	5	5	1011	11	B			

To differentiate between decimal and hexadecimal numbers, hexadecimal numbers are preceded by the letter "X" and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are: X'1234', X'2EC6', X'AE40', X'EEFA', and X'10B9'. With 32 bit systems the letter Y may be used to distinguish between 16 and 32 bit references (X for 16 bit, Y for 32 bit notation).

4.2 Part Numbering System

Perkin-Elmer parts, drawings, and publications employ a common numbering system. The part number and drawing numbers for drawings which describe the part are related. Figure 2 shows the format used for Perkin-Elmer part numbers. The fields are described in the following paragraphs.

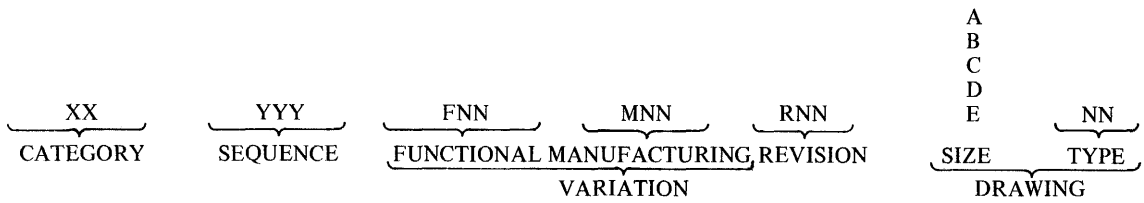


Figure 2. Part Number Format

4.2.1 Category Field. The two-digit Category number indicates the broad class or category to which a part belongs. Typical examples of category number assignments are:

01 - Basic Hardware Systems
02 - Basic Hardware Expansions
03 - Basic Software Systems
04 - Software Packages
05 - Micro-programs
06 - Test Programs
07 - Subroutines of General Utility
10 - Spare Parts Packages
12 - Card File Assemblies
13 - Panels
17 - Wire and Cables
19 - Integrated Circuits
20 - Transistors
27 - Peripheral Equipment
29 - Manuals
34 - Power Supplies
35 - Assembled Printed Circuit Boards
36 - Electro-Mechanical Devices

4.2.2 Sequence Field. The Sequence number identifies a particular item within the category. Sequence numbers are assigned serially, and have no other significance.

NOTE

The Sequence Field, like all other part number fields, may be lengthened as required. The field lengths shown on Figure 2 are minimum lengths (insignificant zeros must be added to maintain these minimums).

A part number must contain a Category number and a Sequence number. All other fields are optional.

4.2.3 Functional Variation Field. The optional Functional Variation Field consists of the letter "F" followed by two digits. The F field is used to distinguish between parts which are not necessarily electrically or mechanically equivalent, but which are described by the same set of drawings. For example, a power supply may be strapped internally to operate on either 110 VAC or 220 VAC. Except for this strap, all power supplies of this type are identical. The strapping option is easily described by a note on the assembly and test specification drawings. Therefore, this is a functional variation.

4.2.4 Manufacturing Variation Field. The optional Manufacturing Variation Field consists of the letter "M" followed by two digits.

The M Field is used to distinguish between parts which are electrically and mechanically equivalent (interchangeable), but which vary in method of manufacture. For example, if leads are welded instead of soldered on an assembly, the M Field changes.

An important exception to the meaning of the M Field exists for categories related to software. In software, the M Field number, when used, indicates the form in which a particular program is presented. For example, define a program as a set of machine instructions. These same identical instructions may be presented on punched cards, paper tape, or magnetic tape; and for any of these they could be in symbolic form or in relative or absolute binary form. Thus, there are many ways to present the same identical program.

The format for the M field and its meaning for software is:

Mxy

where x identifies the media selection (i.e., paper tape, mag tape, cassette, etc.) and
y identifies object or source and the format.

Meaning of x		Meaning of y
Paper tape	1	1 Object program standard format 32 bit Processor
Cassette	2	4 Memory Image
Mag tape (800)	3	6 Object program standard format 16 bit Processor
Cards	4	7 Object non-standard format
Disc (2.5)	5	8 Object established task
		9 Source program

The above numbers refer to the physical program placed on an approved media for Perkin-Elmer Software. A paper tape object program in standard format and for a 16 bit Processor has an M16 identifier. A magnetic tape object program in standard format and for a 32 bit Processor has an M31 identifier.

In addition to the above, there are several unique M numbers which have special meaning:

M95 always refers to a software package reference document
M99 always refers to a documentation package.
M00 always refers to a conceptual object program divorced from any media. This reference is used for all parts lists when object programs may be on any media.
M90 always refers to a conceptual source program and is used on all parts lists where any media may be used.

NOTE

M00 and M90 may only be used on parts lists and never identify a physical program on any media.

4.2.5 **Revision Field.** The optional Revision Field consists of the letter "R" followed by two digits. The R Field is used to indicate minor electrical or mechanical changes to a part which do not change the part's original character. R Field changes often reflect improvements. A part with a revision level HIGHER than the one specified will work. A part with a revision level LOWER than specified should not be used.

4.2.6 **Drawing Field.** The optional Drawing Field consists of a letter from "A" to "E" followed by two digits. The letter indicates the size of the original drawing. The sizes for each letter are:

A - 216 mm X 279 mm (8½" X 11")

B - 279 mm X 432 mm (11" X 17")

C - 432 mm X 566 mm (17" X 22")

D - 566 mm X 864 mm (22" X 34")

E - 864 mm X 1118 mm (34" X 44")

The two digits indicate the drawing type as follows:

01 - Parts List	13 - Program Listing
02 - Machine Details	14 - Abstracts
03 - Assembly Details	15 - Program Description
05 - Art Details	16 - Operating Instructions
06 - Wire Run List	17 - Program Design Specifications
08 - Schematic	18 - Flow Charts
09 - Test Specification	19 - Product Specification
10 - Purchase Specification	20 - Installation Specification
11 - Bill of Material	21 - Maintenance Specification
12 - Information	22 - Programming Specification

4.2.7 **Examples.** The following list provides examples of the part numbering system. The numbers were arbitrarily selected, and in most cases are fictitious.

35-060	The 60th printed-circuit board assigned a part number under this system.
35-060M01	A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in method of manufacture.
35-060F01	A printed-circuit board not electrically and mechanically interchangeable with the 35-060, but described by the same set of drawings.
35-060R01	A revised 35-060 printed-circuit board. Probably supercedes the 35-060.
35-060A01	The 216 mm X 279 mm (8½" X 11") parts list for a 35-060.
35-060B08	The 279 mm X 432 mm (11" X 17") schematic for a 35-060.
06-072	The 72nd utility program assigned a part number.
06-072A13	An 216 mm X 279 mm (8½" X 11") listing of the 06-072 program.
06-072M03	An absolute binary deck of punched cards for the 06-072 program.
06-072A12	The 216 mm X 279 mm (8½ X 11") information drawing on the 06-072 program. Probably a part of the program.
29-060	The 60th manual assigned a number under this system. Note that this number is not referenced in any way to the part number of equipment described in the manual.

4.3 Drawing System

This section describes the drawings provided with Perkin-Elmer equipment. Note that drawings provided with peripheral devices and other purchased items may vary from the system described in this section.

A digital system may be divided into a collection of functionally independent circuits such as memory, Processor, and I/O device controllers. These circuits may or may not be saleable units in their own right, but in the electrical sense they are essentially self contained and capable of performing their function with minimum dependence on other functional circuits in the system. Hence a functional circuit is treated as a building block. Each schematic contains a variety of information including type and location of discrete Integrated Circuits (IC's), pin connections, all interconnections within the schematic, connector pin numbers and connections to other schematics. Further, the schematics are drawn to reflect, in an orderly fashion, all logical operations performed by the circuits. Generally, symbols used on schematics conform to MIL-STD-806B.

Registers are named according to the following rules:

1. The register Mnemonic name has a maximum of three letters, excluding "I, O, Q, and Z".
2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant positions, and continuing to N-1 on the right, where N is the number of bits in the register.
3. The 00 bit is the Most Significant Bit and the N-1 is the Least Significant Bit.

The IC's, mounted directly on the logic board, are represented on the schematic drawings by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol Mnemonic designation. Refer to Figure 3.

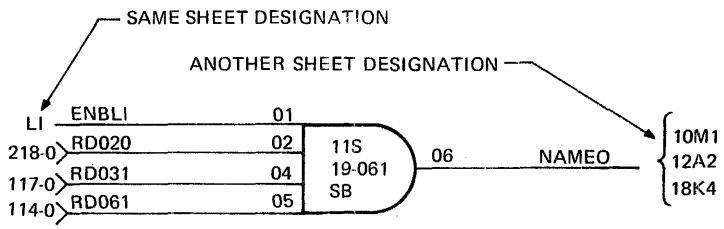


Figure 3. Example of a Schottky Buffer

The designations, numbers, and references shown in Figure 3 are:

11S - This indicates the component location on the logic board. Figure 4 illustrates the method generally used to determine component location on a logic board. With the logic board oriented so that the header connectors (Conn 0 and Conn 1) are on the right, the components are numbered from left to right starting in the upper left corner. That is, the first IC in the upper left corner is 00A and the first capacitor is C1. Test points are lettered right to left from A-Y (omitting I, O, L, E).

19-061 - The number 19 is the category number of ICs, and the 061 is the sequence number of the component.

SB - Indicates this component is a Schottky Buffer. Some other common designations used are:

P - Power Gate
SA - Schottky AND Gate
SB - Schottky Buffer
SG - Schottky Gate
SGO - Schottky Gate, Open Collector
HG - High Speed Gate
HPO - High Speed Power Gate, Open Collector
SFF - Schottky Flip-flop

L1 - This input lead is from area L1 on the same schematic sheet.

10M1, 12A2, 18K4 - Indicate outputs to another logic schematic sheet.

218-0, 117-0, 114-0, - Indicate inputs from Connector 0.

Note that the pin numbers (01, 02, 04, 05 and 06) correspond directly to the actual IC pin numbers.

Figure 4 also shows the locations of the header connectors (Conn 0 and Conn 1) and the cable connectors (Conn 2 and Conn 3). All logic boards always contain Header Connectors 0 and 1, however, any combination (either, both, or none) of cable connectors (Conn 2 and Conn 3) may be provided.

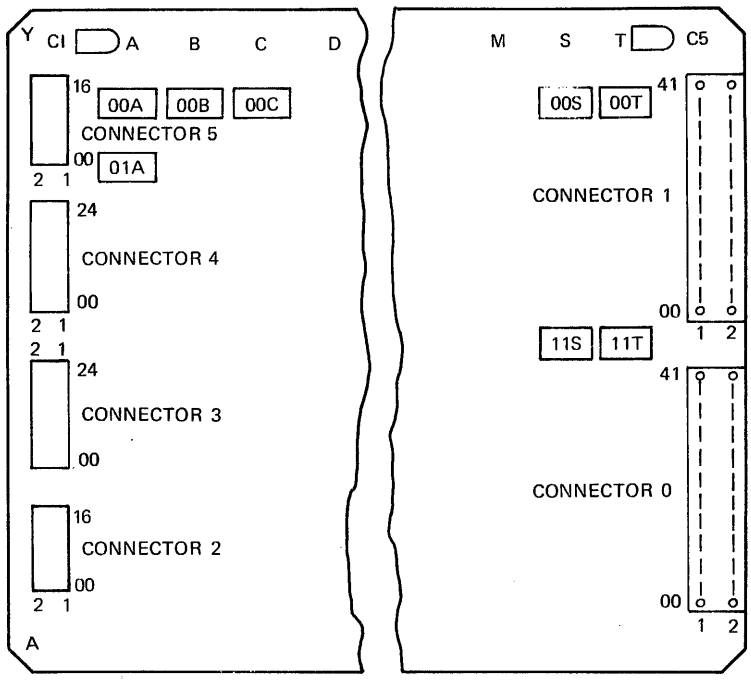
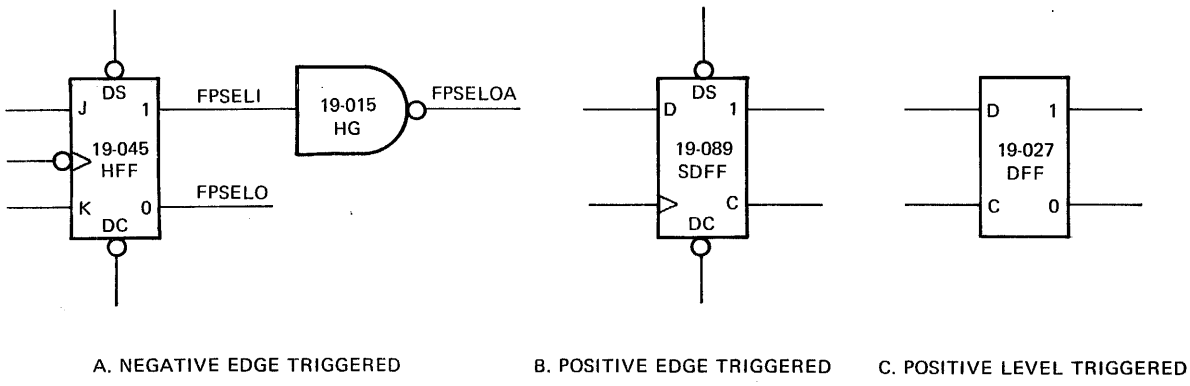


Figure 4. Example of a Logic Board Layout

Clocked devices, flip-flops and counters in particular, are drawn in a manner which indicates information concerning their inputs. An input which has a circle adjacent to the pin designation implies a low active signal is required to perform the specified operation. In addition, a rotated V at the clock input shows that the device changes state on an edge. Thus, if no circle is present the chip is positive edge triggered. Refer to Figure 5 for examples.

Figure 6 provides the pin numbering scheme for the header and cable connectors. Header connectors always have 2 rows of pins and 42 positions. Cable connectors always have 2 rows of pins but may vary in the number of positions.



A. NEGATIVE EDGE TRIGGERED

B. POSITIVE EDGE TRIGGERED

C. POSITIVE LEVEL TRIGGERED

Figure 5. Examples of Clocked Devices

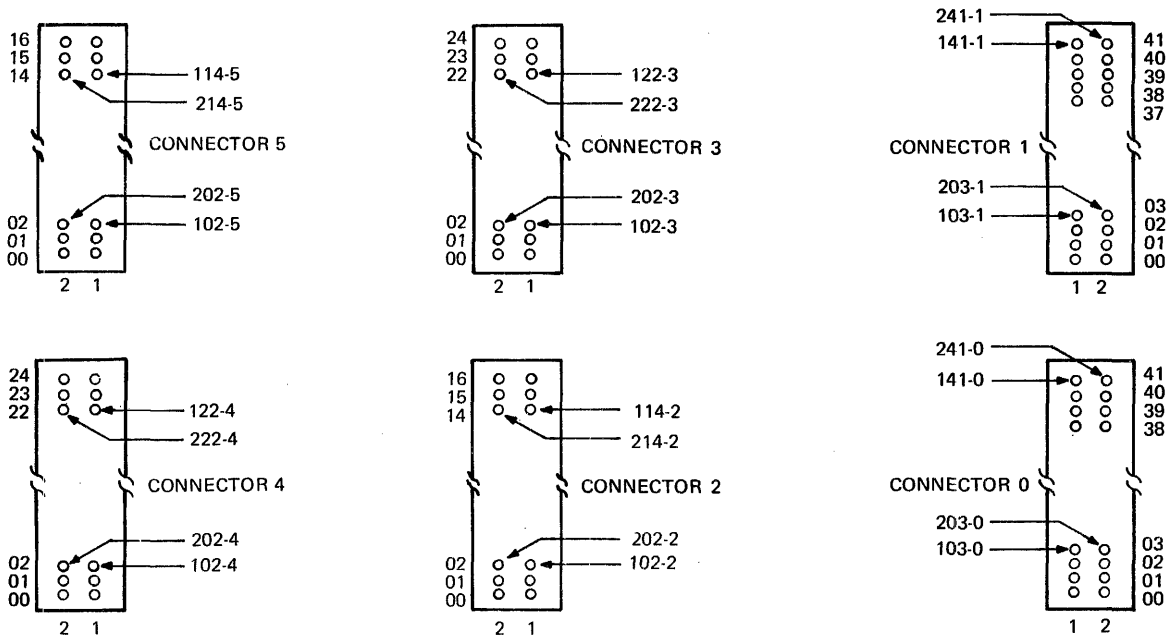


Figure 6. Connector Pin Numbering

A net is defined as an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end (usually an output where the signal is generated) and one or more terminating ends. Often it is convenient to assign descriptive mnemonic names to nets as a way of identifying them on schematics. Whether a net is named or not is sometimes arbitrary. However, a net is always assigned a name if:

1. The net is contained on one drawing sheet but is not shown as a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

If a net is named, the following rules are observed.

1. All mnemonic names are a maximum of six characters.
2. All decimal digits and upper case letters are permitted.
3. No other characters permitted.
4. Where possible, Mnemonics are descriptive. However, it should be recognized that descriptive names are not always possible and a danger of misinterpreting a Mnemonic exists.
5. Mnemonic names are not repeated within a schematic.
6. Every Mnemonic is suffixed by a state indicator. This indicator consists of the digit "1" for the logically true state, or the digit "0" for the logically false state. For example, the set side of a flip-flop would have the "1" state indicator, while the reset side would have the "0" state indicator. The state indicator for a function changes each time that function is inverted. Thus, the state indicator permits assigning the same Mnemonic to functions that are identical except for an inversion.
7. When a logical function is inverted, an inversion indicator is added after the state indicator. This allows for functionally equivalent, but electrically different nets to have the same Mnemonic name. For example, assume a signal NAME1, NAME1 may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

Sometimes a net fans-out to many sheets in a schematic. It is also possible for a net to fan-out to sheets in different schematics. In these situations, the net is assigned a mnemonic name. The net is also "zoned" from sheet to sheet to allow for properly identifying the originating and terminating ends of the net. The originating end of a net is defined as the collector at which a signal is generated. All other points to which the net connects are called terminating ends. When a lead leaves a sheet at the originating end, it is zoned to each and every sheet on which the net reappears, by indicating first the page number, followed by the schematic number that contains the page. For example, assume that the gate shown on Figure 3 is on a schematic, Sheet 20. The output NAME0, appears on Sheets 10, 12 and 18 of the schematic. Note that the schematic number is implied. When a net enters a sheet from another sheet, it is labeled, with the same Mnemonic name, and is zoned back to the originating end of the net only. Thus, on Figure 3, the ENBL1 may, however, have many other terminations in addition to the one shown. Generally, then, when a net leaves the sheet where it originates, it is zoned to every other sheet where the net terminates, while the terminating end is zoned only to the originating sheet. Note that in the Model 8/32 schematics, signals are co-ordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the Back Panel Map must be used.

When a lead leaves a logic board, it usually does so through a logic board back panel connector pin. These connector pins must be shown on the schematic even if the complete net is shown on one drawing sheet. Only the connector pin number need be indicated under the pin symbol, since the connector number itself is implied by the logic board location number in the logic symbol or in the footnote. Thus, on Figure 3, RD061 enters the logic board on Pin 114 of Header Connector 0.

Figure 7 is a typical schematic sheet with call-outs illustrating many of the conventions described in this section.

The schematic drawings for the basic Digital System and some of the more common expansions are commonly included in the rear of the appropriate Digital System Maintenance Manual. Schematic drawings for other expansions are included with the expansion or with the publications that describe the expansion.

REVISIONS
AREA NO2: ADDED 100Ω RES.
P6 | | | 12-1-72 | SS

POSITIVE EDGE TRIGGERED FLOP
PULL UP NET
TEST POINT
BACK PANEL CONNECTION
NO. CONTACT OF RELAY K1
N.C. CONTACT OF RELAY K1
P/O K1 P/O SCLR RELAY
P/O DISPLAY
CPU-LO BOARD 35-520
FRONT OR I/O CONNECTOR
TO LOCATION B5 ON SHEET 15
PULL UP NET WITH RESISTOR EXTERNAL TO THIS SHEET
+5 VDC
+15 VDC
RELAY COIL
P/O K1 SCLR RELAY
1MS TIMER
POWER FAIL F/F
PAGE REFERENCES REMAINING ON SAME PHYSICAL BOARD
MNEMONIC B150 "B" BUS BIT 15 ACTIVE STATE "0"
NO CONNECTION
PRIMARY POWER FAIL 35-448
OSCILLATOR & INITIALIZE RELAY

NOTES
ALL APPARATUS ON THIS SHEET LOCATED ON CPU-N1 BOARD 35-446 UNLESS OTHERWISE SPECIFIED

Figure 7. Functional Schematic Format Drawing

NAME	DATE	TITLE
E MCGINLEY	11-9-72	FUNCTIONAL SCHEMATIC MODEL PROCESSOR
		01-058 D08 2

APPENDIX 1
PART NUMBER CROSS REFERENCE LIST

PERKIN-ELMER PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-001	Dual 4 Input NAND DTL	861*
19-002	Triple 3 Input NAND DTL	863
19-003	Quad 2 Input NAND DTL	849
19-004	Hex 1 Input NAND DTL	837
19-005	Dual Power Gate DTL	844*
19-006	Dual Buffer DTL	832*
19-007	Flip-Flop DTL	848*
19-008	Gate Expander Dual 4 Input DTL	833*
19-009	8 Bit Stack DTL	930*
19-010	Differential Comparator LIN	710C
19-012	Dual 4 Input NAND Buffer TTL	74H40
19-013	Quad 2 Input NAND DTL	946
19-014	Dual J-K Flip-Flop DTL	855*
19-015	Hex Inverter 1 Input	74H04
19-016	Quad 2 Input NAND TTL	74H00
19-017	Triple 3 Input NAND TTL	74H10
19-018	Dual 4 Input NAND TTL	74H20
19-019	Single 8 Input NAND TTL	9007*
19-020	Operational Amplifier LIN	1709*
19-021	Quad 2 Input Power DTL	1644*
19-022	Dual J-K Flip-Flop TTL	3061*
19-023	Selected Dual Buffer 19-006 with 20-30 nanosecond delay DTL	932*
19-024	Triple 3 Input AND TTL	74H11
19-025	Dual 4 Input AND TTL	74H21
19-026	2-2-2-3 Input AND/OR TTL	74H52
19-027	4 Bit Adder TTL	7475
19-028	4 Bit Serial Adder TTL	7483
19-029	Quad Exclusive – OR TTL	7486
19-030	4 Bit Shift Register TTL	7495
19-031	One Shot TTL	74121
19-032	1 of 10 Decoder Open Collector	74145
19-033	Dual Sense Amplifier LIN	7524
19-034	Retriggerable One Shot TTL	74122
19-035	4 Bit Up/Down Counter TTL	74193
19-036	Quad 2 Input Open Collector TTL	7438
19-037	High Performance Operational Amp	748393
19-038	Dual 4 line to 1 line Mux TTL	74153
19-039	4 Bit ALU TTL	74181
19-040	4 Stage Look Ahead Carry TTL	74182
19-041	4 x 4 Register Stack TTL	74170
19-042	Dual Retriggerable One Shot TTL	74123
19-043	Quad 2 Input NAND Open Collector TTL	74H01
19-044	Hexadecimal Inverter Open Collector TTL	74H05
19-045	Dual J-K Flip-Flop TTL	74H106*
19-046	Quad RS-232C Line Driver	ML1488
19-047	Quad RS-232C Line Receiver	MC1489A

*Obsolete

APPENDIX 1
PART NUMBER CROSS REFERENCE LIST (Continued)

PERKIN-ELMER PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-048	8 Bit Shifter 24 Pin Dip	74198
19-049	1024 Bit PROM TTL	DM8587
19-050	8 Input NAND TTL	74H30
19-051	1024 Bit PROM TTL	74187
19-052	Dual 4 Input Buffer	*832
19-053	4 2-line-to-1-line Data Sel. Mux	74157/9322
19-054	Quad 2 Input NAND STTL	7400
19-055	Quad 2 Input NAND STTL	74S00
19-056	Quad 2 Input NAND Open Collector STTL	74S03
19-057	Hex 1 Input Inverter STTL	74S04
19-058	Triple 3 Input NAND STTL	74S10
19-059	Triple 3 Input AND STTL	74S11
19-060	Dual 4 Input NAND STTL	74S20
19-061	Dual 4 Input Buffer STTL	74S40
19-062	2-2-3-4 Input AND/OR Inverter STTL	74S64
19-063	Dual D Edge Triggered Flip-Flop STTL	74S74
19-064	Dual J-K Flip-Flop STTL	74S112
19-065	Quad 2:1 Mux Non-Inverting STTL	74S157
19-066	Quad 2:1 Mux Inverting STTL	74S158
19-067	4 Bit ALU STTL	74S181
19-068	4 Stage Carry Look Ahead Carry STTL	74S182
19-069	8 line to 1 line Mux STTL	74S151
19-070	4 Bit Synchronous Counter TTL	74161
19-071	Quad D Edge Triggered Flip-Flop	74175
19-072	4 Bit Left/Right Shift Register TTL	74194
19-073	Dual 4:1 Mux Tri-State TTL	8214(NAT)
19-074	8 Bit Priority Encoder TTL	9318(F)
19-075	16 x 4 Register Stack TTL	3101(INT)
19-076	1024 Bit Memory MOS	TM54062
19-077	256 Bit Memory TTL	6531(MON)
19-078	Dual 4 Input NAND Open Collector	74S22
19-079	Comparator Dual	NE521
19-080	1024 Bit PROM TTL	82S29(SIG)
19-081	Univ. Asynchronous Receiver/Transmitters	TR1042A(Western Digital)
19-082	2-2-3-4 Input AND/OR Invert Open Collector STTL	74S65
19-083	9 Bit Parity Generator/Checker STTL	82S62(SIG)
19-085	Timer	MC1555
19-086	741 C DIP Operational Amplifier	741
19-087	747 DIP Operational Amplifier	747
19-088	733 C DIP Operational Amplifier	733
19-089	Dual D Edge Triggered Flip-Flop	74H74
19-090	High Speed (710) Differential Comparator DIP	710
19-091	Retriggerable Single One Shot	9600
19-092	Negative Voltage Regulator	1463
19-093	Positive Voltage Regulator	1469
19-094	Positive Voltage Regulator	723
19-095	Linear Positive Voltage Regulator	805
19-096	First In-First Out Serial Memory 64 Word 4 Bit	3341

*Obsolete

APPENDIX 1
PART NUMBER CROSS REFERENCE LIST (Continued)

PERKIN-ELMER PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-097	Amplifier	(RES)
19-098	Quad 2:1 Multiplexor Non-Inverting	74157
19-099	Dual Sense Amplifier Inverting	75234
19-100	Dual Driver 8 Pin DIP	75452
19-101	Quad-2 Input Positive NAND Buffer	7437
19-102	6-1 Input Buffer/Buffer Open Collector	7407
19-103	1 of 10 Decoder	7442
19-104	Current Switch Memory Driver	75325
19-105	Dual Differential Driver	75114/9614
19-106	Dual Differential Receiver	75115/9615
19-107	Dual Sense Amplifier	7520
19-108	Quad 2 Input NAND	7400
19-109	Hex Inverter Buffer Driver Open Collector	7406
19-110	Hex Inverter	7404
19-111	Dual 4 Input NAND Buffer	7440
19-112	Optically Coupled Isolator	4N25
19-113	360 Dual Line Driver	75123
19-114	360 Triple Line Receiver	75124
19-115	Quad 2 Input AND TTL	74H08
19-116	Dual 4:1 Multiplexor STTL	74S153
19-117	4 Bit Magnitude Comparator STTL	74S85
19-118	Quad Bus Transceiver TTL	26S12A
19-119	Expandable AND/OR Invert TTL	74H55
19-120	Dual Timer	NE556
19-121	Matched Pair 19-085 (P.S. Timing)	MC1555*
19-122	1024 Bit PROM TTL	SEE 19-051
19-123	Dual Voltage Controlled Oscillator	74S124
19-124	4-2 Input NAND Buffer STTL	74S37
19-125	4-2 Input NAND Buffer STTL	74S38
19-126	Dual 2 Wide 2 Input AND/OR Inverter STTL	74S51
19-127	4-2 Input Exclusive OR STTL	74S86
19-128	13 Input NAND, 3-State STTL	74S134
19-129	3/8 Decoder STTL	74S138
19-130	2-4 Input NAND 50 Ohm Line Driver STTL	74S140
19-131	4D FF STTL	74S175
19-132	4 2/1 Mux STTL	74S258
19-133	4 Bit Binary Full Adder TTL	74283
19-134	Hexadecimal Buffer/Inverter TTL	8T98
19-135	4 Bit Binary Counter STTL	(98S16)
19-136	1 of 10 Decoder HS & HV	74145
19-137	Dual Peripheral Positive OR Driver 8 Pin DIP	75453 (SIG)
19-138	Character General	2513
19-139	Driver/Decoder	7447AN
19-140	8 Bit Latch	9334PCQM
19-141	Multi-Port Register	9338PCQM
19-142	1024 Bit PROM TTL	SEE 19-080
19-143	4K x 1 NMOS RAM	9050
19-144	4-Hystersic Rec	8T380
19-145	Voltage Regulator + 15 500 Milliamperes	78M15AUC
19-145F01	Voltage Regulator + 12 500 Milliamperes	78M12AUC
19-145F02	Voltage Regulator -15 500 Milliamperes	LM340T-15

*Obsolete

PERKIN-ELMER PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-146F00	Voltage Regulator -15 500 Milliamperes	79M15/LM320T-15
19-146F01	Voltage Regulator -12 500 Milliamperes	79M12/LM320T-15
19-146F02	Voltage Regulator -5 500 Milliamperes	79M05
19-146F03	Voltage Regulator -5 500 Milliamperes	7905/LM320T-5
19-147F01	8 Channel Analog Mux	H11-181A-5
19-147F02	8 Channel Analog Mux	Analog Devices A07503JN
19-148	Voltage Follower	LM310D
19-149	High Speed Op Amp	HA2-2525-5
19-150	2 Channel Analog Switch	DG1828A
19-151	Low Level Inst Amp	AD521JD
19-152	Linear Amp	BB3660J
19-153	4-2 Input NAND LPTTL	74LS00
19-154	Hex Inverter LPTTL	74LS04
19-155	3-3 Input NAND LPTTL	74LS10
19-156	2-4 Input NAND LPTTL	74LS20
19-157	8 Input NAND LPTTL	74LS30
19-158	4-2 Input NOR LPTTL	74LS02
19-159	4-2 Input OR LPTTL	74LS32
19-160	4-2 Input AND LPTTL	74LS08
19-161	3-3 Input AND LPTTL	74LS11
19-162	2-4 Input AND LPTTL	74LS21
19-163	4-2 Input NAND Schmitt Trigger LPTTL	74LS132
19-164	4-2 Input NAND Buffer LPTTL	74LS37A
19-165	2-D FF LPTTL	74LS74
19-166	2-JK FF LPTTL	74LS112
19-167	4-D FF LPTTL	74LS175
19-168	3 to 8 Decoder Demux LPTTL	74LS138
19-169	Hex Inverter Open Collector LPTTL	74LS05
19-170	4-2 Input NAND Open Collector LPTTL	74LS03
19-171	Dual Multivibrator	74LS123
19-172	4-2 Input Exclusive OR LPTTL	74LS86
19-173	8 to 1 AND/OR Invert Mux LPTTL	74LS151
19-174	4-2 Input AND/OR Mux LPTTL	74LS257
19-175	4-2 Input AND/OR Mux LPTTL	74LS157
19-176	4-2 Input Mux LPTTL	74LS258
19-177	4-1 Input AND/OR Mux LPTTL	74LS153
19-178	3-3-2-2 Wide AND/OR Inverter LPTTL	74LS51A
19-179	4-3-3-2 AND/OR Inverter LPTTL	74LS54
19-180	4 Bit Counter LPTTL	74LS161
19-181	4 Bit Up/Down Counter LPTTL	74LS193
19-182	4 Bit Left/Right Shift Register TTL	74LS194
19-183	2-Line Driver	75110
19-184	4 Bit Micro Controller	AMD2901
19-185	4K-Bit ROM	N82S115
19-186	4K-Bit PROM	82S215N
19-187	Quad 2:1 Mux with Storage LPTTL	74LS298
19-188	ROM Chip Programmed In House 16 Bit LSU	
19-189	ROM Chip Programmed In House 32 Bit LSU	
19-190	Quad Comparator	LM339
19-191	Quad 2-Input NOR Gate	CD4001AE

PERKIN-ELMER PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-192	Dual D Flip Flop	CD4013AE
19-193	1024 Bit PROM TTL	SEE 19-051
19-194	2K PROM TTL	N825131
19-195	2K PROM TTL	SEE 19-051
19-196	Quad 2 Input 3 State Mux. Non Inverting	74S257
19-197	1024 B Dynamic RAM (NMOS)	MK4096N-16
19-198	Field Programmable Logic Array	82S00
19-199F03	Field Programmable Logic Array	
19-200	16 x 4 First In-First Out (FIFO)	9430
19-201	CPU	MC6800
19-202	Peripheral Interface Adapter (PIA)	MC6820
19-203	Sync Serial Data Adapter (SSDA)	MC6852
19-204	1K RAM	MCM6810A
19-205	2 Phase Clock	MC6870A
19-206	4 Input 3 State Line Transceiver	8T26/8T26A
19-207	Error Checking, Polynomial Gen.	MC8506P
19-208	Dual VCO	MC4024P
19-210	CPU	2608-1/MCM6830P
19-213F01	5/16 Shift Control PLA	
F02	8/16E Shift Control PLA	
20-001	Transistor NPN High Speed Switch	2N3646
20-002	Transistor PNP 500 MA	MPS6534
20-003	Transistor	DT5-423/2N3902
20-004	Transistor NPN	2N5189/64493
20-005	Transistor	2N3056
20-006	Transistor NPN 15 Amps 100W T03 case	2N3055
20-007	Transistor NPN 3 Amps	TIP31A
20-008	Transistor PNP 3 Amps	TIP32A
20-009	Transistor Triac 2 Amps 100V	A03001
20-010	Transistor NPN 500 MA Code Driver	2N5845/2N5845/ 74659A
20-011	Transistor Photo	2N5777
20-012	Transistor PNP High Current Switch	2N2907/TS3413
20-013	Transistor NPN	2N3302
20-014	Transistor NPN	2N4238
20-015	Transistor PNP	2N4235
20-016	Transistor PNP	2N3740
20-017	Transistor NPN	2N3766
20-018	Transistor, Power Silicon NPN	2N3054
20-019	Transistor	2N6038
20-020	Transistor Switching 1 Amp T05 can	2N3725
20-021	Transistor NPN Silicon	MPS3646
20-022	Transistor NPN	2N1711
20-023	Transistor PNP	2N905A/J2N2905A
20-024	Transistor Switch	2N3776
20-025	PNP Hi Speed Switch	2N3467
20-026	Transistor Module, Quad	FSQ1079/FPQ3724
20-027	Transistor	2N2369
20-029	Transistor	
20-030	Transistor	HPX002
20-031	Transistor	2N3568

APPENDIX 1
PART NUMBER CROSS REFERENCE LIST (Continued)

PERKIN-ELMER PART NO.	TYPE	VENDOR/JEDEC NUMBER
20-032	Transistor NPN	SEE 2N6486 SPEC
20-033	Transistor	KE4393
20-034	Transistor	2N3904
20-035	Transistor	2N3906
20-036	Transistor	MP54356
20-037	Transistor	D45H2
20-038	Transistor	2N2520
20-039	Transistor	2N222A
20-043	MOS FET	
21-025F01	1K ohm-15 to Common DIP	898 1-1K ohm (Beckman)
21-025F02	470 ohm-15 to Common DIP	898-1-470 ohm (Beckman)
21-025F03	330 ohm-15 to Common DIP	898-1-330 ohm (Beckman)
23-001	Diode High Speed-High Current	1N4150
23-002	Diode 5.1 V Zener	1N4733A
23-003	Diode 10V Zener	1N4750A
23-004	Diode 6.1 V Zener	1N4735A
23-007	Diode Mot Bridge	MDA962-2
23-008	Diode Int. Rectifier	40HF-5R
23-009	Diode	1N4735
23-010	Diode Int. Rectifier	S1Y1P
23-011	Diode Rectifier	2N681
23-012	Diode Termistor	1D2032
23-013	Diode 9.3V	1N2163
23-014	Diode	1N3880
23-015	Diode	1N3889
23-016	Diode Bridge Rectifier	YS448
23-017	Diode	1N2070
23-018	Diode 18 V Zener	1N4746
23-019	Diode	1N3615
23-020	Diode 8.2V Zener	1N756A
23-021	Diode 9.1 V Zener	1N757A
23-022	Diode 3.3V Zener	1N746A
23-023	Diode Bridge Rectifier	KDH250
23-024	Diode, Power Fast Rec. 30 Amps	1N3909
23-025	Diode, Power Fast Rec. 3 Amps	MR841/A115A
23-026	Triac 600V 30 Amps	2N6162
23-027	Diac 32V	1N5761
23-028	Power SCR Thyristor	2N4441
23-029	Diode	1N4607
23-030	Diode	1N4156A
23-031	Diode 6.8 V Zener	1N4736A
23-032	Diode 9.1 V Zener	1N4739
23-033	16 Diode Array	45190 (Litton)
23-034R01	Switch Diode 600 ma	TSC1N4607
23-035	Diode 40A	MBA4030
23-036	Diode	MPD-400
23-037	Zener Diode 2.4V	1N4370
23-041F00	Low Voltage Zener Diode	LVA51A40114/

APPENDIX 1
PART NUMBER CROSS REFERENCE LIST (Continued)

PERKIN-ELMER PART NO.	TYPE	VENDOR/JEDEC NUMBER
23-041F02	Low Voltage Zener Diode	LVA51A22819 LVA62A22941/ LVA62A40212
23-042	Power Schottky	SD41
23-043F00	Zener Diode Avalanche 5.1V	
23-043F01	Zener Diode Avalanche 5.6V	
23-043F02	Zener Diode Avalanche 6.2V	
30-013	4.7uH Inductor	
30-013F02	1.5uH Inductor	
30-013F03	2.2 uH Inductor	
30-018	100 nanoseconds Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
30-019	50 nanoseconds Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
33-032	Hexadecimal Switch	

PROCESSOR

01-078R09A21
December 1978

METRIC

MODELS 8/32, 8/32C, AND 8/32D PROCESSORS MAINTENANCE SPECIFICATION

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MODELS 8/32, 8/32C, AND 8/32D PROCESSORS MAINTENANCE SPECIFICATION

1. INTRODUCTION

The Perkin-Elmer M83-Series 8/32 Digital Systems are low cost, general purpose systems, versatile enough to perform a wide range of industrial control, data processing, and scientific computation. The processors are well suited to the real-time scanning of hundreds of instrument readings, process alarms, and pulse trains. They are particularly useful where larger amounts of main Processor time are needed for computation.

1.1 Packaging

Each 8/32 Processor is contained in a 483 mm X 356 mm (19" X 14") RETMA Twin Chassis allowing 16 board positions. The basic Processor with 128KB of core memory in the 8/32 and 8/32C or 256KB of core memory in the 8/32D uses 12 board positions and allows four positions for I/O expansion or planned Processor options.

1.2 Processor

The current basic Processor configurations are Model 8/32C with a basic 128KB memory and Model 8/32D with a basic 256KB memory (Product Number M83-030). Other features such as parity, additional memory, etc. are optional. All references to Model 8/32 in this specification apply to the 8/32, 8/32C, and 8/32D models unless otherwise specified.

The Model 8/32 uses a technique commonly referred to as "emulation" to implement the standard Perkin-Elmer user repertoire. This technique requires a micro-processor, or sub-processor, not apparent to the user, employing one or more of the micro-instructions in sequence to implement one user level instruction. The basic micro-program is contained in 1,280 words of Read-Only-Memory (ROM). The Model 8/32 employs a 32 bit micro-instruction word and 32 bit internal bussing. The basic instruction time of the micro-processor is 260 nanoseconds per micro-instruction.

1.3 Control Store

The Model 8/32 uses 1,280 words of control store which is mounted on the CPB board. The control store may be optionally expanded by a 512 word and/or a 2,048 (2K) word Writable Control Store (WCS). Three user instructions are used for manipulating the WCS.

1.4 Peripherals

The Model 8/32 interfaces to, and is compatible with, all standard Perkin-Elmer peripheral controllers and controllers designed to the standard Perkin-Elmer Multiplexor Bus. Any number of devices up to 1,023 can be accommodated, but a maximum of 16 can be interfaced directly to the Multiplexor Bus or the Extended Selector Channel Bus.

2. INTERNAL ARCHITECTURE

The architecture of the Model 8/32 encompasses a principle of modules communicating over a common bussing system, directed by instructions from a control memory which specify the module to which an instruction is directed and the function to be performed. In theory, the function of any module is arbitrary and the significance of various instructions take meaning only when applied to a specific module. Thus, a computer achieves a capability and personality determined by what functions can be performed by its complement of modules.

2.1 Modules

The Model 8/32 architecture accommodates eight modules which communicate over four Processor busses. The basic Processor is comprised of three modules.

1. Central Processing Unit (CPA, CPB, and CPC). The CPU contains the Processor registers. This control module (module 0) controls the user memory, control memory, register gating, and sequencing of instructions.
2. Arithmetic Logic Unit (ALU). The ALU (module 1) provides the basic arithmetic/logical capability of the Processor.
3. Input/Output Unit (IOU). The IOU (module 2) provides the I/O capability of the Processor by generating the standard Perkin-Elmer Multiplexor (I/O) Bus for peripheral communications. It is capable of various byte manipulations of data presented on the buses. In addition, the I/O module contains the Display Console controller, the Teletypewriter controller, the Power monitor and the System Initialize circuits.

The architecture accommodates five additional arbitrary modules such as floating point, Boolean manipulators, or special nature designs.

2.2 Micro-Instructions

The micro-instruction word is 32-bits long. In addition to the branch and write instructions, there are three types of instructions to the modules. These minimally encoded instructions provide 112 combinations of module/function commands. The micro-instruction can simultaneously direct two operands and a result independently on three of the computer's busses; generate 12-bit immediate field operands; select the address of the next micro-instruction; perform encoded micro control of the computer's functions such as reading/writing main memory; incrementing user location and memory address registers; controlling the user status register; and decoding the next user instruction.

2.3 Interrupts

The Model 8/32 has nine hardware priority interrupts, most of which can be masked by various bits of the Program Status Word (PSW). The occurrence of a recognized interrupt causes the micro-program to trap to one of nine specific control store locations associated with the interrupts. Among the nine interrupts are four priority levels of external interrupt all of which are always available. Though available, the last three external interrupt priority levels are practical only if additional optional register sets are installed.

2.4 Registers

The Model 8/32 can have up to 8 sets of 16 general registers each. Fifteen registers in each set may be used as index registers. In addition, there are 16 floating point registers, 8 additional general purpose registers, plus 5 registers associated with the user level machine control that are available to the micro-programmer.

2.5 Processor Timing

Communications between modules are request/response. Timing is completely asynchronous (rather than quantized) to achieve maximum speeds. In addition, interlocks are provided between the control memories and the CPU to facilitate programming the micro machine. The control module operates on a 130 nanosecond clock, allowing a minimum instruction execution in 260 nanoseconds. Internal timing within the other modules can be selected to best suit the needs of the module.

3. FUNCTIONAL DESCRIPTION OF THE BASIC PROCESSOR

3.1 Processor Busses

The functional characteristics of the Processor can best be described in terms of its registers, busses and related gating. There are four busses which are the key to the modular design philosophy of the Model 8/32 architecture. Refer to Figure 1. An understanding of the bus structure is necessary to determine how each module of the Processor interrelates, and how the registers and gating of each module contribute to the function of the module it is designed to serve.

3.1.1 Control Bus (C Bus). The Control Bus of the computer is commanded by the control module and is, in essence, a reflection of that segment of the micro-instruction selecting the function and module to be addressed, plus timing to affect data transfers. Also included is a means (the CC Bus) for a module to transfer data to the Condition Code of the PSW. The Control Bus signals are described in the following paragraphs:

Module Select Lines (MSEL00:02). These three lines contain the address of a module for which the current micro-instruction is intended. One of the eight arbitrary modules can be selected by the instruction to perform some function. These three lines reflect Bits 0:2 of the micro-instruction.

Function Select Lines (FSEL00:03). These four lines reflect Bits 16:19 of the micro-instruction and normally select 1 of 16 arbitrary functions to be performed by the selected module.

Start (STRT). STRT signals the modules that data on the busses is valid. It is, in effect, a request from the control module for a response to a micro-instruction. Data is held static on the A and B Busses while STRT is active. The control module holds STRT active until it recognizes a response on the Module Finished (MFIN) line and has stored the results presented on the S Bus.

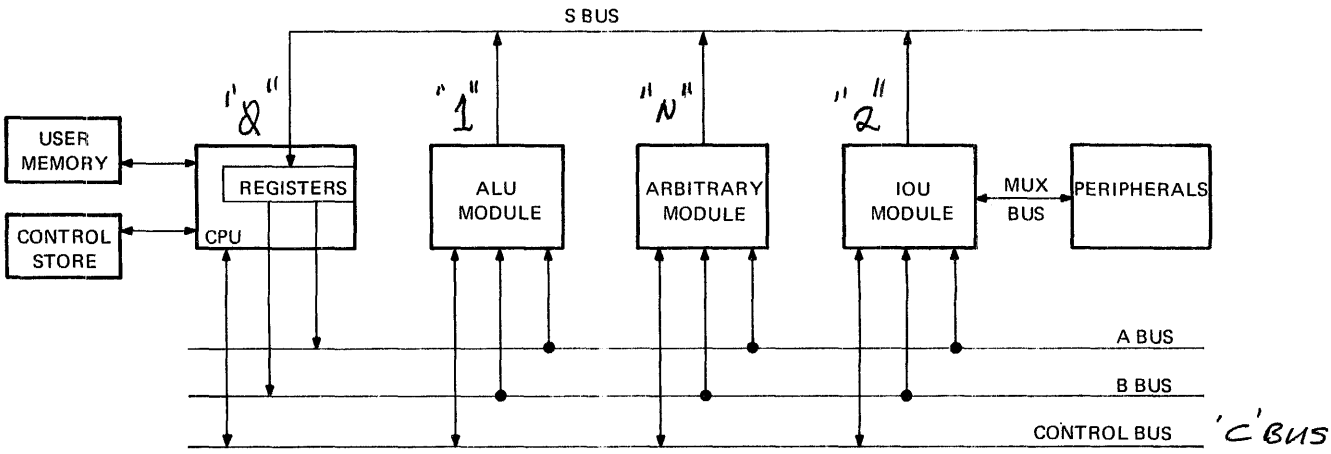


Figure 1. Model 8/32 Module Concept

Module Finished (MFIN). MFIN is a response to the control module from a selected module indicating that it has recognized STRT and completed the selected function. The selected module gates data and other responses onto the S Bus prior to returning MFIN. The data and responses must be held on the busses until the control module removes STRT. This time is indefinite and depends on events within the control module.

Module Signal (MSIG). This is a control signal manipulated by the selected module to indicate some arbitrary condition to the control module. It may be tested by the control module during a normal micro-instruction to the selected device, to control a conditional branch in the micro-program.

Condition Code Bus (SCC, VCC, CCC, GCC, and LCC). SCC signals the control module that the selected module wishes to manipulate the Condition Code of the Program Status Word. If the micro-programmer has enabled this manipulation, the Condition Code is forced to a status specified by the selected module. The status is unconditionally forced into the CPU flags. This is done concurrent with a normal instruction to the selected module. VCC, CCC, GCC, and LCC specify the status forced into CPU flags and the Condition Code of the Program Status Word, and represent overflow, carry, greater than, and less than, respectively.

3.1.2. A, B, and S Busses. The A, B, and S Busses are the primary data links between the control module and the selected module. Gating of data to/from each of these busses is controlled by the micro-instruction. Most of the registers of the control module can be gated to/from these busses.

Data is selected by the micro-instruction from two independent sources and transmitted to a selected module over the A and B Busses. The module is thus presented simultaneously with two operands. The resulting data is returned to the control module via the S Bus. The destination of the S Bus is selected by the micro-instruction.

3.1.3 Typical Bus Exchange. The use of the A, B, and S Busses can be summarized by the following example.

1. The micro-instruction selects a module (MSEL00:02) and directs it to perform some function (FSEL00:03).
2. The operands are selected from somewhere in the control module and gated onto the A and B Busses.
3. The control module informs the selected module that all data on the busses is valid and that it may begin (STRT).
4. The selected module performs the function (S) = (A) F (B) and gates the results to the S Bus.
5. The selected module may manipulate the Condition Code via SCC, VCC, GCC, LCC, and CCC.
6. The selected module activates MFIN to signal the CPU module that the operation is complete and the results are presented on the S Bus.
7. The control module recognizes MFIN, gates the S Bus to the destination specified by the micro-instruction, and then removes STRT.
8. The selected module deactivates itself when STRT is removed.

3.2 Registers

The following registers are part of the control module.

3.2.1 A Stack/B Stack. The A stack and B stack are redundant sets of register banks containing the general purpose registers of the CPU. The registers are duplicated to allow simultaneous gating of any register in the stack onto either the A Bus or the B Bus. These registers are gated onto the A and B Busses and are loaded from the S Bus under control of the micro-instruction.

3.2.2 Memory Data Register (MDR). This register provides the data buffer between the CPU and the user level memory. The MDR can be gated onto the B Bus and loaded from the S Bus under control of the micro-instruction. It is, of course, also loaded under control of the memory when a memory read cycle is requested. Hardware interlocks are employed to synchronize the memory to the CPU.

3.2.3 Memory Location Register (MLC). The MLC is a general purpose register which can be gated to the B Bus and loaded from the S Bus, and can be incremented by the length of the emulated instruction to facilitate the emulation of the user level repertoire. This register keeps track of the current instruction location of the emulated machine.

3.2.4 Memory Address Register (MAR). This register contains the address of the user memory that the micro-programmer is reading or writing. The MAR can be loaded from the S Bus under control of the micro-instruction, or incremented by four under micro-control. The least significant bit of the MAR is used to control byte steering for the byte-oriented instructions of the user repertoire (refer to I/O Section). As in the MDR, timing conflicts are resolved by hardware interlocks.

3.2.5 Program Status Word (PSW). The Program Status Word is an 18-bit register which may be gated onto the A Bus and loaded from the S Bus under control of the micro-instruction. Various bits of the PSW are used to enable associated hardware interrupts. PSW Bits 28:31 contain the Condition Code of the user level computer. These bits may be compared and tested against corresponding bits of the user instruction under Module 0 micro-instructions to emulate user branch instructions. In addition, they can be manipulated by any module designed to do so, if they are enabled by the micro-programmer.

3.2.6. User Destination Register, User Source Register (YD, YS). These two control registers store Bits 08:11 and 12:15 respectively, of the current user level instruction being emulated, and allow the micro-programmer to indirectly reference the general registers selected by the user instruction. The YD is compared to the PSW Condition Code on certain micro-instructions to emulate user level branches. These registers can be examined by gating them onto the A and B Busses under micro-instruction control. The YD can also be loaded from the S Bus.

3.2.7 User Instruction Register (UIR), Memory User Destination Register (UDR), and Memory User Source Register (USR). These three registers are loaded with Bits 0:7, 8:11, and 12:15, respectively, of the next user level instruction to be emulated. The 8-bit op-code stored in the UIR is used to vector to the emulation sequence for the next user instruction. It is also used to interrogate a ROM which has been configured to decode privileged and illegal user level instructions. The contents of the UDR and USR are transferred to the YD and YS at the beginning of the next emulation.

3.2.8 ROM Location Register (RLR). This register stores the current address of the control store instruction. It is loaded from the ROM Address Gates (RAG) at the beginning of every instruction except interrupt trap instructions and execute type instructions (explained in the section on micro-programming). The RLR is a 12-bit register allowing direct addressing of the control store up to 4K instructions.

3.2.9 ROM Instruction Register (RIR). This 32-bit register stores the current micro-instruction. The RIR is the focus of control of the CPU.

3.3 Interrupts

The hardware of the computer provides nine priority interrupts. Each interrupt has a unique control store trap location associated with it. Recognition of an interrupt causes the micro-instruction stored at its respective trap location to be performed. The RLR contents are preserved to allow the address of the interrupted sequence to be saved, if desired, so that control can be returned at the completion of the interrupt routine. Certain interrupts are enabled/disabled by bits of the PSW.

3.4 Control Store Memory

128KBits

The Model 8/32 can accommodate a maximum of 4K x 32 bits of control store memory. The computer allows data as well as instructions to be retrieved from its control memory. This capability expands its versatility by allowing data such as sine tables, translation tables, and matrices to be stored and operated upon efficiently by the micro-programmer.

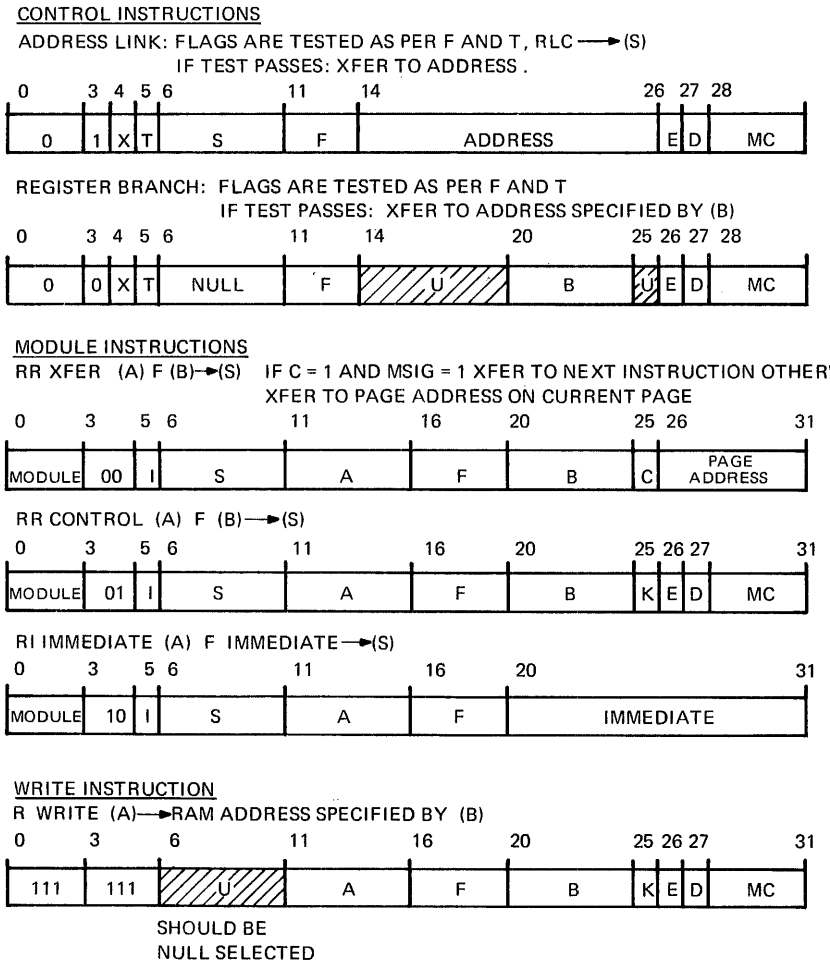
On models so equipped, the Processor can alter its control store (write into its memory). This capability to store and retrieve data provides the power of a hardware computer at micro-instruction speeds.

3.5 Micro-programming

The control store of the Model 8/32 is a 32-bit word memory which may read indirectly by an instruction to retrieve data, and may be written into by an instruction if it is a writable memory. The Model 8/32 contains a 1,280 x 32 ROM array containing the user repertoire and support programs.

The basic instruction format provides the computer with a three address capability, but various options of the repertoire can modify this to range from two to four. Figure 2 displays the different types of instructions and their modifiers.

The format of the micro-instruction specifies which module is to be addressed, allowing only one module of the computer to be addressed at any one time. All other modules must ignore the communications in process. Bits 0:2 of the instruction selects the module to which the instruction is addressed.



A SELECTS REGISTER GATE TO A BUS
B SELECTS REGISTER GATED TO B BUS
S SELECTS REGISTER TO RECEIVE S BUS
F SELECTS FUNCTION OF ADDRESSED MODULE
E ENABLE SETTING OF CONDITION CODE
C IF SET TRANSFER IS CONDITIONAL
I B FIELD IS INDIRECT ADDRESS OF DATA
D DECODE NEXT INSTRUCTION
K FSEL EXTENSION
U UNUSED
T TESTED F FIELD FOR THE "TRUE" CONDITION
X EXECUTE

MC FIELD DESIGNATIONS (MEMORY CONTROL)

0000	NO MEMORY ACTION
0001	INCREMENT MLC BY INSTRUC. LENGTH
0010	PRIVILEGED WRITE HALFWORD
0011	DATA WRITE HALFWORD
0100	NOT USED
0101	INCREMENT MAR BY 4; WRITE DATA F W
0110	PRIVILEGED WRITE FULLWORD
0111	DATA WRITE FULLWORD
1000	READ HALFWORD AND SET BIT
1001	INCR. MLR BY INSTR. LENGTH; READ INSTR.
1010	PRIVILEGED READ H W
1011	DATA READ HALFWORD
1100	INSTRUCTION READ
1101	INCREMENT MAR BY 4, READ DATA F W
1110	PRIVILEGED READ F W
1111	DATA READ FULLWORD

Figure 2. Control and Module Instructions

3.5.1 Module 0. Module 0 addresses the control module. As shown in Figure 2, instructions are interpreted differently for Module 0 than the others. In the normal sequence of instructions (e.g., no branches), the hardware of the control module controls the reading of its memories, and gates the registers specified by the instruction. When it is addressed by an instruction, it is for the purpose of a conditional transfer. Module 0 does not manipulate the Condition Code or Processor flag register.

Branch/Execute Instructions. There are two types of transfers recognized by Module 0. The most common is the Branch. The Branch (BR) instruction conditionally transfers control of the CPU to a specified address of control memory and proceeds sequentially from there. The second type of transfer, commonly called an execute, transfers control to a single instruction at a specified address of control memory, then normally returns to the original sequence. Any type of instruction may be executed including additional execute instructions to any depth. However, an execute which results in a branch does not return to the continuing sequence. Bit 04 of the instruction determines whether the instruction is a branch or execute type.

Address Link/Register Return. There are two types of Module 0 instructions: address link and register return. They are selected by the state of Bit 03 of the instruction.

The linked transfer is similar in function to the user level Branch and Link (BAL) instruction, and can be used to transfer to subroutines when they may be entered from more than one location. The location of the next sequential instruction, following the transfer, is deposited in the register specified by the Link field of the instruction (Bits 11:15), and a transfer is conditionally executed to the effective address.

When the address link is selected, the transfer address is specified by Bits 14:25 of the instruction.

The register return is used when the transfer address is contained in a register. In this instruction, a branch is taken to the location contained in the register specified by Bits 20:24.

Conditional Branches. All transfers are conditional upon a state selected by the F field and T field of the instruction. By selective coding of the F field, either the Condition Code of the user level machine or the status of the CPU can be tested. The codes are shown in Table 1.

TABLE 1. FUNCTION CODES FOR CPU INSTRUCTIONS

X	T	F	MNEMONICS	OPERATION
0	0	110	BAL	Branch and Link Unconditional
0	0	111	BALA	Branch and Link and Arm Interrupts
0	1	111	BALD	Branch and Link and Disarm Interrupts
0	0	000	BALZ	Branch and Link on CPU Zero
0	1	000	BALNZ	Branch and Link on Not CPU Zero
0	0	001	BALL	Branch and Link on CPU Less
0	1	001	BALNL	Branch and Link on CPU not Less
0	0	010	BALG	Branch and Link on CPU Greater
0	1	010	BALNG	Branch and Link on CPU not Greater
0	0	101	BALV	Branch and Link on CPU Overflow
0	1	101	BALNV	Branch and Link on No CPU Overflow
0	0	100	BALC	Branch and Link on CPU Carry
0	1	100	BALNC	Branch and Link on no CPU Carry
0	0	011	BALF	Branch and Link if the logical product of user M1 field and User's CC is Zero
0	1	011	BALTF	Branch and Link if the logical product of user M1 field and User's CC is not Zero
0	1	110	BDC	Branch & Mask Console interrupt (no real branch is performed)

3.5.2 Non-CPU Instructions. As stated previously, when the module number is not zero, the CPU does not operate on the instruction, and the fields are interpreted differently. The module field (Bits 0:2) and the F field (Bits 16:19) are interrogated individually by the other modules. There are four types of non-CPU instructions selected by Bits 3 and 4 of the instruction. They are:

1. RRX. The RRX is a Register-to-Register and Transfer instruction. It is effectively a four-address instruction in that it gives the register address of the two operands, the register address for the results, and the location for the next sequential instruction.

   The two operands are addressed by the A field (Bits 11:15) and the B field (Bits 20:24). The contents of these two registers are gated, respectively, to the A Bus and B Bus of the computer.

   The S field (Bits 6:10) selects the destination register to which the results are gated from the S Bus.

   The page address field (Bits 26:31) selects the low order address of the next instruction. The high order bits are taken from the current location address. The C field (Bit 25) being true makes the transfer conditional upon a signal returned by the addressed module at the completion of the instruction. (The ALU, for example, returns the Carry flag as its signal.) If the module signal, which is designated MSIG, is true, and Bit 25 of the micro-instruction is true, the branch does not occur, and the next sequential instruction is executed. Any other condition causes the transfer to be effected.

2. RRC. The RRC is a Register-to-Register Control type instruction. The interpretation of the instruction fields is identical to that of the RRX, with the exception of Bits 25:31 which contained the page address within a RRX instruction. Bits 25:31 of the RRC instruction provide the micro-control of the CPU and are described in Section 3.5.3.

3. RIM. The RIM instruction provides an immediate field for ease of generating constants and bit masks. Immediate, is the term generally used to infer that the immediate contents is the actual operand rather than the address where the operand is found. This 12-bit immediate field (RIR 20:31) is converted to a 16-bit operand by extending the sign bit (RIR 20) when gating onto the B Bus. The S field and A field of the instruction are interpreted identically to that of the RRX and RRC instructions.

4. RWT. The RWT is the Store or Write instruction of the repertoire if the CPU is equipped with an optional writable control store. There are several notable differences pertaining to this instruction.

   -Although the module number cannot be zero, it may be any other, as the CPU never communicates with the other modules.

   - The S field is not interpreted and should be null selected.

   - The F field is not interpreted.

   - The B field addresses the register containing the address to be written into.

   - The A field addresses the register containing the data to be stored in control store.

   Bits 25:31 of the RWT instruction are interpreted as a control field, as in a RRC instruction.

3.5.3 Micro-Control (MC). To facilitate the emulation task of the CPU, certain instructions allow an order of micro-control within the CPU. The instructions possessing this capability are the Module 0 (RRC and RWT) instructions.

MC Field. The MC field is the user memory micro-control which allows various controls over the user memory instruction Location Counter (MLC), the user Memory Address Register (MAR), and the reading and writing of the user memory. The significance of the bits of the MC field are shown in Table 2.

There are certain hardware connotations to the MC operations which are not made apparent by Table 2. They are:

1. The micro-control specified by the MC field is conditional when used within Module 0 instructions. The read memory is only effected if the operation does not result in a transfer. (This conditioning is used to expedite the emulation of the user branch instruction.)

2. All of the micro-control is effected before the STRT occurs with the exception of data read and data write. This control is effected after completion of the instruction, which allows the micro-programmer to use the MAR or MDR as a destination and begin a read/write data immediately. It also allows the execution of the increment and the addressing of the MAR as the destination register simultaneously, which has functional utility.

D Field (Decode Instruction). The D field bit informs the CPU to halt the sequential flow of micro-instructions and begin to emulate the next user instruction. The Operation-Code (op-code) field of the new user instruction is in the UIR and provides a vector to a control store address where the emulation sequence begins. This implies that the micro-programmer must have done an instruction read in the current or a prior instruction using one of the proper MC field designations. The execution of a decode is conditional when used within Module 0 instructions, and, like the instruction fetch, is only performed if the operation does not result in a transfer.

E Field. This field is used to Enable (E) or disable changing of the Condition Code (CC) of the PSW. When changing is enabled, the Condition Code is changed under control of the module addressed until again disabled by this field. (The ALU, for example, jams its C, V, G and L flags into the Condition Code upon completion of its function.) The meaning of the Condition Code is a function of the module addressed. Flags are disabled at the beginning of an emulation sequence.

K Field. The K field of the micro-instruction is an extension of the F field of the instruction. It is available only on the RRC and RWT instructions and constitutes the Control Signal (KSIG) to the modules. Its meaning, just as the F field, is defined by the module addressed by the current RRC instruction. The ALU, for example, reinterprets shifts to be halfword when KSIG is active. It is also used to extend the functions of the I/O module.

TABLE 2. MC FIELD

BITS				MEANING	
28	29	30	31		
0	0	0	0	No Action	
0	0	0	1	IL	Increment LOC by Instruction Length
0	0	1	0	PW2	Privileged Write Halfword (two bytes)
0	0	1	1	DW2	Data Write Halfword
0	1	0	0	No Action	
0	1	0	1	I4DW4	Increment MAR by 4, Data Write Fullword
0	1	1	0	PW4	Privileged Write Fullword
0	1	1	1	DW4	Data Write Fullword
1	0	0	0	RAS	Read Halfword and Set Sign Bit
1	0	0	1	ILIR	Increment LOC by Length and Read Instruction
1	0	1	0	PR2	Privileged Read Halfword
1	0	1	1	DR2	Data Read Halfword
1	1	0	0	IR	Instruction Read
1	1	0	1	14DR4	Increment MAR by 4, Data Read Fullword
1	1	1	0	PR4	Privileged Read Fullword
1	1	1	1	DR4	Data Read Fullword

IL — The Location Counter (LOC) is incremented by the length in bytes of the last user level instruction fetched.

PW2 — The Memory Access Controller (MAC) is disabled and the halfword in MDR (Bits 16:31) is written into the addressed location.

DW2 — The halfword in MDR (Bits 16:31) is written into the addressed location. MAC is not disabled.

I4DW4 — The Memory Address Register (MAR) is incremented by four, then the fullword in MDR (Bits 0:31) is written into the location addressed by MAR.

PW4 — The MAC is disabled and the fullword in MDR (Bits 0:31) is written into the addressed location.

DW4 — The fullword in MDR (Bits 0:31) is written into the addressed location.

RAS — The halfword at the addressed location is read then re-written with Bit 0 of the halfword set. The original value of the halfword replaces MDR Bits 16:31. Bits 0:15 of the MDR are set equal to Bit 16 of MDR (sign extension).

ILIR — LOC is incremented by the length in bytes of the last user instruction fetched, then an Instruction Read is started from the address specified by the new value of LOC.

PR2 — The MAC is disabled and the halfword at the addressed location is read and copied to MDR Bits 16:31. Bits 0:15 of MDR are set equal to MDR Bit 16.

DR2 — The halfword at the addressed location is read and copied to MDR Bits 16:31. Bits 0:15 of MDR are set equal to MDR Bit 16.

IR — An Instruction Read is started from the memory address specified by LOC.

I4DR4 — MAR is incremented by four, then the fullword at the location addressed by the new value of MAR is read and copied to MDR.

PR4 — MAC is disabled, then the fullword at the location addressed by MAR is read and copied to MDR.

DR4 — The fullword at the location addressed by MAR is read and copied to MDR.

3.5.4 Control Store Data Storage. Data may be retrieved from the ROM or the Writable Control Store (WCS) during execution of RRC, RRX, or RIM instructions when the I field bit (instruction Bit 5) is true. When the I field bit is set, the data addressed onto the B Bus is used as the store address of the ROM or WCS, and causes the CPU to replace this data with the addressed data before signaling the addressed module to begin its task.

3.5.5 Interrupts. The hardware of the computer provides nine priority interrupts. Each interrupt has a unique trap location associated with it. Recognition of an interrupt causes the instruction stored at its respective trap location to be performed. The RLR contents are preserved to allow the address of the interrupted sequence to be saved, if desired, so that control can be returned at the completion of the interrupt routine. Certain interrupts can be disabled by bits of the PSW as designated in Register Peculiarities and Tables 3 and 4. In addition, all interrupts can be enabled/disabled as a group by a micro-instruction. All interrupts not masked by PSW bits are interrogated when a new user level instruction is decoded, regardless of the status of the group enable. The group enable is automatically disabled at the beginning of a user emulation, and must be enabled by instruction if the programmer wishes to recognize interrupts. Tables 3 and 4 list by priority the pertinent information for each interrupt.

TABLE 3. INTERRUPT TRAPS

INTERRUPT	TRAP ADRS (HEX)	MASK	GROUP ENABLE
Memory Access Controller (Instruction)	1FE	PSW21	NO
Memory Access Controller (Data)	207		
Primary Power Fail	206	NONE	YES
Machine Malfunction	205	PSW18	YES
Display Panel	204	NONE	YES
External Interrupt Level 0	203	See Table 3	YES
External Interrupt Level 1	202		
External Interrupt Level 2	201		
External Interrupt Level 3	200		
Illegal Instruction	208	NONE	N/A
Privileged Instruction	208	PSW23	N/A

PSW Bits 17 and 20 define the external Interrupt enable status of the Processor as shown below:

PSW BITS		
17	20	
0	0	All Levels Disabled
0	1	Higher Levels Enabled
1	0	All Levels Enabled
1	1	Current and Higher Levels Enabled

where the current level is a function of the currently active register set. See Table 4.

TABLE 4. EXTERNAL INTERRUPT ENABLE

PSW BITS					EXTERNAL INTERRUPT ENABLED			
17	20	25	26	27	LEVEL 0	LEVEL 1	LEVEL 2	LEVEL 3
0	0	X	X	X	NO	NO	NO	NO
0	1	0	0	0	NO	NO	NO	NO
0	1	0	0	1	YES	NO	NO	NO
0	1	0	1	0	YES	YES	NO	NO
0	1	0	1	1	YES	YES	YES	NO
0	1	1	0	0	YES	YES	YES	NO
0	1	1	0	1	YES	YES	YES	NO
0	1	1	1	0	YES	YES	YES	NO
0	1	1	1	1	YES	YES	YES	NO
1	0	X	X	X	YES	YES	YES	YES
1	1	0	0	0	YES	NO	NO	NO
1	1	0	0	1	YES	YES	NO	NO
1	1	0	1	0	YES	YES	YES	NO
1	1	0	1	1	YES	YES	YES	YES
1	1	1	0	0	YES	YES	YES	YES
1	1	1	0	1	YES	YES	YES	YES
1	1	1	1	0	YES	YES	YES	YES
1	1	1	1	1	YES	YES	YES	YES

3.5.6 Registers. The basic CPU has up to 8 sets of general registers each containing 16 user registers, 16 floating registers, and 8 general purpose registers for use by the micro-programmer. In addition, the bulk of the remaining CPU registers is also available to the micro-programmer.

A register is available to the micro-programmer if he can address it to one or more of the internal busses. Table 5 tabulates the addressable registers and their respective address on the designated bus. Also listed are register mnemonics, descriptions, and the register peculiarities.

TABLE 5. REGISTER ADDRESSING

BUS ADDRESS (HEX)	S BUS	B BUS	A BUS
00:0F (16 General Registers)	URn	URn	URn
10:17	MRn	MRn	MRn
18	YS	YS	YS
19	YD	YD	YD
1A	MLC	MLC	YX
1B	MDR	MDR	YDP1
1C	MAR	EFFECTIVE ADDRESS	
1D	PSW	YSI YD	PSW
1E	YDI	YDI YSI	
1F	NULL	NULL	NULL

Register Mnemonics and Descriptions.

MNEMONIC	REGISTER	COMMENT
UR	User General Registers	16 registers manipulated by emulated language
MR	Micro-level General Registers	8 additional GP registers available to the micro-program
PSW	Program Status Word	16 bit register containing interrupt enables and flags
MDR	Memory Data Register	
MLC	Memory Location Counter	Location Counter of emulated program
MAR	Memory Address Register	
NULL	No register selected	Gates 0 to A and B Busses, S Bus data is lost
YS	User Source Register	Register selected by Bits 12:15 of emulated instruction (contents of USR)
YSI	User Source Register Immediate	Bits 12:15 of the emulated instruction (USR) gated onto B Bus
YX	User Index Register	Same as YS except NULL gated to A Bus if field is 0 (contents of USR=0)
YD	User Destination Register	Register selected by Bits 8:11 of emulated instruction (contents of UDR)
YDI	User Destination Register Immediate	Bits 8:11 of the emulated instruction (UDR) gated onto the A Bus
YDP1	User Destination Register Plus 1	Register selected by Bit 8:11 of emulated instruction +1 (must be odd)
YDI	User Destination Register Immediate	S Bus 28:31 replaces UDR contents

Register Peculiarities. The last four bits of the PSW contain the Condition Code of the emulated computer. In general, these bits can be manipulated by any addressed module unless the PSW is the S Bus destination or their change has been inhibited by the micro-instruction. The individual bits of the PSW which have hardware implications are:

PSW 17, 20, 25:27	ATN interrupt enable and level selection
PSW 18	Machine Malfunction enable
PSW 23	Privilege instruction/Memory Protect enable
PSW 25:27	User register set selection
PSW 28	C flag of Condition Code
PSW 29	V flag of Condition Code
PSW 30	G flag of Condition Code
PSW 31	L flag of Condition Code

The following additional registers have the indicated capabilities and connotations.

1. The MDR receives data asynchronously from memory. It is used in the address calculation for RX3 instructions.

2. The MDR, MAR, and MLC being addressed cause the Processor to interlock with memory when they are the source or destinations of the current instruction and the Processor is requesting memory service.

3. The MAR and MLC can be incremented by the micro-control.

4. The MLC is used in the address calculation for RX2 instructions.

3.5.7 CPU Flags. The CPU contains a flag register which is independent of the PSW flags and is manipulated by any module which attempts to affect the PSW Condition Code by activating the SCC control line of the CPU Control Bus. When the SCC control line is active, the state of the VCC, CCC, GCC and LCC are unconditionally jammed into the CPU flag register and conditionally into the PSW Condition Code. The changing of the PSW is controlled by the micro-programmer by the E field of the micro-instruction. The state of the CPU flags can be individually tested by the Module 0 instructions.

3.5.8 Arithmetic Module (ALU) Programming. The Arithmetic Logic Unit (ALU) in all 8/32 processors is optionally capable of performing both fixed point arithmetic and logical operations and single precision floating point arithmetic operations. The 05-058F01 micro program of the basic 8/32 permitted the user to address the ALU as Module 1 for fixed point operations, or as Module 3 for single precision floating point operations. The 05-058F02 micro-program of Models 8/32C and 8/32D, however, normally permits the user to address the ALU only as Module 1 for fixed point operations. All single and double precision floating point operations are available through the optional DFU unit. If the optional DFU is present, it is addressed as Module 6; if two optional DUFs are present they are respectively addressed as Modules 6 and 4. For information concerning the DFU, see the 8/32 DFU Instruction Manual, publication number 29-538. In Models 8/32D, the Module 3 single precision floating point facilities of the ALU may be made available for special purposes through the use of the optional Writable Control Store (WCS). See Appendix 1 of this specification for more information concerning Module 3 operations. The discussion of the ALU in this section is directed only to its fixed point operations. The ALU is capable of performing 15 operations. Refer to Table 6. Communication with the ALU is asynchronous. By design, the ALU is never busy and for the majority of ALU functions, response is within 130 nanoseconds. (This allows most ALU referenced instructions to be completed in 260 nanoseconds.)

TABLE 6. MODULE 1 OPERATION

F FIELD				MODULE 1 (FIXED POINT)
0	0	0	0	Subtract
0	0	0	1	Add
0	0	1	0	Subtract with Carry
0	0	1	1	Add with Carry
0	1	0	0	Not used
0	1	0	1	Logical AND
0	1	1	0	Logical Exclusive OR
0	1	1	1	Logical OR
1	0	0	0	*Logical Shift Right
1	0	0	1	*Logical Shift Left
1	0	1	0	Rotate Right
1	0	1	1	Rotate Left
1	1	0	0	*Arithmetic Shift Right
1	1	0	1	*Arithmetic Shift Left
1	1	1	0	Signed Multiply
1	1	1	1	Signed Divide

* When used in conjunction with the K bit of the RRC instruction, shifts are halfword (16 bits).

For functions which require more than one ALU cycle (i.e., shifts, rotates, and multiply/divide), the ALU does not respond with a finish signal until the completed results are on the S Bus.

Multiply/divide can be performed only on the 32 general registers and must address the same register pair on both the A and S Busses. The same restrictions that apply to these operations at the user level must be adhered to at the micro level.

A user emulated multiply/divide instruction is micro-coded by selecting the ALU (Module 1); addressing the UDR on the S Bus, the UDRP1 onto the A Bus, the USR onto the B Bus, and the required function code for the operation. When the ALU signals its completion, the results have already been deposited in the UDR.

To implement a shift or rotate instruction, the register to be manipulated is addressed onto the A Bus, the shift count is put onto the B Bus (27:31), and the S Bus is gated to the destination register.

The ALU generates valid CPU flags for all instructions except multiply/divide. The C flag is gated as MSIG.

3.5.9 I/O Module Programming. The I/O module performs a multiplicity of functions. In general, it is addressed to communicate with the multiplexor channel through the multiplexor bus. It has the additional capability of performing byte manipulations for the CPU both in conjunction with an I/O exchange and without one. Furthermore, the I/O module contains the Machine Control Register (MCR) which stores machine trouble conditions and interrupts the CPU. The contents of the MCR can be sensed, tested and cleared. Module Number 2 has been assigned to the I/O module.

Multiplexor Channel. The Multiplexor Channel, generated on the I/O module, is operationally identical to the standard Perkin-Elmer Multiplexor Bus in all respects. The Multiplexor or Bus is a byte or halfword-oriented I/O system which communicates with up to 255 peripheral devices.

A single instruction from the CPU contains the device address, the encoded function, and up to 16 bits of output data when needed. The Multiplexor Bus generator provides single or multi-cycle operation to address the device, transmit the decoded function, send or receive over 16 bi-directional data lines, and synchronize the exchange.

The normal byte or halfword operation consists of an address cycle and a data cycle. However, during a Read/Write block sequence, the address cycle is not used. For halfword functions (RDH/WDH) with a byte oriented device controller, two data cycles are used to transfer the halfword.

Byte Manipulation. The I/O module has the capability of performing byte manipulation both in conjunction with an I/O operation and without one. The byte steering is under control of the least significant memory address bit in the MAR and also the KSIG line. For halfword operations, this manipulation is inoperative but the double data cycle with packing/unpacking results when the Halfword (HW) Test line is inactive.

I/O Module Function Codes. The encoded I/O module functions and the byte manipulations are described in Section 3.7.3.

Machine Control Register (MCR). The Machine Control Register (MCR) consists of four flip-flops, four straps, and the Console Attention (CATN) and SNGL leads from the Display controller. MCR bit assignments are:

BIT	MNEMONIC	MEANING
15	EPF	Early Primary Power Fail
14 (8/32C, 8/32D)	~~DMPF~~	Data/Instruction Memory Parity Fail
(14 8/32 only)	IRLMP	Instruction Read Local Memory Parity Fail
(13 8/32 only)	DMPF	Data Memory Parity Fail
13 (8/32C, 8/32D)	---	Unused
12	IA/STF	Illegal Address and/or Start Timer Fail
11	STF	Starter Timer Fail
10	CATN	Console Attention flip-flop (from Display Controller)
09	RSET	Register Sets Available
08	spare	spare (strap)
07	SNGL	SNGL flip-flop (from Display Controller)
05	HWCRC	Hardware Assist CRC option (strap)
04	DFU	DFU option (strap)
06	MCR061	INIT Button is being depressed

On the basic Model 8/32, the IRLMP flip flop stores the signal received from the Local Memory Interface (LMI), and the DMPF flip flop stores the signal received from the Memory Bus Controller (MBC). On Models 8/32C and 8/32D, the DMPF flip flop (bit 14) stores signals received from the MBC. Signals to get the EPF and STF bits are generated on the IOU board by the Power Monitor and Statt Timer circuits. The composite bit (MCR12) can be strapped to represent IA, STF, or both. MCR11 is always set by STF. The testable straps are wired for logical ONE or ZERO as required. A Machine Malfunction (MMF) interrupt is generated when any of Bits 12, 13, 14 or 15 are true. The SMCR function gates MCR12:15 to the CC Bus, MCR08:15 to S08:15, and MCR04:05 to S04:05. The CMCR operation clears MCR11:15 where there are ONES in B11:15. This permits selective clearing of some bits while the rest of the MCR continues to monitor other machine functions without loss of data.

Start Timer (STRT). A 35 microsecond timer is started by the STRT signal and cleared by the MFIN signal from any selected module. Should the timer run out before the MFIN signal arrives, a malfunction exits; i.e., non-existant module, circuit trouble, or no SYN return from the Multiplexor Channel. If a D Bus function was called for, the False SYNC code (0100/CVGL) is placed on the CC Bus and a pseudo MFIN signal is sent to restart the CPU clock. Also, if the function required is of the Sense Status type, X'04' replaces the proper byte as determined by CA311, and the other byte is gated to the S Bus unchanged. For a non-D Bus operation, the Start Time Fail (STF) bit is set in the Machine Control Register (MCR11), and a pseudo MFIN signal is sent to restart the CPU clock. If STF is strapped into MCR12, the MMF interrupt is also generated.

3.6 Processor Block Diagram Analysis

3.6.1 CPU (Figure 3). The architecture of the Processor is structured about four busses which provide intercommunication between the CPU and the remaining modules.

The CPU selects the module via the Control Bus (C Bus), specifies the function, and signals that data is available on the A and B Busses. The addressed module signals when it has completed its function and transmits flag type data back over this bus.

The A Bus and B Bus contain the two operands offered simultaneously to the addressed module to be manipulated. Most of the CPU registers can be gated onto the A and B Busses.

Data from an addressed module is returned to the Processor via the S Bus.

The ROM Instruction Register (RIR) is a 32-bit register that latches the current instruction read from the control store memory to provide the control gating for each instruction. Data can also be gated from the RIR onto the B Bus for indirect data fetches. One of the many functions performed by the encoded instruction is register gating. This is performed by the select logic to encode the A, B, and S SEL lines, these lines determine which registers are gated onto the A and B Busses, and which register is the S Bus destination.

The Control Store Address gates (CSA) select the address of the control store to be interrogated next. Inputs to the CSA may be the ROM Location Counter (RLC) to select the next instruction, certain bits of the RIR for branching, the B Bus for indirect addressing or branches, the translated vector for the next user instruction to be emulated (XLTR), or interrupt trap address from the interrupt logic.

The ROM Location Register (RLR) preserves the address of the current instruction. It is loaded with the address of the current instruction every time the RIR is loaded, except when the instruction is an interrupt or execute type which do not alter the ROM Location Register. The RLR is gated to the RLC to perform RLR+1 for the next sequential instruction.

The general register sets and the 8 general micro-registers are contained in the A stack and B stack. This is a redundant pair of register stacks, implemented as such to allow gating of any two registers of the machine simultaneously onto both the A Bus and B Bus. Gating of these stacks is controlled by the A, B, and S SEL lines, just as the other A, B, and S source and destination registers.

The Program Status Word register (PSW) is an architectural feature of the user level machine. Certain bits of the PSW are used to mask interrupts, control the privileged mode of the Processor, and to contain the Condition Code of the user level program. This register can be gated to the A and from the S Busses. The Condition Code portion can also be loaded independently of the register addressing.

The Memory Location Counter (MLC) aids the emulation capability of the Processor. It is used to contain the memory location of the current user level instruction. In addition to being capable of being gated to/from the B and S Busses, this register may be incremented by the length of the last emulated user instruction under micro-control of the programmer.

The Memory Address Register (MAR) contains part of the address to be used by the main memory for a read/write operation. This register can be loaded from the S Bus, and may also be incremented by micro-control of the programmer. The manipulation of this register is interlocked with the memory operation by hardware to remove timing restraints from the micro-programmer.

The Memory Data Register (MDR) is loaded from the S Bus with data to be written into the main memory, or it is loaded from the Memory Data Bus with the contents of the addressed memory on a memory read operation. This register may be gated onto the B Bus of the Processor, and, like the MAR, hardware interlocks remove the timing considerations of the memory system from the micro-programmer when this register is referenced.

The User Instruction Register (UIR) stores the 8-bit op-code of the next user instruction to be emulated. It is loaded from memory when a Read operation is designated as an instruction fetch by the micro-code. The 8-bit op-code is translated to a vector which designates the beginning address of the emulation sequence for a particular instruction. The 8-bit op-code is also gated to a Privileged/Illegal ROM which is coded to detect these types of instructions and cause an interrupt to the Processor.

The memory User Destination Register (UDR) and memory User Source Register (USR) store the destination and source fields of the next instruction to be emulated when it is read from memory. This data is transferred to the User Destination Register (YDR) and User Source Register (YSR) at the beginning of a new emulation sequence to provide residual control for the instruction.

Memory Control is effected by the micro-control field of the micro-instruction. The ability is provided to cause data read, data write, and instruction read.

3.6.2 ALU. The ALU is a standard module of the Model 8/32 and provides the basic arithmetic/logic capability. It communicates with the CPU over the A, B, S, and C Busses in a manner identical to other modules.

The ALU becomes active when it recognizes its address on the Control Bus (Module Number 1), and the CPU signals start (STRT). The function to be implemented is determined from the Control Bus.

ALU functions may be of two types. The simple functions (add/subtract and logical) cause the ALU to immediately return a Module Finished signal (MFIN). For these type of instructions, the A and B Busses are gated through the ALU, and the required function is performed and gated onto the S Bus.

For the complex type functions (multiply/divide and shift) the ALU clock is enabled and a hardware sequence is entered to perform the required operation. The shift gates are used to shift the A Bus or the Sum Bus right or left back into the A latch and onto the A Bus again as determined by the ALU algorithms. In the case of fixed point multiply/divide the ALU stores half of the completed results before signaling the CPU with MFIN. The other half is dumped onto the A Bus from the MQ register and gated through the ALU onto the S Bus when MFIN is activated.

3.6.3 IOU Board. (Refer to the Block Diagram in IOU section.) The IOU board contains the I/O Control, the Display controller, the TTY controller, the Machine Control Register (MCR), the Power Monitor, Initialize circuits and the Start Timer.

The Display and TTY controllers have access to the CPU via the Multiplexor Channel D Bus and the I/O Control in the same manner as other peripheral device controllers. The Display controller provides a visual display of the contents of all system registers and any main memory location, together with the capability of manually entering data and programs. It shares D Bus drivers/receivers with the TTY controller and signals the CPU directly with the Display (DSPLY) interrupt. The Console Attention (CATN) signal appears as Bit 10 of the MCR.

The TTY controller, which supports the Model 33/35 Teletype, provides serial/parallel conversion and all standard TTY control features. It contains a full character buffer in the receive mode to permit a program service interval of one character time (100 milliseconds). The detailed descriptions of the Display and TTY controllers are covered in Sections 12 and 13 respectively.

I/O Control. The I/O Control performs a multiplicity of functions. The main function is to generate Multiplexor Channel D Bus from the CPU busses whenever it is addressed by Module Number 2 and the proper function selections are made. The control also performs byte manipulation for the CPU both in conjunction with an I/O operation and without. Common function decoders also generate signals to sense/clear the MCR (which stores Machine Malfunction conditions), to set the system Stop flip-flop with a Power Down/Initialize function (FPOW), and to gate 4-bits of the B Bus (12:15) to the front terminal strip of the chassis for external signaling purposes; e.g., multi-CPU operations.

Four function select lines together with the KSIG line pick 1 of 32 possible functions as shown on Table 7.

TABLE 7. I/O CONTROL FUNCTIONS

FSEL0X					FUNCTION	
	0	1	2	3	KSIG=0	KSIG=1
0	0	0	0	0	RD	RDR
1	0	0	0	1	WD	WDR
2	0	0	1	0	SS	SSR
3	0	0	1	1	OC	OCR
4	0	1	0	0	RDH	*STBR
5	0	1	0	1	WDH	*LBR
6	0	1	1	0	ACK	*LDWAIT
7	0	1	1	1	*SMCR	*CMCR
8	1	0	0	0	RDA	RDRA
9	1	0	0	1	WDA	WDRA
A	1	0	1	0	SSA	SSRA
B	1	0	1	1	OCA	OCRA
C	1	1	0	0	RDHA	*STB
D	1	1	0	1	WDHA	*LB
E	1	1	1	0	*THW	*EXB
F	1	1	1	1	*POW	*POUT

* Functions that do not require operation of the Multiplexor Channel D Bus.

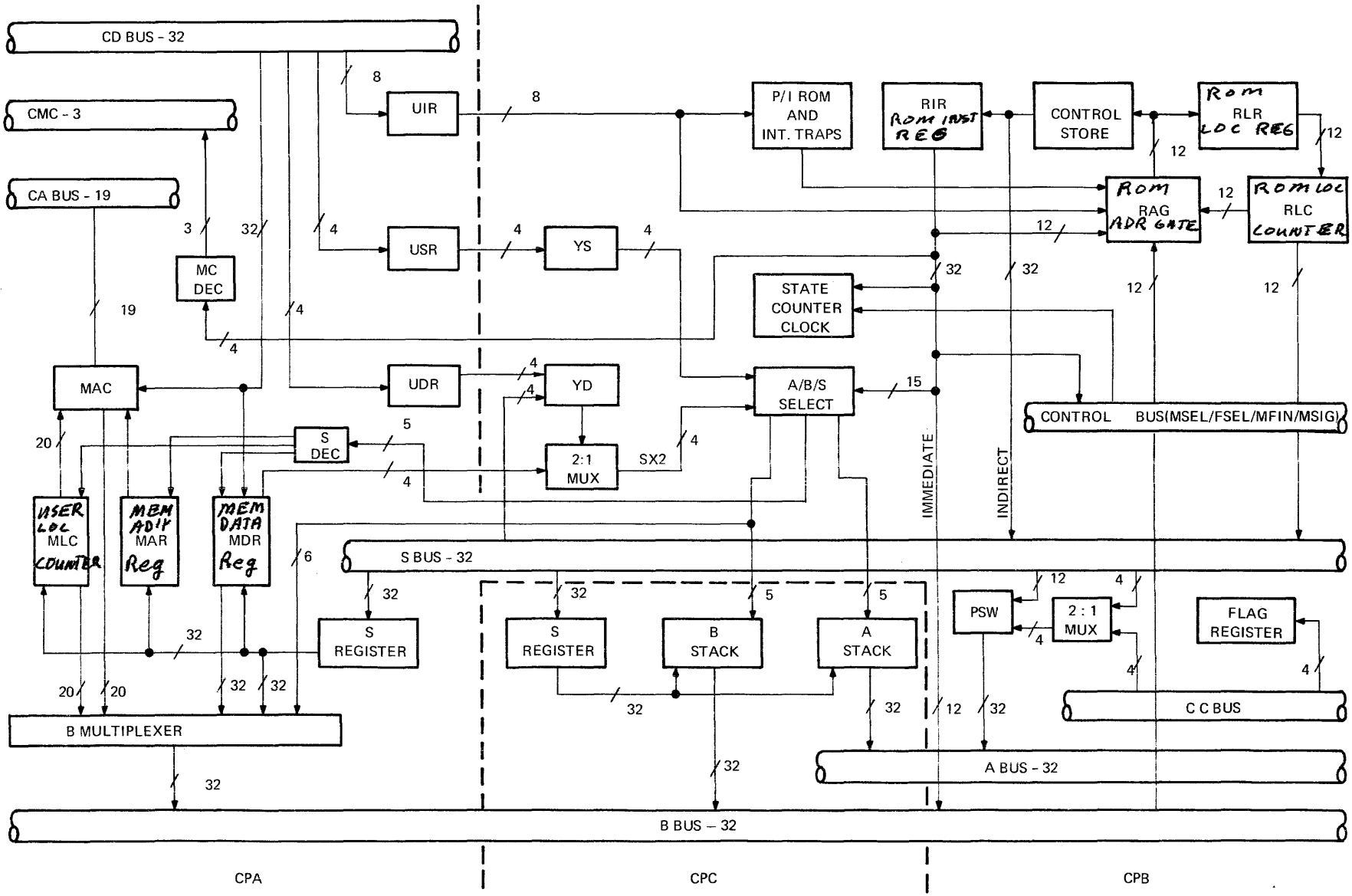


Figure 3. CPU (CPA, CPB, and CPC) Block Diagram

The D Bus functions may be performed with or without an address cycle depending upon the state of FSEL00. KSIG is used to specify register type operations or to distinguish between the halfword functions (RDH/WDH) and some non-D Bus operations (STB/LB).

The function mnemonics are listed as follows:

MNEMONIC	FUNCTION	COMMENT
RD/RDA	Read Data	byte/indexed
WD/WDA	Write Data	byte/indexed
OC/OCA	Output Command	byte/indexed
SS/SSA	Sense Status	byte/indexed
RDR/RDRA	Read Data	byte/register
WDR/WDRA	Write Data	byte/register
OCR/OCRA	Output Command	byte/register
SSR/SSRA	Sense Status	byte/register
ACK	Acknowledge Interrupt	byte/register
RDH/RDHA	Read Data Halfword	two data cycles for byte controllers
WDH/WDHA	Write Data Halfword	two data cycles for byte controllers
THW	Test HW Control Line	State of HW→MSIG
STB	Store Byte	halfword/indexed
LB	Load Byte	byte/indexed
STBR	Store Byte	halfword/register
LBR	Load Byte	byte/register
SMCR	Sense Machine Control Register	
CMCR	Clear Machine Control Register	
EXB	Exchange B-Bytes	
LDWAIT	Load Wait Flip-Flop	B (16) to FWAIT
POW	Release Initialize Relay	
POUT	Gate Output Pulses	

I/O Control/Operation. When the I/O Control is addressed and given a D Bus function code, it creates a one, two or three cycle Multiplexor Channel operation. The device address on A Bus (22:31) is gated to D Bus (06:15) together with the ADRS Control line whenever address type functions are specified. The returned SYN signal terminates the address cycle and initiates the next control function (DA, DR, CMD or SR). Delay timing within each cycle insures that the relationship of the Control line and D Bus signals meet the Multiplexor Channel Timing requirements.

The halfword functions (RDH/WDH) have a single data cycle when the Halfword (HW) Test line is active and two data cycles when a byte oriented controller is addressed (HW Test line inactive).

Output data is gated from the B Bus to the D Bus. The input data is gated from the D Bus to the input Data Register and then onto the S Bus, via ROM controlled S Bus Multiplexors. In a Sense Status operation, Data Register Bits 12:15 are also gated to the Condition Code (CC) Bus via the CC MUX. On all other D Bus operations, four zeros are placed on the CC Bus together with the CC strobe (SCC0). These zeros clear the CPU flag register but do not enter the PSW unless the CPU Enable bit is set.

At the end of the operation, the I/O Control returns a MFIN signal to restart the CPU clock.

The ACK function generates a single cycle on the D Bus and activates one of four Acknowledge lines, according to B30:31.

Byte handling functions. Selected bytes from the A and B Busses are gated onto the S Bus, via ROM controlled S Bus Multiplexors. (See IOU section for details.)

POW, POUT, LDWAIT, SMCR, CMCR, and THW Functions. These functions are described in detail in the IOU section.

Power Monitor. The Power Monitor contains the Primary Power Fail (PPF) detect circuits, the system Initialize Relay (K1) and the associated delay circuits used to control the relay amplifier. This logic provides an orderly system shutdown whenever the system is initialized or when power is turned off or lost.

The 12VAC input from the CPU logic supply is monitored for low line voltage. When trouble is detected, the Early Power Fail (EPF) bit is set in the MCR to create an MMF interrupt. After approximately 1 millisecond, the PPF interrupt is generated and the relay release operation begins. The POW function also initiates the release operation.

For multi-CPU systems, the various Power Monitors may be interconnected for proper sequencing of the sub-systems.

4. CPA GENERAL DESCRIPTION

4.1 CPA Block Diagram Description (Refer to Figure 4.)

The major Processor elements contained on the CPA are the Memory Address Registers (MAR), Memory Data Registers (MDR), the memory address arithmetic unit, the Memory Access Controller (MAC), part of the B Bus Multiplexor (BMUX), and an S-Bus buffer register (SREG).

The Memory Address Registers consist of the Memory Location Counter (MLC) and the Memory Address Register (MAR). The Memory Data registers consist of the Memory Data Register (MDR), the User Instruction Register (UIR), the User Destination Register (UDR), and the User Source Register (USR).

The memory address arithmetic unit consists of a Summer (SUM1X), a Multiplexor (MALX), a second Summer (SUM2X) and a second Multiplexor (MUXB). MALU

The Memory Access Controller (MAC) consists of a set of 16 Base Registers (BR), a Status Register unit (STATR), and Base Register arithmetic logic (SUM3X and LIMIT).

The B-Bus interface consists of the B Multiplexor (BMUX) and the B-Bus Addressing circuit (BADR). The S-Bus interface consists of the S Buffer Register (SREG) and the S-Bus Addressing circuit (SADR). Additional logic (MC Decoder) is used to decode the 4-bit MC Bus from the CPA to provide the CPB and the memory system with appropriate commands.

4.1.1 CPA Block Diagram Analysis (Figure 4). The following paragraphs provide brief descriptions of the function and data interfaces of each of the blocks in the CPA.

Memory Location Counter (MLC). The MLC is a 20-bit register which stores the starting address of the most recent instruction. It is loaded by a micro-instruction command (micro-control) from the S-Bus through SREG and an ST Bus, and it can be incremented by micro-control. Its outputs are connected to MALX for instruction fetches; to MUX B for relatively-addressed (RX2) data operations, and to BMUX for connection to the B-Bus.

Memory Address Register (MAR). The MAR is a 20-bit register which stores the absolute address for RX1 data operations, the relative address for RX2 data operations, and the total index (sum of the contents of the first and second index registers) for RX3 data operations. It can be loaded from the ST Bus or incremented by micro-control, and its outputs connected, except for Bit 31, to SUM2X for data address calculation. Bit 31, which is only used in I/O operations, is connected directly to Bit 31 of the Memory Address Bus (CA310).

Memory Data Register (MDR). The MDR contains a 32-bit register and a 32-bit multiplexor. The MDR is used to store data read from memory, to store data to be written into memory, and to store the absolute (non-indexed) address for RX3 data operations. The inputs are connected to the ST Bus for loading from the S-Bus or to the Memory Data Bus (CD00:31) for loading from memory. The outputs are connected to BMUX for connection to the B-Bus and, through a set of CD gates, to the CD Bus for writing into memory. The outputs MDR12:31 are also connected to MUXB for use in RX3 data operations.

User Instruction Register (UIR). The UIR is an 8-bit register which stores the Operation-Code (op-code) of the most recent instruction. It is loaded from CD16:23 on all instruction fetches, and the outputs are connected to CPB through front Connector 5.

User Destination Register (UDR) and User Source Register (USR) are used as follows: The UDR is a 4-bit register which stores the R1 field of all user instructions, and the USR is a 4-bit register which stores the R2 field of RR instructions, the N field of SF instructions, and the X2 (or FX2) field for indexed instructions. These registers are loaded from CD24:27 and CD28:31, respectively, on all instruction fetches, and the outputs are connected to CPB through front Connector 5.

Summer 1 (SUM1X). The SUM1X is a 20-bit adder which provides temporary increments to the MLC for RX and RI instruction fetches, and, when properly enabled by PSW 21, adds the relocation field from MAC Base Register (BR), if used, to the program address from MALX.

Multiplexor (MALX). The MALX is a 20-bit multiplexor which selects between MLC and the output of SUM2X, for instruction fetches and data operations respectively.

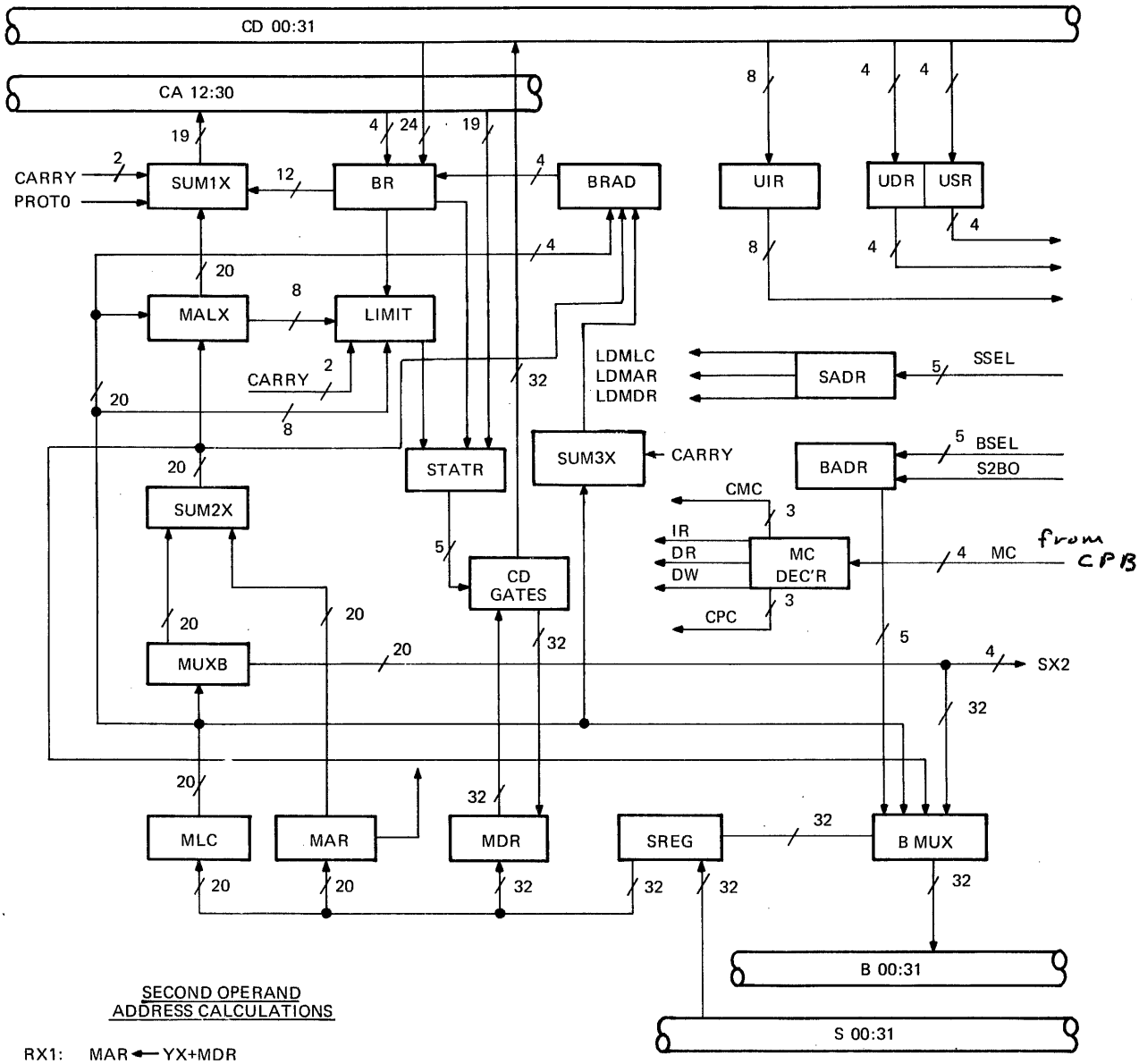
Summer 2 (SUM2X). The SUM2X is a 20-bit adder which sums MAR with MLC (for RX2 instructions), or MDR (for RX3 instructions), or neither (for RX1 instructions).

Multiplexor B (MUXB). The MUXB provides selection between MLC and MDR for inputs to SUM2X.

B Bus Addressing Circuit (BADR). The BADR is a decoder which accepts the BSEL00:04 Bus, instruction format data, and a special command line S2B0 as inputs, and by means of BMUX, connects the appropriate outputs from SR, MDR, MLC, and SUM2X to the B Bus.

S Bus Addressing Circuit (SADR). The SADR is a decoder which accepts the SSEL00:04 Bus as inputs and causes MAR, MLC, or MDR to load from the SR00:31 Bus. SR is a buffer register which loads from the S Bus at each system clock and drives the SR00:31 Bus.

MC Decoder. The MC Decoder accepts the MC00:03 Bus from the CPB and decodes this bus to provide the Memory Command Bus CMC00:02 and all of the internal CPA control signals.



SECOND OPERAND ADDRESS CALCULATIONS

RX1: MAR ← YX+MDR
CA ← MAR+BR

RX2: MAR ← YX+MDR
CA ← MAR+MLC+4+BR

RX3: MAR ← YX+SX2
CA ← MAR+MDR+BR

INSTRUCTION ADDRESS CALCULATION

CA ← MLC+BR

Figure 4. CPA Block Diagram

4.1.2 Memory Access Controller (MAC) Block Diagram Analysis (Figure 4). The following paragraphs provide brief descriptions of the function and data interfaces of each of the blocks in the MAC.

MAC Base Registers (BR). The BRs are a set of 16 24-bit registers which store the relocation, limit and interrupt control data for the Memory Access Control (MAC). BR receives a 4-bit address from the Base Register Address System (BRAD), is loaded with 24-bits of data from the MDR on command from the micro-program, provides an 8-bit limit field (BR04:11) to the Limit Comparator (LIMIT), a 12-bit relocation field (BR12:23) to SUM1X, and a 4-bit interrupt control field (BR24:27) to STATR.

MAC Base Register Address System (BRAD). The BRAD contains a 4-bit register, two 4-bit multiplexors, a 4-bit adder, and provides addresses to the BR from three sources: the Memory Address Bus CA26:29 for loading, MCL12:15 for instruction fetches, and MALX12:15 (through the 4-bit register) for data operations. The 4-bit adder provides a carry capability whenever MLC is incremented across a memory segment boundary.

MAC Status Register Unit (STATR). The STATR is a 5-bit Interrupt Status register with associated address decoding and interrupt controls. STATR is disabled whenever PSW21 is inactive or whenever a privileged micro-control is effected. (Privileged in this context means that MAC relocation and protection are disabled, exactly as if PSW21 were made inactive.)

When relocation and protection are disabled, a decoder senses CA12:31 and traps the locations assigned to the MAC. It is then possible to load BR or to read the five bits of STATR using the same procedures that are used to read from or write to memory. When relocation and protection are enabled, references to the trapped locations results in accesses to memory. The Memory Access Interrupt logic is also activated, under control of BR24:27.

MAC Limit Comparator (LIMIT). The Limit Comparator compares each memory address with the 8-bit limit field in BR and, when the protect function is enabled, causes an interrupt to be generated if an attempt is made to access a memory address which is larger than the limit.

MAC Summer 3 (SUM3X). The SUM3X monitors the MLC and anticipates when the incremented MLC (for RX and RI instructions) passes a segment boundary. When this occurs, the BR address is incremented by one, and a delay is initiated to allow time for a BR address change.

4.2 Memory Addressing (Refer to Functional Schematic 35-536D08 for mnemonic location.)

The 8/32 memory address data is derived from MLC, MAR, MDR, the MAC BR, and two carry signals. Selection from among these sources, and the computations used to arrive at the final address, are determined by the machine cycle (instruction fetch or data operation), instruction format (RR, SF, RX, or RI), and status of the Memory Access Controller (MAC).

During instruction fetches, which are initiated by particular states of the MC00:03 Bus from CPB, the program memory address is taken from MLC. RX and RI instructions require increasing the effective address by two or four bytes to access the second and third halfwords of the instruction. If relocation is enabled by PSW21, an additional 12-bit relocation field is added to MLC. The effective address is then:

$$CA = MLC + BR\ (MAC) + carries\ (2\ or\ 4)$$

this addition occurs in SUM1X. (Sheet 8)

When memory is accessed for data operations in response to a user instruction, the effective address may be the sum of as many as five parts: an absolute address, a relative displacement, a first index, a second index, and MAC relocation field. For RX1 instructions, the absolute address is contained in MDR18:31 and the index in a user register addressed by the contents of register YX in CPB. For RX2 instructions, the relative displacement is contained in MDR17:31, the reference address in MLC (incremented by four) and the index in a user register addressed by the contents of register YX in CPB.

For RX3 instructions, the absolute address is contained in MDR 24:31, the first index in the user register addressed by the contents of register YX in CPB, and the second index in the user register addressed by the contents of register SX in CPA. Each of these program addresses can then be modified by the MAC relocation field from BR. The address calculations are:

RX1:	MAR	(YX) + MDR
	CA	MAR + BR
RX2:	MAR	(YX) + MDR
	CA	MAR + MLC + 4 + BR
RX3:	MAR	(YX) + (SX)
	CA	MAR + MDR + BR

In each of these formats, the first addition is performed in the ALU and, the second addition is performed, simultaneously, by hardware in the CPA.

4.2.1 CPA Address Computation Instruction Fetch Address Computation. (Sheets 3, 6 and 8) The computation CA MLC + carries + BR is done in SUM1X as shown on Sheet 8. It consists of five 19-067 4-bit ALU ICs and one 19-068 Carry look-ahead IC which is connected across the 16 most significant bits of the ALU. The "A" inputs to the ALU ICs are connected to MALZ12:31. For instruction fetches, SIR1 is active, and the outputs of MALX16:31 are MLC12:31 (Sheet 3) and the outputs of MALZ12:15 are either MLC12:15 or are open, depending on whether the MAC is enabled. If the MAC is disabled PROT1 (8R2) is inactive and MALX12:15 are enabled. If MAC is enabled, PROT1 is active (high) and MALX12:15 are inactive and effectively all zeros.

The "B" inputs to SUM1X28:30 (8D7) are derived from Carry signals C00 and C01 (Sheet 1), and RX2F1 (Sheet 10). For RX1, RX2, and RI1 formats, MLC must be incremented by two bytes to read the second halfword of the instruction from memory. C001 is made active, and both C011 and RX2F1 are inactive. Since the ALUs of SUM1X are operating on low-active data, these conditions cause the B1 input to be active (low) through the NAND gate (8B4), the B2 input to be inactive (high), and a count of two bytes to be added to MLC28:31 to produce CA28:30. If a Carry (Cn+4) is produced by the lowest-order ALU, this is propagated through the remaining bits of CA by means of the 19-068 Carry look-ahead IC device.

For RX3 and RI2 instructions, which require that three halfwords be read from memory, C011 is made active after the second halfword is read from memory. This disables the B1 input to the ALU (8D7) and, through the AND-OR-Invert gate (8B3), causes the B2 input to the ALU to become active, adding four bytes to the memory location from MLC.

When MAC is disabled, PROT1 (8R2) is inactive, PROT0 (8E6) is active (high) and the ALU is in the A only mode, producing CA← MLC + carries. When the MAC is enabled, PROT1 is active, PROT0 is inactive, and SUM1X is placed in the A + B mode, where the B inputs to SUM1X12:23 are BR120:230 (Sheet 6), producing CA←MLC + carries + BR.

Data Read/Write Address Computation (Sheets 3, 4, 6, 8 and 9)

The address computations required for data operations are determined by the instruction format, as shown previously in Section 4.2.

For RX1 instructions, the computation which must be performed in hardware is:

CA← MAR + BR

The following conditions exist at the inputs to the gates (8A3 and 8A4) which produce ALU inputs B1 and B2; SDRDW0 is active, and C011 and RX2F1 are inactive. Both B1 and B2 are thus held inactive, inhibiting any address carries into SUM1X. The Memory Address Bus CA12:30 is then equal to the outputs of MAMLX12:30, if the MAC is disabled, or the sum of MAMLX12:30 and BR12:23 if the MAC is enabled.

MAMLX (Sheet 8) is a 20-bit wide, two-input multiplexor which switches the inputs to SUM1X between MLC and SUM2X, depending on the machine cycle as indicated by SIR1. For data operations, SIR1 is inactive, and MAMLX←SUM2X.

SUM2X (Sheet 9) is a 20-bit ALU similar to SUM1X. The A inputs are MAR12:31, and the B inputs are MUXB12:31. The A inputs to MUXB are MLC12:31, the B inputs to MUXB are MDR12:31 and the select input to MUXB is RX3F1, so that for RX3 instructions MUXB←MDR and for other formats MUXB←MLC. The control inputs to the ALU are RX1D0A and RX1D0B, which are both active low for RX1 instructions. This control condition cause the outputs of SUM2X to be equal to the A inputs, or MAR12:31, and the address calculation for RX1 instructions is correct.

For RX2 instructions, the computation which must be performed in hardware is:

CA←MAR + MLC + 4 + BR

Since RX1D0A and RX1D0B are inactive (high) SUM2X is in the A plus B mode. The A inputs are MAR12:31, and the B inputs are MUXB12:31. The select input to MUXB (Sheet 9) is RX3F1, which is inactive (low) for RX2 instructions. MUXB12:31 are then connected to the A inputs, which are MLC12:31. Thus SUM2X calculates MLC + MAR.

Since the RX2F1 input to the AND-OR-Invert gate (8B4) is active, when the system control state reaches State 0(CS001 active) a carry is enabled at the 4-bit ALU (8D7). This increments the output of the ALU (Sheet 8) by four. If the MAC is enabled, BR12:23 are summed into the ALU and into the address. If the MAC is not enabled, the address output is MAMLX + 4. Since SIR1 (8C3) is inactive, MAMLX12:31 is SUM2X12:31 and, as shown previously, this is MAR + MLC. Thus, CA MAR + MLC + 4 + BR as required for RX2 instructions

For RX3 instructions, the computation which must be performed in hardware is:

CA←MAR + MDR + BR

The calculation of MAR + MDR is done in SUM2X by RX3F1 (9C2) becoming active and switching MUXB12:31 to MDR12:31. The final calculation is done by the ALU (Sheet 8) as for RX1 instructions.

Since MDR is used to provide part of the address for data reads and data writes, it is essential that the address be kept stable during the memory operation. For data reads, MDR is used as a double-rank buffer. The data from memory is loaded into the register (Sheet 4), by making both MCLK0 and the Load inputs on Pin 09 of the 19-070 IC devices simultaneously active (low). The outputs MDR00:31 do not change until MCLK0 becomes inactive, which occurs after memory has been read and the address may change. For data writes, where the data word must be loaded into MDR to write into memory, the calculated address is first loaded into MAR, and then the data is loaded into MDR. This last operation is performed by the micro-program.

4.2.2 Base Register Selection

The Base Registers (BR) are selected for loading or when MAC is enabled for relocation and protection. When selected for loading, the registers are addressed in the same manner as memory locations and the associated memory locations receive and store the same data as the BR. When the MAC is enabled, the BR is selected using the four most significant bits of the program address: MLC12:15 for instruction fetches and SUM2X12:15 for data operations.

There are 16 Base Registers (BR), selected by the four address bits at Pins 01, 13, 14, and 15 of the 19-075 IC devices (Sheet 6). The 1MB memory is segmented into 16 64KB segments, and the four most significant bits of the 20-bit program address determine which segment, and therefore which Base Register (BR) is in use. For instruction fetches, the 4-bits are taken from MLC12:15. For data reads or writes, the 4-bits are taken from SUM2X12:15.

Base Register Selection for Loading. The Base Registers (BR) and the Status Register (STATR) (see Section 4.1.2) are assigned a group of memory addresses starting with an odd multiple of X'100' from '300' to '900', and ending at address '43' within the group. The MAC is configured to trap all 256 addresses within the group. The particular group used is a function of the system I/O requirements, and selection of the starting location of the group is by means of one or more jumpers (7B8). Table 8 shows the required jumpers for various starting locations.

TABLE 8. STARTING LOCATION JUMPERS

8/32 is wired

STARTING LOCATION	05J11 TO:	05J13 TO:	05J15 TO:
'300'	05J06 *	05J03 *	05J01 *
'500'	05J05	05J04	05J01
'700'	05J06	05J04	05J01
'900'	05J05	05J03	05J02

Whenever the MAC is disabled, by PSW21 being reset or a Privileged memory command present, PROTO (7A5) is inactive, and if any address within this trapped interval appears on the CA Bus, a SRTR1 signal (7N6) is made active. This signal (6C8) causes a multiplexor to switch the address inputs of the 19-075 Base Register IC devices (Sheet 6) to CA26:29. The desired register is then selected. If the address is obtained because of a memory write command, a request pulse (CREQ0) is transmitted to memory and, simultaneously, an active pulse appears on RQFF0 (7A9). This causes the flip-flop (7F8) to be set, making BRWR1 active (7N7). This signal is gated with CA300, the halfword select bit of the memory address, and with FWWRT0, a signal (2M7) which is active whenever a fullword write is commanded, to produce SEGWEA0 and/or SEGWEB0. These in turn enable writing from MDX041:271 into the odd or even halfwords of BR, or both.

Base Register Selection for Relocation and Protection (R and P). Whenever PROT0 (7A5) is active, due to PSW21 being set and no privileged memory operation in the Micro-Control (MC) field of the micro-instruction, SRTR1 (7N6) is made inactive. This causes the 19-132 multiplexor at the address inputs to BR (Pins 01, 13, 14, and 15 of the 19-075 Base Register IC devices) to be connected to the output of a 19-133 4-bit adder (6B6). The four address bits to BR then depends on whether an instruction fetch or a data operation is being performed and also whether the carrys needed for fetching the second and third halfwords of RX and RI instructions increment MLC beyond a segment boundary.

For instruction fetches, the segment number and therefore the Base Register (BR) address is determined by MLC12:15. Whenever relocation and protection are enabled, and a data operation is not being performed, SRTR1 (6A8) and SDRDW1 (6A4) are inactive, and the address inputs to BR is connected to MLC12:15 through the multiplexors (Sheet 6).

If the program address for an instruction fetch is within one halfword of a segment upper boundary, and the instruction format is RX or RI, the subsequent halfword carry causes the four most significant bits of the program address to increment by one. MLC12:15 does not change, so a simulated carry C3X0 (6A5) is made active by the circuits shown on Sheet 12, which are discussed later. An active C3X0 increments the output of the 19-133 IC Adder (6A6) by one and causes the BR address to increase by one.

If the program address for an instruction fetch is with two halfwords of a segment upper boundary and the instruction format is RX3 or RI2, the second carry into the program address causes the four most significant bits of the program address to increment by one. C3X0 is made active and the BR address is incremented by the adder (6A6).

Sheet 12 shows the circuits which generate the simulated carry signal C3X0. The instruction location within the segment is contained in MLC16:30. For a carry to cause the instruction location to move to the next segment, all of the bits in MLC from MLC29:16 must be active. In addition, if MLC30 is active, the first carry of the instruction fetch sequence propagates up to the Base Register (BR) select bits MLC12:15.

If MLC16:23 are active, the input on Pin 05 of the C3X0 gate is high, whenever SIR1 is active (during an instruction fetch). If, at the same time MLC24:29 are active, the inputs on Pin 01 of the 19-058 gates at locations 12E5 and 12E6 are active. If MLC30 is also active, and C001 becomes active, signals GT0, GT1, and C3X0 all become active.

If MLC30 is inactive, C001 does not generate C3X0. However, if the instruction format is RX3 or RI2, C011A becomes active when the third halfword is read from memory. This causes GT0, GT1, and C3X0 to become active, signalling that the address has incremented beyond the segment upper boundary. GT0 and GT1 are used in limit checking and are discussed later.

When a data operation is commanded by the micro-control bits, a SDRDW1 signal (2S9) is decoded from MC00:03 and latched in a tracking latch (Sheet 2) when DREQ1 becomes active at the start of the memory operation. This causes the multiplexor outputs (6B4) to be connected to the inputs of a quad flip-flop (6B2). These flip-flops store the four most significant bits of the most recent data operation, so that as soon as it is determined that a data operation is to be performed, the Base Register (BR) address lines are switched to what is most likely the correct segment. If, however, the new data address is in a different segment than the most recent data address, a 19-117 4-bit comparator (6C2) is enabled to compare the new segment number on SUM2X 12:15 to the old segment number stored in the 19-131 quad flip-flop. Approximately 100 nanoseconds after the start of the data operation a P100N1 pulse is gated into the quad flip-flop and updates the stored segment number. The output AEQB1 of the comparator is used to cause an 80 nanosecond delay in memory operation whenever the segment number changes, to allow time for the new base register to be accessed and the address calculation to change.

4.2.3 Base Register Write Operation. As described in Section 4.2.2, the Base Registers (BR) are addressed from CA26:29 whenever relocation and protection are enabled and one of the trapped memory locations is addressed on the CA Bus. If, at the same time the MC field of the micro instruction calls for a Write operation, a SDW1 signal is decoded from the MC field and appears active (7H8). Subsequently, a request is made to memory and a RQFF0 signal (7A9) becomes active for approximately 50 nanoseconds. The leading edge of RQFF0 sets the flip-flop (7G8) and causes BR WR1 (7N7 and 6H2) to become active.

The Base Registers (BR) are addressed in exactly the same way as memory locations, so that the even halfword, the odd halfword, or the fullword can be written into. If the memory command is Full Word Write, a FWWRT0 signal (6J1) becomes active. This gates BRWR1 to SEGWEA0 and SEGWEB0, the Write Enable inputs to the Base Register (BR).

SEGWEA0 is active whenever FWWRT0 or CA300 are active, and enables writing into the most significant, or even, halfword of the Base Register BR16:27. SEWEB0 is active whenever FWWRT0 is active or CA300 is inactive, and enables writing into the least significant, or odd, halfword of the Base Register, BR02:15.

The data inputs to BR are connected to the outputs of multiplexor MDX04:27. For fullword write operations, MDX04:27 are switched to CD04:27, which in turn are connected to MDR04:27 (Sheet 4 and Sheet 11). For halfword write operations, the data to be written into BR is contained in MDR16:31, whether the location to be written into is odd or even. This data is brought to the odd halfword inputs to BR16:27 from MDR16:27 through tri-state gates (Sheet 11) to CD16:27 and through MDX16:27 to BR. This data is also routed from MDR20:31 through tri-state gates (Sheet 11) to CD20:31 and through gates (11L4 to 11L9) to MDX04:15 and the inputs to BR04:15. Thus, the halfword data is presented simultaneously to the inputs to both the odd and even halfwords of BR. It is written into whichever halfword has an active Write Enable i.e., SEGWEA0 or SEGWEB0.

4.2.4 Status Register Selection, Read and Write Clear. As described in Section 4.2.2, memory references to the locations assigned to the Base Registers (BR) and Status Register (STATR) are trapped by logic shown on Sheet 7. Whenever the address is '-----40' thru '-----43', and a memory reference is started so that the flip flop at 7F8 is set, a STAT0 signal (7M7) becomes active. If the memory reference is a read reference, the SDR1 signal (7K 9) is active, and when memory is read, MDRCLK 1 (7L9) also becomes active. This causes RSTR0 (7R9) to become active which connects the outputs of the Status Register flip flops IR27 31 (sheet 7) to the CD Bus by means of five tri-state gates (Sheet 11). To insure that the CD Bus is not being driven from the memory at the same time that it is being driven from the Status Register, the STAT0 signal causes the CMC Bus (2R9) to change from a Read command to a Write command so that the memory does not drive the CD Bus.

If the memory reference is for a Write operation, the Status Register is cleared. SDW1 (7L7) is decoded from the micro-instruction MC field and, when STAT0 is active, an active condition of RQFF0 caused by the memory reference makes CSTA0 active which clears the Status Register flip-flops IR27:31.

4.2.5 Memory Access Interrupts. Whenever the Memory Access Controller (MAC) is enabled, because PSW21 is set and a privileged memory reference is not in process, certain conditions may be detected which causes the CPA to signal the CPB that an interrupt must be taken. This signal occurs in one or more of the following ways:

1. For interrupt conditions which occur during data references to memory, a Memory Access Interrupt (MAI0) signal is made active (7N4).

2. For interrupt conditions which occur during instruction fetches, an ININT0 signal is made active (7N2) and the output of the User Instruction Register UIR24:31 (Sheet 5) is forced to 'FF'.

Memory Access Interrupt During Data Operations. There are four conditions which causes a Memory Access Interrupt (MAI0) signal to become active during a data operation. These are each represented by a bit in the Status Register IR27:30, as shown in Table 9. Also shown are the conditions of BR25:26 which enable the two Write Protect interrupts, which are described as follows:

TABLE 9. MEMORY ACCESS INTERRUPT SIGNALS

BR25:26	IR BIT	MEANING
--	27	INVALID ADDRESS
--	28	NON-PRESENT ADDRESS
X1	29	WRITE PROTECT VIOLATION
10	30	WRITE/INTERRUPT CONDITION

1. Invalid Address Interrupt for Data Operation. An invalid address is an address which exceeds the upper limit of a memory segment as determined by BR04:11 (the Limit field). A pair of 19-117 comparators (Sheet 6) continually compares these Base Register (BR) bits to the eight most significant bits of the un-relocated program address MALX16:23 and, when an attempt is made to address a location beyond the Limit field, LIME1 (6N6) becomes active.

   As soon as the memory reference is started, DREQ1 (7A1) becomes active, so that the output of an AND gate (7C1) becomes active if LIME1 is active due to an invalid address. This enables setting of the IR 27 flip-flop (7D1) and, since SIR0 is inactive (high) causes NW0 and NW1 (7K2) to become active, which enables setting of the MAI flip flop (7M4).

   As soon as an attempt is made to reference memory for a data operation to the invalid address, a RQFF0 signal (7A9) becomes active for 50 nanoseconds. If the MAC is enabled, SPROT1 (7A5) is active. Because the MAC is enabled, SRTR0 (7A5) is inactive (high), so that the leading edge of RQFF0 sets the IR27 and the MAI flip-flops.

   If the memory reference is for a data write, SDW1 (7J5) is active, and NW1 causes CDW0 to become active. CDW0 (2K8) causes the Write command to memory on CMC00:02 to be converted to a Read command. When DREQ1 becomes inactive at the end of the memory operation, NW1 becomes inactive. However, since IR27 is set, CDW0 is maintained active as long as both the IR27 and MAI flip flops are set and SPROT1A is active, or until the SDW1 signal is made inactive by another type of memory reference.

As described in Section 4.2.4, the MAI flip flop is cleared whenever a read or write reference to the Status Register (STATR) is made. This removes the CDW0 signal, allowing memory Write operations to resume. Also attempting to write into the Status Register clears IR27, making CDW0 inactive and permitting Write operations to resume.

2. Non-Present Address Interrupt for Data Operations. When BR27 is reset, and any memory reference is made, the IR28 and MAI flip flops are set similarly to the invalid address interrupt described previously.

3. Write Protect Violation. Whenever the MAC is enabled and BR26 is set, the IR29 flip flop (7D4) and the MAI flip flop are set if an attempt is made to write to memory. All attempted Write operations are changed to reads by CDW0 until the MAI or IR29 flip flops are reset.

4. Write/Interrupt Condition. Whenever the MAC is enabled, BR25 is set and BR26 is reset, the IR30 and MAI flip flops are set, but writes are not changed to reads. This allows the program to continue while the Processor is interrupted.

Memory Access Interrupts During Instruction Fetches from Memory

There are three conditions which cause MAI0 to become active during an instruction fetch. These are shown in Table 10 together with the Status Register bits which represent the condition and the Base Register bit, if any, which enables the interrupt.

TABLE 10. MEMORY ACCESS INTERRUPTS

BR24	IR	MEANING
- -	27	INVALID ADDRESS
- -	28	NON-PRESENT ADDRESS
1	31	EXECUTE PROTECT VIOLATION

1. Invalid Address Interrupt for Instruction Fetch. The Invalid Address Interrupt for Instructions is similar to that for data operations except that CDW0 is not made active, and the MAI flip flop is not set. Instead, a latch (7M2) is set, causing ININT0 to become active. At the same time that ININT0 is made active to the CPB, ININT0 A is made active (5A9), presetting the UIR to 'FF'. This simulated user operation code is used in CPB to vector to a micro-code subroutine to process the interrupt while preventing the data at the invalid address from being executed as an instruction. The active condition of ININT0 is maintained until another instruction fetch is started, at which time ISTB0 (7L2) becomes active and resets the ININT latch. IR27 remains set until the Status Register is cleared.

2. Non-Present Address Interrupt for Instructions. When BR27 is reset and an instruction fetch is attempted, IR28 and ININT0 are set. Subsequent operation are similar to the Invalid Address interrupt (see 1).

3. Execute Protect Violation. When BR24 is set, and an attempt is made to fetch and execute an instruction; IR31, ININT0, and MAI0 are made active. Any subsequent attempts to write into memory are changed to reads until IR31 or MAI are reset. The UIR output to CPB is forced to 'FF' by ININT0 and remains so until the next instruction fetch.

4.3 Memory Reference Operations

All Processor operations which require reference to memory begin with a specification in the MC field of the micro-instruction. Table 11 shows the interpretation of MC00:03, and lists the micro commands in terms of the effect on memory reference operations.

TABLE 11. MICRO COMMANDS

OPERATION	MC 00:03
INSTRUCTION READ	1001 1100
DATA READ	1X1X 1000 1101
DATA WRITE	0X1X 0101

4.3.1 MC Field Decoding (Sheet 2). The MC Bus MC00:03 is connected to the CPA via front cable Connector 2. The following commands are decoded directly from the MC field; providing that PASSIA is not active, signifying that a branch is not occurring (for conditional micro-instructions, implementation of the MC field is inhibited whenever a branch is allowed):

CPC001	-	Increment MLC by the length of the last command
CPC011	-	Increment MAR by four
IR1	-	Instruction Read
DRDW1	-	Data Read/Write operation
RH0	-	Read Halfword

The following commands are decoded and stored in quad flip flops (Sheet 2):

SDR0	-	Data Read
SPROT1	-	Relocation and Protection enabled
SRH0	-	Read Halfword
SDW0	-	Data Write
SIR1	-	Instruction Read

These commands are stored whenever a new Memory Reference MC field is presented to CPA (as decoded by a 19-058 gate at 2F9) and a system clock CK1A occurs while the Processor is in Control State 0 (2H8). Since a new micro-instruction is read into the RIR of the CPB each time the Processor enters Control State 0, and a system clock occurs at the following transition from Control State 0, these flip flops always have stored the most recently commands to memory. The decoded function DRDW1 from a 19-116 decoder (2L4) is stored differently in a tracking latch (2N9). As long as no memory references are in operation, SDRDW1 tracks the decoded DRDW1. When a memory reference is started, DREQ1A (2L5) becomes active and remains active as long as memory is being interrogated. This signal freezes SDRDW so that the Processor cannot start another memory operation until the first is completed.

The Memory Command Bus CMC00:02 is effectively stored in the quad flip-flop at 2J7. However, these signals are enabled by DREQ1 in gates 2M7, and 2M8, and are modified by STAT0 and CDW0 from the MAC. When STAT0 is active, which can only occur when the Status Register is addressed, the memory is forced to a write condition, which causes the memory to release the CD Bus so it can be driven by the Status Register. CDW0 is active only when an illegal data write memory reference is commanded, which causes all memory Write operations to be converted to Read operations, by modifying Memory Command Bits CMC00:01.

4.3.2 Strobes and Delayed Clock. Each memory reference is started by one or more strobes. A NAND gate (12B1) accepts System Clock (CLK1A), the Instruction Read decoded command (IR1), a CS001 signal which indicates that a new micro-instruction is in the RIR and should be executed, and PASS0A from CPB which indicates that no branch is taking place. This combination makes ISTB0 and DSTB0 active. DSTB1 is the input to two cascaded 100 nanosecond delay lines (Sheet 12). The quiescent levels of the delay line outputs are low, except when a pulse which propagates down the delay line causes the outputs to become high. The 20 nanosecond tap is connected to a gate at 12J1 together with DSTB0. The resulting output STB0 is a 20 nanosecond wide negative pulse occurring after the trailing edge of DSTB0. This pulse is used to reset the MCLK0 latch (4A3).

When DSTB0 becomes active, a flip-flop at 12K2 is preset and a flip flop at 12K3 is cleared. The outputs, both high, of these flip flops are gated in an AND-OR-Invert gate (12M3) to produce DLCK0, which becomes active at the trailing edge of CLK1, when SIR1 becomes active, or at the leading edge of CK1A when SDRDW becomes active.

The width of DLCK0 is determined by whether an instruction or a data operation is in process and whether, in each case, a change in memory segment, and therefore the Base Registers, is required.

During an instruction fetch, SIR1 is active and DLCK0 terminates when the flip-flop at 12K2 is reset. The clock for this flip flop occurs approximately 40 nanoseconds after the trailing edge of DCLK0. If, at this time, the MLC has been incremented and a carry is being propagated to the four most significant bits of MLC (MLC12:15), C7X1 and CK1A (12B1) become active and the two gate latch at 12F3 is set. The output connected to the D input of the flip flop is high, and the flip flop is not reset at the trailing edge of the 40 nanosecond clock.

If MLC12:15 are not going to change, the Base Register (BR) selection does not change, and C3X1 remains low. The latch is reset at the end of every memory operation by P180N0·P200N1, the D input to the flip flop remains low, and DLCK0 is terminated approximately 60 nanoseconds after the trailing edge of CK1A.

During a data operation, ISTB0 is not generated, but DSTB0 and STB0 occur when CK1A, STRT1, and DRDW1 are all active simultaneously, that is, during the system clock which is to initiate a data reference to memory. At this time, SDRDW1 is made active, and DLCK0 terminates when the flip flop at 12K3 is set. The clock to this flip flop occurs approximately 80 nanoseconds after the trailing edge of DSTB0. At this time, a 4-bit comparator (6C2) is comparing the stored segment number with the desired segment number as indicated by SUM2X 12:15, and, if the two are different, AEQB1 at the D input to the flip flop is low. The flip flop remains reset and DLCK0 continues. If the actual and desired segment numbers are the same, AEQB1 becomes active, the flip flop is set and DLCK0 terminates approximately 100 nanoseconds after the trailing edge of CK1A.

If DLCK0 is not terminated at 60 nanoseconds for instructions or at 100 nanoseconds for data references, a pulse generated by P180N0·P200N1 direct clears the first flip flop and direct sets the second flip-flop, terminating DLCK0 at approximately 180 nanoseconds and allowing time for the memory address to settle before a memory request CREQ0 is activated.

If the MAC is disabled, SPROT0 (12B4) is inactive. This gates P080N1 and terminates DLCK0 approximately 80 nanoseconds for both instruction and data references.

4.3.3 Instruction Read (see Figures 5A, 5B, and 5C, Instruction Read). When an MC field decodes to Instruction Read, IR1 (2N5) becomes active. Since the new MC field is stored in RIR during Control State 0, the conditions required by the four-input 19-060 NAND gate (12B1) are met when the next system clock CK1A becomes active. This causes ISTB0 and DSTB0 to become active. ISTB0 (1L5) causes the IREQ flip flop (1L5) to be direct-set, making IREQ0 active, and DISTB0 (1L6) makes DREQ0 active.

Following the trailing edge of DSTB0, a 20 nanosecond STB0 pulse is made active (12K2).

The negative-going DSTB0 sets two flip-flops on Sheet 12. Since SIR1 (2K7) is latched active at the trailing edge of CK1A, DLCK0 (12R3) becomes active at the trailing edge of DSTB0 (and CK1A) (1K5). DLCK0 and STB0 become active at the same time, but DLCK0 remains active longer than STB0. DREQ1 is made active before DLCK0, so that at the trailing edge of DLCK0 (which is variable depending on addressing conditions) a preset is applied to the CREQ flip flop (1L2). This preset pulse is only 20 nanoseconds wide because it is gated by SHP1 from a 30-019 delay line (1N4), which is pulsed by the leading edge of DLCK0. After 50 nanoseconds, the delay line output is inverted (IR3) and clocks the CREQ flip flop off, so that 50 nanosecond CREQ0 and RQFF0 pulses are generated.

CREQ0 is transmitted to the memory subsystem to request a memory operation in accordance with the Memory Command Bus CMC00:02. At the same time RQFF0 is made active (1A1), causing MDRCLK0 and MDRCLK1 to become active.

Whenever memory is not being referenced, DREQ1 is inactive. This signal holds a two-stage Johnson Counter, consisting of two flip flops (Sheet 1), reset. As soon as DREQ1 becomes active, this counter is free to be clocked.

The leading edge of MDRCLK1 causes the C00 flip flop to be set, making C001 and C000 active. C001 and C010 are gated by CD170 (1G7) in a 19-062 AND-OR-Invert gate. If CD170 is inactive (high) for RR and SF formats, the D input to the DREQ flip flop (1M7) is low.

When the memory has completed the operation requested, CRDY0 (1A2) becomes active for 50 nanoseconds. This causes MDRCLK1 and MDRCLK0 to become inactive. The trailing edge of MDRCL0 resets DREQ0 if the D input is low, which occurs if CD170 is high. This condition results when the instruction format that is being read from memory is SF or RR. The trailing edge of MDRCLK0 also always resets IREQ0. Thus, the memory operation terminates after one halfword if the instruction is SF or RR.

If CD170 is low at the trailing edge of MDRCLK0, DREQ1 is not reset. A delayed MDRCLK propagates through the delay network (1D2) and produces a positive pulse at the output of the AND gate at 1K3. Since DREQ1 and SHP1 are both active, the CREQ flip flop is direct set and another request to memory is started. The second RQFF0 makes MDRCKL0 active, and the leading edge of MDRCLK1 sets the C011 flip flop (1D6). When memory places the second halfword of the instruction on the CD Bus, Bits CD16 and 17 and the operation code in UIR are examined (Sheet 10) to determine if the instruction format is RX3 or RI2. If it is, the RXIL0 signal (1E7) is made active. When CRDY0 is returned by memory, MDRCLK0 becomes inactive. If RXIL0 is low, the D input to the DREQ flip flop is high, and DREQ0 remains active. If the instruction format is RX1, RX2, or RI1, requiring only two halfwords from memory, RXIL0 is inactive and DREQ0 is terminated at the trailing edge of MDRCLK0.

If DREQ0 remains active after the second CRDY0 is received from memory, the second MDRCLK1 propagates through a delay network at 1D4 producing a delayed pulse DD1 (1J3) which causes another CREQ0, and causes the memory to read another halfword – the third halfword of RX3 and RI2 instructions – onto the CD Bus. The leading edge of the third MDRCLK1 causes the C001 flip-flop to reset. The AND-OR-Invert gate (1G8) decodes C000·DREQ1 and causes the D input to the DREQ flip-flop to become low. The trailing edge of the third MDRCLK0 then terminates DREQ0.

In addition to sequencing out the correct number of halfwords for instruction fetches, the signals developed on Sheet 1 also control loading of the data into the UIR, USR, UDR, and MDR. Whenever an instruction is fetched, the first halfword, on CD16:31, is always loaded into UIR (CD16:23), UDR (CD24:27), and USR (CD28:31) (Sheet 5). The load pulse LDUIR0 (5A3) is obtained from a gate at 4M2 and consists of MDRCLK0 gated by IREQ1, which is active only during the first halfword out of memory.

The second halfword is loaded into both the most and least significant halfwords of the MDR (Sheet 4). The 19-070 devices used for the MDR require a simultaneous low at the Clock (Pin 2) and Load (Pin 9) inputs. Loading occurs on the trailing edge of the Load input. The Clock input MCLK0 is pulsed low at the beginning of each instruction fetch by STB0 setting a two-gate latch at 4B3, and remains low until DREQ0A is terminated and at least one system clock CK0A has occurred. This never occurs until the second and, if required, third halfwords have been loaded into MDR, since DREQ0A is active during the entire instruction fetch.

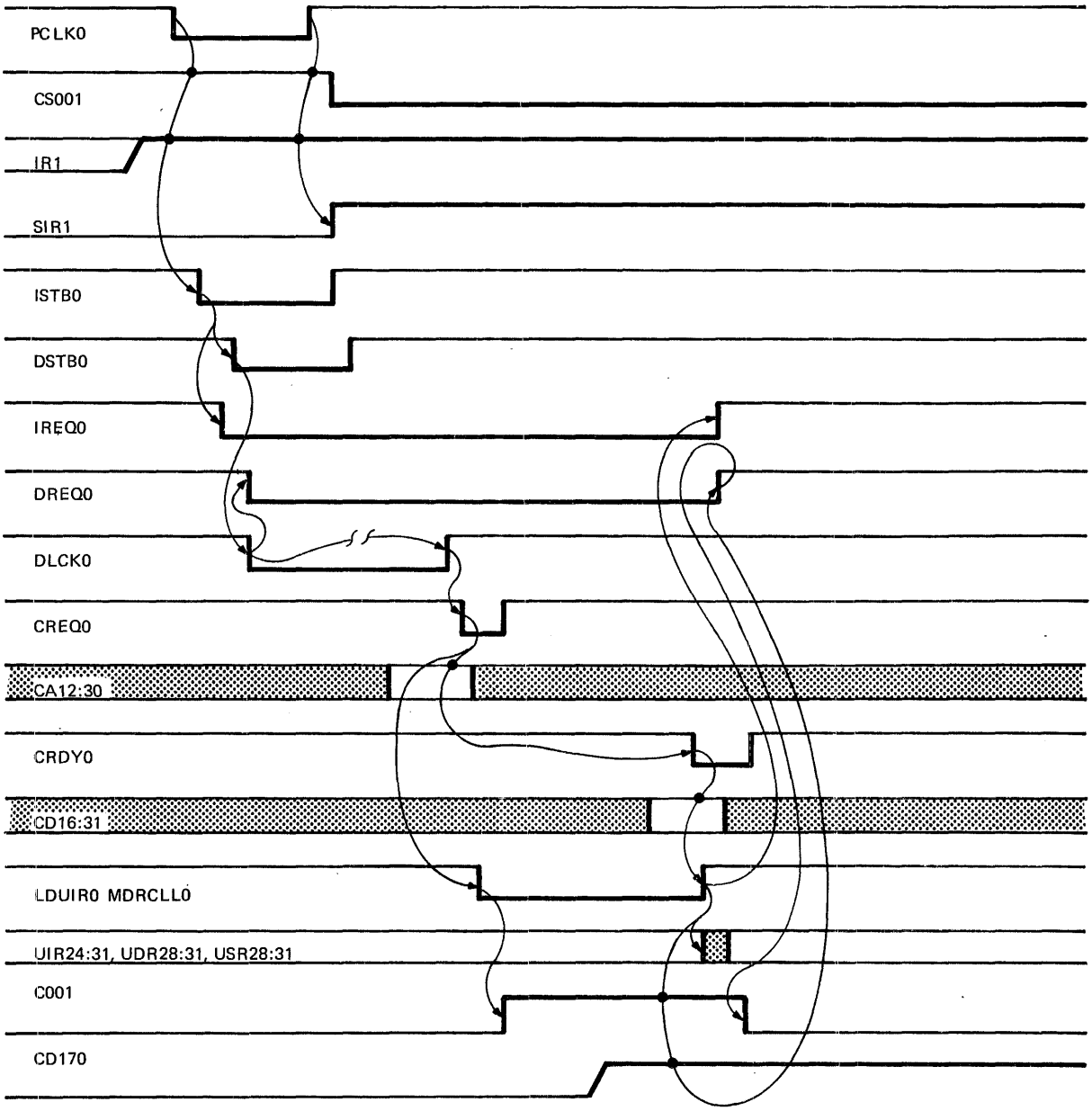


Figure 5A. Instruction Read, RR or SF Formats

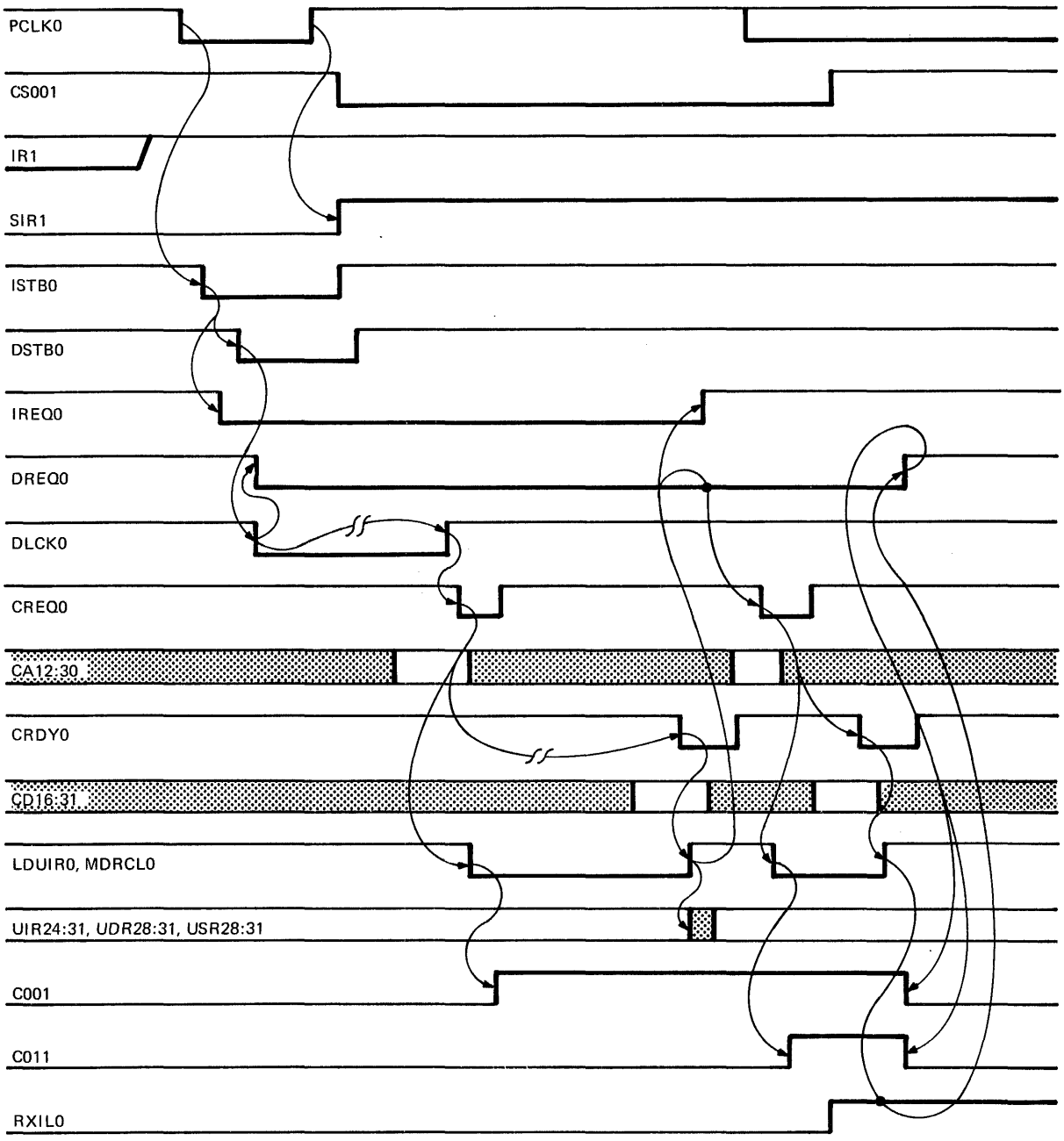


Figure 5B. Instruction Read, RX1, RX2 or RI1 Formats

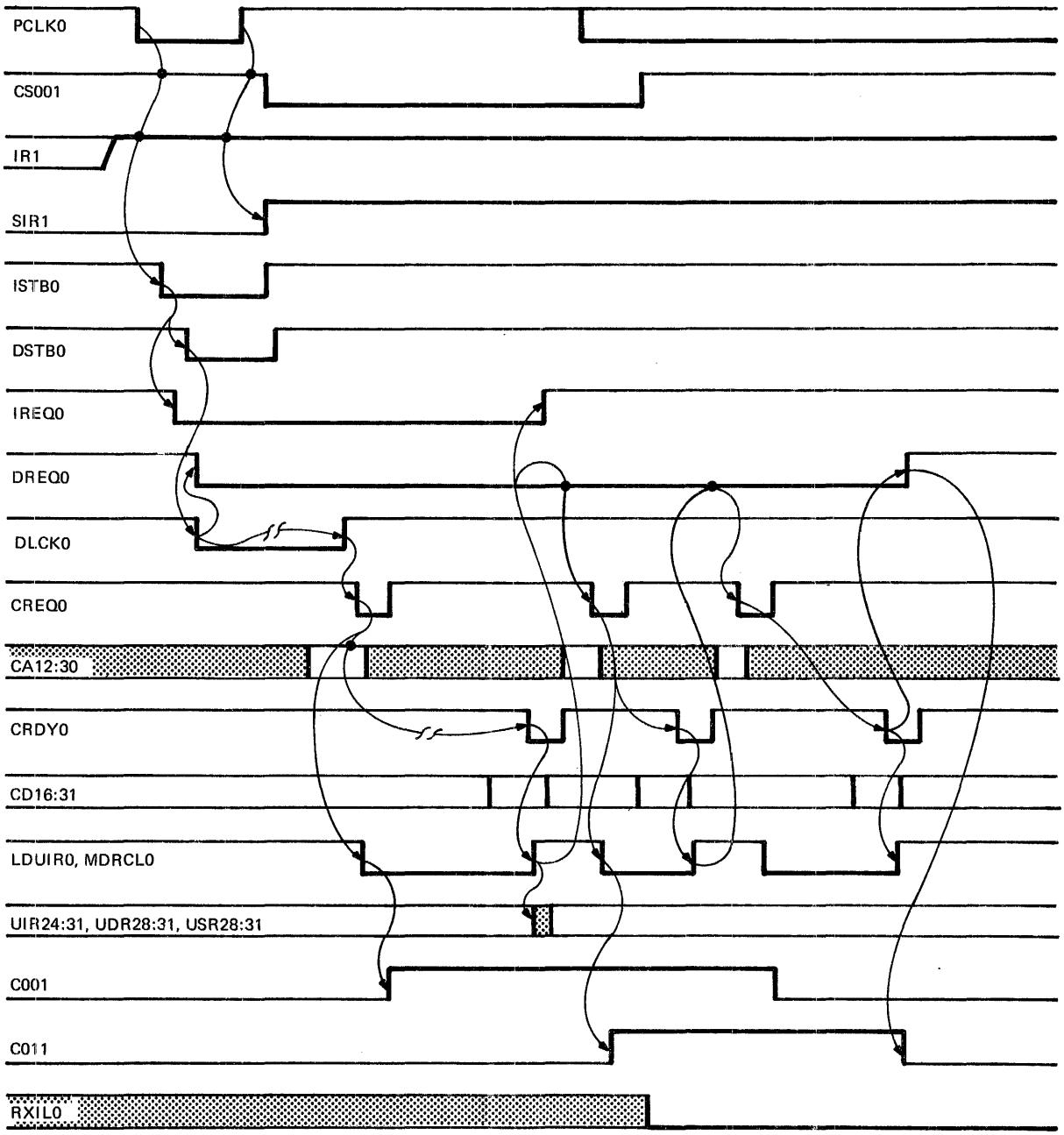


Figure 5C. Instruction Read, RX3 or RI2 Format

While MCLC0 is low, the second MDRCLK0 is gated through AND-OR-Invert gates (Sheet 4) since IREQ1A (4D1) and CC0 (4J2) are both low, causing the data at the inputs to MDR00:31 to be accepted. The data inputs to MDR16:31 are received from CD16:31 through MDX16:31 (Sheet 4) since LDMDR0 is high at this time. However, the 19-066 multiplexors to MDX00:15 (Sheet 4) are disabled because the control input CDXN0 is inactive. CDXN0 comes from an AND-OR-Invert gate (11C3), is inverted at 4J4, and is inactive when C011 is active, which occurs during the second and third halfwords. At this time, tri-state gates (Sheet 11) connect MDX00:15 to CD16:31, so that the data on CD16:31 (the second halfword) is written into both MDR00:15 and MDR16:31.

When the third halfword is available on CD16:31, CC0 is inactive and no load pulse appears at MDR00:15. However, a second load pulse appears at MDR16:31, and the new data on CD16:31 is written into MDR16:31, overriding the previously written second halfword.

When DREQ0A becomes inactive and a system clock has been generated, MCLK0 terminates, and the data which had been loaded into MDR00:31 appears in the outputs of the 19-070 devices.

Instruction Format Decoding and Storage. Since a possible micro-command could be "Increment MLC by the length of the last instruction" it is necessary to store information about instruction format. In addition, information is required to make MDR output appear as proper fullwords, although for RX1, RX2, and RI1 instructions, only the least significant halfword of MDR has meaningful data.

Part of format decoding is accomplished by PROM (I0B3). UIR outputs are used as address inputs to PROM, and the four outputs are RX001, signifying RX type instruction; RI021, signifying RI2 type instruction; RRSF1 signifying SF or RR format; and RI1X1, signifying RI1 type instruction.

A CC0 signal produces a clock signal when the second halfword of a two or three halfword instruction is available on the CD Bus. Figure 6 shows the relationship of CC0 to MDRCLK0. At the trailing edge of CC0, a flip flop at 10J6 is set whenever an RR, SF, RX3, or RI2 instruction is decoded from the PROM (10C3) and the states of CD16 and 17. Whenever this flip-flop is set, and CPC001 is active, an INCR1 signal is made active (10M6). CPC001 is a decode from the MC field which commands that the MLC be incremented by the length of the last instruction, so that INCR1 commands that the MLC be incremented by one or three halfwords (two or four bytes).

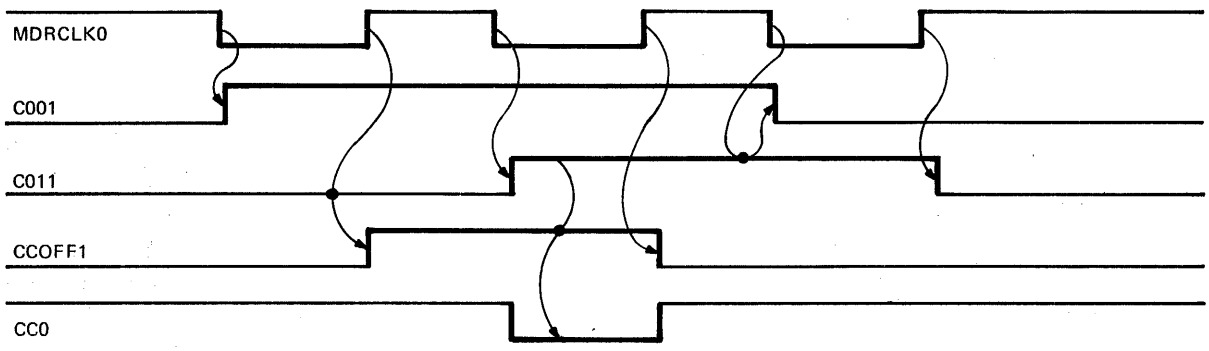


Figure 6. Second Halfword Clock Timing

Whenever an instruction is fetched and RRSF1 (10C3) is inactive, the instruction must have two or three halfwords – a gate at 10L7 decodes this condition and makes INCR021 active, commanding that the MLC be incremented by at least two halfwords (four bytes). Taken together, INCR1 and INCR021 indicate that MLC be incremented by one, two, or three halfwords.

The RXIL0 signal (10M5) is used (1E7) to cause the third halfword of RX3 and RI2 instructions to be read from memory. This signal comes from the RI021 output of the PROM and the output of a gate at 10G2 which decodes RX001·CD171·CD160·SDR0, which is the definition of an RX3 instruction format. The RXIL0 signal is not stored because it is only needed at the second halfword readout from memory.

Whenever the RX3 decode shown previously is active at the D input to the RX3 flip flop (10J1), a LDH0 signal which is used to load the MDR's most significant halfword is also used to set the RX3F1 signal.

A similar decode RX001·CD161·SDR0 is used to detect an RX2 instruction and set the RX2 flip flop (10J3). When the RX3 flip flop and the RX2 flip flop are set, two signals, RXID0A and RX1D0B, are made active to control the arithmetic function of SM2X (Sheet 9). The decode of RX001·CD160·CD170·SDR0 is used to detect an RX1 instruction and set the RX1D0 flip flop (10M1). This flip flop is reset during the first halfword of an instruction request or upon loading the MDR by a microcode instruction. This signal (12H7) is used to control the effective MDR output as read to the B Bus. For RX1 instructions, B00:15 are made equal to MDR16 whenever MDR is gated to the B Bus. The RX2 output (10J4) is also used (12H7) to extend the least significant halfword on the B Bus, but for RX2 instructions it is MDR17 which is used. Another circuit (12H9) switches the signal BIT161 to MDR171 for RX2 instructions.

A RX3D0 signal (10M5) is used in CPB to control double indexing. This signal is enabled by RX3EN1 which is made active at the start of each memory reference and inactive whenever MAR is loaded. This occurs when MAR←YX+SX.

A MSIG0 signal (10N4) is used to indicate to CPB that an RX2 instruction is being executed. This signal is tested by the micro-code for certain instructions. When an instruction other than RX2 is being executed, MSIG0 can become active from other sources. JUTY1 is made active for instructions other than RX2 to indicate to CPB that MSIG0 should be ignored.

4.3.4 Data Read Operation. (see Figure 7 Data Read Operation). When the MC field of the RIR in the CPB indicates a memory Data Read operation (see Section 4.3) the following signals are made active: SDR0, SDR1 (2N2), DRDW1 (2M4), and SDRDW1 and SDRDW0 (2R9). In addition, if the command is for halfword read, SRH0 (2N2) is made active, and if the command is a privileged read, SPROT1 (2N2) is also made active.

When DRDW1 is active during Control State 1, and if no interrupts are being processed, STRT1 (12A2) is active. When CK1A becomes active, DSTB0, STB0 and DLCK0 are initiated.

DSTB0 causes DREQ0 (1R7) to become active, and the trailing edge of DLCK0 (after 100 nanoseconds if there is no change in Base Register or after 190 nanoseconds if the Base Register address changes) causes CREQ0 to be initiated. This makes MDRCLK1 and MDRCLK0 active. When data is available on the CD Bus, memory generates CRDY0, which terminates MDRCLK0 and MDRCLK1.

Since a Data Read operation is proceeding, SIR1 (1G4) is inactive, and $\overline{\text{SIR0}}$ ($\overline{\text{1G7}}$) at the input to the AND-OR-Invert gate is high. At the leading edge of MDRCLK1, the C001 flip-flop is set, and the output of the AND-OR-Invert gate connected to the D input to the DREQ flip-flop becomes low. At the trailing edge of MDRCLK0, the DREQ flip-flop is reset, terminating memory Data Read operation.

Data is loaded into the 32-bit MDR from the 32-bit CD Bus on the trailing edge of MDRCLK0. At this time SIR1 (4A3) is low, enabling DREQOA to pass through two gates and become MCLK0.

Since SDR1 (4A2) is active, MDRCLK1 is gated to Load inputs (Pin 9) from all stages to the MDR, and data is loaded at the trailing edge of MDRCLK0. However, DREQ0A is terminated at the trailing edge of MDRCLK0, so that the new data appears at the outputs from MDR at the trailing edge of MDRCLK0.

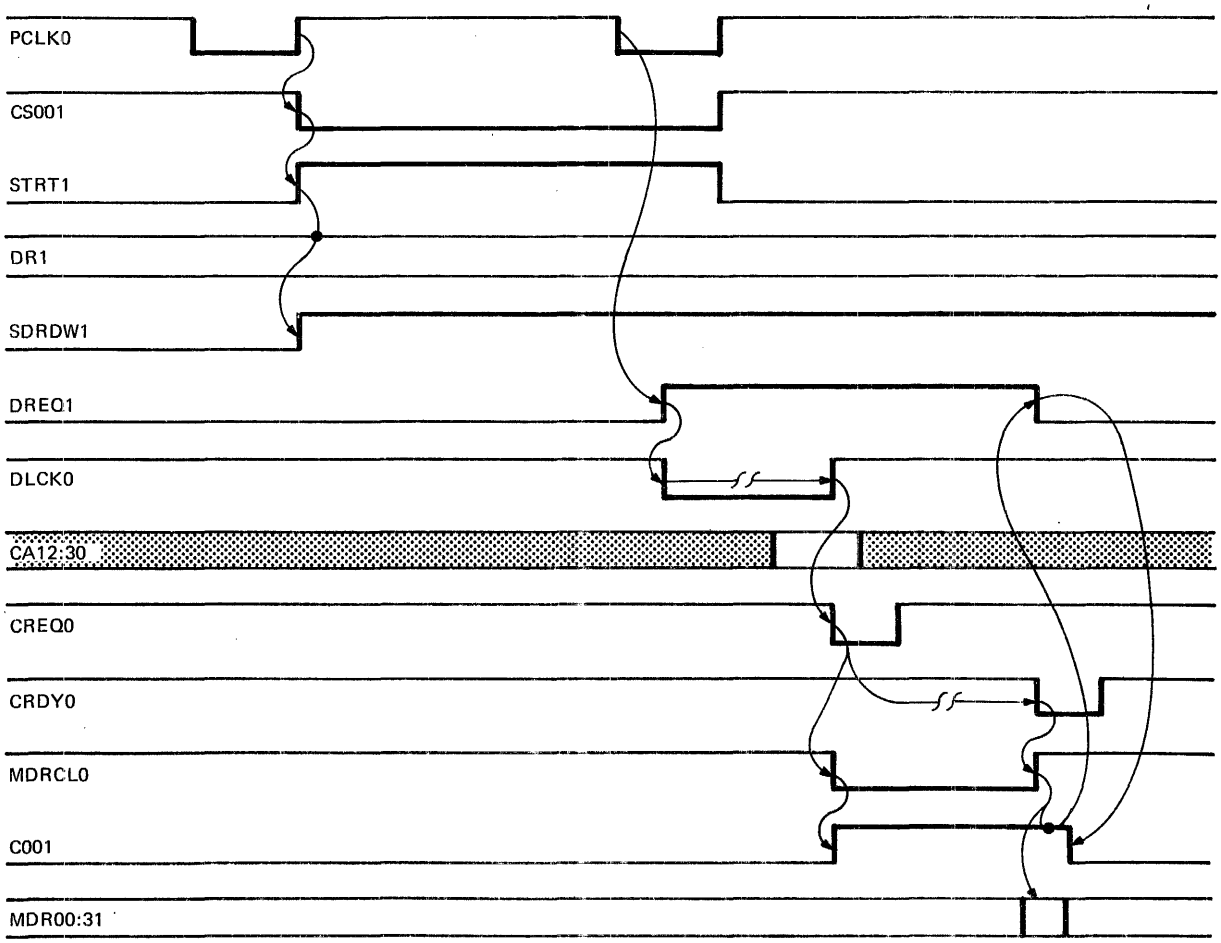


Figure 7. Data Read Operation

The Read operation does not distinguish between fullword and halfword read. However, when halfword read is commanded, SRH0 (2N2) becomes active. This causes the B-Bus multiplexor select signal BMXSLA (12N7) to be set on the following system clock CK0A, and the B-Bus multiplexor is switched from MDR00:31 driving B00:31, to MDR16:31 driving B16:31, and MDR16 driving B00:15. The Halfword Sign Bit 16 is propagated through the most significant bits of the B Bus.

The Read operation does not distinguish between normal read and privileged read. However, when a privileged read is decoded from the MC field, SPROT1 is reset, and all operations are accomplished with program addresses, without relocation and protection.

4.3.5 Data Write Operation (see Figure 8 Data Write Operations). When the MC field of the RIR in the CPB indicates a memory Data Write operation (see Section 4.3) the following signals are made active: SDW1, SDW0 (2N3), DRDW1 (2M4), and SDRDW1 and SDRDW0 (2R9). If the command is a privileged write, SPROT1 (2N2) is also made active.

All of the operations described previously for data read occurs for data write, except for loading MDR from the CD Bus. Before the Write operation is initiated, the required data loaded into MDR by the micro-program, as described in Section 4.4.4. MDR is gated to the CD Bus (Sheet 11). When SDW1 is active (11A3), the control inputs to the tri-state gates (Pins 1 and 15 of the 19-134 devices) become low. This places the output of MDR00:31 on CD00:31 for writing into memory.

When SDW0 (4C3) is active, the gates producing MCLK0 are inhibited, and, since the clock input to the 19-070 devices of MDR are not enabled, the data in MDR is not disturbed during the data Write operation.

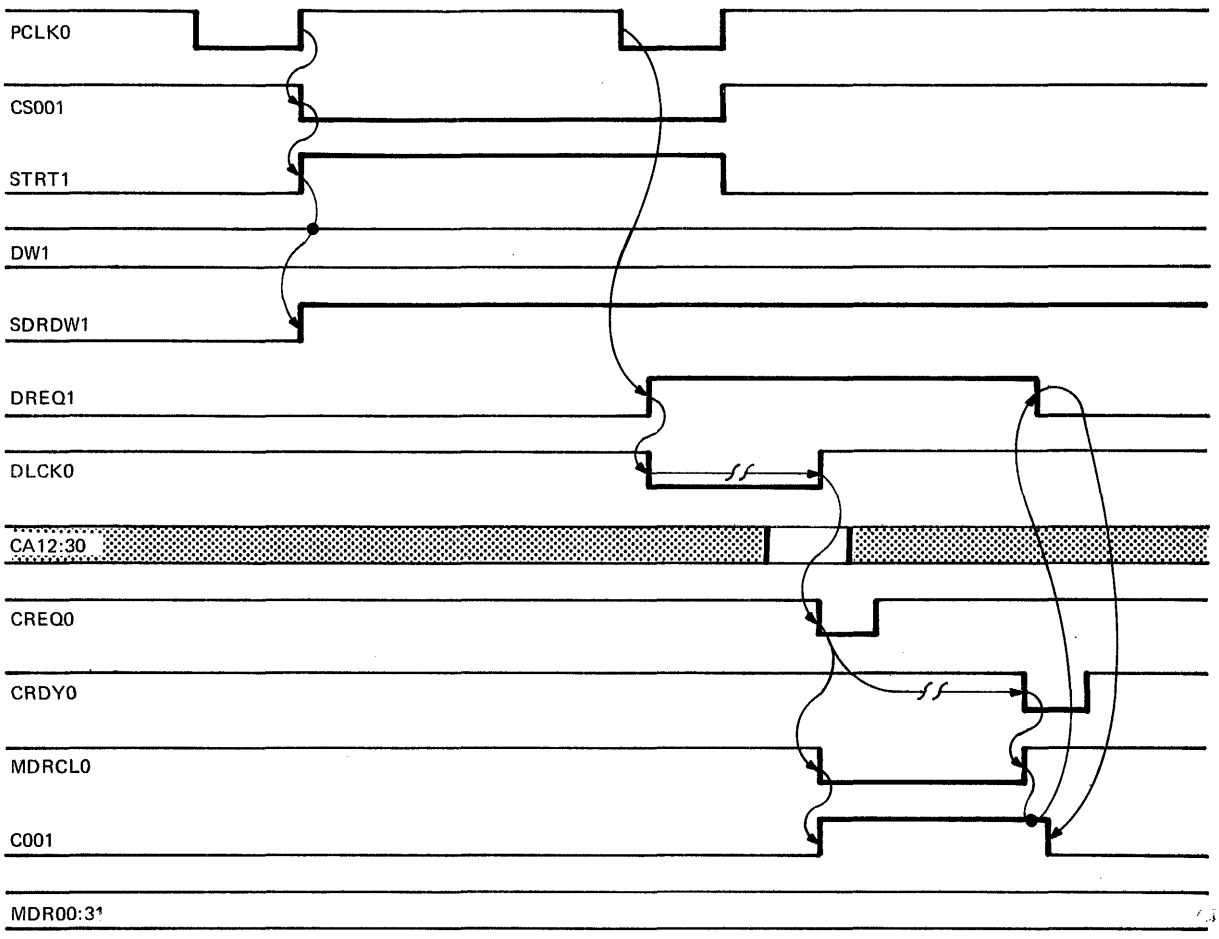


Figure 8. Data Write Operations

4.3.6 CD Bus Interface. The CD Bus interface is a bi-directional interface with various parts of CPA, including multiplexing between the even and odd halfwords CD00:15 and CD16:31. Figure 9 shows the various data paths which are involved in this interface.

For Fullword Data operations, CD00:31 are connected to MDX00:31, a tri-state multiplexor, and hence to the inputs of MDR00:31 for loading from memory. The outputs of MDR00:31 are connected through CD gates to CD00:31 for writing into memory.

For Halfword Write operations, MDR00:31 are connected to CD00:31 although the data on CD00:15 is meaningless. Memory insures, based on the Memory Command Bus CMC00:02, that only CD16:31 are written for Halfword Write operations.

For Halfword Read operations, CD00:15 are multiplexed into MDR00:15, and CD16:31 into MDR16:31, although the data on CD00:15 is meaningless. When the MDR is multiplexed to the B Bus for Halfword Read operations, B00:15 is connected to MDR161, propagating the Halfword Sign Bit MDR16 through the most significant bits (B00:15).

During instruction fetches, for RX1, RX2, and RI1 formats, the second halfword of the instruction appears on CD16:31. Through the upper CD gates in Figure 9, and through MDX16:31, this halfword is written into both halfwords of MDR. For these formats, MDR00:15 is replaced on the B Bus with MDR161 for RX1 and RI1, and MDR171 for RX2 formats.

For RX3 and RI2 formats, the second halfword is also loaded into both MDR halfwords. The third halfword also appears on CD16:31 and is loaded into MDR16:31 through MDX16:31, so that MDR00:31 ends up with the second instruction halfword in MDR00:15 and the third halfword in MDR16:31.

When conditions are correct for writing into the MAC Base Registers (BR), the data in MDR is placed on the CD Bus as if to write into memory (the data is actually written into memory) and the memory command (fullword or halfword, even or odd halfword) determines the connections from CD to BR. For fullword write the inputs to BR04:15 are connected to CD04:15 through MDX00:15, and the inputs to BR16:27 are connected to CD16:27 through MDX16:31. For writing the most significant (even) halfword BR04:15 only, the data, which appear on CD16:31 is connected to the inputs of BR04:15 through the CD gates on Sheet 11. For writing a halfword into BR16:27, the data is connected through MDX16:31.

When IR27:31 is to be read out, MDR is disconnected from CD by disabling the lower CD gates, and a set of four tri-state gates at 11A1 are enabled, connecting IR27:31 to CD27:31.

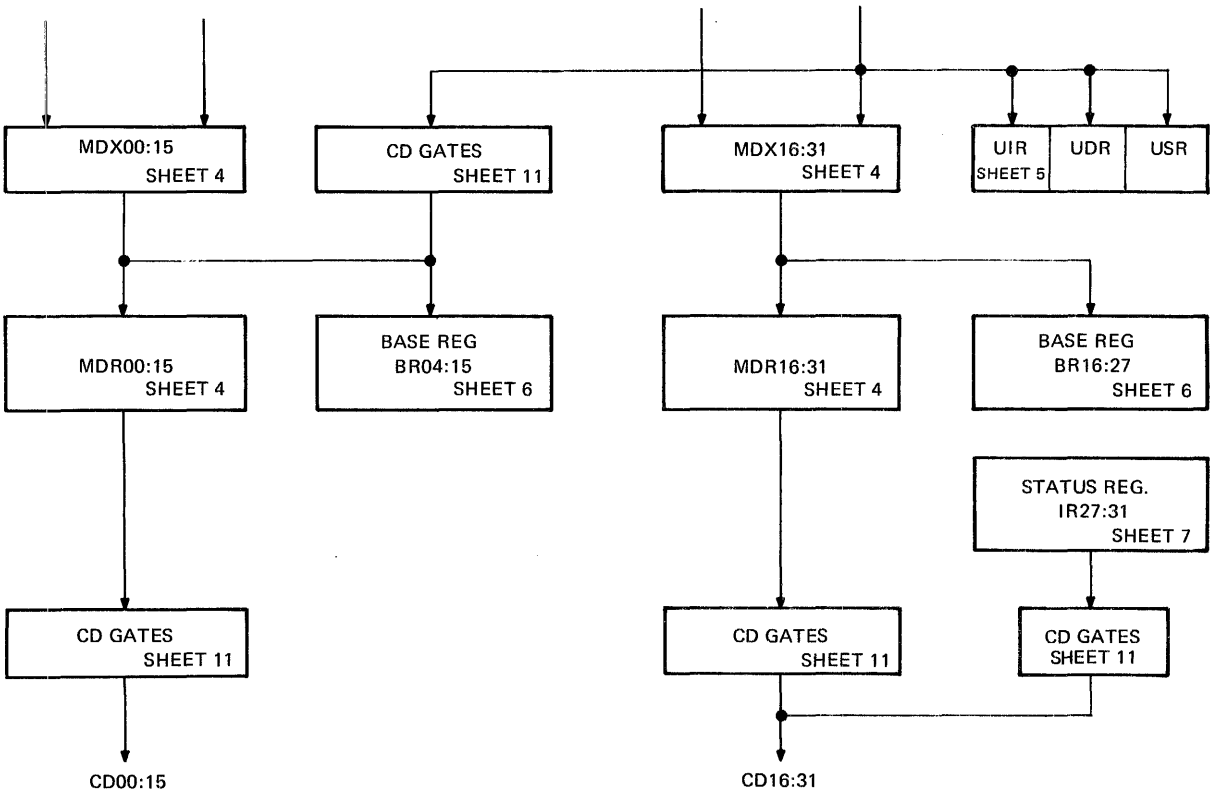


Figure 9. CD Bus Interface

4.3.7 Incrementing MAR and MLC. Certain codes of the MC field indicate that the MLC or the MAR must be incremented before the next instruction is executed. Table 12 lists these micro-commands with the appropriate MC fields.

TABLE 12. INCREMENT MICRO-COMMANDS

	MC00:03
INCREMENT MAR BY 4	X101
INCREMENT MLC BY LENGTH OF LAST INSTRUCTION	X001

The increment commands are decoded (2E5) into CPC001, to increment MLC; and CPC011, to increment MAR.

Incrementing MLC. Whenever CPC001 (2E5) is active, and the Processor is in Control State 0 (CS001 at 10J8 is active) one or both of the increment signals INCR1 and/or INCR021 are active, depending on the length of the previously executed instruction (see Section 4.3.3).

On Sheet 3, there is a four-bit address loop which is used to increment MLC by two, four, or six depending on the state of INCR1 and INCR021. The 19-131 quad flip-flop (3D4) stores the four least significant bits of MLC. The inputs to these flip-flops come from a 19-066 multiplexor (3D1), and the inputs to this multiplexor are either SR28:31, for loading MLC from the S Bus, or ADA28:31, the outputs of a 19-133 four-bit adder (3D8). As long as LDMLC0 (3C2) is inactive (high) the multiplexor, flip flops, and adder form a loop. At each system clock CK0B, the contents of the quad flip flop are updated with the outputs of the four-bit adder. As long as INCR1 and INCR021 are both inactive, no change occurs in MLC. When INCR1 becomes active, the output of the adder increases by two, and this incremented data is loaded into MLC28:31 at the next system clock. When INCR021 becomes active, the output of the adder increases by four, and this incremented data is loaded into MLC28:31 at the next system clock. If both INCR1 and INCR021 are active, the output of the adder increases by six, and this incremental data is stored in MLC28:31 at the next system clock.

Whenever the incremented output of the adder overflows ADA28, a carry is propagated MLC12:27 from the C4 terminal of the 19-133 adder (3E8). The carry input to MLC15 is brought to 6A5 to cause an increment in the MAC Base Register (BR) address.

Incrementing MAR. Whenever the "Increment MAR by four" command results in CPC011 becoming active, MAR12:29 (Sheet 3) is incremented by one. However, an increment of one at MAR29 represents an increment of four bytes, since MAR30:31 are stored in two flip-flops at 3A7 and 3B7, and these two bits are not incremented. CS001 is used (3F3) to enable counting of MAR, so that only one increment occurs for each increment command.

4.4 S Bus Operations

All data and addresses from the Processor to memory communicate via the S Bus and CPA. The data are stored in a register on CPA (SR00:31), the outputs of which are connected to the inputs to MDR, MLC, MAR, and the B multiplexor.

The S Register shown on Sheet 5 is loaded from the S Bus on the leading edge of CPX (5F8 and 4K3) which is synchronous with the leading edge of the system clock.

4.4.1 S Address Decoding. Information about the destination of the data on S00:31 is obtained on SSEL00:04 from the CPB. Whenever data is available on the S Bus for loading into a Processor register, a STRT1 signal is made active by CPB, and STRT0 (2B7) enables a 19-129 3-to-8 decoder (2B7). Table 13 shows the coding of SSEL00:04 for loading MDR, MAR, and MLC; the 19-129 decoder implements the decoding in accordance with this table.

4.4.2 MAR Load. MAR is a 20-bit register which consists of two flip-flops at 3A7 and 3B7, and five 19-135 4-bit counters. The two flip-flops store the two least significant bits of MAR (MAR30:31) which do not require incrementing. The 4-bit counter stores MAR12:29, since MAR is incremented on command by four bytes only.

Loading of MAR occurs whenever SSEL00:04 decodes to LDMAR0 active (low). During this condition the trailing edge of the system clock CK1A (3A2) causes the data on SR12:31 to be loaded into MAR12:31 (Sheet 3).

4.4.3 MLC Load. MLC is a 20-bit register which consists of a 19-131 quad flip flop (3D4) and four 19-135 4-bit counters. The quad flip flop, which stores MLC28:31, is loaded through a 4-bit multiplexor (4D2) from SR28:31 when LDMLC0 (from SSEL00:04) is active (low) and MLC12:27 is loaded directly from SR12:27 on the trailing edge of the system clock CK0B.

4.4.4 MDR Load. MDR00:31 (Sheet 4) is loaded from SR00:31 through a multiplexor MDX00:31 whenever LDMDR0 (decoded from SSEL00:04) is active. Loading occurs whenever the Load input to the 19-070 devices (Pin 9) and the Clock input (Pin 1) are simultaneously low.

LDMDR0 gates CK1B (Sheet 4) into the Load inputs. LDMDR1 gates CK1B into the MCLK0 inputs (Sheet 4). Loading effectively occurs at the trailing edge of the system block.

TABLE 13. BUS SELECT DECODING

BUS ADDRS (HEX)		S-BUS (06:10)	B-BUS (20:24)	A-BUS (11:15)
00:OF and M37		UR	UR	UR
00:OF and M37		FR	FR	FR
10:17		MR	MR	MR
18	11000	YS	YS	YS
19	11001	YD	YD	YD
1A	11010	MLC	MLC	YX
1B	11011	MDR	MDR	YDP1
1C	11100	MAR	MAR	--
1D	11101	PSW	YSI	PSW
1E	11110	YDI	YDI	--
1F	11111	NULL	NULL	NULL

A – Select: YDP1 – Even YD converted to Odd Number by forcing LSB to ONE. Also manipulated by RWC0 line for 64 bit Read operations

B – Select: On RX3 operations and B-Field = X'1B' (MDR),
1. SX2 = 0, Convert X'1B' to X'19' (4D)
2. SX2 = 0, Convert X'1B' to X'1F' (NULL)

S – Select: On 64 bit Write operations, Even S-SEL converted to Odd number by forcing LSB to ONE

4.5 B Bus Operations

All data from MLC, MAR, and MDR (except for the 4-bit SX2 field) communicate from CPA to the Processor on the B Bus (B00:31). A 32-bit multiplexor shown on Sheet 13 selects from among the sources.

4.5.1 B-Bus Source Selection. B-Bus source addresses are received by CPA on a 5-bit BSEL00:04 Bus and a single S2B0 line. When S2B0 is active, it overrides the BSEL00:04 address and causes the B Multiplexor on Sheet 8 to connect SR00:31 to B00:31. When S2B0 is active it disables the decoder at 12K5 which produces select signals for the B Multiplexor and enables BMXNA1, which enables the eight 4-bit multiplexors (Sheet 13) to connect the S Register to the B Bus. When S2B0 is inactive, BMXNA1 is inactive, and the SR-to-B multiplexors are disabled. If BSEL001 is active, a RGEN0 signal (12N6) is active, enabling a 19-129 3:8 decoder (12K4). The select signals BSEL011:041 are decoded into BMXNB1, BMXNC1, and BMXSLB1. When BMXSLB1 is low, the MDR is multiplexed to the B Bus. When BMXNC1 is low, and BMXSLB1 is high, MLC12:31 is connected to B12:31, and B00:11 is made inactive. When BMXNC1 is low and BMXSLB1 is low, the outputs SUM2X12:31 of the program address ALU are multiplexed to B12:31.

4.5.2 MDR Halfword Operation for Halfword Data Read. When a halfword is read from memory into MDR16:31, it is necessary to convert this to fullword format by extending Bit 16 across B00:15. This is accomplished at 12M7 by latching up BMXSLA1 in a flip-flop whenever the SRH0 signal (12H7) is active. Since at this time, during a Data Read operation, RX2F0 (12G9) is high, BIT161A and BIT161B (12N9) are both the same as MDR161. When BMXSLA1 is active (high) (Sheet 13) and BMXNB1 is low (selecting the MDR to drive the B Bus) each of the B-Bus signals B00:15 are connected to BIT161A or BIT161B.

4.5.3 MDR Halfword Operation for Instruction Fetches. When an RX1 or RI1 instruction is read from memory into CPA, the second halfword is loaded into MDR16:31. When MDR is gated to the B Bus, MDR161 must be propagated through B00:15 in the same manner as when a Halfword Read operation is performed, and the same circuits, using the RX1D0 or RI1X0 signals in place of SRH0, cause this result to be obtained. When an RX2 instruction is fetched from memory, the RX2F0 and RX2F1 signals (Sheet 12) are made active. This causes BMXSLA1 to become active, propagating BIT161A and BIT161B on B00:15, and connecting BIT161A and BIT161B to MDR171, so that MDR171 is propagated through B00:15 in place of MDR161.

5. CPB FUNCTIONAL DESCRIPTION (Refer to Functional Schematic 35-537D08.)

As stated previously, the logic of the control module is divided among the three CPU boards – The CPA, CPB, and the CPC. The 35-555 CPC board contains the register stacks and optional Writable Control Store, and the 35-536 CPA board contains the memory control and base register circuits. The major portion of the CPU's control logic, i.e., the control store, state counters, clock, register gating, interrupts, Module 0 gating, and their associated logic is contained on the 35-537 CPB board. The following information refers exclusively to the 35-537 CPB board and its associated schematics.

5.1 State Counter and Control

The CPU control logic is governed basically by two flip-flops which determine the current state of the Processor. The flip-flops are referred to as Control State A (CSA) and Control State B (CSB). The CPU can be in one of the four possible binary combinations of these two elements, which are decoded as Control State 0:3.

The four states of the CPU are represented by the transition diagram in Figure 10.

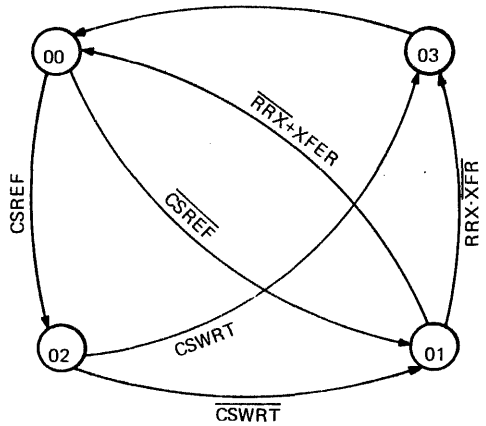


Figure 10. CPU State Diagram

The basic functions of the CPU can be described by correlating the significant logic events of this diagram.

5.1.1 Control State 0 (CS00). An instruction sequence begins in CS00. This state constitutes instruction decoding time. Module number and function selects are gated to the Control Bus. The registers to be selected are decoded, and gated onto the A and B Busses. Logical decisions are made as to the next state transition, micro control of memory, and interrupt recognition. All micro control of memory with the exception of data read and data write is accomplished on the transition from CS00.

When the CPU makes a transition from CS00, it enters Control State 1 (CS01) or Control State 2 (CS02) depending on whether the micro-instruction is a Control Store Reference (CSREF). CSREF is selected by the I Bit (see Figure 10) of the micro-instruction.

5.1.2 Control State 2 (CS02). CS02 is only entered for the purpose of reading data from or writing data into the control store memory. When it is entered for reading, the intent is to replace the data on the B Bus with the data stored at the address specified by the B Bus before signaling a module to Start (STRT). This is accomplished on the transition from CS02 to Control State 1 (CS01). When the state is entered for Control Store Writing (CSWRT), there is no further module communications, and the next transition is to Control State 3 (CS03) to gate the next sequential instruction from control store.

5.1.3 Control State 1 (CS01). This state is entered from CS00 if there was no Control Store Reference (CSREF), or from CS02 when the instruction specified an indirect reference from control store, and is the state where communications to the other modules is performed. At this point, data is valid on the A and B Busses and if the module selected is other than Module 0, STRT is active and the CPU halts until the referenced module returns the Module Finished signal (MFIN).

The transition from CS01 can be to CS00 or CS03.

Control State CS01 to CS03. This transition only occurs on an RRX instruction if the transfer is conditioned and logically should not occur (see RRX instruction description). This transition is necessary because the instruction at the transfer location has been read from the control store during CS01 and the next sequential instruction must then be selected during CS03.

Control State CS01 to CS00. This transition is the default transition when the transition to CS03 is not made.

The ROM instruction Register (RIR) is always loaded on the transition from CS01.

5.1.4 Control State 3 (CS03). This state is entered from CS02 after a Control Store Write (CSWRT) or on a conditional RRX transfer if the transfer is not taken. The only logical function performed in CS03 is addressing the next sequential micro-instruction. The RIR is always loaded on the transition from CS03.

5.1.5 Control State logic. The control state flip-flops (14H2) are initialized to CS03 by XCLR0 on system clear or whenever an address is jammed into the ROM Location Register (RLR). These flip-flops are implemented in D type logic optimized to implement the state diagram of Figure 10. The logic implementation is shown in Table 14.

TABLE 14. CONTROL STATE LOGIC IMPLEMENTATION

TRANSITION	CSA ACTIVE LOGIC	CSB ACTIVE LOGIC	COMMENTS
CS00 to CS02	NONE	CS001·RIR051·MOD000	CONTROL STATE 0 AND INDIRECT BIT SET AND NOT MODULE 0
CS00 to CS01	CS001·(RIR050 + MOD001)	NONE	CONTROL STATE 0 AND MODULE 0 OR INDIRECT BIT NOT SET
CS02 to CS01	CS021	NONE	ANY TRANSITION FROM CS02 SETS CSA
CS02 to CS03 CS01 to CS00	CS021 NONE	CS021·RIR031·RIR021 NONE	CONTROL STATE 2 AND CSWRT INSTRUCTION
CS01 to CS03	RRX1·CS011·RIR251·MSIG1·JUTY0	RRX1·CS011·RIR251·MSIG1·JUTY0	RRX INSTRUCTION AND CS01 AND CONDITIONAL AND MSIG1 AND MSIG NOT INHIBITED BY CPA (JUTY0)*
CS03 to CS00	NONE	NONE	

* For an explanation of JUTY1, see Section 4.3.3

The control state flip-flops are encoded as CS00:03 by gates located at 14M. Note that STRT is encoded as CS011. It is inhibited by INT1 or TRAP121 which are interrupt signals and effectively neutralize the instruction to cause a null cycle to fetch the interrupt instruction.

5.2 Clock and Control (Sheet 13)

The clock for the CPU is a gated oscillator which uses a dynamically selected tap of a delay line to establish the clock frequency. Figure 11 shows a simplified illustration of the clock logic.

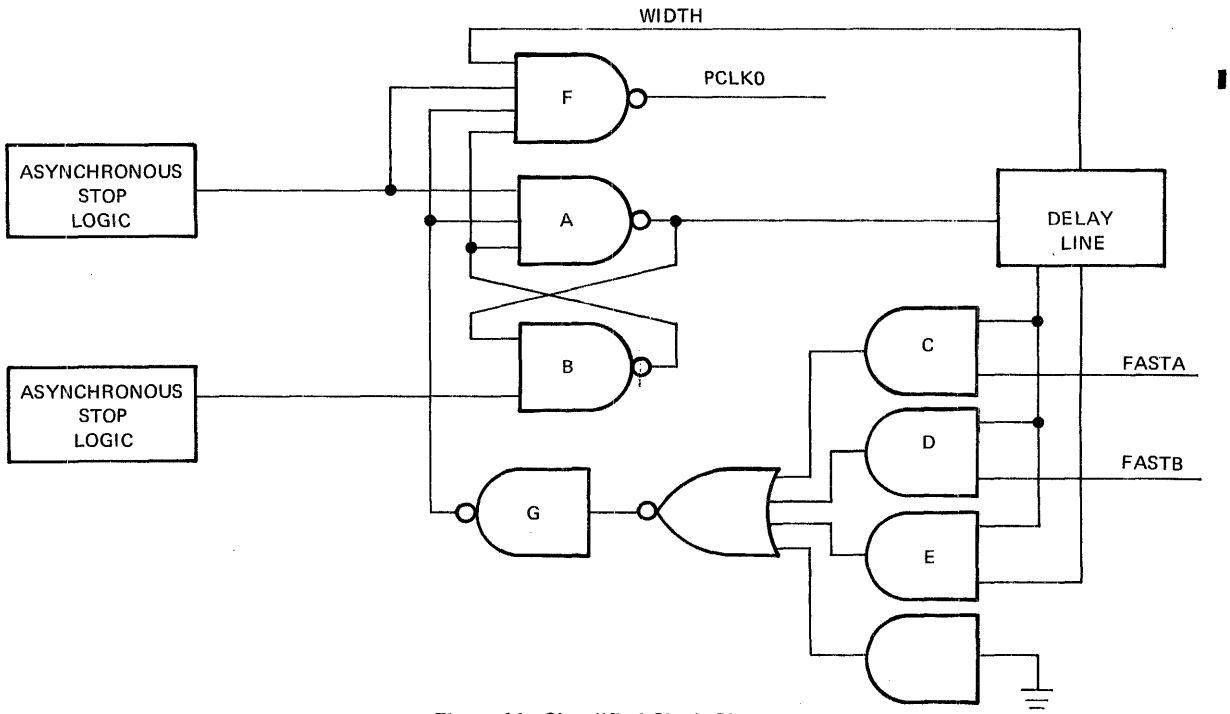


Figure 11. Simplified Clock Circuit

The basic oscillator is comprised of the delay line driver (Gate A), the delay line itself, three gates which are used to dynamically select the desired delay (Gates C, D, and E), and Gate G which provides the necessary inversion for oscillations.

The oscillator can be gated by additional inputs to Gate A. One input is provided by synchronous logical conditions which would cause the clock to stop (i.e., MFIN, or memory interlocks). The second input is from asynchronous conditions (i.e., external stops, manual clock control) and is enabled and latched by Gates A and B to provide proper synchronism to the oscillator. Gate F provides the primary clock for the CPU (PCLK0) and is enabled by the oscillator and the two stop functions. An additional input is a width control from the delay line to modify the duty cycle of the primary clock.

As mentioned, the taps of the delay line are dynamically selected by Gates C, D, and E. The purpose of this is to provide two basic clock frequencies to the CPU. The necessity of this is caused by decoding and access time of the control state and address gating. Since this time is normally longer than one normal clock period, the address gating is decoded so that if the normal transition of the CPU state for the instruction is from CS00 to CS01, both states can be used to access the next micro-instruction. However, if any other state is entered, only one state is provided to access the next instruction and the clock is stretched out. The logic is designed such that if either Gate C or D is enabled, that state is provided the minimum time period; if neither is enabled, the longer period is established.

The actual logic for the clock circuits is on Sheet 13 of the CPB schematics. There are, however, two delay lines cascaded to provide the necessary delay. It should also be noticed in the actual circuit that an eight position switch allows selection of four different taps for each delay for marginal, nominal, and slow clock adjustments. (Note that only one switch of each set can be closed at one time.)

The logic represented by FASTA and FASTB on Figure 11 can be observed as CS01 and CSB0 $\overline{(MOD000 \cdot RIR051 + MOD001 \cdot RIR031)}$, which indicates that CS01 is always a fast clock unless there is a control store reference (MOD000·RIR051) or the instruction is a Register Link (MOD001·RIR031). CS02 and CS03 are always afforded a slower clock.

The synchronous stop logic is provided by the 19-062 gate (13F3). The following logical conditions can be observed at this gate.

CS011·D1·IREQ1. This logic is used to stop the Processor in CS011 when the decode bit is set (use the op-code of the instruction for a control store vector) and the memory has not completed the reading of the op-code (IREQ1). The LC delay network on IREQ1 is used to delay the response to IREQ to provide adequate access time of the control store when IREQ is removed.

STRT1·CS011·MOD000·MFIN0. This logic stops the Processor clock when communicating with the other modules until MFIN is returned.

INT0·DREQ1·CS001 (MC001 + MC011 + MC021 + MC031). This gate stops the Processor clock in CS00 if it is a valid instruction (INT0), if any memory control is selected, and memory is busy (DREQ1).

The remaining gate stops the Processor clock at CS00 if it is not an immediate and the MDR is selected on the B Bus or at CS01 if the MDR, MAR, or MLC are selected as S Bus destinations and the memory is busy (DREQ1).

5.3 Control Store

The CPU is directed through its paces by instructions fetched from control store and loaded into the ROM Instruction Register (RIR). The sequential and non sequential (branch) flow of instructions is controlled by the CPU logic by the control store address selection which determines where the next instruction is coming from.

A simplified block diagram of this control is shown in Figure 12.

RIR. The ROM Instruction Register is loaded at the beginning of each instruction from the control store and holds the instruction for interrogation by the control logic while data or the next instruction is accessed. The RIR and MC field logic is located on Sheet 11 of the schematics.

Control Store. The control store holds the micro-program of the computer. Data may also be retrieved from the control store. The maximum addressable range of control store is 4K words. The 8/32 micro-program is contained in 1,280 words of control store (Sheet 10).

RLR. The ROM Location Register stores the address of the current micro-instruction. It is loaded at the beginning of each instruction from the control store address gates unless it is an interrupt or an execute type instruction. It is not changed on an interrupt so that the address from the interrupted sequence can be preserved if desired (Sheet 9). Execute instructions are described in the Micro Instruction Reference Manual, 29-438.

RLC. The ROM Location Counter is used to add one to the RLR on sequential instructions. It is the RLR + 1 loaded back into the RLR that causes the RLR to increment. The switch input from the test aid is a second input to the RLC. When it is desired to JAM an address into the RLR, the test aid logic clears the RLR and gates the desired logic to the RLC and through the address gates to select the desired starting address (Sheet 9).

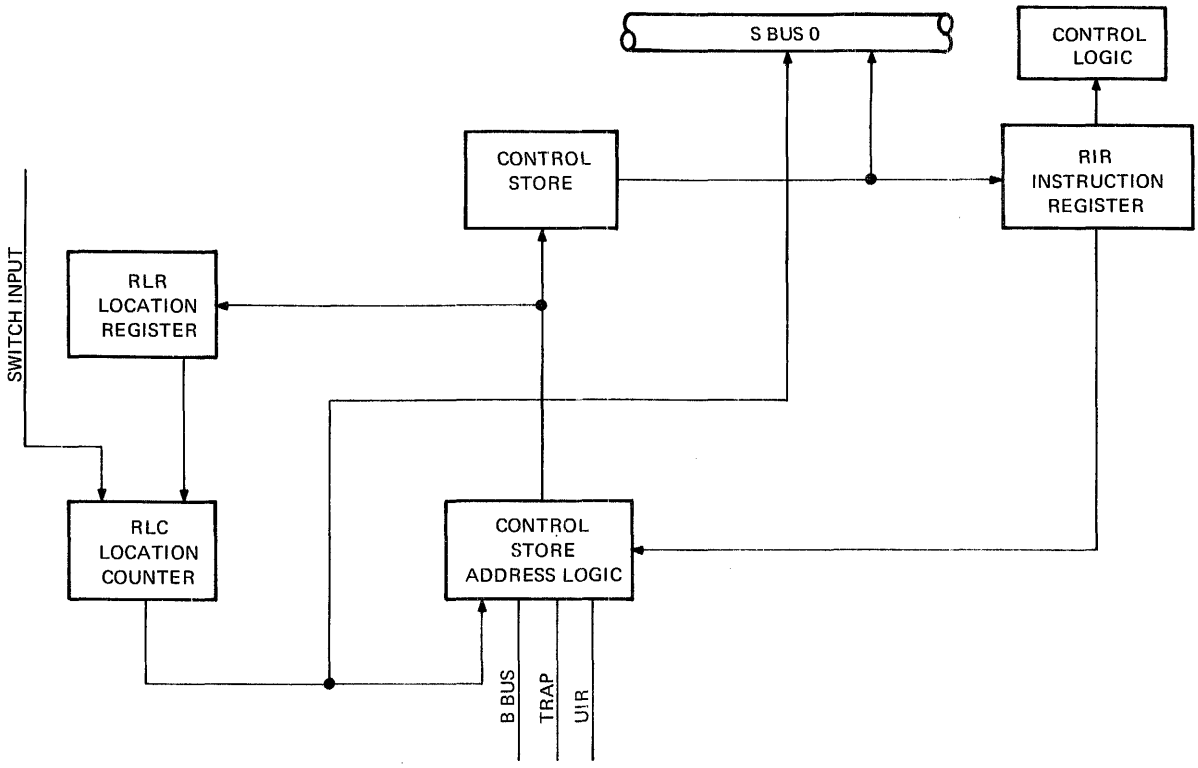


Figure 12. Simplified Control Store Diagram

Control Store Address Gates. The Control Store Address gates select one of five possible inputs for control store addresses. The simplified diagrams (Figures 13A and 13B) show the multiplexor selection for the various address paths. By correlating the diagrams to the actual schematics on Sheets 8 and 9 it is seen that when NEXT is gated (next sequential address) the actual data is RLC4:15. In the same manner for REGLNK or CSREF it is B20:31, and for ADRS LNK it is RIR14:25.

5.4 Bus Selection

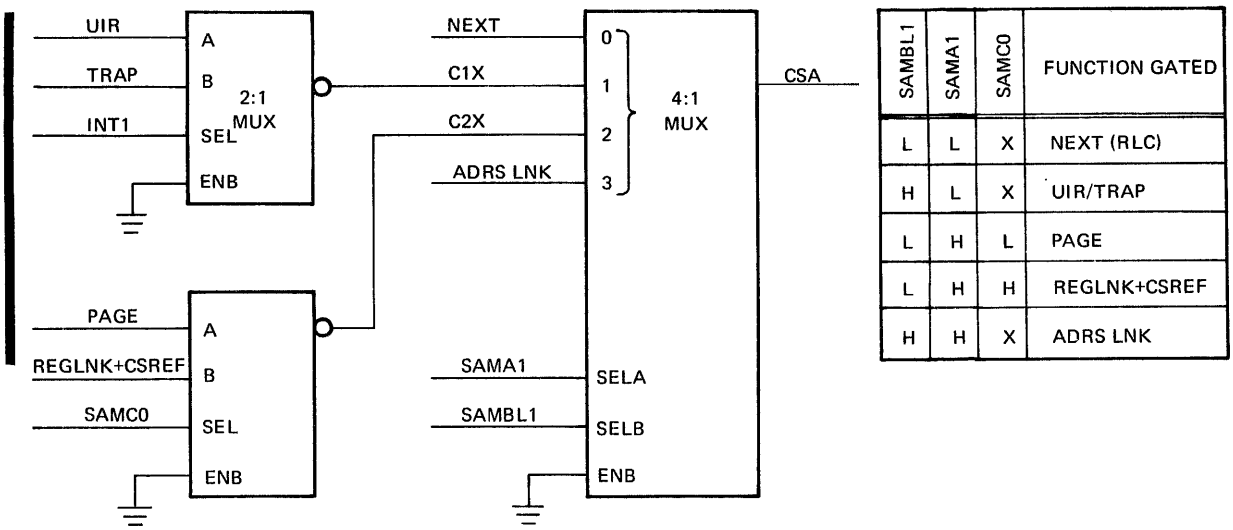
5.4.1 ASEL. The effective register to be gated into the A Bus is selected by ASEL00:03 (3H2). The actual bus address can be derived from the A Field of the instruction, the YS register, or the YD register. Signal AYDS0 (3A3) decodes from the A field of the instruction whether the A field of the instruction directly or the YS/YD register is used for the ASEL and selects the appropriate side of the multiplexor (3H2). When the YS/YD selection is made, that selection is made by RIR151 at the multiplexor (3C2). The AEN0 signal is used to null select the field if the YX (user index register) is selected and index register zero (no selection) is made to gate zeros to the A Bus.

5.4.2 BSEL. The effective register to be gated to the B Bus is selected by BSEL0:3 (3M4). The effective bus address can be derived from the B field of the instruction, the YS register, the YD register, or the second level index register in the case of an RX3 instruction. The BYDS0 signal (3J8) is used to select either the B field of the instruction or the YS/YD/SX2 register at the multiplex (3K6).

The BYDS0 signal is inactive unless the YD or YS register is selected by the micro-instruction and RIR20:24 (the B field of the instruction) is gated at BSEL0:4. When the B field selects the YS/YD register, the BYSD0 signal becomes active and the YS or YD register is gated to the BSEL from the multiplexor (3C7).

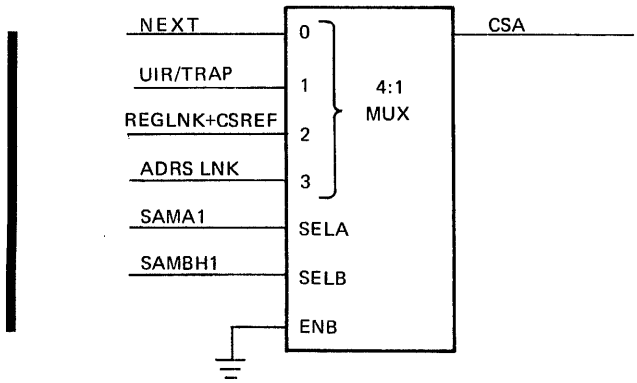
An exception is created when the MDR is selected during an RX3 instruction when the signal RX3D1 from CPA is active. In this case, the BYDS0 signal is made active again and the second level index register field of the MDR, which is sent from CPA as SX28:31 is selected through the multiplexors (2K2 and 3C7) becomes the address of the B register. The SX2NZ1 signal (3E8) determines if the register selected is zero and causes a null selection on the B Bus to be disabling (BEN0) to the BSEL multiplexor. The intent of this is to cause the first and second level indexing to be performed in the ALU as the CPA hardware adds the MDR to MAR to allow RX3 type indexing to be performed transparent to the micro-programmer. See the Micro Instruction Reference Manual, 29-438.

5.4.3 SSEL. The effective address to be gated to SSEL0:4 is determined by the SEL field of the instruction. The multiplexor (4E1) selects either the S field itself (RIR06:10) or the YS/YD register for the effective address. When the effective address is YS/YD, the multiplexor (4C2) selects the proper register as per RIR101 from the S field. The effective S address is then latched at CS001 and held available during CS001 of the next instruction when the CPC is storing the results back into the register stack.



SAMBL1	SAMA1	SAMC0	FUNCTION GATED
L	L	X	NEXT (RLC)
H	L	X	UIR/TRAP
L	H	L	PAGE
L	H	H	REGLNK+CSREF
H	H	X	ADRS LNK

Figure 13A. Control Store Address Gating Low (CSA10:15)



SAMB1	SAMA1	FUNCTION GATED
L	L	NEXT (RLC)
H	L	UIR/TRAP
L	H	REGLNK+CSREF
H	H	ADRS LNK

Figure 13B. Control Store Address Gating High (CSA4:9)

5.5 Interrupts

The Model 8/32 employs a hardware priority interrupt scheme which has nine vector traps. See the Micro Instruction Reference Manual, 29-438.

There are three different interrupt mechanisms.

1. MAI interrupt. The MAI interrupt is an immediate interrupt and cannot be disabled. It is caused by a data read/write violation in the Memory Access Controller (MAC) on CPA. When this interrupt is sensed, the next instruction is interrupted and a trap to 207 is taken. It is the highest priority interrupt. In addition, all registers are inhibited from changing until the interrupt is acknowledged. This is accomplished by the TRAP120 term in the STRT logic (14J5).

   A MAI interrupt is acknowledged when MAI0 (12B8) becomes active, setting the flip-flop at 12D8. This is syncronized by the flip-flop at 12G8 which causes the flip-flop at 12M3 to set at the transition from CS01 or CS03. This flip-flop (12M3) being set activates the INT1 signal which tells the CPU logic that an interrupt is in process (INT1 causes the CPB logic to in effect, "throw away" the current instruction without operating on it while it fetches the next instruction from the interrupt trap). INT1 stays active until the next transition from CS01 or CS03 when the instruction at the trap address is loaded into the RIR. The flip-flop at 12G8 is also input to the priority encoder (12H5) where it forces the trap address "7" for the interrupt vector.

2. Group Interrupts. The second class of interrupts are second priority interrupts and are enabled/disabled as a group by the flip-flop at 12M3. This flip-flop (12M3) may be set/reset by Module 0 instructions, and is automatically enabled at the end of an emulation sequence (D1·PASS0·CSA0) to field all active interrupts and disabled at the entry to a new emulation sequence (D1·PASS0·CSA1). Interrupts in this group are also enabled by PSW bits as described in Section 5.7.

   Interrupts in this group are interrogated and latched in registers CS01 (12D3 and 12D6). These registers are prevented from changing while an interrupt trap is being processed to keep the address stable to the control store. These interrupts are then conditioned by their respective PSW bits (note that ATN0:3 interrupts are conditioned by a PROM addressed by several PSW bits at 12D2), and activate the priority encoder 12H4. If this device is enabled by TEN0 the next CS01 or CS03 sets the flip-flop at 12M6 causing the Processor to activate INT1 and begin an interrupt cycle.

3. Priviledged/Illegal Interrupts. These interrupts are the lowest priority interrupts and are activated only at the end of an emulation sequence if there are no other interrupts pending. All possible instructions are programmed as privileged, illegal, or neither in a PROM addressed by the UIR (Users Instruction Register). The output of this PROM is then interrogated at the end of each emulation sequence (D1·PASS0·CSA1) for privileged or illegal instructions. An exception is the MAC instruction interrupt which disables the illegal instruction interrupt and sends an op-code of 3FF as UIR24:31, and sets the flip flop at 12M7 thus activating INT1 and causing the CPU to begin the interrupt sequence.

5.6 PSW Register

The PSW register is an architectural feature of the user level machine and is used to enable interrupts, select register stacks, and contains the Condition Code for user level branch tests.

The PSW (Sheet 5) is loaded when it is addressed as the S Bus destination. A peculiarity of the PSW is that the Condition Code (PSW28:31) can be modified by the current instruction if it is enabled by the microcode (see Section 3.5.3) and the module selected is manipulating the CPU flag register (SCC0 active). See Section 3.5.7. This logic is accomplished by multiplexing the S BUS which is latched in SR28:31 (4C5) at the clock's leading edge with the data to be jammed into the Processor flag register (4E7 and 4E8) from CC0, VCC0, GCC0, and LCC0 at the multiplexor (4E5). A Composite Clock CCCLK0 (4K7) is generated for the PSW28:31 latch.

5.7 Branch Control

The PSW Condition Code (PSW28:31) (4K5) and the Processor flag register (4E7 and 4E8) can be tested for conditional branches by Module 0 instructions.

The PSW Condition Code is compared to the YD register (14B7) for the BTC and BFC tests of the user level architecture and, input to the 8:1 multiplexor (14F5) along with the Processor flag register where the appropriate input is selected by the F field of the instruction as an input to the PASS gate (14K8). PASS0 and PASS1 is tested throughout the CPB logic where pertinent for branch decisions.

5.8 A, B, and S Gating

Various registers are gated to the A, B, and S Busses by the CPB.

YSI and YDI. These registers are gated to the B Bus by the multiplexor at 2H4.

PSW. This register is gated to the A Bus by the tri-state buffers (4M4, 5M3, 5M6, and 5M7).

RIR20:31. These bits are gated to the B Bus for immediate operands (with Bit 20 extended as the sign bit) (Sheet 6).

CSD00:31. The Control Store Data Bus is gated to the S Bus for control store data references (Sheet 7).

RLC04:15. The RLC is gated to the S Bus for link addressing (Sheet 7).

5.9 Test Aids (Sheet 1).

The following test aids are incorporated on the CPB board.

5.9.1 Address Match/Stop/JAM. A control store address can be selected on the three hexadecimal rotary switches located on the front edge of the CPB board (1B2, 1B4, and 1B7) which can be used to sync on, stop on, or JAM to the RLR for a starting address. These switches are compared to the Control Store Addresses (CSA04:15) at the comparators (1G2, 1G4, and 1G7) and produce an output which is ANDed with Clock (CLK1B) and CS000 (1J6) to provide a scope SYNC at TP101-7 (1M6). The output of these switches is also routed to the RLC to provide a way to force a predetermined address. (See Section 5.3.)

0 - Off
1 - MATCH
2 - SINGLE
3 - JAM

5.9.2 MATCH/JAM/SNGL. A rotary switch in conjunction with a push button switch (1M7, and 1M9) is used to control three flip-flops for the purpose of stopping at a selected control store address (MATCH), JAMMING the RLR to a desired address, and single stepping the CPB clock.

When the switch is in the SNGL mode (SNGL LED bit) (1N7), every Processor clock resets the RUN flip-flop (1L8) which generates KLCLK0, an input to the CPU clock circuit. A subsequent toggle of the momentary push button sets the RUN flip-flop and allows the clock to run and generate another clock, resetting the RUN flip-flop.

When the switch is in the JAM mode, a toggle of the push button sets the JAM flip-flop (1L7) which enables JB041:051 to the RLC and causes SETRLC0 (1L5) to clear the RLR.

When the switch is in the MATCH mode, an address comparison sets the MTCH flip-flop (1L6) which activates KLCLK0 in the same manner as SNGL and halts the Processor clock. Subsequently toggling the push button resets the MTCH flip-flop causing the Processor to run until it once again gets an address comparison.

6. CPC GENERAL DESCRIPTION (see CPC Block Diagram Figure 14).

Processor board CPC consist of the A Stack (ASTK), B Stack (BSTK), A Address Logic (AAD), B Address Logic (BAD), Write Clock Timing Logic (WCLK) S Buffer Register (SBUFF), and Register Set Select Logic (RSSL).

ASTK is shown on Functional Schematic 35-555 Sheet 1, BSTK on Sheet 2, AAD and BAD on Sheet 4, WCLK on Sheet 5, SBUFF on Sheet 3, and RSSL on Sheet 3 and Sheet 5.

ASTK is a 256X32 Read/Write Register array. The 32 inputs are connected to the outputs of SBUF (SB001:311) and the 32 outputs (A000:310) are connected to the A Bus which runs along the lower back panel. There are eight address inputs (AAD000:040, AAD051, PSW260A, and PSW270A), a Bus Enable control (ASTKN0), and a Write Clock (WCLK0A).

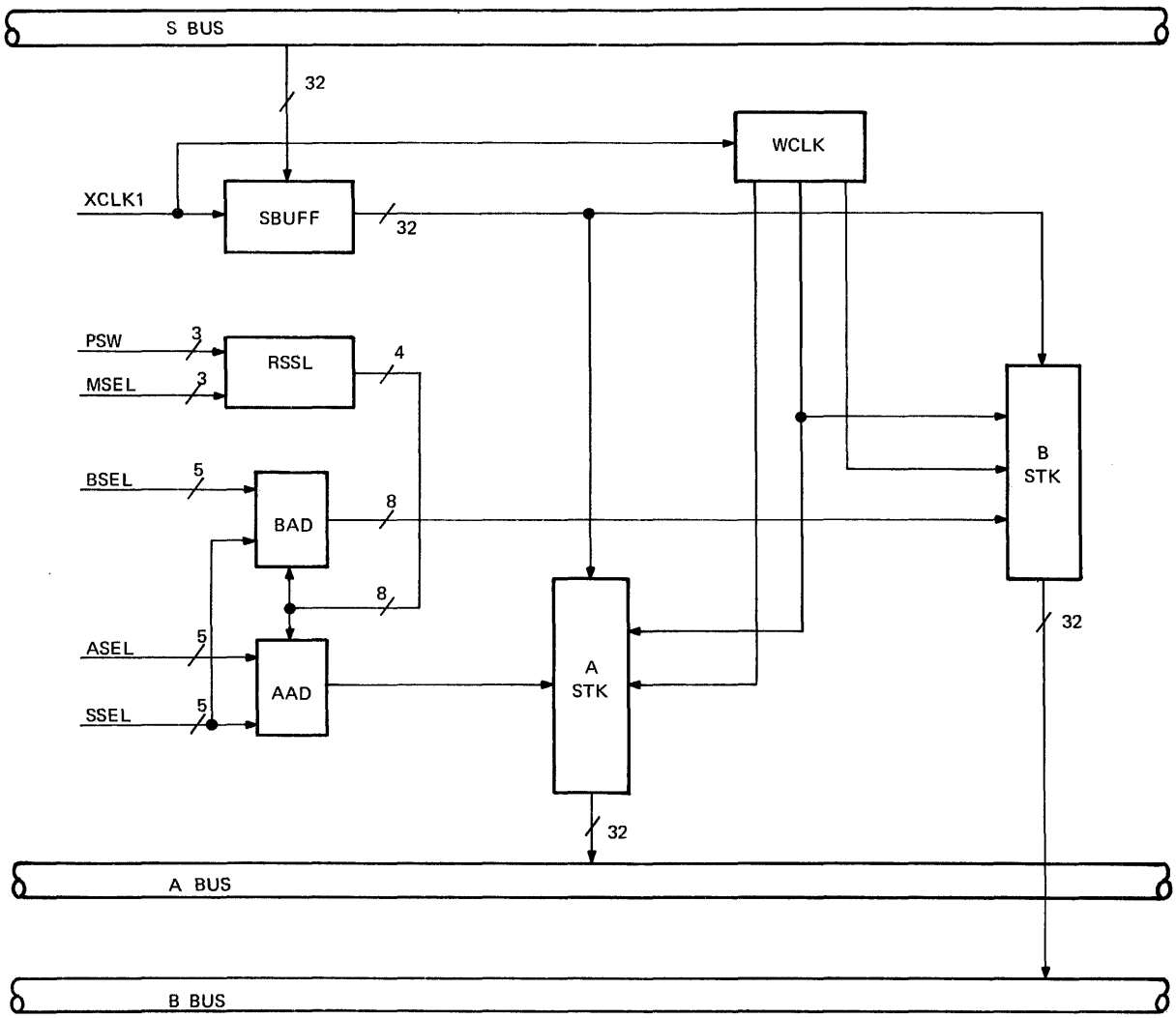


Figure 14. CPC Block Diagram

BSTK is identical to ASTK, except that it is connected to the B Bus (B000:310) and receives B Address inputs (BAD000:040, BAD051, PSW260B, and PSW270B) and B Bus Enable (BSTKN0).

ASTK and BSTK can be individually addressed to the A Bus and B Bus, but are always simultaneously selected for loading from SBUFF.

RSSL receives three PSW bits (PSW260, 270 and 251), three Module Select bits (MSEL000:020), and three internal signals (AKL0, BKL0, and SKL0). AKL0 is active whenever a Micro-program Register (MR0:7) is selected for the A Bus independent of the state of the PSW bits. BKL0 is similarly active for the B Bus. SKL0 is active whenever MR is selected to receive data from SBUFF. The four outputs of RSSL (PSW260A, 260B, 270A, and 270B) are used as stack address bits, together with AAD051 and BAD051, to select one of eight sets, from 16 registers each, in ASTK and BSTK for the 16 General Registers (GR0:F).

AAD receives a 5-bit A Select Bus (ASEL001:041), a 5-bit S Select Bus (SSEL001:041), PSW Bit 251 from the CPB, and control signals from WCLK and RSSL. ASTK address bits AAD000:040 and AAD051 are decoded from these inputs.

BAD receives a 5-bit B Select Bus (BSEL001:041), an S2B0 signal, the other inputs to AAD (except ASEL), and produces BSTK Address Bits BAD000:040 and BAD051.

SBUFF is a 32-bit register having inputs connected to the S Bus (S000:310) and having outputs (SB001:311) connected to the data inputs of ASTK and BSTK. The clock input to SBUFF is SCLKI from WCLK.

WCLK produces the timing signals for CPC. Inputs from CPB are PCLK0, the System Clock; STRT0, the Start command for most operations; and SCLR0, the System Clear signal. An input from the ALU is RWC0, which initiates and times 64-bit register Read and Write operations. Outputs from WCLK are WSELI, WSELIA, WSEL0, WSEL0A, WCLK0, WCLK0A, SODD041, and DWC0. The latter two signals are also used in 64-bit Read and Write operations.

6.1 A and B Stacks (ASTK and BSTK).

Refer to Functional Schematic 35-555, Sheets 1 and 2. The A and B Stacks are functionally identical, so only the operation of the A Stack is described.

The Stack (ASTK) consists of 32 19-077 256x1 Read/Write memories. The data input terminal of each bit cell is connected to the appropriate output of SBUFF (SB001:311). Whenever the enable signal ASTKN0 is active (low) and a Write Clock (WCLK0) is made active (low), the data levels "1" or "0", present at each data input terminal is stored in the bit location for that cell determined by the state of the eight address lines (AAD000:040, AAD051, PSW260A, and PSW270A) which are common to all 32 cells. Thus, after a simultaneous active state of ASTKN0 and WCLK0, lasting at least 40 nanoseconds, the 32-bit output of SBUFF is stored in a specific location in ASTK.

When WCLK0 is made inactive (high) and ASTKN0 remains active, the stored data from the selected location is presented at the ASTK outputs which are connected to the A Bus (A000:310).

When ASTKN0 is made inactive (high) the ASTK outputs are placed in a high-impedance state, removing ASTK from the A Bus.

Figure 15 shows the timing of the ASTK address signals, control signals, and outputs for a Write operation at the nominal 130 nanoseconds clock period. These are described in more detail in Section 6.4.

6.2 S Buffer (SBUFF)

Refer to Functional Schematic 35-555, Sheet 3. SBUFF consists of eight 4-bit 19-131 registers. The data input to each cell of each register is connected to the appropriate S Bus signal (S000:310) and the data output of each cell is connected to the appropriate data input of ASTK and BSTK (SB001:311).

The clock inputs (SCLK1) are derived from a NAND gate at 5C5. For 32-bit operations, SCLK1 is PCLK0 inverted. For 64-bit operations, two SCLK1 active states are generated; the first during the first WCLK0 derived from RWC0 and the second SCLK1 during the subsequent PCLK0. SBUFF is loaded on the leading edge of SCLK1.

Figure 16A shows SBUFF timing for a 32-bit write, and Figure 16B shows the timing for a 64-bit write.

6.3 Stack Addressing

(Refer to Functional Schematic 35-555 Sheet 4 and Figure 17).

The stack addressing scheme is described in terms of ASTK. To explain BSTK, substitute B for A.

6.3.1 Read Addressing. ASTK is addressed for reading to the A Bus with ASEL001:041, MSEL000:020, PSW 251, PSW260, and PSW270. There are 9 sets of 16 registers each of which are addressed as Fixed-Point General Register (GR) Sets 0:7, and Micro-programming Register (MR).

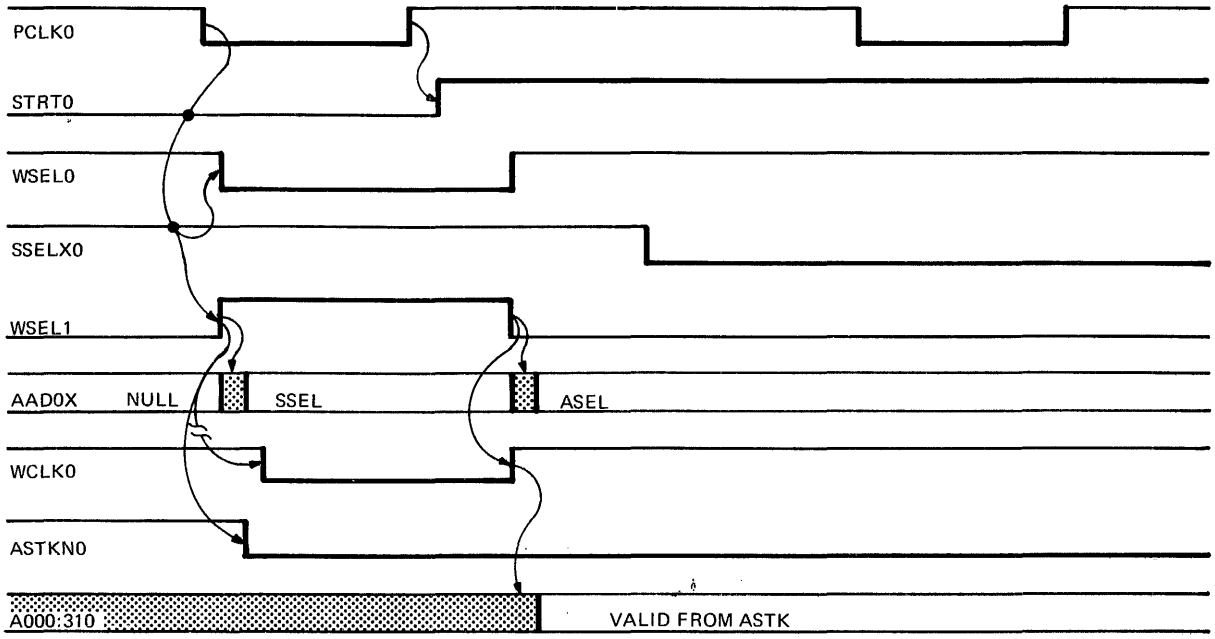


Figure 15. A Stack Timing Diagram, 32-Bit Write

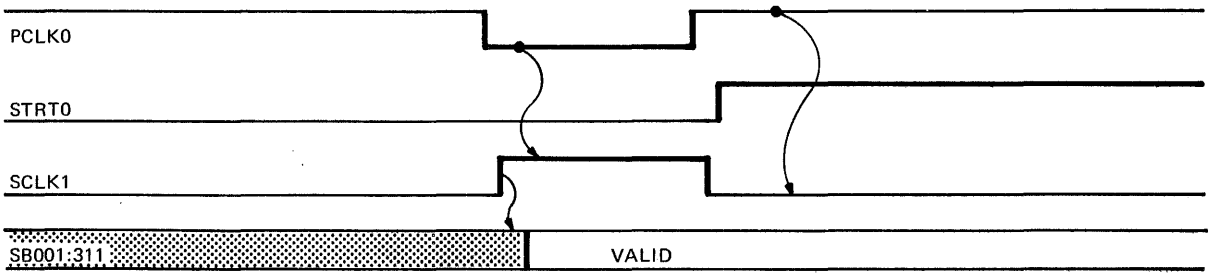


Figure 16A. SBUFF Timing, 32 Bit Write

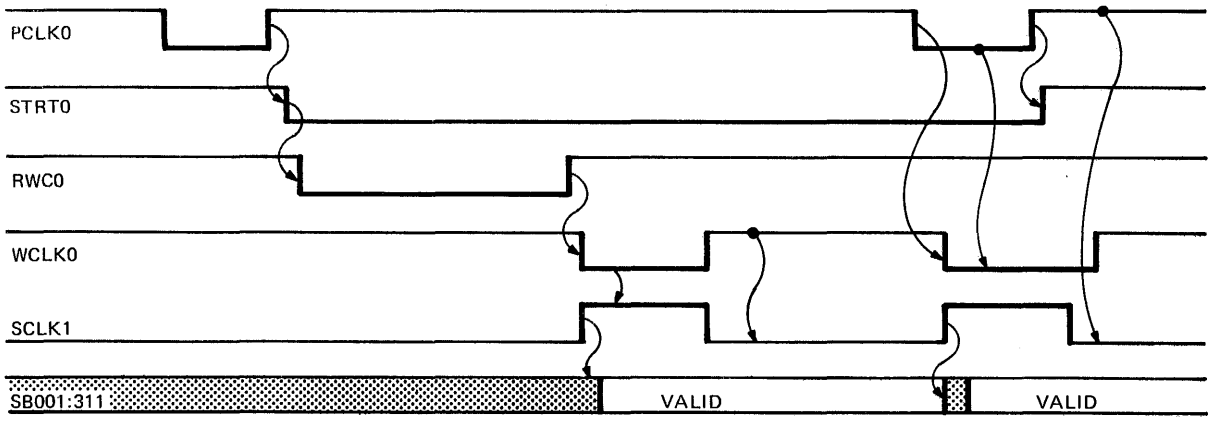


Figure 16B. SBUFF Timing, 64 Bit Write

The register sets are addressed by means of Select Bit ASEL001, the Module Select Bits MSEL000:020, and PSW Bits 25:27. When Module 1 is selected (MSEL000·MSEL010·MSEL021) ASEL001 inactive (low) selects GR, and ASEL001 active (high) selects MR.

One of the eight sets of GR is selected by decoding PSW25:27 in accordance with the coding shown on Figure 17. When MR is selected, the PSW bits are ignored.

REGISTER SET			ADDRESS INPUTS ASEL* 0 1 2 3 4	MOD	PSW 25 26 27	AAD* 0 1 2 3 4	PSW 5261A* 271A*	IC PIN 2 1 15 14 11 10 9 7
FIXED POINT GENERAL REGISTER	SET	0	0 X X X X	1	0 0 0	1 X X X X	0	0 0
		1			0 0 1			0 1
		2			0 1 0			1 0
		3			0 1 1			1 1
		4			1 0 0	0 X X X X	0	0 0
		5			1 0 1			0 1
		6			1 1 0			1 0
		7			1 1 1			1 1
MICRO PROGRAMMING REGISTERS (MR0:7)			1 X X X X	X D D D		0 X X X X	1	0 0

X = "1" or "0"
D = Don't Care

. Use: BSEL, BAD, PSW261B, and PSW271B

Figure 17. Stack Addressing Scheme

The address inputs to the memory elements are developed on Sheet 4 in accordance with Figure 17. When WSEL0 is active and WSEL1 inactive, the following logical relations are obtained:

AAD001 = ASEL001 + M37X1·PSW251
AAD010:040 = ASEL010:040
AAD050 = M37X0·ASEL000
PSW261A = M7X1 + PSW261·ASEL000·M37X0
PSW271A = PSW271·ASEL000·M37X0

The enable input ASTKN0 to ASTK is developed on Sheet 4 as follows:

ASTKN0 = ASEL001·ASEL011

64-Bit Read from ASTK. When pairs of registers are to be read for Double-Precision instructions (Fixed-Point divide) the addressed register location is always odd. When the first 32-bit word is read, RWC0 is active (low) causing DWC0 (4G5) to be low, forcing AAD040 high, and converting the address to the next lower even register. RWC0 is then made inactive and the second 32-bit word is read from the addressed odd location. The 64-bit read is only implemented for ASTK. BSTK does not respond to RWC0.

6.3.2 Write Addressing. ASTK is addressed for writing from SBUFF with SSEL001:041, MSEL000:020, PSW251, PSW261, and PSW271.

Selection at the register set for writing is similar to selection for reading, except that SSEL001:041 are used in place of ASEL001:041, and S37X1 and S7X1 are used in place of M37X1 and M7X1. S37X1 is latched up with M37X1 on the leading edge of CS001·CLK1, and S7X1 is similarly latched up with M7X1.

For 32-bit Write operations, when WSEL1 is active and WSEL0 is inactive, the address inputs to the memory elements are developed on Sheet 4 in accordance with the following logical relations:

AAD001	= SSEL001 + S37X1·PSW251
AAD010:040	= SSEL010:040
AAD050	= S37X0·SSEL000
PSW261A	= S7X1 + PSW261·SSEL000·S37X0
PSW271A	= PSW271·SSEL000·S37X0

The enable input ASTKN0 to ASTK is developed on Sheet 4 as follows:

ASTKN0 = SSEL001·SSEL011

Write addressing of BSTK is similar to ASTK, with the substitution of B for A.

64-bit write into ASTK (Sheet 5). When pairs of registers are to be written into for Double-Precision instructions (Fixed-Point Multiply and Divide) the addressed register is always even. During the read part of the read/write sequence, RWC0 is active (low), and if STRT0 is also active, the flip-flop at 5D3 is set. This enables the present inputs to the WSEL flip-flops (5D3), and when RWC0 becomes inactive, these flip-flops are set and WSEL1A is made active. Through the mechanism described in Section 4, a WCLK0 is generated which sets the flip-flop in 5E1 and resets the flip-flop in 5D3.

The preset signal which sets WSEL1 from RWC0 becoming inactive, is ORd with PCLK0 at 5C5, and produces SCLK1, to load SBUFF from the S Bus with the first 32-bit word of the 64-bit result.

When the flip-flop in 5E1 is set by the trailing edge of the first WCLK0, S0DD041 is made active although SSEL042 is inactive because of an even register selection. The next time PCLK0 becomes active, a second WCLK0 is generated. The second 32-bit word is then loaded into the register location which is one higher than the addressed location. At the trailing edge of the second WCLK0, the latter flip-flop is reset.

Figure 16B shows the timing for the 64-bit Read/Write operation.

6.4 Read/Write Control. (refer to Functional Schematic 35-555, Sheet 5.)

ASTK and BSTK are normally in the Read mode, since WSEL1 and WSEL1A are inactive, and WSEL0 and WSEL0A are active. Referring to Section 6.3, this causes ASTK to drive the A Bus and BSTK to drive the B Bus from register locations determined by the address select lines ASEL, BSEL; the PSW Bits 25, 26, and 27; and MSEL00:02.

If the CPU micro-program requires writing data into the register stacks, STRT0 becomes active and either SSEL001 (for MR selection) or SSEL011 (for GR or FR selection) but not both, becomes active. SSELX0 remains inactive (high) and the J inputs to the WSEL flip-flops at 5G3 are enabled. At the leading edge of the following system clock (PCLK0) from CPB, the flip-flops are set, causing WSEL0 and WSEL0A to become low and WSEL1 and WSEL1A to become high. (This changes the stack addressing inputs to the SSEL Bus.) The high state of WSEL1 is propagated down a 100 nanosecond delay line at 5E5, and after the first 10 nanoseconds, WCLK0 and WCLK0A are made active for 50 nanoseconds. At the end of WCLK0, the WSEL flip-flops are reset through the direct clear input, terminating the Write operation and returning ASTK and BSTK to the Read mode.

The 64-bit Read and Write operations are modification to the basic read/write cycle, and have been described previously.

7. ALU (refer to Functional Schematic 35-538D08)

The ALU is a standard module of the Model 8/32 System which implements fixed point arithmetic/logical functions. The ALU communicates with the CPU over the A, B, S, and C Busses with all communications being completely asynchronous. The ALU becomes active when it recognizes its address on the Control Bus. The ALU is addressed as Module Number 1. The CPU signals a Start (STRT) and the ALU performs the function as determined from the Control Bus (FSEL). Refer to Table 15. ALU functions may be of two types. The simple functions (fixed point Add, Subtract, and logicals) causes the ALU to immediately return a finish signal (MFIN) as these functions are completed within 130 nanoseconds. For these instructions (refer to Figure 18), the A and B Buses are gated to the ALU chips where the function is performed and the result is gated to the S Bus. The ALU does not generate a clock for any of these functions and all gating is performed asynchronously.

For the complex functions (Multiply, Divide, and Shifts) the ALU clock is enabled and the hardware implementation of these instructions is sequential. For these instructions the Multiplier/Quotient (MQ) shift register, the A Latch (AL) register, and the three shift multiplexors are enabled to perform the iterative operation determined by the instruction. The shift multiplexors are used to shift A or S right or left into the A latch as outlined in the ALU algorithms. For these functions, the ALU does not return MFIN until the operation is completed and the result is on the S Bus.

TABLE 15. ALU FUNCTION CODES

FSEL(HEX)	OPERATION MSEL=X'1'
0	SUBTRACT
1	ADD
2	SUBTRACT WITH CARRY
3	ADD WITH CARRY
4	UNUSED
5	LOGICAL AND
6	EXCLUSIVE OR
7	LOGICAL OR
8	*LOGICAL SHIFT RIGHT
9	*LOGICAL SHIFT LEFT
A	ROTATE RIGHT
B	ROTATE LEFT
C	*ARITHMETIC SHIFT RIGHT
D	*ARITHMETIC SHIFT LEFT
E	MULTIPLY
F	DIVIDE

*KSIG is an extension of the FSEL field and is used to signal halfword shifts.
KSIG is only valid for shift instructions and should not be set for any other instruction type.

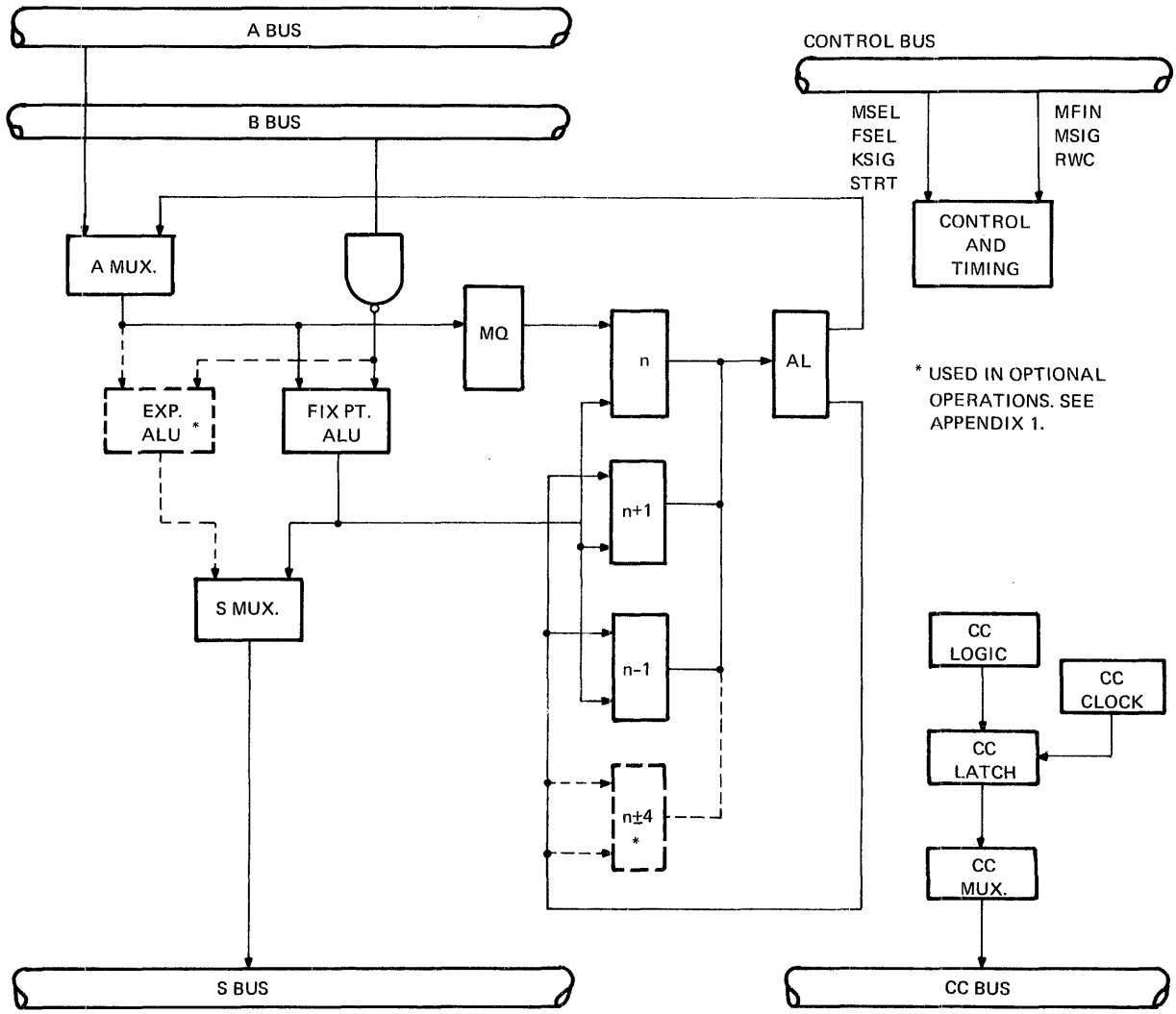


Figure 18. ALU Functional Block Diagram

7.1 Arithmetic State Register (AS) (Sheet 5).

For Module 1 operations the ALU can be in one of four arithmetic states as designated by the conditions of the State Registers ASA, ASB, and ASC.

AS001 = ASA0•ASB0•ASC0,
AS011 = ASA1•ASB0•ASC0,
AS021 = ASA0•ASB1•ASC0,
AS031 = ASA1•ASB1•ASC0,

The State Register is direct cleared by STRT1, therefore AS001 is the quiescent state of the ALU. Furthermore, the ALU remains in AS001 for the simple functions (FSEL000) previously described and only makes state transitions for the complex functions (FSEL001) when a clock is generated. The various transitions which are possible are described in the ALU Algorithms section. The State Register is implemented in J-K type logic which is tempered with a clock (activated only for FSEL001). The transition diagram is shown in Figure 19 and the logic determining each transition is listed in Table 16.

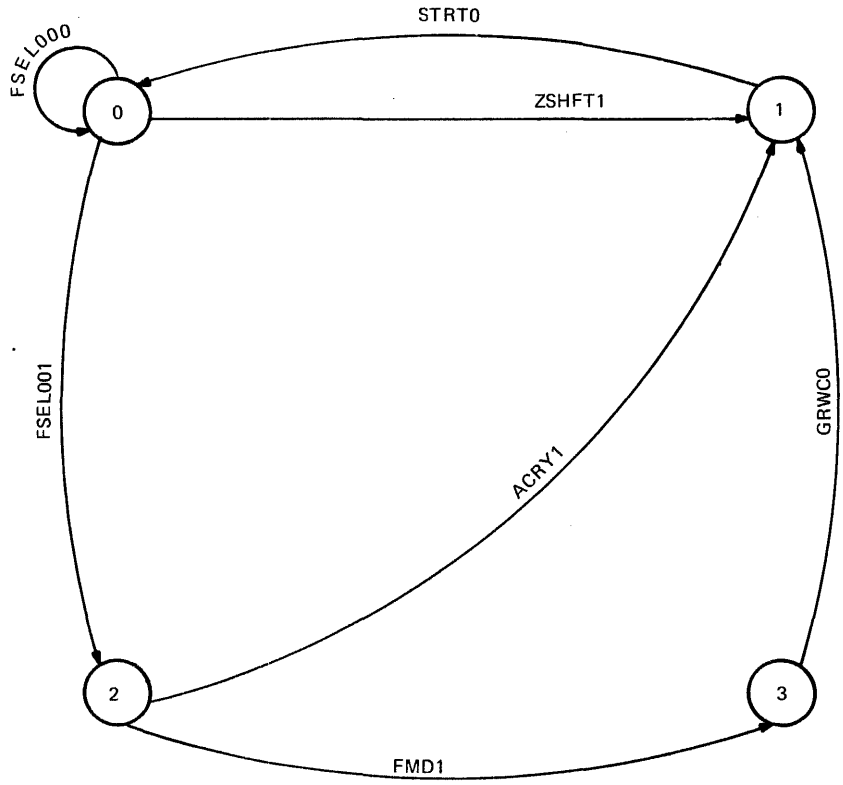


Figure 19. ALU State Transitions

7.2 ALU Flow Charts and Algorithms

1. Simple Functions (FSEL000)

These arithmetic/logical functions do not require that the ALU clock be generated; they employ combinational logic to perform the required function. When one of these functions is to be performed, ALSTRT1 is used to gate MFIN0 back to the CPU, relying on the basic CPU clock frequency to allow the operation to be performed by the basic arithmetic/logical elements and the result to appear on the S Bus before being strobed into the destination register. Shown in Figure 20 is a timing diagram for the immediate response functions with respect to the CPU clock. Note that STRT0 is precisely the width of one CPU clock cycle or approximately 130 nanoseconds. Upon receipt of STRT0, the ALU immediately ($\approx$ 15 nanoseconds) returns MFIN0 to prevent inhibiting the CPU clock. As the CPU latches the S Bus on the leading edge of the active clock, it is necessary for the ALU to complete its function and present the results to the S Bus within 70 nanoseconds. On the trailing edge of the active clock, the CPU switches control states and releases STRT0. It is during this next control state that the CPU writes the result into the destination register.

TABLE 16. STATE REGISTER LOGIC

TRANSITION	ASA LOGIC	ASB LOGIC	ASC LOGIC	COMMENT
AS001 TO AS011	J = ZSHFT1			ABORT SHIFT IF SHIFT COUNT IS ZERO.
AS001 TO AS021		J = EAS0·AS001		UNCONDITIONAL TRANSFER IF NOT FLT. PT. ADD/SUB.
AS021 TO AS011	J = ACRY1	K = ACRY1	J = ACRY1	SHIFT COMPLETE
AS021 TO AS031	J = ACRY1	K = FMD0		FIX PT. MULT./DIV. COMPLETE.
AS031 TO AS011		K = GRWC0·AS031		FIX MULT/DIVIDE–FIRST HALF OF RESULT WRITTEN INTO DESTINATION REGISTER.
AS011 TO AS001	RESET = STRT1	RESET = STRT1	RESET = STRT1	RESET TO AS001 WHEN CPU REMOVES STRT1.

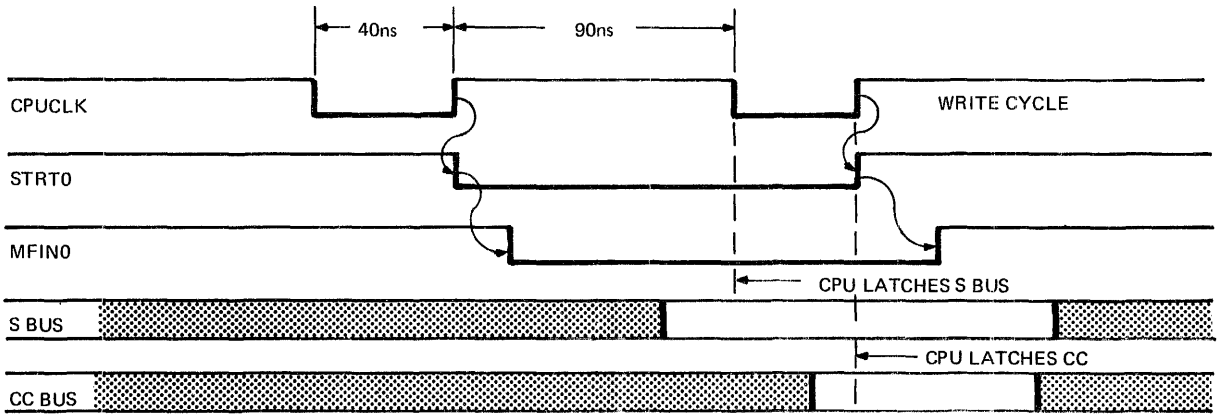


Figure 20. ALU Bus Timing – Immediate Response Functions (FSEL000)

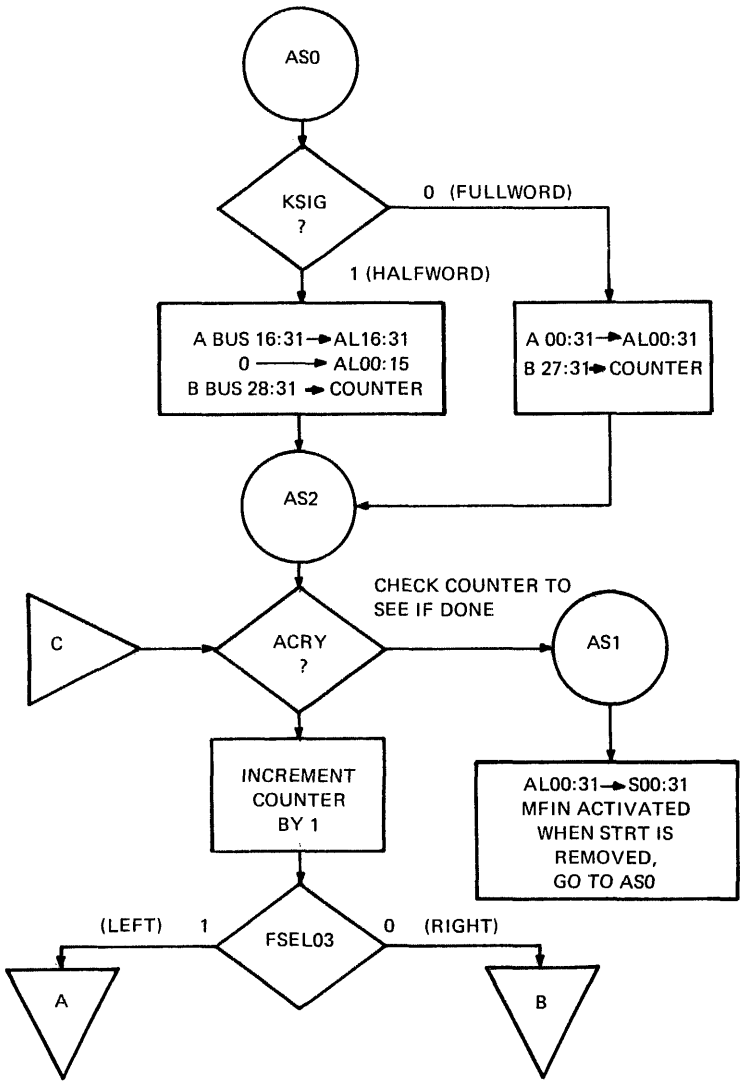
The fixed point simple functions are Subtract, Add, Subtract With Carry (SWC), Add With Carry (AWC), logical AND, logical Exclusive OR, and logical OR. When the instruction to be performed is an Add/Subtract, the carry state into the arithmetic element must be generated. This is done by the gate (9B8) whose output is labeled CIN310. Since the 19-067 device performs a subtraction by internal 1's complement addition, a carry must be generated for Subtract. Similarly, a carry in is generated for Add With Carry (A+B+1) and suppressed for Subtract With Carry (A-B-1).

2. Complex Functions (FSEL001)

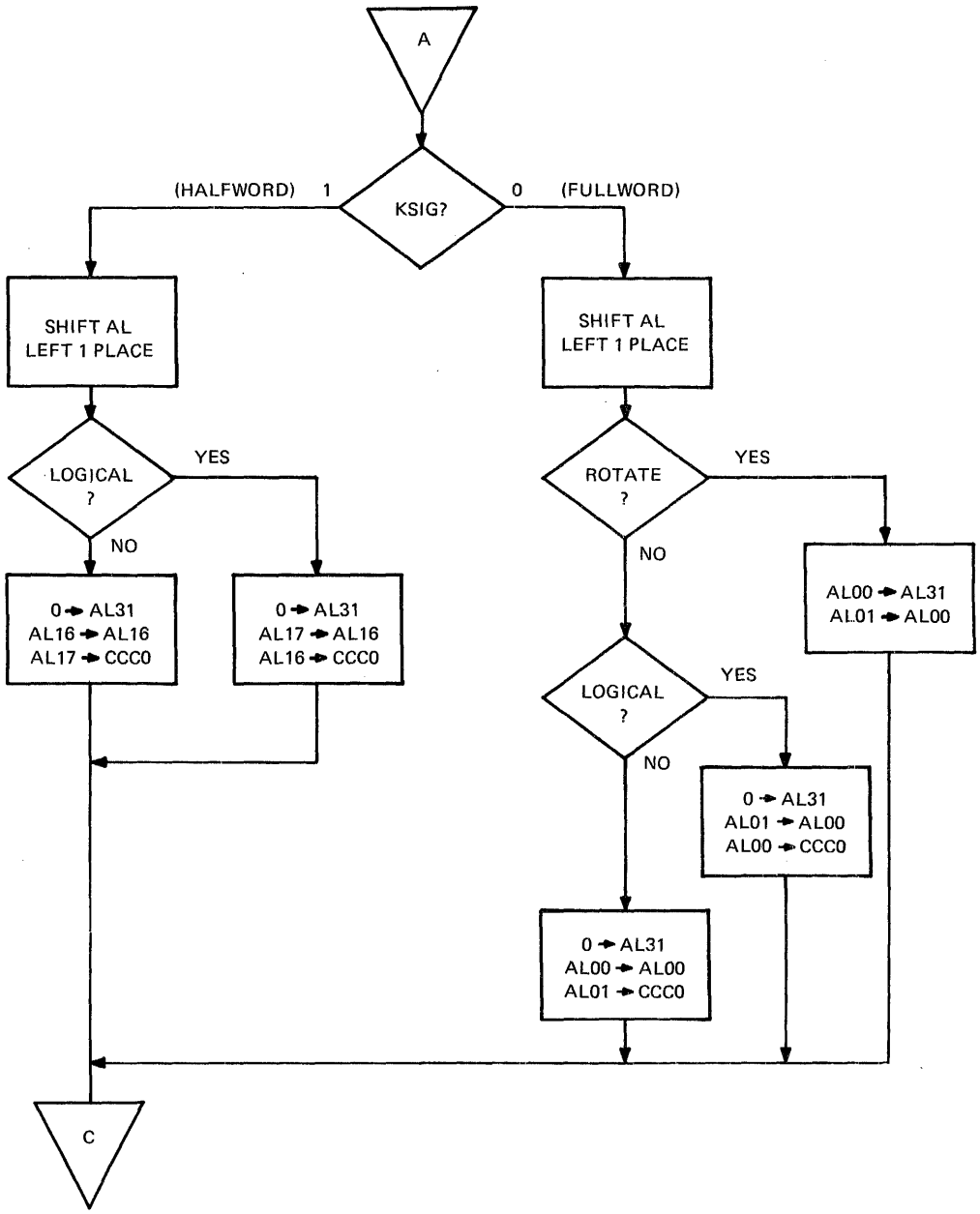
Shift Instructions

The ALU can perform both halfword (16-bits) and fullword (32-bit) shifts. When a shift is to be performed, the word to be shifted is taken from the A Bus and the shift count is taken from the B Bus (B27:31). In AS001, the A Bus is transferred to the AL register. If a halfword shift is to be performed, KSIG1 is set, and the most significant 16-bits of the AL register are inhibited by killing the clock to those devices. The shift occurs in AS021, AL being continuously loaded from the proper shift multiplexor. When the correct number of shifts have occurred, ACRY1 forces the transition to AS011. During AS011, the contents of the AL register are transferred to the S Bus, the flags are generated onto the CC Bus, and MFIN is returned to CPU. Following are Shift Functions Flow Charts and Shift Function algorithms. The flow charts and algorithms are complementary and may be used together or individually, whichever is more convenient.

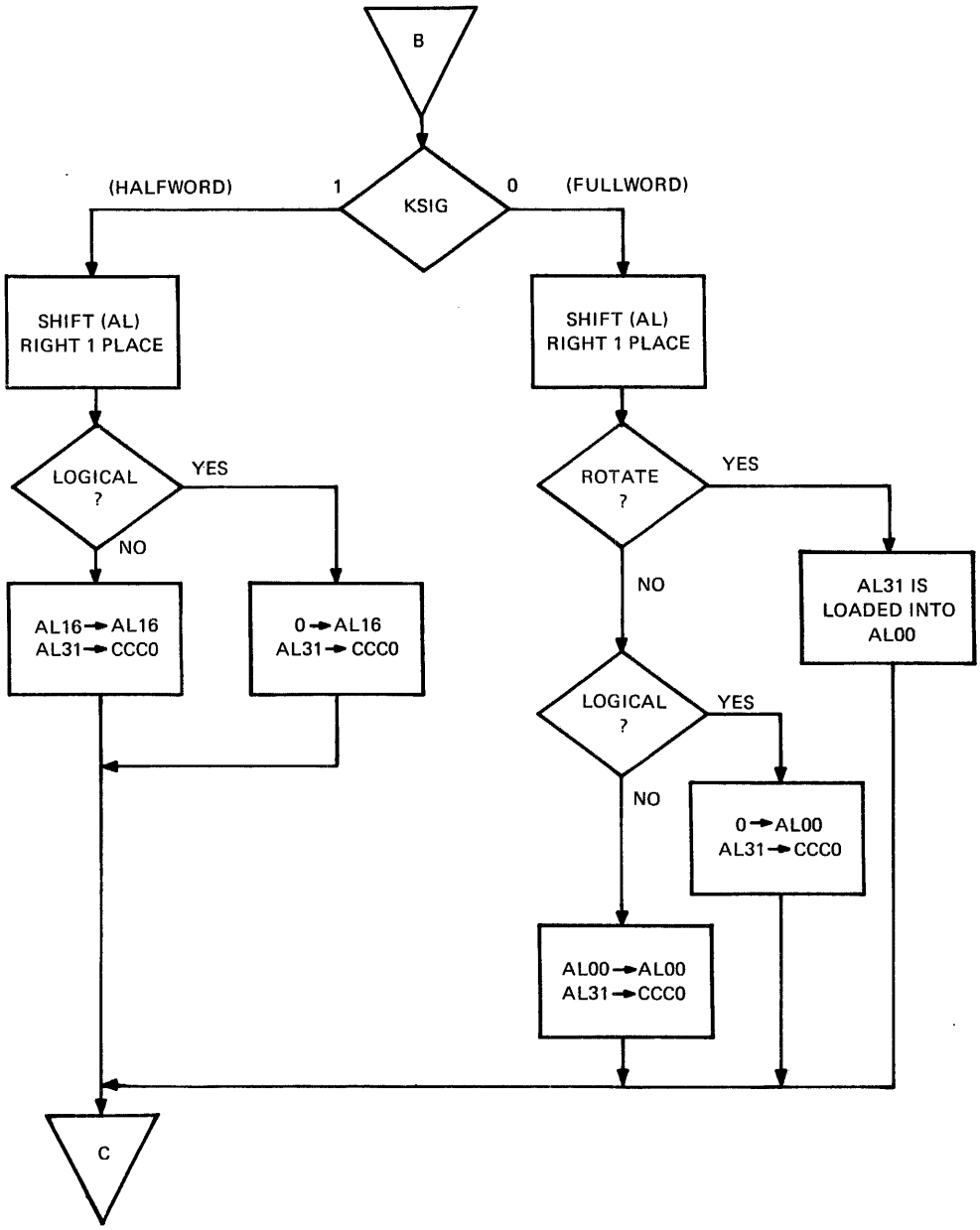
SHIFT FUNCTIONS FLOW CHART (SECTION 1 OF 3)



SHIFT FUNCTIONS FLOW CHART: SHIFT LEFT (SECTION 2 OF 3)



SHIFT FUNCTIONS FLOW CHART: SHIFT RIGHT (SECTION 3 OF 3)



The Shift Algorithms are:

AS001 if KSIG0, A00:31→AL00:31
if KSIG1, A16:31→AL16:31, 0→AL00:15
B27:31→ACNT01:05
AS001→AS021

AS021 if ACRY1, AS021→AS011
ACNTΣ1→ACNT

if FSEL030
- if KSIG0
  - AL00:30→AL01:31
  - if ROTATE, AL31→AL00
  - if LOGICAL, 0→AL00
  - if ARITH., AL00→AL00
- if KSIG1
  - AL16:30→AL17:31
  - if LOGICAL, 0→AL16
  - if ARITH., AL16→AL16

if FSEL031
- if KSIG0
  - AL02:31→AL01:30
  - if ROTATE
    - AL00→AL31
    - AL01→AL00
  - if LOGICAL
    - 0→AL31
    - AL01→AL00
  - if ARITH
    - 0→AL31
    - AL00→AL00
- if KSIG1
  - AL18:31→AL17:30
  - if LOGICAL
    - 0→AL31
    - AL17→AL16
  - if ARITH.
    - 0→AL31
    - AL16→AL16

AS011 AL00:31→S00:31
MFIN→1

Fixed Point Multiply

The ALU performs signed multiplication on two 32-bit operands. The multiplicand is transferred from the A Bus to the MQ register during AS001 and the multiplier remains on the B Bus throughout the operation.

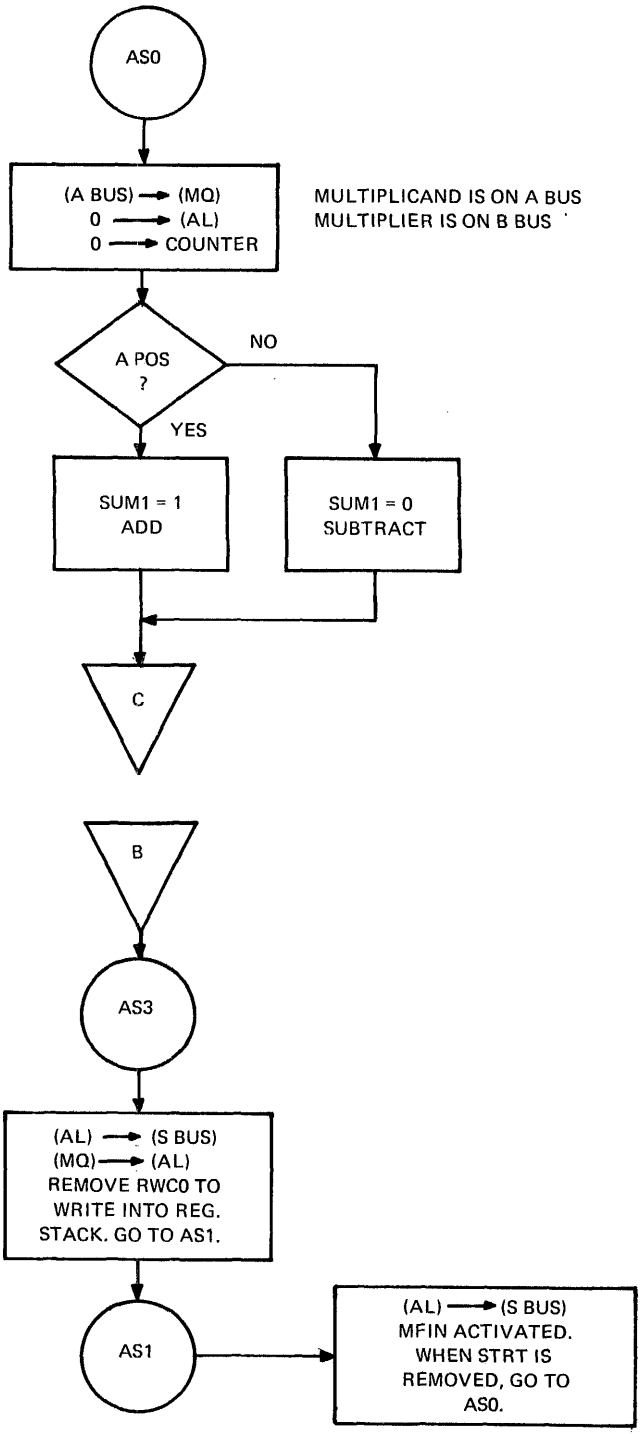
If the multiplicand is positive, a product is formed by adding the multiplier to the shifted product conditional upon the multiplier. If the multiplicand is negative, the product is formed by subtracting the multiplier from the shifted partial product conditional upon the 2's complement of the multiplicand.

Multiplication is accomplished by examining each successive bit of the multiplicand as it is shifted out of the MQ register. A 32-bit product is formed by shifting either AL (the partial product) or S (=ALΣB) back into AL and into the MQ conditional upon M1, the multiplicand bit. The logic gate for M1 is located at 7N6. If SUM1 is set (multiplier positive), M1 is simply MQ311. If SUM0 is set (multiplicand negative) M1 becomes the 2's complement of the multiplicand. The 2's complement fo the multiplicand is taken by detecting the first MQ bit which is set and thereafter complementing the remaining MQ bits. This is accomplished by the complement flip-flop (7J7) and the M1 logic gate.

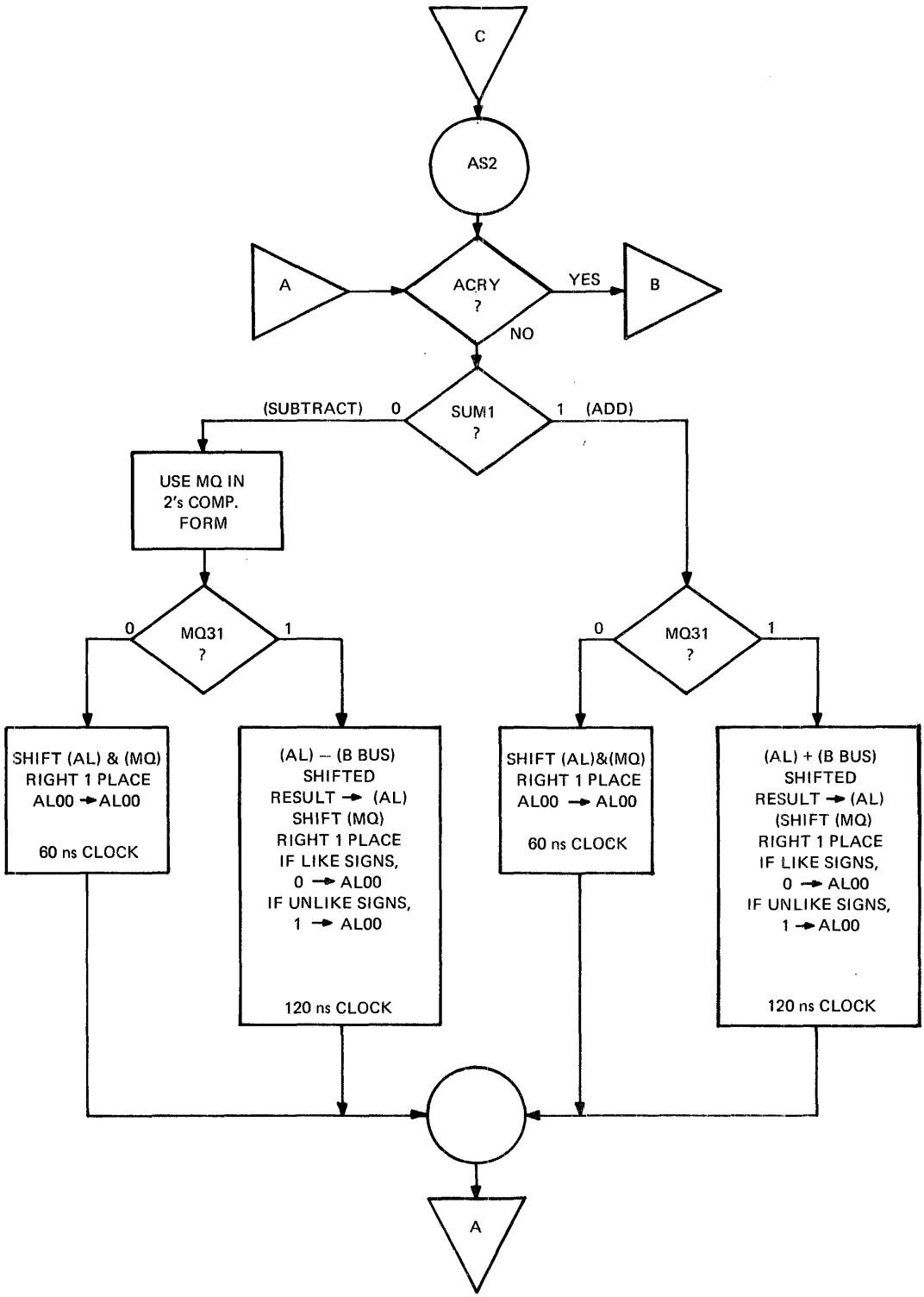
Inherent in the Multiply algorithm is a look ahead feature which permits deciding in advance whether to add and shift, or just shift the partial product. If M1 is set, AL is added to B and the sum is shifted into the AL and MQ registers. If M1 is reset, the AL is shifted back into the AL and MQ registers. Since more time is required to perform both an add and shift (M1) the ALU clock is divided by two when M1 is set and permitted to run at its basic speed when not set (see Section 7.3 ALU Clock).

When the Multiply is completed, the most significant portion of the result is written into the destination register in AS031 and MQ is transferred to the AL. In AS011, the least significant portion is written into the destination register.

FIXED POINT MULTIPLY FLOW CHART (SECTION 1 OF 2)



FIXED POINT MULTIPLY FLOW CHART (SECTION 2 OF 2)



The algorithm for Multiply is:

```
AS001   A00:31→MQ00:31
        0→AL00:31
        0→ACNT01:05
        if A000, 1→SUM1
        if A001, 0→SUM0
        AS001 →AS021
AS021   if ACRY1, AS021→AS031
        GRWC→0
        ACNT Σ1→ACNT
        if SUM1, ALΣB
        if SUM0, ALΔB
        if M1 { S00:S30→AL01:31
                (A00⊕B00)·ZSUM0→AL00
                MQ00:30→MQ01:31
                S31→MQ00
        if M0 { AL00:30→AL01:31
                AL00→AL00
                MQ00:30→MQ01:31
                AL31→MQ00
AS031   AL00:31→S00:31
        MQ00:31→AL00:31
        if GRWC0, AS031 →AS011
AS011   AL00:31→S00:31
        MFIN→1
```

Fixed Point Divide

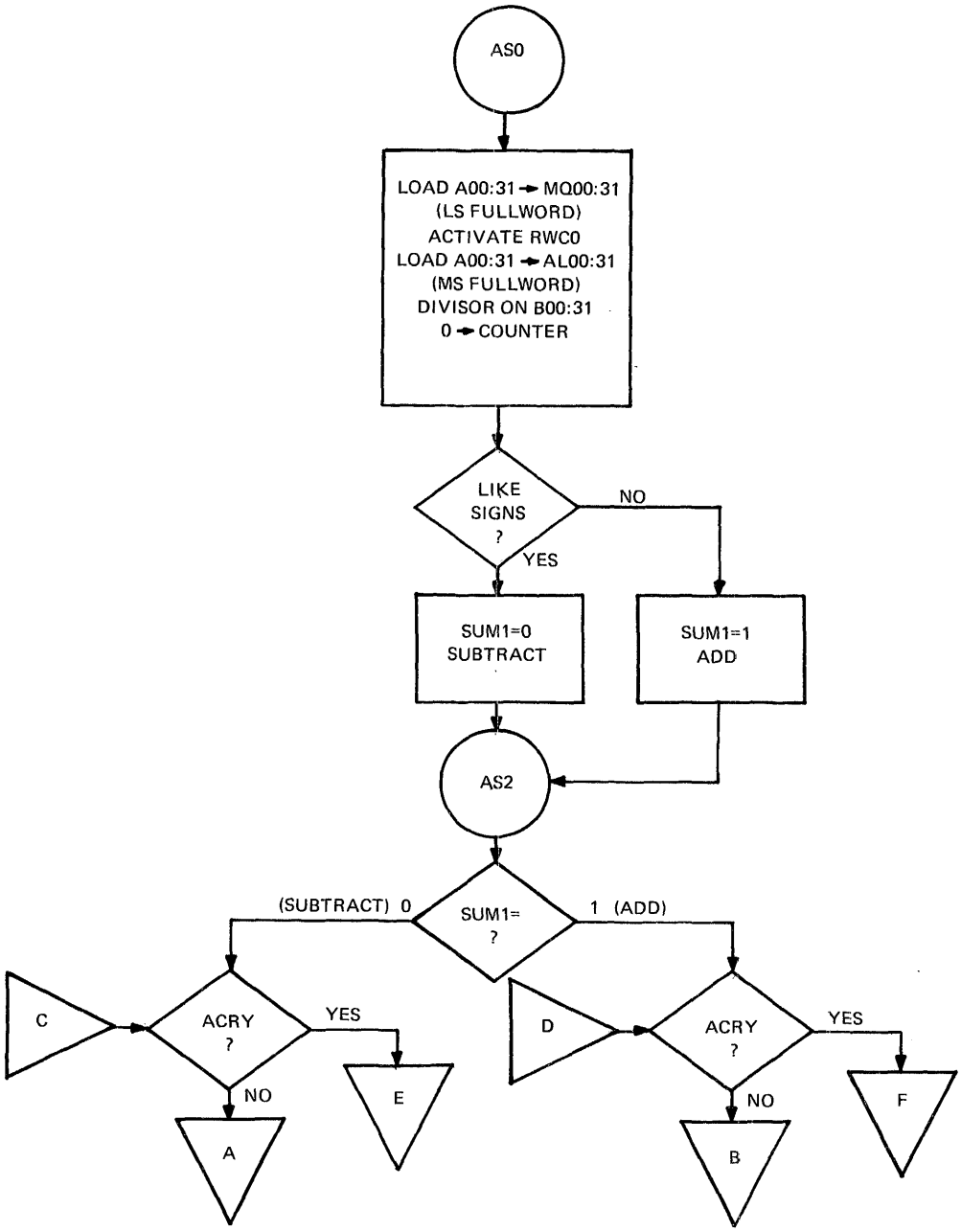
The Fixed Point Divide algorithm is implemented by subtracting the divisor from the shifted dividend to determine if it is greater or not. If the dividend is determined to be smaller than the divisor, the quotient digit for that test is made to be a zero, and the dividend is shifted left again to repeat the process. If the dividend is determined to be larger, the quotient digit for that test is made to be a one and the difference, shifted left, is stored as the new dividend. In the implementation of signed divide, if the two operands are of unlike signs, the subtraction is performed by the addition of the unlike operands and the 1's complement of the quotient is accumulated. When the complemented quotient is formed, it is corrected to the 2's complement in AS011.

An obstacle in performing signed division using complementary arithmetic arises when the intermediate dividend is a negative number and both the intermediate quantities (the absolute value of the dividend - divisor) and the remainder equal zero because the logic does not detect the quotient digit of 'one'. When this case arises, the computed result = true quotient −1, with the remainder equal to the divisor. To detect this case, a flip-flop (RZR0) (7F1) monitors this condition and causes a correction cycle in AS011.

Because of the difference in scaling of the divisor (2^{63}) and the dividend (2^{31}) and the fact that both the quotient and remainder must be scaled (2^{31}), an extra division cycle is performed in AS031 to compute Q31. To properly scale the remainder, the last summation is inhibited from shifting. Moreover, if the absolute value of the Q31 digit is '1', the correct remainder is on the S Bus during the first cycle of AS031 and remains there throughout AS031. Should the absolute value of the Q31 digit be '0', the correct remainder is in the AL register, and ALU control is modified to force the transfer of AL to the S Bus.

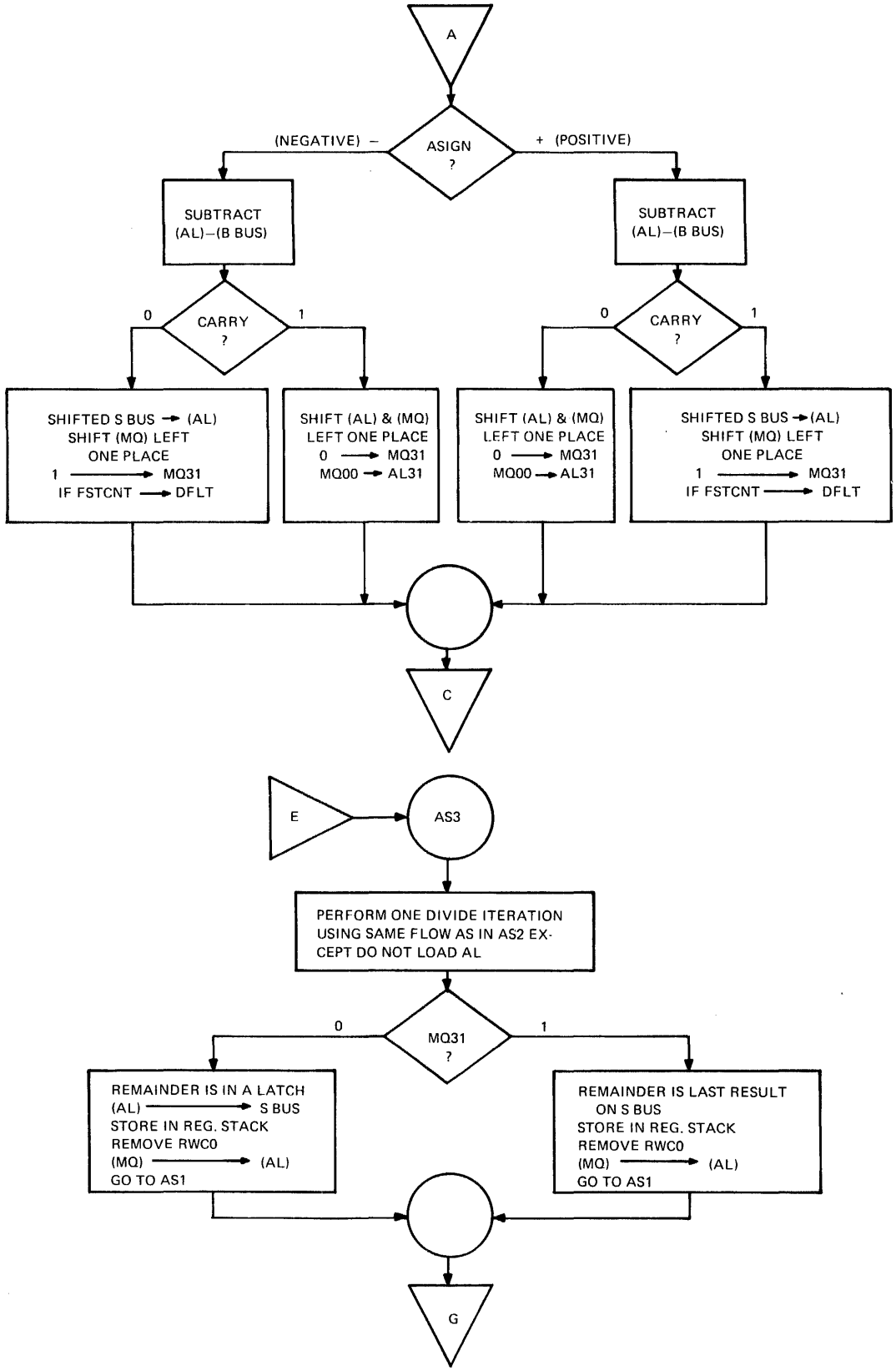
The least significant portion (remainder) of the result is written into the destination register in AS031, and the most significant portion (quotient) is written into its destination register in AS011.

FIXED POINT DIVIDE FLOW CHART (SECTION 1 OF 4)



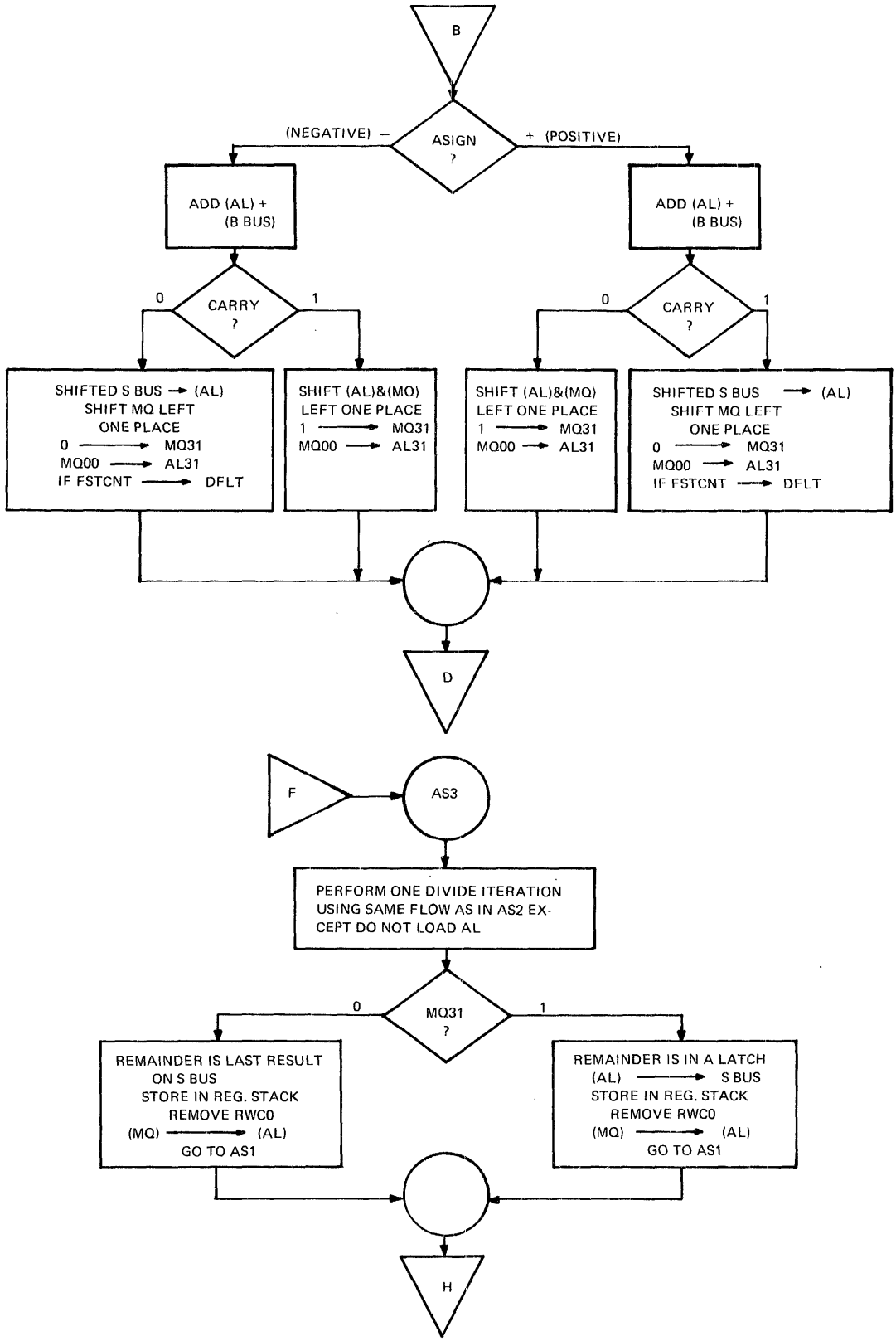
FIXED POINT DIVIDE FLOW CHART: LIKE SIGNS (SECTION 2 OF 4)

536

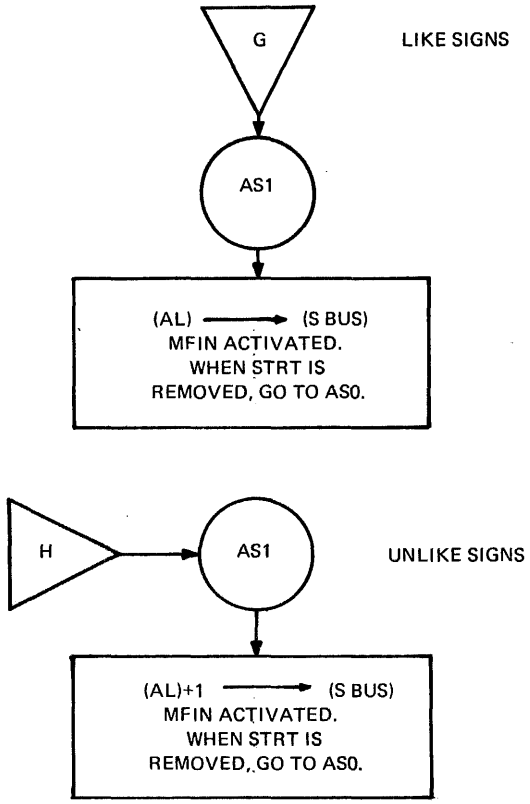


FIXED POINT DIVIDE FLOW CHART: UNLIKE SIGNS (SECTION 3 OF 4)

537



FIXED POINT DIVIDE FLOW CHART (SECTION 4 OF 4)



The algorithm for Fixed Point Divide is:

AS001 A00:31→MQ00:31
GRWC→0
if A00 $\bar{\oplus}$ B00, SUM0→1
if A00 $\oplus$ B00, SUM1→1
0→ACNT01:05
0→RZR01
A00:31→AL00:31
AS001→AS021

AS021 if (FSTCNT1 and |Q|=1), DFLT→1
if ACRY1, AS021→AS031
ACNT Σ1→ACNT
if SUM0, (ALΔB)
if SUM1, (ALΣB)

if COUT000 $\bar{\oplus}$ BG001 {
1→MQ31
MQ01:31→MQ00:30
MQ00→AL31
AL01:31→AL00:30

if COUT000 $\oplus$ BG001 {
0→MQ31
MQ01:31→MQ00:30
MQ00→AL31
S01:31→AL00:30

AS031

if SUM0, AL Δ B

if SUM1, AL Σ B

if COUT000 $\overline{\oplus}$ BG001 { 1→MQ31 ; MQ01:31→MQ00:30

if COUT000 $\oplus$ BG001 { 0→MQ31 ; MQ01:31→MQ00:30

if (MQ31 $\oplus$ AXB1)·SUM0, (ALΔB)→S00:31

if (MQ31 $\oplus$ AXB1)·SUM1, (ALΣB)→S00:31

if MQ31 $\overline{\oplus}$ AXB1, AL00:31→S00:31

MQ00:31→AL00:31

if GRWC0, AS031→AS011

AS011

AL00:31→S00:31

MFIN→1

7.3 ALU Clock (Sheet 6)

The ALU clock is a gated oscillator whose basic frequency is determined by a tapped delay line. The basic clock period is factory adjusted for 60 nanoseconds. The clock is enabled for all complex operations (FSEL001). It may be inhibited for test purposes by removing the ground strap from Connector 7. With the ground strap removed, the ALU may be single stepped through an instruction using the push button switch located at 16R. The enable logic at gate 13A06 is true when the conditions ALSTRT1·FSEL001·AS010 are met. This results in a clock output at MQCLK0, ACLK1, ACLK0, ALCLKA0, and ALCLKB0. The clock is inhibited during AS011 and the ALU becomes static until the CPU removes STRT.

For shifts, the basic 60 nanosecond clock provides the ALU with enough time to perform the required operations. However, for Multiply/Divide and other special cases, 60 nanoseconds is insufficient time to perform the required operation. For example, when dividing, both a subtraction and a shift must be performed in each iterative cycle. For these cases, the ALU clock period is doubled. The disable logic at gate 13B08 determines if the 120 nanosecond clock is to be generated. The cases when this is true are as follows:

1. Always when dividing.

2. In CAE on the first count of AS021 to permit the transfer of either operand (A or B) through the ALU chips to the AL. (see CAE algorithm).

3. When multiplying if the M1 bit is set. If M1 is set, both an add and shift are performed. If M1 is reset, only a shift need be performed.

7.4 Arithmetic Iterative Counter (ACNT01:05) (Sheet 4)

The iterative shifting of the ALU is controlled by a modulo 32 counter which is enabled during AS021. It is in AS021 that the iterative operations of shift and Multiply/Divide occur and this counter is used to determine completion of the operation and, therefore, the time at which transition to the next arithmetic state should occur. For fixed point operations the counter is used in two different modes as described below.

1. Shifts.

For these operations, the counter is loaded with the 1's complement of the shift count which is taken from the B Bus and loaded at the transition from AS001 to AS021. The most significant bit is inhibited for halfword shifts if KSIG is set. The transition from AS021 is enabled when the counter reaches a count of 30, as determined by the logic signal ACRY1 (gate 09D06). Should a shift count of zero occur, this is detected in the Arithmetic State Register and the operation is aborted by inhibiting the transition to AS021.

2. Fixed Point Multiply/Divide

For these two instructions, the counter is initialized to a count of zero and is enabled to count during AS021. When the counter reaches a count of 31_{10}, the transition from AS021 to AS031 is enabled by ACRY1.

7.5 Arithmetic Condition Code (Sheets 2 and 3)

The ALU gates appropriate Condition Code flags to the CPU for all ALU functions. When the ALU senses its address and receives a start (STRT) it signals the CPU with SCC0 that a new Condition Code is available. Figure 18 (ALU Functional Block Diagram) shows that the ALU Condition Code circuits consist of combinational logic which determines the resultant condition of each instruction. These are latched in a register. The clock which latches the Condition Code is gated in one of two ways. For the simple functions (FSEL000), the clock results from STRT, delayed an appropriate amount of time to allow the ALU to complete its function. For complex functions (FSEL001), the clock is generated in AS011 at the conclusion of an instruction. The Condition Code is then gated onto the bus through a tri-state multiplexor. The representation of each flag is as follows.

1. VCC0 (Arithmetic Overflow).

The logic for this flag is shown on Sheet 3 (SVCC0). It is enabled for fixed point Add, Subtract, and Divide. The flag is active for fixed-point Add/Subtract instructions when an overflow is determined by the logic:

$$ASIGN0 \cdot S001 \cdot (BG001 + SUM1) \oplus ASIGN1 \cdot S000 \cdot (BG001 \,\overline{\oplus}\, SUM1).$$

The V flag is active for fixed point Divide on the first iteration of the Divide if the quotient bit is determined to be a one. This condition is called a Divide Fault (DFLT) and indicates that the result cannot be contained in 31 bits plus sign. The V flag also sets for fixed point Divide at the end of the divide algorithm if the calculated sign of the quotient is incorrect.

2. CCC0 (Carry).

The logic for this flag is shown on Sheet 2. It is enabled for fixed point Add/Subtract, Shifts, and Divide. For fixed point Add/Subtract the logic is SUM1 COUT00+SUM0 COUT000 respectively. The C flag is also active for fixed point Divide to signal a divide fault. For Shift type instructions, the C flag is the state of the last bit to be shifted. This is selected by the eight to one (8/1) multiplexor whose select control lines are encoded to yield the proper bit for every type shift. The selected bit is then latched by the flip-flop shown at 2E2.

It should also be noted that the Module Signal (MSIG0) from the ALU is identical to CCC0.

3. LCC (Less Than Zero)

The L flag represents the sign of any arithmetic operation. For fullword fixed point operations it is the sign of the result and for halfword shifts it is the sign of Bit 16 (S161).

4. GCC0 (Greater Than Zero)

This flag logically represents the occurrence of not less than zero and results not equal to zero. This can be logically represented as follows:

$$GCC0 = LCC0.ZSUM0$$

7.6 Arithmetic Elements and ROM Control (Sheets 9:17)

The heart of the ALU is built from the four bit arithmetic/logical elements (Perkin-Elmer Part Number 19-067) and a format ROM used to control them. Also used in conjunction with the ALU chips are a two level carry-look ahead scheme (Perkin-Elmer Part Number 19-068).

As previously stated, the ALU is essentially controlled by a 256X4 bit ROM. FSEL001:031 and MSEL011 address the ROM and determine the required control for the given instruction. ASIGN1, BSIGN1, and FAXB1 provide needed additional information to insure correct control for fixed point Multiply/Divide. Shown in Table 17 is a listing of ALU control and the respective operations as a function of the address bits. One additional control bit (ALOG1) is required to correctly specify logical operations from arithmetic operations. The logic for this gate (12L2) is:

MSEL010•FSEL000•FSEL011

and essentially decodes the logical operations as per the FSEL field.

There is a level of gating beyond the ROM outputs on AM0D00:03. This is to provide a basic overide function. The function provided is to transfer A to S. This is accomplished by XFR0 (12M5). The cases for which this is necessary are as follows.

1. In AS001 for shifts and Multiply/Divide to transfer operand from the A Bus to the A latch.
2. In AS011 to transfer contents of A latch to the S Bus.
3. In AS031 in fixed point multiply to transfer contents of A latch to the S Bus.
4. In AS031 of divide to transfer contents of A latch to S Bus under certain conditions (see divide algorithms).

7.7 MQ Register (Sheets 10:17)

The Multiplier Quotient Register is used exclusively in Multiply/Divide instructions. It is comprised of eight MSI four bit shift registers which are capable of shifting left or right.

Control for the MQ registers is located at 7N4. The A Bus is always loaded into MQ in AS001 by forcing both SR1 and SL1 high. This is accomplished by clearing the Control flip-flop (7K4) with STRT1. For multiply, SR1 is active to perform right shifts and SL1 is inactive. The opposite is true for divide when shifts left are performed.

TABLE 17. ALU ROM CONTROL

BSIGN1	ASIGN1	FSEL001	FSEL011	FSEL021	FSEL031	AMOD031	AMOD021	AMOD011	AMOD001	FUNCTION	COMMENTS
X	X	0	0	0	0	0	1	1	0	SUM0	SUBTRACT
X	X	0	0	0	1	1	0	0	1	SUM1	ADD
X	X	0	0	1	0	0	1	1	0	SUM0	SUB. WITH CARRY
X	X	0	0	1	1	1	0	0	1	SUM1	ADD WITH CARRY
X	X	0	1	0	1	1	1	0	1	A·B	LOGICAL AND
X	X	0	1	1	0	0	1	1	0	A⊕B	LOGICAL EX. OR
X	X	0	1	1	1	0	1	1	1	A + B	LOGICAL OR
X	X	1	0	0	0	0	0	0	0	A	LOG. SHIFT RIGHT
X	X	1	0	0	1	0	0	0	0	A	LOG. SHIFT LEFT
X	X	1	0	1	0	0	0	0	0	A	ROTATE RIGHT
X	X	1	0	1	1	0	0	0	0	A	ROTATE LEFT
X	X	1	1	0	0	0	0	0	0	A	ARITH. SHIFT RIGHT
X	X	1	1	0	1	0	0	0	0	A	ARITH. SHIFT LEFT
X	0	1	1	1	0	1	0	0	1	SUM1	MULT.: A POS.
X	1	1	1	1	0	0	1	1	0	SUM0	MULT.: A NEG.
0	0	1	1	1	1	0	1	1	0	SUM0	DIV.: SIGNS ALIKE
0	1	1	1	1	1	1	0	0	1	SUM1	DIV.: SIGNS DIFFER
1	0	1	1	1	1	1	0	0	1	SUM1	DIV.: SIGNS DIFFER
1	1	1	1	1	1	0	1	1	0	SUM0	DIV.: SIGNS ALIKE

NOTE: SUM1 = SUM, SUM0 = DIFFERENCE

7.8 AL Register and Shift Multiplexors (Sheets 10:17)

The AL registers are comprised of eight MSI quad D type flip-flops with double rail output. They are used in all complex functions (FSEL001) as a holding register for shift type operations.

Shifts are performed by enabling one of four multiplexors depending on the type of shift to be performed. The multiplexor outputs are OR - tied together and perform the following types of shifts.

1. n: has S001:311 and MQ001:311 as inputs. Does not shift; used for transferring MQ or A Bus to AL register.

2. n+1: has S011:311 and AL021:311 as inputs. Performs left one shifts for Shift instructions and Divide instructions. End points are determined by AGL001 and AGL311 (Sheet 8).

3. n-1: has S001:301 and AL001:301 as inputs. Performs right one shifts for Shift instructions and Multiply instructions. End points are determined by AGR001 and SGR001 (Sheet 8).

IOU

8. I/O GENERAL DESCRIPTION

The 8/32 Input/Output Unit (IOU) performs a multiplicity of functions. Its main function is to communicate, via the Multiplexor Channel, with up to 1,023 peripheral devices. It has an additional capability of performing byte manipulations for the CPU both in conjunction with and without an I/O exchange. In addition, the I/O module contains the Machine Control Register (MCR), the Display Controller, the Teletype Controller, the Power Monitor and System Initialize circuit, and the Start Timer. Module Number 2 is assigned to the IOU module.

9. FUNCTIONAL DESCRIPTION

9.1 I/O Control Functions

IOU communicates with both the CPU (via the A, B, S, and CPU Control Busses) and peripheral controllers (via the Multiplexor Bus) using request/response signaling. Timing is completely asynchronous (rather than quantized) to achieve maximum speeds.

IOU becomes active when it recognizes its address (Module Number 2) on the Memory Select (MSEL) lines from CPU and STRT0 goes active. The function decode logic then directs the control and gating logic to perform a required function, encoded on Function Select lines (FSEL00:03) and KSIG. (Function Code Extension line). At the completion of the operation, a MFIN signal is sent back to the CPU.

IOU control is capable of performing 32 functions shown in Table 18.

Functions in Table 18 are divided into three distinct categories.

1. Multiplexor Channel Operations (D Bus Operations).
2. Byte Manipulations.
3. Auxiliary Functions.

TABLE 18. FUNCTION MNEMONICS

MNEMONIC	FUNCTION	COMMENT
RD/RDA	READ DATA	BYTE/INDEXED
WD/WDA	WRITE DATA	BYTE/INDEXED
OC/OCA	OUTPUT COMMAND	BYTE/INDEXED
SS/SSA	SENSE STATUS	BYTE/INDEXED
RDR/RDRA	READ DATA	BYTE/REGISTER
WDR/WDRA	WRITE DATA	BYTE/REGISTER
OCR/OCRA	OUTPUT COMMAND	BYTE/REGISTER
SSR/SSRA	SENSE STATUS	BYTE/REGISTER
ACK	ACKNOWLEDGE INTERRUPT	BYTE/REGISTER
RDH/RDHA	READ DATA HALFWORD	TWO DATA CYCLES FOR BYTE CONTROLLERS
WDH/WDHA	WRITE DATA HALFWORD	TWO DATA CYCLES FOR BYTE CONTROLLERS
THW	TEST HALFWORD	MSIG GENERATION
STB	STORE BYTE	HALFWORD/INDEXED
LB	LOAD BYTE	BYTE/INDEXED
STBR	STORE BYTE	HALFWORD/REGISTER
LBR	LOAD BYTE	BYTE/REGISTER
SMCR	SENSE MACHINE CONTROL REGISTER	
CMCR	CLEAR MACHINE CONTROL REGISTER	
EXB	EXCHANGE B-BYTES	
LDWAIT	LOAD WAIT FLIP-FLOP	B 16 to FWAIT
POW	RELEASE INITIALIZE RELAY	
POUT	GATE OUTPUT PULSES	

9.1.1 Multiplexor Channel Operations. D Bus functions include: RD, RDR, WD, WDR, SS, SSR, OC, OCR, RDH, WDH, ACK, RDA, RDRA, WDA, WDRA, SSA, SSRA, OCA, OCRA, RDHA, and WDHA (see Table 18).

When the I/O control is addressed and given a D Bus function code, it creates a one, two, or three cycle Multiplexor Channel operation.

The device address on A Bus (22:31) (refer to 8/32 IOU Block Diagram Figure 21) is gated to D Bus (06:15) together with the activating ADRS Control line whenever address type functions are specified. The addressed controller responds by returning a SYN signal which terminates the address cycle and starts a data cycle.

Delay timing within each cycle insures that the relationship of the MUX Bus Control lines and D Bus signals meet the Multiplexor Channel timing requirements.

The halfword functions (RDH/WDH) have a single data cycle when the Halfword (HW) Test line is active (communicating with halfword-oriented controller). Two data cycles are required when HW is inactive (byte-oriented controller is being addressed).

Output data is gated from the B Bus to the D Bus via the D Bus tri-state multiplexors controlled by ROM.

Input data coming from the D Bus is latched in the D Bus receivers and then gated onto the S Bus through S Bus Multiplexors which are also ROM controlled. In a Sense Status operation, D Bus receiver Bits 12:15 are also gated to the Condition Code (CC) Bus via the CC Mux. During all other D Bus operations, four zeros are placed on the CC Bus together with CC Strobe (SSC0).

At the end of the operation, the I/O control returns a Module Finished (MFIN) signal to restart the CPU clock.

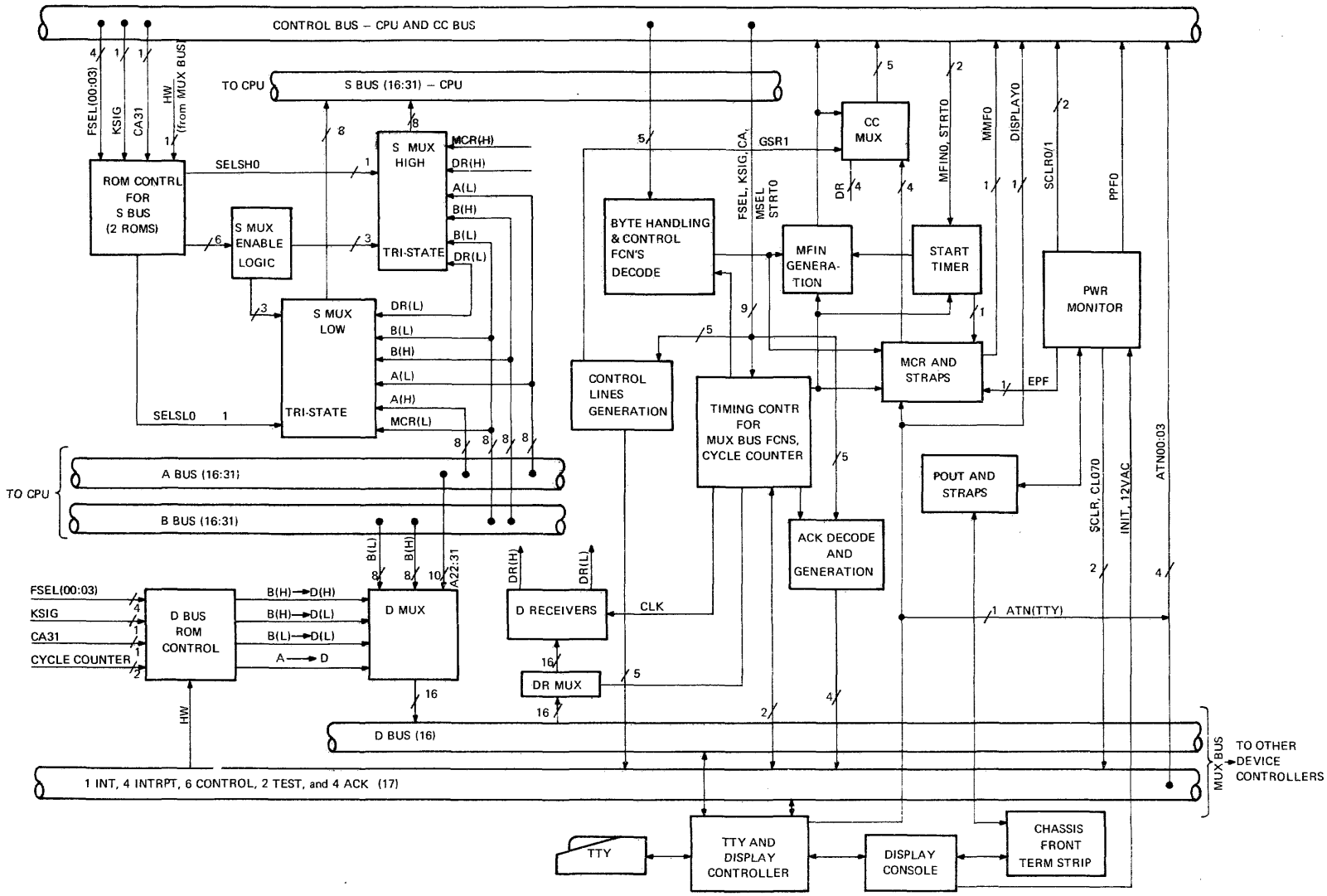


Figure 21. IOU Block Diagram

The ACK function generates a single cycle on the D Bus during which it activates one of four ACK lines and gates 10-bits of interrupting device address from the D Bus onto the S Bus.

All Multiplexor Channel functions are covered in detail in Section 10.

9.1.2 Byte Manipulations Functions. These include: STBR, LBR, STB, LB, and EXB (see Table 18). These functions do not activate the D Bus since only selected bytes are gated from the CPU's A and B Buses back onto the CPU's S Bus. This is achieved by ROM controlled S Bus Multiplexors. See Section 11.1 for more detailed description of these functions.

9.1.3 Auxiliary Functions. These include: SMCR, CMCR, LDWAIT, THW, POW, and POUT (see Table 18).

The SMCR and CMCR functions provide a means for Sensing and Clearing the Machine Control Register (MCR).

The LDWAIT function controls the ON/OFF indicator light on the Display Console.

The THW function generates MSIG according to the state of the HW (Halfword) Test line.

The POW function releases the System Clear relay.

The POUT function gates 4-bits on the B Bus (27:31) to a set of board stakes for external signaling purposes.

All auxiliary functions are covered in more detail in Section 11.2.

9.2 Machine Malfunction and Power Fail Hardware

Space is also provided on the 8/32 IOU board for a Machine Control Register (MCR), which stores machine trouble conditions; a Power Monitor and System Initialize circuit, and a Start Timer. This additional IOU hardware is covered in Section 10.11.

10. MULTIPLEXOR CHANNEL (MUX) BUS

10.1 Multiplexor Channel IOU

The main function of the IOU board is to provide a means for communicating with up to 1,023 peripheral device controllers and interfaces, including Display Console and Teletypewriter. IOU accomplishes this by generating Multiplexor Channel D Bus from the CPU busses whenever it is addressed by Module Number 2 and D Bus operation is requested by the CPU.

This byte of halfword oriented input/output system consists of 33 lines:

16 Bi-directional Data lines (also used for address).
6 Control lines (to identify the contents of the data line).
2 Test lines.
4 Interrupt lines.
4 Acknowledge lines (daisy-chains).
1 System Initialize line.

The 4 Interrupt lines terminate on the CPU-B (CPB) board and the 4 Acknowledge lines originate on the IOU module. The Initialize line is available to all system modules, controllers, and the local memory. Only one Interrupt line and one acknowledge daisy-chain is provided on a given I/O back panel. A single instruction from the CPU contains the 10 bit device address, the encoded function and up to 16 bits of output data when needed. The MUX Bus generator provides single or multicycle operation to address the device controller, transmit the decoded function and send or receive over the 16 Bi-directional Data lines and synchronize the exchange. The normal byte or halfword operation consists of address cycle, followed by a data cycle. During a Read/Write Block sequence, the address cycle is not used. For halfword functions (e.g., RDH or WDH) with a byte oriented controller, two data cycles are used to transfer the halfword.

The following definitions apply to the lines in the MUX Bus:

16 Data Lines (D00:15)

The 16 Bi-directional Data lines are used to transfer one 8-bit byte or one 16-bit halfword between the CPU and the device controller. Data Lines D08:15 are used for byte transfer. The 10-bit address sent from the CPU (or returned on an Acknowledge operation) uses Data Lines D06:15.

Control Lines (Manipulated by the Processor)

SR — Status Request. The Processor signals the last addressed device controller to send the device status to Data Lines D08:15, followed by a SYN.

DR — Data Request. The Processor signals the last addressed device controller to present data to the Data lines, followed by a SYN. (One byte or halfword of data is sent depending on whether the device is halfword or byte oriented.)

DA — Data Available. The Processor signals the last addressed device controller that the data on the Data lines is valid. The device controller accepts the low byte or the entire halfword and responds with a SYN.

CMD — Command. The Processor signals the last addressed device controller that the command byte on Data Lines D08:15 is valid. The device controller accepts the command byte and responds with a SYN.

ADRS — Address. The Processor signals that it presented 10-bits of address on Data Lines D06:D15. The device controller that recognizes its address responds with a SYN.

If no device controller recognizes its address in approximately 30 micro-seconds, the IOU generates a False SYN (FSYN).

CL070 — This line is activated by the IOU whenever any of the following occur:

1. The Initialize key on the Display Console is depressed.
2. The key-operated ON/OFF/LOCK Power Switch on the Display Console is turned OFF.
3. The primary power input falls below minimum operating level.
4. Auxiliary initialize inputs are activated (e.g., from LSU).

Test Lines (Manipulated by device controllers).

HW — Halfword. The Halfword line is activated by a halfword oriented device controller whenever it is communicating normally with the Processor (when its address flip-flop is set).

SYN — Synchronize. This signal is generated by the device to inform the Processor that it has properly responded to a Control line.

Interrupt and Acknowledge Lines.

ATN 00:03 — Attention. Any device controller desiring to interrupt the CPU, activates one of the four ATN lines and holds that line until the corresponding ACK signal is received.

ACK 00:03 — Acknowledge. The CPU acknowledges one of the four interrupts by asking the IOU to perform an ACK function. The IOU in response activates one of the four ACK lines, selected by 2-bits of the B Bus (30:31), each of which can feed a daisy-chain priority wiring pattern. The responding device controller presents its address on Data Line D06:15, followed by a SYN signal.

Initialize Line

SCLR — System Clear. This is a metallic contact to ground that occurs during Power Fail, Power Up or Initialize. The current carrying capability of the contact is limited. External circuits should not be connected directly to it. Refer to the bus buffer or buffered I/O channel for these applications.

NOTE:

All Control lines, except ACK are connected in parallel to all devices. These lines are activated by the Processor in response to an external interrupt. The ACK line is connected in series with all devices. If no interrupt is pending in the first controller when the ACK signal arrives, the signal is passed on daisy-chain fashion to the next controller, and so on until it is captured by the interrupting controller. See definition of ACK.

All busses are the false type (i.e., a low voltage level is active and a high voltage level is inactive.)

Each device controller is permitted one TTL load on any of the Data lines, Control lines, Acknowledge line, or the Initialize line. Furthermore, each device controller is permitted one OR tie onto a Data line, Test line, or Interrupt line. The controller bus driver must be either a high-power open-collector TTL gate or the tri-state equivalent.

A maximum of 16 I/O device loads can be driven from the IOU's unbuffered MUX Bus including Selector Channels, Bus Buffers, Bus switches, and Sub-Channel Controllers.

10.2 - Multiplexor Channel Timing

Input and output operations on the MUX Bus use request/response signaling. This allows the system to run at its maximum speed. Timing for typical input/output operations are shown on Figure 22. Detailed timing is shown on Figures 23 and 24.

On output, the CPU places signals on Data Lines D08:15, followed by an appropriate Control line signal. This Time delay (t1) varies but it is guaranteed to be at least 100 nanoseconds. When the device controller has received the Data line information, it sends the SYN signal to the CPU which terminates the Control line signal. The SYN Time delay (t2) should be only long enough to guarantee proper reception of the output data. The Control line/Data line removal time (t3) is guaranteed to be at least 100 nanoseconds. The SYN removal time (t4) should be minimized since the CPU does not proceed until the SYN signal is removed.

It should be noted that the times shown are defined for signals on the MUX Bus. Within a given controller, one signal may pass through more gates than another signal and these additional delays must be considered.

For the input operation, the CPU activates one of the input type Control lines and the currently addressed device controller gates onto Data Lines D08:15—keeping Time delay (t1) at a minimum. The SYN Time delay (t2) must guarantee that all the returned data is on the Data lines, considering the slowest data gates and the fastest SYN gates. The CPU removes the Control line signal when SYN is received, with a minimum Time delay (t4) of 100 nanoseconds. The SYN removal time (t3) should be minimized since the CPU does not consider the operation complete until the SYN signal is removed. When the Control signal is ACK, Time delay t1 includes the cumulative contention circuit delays for all the controllers, between the responding controller and the CPU.

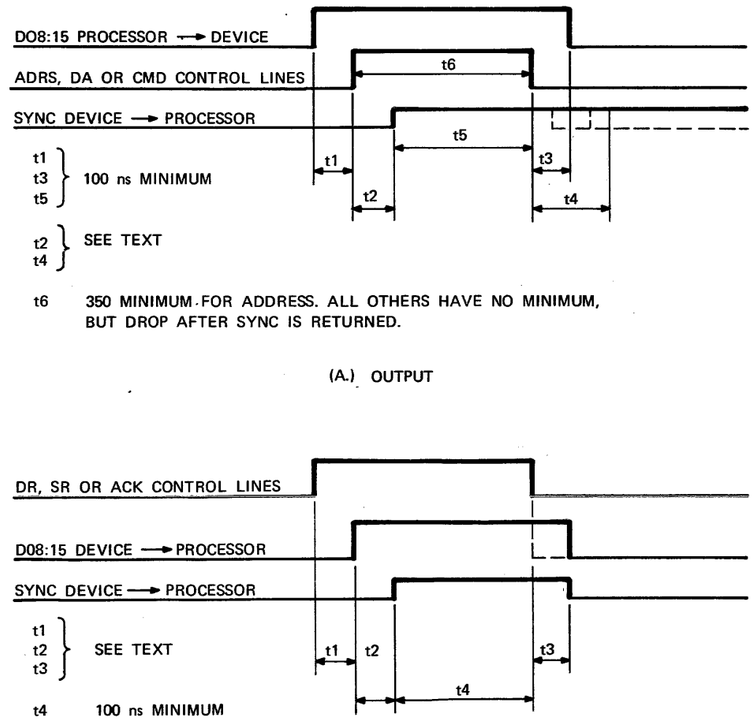
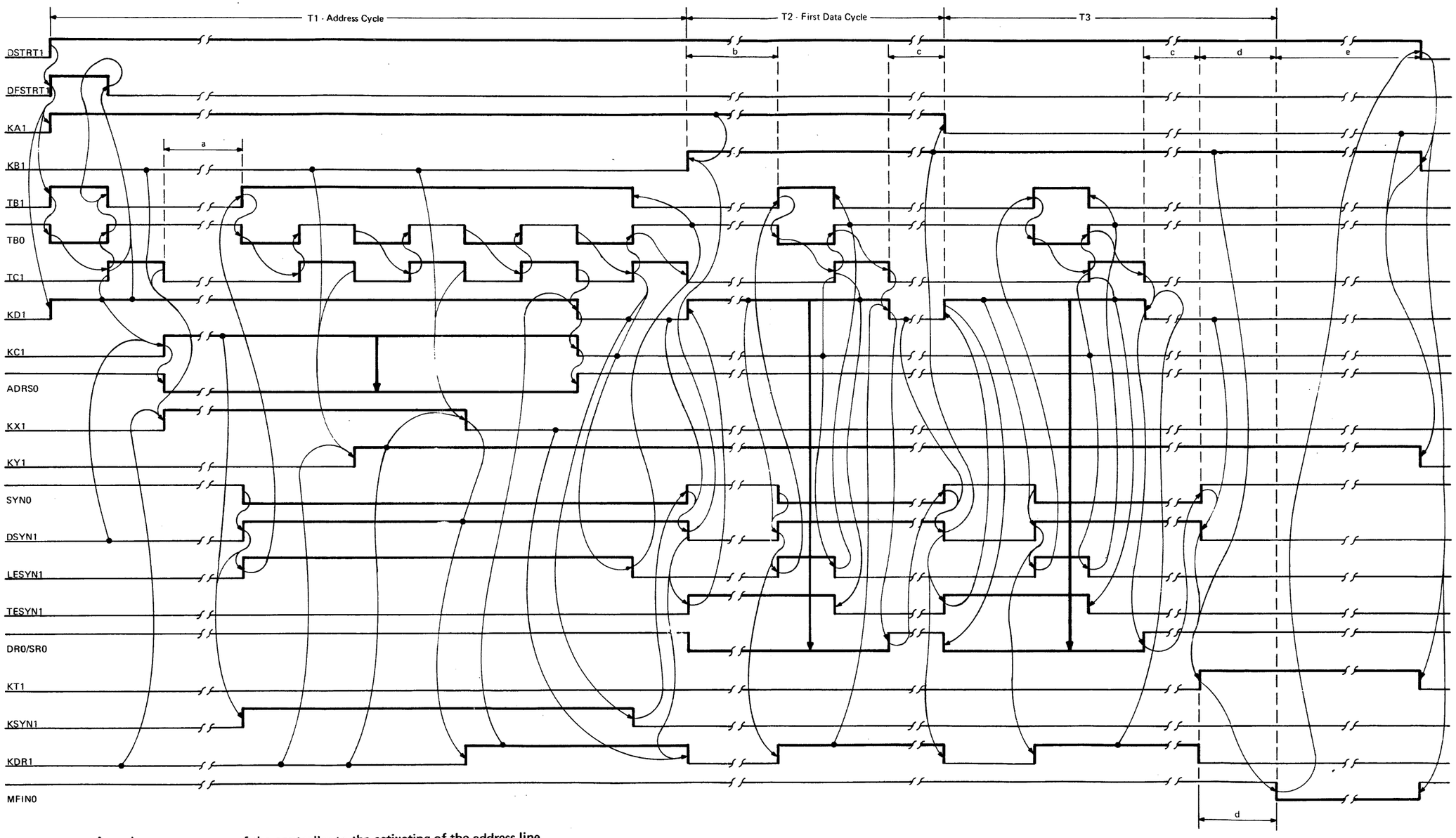
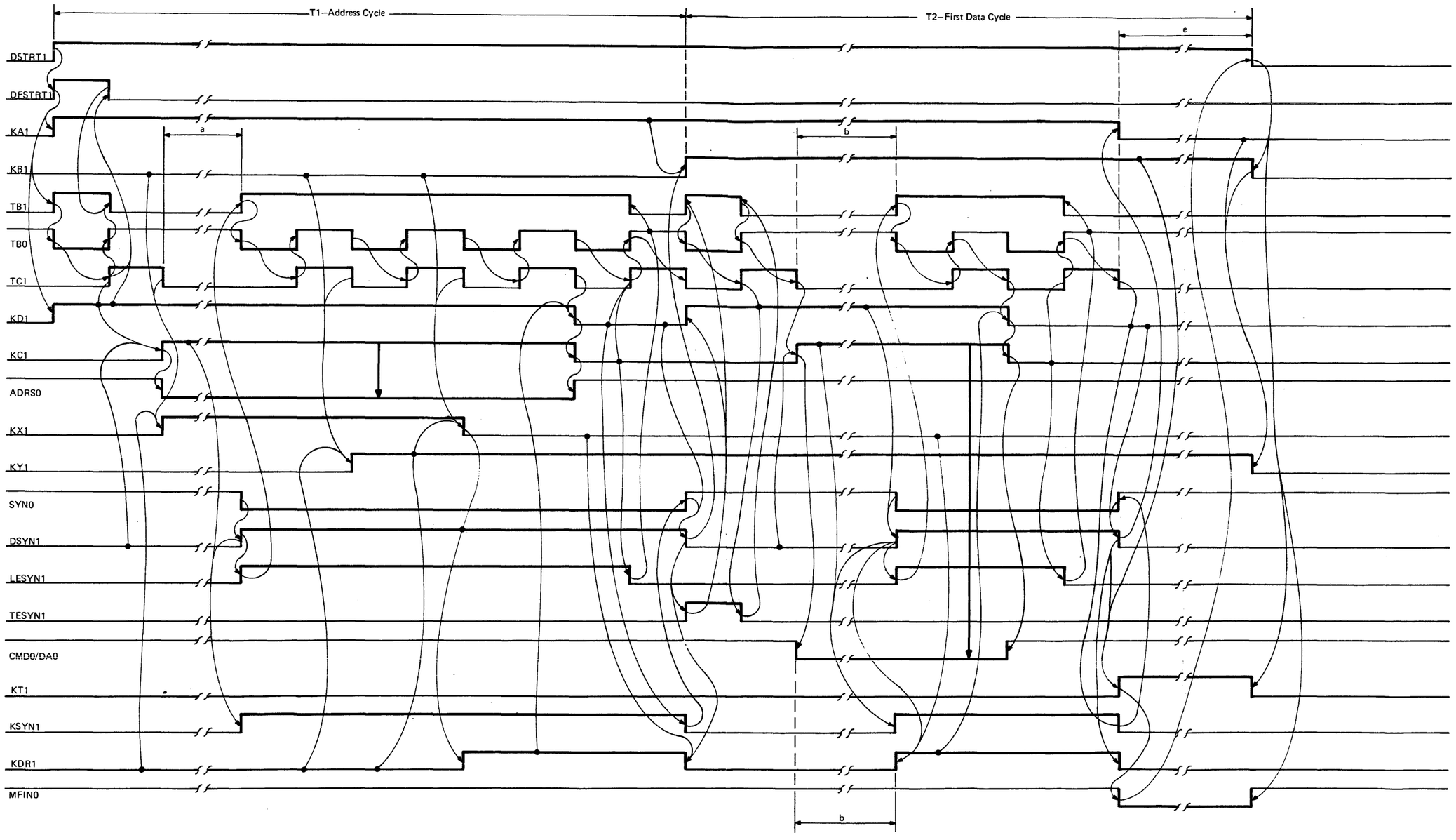


Figure 22. Multiplexor Channel Timing



a = Asynchronous response of the controller to the activating of the address line.
b = Asynchronous response of the controller to the activating of the DR/SR lines.
c = Time which particular controller needs to remove SYN after Processor removes control line.
d = 60 nanoseconds delay in generating MFIN for MUX operations (Input functions only).
e = Time required by the processor to remove STRT0 after sensing MFIN0.

Figure 23. Multiplexor Channel (Input) Timing ADRS and SR/DR



a = Asynchronous response of the controller to the activating of the address line.
b = Asynchronous response of the controller to the activating of the CMD or DA lines.
e = Time required by the processor to remove STRT0 after sensing MFIN0.

Figure 24. Multiplexor Channel (Output) Timing ADRS and CMD/DA

NOTE

With a SYN delay of 50 nanoseconds, device controllers must be designed to accept a minimum width of 170 nanoseconds on all Control lines and Acknowledge signals except ADRS, which is guaranteed to be 350 nanoseconds minimum. The SYN delay in the device controller may be increased to effectively lengthen the Control line signals if it is absolutely necessary. It is essential to realize that the CPU does not proceed until the SYN signal is returned and removed. While the slower data transfer rates may not affect a particular controller, the overall system performance is degraded. Furthermore, if a device controller fails to respond with a SYN signal within 25 to 35 microseconds, the CPU aborts the I/O operation.

10.3 Multiplexor Channel and Multiplexor Operations (MUX)

Operational and circuit description also refer to Section 9.1.1. This section covers the circuits which implement the D Bus operations.

10.3.1 MUX Channel Operation. MUX Channel is a byte or halfword oriented Input/Output system which communicates with up to 1,023 peripheral device controllers or interfaces. When I/O control is addressed and given a D Bus function code, it creates one, two, or three MUX Channel operations. The halfword functions (RDH/WDH) have a single data cycle when the HW (Halfword) Test line is active and two data cycles when a HW is inactive (communicating with byte-oriented controller).

10.3.2 Typical Output Case. (All cycles: Processor→Devices). A device controller receives 10-bits of address (over Data Lines D06:15) during the address cycle (T1). In the following first data cycle (T2), an 8-bit Command byte, or one byte of data (over Data Lines D08:15), or a Halfword of data (over Data Lines D00:15) is sent to the device.

For Halfword (HW) functions the cycle counter generates a second data cycle (T3) if necessary, in which case an additional byte of the Processor data is sent to the device over Data Lines D08:15 (see Section 10.3.1).

10.3.3 Typical Input Case. (Address Cycle: Processor→Device, Data Cycles: Device→Processor). A device controller receives 10 bits of address (over Data Lines D06:15) during the address cycle. In the following first data cycle, an 8-bit device Status byte, or one byte of device data (over Data Lines D08:15), or a halfword of device data (over Data Lines D00:15) is gated on the Processor's S Bus.

For Halfword (HW) functions, the cycle counter generates a second data cycle if necessary, in which case an additional byte of the device data is sent to the Processor (see Section 10.3.1).

10.3.4 I/O Function Gating. Table 19 shows IOU function gating specifications.

A single instruction from the CPU contains the device address, the encoded function, and up to 16 output data when needed.

D Bus functions may be performed with or without address cycle depending on the state of FSEL00.

KSIG is used to specify register type operations or to distinguish between Halfword (HW) functions (RDH/WDH) and some non D-Bus operations (STB/LB).

For byte designation used in Table 19 refer to the following information.

B(H) refers to Bits 16:23 from the corresponding B Bus.
B(L) refers to Bits 24:31 from the corresponding B Bus.
A(H) refers to Bits 16:23 from the corresponding A Bus.
A(L) refers to Bits 24:31 from the corresponding A Bus.
S(H) refers to Bits 16:23 from the corresponding S Bus.
S(L) refers to Bits 24:31 from the corresponding S Bus.
D(H) refers to Bits 00:07 from the corresponding D Bus.
D(L) refers to Bits 08:15 from the corresponding D Bus.
MCR(L) = MCR08:15
MCR(H) = MCR00:07

Note that Bits 00:15 of the Processor's A, B, and S Busses do not have an appearance on the IOU module (see block diagram Figure 21). The contents of S00:15 is zero when bytes are gated to S(H) and/or S(L).

10.3.5 MUX Bus Generation. (Circuit Description and Internal Timing.) The circuits which generate the D Bus and the companion Control Test lines are described in this section. Also a detailed description of one output function (WDA), and one input function (RDHA) are used to explain the operation of the MUX generation circuits.

1. MUX Generation Circuits. As seen on Figure 25, there are five general circuit groups for MUX generation:

   a. Input circuits.
   b. Cycle counter.
   c. Control line logic and bus drivers.
   d. D Bus gating and receiving logic.
   e. Internal Timing Differentiation and control logic.

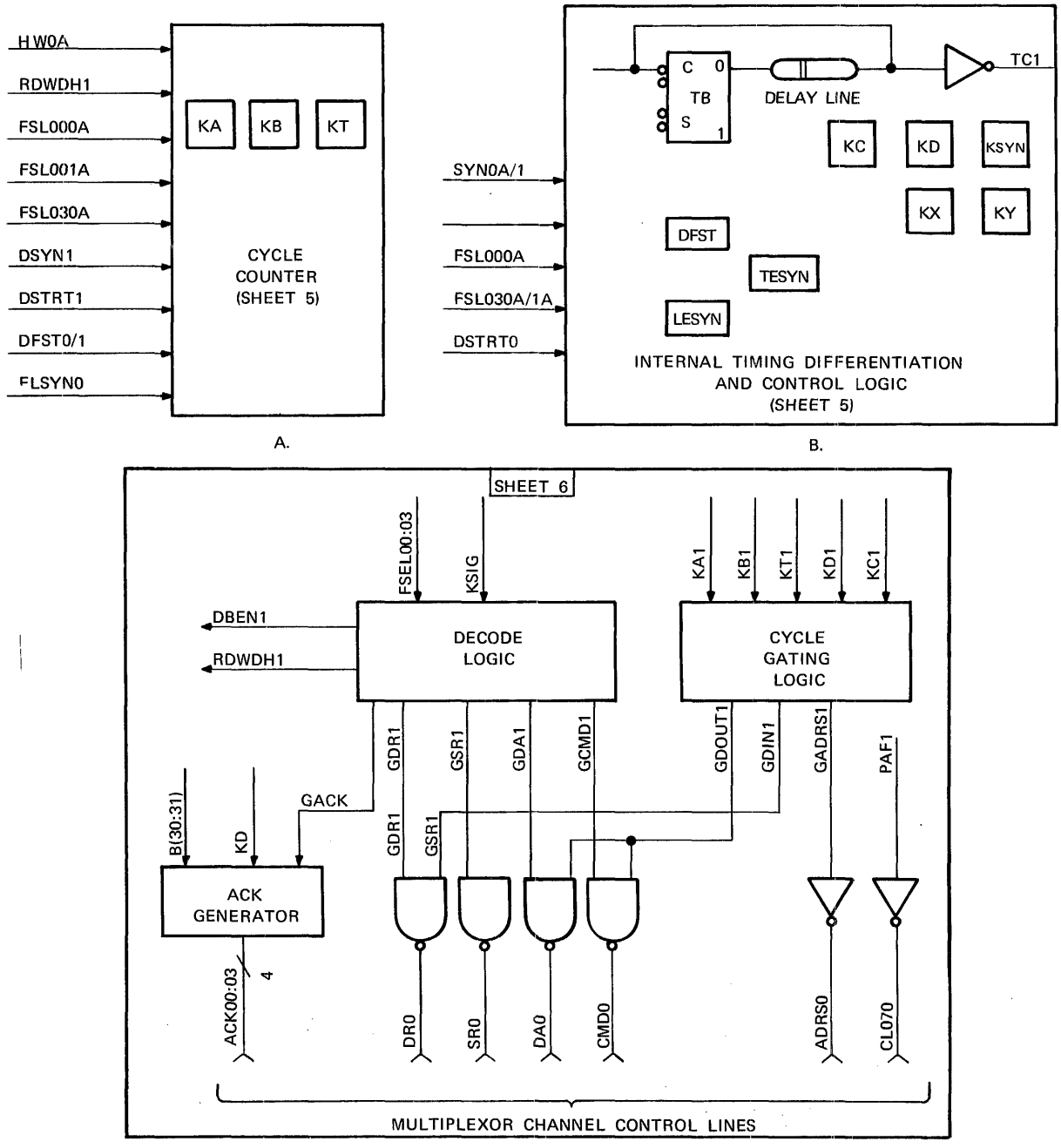


Figure 25. Multiplexor Circuit Generation Description

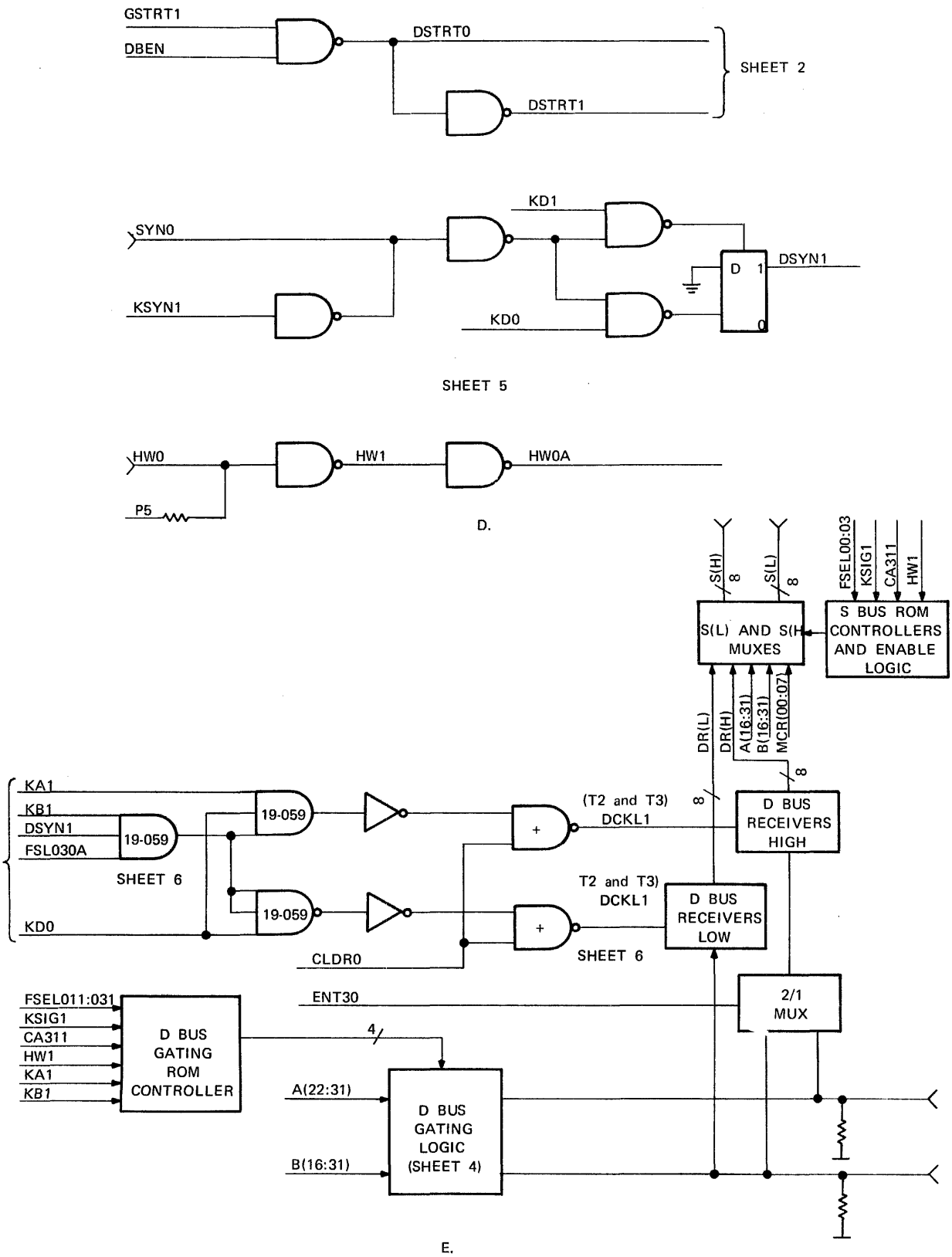


Figure 25. (Continued) Multiplexor Circuit Generation Description

The two edge triggered D type flip-flops KA and KB, connected as a Johnson Counter, together with the KT flip-flop (5N5) make up the cycle counter circuit. The sequence starts with DFST0 setting the KA flip-flop (5J6). When there is no address cycle, DFSTI and FSL000A (5K5) also set the KB flip-flop (5L6). The counter advances on the trailing edge of the DSYNI (5E7) signal which is stretched (if necessary) on the ADRS, CMD, and DA cycles. This insures that any byte gated to the D Bus remains for at least 100 nanoseconds after the associated Control line signal is removed. The sequence stops when the Terminate flip-flop (KT) (5N5) is set and the MFIN line to the CPU is activated. Operation of the KSYN flip-flop (5G8) which provides the SYN stretch, is described later.

A timing chart for the cycle counter is shown on Figure 26. From the idle time period T0, the counter is preset into period T1 or T2 depending upon the presence or absence of an address cycle. The sequence normally terminates at the end of T2 unless a halfword operation with a byte oriented device requires a second data cycle, T3 (ENT30) (5N7).

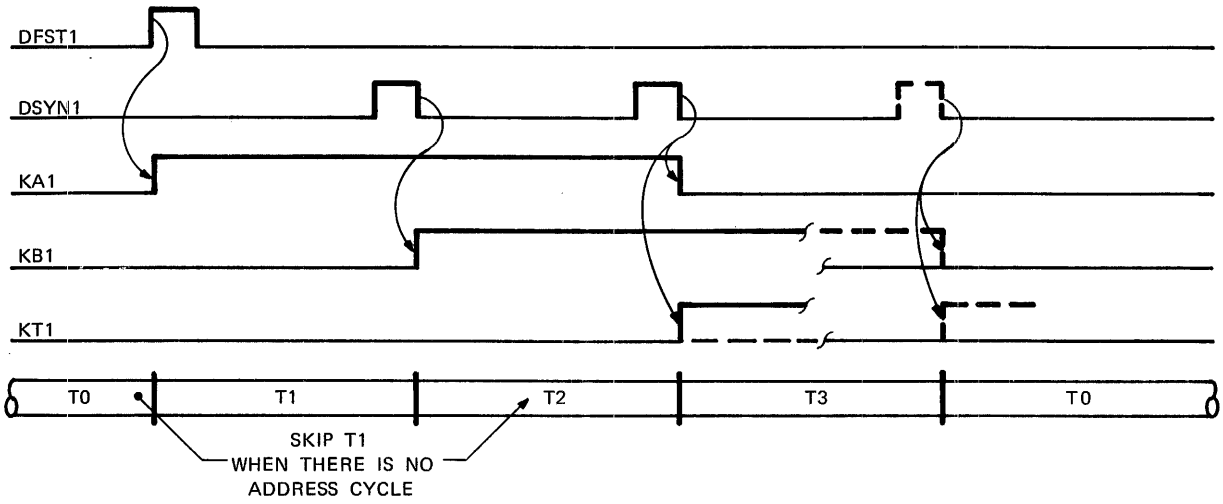


Figure 26. Cycle Counter

All D Bus operations begin when DBENI is gated by the GSTRTI signal (1G8) to produce the DSTRT0 and DSTRTI signals (5G9). These signals in turn are used by the STRT timer (14H8), the cycle counter, and the timing control circuit.

The SYN0 Test line is the main source of timing in the request/response signalling system used on the Multiplexor Channel. It must be carefully terminated and deglitched before being presented to the cycle counter and timing control. The leading edge of the Test line is gated by KD1 (5G6) to direct set the DSYN flip-flop (5E7). When the Control line signal to the bus is terminated, the KD flip-flop is cleared and the Test line is now connected to the clock input of the D type, edge triggered, DSYN flip-flop where the trailing edge clears the flip-flop. Once the DSYN flip-flop has been set or cleared, ringing or noise near the edges of the SYN0 signal is ignored. The trailing edge of SYN0 (5A6) is extended on output operations by the high KSYN1 signal (5A6). This is described in detail later.

The Halfword Test line (HW0) (5J2) produces the signals HW1 and HW0A which control data gating on the D Bus and indicate to the Multiplexor Channel circuits whether a byte oriented or halfword controller is in use.

The 10-bus drivers (Figure 25C), are the source of the Multiplexor Channel Control lines. Inputs are cycle gating and function decoder signals. GDOUTI (6M2) is active for output functions. GDINI (6K3) is active for input functions.

Both contain the intra-cycle timing signals KC1 (6N2) or KD1 (6L2). When data is placed on the D Bus for ADRS/CMD, or DA operations, the KC1 pulse provides the Control line timing, delayed 100 nanoseconds from the beginning of the cycle. For ACK, SR, or DR operations, the non-delayed KD1 pulse gates the Control lines. Both KC1 and KD1 are removed 100 nanoseconds after SYN0 is received, in accordance with Multiplexor Channel timing requirements. Only one out of four ACK lines is made active during any given ACK functions. The 19-129 3:8 decoder (6D2) selects the active ACK line according to the state of Bits 30 and 31. The signal CL070 (14K7) goes low active when Primary Power Failure (PPF1) is detected high, or INIT, or POFF go high.

The D Bus consists of 16 Bi-directional Data Lines terminated on the IOU board.

The 19-134 tri-state D Bus drivers multiplex 10-bits of A Bus and 16-bits of B Bus onto the D Bus. Their tri-state outputs are tied together in two groups to form D Bus high and D Bus low. Only one output for each D Bus line is enabled at a time, the others are in the high impedance state. This is achieved with the help of the D Bus ROM controller (4D3). Unlike the static selection of the S MUX controller, the D Bus ROM controller address selection (hence enabling of D Bus drivers) changes on every cycle of the sequence (KAI and KBI are used as address select onputs).

The 19-071 edge triggered D latches, used as D Bus receivers, load on the low to high transition of the clock leads DCKL1 and DCKH1 (6A5). The high byte register normally receives data from D00:07 during period T2 (KA1 and KB1) gated through the two-to-one MUX by ENT30 (6H6) in the high state. For the double data cycle, ENT30 is low active so that the first byte on D08:15 enters both DR00:07 and DR08:15 during T2. The second byte on D08:15, during T3, is registered in DR08:15 only to overwrite the first byte. Clock logic for DCKL1 and DCKH1 (6A2) uses the common term KB1·DSYN1. FSL030A which is active for all input functions, including ACK during periods T2 and T3. Final gating with KD0 loads the registers at the moment the selected Control line signal is removed; i.e., about 100 nanoseconds after the beginning of the SYN signal when the Data Lines have settled. The Data Register outputs feed the S MUX and the CC MUX.

The timing and control circuits provide the intra-cycle timing and SYN stretching features mentioned in earlier sections. These circuits consist of six edge triggered J/K flip-flops, a two stage counter, an R/S flip-flop, a 100 nanosecond tapped delay line, and the interconnecting logic. Three of the flip-flops, DFST (5E5), LESYN (5G2), and TESYN (5E6) detect the transitions of the DSTRT0 and DSYN1 signals respectively, and feed the delay line R/S flip-flop combination.

The TB flip-flop (5B4) is set by a low signal on Terminal 1, 2 or 4. A low signal on Terminal 9, 10, or 12 clears the flip-flop. When a momentary set pulse is applied, the high-to-low transition at TB0 travels down the delay line emerging after X nanoseconds as TC0 (5C2) to clear the flip-flop. This produces pulses TC0 and TC1 which are X nanoseconds wide and start X nanoseconds after the set TB pulse (where X is the tap delay plus the flip-flop transition times). Using the 50 nanosecond tap (Terminal 13 of the line), X is approximately 50 nanoseconds and the trailing edge of TC1 occurs 100 nanoseconds after the set pulse. When the set pulse is long enough to still be present after the end of TC0, TB0 again goes low to generate another pulse; i.e., the circuit acts like a gated oscillator. As seen on the timing charts which follow, both the single and multi-pulse modes are used.

The timing chart on Figure 26 shows a data output operation (CMD or DA) with an address cycle. The sequence starts with period T1 when the KA flip-flop is set. At the end of the first SYN pulse, the KB flip-flop is set and period T2 starts. The end of the second SYN pulse clears the KA flip-flop and sets the KT flip-flop. With KT0 low, gating to the D Bus/Control lines is suppressed (6L1) and the pulse generator is killed (5C3).

On both address and data cycles, the data bytes must be on the D Bus at least 100 nanoseconds before the Control line signal starts and must remain active for 100 nanoseconds after the Control line signal is removed. In addition, the Control line must remain active for 100 nanoseconds after SYN arrives. The width of the ADRS0 Control line pulse must be at least 350 nanoseconds. This insures that the Address flip-flop on a controller, separated from the CPU by one or more bus buffers, can be reliably cleared even with a fast SYN response from a local controller.

The DFST1 lead sets the Delay Line flip-flop (TB) (5B4) if it is either an output data cycle (FSL030A low) (5A4) or an address cycle (FSL000A low) (5A4). The KD flip-flop (5G6) is always set by DFST. Flip-flop KC (5G5) toggles set at the end of TC1 since its J input DSYN0 and direct clear (KD1) are both high. KC1 sets the KSYN flip-flop (5H8) and gates the Control lines as described earlier. The LESYN flip-flop (2G3) sets on the leading edge of DSYN and sets the TB flip-flop again. The KD flip-flop toggles clear on the first TC1 pulse after its K input goes high and in turn direct clears the KC flip-flop. For non-address cycles, the K input to the KD flip-flop (KDK1) goes high as soon as SYN is received, the next TC1 pulse clears the KD flip-flop after 100 nanoseconds. On the address cycle (period T1 with the KB flip-flop cleared), the TC1 pulses are fed to a two stage Johnson Counter, flip-flops KX and KY (5M8). The KDK1 input to the KD flip-flop is held low until after three TC1 pulses have been registered on the KX and KY flip-flops. The next TC1 pulse clears the KD flip-flop. In this manner the minimum width of KC1 and the ADRS0 signal are equal to 300 nanoseconds plus the SYN return delay (KDK1 = KXO·DSYN1). The KSYN flip-flop is cleared 100 nanoseconds after the KD flip-flop is cleared since its K input (KD0) is high when the next TC1 pulse arrives. KSYN (5A5) forces SYN1 and DSYN1 high as long as the KSYN flip-flop is set. This insures that DSYN1 and SYN0 remain active for at least 100 nanoseconds after KC1 and the Control line signals, gated by KC1, are ended. A fast SYN response from a device controller is not able to terminate the cycle prematurely and violate the timing rules for the D Bus.

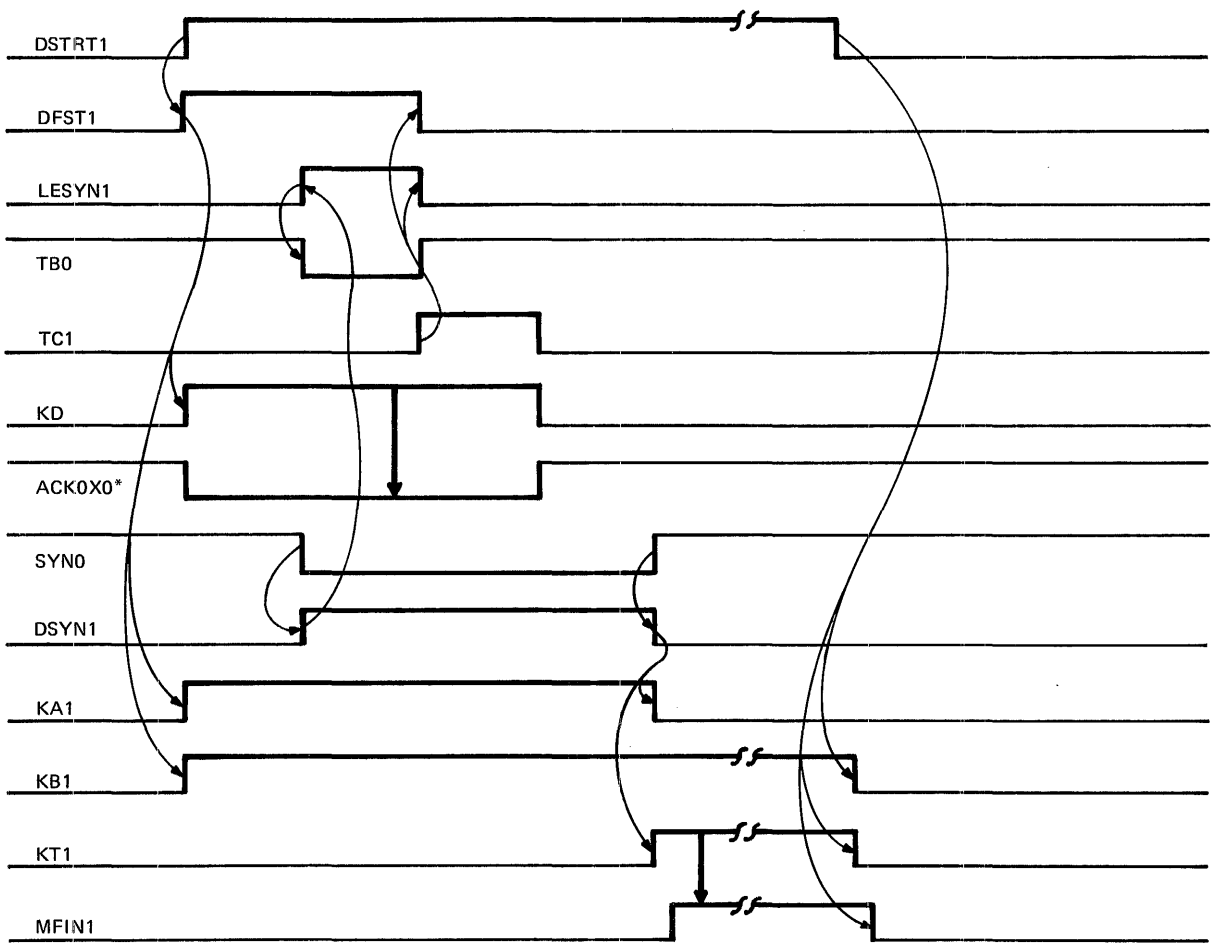
Note that the LESYN flip-flop remains set until the first TC1 pulse after the KC flip-flop is cleared. This produces the multi-pulse mode of the delay line; i.e., a group of TC1 pulses at 100 nanosecond intervals. Also note that while the KD flip-flop is not used directly for Control line timing, it is part of the logic for the KC and KSYN flip-flops.

The TESYN flip-flop (5E6) sets on the trailing edge of the DSYN1 signal and sets the TB flip-flop again if an output data cycle is required (FSL031A) (5B5). The KD flip-flop is direct set by TESYN. Timing for the output data cycle is similar to the ADRS cycle with two exceptions. First, the KX and KY flip-flops are not used to stretch the Control line signal and second, a double data cycle may be generated for the WDH operation to a byte oriented device. During the T2 SYN pulse, the logic that sets the KT flip-flop (5N6) also produces a low level on SKT0 (5N3). This causes the TESYN flip-flop to ignore the end of SYN1 (since both the J and K inputs are low) and the TB flip-flop is not set. When a double data cycle is needed, the set KT logic does not become active until period T3. The TESYN flip-flop sets on the end of the T2 SYN signal and thus pulses the TB/delay line circuit for timing control during period T3. It also applies to the ADRS and DR operations.

Figure 23 shows timing for a data input operation (SR or DR) with an address cycle. The TB flip-flop is set with DFST since KC1 is needed for Control line gating during the address cycle. It also applies to the ADRS and DR operations. The KX and KY counter insure the minimum width of the ADRS0 signal. TESYN sets the KD flip-flop at the end of period T1 but does not set the TB flip-flop. KD1 gates the Control lines for the input bytes. The KC and KSYN flip-flops are not used on the data cycles. A double data cycle is produced for the RDH operation to a byte oriented device.

For non-address functions, the sequences start with period T2 since the KA and KB flip-flops are both set with DFST. The data cycles on Figures 23 and 24 are essentially the same.

Timing for the ACK function is shown on Figure 27. It consists of a single data cycle (T2). The KC and KSYN flip-flops are not required. The TB flip-flop and the delay are pulsed only by LESYN to time the removal of the Control line signals.



* One of ACK00:03 selected by B30:31

Figure 27. Multiplexor Channel Timing, ACK

On all timing charts, the KT flip-flop generates S Bus and CC Bus gating and eventually the MFIN0 signal. This restarts the CPU clock causing the removal of STRT0, which in turn removes GSTRTI, DSTRT, and the MFIN signals.

A group of clear signals insures proper circuit states for initialize and other operations. CLRA0 (5N6) is low for SCLR0B low or any non-D Bus operation (DSTRT1 low). It clears the cycle counter and kills the pulse generator. CLRB0 (5C8), used by DFST and TESYN, cannot use DSTRT1 for clearing due to a possible race condition when the DFST flip-flop toggles set. It combines SCLR0B, TC1/KD1 (as per timing charts), and MFIN0A a copy of the MFIN0 generated by the IOU board.

CLRC0 (5H8) is low whenever the IOU cycle timer is inactive (period T0). CLRD0 (2C3) uses CLRC0 or TC1/KC0 (as per timing charts) to clear the LESYN flip-flop.

2. Output Operations (WDA). (See Section 10.3.2 and Figures 25E and 24.) A detailed description of the WDA (Address, Write Data) operation is used as an example of output operations.

The cycle timer must generate two cycles to execute the WDA instruction. The address cycle (TI) starts when DSTRT0 sets the DFST flip-flop (see Section 10.3.5). The 10-bits of address must be placed on the D Bus. This is accomplished by the D Bus controller outputs Y1, Y2, Y3, and Y4 equal to HHHL whenever address cycle (T1) is detected, see Figure 28, which shows all possible D Bus gating situations for WD and WDA instructions. The ADRS Control line is activated approximately 100 nanoseconds after the beginning of the address cycle to inform the interrupting device controller that the D Bus contains 10-bits of address. The trailing edge of KSYNI (SYN stretching signal) (5A5) starts the data output cycle (see Figure 24), in which either:

$$\left\{\begin{matrix}0 \longrightarrow D(H) \\ B(H) \longrightarrow D(L)\end{matrix}\right\} \quad \text{for CA311=L} \qquad \text{or} \qquad \left\{\begin{matrix}B(H) \longrightarrow D(H) \\ B(L) \longrightarrow D(L)\end{matrix}\right\} \quad \text{for CA31=H}$$

has to be gated onto D00:15. See Figure 28 and Table 19.

The DA Control line is activated about 100 nanoseconds after the beginning of the output data cycle (T2) to inform the interrupting device controller that the output data is settled on the D Bus. Interrupting device controller latches the data and responds with a SYN. The trailing edge of the KSYN (SYN stretching signal) (5A5) sets the KT flip-flop which generates MFIN (Module Finished) signal.

3. Input Operations (RDHA). (see Section 10.3.3 and Figures 25E and 23.) A detailed description of the RDHA (Address, Read Data Halfword) operation is used as an example of output operations. The cycle timer must generate three cycles to execute the WDA instruction. See Figure 23. The address cycle is identical to the one described in Section 2. Output Operations (WDA). The trailing edge of KSYNI starts the first data input cycle (T2), in which D00:15 is latched in the D Bus Receivers DR00:15. The Data Request (DR) Control line is activated at the start of the data cycle (T2) to signal the controller to put the data on D00:15 and activates the SYN line. If HW0 is active (Halfword oriented controller) only one input data cycle is necessary. If HW0 is high (byte-oriented controller) then it sends the most significant byte in T2 and the least significant byte (always via D08:15) in T3, the second data cycle. The latching of the D Bus in the D Receivers occurs approximately 100 nanoseconds after SYN is received (to insure settling the data).

The contents of the Data Receivers must be placed on S16:31. This is accomplished by two ROM controllers which control the multiplexing on the S Bus. See Figures 25E and 29.

11. BYTE MANIPULATION AND AUXILIARY FUNCTIONS

11.1 Byte Manipulation Functions

(STBR, LBR, STR, LB, and EXB – see Tables 19 and 20.)

These functions do not activate the MUX Bus since there is only need to gate selected bytes from A and B Busses onto the S Bus. Page 2 of the 35-539D08 schematics show the gating onto the S Bus High. The 19-132 tri-state S Bus 2:1 Multiplexors are tied in two pairs of three each, to allow for effective 6:1 Multiplexing (see Figure 21 block diagram). Only one output of the three tri-states is enabled at a time. Enable and select inputs are generated from Y1 to /4 outputs of S(H) ROM controller and from STC1 line active for non-D Bus operations. The same concept is used for generating S Bus low. (Page 3 of the 35-539D08 schematics.) ROM controller's S Bus generation for STB instruction is shown on Table 20.

Enable inputs of the S MUX low are used for MFIN generation for the case of byte handling operations (SMFIN is on Page 7 of the 35-539D08 schematics). These lines also become active for D Bus and SMCR operation so that the additional signals (SMCR0 and STC1) (7G7) are needed to insure that SMFIN0 (7H8) goes active only for five byte handling operations.

TABLE 19. I/O MODULE FUNCTION GATING

HEX. EQUIV. OF FSEL	FUNCTION	FSEL 0	FSEL 1	FSEL 2	FSEL 3	KSIG	CA31	HW	CA31=0 OR HW=0 DESTINATION(H)	CA31=0 OR HW=0 DESTINATION(L)	CA31=1 OR HW=1 DESTINATION(H)	CA31=1 OR HW=1 DESTINATION(L)	OTHER
0	RD	0	0	0	0	0	0/1	X	D(L)→S(H)	B(L)→S(L)	B(H)→S(H)	D(L)→S(L)	ZERO→CC
	RDR	0	0	0	0	1	X	X	ZERO→S(H)	D(L)→S(L)	ZERO→S(H)	D(L)→S(L)	
1	WD	0	0	0	1	0	0/1	X	ZERO→D(H)	B(L)→D(L)	B(H)→D(H)	B(L)→D(L)	ZERO→CC
	WDS	0	0	0	1	1	X	X	B(H)→D(H)	B(L)→D(L)	B(H)→D(H)	B(L)→D(L)	
2	SS	0	0	1	0	0	0/1	X	D(L)→S(H)	B(L)→S(L)	B(H)→S(H)	D(L)→S(L)	D(12:15)→CC
	SSR	0	0	1	0	1	X	X	ZERO→S(H)	D(L)→S(L)	ZERO→S(H)	D(L)→S(L)	D(12:15)→CC
3	OC	0	0	1	1	0	0/1	X	ZERO→D(H)	B(H)→D(L)	B(H)→D(H)	B(L)→D(L)	ZERO→CC
	OCR	0	0	1	1	1	X	X	B(H)→D(H)	B(L)→D(L)	B(H)→D(H)	B(L)→D(L)	
4	*RDH	0	1	0	0	0	X	0/1	D(L)1→S(H)	D(L)2→S(L)	D(H)→S(H)	D(L)→S(L)	ZERO→CC
	STBR	0	1	0	0	1	X	X	B(H)→S(H)	A(L)→S(L)	B(H)→S(H)	A(L)→S(L)	
5	*WDH	0	1	0	1	0	X	0/1	B(H)→D(L)1	B(L)→D(L)2	B(H)→D(H)	B(L)→D(L)	ZERO→CC
	LBR	0	1	0	1	1	X	X	ZERO→S(H)	B(L)→S(L)	ZERO→S(H)	B(L)→S(L)	
6	ACK	0	1	1	0	0	X	X	D(H)→S(H)	D(L)→S(L)	D(H)→S(H)	D(L)→S(L)	ZERO→CC
	LDWAIT	0	1	1	0	1	X	X	NA	NA	NA	NA	B(16)→FWAIT
7	SMCR	0	1	1	1	0	X	X	MCR(H)→S(H)	MCR(L)→S(L)	MCR(H)→S(H)	MCR(L)→S(L)	MCR(12:15)→CC
	CMCR	0	1	1	1	1	X	X	NA	NA	NA	NA	B(27:31)CLEARS MCR(11:15)
8	RDA	1	0	0	0	0	0/1	X	SAME AS RD AND RDR BUT PRECEDED BY ADDRESS CYCLE [A (22:31)→D (06:15)]				
	RDRA	1	0	0	0	1	X	X					
9	WDA	1	0	0	1	0	0/1	X	SAME AS WD AND WDR BUT WITH ADDRESS CYCLE				
	WDRA	1	0	0	1	1	X	X					
A	SSA	1	0	1	0	0	0/1	X	SAME AS SS AND SSR BUT WITH ADDRESS CYCLE				
	SSRA	1	0	1	0	1	X	X					
B	OCA	1	0	1	1	0	0/1	X	SAME AS OC AND OCR BUT WITH ADDRESS CYCLE				
	OCRA	1	0	1	1	1	X	X					
C	*RDHA	1	1	0	0	0	X	0/1	SAME AS RDH BUT WITH ADDRESS CYCLE				
	STB	1	1	0	0	1	0/1	X	A(L)→S(H)	B(L)→S(L)	B(H)→S(H)	A(L)→S(L)	
D	*WDHA	1	1	0	1	0	X	0/1	SAME AS WDH BUT WITH ADDRESS CYCLE				
	LB	1	1	0	1	1	0/1	X	ZERO→S(H)	A(H)→S(L)	ZERO→S(H)	B(L)→S(L)	
E	THW	1	1	1	0	0	X	X	NA		NA		HW→MSIG
	EXB	1	1	1	0	1	X	X	B(L)→S(H)	B(H)→S(L)	B(L)→S(H)	B(H)→S(L)	
F	POW	1	1	1	1	0	X	X	NA	NA	NA	NA	RELEASE SCLR RELAY
	POUT	1	1	1	1	1	X	X	NA	NA	NA	NA	B(27:31)→CABLE

TABLE 20. STB INSTRUCTIONS

FUNCTION	ROM ADDRESS SELECT IDENTICAL FOR BOTH S BUS CONTROLLERS 1 FSEL001	2 FSEL011	3 FSEL021	4 FSEL031	7 KSIG1	6 CA311	5 HW1	DATA TO BE GATED ON S(H) = S(16:23)	S(H) ROM.S OUTPUTS 12 SEL Y1	11 A Y2	10 B Y3	9 C Y4	DATA TO BE GATED ON S(L)≡S(24:31)	S(L) ROM'S OUTPUTS 12 SEL Y1	11 A Y2	10 B Y3	9 C Y4
STB	H	H	L	L	H	L	L	A(L)→S(H)	H	L	L	H	B(L)→S(L)	L	L	H	L
	H	H	L	L	H	L	H		H	L	L	H		L	L	H	L
	H	H	L	L	H	H	L	B(H)→S(H)	H	L	H	L	A(L)→S(L)	H	L	L	H
	H	H	L	L	H	H	H		H	L	H	L		H	L	L	H

FUNCTION / ADDRESS SELECT	FSEL011	FSEL021	FSEL031	KSIG1	CA311	HW1	KA1	KB1	CYCLE COUNTER STATE	DATA TO BE GATED ON D(00:15)	Y1	Y2	Y3	Y4
	15	1	2	3	4	7	6	5			12	11	10	9
	D BUS CONTROLLER INPUTS										D BUS CONTROLLER OUTPUTS			
	L	L	H	L	L	L	L	L	T0	DRIVERS IN H-Z	H	H	H	H
	L	L	H	L	L	L	L	H	T3	WILL NEVER OCCUR	X	X	X	X
	L	L	H	L	L	L	H	L	T1	A(22:31)→D(06:15) 0→D (00:05)	H	H	H	L
	L	L	H	L	L	L	H	H	T2	0→D(H) B(H)→D(L)	H	L	H	H
WD AND WDA	L	L	H	L	L	H	L	L	T0	DRIVERS IN H-Z	H	H	H	H
	L	L	H	L	L	H	L	H	T3	WILL NEVER OCCUR	X	X	X	X
	L	L	H	L	L	H	H	L	T1	A(22:31)→D(06:15) 0→D(00:05)	H	H	H	L
	L	L	H	L	L	H	H	H	T2	0→D(H) B(H)→D(L)	H	L	H	H
	L	L	H	L	H	L	L	L	T0	DRIVERS IN H-Z	H	H	H	H
	L	L	H	L	H	L	L	H	T3	WILL NEVER OCCUR	X	X	X	X
	L	L	H	L	H	L	H	L	T1	A(22:31)→D(06:15) 0→D(00:05)	H	H	H	L
	L	L	H	L	H	L	H	H	T2	B(H)→D(H) B(L)→D(L)	L	H	L	H
	L	L	H	L	H	H	L	L	T0	DRIVERS IN H-Z	H	H	H	H
	L	L	H	L	H	H	L	H	T3	WILL NEVER OCCUR	X	X	X	X
	L	L	H	L	H	H	H	L	T1	A→D	H	H	H	L
	L	L	H	L	H	H	H	H	T2	B(H)→D(H) B(L)→D(L)	L	H	L	H

Figure 28. D Bus ROM Controller Data Gating for WD and WDA

FUNCTION	ROM ADDRESS SELECT IDENTICAL FOR BOTH S BUS CONTROLLERS							DATA TO BE GATED ON S(H) = S(16:23)	S(H) ROM CONTROLLER OUTPUTS				DATA TO BE GATED ON S(H) = S(24:31)	S(L) ROM CONTROLLER OUTPUTS			
	FSEL001	FSEL011	FSEL021	FSEL031	KSIG1	CA311	HW1		Y1 Y1	A Y2	B Y3	C Y4		SEL Y1	A Y2	B Y3	C Y4
	1	2	3	4	7	6	5		12	11	10	9		12	11	10	9
RDH	L	H	L	L	L	L	L	DR(H)→S(H)	L	H	L	L	DR(L)→S(L)	L	L	L	H
	L	H	L	L	L	L	H		L	H	L	L		L	L	L	H
	L	H	L	L	L	H	L		L	H	L	L		L	L	L	H
	L	H	L	L	L	H	H		L	H	L	L		L	L	L	H
RDHA	H	H	L	L	L	L	L	DR(H)→S(H)	L	H	L	L	DR(L)→S(L)	L	L	L	H
	H	H	L	L	L	L	H		L	H	L	L		L	L	L	H
	H	H	L	L	L	H	L		L	H	L	L		L	L	L	H
	H	H	L	L	L	H	H		L	H	L	L		L	L	L	H

Figure 29. ROM Controller Data Gating for RDH and RDHA

11.2 Auxiliary Functions

(SMCR, CMCR, LDWAIT, THW, POW, and POUT – see Table 19).

These functions are described in this section. The SMCR function provides a means for sensing 16-bits of MCR, (Machine Control Register) see Section .

The SMCR function is decoded by a 3:8 decoder (7B7), MCR11:15 is placed on the CC Bus by 2:1 CC Bus MUX (7E2). The SMCRO line also generates MFIN and the strobe for Condition Code. The contents of MCR00:15 is gated onto the S00:15 by the 19-132 S Bus Multiplexors (ROM controlled) shown on Pages 2 and 3 of the 35-539D08 schematics.

The DMCR function is decoded by the 19-129 3:8 decoder, whose CMCR0 output enables the four least significant bits of the B Bus (7B2) to clear selectively four MCR registers. (Ones in B27:31 clear the corresponding MCR registers.)

The LDWAIT function is decoded by the 19-129 3:8 decoder, it controls the indicator light on the Display Console (ON or OFF) according to the state of B16.

The THW function is decoded by the 19-129 3:8 decoder (7B7) it generates MSIG according to the state of the HW (Halfword) Test line.

The POUT function is decoded by the 19-129 3:8 decoder it gates four bits (B27:31) to a set of board stakes for external signalling purposes. These signals may be wired to the front chassis terminal strip by adding optional wires to the Display Console connector at the IOU board. The MFIN signal to the CPU is delayed by a timer to set the output pulse width at 1.0±0.3 microseconds.

The POW functions releases the System Clear relay, (see Section 10.11).

12. DISPLAY CONTROLLER

The display controller has access to the CPU via the Multiplexor Channel D Bus and the I/O control in the same manner as other peripheral device controllers. The display controller provides a means for reading the contents of all the system registers or any main memory location and transferring the data to the Display Console.

Data and programs can also be manually entered from the Display Console to the controller and then to the CPU. The display controller signals the CPU directly via the Display (DSPLY) interrupt.

12.1 Addressing Logic

The Display Console device address is wired as (X'01'). The D Bus lines D08:15 are buffered and inverted to create double rail Data Lines (Sheet 8). Two more bits of the D Bus (06:07) are used directly in address decoding logic on Page 9 of the 35-539D08 schematics.

The decoded Display Console address activates B1 line (9H4), which sets the ADB flip-flop (9M4) at the trailing edge of the ADRS0 Control line signal. B1 also generates ADSYNB0 (10K4) which generates the SYN signal and clears the CATN flip-flop (10F6).

12.2 Data Output

The byte of data transferred between the display controller and the Display Console Makes use of 8-bidirectional lines SD00:07 (8H4). Data is placed on this SD Bus when the DAGB0 line is active and is gated to one of the four display registers in the Display Console, by one of the load signals, LA or LB (13J5). LA and LB generation logic is shown on Page 13 of 35-534D08 schematic. Two one-shot timers (13E2 and 13J2) insure that the loading signals conform to Display Console specifications. The XA flip-flop is reset by RST0=ADRSI·INCR0·B1.

12.3 Data Input

XC flip-flop (13E8) controls the SHI0 and SL00 signals which gate the contents of the two least significant bytes of the Console Switch Register to the Processor via SD00:07. The RST0 signal clears the XC flip flop in the same manner as it cleared XA.

12.4 Status Input

The Status byte encoding is shown in Chapter 11, in the Model 8/32, 8/32C, 8/32D Users Manual, Publication Number 29-428.

12.5 Control Logic

Complimentary pulsed ESN00 and ESNC0 signal from the console are fed into a deglitching R-S flip-flop (10C5). ESN00 and ESNC0 are activated by depressing various keys of the Display Console keyboard (see Section 12.1). This results in setting a CATN flip-flop and generating display controllers private interrupt to the CPU-DSPLY (10J8). DSPLY interrupt is also generated by depressing the SNGL key on the Console keyboard, which sets the SNGL flip-flop. The SNGLO flip-flop (10F8) can be sensed by CPU as MCR07. The INCR flip-flop (10C2) which determines either incremental or normal mode sets on the trailing edge of the CMGB0 control line. All Control lines for the display controller (6N5-9) are derived from the MUX Bus control lines by gating them with the output of the controllers Address flip-flop ADB (9M4). These Control lines are also used for the Display Consoles SYN generation (7C8). The D Bus drivers and receivers, SYN generation logic, and part of the address decode logic is shared with the Teletypewriter controller.

13. TELETYPE CONTROLLER

The built-in Teletype (TTY) device controller interfaces an ASR;KSR 33 or 35 TTY to the Processor. It provides the serial/parallel conversion required for data transfer between the parallel D Bus and the serial, eight level, start/stop ASCII code signal used by the TTY (see Figure 30).

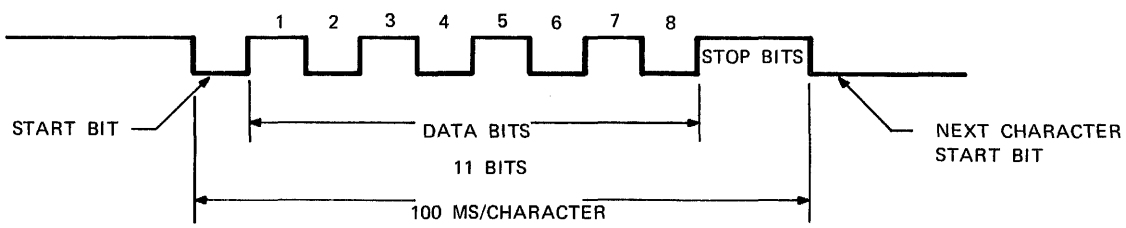


Figure 30. Serial ASCII Code U (Even Parity)

13.1 Block Diagram Analysis

Figure 31 is a block diagram of the TTY controller. The control circuits consist of the Command flip-flops (read or write, etc.) which direct the flow of information, circuits to control ATN/ACK functions, and logic to generate the status bits and control the timer.

The serial information received from the TTY is sampled by the timer and strobed into the Shift Register. When all the data has been shifted in, the data in the Shift Register is transferred to the Buffer Register. It is then gated through D Bus tri-state drivers on D08:15), by the Data Request signal (DRG), Status Request Signal (SR), and Address (ADRS) Control lines. A bit-by-bit copy of the received data may also be sent to the TTY printer/tape punch when the Block flip-flop (BLK) is cleared. In the Write or Send mode, the data byte is placed directly (parallel) into the Shift Register and then shifted out (serially) to the TTY.

13.2 Bus Communications and Address Circuits

Communications between the Processor and the TTY controller is via the Control lines, Test lines, and the low order eight bits of the D Bus. The bus receivers (Sheet 8) are shared with the display controller. The Data Lines D08:15 are buffered to form the DL00:07 lines. When the wired address X'02' is detected, Line A0 is active and the TTY address flip-flop (ADA) (9M3) is toggled set on the trailing edge of the ADRS1 signal (9J2). This enables the other Control lines for the TTY controller (Sheet 10). While the ADRS1 signal is active, the ASYNA0 line goes low and generates the return SYN0 signal (11G9).

The D Bus sent logic consists of 19-136 tri-state bus drivers (Sheets 8, 9, and 11) controlled directly by DRGA0, SRGA0 and ATSYN0 TTY Control lines, which are derived from the corresponding MUX Bus control and TTY Address flip-flop (Sheet 10).

NOTE:

For systems where X'02' has been assigned to another device, the TTY controller may be strapped for X'82'. (see Sheet 7).

13.3 Status and Commands

The bit assignments for TTY status and command bytes is shown in Table 21.

TABLE 21. TELETYPE STATUS AND COMMAND BYTE

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE	ERR	*	BRK	*	BSY	EX	*	DU
COMMAND BYTE	DISABLE	ENABLE	UNBLOCK	BLOCK	WRITE	READ		
	DISARM							

* Unassigned status (will return zero).

STATUS BYTE

ERR — The Error bit is set when a character is not taken from the controller buffer before another character is assembled.

BRK — The Break bit is set at the end of one character time when the line is held in the space condition for a period greater than a character period.

BSY — Read Mode. The Busy bit is normally set and is reset when data is available for transfer to the Processor. Write Mode. The Busy bit is normally reset and is set when data is being transferred to the terminal.

EX — The Examine bit is set when BRK or ERR is set.

DU — The Device Unavailable bit is set when the terminal is powered down or in Local mode.

COMMAND BYTE

DISABLE	Disables device interrupts; allows queuing of interrupts.
ENABLE	Enables device interrupts. Note that a command byte with both Bits 0 and 1 set, DISARMS the interface, no interrupt queuing.
UNBLOCK	Allows the Printer to print data entered via the keyboard or tape reader.
BLOCK	Disables the Unblock feature.
WRITE	The interface is placed in the Write mode.
READ	The interface is placed in the Read mode.

The command flip-flops EBL, ARM, BLK, and WT (9J7, 9L7) are loaded with the trailing edge of the CMGA0 signal (9D7). The contents of the flip-flops remain unchanged if the D input is low. The Write Storage flip-flop (WT) (9L7) unconditionally accepts the Read/Write signal from the Processor, however, the Write Execution flip-flop (WRT) (12D5) can only be updated when the timer has stopped; i.e., when TMG0 (12A4) is high.

The EBL and ARM flip-flops (12J7) are loaded from DL00 and DL01 as described in Table 21. They control the action of the Interrupt flip-flop (INTR) (12E8) and the interrupt line ATN0 (12G7).

The Block flip-flop (BLK) controls the serial feedback of data from the TTY receiver to the TTY driver. When reading a non-ASCII tape, it is inconvenient and undesirable to permit the received data to reach the printer/stunt box and operate the bell, line feed, form feed, etc., functions. This feedback is broken when the BLK flip-flop is set. Sending data to the TTY from the Shift Register is not affected by the BLK flip-flop.

The Busy (BSY) status bit is controlled by the Write Execution flip-flop not the WT flip-flop. The Break bit remains set as long as the Break key is depressed at the TTY. The Error bit (overflow) is cleared by either a Data Request, any command, or the system initialize signal SCLR0.

13.4 Timer Circuits

The timer consists of the control flip-flop (TMG) (12D2), a 440 HZ multi-vibrator MTA (12H3) and MTB (12K3), a two-stage clock counter MTC (12G4) and MTD (12H4), and a character counter (TA, TB, TC, and TD) (12L6). In the idle or reset state with the TMG flip-flop cleared, TMG1 (12D2) is low to disable MTA and MTB, to clear MTC and MTD, and to preset the character counter to the count of five.

When the TMG flip-flop is toggled set at the end of DAGA0 (12A2) in the Write mode; TMG1, TMG1A and DTMG1 all go high to enable the timer. The 440 Hz pulse train (MTB1) (12L3) drives the two-stage counter (MTC and MTD) and a decoder gate to generate the 110Hz train of clock pulses (CLK0 and CLK1) (12K4) and the shift pulses (SHFT1) (12N4). After the end of the ninth clock pulse, TB1, TC1, and TD1 are all high, thus forcing FSTP0 (12M5) low to terminate the train of shift pulses. During the eleventh clock pulse, EOC0 (12A2) goes low, and the TMG flip-flop is toggled clear on its trailing edge. This produces a train of eleven clock pulses and nine shift pulses having a period of 9.09 milliseconds (110Hz) with the trailing edge of the first pulse occuring 9.09 milliseconds (one bit period) after TMG is set. The pulse width is approximately 1.15 milliseconds (one-eighth of a bit period).

The idle timer is also started (by the direct set pulse ST0) (12E3) when the received Start bit arrives from the keyboard or tape reader or due to depression of the Break key. This is not dependent on the Read/Write mode since the BRK condition must be detected in both modes. The width of the ST0 pulse is determined by delay Capacitor 02HC1 (8G1) which generates the delayed TMG0 signal DTMG0 (12C4). Since the MTD flip-flop is direct set ST0, the first CLK/SHFT1 pulse occurs 4.545 milliseconds (half of a bit period) after the TMG flip-flop is set; the period of the pulses is still 9.09 milliseconds. Received data is sampled/shifted at the center of each bit. The TMG flip-flop is toggled clear at the end of the EOC and TTMG pulses as before.

13.5 Data Output

The TTY controller is in the Write mode when both the WT and WRT flip-flops are set. To send data to the TTY, the DAGA0 line (11A5) goes low to load DL00:07 into the Shift Register, clears the Start bit flip-flop (DRN) (11N6) and toggles set the Timing Gate flip-flop (TMG) (12D2). Note that if the timer was already running when the Data Available Control signal is received, the DAGA0 signal (11A5) would be blocked by TMG0 (12D2) low, no return SYN would be generated, and the false sync condition would be detected after 35 microseconds. For this reason the WDH instruction must not be used with the TTY controller.

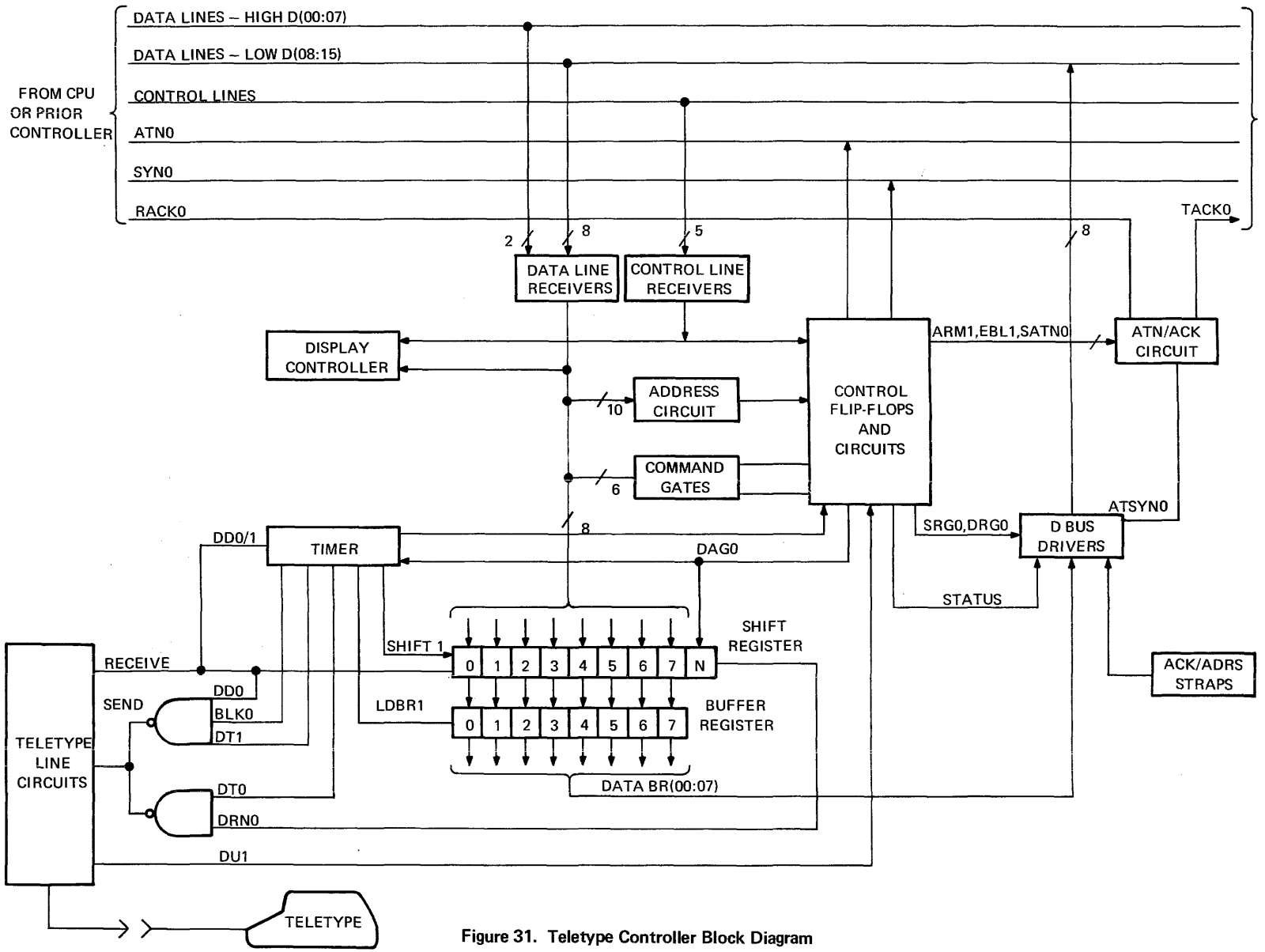


Figure 31. Teletype Controller Block Diagram

When the timer starts, shift/clock pulses are generated as described earlier and shown on Figure 32. The bit stored in the DRN flip-flop is connected to the transmit line (TNSB1) (16D2) by the high states on the device transmitting (DT0) and the TMG1 lines. Since the DRN flip-flop is initially cleared by DAGA0, TNSB1 goes low, and the gate driving TNS0 turns off to send the open-loop Start bit condition. At the end of each shift pulse, as the eight data bits are sequentially transferred into the DRN flip-flop, a high state at the serial input of the Shift Register (DX1) (11B2) gradually loads the register with all ones (including the DRN flip-flop).

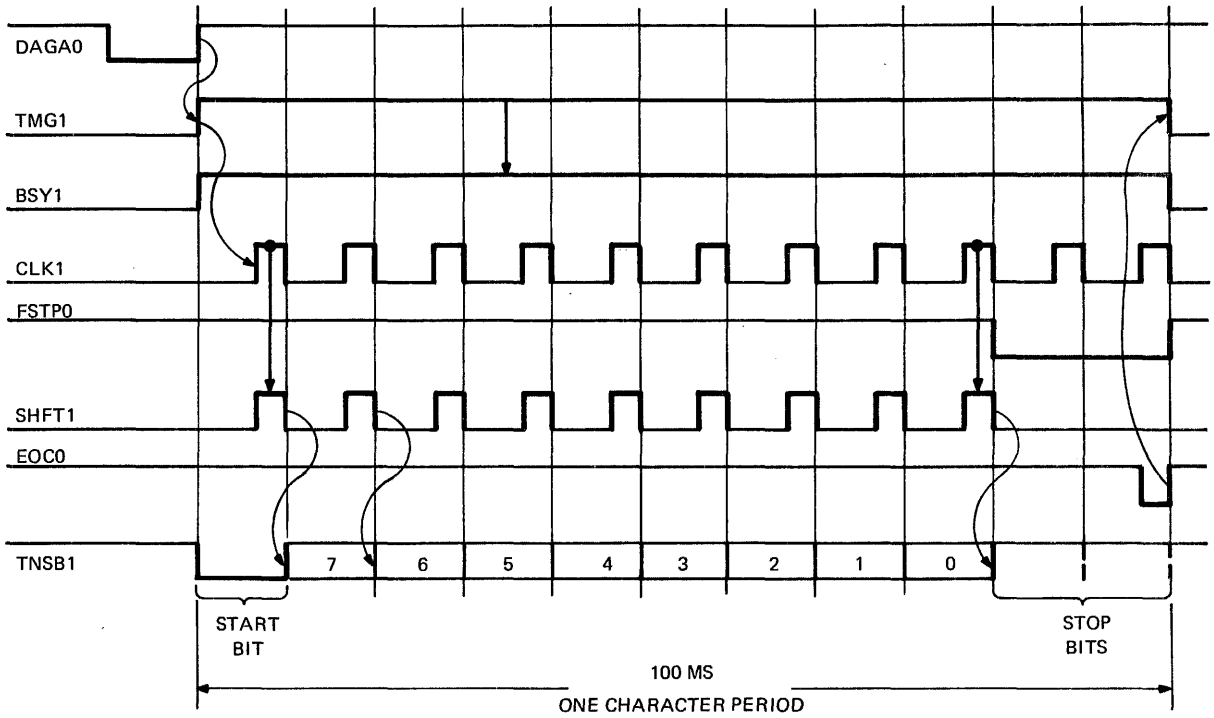


Figure 32. Write Mode (Output) Timing, Teletype

During the last two clock periods, after shifting has stopped, the ONE Level stored in the DRN flip-flop is sent out as the closed-loop Stop bit condition. The EOC pulse clears the TMG flip-flop to generate the closed-loop idle condition.

With the WRT flip-flop set, the status bit BSY1 (12D6) is active when TMG1 is active. Should a command which clears the WT flip-flop (Read mode) be received while the timer is running, the WRT flip-flop (and the definition of BSY status) does not change until the TMG flip-flop is cleared and TMG0 (8F8) gates WT1 into the WRT flip-flop.

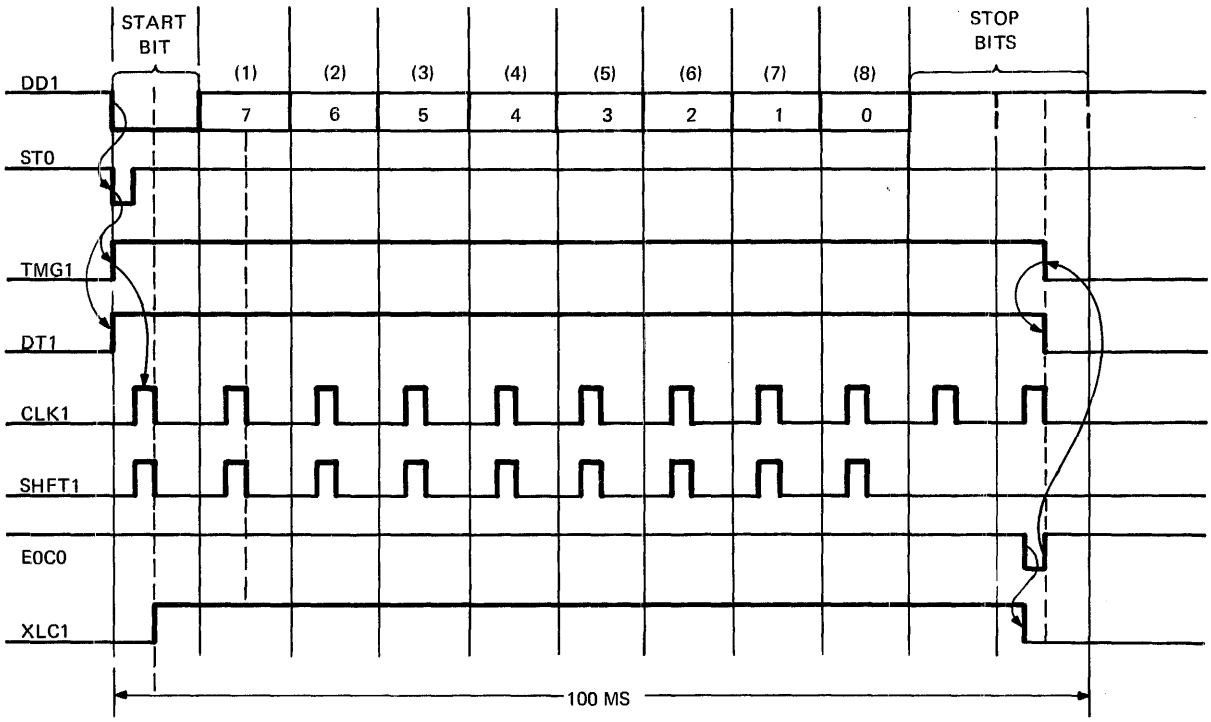
13.6 Data Input

The timer circuit can be started from the TTY receive loop in either the Read or Write mode as described in Section 13.4. This insures that the Break condition is always detected. However, serial data cannot enter the Shift Register (DX1) (11B2), unless the TTY controller is in the Read mode; i.e., the WRT flip-flop is cleared and WRT0 high. The Load Buffer Register pulses (LDBR1) (8G2) are generated only in the Read mode.

The Device Data line (DD1) (16G7) is high active when there is current flowing in the receive loop. This represents the logic ONE level and also the idle loop condition. The signal from the receive loop is filtered by an RC network (180 ohms/2.2 mfd) (16J8) and then reshaped by the Schmidt Trigger circuit (composed of a pair of inverters and two resistors) (1GE7) to generate the DD0 and DD1 signals.

When DD0 and DD1 first become active, the timer is started by the ST0 pulse (as described in Section 13.4) and the Device Transmitting flip-flop (DT) (11J6) is set. This flip-flop forces the TNSB1 line high and partially selects the TNSA1 gate, subject to a high level on the BLK0 and DD0 lines; i.e., the serial feedback circuit to the TTY Printer/Punch. The DT flip-flop also arms the Line Check flip-flop (XLC) (11M7) by placing a high level on the D input.

As seen on Figure 32, the XLC flip-flop is toggled set at the end of the first SHFT pulse. During the first SHFT pulse, the receive loop is checked to insure that the loop is still open; i.e., a legitimate Start bit has started the timer. If the loop is closed, DD1 is high and the Start Glitch pulse (GLTCH0) (12B2), is generated to clear the TMG flip-flop at the end of the SHFT pulse. The timer is reset, there are no EOC or LDBR pulses, the Buffer Active flip-flop (BA) (8E8) and the BSY status are unchanged.



Note: Bit Designations (X) are Paper Tape Channel Numbers.

Figure 33. Read Mode (Input) Timing, Teletype

The serial data at the Shift Register input (DX1) (11B2) is active when the DD1 line is active. The nine SHT1 pulses move the received data into and along the Shift Register until the Start bit and the eight data bits occupy DRN and SR00:07. Shifting occurs at the end of each SHFT pulse; i.e., the center of each bit.

The TMG flip-flop toggles clear at the end of the EOC pulse and clears the DT flip-flop. The XLC flip flop is cleared by EOC if the loop is closed due to a Stop bit, DD1 high (16E7). In the case of a missing Stop bit (or Break condition), the XLC flip-flop remains set after the EOC pulse has cleared the TMG flip flop. The function TMG0·XLC1 causes BRK0 (8K7) to go low, and lines BRK1, EX1, and EX0 to become active. The timer cannot restart on the open loop condition since ST0=DTMG0·DD0·XLC0.

The BRK condition continues until the receive loop is closed. The DD1·TMG0 function then clears the XLC flip-flop.

In the Read mode, BSY1 (12D6) is low whenever the Buffer Active flip-flop (BA) (8E8) is set. The EOC1 pulse generates the LDBR1 pulse to load the Buffer Register and toggle set the BA flip-flop. The DRGA0 signal (8A9) clears the BA flip-flop when the buffer is gated to the D Bus. An overflow or error state exists if the LDBR1 pulse finds the BA flip-flop still set, the Overflow flip-flop (OV) (8G8) is then set. The OV and BA flip-flops are cleared by the DRG pulse, any CMG pulse, or the initialize signal SCLR0B.

13.7 Interrupt Circuit

The TTY controller generates an interrupt for a negative transition on BSY1. This transition toggle sets the DFBSY0 (12E7) flip-flop which in turn direct sets the INTR flip-flop (12E8). This forces ATN1 high and ATN0 low.

The Processor responds by executing an Acknowledge interrupt. When the TTY controller has first priority, the RACK0 lead goes low forcing RACK1 and DRACK1 high. With GATN1 high, the TACK0 gate is blocked and the ATSYN0 line goes low. This gates the controller address X'02' to the D Bus, generates the return SYN0, direct clears the DFBSY flip-flop, and clears the INTR flip-flop at the end of ATSYN0.

When the system uses the Memory Protect and/or the Real Time Clock controllers, the RACK0/RACK0 daisy-chain is wired to the higher priority controllers before it reaches the TTY over the back panel.

As noted, in Section 13.3, the Disable command clears the EBL flip-flop forcing the EBL1 (9H7) and GATN1 lines low. Interrupts may be queued by setting the INTR flip-flop. The Disarm command forces the ARM 1 lead (9H8) low to clear the INTR flip-flops and hold them clear; interrupts are not queued.

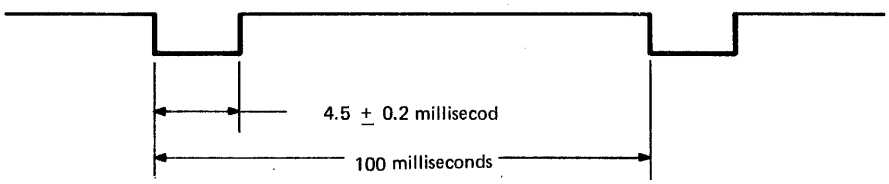
13.8 Initialization

The system initialize signal SCLR0 (15K2) conditions the TTY controller by setting the BLK flip-flop and clearing all other control flip-flops. This presets the controller in the Read mode with interrupts disarmed.

13.9 TTY Timer Adjustment

The only adjustment on the TTY controller controls the frequency of the 440Hz timing multivibrator. The adjustment is made in the following manner:

1. Initialize the system.
2. Connect an oscilloscope to TP-TMG1A (located at the stake near Connector 2).
   Vertical scale: 2 volts/centimeter
   Horizontal scale: 1 milliseconds/centimeter
   Sync: internal, negative
3. Generate a continuous stream of data from the TTY by reading a tape or by the Repeat function of the keyboard.
4. Adjust Potentiometer at location 14R (next to the test point TMG1A) for the waveform shown below.



13.10 Machine Control Register (MCR) (Sheet 7)

A Machine Malfunction (MMF) interrupt is generated when Bit 11, 12, 13, 14, or 15 of the Machine Control Register (MCR) is set (7G4). The MCR bits are assigned and gated (with the SMCR function) as indicated in Table 22.

The CMCR function clears MCR11:15 where there are ONES in B27:31. The system Initialize (SCLR0) clears MCR10:15 -- the straps are not affected. The SMCR function is described in Section 11.2.

13.11 Power Monitor and System Initialize

All circuits for the Power Monitor are on Sheet 15. The master reset signal SCLR0 (15F2) is active when the Initialize Relay K1 (15B9) is de-energized. During normal operating conditions, all voltages are present and the POWDN0 line (15G7) is high. This allows the voltage comparator output to remain high. As long as the voltage comparators output is high, the Initialize Relay K1 remains energized and the SCLR0 line is held high to +5 volts by a resistor (15E2).

If any of the four items listed in Section 10.1 (CL070) occur, the STPF1 line (14J2) goes high and starts the one millisecond EPF timer (14K2). The leading edge of EPF0 (14L2) sets Bit 15 in the MCR (7G2), generating a Machine Malfunction (MMF) interrupt. In response to MMF, the user has an opportunity to do any necessary system resetting and data storage.

TABLE 22. MCR BIT ASSIGNMENT

BIT	MNEMONIC	MEANING	S-BUS	CONDITION CODES
MCR15	EPF	EARLY MF	S31 and	LFC0
MCR14	IRMP	INSTRUCTION PARITY FAIL	S30 and	GFC0
MCR13	DMPFO	DATA PARITY FAIL	S29 and	VFC0
MCR12	APF	AUTO DRIVER PARITY FAIL	S28 and	CFC0
MCR11	STF	STRT TIME OUT FAIL	S27	
MCR10	CATN	CONSOLE ATTENTION	S26	
MCR09	RSTS	REGISTER (STRAP)	S25	
MCR08	SPARE	(STRAP)	S24	
MCR07	SNGLI	DISPLAY CONTROLLER SNGL F-F	S23	
MCR05	BNK B	BANK B (STRAP)	S21	
MCR04	BNK A	BANK A (STRAP)	S20	
MCR06	MCR061	INIT BUTTON IS BEING DEPRESSED	S22	

At the end of the one millisecond EPF delay, the trailing edge of EPF0 (14G5) toggle sets the Primary Power Fail flip-flop (PPF) (14H5) causing the PPF interrupt (14K6) to be sent to the CPU and a low active signal on CL070 (14K6). PPF1 also starts another one millisecond timer XPF (14K5). When the PPF interrupt is detected, the micro-program stores the PSW and register stack in the main memory and sends the POW function to the IOU. The Stop flip-flop (STP) (14N5) is either toggled set by the trailing edge of XPF1 or direct set by FPOW0 (14N4), whichever occurs first. When STP1 goes high, POWDN0 goes low to turn off the transistors of the Darlington circuit and de-energize the Initialize Relay K1. The GSTP1 lead (15J7) is normally high. It is unused except in some multi-CPU systems.

Loss of AC or DC power also de-energizes the relay. POWDN0 goes low when the -15 volt input (N15) (15D8) to the inverter is lost. The Darlington circuit cannot operate the relay if either the +5 volt collector supply (P5) or the +15 volt base supply (P15) (15B6) is missing. Should the AC input (AC1 and AC3) (15B2) be too low or missing, the Power Fail Detector circuit removes the base drive to the Darlington circuit.

If the AC input is lost (or fluctuates enough) the potential at the base of 02BQ3 becomes more negative, 02BQ3 conducts and supplies base drive to 02BQ1. The 4.7K resistor (15K4) provides positive feedback from 02BQ1 to 02BQ3 causing these transistors to turn on. The emitter voltage of 02BQ3 drops, 02BQ4 turns off, 02BQ2 turns on and commences to discharge the delay capacitors (15B6). With 02BQ1 conducting, its collector voltage approaches ground and generates the low active signal PFDT0 (15K4). As described earlier, this starts the sequence which puts a low level on POWDN0 and completes the capacitor discharge. The Darlington circuit has no base drive so the relay is deenergized.

The Initialize Relay K1 is a dry reed unit with Single Pole Double Throw contacts. The normally closed contact of the de-energized relay (K1) provides a metallic ground on the system Initialize line (SCLR0 (15K2).

For a sequence due to POFF, LSU, INIT0, EXA0, or EXB0 low (14A2) clearing STP allows the POWDN0 lead to go high and the delay capacitors (15B6) to charge slowly through the base resistors of Transistor 03AQ1. When the threshold of the Darlington circuit is reached, the circuit conducts and the Initialize Relay K1 is energized thereby removing the ground from the SCLR0 line.

In the case where Initialize is caused by a failure to P5, N15, P15 or the AC supply, the Initialize Relay K1 de-energizes and remains in that state until the fault is corrected.

13.12 Primary Power Fail Check

The Primary Power Fail Detector is located on the IOU board. The circuit is checked and adjusted as follows:

1. Connect the Primary Power Cord of the CPU power supply into a variable voltage source (Variac or equivalent).

2. With the line voltage set at the nominal value of 115.0 VAC, turn the Power on.

3. Adjust Potentiometer at location 00R to generate the Power Fail condition of CL070 (back panel Terminal 122-0) when the AC line voltage is set for 103.5V (i.e., 10% low). System Initialize line (SCLR0) Terminal 105-0 should become low active in less then 2 milliseconds after STPIA (Test Point 110-4) goes active.

4. With nominal line voltage, load the Model 8/32 Test Program and depress the RUN Key. While the program is running, remove the AC line cord from the primary power source.

NOTE:

The TTY will run-open if connected into a different power source.

5. Connect the AC line cord back into the power source. The TTY should stop cycling. Depress the EXEcute switch and the test program should continue to run.

6. Repeat Step 4, but turn the Console Power switch OFF instead of removing the AC line cord.

13.13 Start Timer

The Start Timer circuit is shown at location 15E6. With the timer-kill (KSTM1) (15C7) in its normally low state, the ungated STRT0 signal (15B8) enables the 30 microsecond timer STMA (15E6). When the selected module generates a MFIN0 (15H8) signal, then it clears the timer and disables the timer flip-flop (STMB) (6F8).

The STRT Timer (30 microseconds) is activated whenever the CPU sends the STRT signal to the various system modules (ALU, FAU, IOU, etc.) and is cleared by the MFIN signal from the module addressed by the MSEL (00:02) lines. Should the time out occur before the MFIN signal arrives, one of the two things happen.

1. On non-MUX Bus operations, Bit 11 of the MCR is set, a pseudo MFIN signal restarts the CPU clock, and the MMF interrupt is generated.

2. In the case time out occurs during a MUX Bus operation, the MCR is unchanged, the False Sync code (0100/CVGL) is placed on both Condition Code Busses and a pseudo MFIN restart the CPU clock. If the MUX Bus operation happens to be of the sense type, X'04' is gated to the proper byte as determined by CA311 and the other byte is gated to the S Bus unchanged.

14. S AND D BUS ROM CONTROLLERS

14.1 S Bus High ROM Controller (19-142F45)

000-007	HLLL HLLL LHLH LHLH LLLL LLLL **LLLL LLLL**	19-084R00F78
008-015	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
016-023	HLLL HLLL LHLH LHLH LLLL LLLL LLLL LLLL	19-084R00F78
024-031	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
032-039	LLHL LLHL LLHL LLHL LHLH LHLH LHLH LHLH	19-084R00F78
040-047	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
048-055	LLHL LLHL LLHL LLHL LLLL LLLL LLLL LLLL	19-084R00F78
056-063	LLHH LLHH LLHH LLHH LLLL LLLL LLLL LLLL	19-084R00F78
064-071	HLLL HLLL LHLH LHLH LLLL LLLL LLLL LLLL	19-084R00F78
072-079	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
080-087	HLLL HLLL LHLH LHLH LLLL LLLL LLLL LLLL	19-084R00F78
088-095	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
096-103	LLHL LLHL LLHL LLHL HLLH HLLH LHLH LHLH	19-084R00F78
104-111	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
112-119	LLLL LLLL LLLL LLLL LHLL LHLL LHLL LHLL	19-084R00F78
120-127	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
128-135	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
136-143	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
144-151	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
152-159	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
160-167	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
168-175	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
176-183	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
184-191	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
192-199	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
200-207	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
208-215	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
216-223	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
224-231	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
232-239	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
240-247	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78
248-255	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	19-084R00F78

000-007	LHLL	LHLL	HLLL	HLLL	HLLL	HLLL	HLLL	HLLL	19-084R00F79
008-015	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
016-023	LHLL	LHLL	HLLL	HLLL	HLLL	HLLL	HLLL	HLLL	19-084R00F79
024-031	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
032-039	HLLL	HLLL	HLLL	HLLL	HLLH	HLLH	HLLH	HLLH	19-084R00F79
040-047	LLLL	LLLL	LLLL	LLLL	LHLL	LHLL	LHLL	LHLL	19-084R00F79
048-055	HLLL	HLLL	HLLL	HLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
056-063	LLHH	LLHH	LLHH	LLHH	LLLL	LLLL	LLLL	LLLL	19-084R00F79
064-071	LHLL	LHLL	HLLL	HLLL	HLLL	HLLL	HLLL	HLLL	19-084R00F79
072-079	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
080-087	LHLL	LHLL	HLLL	HLLL	HLLL	HLLL	HLLL	HLLL	19-084R00F79
088-095	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
096-103	HLLL	HLLL	HLLL	HLLL	LHLL	LHLL	HLLH	HLLH	19-084R00F79
104-111	LLLL	LLLL	LLLL	LLLL	LLHL	LLHL	LHLL	LHLL	19-084R00F79
112-119	LLLL	LLLL	LLLL	LLLL	LHLH	LHLH	LHLH	LHLH	19-084R00F79
120-127	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
128-135	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
136-143	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
144-151	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
152-159	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
160-167	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
168-175	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
176-183	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
184-191	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
192-199	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
200-207	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
208-215	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
216-223	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
224-231	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
232-239	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
240-247	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79
248-255	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	19-084R00F79

000-007	HHHH	HHHH	LHHH	HHHH	HHHH	HHHH	**LHHH**	**HHHH**		19-084R00F80
008-015	HHHH	HHHH	LHHH	HHHH	HHHH	HHHH	LHHH	HHHH		19-084R00F80
016-023	HHHH	HHHH	LHHH	HHHH	HHHH	HHHH	LHHH	HHHH		19-084R00F80
024-031	HHHH	HHHH	LHHH	HHHH	HHHH	HHHH	LHHH	HHHH		19-084R00F80
032-039	HHHH	HHHH	LHHH	HHLH	HHHH	HHHH	LHHH	HHLH		19-084R00F80
040-047	HHHH	HHHH	LHHH	HLHL	HHHH	HHHH	LHHH	HLHL		19-084R00F80
048-055	HHHH	HHHH	LHHH	HLHL	HHHH	HHHH	LHHH	HLHL		19-084R00F80
056-063	HHHH	HHHH	LHHH	HLHL	HHHH	HHHH	LHHH	HLHL		19-084R00F80
064-071	HHHH	HHHH	LHHH	HHHH	HHHH	HHHH	LHHH	HHHH		19-084R00F80
072-079	HHHH	HHHH	LHHH	HHHH	HHHH	HHHH	LHHH	HHHH		19-084R00F80
080-087	HHHH	HHHH	LHHH	HHHH	HHHH	HHHH	LHHH	HHHH		19-084R00F80
088-095	HHHH	HHHH	LHHH	HHHH	HHHH	HHHH	LHHH	HHHH		19-084R00F80
096-103	HHHH	HHHH	LHHH	HHLH	HHHH	HHHH	LHHH	HHLH		19-084R00F80
104-111	HHHH	HHHH	LHHH	HLHL	HHHH	HHHH	LHHH	HLHL		19-084R00F80
112-119	HHHH	HHHH	LHHH	HLHL	HHHH	HHHH	LHHH	HLHL		19-084R00F80
120-127	HHHH	HHHH	LHHH	HLHL	HHHH	HHHH	LHHH	HLHL		19-084R00F80
128-135	HHHH	HHHH	LHHH	HHHH	HHHH	HHHH	LHHH	HHHH		19-084R00F80
136-143	HHHH	HHHH	LHHH	HHHH	HHHH	HHHH	LHHH	HHHH		19-084R00F80
144-151	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH		19-084R00F80
152-159	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH		19-084R00F80
160-167	HHHH	HLHH	LHHH	HHLH	HHHH	HHHH	LHHH	HLHL		19-084R00F80
168-175	HHHH	HLHH	LHHH	HHLH	HHHH	HHHH	LHHH	HLHL		19-084R00F80
176-183	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH		19-084R00F80
184-191	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH		19-084R00F80
192-199	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH		19-084R00F80
200-207	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH		19-084R00F80
208-215	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH		19-084R00F80
216-223	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH		19-084R00F80
224-231	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH		19-084R00F80
232-239	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH		19-084R00F80

15. EXTENDER BOARD OPERATION

The following steps must be taken to insure proper Extender Board operation when troubleshooting any of the Processor boards on the Extender Board.

1. Remove the 35-537 CPB (lower Slot 7) to modify the CPU Clock speed. An octal switch is located in IC position 15E for this purpose. Switch positions 4 and 8 are to be ON for Extender Board operation. No other switch positions may be placed in the ON position.

2. Place the 28-015 Extender Board in the chassis slot of the board to be tested. Note that there are two sets of backpanel pins on the Extender Board. Plug the board to be tested into the upper set of pins and plug the Extender Board terminator board (see Step 3) into the lower set of pins.

3. One of two terminator boards must be used for Processor Extender Board operation. The 35-598 Terminator is to be used with the CPA board on the extender, and the 35-599 Terminator is to be used with any of the following: CPB, CPC, ALU, and IOU. The terminator is to be installed as described in Step 2.

4. For Extender Board operation of the CPA, CPB, or CPC, 610 mm (24") extender cables (71-362 and 17-363) are required.

16. MNEMONICS

The following lists provide a brief description of each mnemonic found in the Model 8/32 CPA Schematic Drawing 35-536D08, CPB Schematic Drawing 35-537D08, CPC Schematic Drawing 35-555D08, ALU Schematic Drawing 35-538D08, and IOU Schematic Drawing 35-539. The source of each signal on the respective schematic drawing is also provided.

16.1 CPA Mnemonics, Schematic Drawing 35-536D08

MNEMONICS	MEANING	SCHEMATIC LOCATION
ADA281:311	Add-one-loop outputs	Sheet 3
AEQB1	Segment number equality	6E1
B000:310	B Bus	Sheet 13
BDLY0	Base selection delay	6J5
BIT161A, BIT161B	Bit 16 propagate signal	12N9
BMXNA1	B Mux Enable A – S Bus	12N7
BMXNB1	B Mux Enable B – MDR	12L5
BMXNC1	B Mux Enable C, MLC/CA	12N5
BMXSLA1	B Mux Select Line A – Halfword MDR	12J8
BMXSLB1	B Mux Select B – MLC	12L5
BR040:270	Base Register outputs	Sheet 6
BRWR1	Base Register Write Command	7N7
BSEL001:041	B Bus Source Address	12J4
C001, C010, C011	Carry Commands	Sheet 1
C3X0	Carry past segment boundary	12G8
CA310	Address Bit 31	3B8
CA120:300	Memory Address Bus	Sheet 8
CACLR0	Buffered Clear	1N8
CC0	Second HW Clock	1F9
CD000:310	Memory Data Bus	Sheet 11
CDW0	Write Conversion Command	7M5
CK1A	System Clock	4M3
CLINT0	Clear Interrupt flip flop	7R8
CLOCK0	System Clock	4A1
CMC000:020	Memory Command Bus	Sheet 2
CPC011/001	Increment Commands	2F5
CRDY0	Memory Ready (response)	1A2
CREQ0	Memory Request	1R2
CS000	Control State 0	2G8
CSTA0	Clear Status Register	7R8
DREQ0	Data Request	1R7
FSR0	Status Register flip flop	7G8
GT0/1	Greater Than segment limit	12G7
INCR021	Increment MLC by Two HW	10M7

MNEMONICS	MEANING	SCHEMATIC LOCATION
INCR1	Increment MLC by One HW	10M6
IR1	Instruction Read decode	2K7
IR271:311	Status Register outputs	Sheet 7
IREQ0	Instruction Request	1R5
LDMAR0	Load MAR	2C7
LDMCL0	Load MLC	2B6
LDMDR0	Load MDR	2D8
LDUIR0	Load UIR Clock	4M2
LIME1	Limit violation	6N6
MAI0	Memory Access Interrupt	7R4
MALX120:230	Address Multiplexor outputs	Sheet 8
MAR121:311	Memory Address Register outputs	Sheet 3
MARPU1	Pull up resistor	Sheet 3
MC000:030	Microcontrol field	Sheet 2
MCLK0	Memory Data Clock	4F3
MDR001:311	Memory Data Register outputs	Sheet 4
MDRCL0	Memory Cycle Clock	1B2
MDX001:151	MDR input Multiplexor	Sheet 11
MLC121:311	Memory Location Counter outputs	Sheet 3
MSIG0	Module Signal	10R5
NW1	Write Inhibit	7M2
PROT1	Enable Protect/Relocate	2G4
PSW210	Program Status Word Bit 21	2D4
RGEN0	B Bus Register Enable	12N6
RH0	Read Halfword Command	2F8
RI020	RI2 format	10E3
RQFF0	Request flip flop	1N2
RRSF1	RR or SF format	10D3
RSTR/0	Read Status Register	7R9
RX001	RX format	Sheet 10
RX2F0/1	RX2 flip flop	10K4
RX3D0	RX3 Format decode	10R5
RX3EN1	RX3 decode enable	10K5
RX3F1/0	RX3 flip flop	10K5
RXID0	RX1 decode	10M3
RXIL0	RX3/RI2 format	10M5
S000:150	Part of S Bus	Sheet 5
S160:310	Part of S Bus	Sheet 5
S2B0	S Bus to B Bus Override Command	12G6
SCLR0	System Clear	1J8

MNEMONICS	MEANING	SCHEMATIC LOCATION
SDR1	Data Read Command	2N2
SDRDW1	Data Read/Write Command	2S5
SDW1	Data Write Command	2N2
SEGWEA/B	Base Register HW Write	Sheet 6
SIR1/0	Instruction Read Command	2J6
SMC000:030	Buffered MC field	Sheet 2
SR000:310	S Register outputs	Sheet 5
SR001:311	S Register outputs	Sheet 5
SRCK0	Status Register Clock	7C5
SRTR0	Status Register Trap	7N6
SSEL001:041	S Bus Address Select Bus	2A7
STB0	Strobe	12M2
SM2X121:311	Summer two outputs	Sheet 9
SX280:310	Second Index Register Address	Sheet 11
UDR280:310	User Destination Register Address	Sheet 5
UIR240:310	User Instruction Register	Sheet 5
USR280:310	User Source Register Address	Sheet 5
XPU1	Pull up resistor	6E5

16.2 CPB Mnemonics Schematic Drawing 35-537D08

MNEMONICS	MEANING	SCHEMATIC LOCATION
A140:270	A Bus Bits 14:27	Sheet 5
A280:A310	A Bus Bits 28:31	Sheet 4
AEN0	Enables ASEL Multiplexor	3F5
ASEL001:041	Selects Register containing A Operand	Sheet 3
ATN000:030	Interrupt Attention lines	Sheet 12
AYDS1/0	ASEL Multiplexor select line	3E3
B000:310	B Bus Bits 00:31	Sheet 6
B280:310	B Bus Bits 28:31	Sheet 2
BALA0	Branch and Link, ARM Interrupts	14J9
BDC0	Branch and Disarm Console Interrupt	14J8
BEN0	Enables BSEL multiplexor	3J7
BSEL001:041	Selects Register containing B operand	Sheet 3
BYDS0	BSEL Multiplexor Select line	3K8
C1X071:141	ROM Address: Traps or Op-Code pointers	Sheet 8
C2X101:151	ROM Address: B Bus or ROM Instruction Register indirect field	Sheet 8
CCC0	Carry Condition Code	4D6
CCCLK0	Condition Code Clock loads PSW	4M7
CFLG1	Carry flag	4F6
CLK0	CPU Clock	13N4
CLK1A	CPU Clock	13N4
CLK1B	CPU Clock	13N3
CS000:030	CPU Control States	Sheet 14
CSA041:091	ROM Address	Sheet 9
CSA1/0	Counter State A	14M2
CSA100:150	ROM Address	Sheet 8
CSB1/0	Control State B	14M3
CSD001:311	ROM data	Sheet 11
CSREF0	Denotes control store reference	5N3
CSWRT0	Control Store Write	11G4
D1	Decode Bit	11N6
DREQ0	Data Request	13A3
DSPYL0	Display Interrupt	12A4
E1	Execute Bit	11N5
ENFLG1	Enable PSW flags	11R3
ENPG00:40	Page enable for ROM	Sheet 10
ENSMX0	Enables S Bus multiplexor	7F9
ENYSDX0	Enables YSI/YDI to B Bus	3S5
EXEC1/0	Execute Bit of micro-code	5N1
FLGCLK0	Flag Clock latches Condition Code	4K8

MNEMONICS	MEANING	SCHEMATIC LOCATION
FSEL000:030	Function Select lines	Sheet 11
FYX0	User index enable	3D5
GBIM0	Gate Immediate field to B Bus	6D9
GCC0	Greater Than Condition Code	4D8
GEN0	Generate interrupt	12K4
GFLG1	Greater Than flag	4F8
GPSWA0	Enables PSW selection	3M3
ILEGA	Illegal Instruction	12K1
ILEGB	Illegal Instruction	12K2
ILEGC	Illegal Instruction	12K2
INCLK0	Clock Inhibit	13H1
IREQ0	Instruction Request	13A1
INT1/0	Interrupt present	12N6
JB041:151	Jam address Bits 04:15	Sheet 1
JUTY1	Discriminates between RX1, RX2, or RX3 Instructions	14A1
KLCLK0	Disables CPU clock for manual testing	1R8
KSIG0	Extension of FSEL field	11N5
LCC0	Less Than Condition Code	4D9
LFLG1	Less Than flag	4F9
MAI	Memory Access Controller	12B8
MB041:151	Match Address Bits 04:15	Sheet 1
MC000:030	Memory Control field	Sheet 11
MMF0	Machine Malfunction interrupt	12B5
MNCLK1/0	Manual Clock (P.B. switch)	Sheet 1
MOD000/001	Module zero	5M1
MPEN0	Memory Protect enable	12H9
MSEL000:020	Module Select lines	Sheet 11
MSIG0	Module signal	14A1
MTCH	LED indicator signals address match	1S6
MTCH1	Stored XMATCH1	1M6
PASS1/0	Do not take branch	14K8
PCLK0	CPU Clock	13N3
PPF0	Primary Power Fail	12B6
PRIV	Privileged instruction	12K1
PSW141:271	PSW Bits 14:27	Sheet 5
PSW281:311	PSW Bits 28:31	Sheet 4
PSWCLK1	PSW Clock	4K9
RIR000:310	ROM Instruction Register	Sheet 11
RIR201A	Bit 20; ROM Instruction Register	6D9

MNEMONICS	MEANING	SCHEMATIC LOCATION
RIRCLK0	ROM Instruction Register Clock	11H8
RLC041:151	ROM Location Counter	Sheet 9
RLR041:151	ROM Location Register	Sheet 9
RRXINH0	Inhibits transfer in RRX micro-instructions	14H1
RUN 1/0	Run mode	Sheet 1
RX3D0	RX3 instruction	2H3
S00:310	S Bus Bits 00:31	Sheet 7
S2B1	Gates S Bus data to B Bus	14G4
SAMA1	ROM Address Select line	5R4
SAMBL1	ROM Address Select line	5N5
SAMBM1	ROM Address Select line	5N4
SAMC0	ROM Address Select line	5N2
SCC0	Signals new Condition Code available	4G8
SCLRI/0	System Clear	14A5
SETRLC0	Sets CPU to CS031 as a result of JAM	1M5
SIN0	Single Step Clock switch:normally open contacts	1J8
SINC	Single Step Clock switch:normally closed contacts	1J9
SLMDR1	Select MDR	3E8
SLYDD1	Select YDD	4M2
SPSW1	PSW Select line	4M3
SR280:310	Status Register Bits 28:31	Sheet 4
SRCLK1	Status Register Clock	4H3
SSEL011:041	Destination Register Select lines	Sheet 4
STRT1/0	Module Start Signal	14M5
SX280:310	Second Index field	Sheet 2
SX2NZ1	Secondary Index field is non-zero	3E8
SYNC-TP	Test Point:Match Address	1N6
TEN0	Trap Address enable	12J4
TKILL0	External TP for inhibiting clock	13M1
TRAP121	Interrupt Trap Bit 12	12H8
TRAP130:150	Interrupt Trap Bits 13:15	Sheet 12
UIR240:310	User op-code	Sheet 8
USR280:310	User Source Register Select lines	Sheet 2
VCC0	Overflow Condition Code	4D7
VFLG1	Overflow flag	4F7
XMTCH1	ROM Address compares to Match Address	1H6
XS010:040	Destination Register Address	Sheet 4
YDCLK0	User Destination Register Clock	2E2
YDP1F0	YDP1 enable	3E3

MNEMONICS	MEANING	SCHEMATIC LOCATION
YDX281:311	User Index field	Sheet 2
YS280:310	User Destination Register	Sheet 2
YSIX0	Selects YSI/YDI to B Bus	3S5

16.3 CPC Mnemonics, Schematic Drawing 35-555D08

MNEMONICS	MEANING	SCHEMATIC LOCATION
A000:310	A Bus	Sheet 1
AAD000:040	A Stack Address Bus	Sheet 4
AAD051	A Stack Address Bit 5	Sheet 4
AKL0	A Stack PSW suppress	4G1
ASEL001:041	A Bus Select Bus	Sheet 4
ASTKN0	A Stack enable	4K4
B000:310	B Bus	Sheet 2
BAD000:040	B Stack Address Bus	Sheet 4
BAD051	B Stack Address Bit 5	4L2
BKL0	B Stack PSW suppress	4G2
BSEL001:041	B Bus Select Bus	Sheet 4
BSTKN0	B Stack enable	4K5
M37X0	Floating-Point Module Select	4A1
PSW260	PSW Bit 26	5H6
PSW270	PSW Bit 27	5H7
RWC0	Read/Write Control	5A2
S000:310	S Bus	Sheet 3
S2B0	S Buffer to B Bus Over-ride command	4A4
S37X0	Stored floating point Module Select	4A3
SB001:311	S Buffer outputs	Sheet 3
SODD0	S Bus Odd Register command	5F2
SSEL001:041	S Bus Select Bus	Sheet 4
SSELX0	Stack Load Select	4G4
STWRT1	Start Write command	5A3
WSEL1	Write Select	5K4
WSEL1B	Write Select buffered	5N9
WCLK0	Write Clock	5H5
XCLK0	Buffered Clock	5C4

16.4 ALU Mnemonics, Schematic Drawing 35-538D08

MNEMONICS	MEANING	SCHEMATIC LOCATION
A000:310	A Bus	Sheet 10
ACLK1/0	ALU Clock	Sheet 6
ACLKA/B0	ALU Clock	Sheet 6
ACNT051	Bit 5 of iteration counter	4N4
ACRY1	Carry from iteration counter	4R4
AGL001	Bit 0 A input to shift left multiplexor	8R7
AGL311	Bit 31 A input to shift left multiplexor	8H8
AGR001	Bit 0 A input to shift right multiplexor	Sheet 8
AGR081	Bit 8 A input to shift right multiplexor	Sheet 8
AGR161	Bit 16 A input to shift right multiplexor	Sheet 8
AL001:311	A latch outputs	Sheet 10
ALOG1/0	Logic mode	9M8
ALS080:110	Shift multiplexor outputs Bit 8:11	Sheet 12
AM001:311	A multiplexor outputs	10C5
AMOD001:031	Function select control for ALU	Sheet 9
ARITH1/0	Arithmetic shift	1L6
AS000:030	Arithmetic State	Sheet 5
AS001	Arithmetic State	5F8
ASA1	Arithmetic State register A	5N5
ASB0	Arithmetic State register B	5N5
ASIGN1/0	Stored sign of A Bus operand	3G4
AWC1	Add with Carry instruction	1L2
AXB1	Stored Exclusive-OR of Sign bits of A and B operands	6E3
B000:310	B Bus	Sheet 10
BG001:311	B gate outputs	Sheet 10
BGTR1/0	B Operand is Greater in CAE instruction	6D2
BSIGN1/0	Stored Sign of B Bus operand	6E3
CAE1/0	Floating Point Compare and Equalize instruction	1L1
CCC0	CC Bus – C bit (carry)	2N8
CCCLK0	Condition Code Clock	2E3
270	Carry in Bit 27	
230	Carry in Bit 23	
190	Carry in Bit 19	
CIN 030	Carry in Bit 3	Sheet 9
150	Carry in Bit 15	
110	Carry in Bit 11	
310	Carry in Bit 31	

MNEMONICS	MEANING	SCHEMATIC LOCATION
COUT000	Carry out Bit 0	9H9
COUT080	Carry out Bit 8	9E8
DFLT0	Divide Fault	3E2
DV1/0	Divide instruction (fixed or floating point)	1L7
EA0	Floating Point Add instruction	1F2
EAS1	Floating Point Add6Subtract instruction	1L2
ECOUT0	Exponent carry	8D1
ED1/0	Floating-Point Divide instruction	1L1
EC1	Floating Point Compare instruction	1L3
EM1/0	Floating Point Multiply instruction	1L4
EMD1/0	Floating Point Multiply/Divide instruction	1L4
ES0	Floating Point Subtract instruction	1F2
FAXB1	Stored Exclusive-OR of A and B Sign bits	9N6
FD1/0	Fixed Point Divide instruction	1L8
FM1	Fixed Point Multiply instruction	1L8
FMD1/0	Fixed Point Multiply/Divide instruction	1L8
FSEL000:020	Function Code from CPU	Sheet 1
FSTCNT1/0	First Count of arithmetic state 2	6F8
FXS011	Bit 1, exponent sum	8E6
FXS021:071	Exponent ALU outputs	Sheet 8
G001	Carry generate Bit 0	10F2
G041	Carry generate Bit 4	11F2
G081	Carry generate Bit 8	12F2
G121	Carry generate Bit 12	13F2
G161	Carry generate Bit 16	14F2
G201	Carry generate Bit 20	15F2
G241	Carry generate Bit 24	16F2
G281	Carry generate Bit 28	17F2
GATECC1	Gate Condition Code	3G3
GATEEC1	Gate Floating point Condition Code	3R7
GCC0	CC Bus - G bit (greater than)	2R1
GLOW1	Carry generate Bits 16 to 31	9G3
GNP0 GNM0 GN0	Shift Multiplexor Output control	Sheet 7
GRWC0	Generate Read Write control	6K8
GX0	Shift Multiplexor output control	7H8
GXLSB0	Shift Multiplexor output control	7H8
INHA1	Inhibit A Bus	7E6

MNEMONICS	MEANING	SCHEMATIC LOCATION
INHB0	Inhibit B Bus	7E6
INHX1/0	Inhibit exponent	7H5
KSIG0	Function Code Extension bit from CPU	1A7
LCC0	CC Bus – L bit (less than)	2R1
LOG1	Logical shift	1L5
M1/0	Multiply look-ahead bit	7R6
MD0	Multiply/Divide instruction (fixed or floating point)	1L7
MFIN0	Module Finish signal	2J4
MQ001:311	MQ register outputs	Sheet 10
MQCLK0	MQ register Clock	6R7
MQG001	Bit zero input of MQ Shift register	7S8
MQG311	Bit 31 input of MQ shift register	7S9
MP0	Multiply instruction (fixed or floating point)	1L7
MSEL000:020	Module Select code from CPU	Sheet 1
MSIG0	Module Signal (ALU=carry flag)	2R2
NLRZ0	Normalize	5C4
OCMP1	Control signal (one's complement) for CAE instruction	8E2
OCMPL1	Stored Control Signal – one's complement	6E3
OFL1/0	Exponent Overflow	4E2
P001	Carry propagate Bit 0	10F2
P041	Carry propagate Bit 4	11F2
P081	Carry propagate Bit 8	12F2
P121	Carry propagate Bit 12	13F2
P161	Carry propagate Bit 16	14F2
P201	Carry propagate Bit 20	15F2
P211	Carry propagate Bit 24	16F2
P281	Carry propagate Bit 28	17F2
PLOW1	Carry propagate Bits 16 to 31	9G2
ROT1/0	Rotate shift	1L6
ROTR0	Rotate Right shift	1L5
RWC0	Read Write Control signal to CPU	6M8
RWCA1/0	Read Write Control	6F7
RZR01	Remainder Zero flip flop	7G1
S001:311	ALU sum	Sheet 11
S000:310	Sum Bus	Sheet 10
SAP1/0	Shift multiplexor select control	7H4
SBGTR1/0	Set B Greater flip flop	3H3
SC010:050	Arithmetic Shift Count	Sheet 4
SELA0A/B	A multiplexor select control	8R5
SEP1/0	Shift Multiplexor select control	7E5
SETZA0	Inhibits Bits 0:8 in detection of zero sum (ZSUM1)	1OH2

MNEMONICS	MEANING	SCHEMATIC LOCATION
SGAET0	S Bus enable	7M2
SGCC0	Set Greater than Condition Code	3N7
SGR001	Bit 0 S input to shift right multiplexor	8G9
SHFT1/0	Shift instruction	1L9
SL1	Shift Left control	7N4
SLCC0	Set Less than Condition Code	3N7
SOFL0	Set exponent overflow	8J8
SR1	Shift Right control	7N4
STRT0	Start signal from CPU	1A9
SUFL0	Set exponent underflow	8J8
SUM1/0	Add/Subtract mode	9K4
SVCC0	Set Overflow Condition Code	3L5
SWC0	Subtract with Carry instruction	1L2
TDFLT1	Toggle Divide Fault	6G9
UFL1/0	Exponent Underflow	4G6
VCC0	CC Bus – V bit (overflow)	2R2
XFR0	Forces S=A on ALU function control	9M5
XLOAD0	Load pulse for exponent up/down counters	8G7
XOVF1	CAE Instruction; exponential difference is greater than five	8R4
XRPA/B/C/D	Pullup resister for unused logic inputs on IC's (1k ohm to P5)	7G1
SX011:071	Expojent result (stored)	Sheet 8
XSIGN1	Sign of floating point result	3H6
ZSUM1/0	Sum is zero	10J4

16.5 IOU Mnemonics, Schematic Drawing 35-539D08

MNEMONICS	MEANING	SCHEMATIC LOCATION
A1	Output of address decoder for TTY	9H3
A160:310	A Bus low	Sheet 3
AC1/3	12 VAC inputs to Primary Power Fail Detector	15B2
ACK000:030	Acknowledge interrupt MPX Channel	Sheet 6
ADA1	Address flip-flop for TTY controller	9M3
ADB1	Address flip-flop for Display	9M4
ADRS0	Address Control line, MPX channel	6N4
ADSYNA0	Address SYNC for TTY controller	9L2
ADSYNB0	Address SYNC for Display controller	9L4
ARM1	Interrupt Arm flip-flop for TTY	9J7
ATN0	Interrupt Attention for TTY	12G7
ATSYN0	Attention SYNC pulse for ACK address	12N9
B1	Output of address decoder for Display	9H4
B160:310	B Bus low	Sheet 3
BA1/0	Buffer Active flip-flop (sets when buffer is loaded, cleared when buffer unloaded)	8E8
BLK1/0	Serial feedback block flip-flop	9N6
BR001:071	Buffer Register-eight stages, (active only in Read mode)	Sheet 11
BRK0	Break detect signal status Bit L	8H7
BSY1/0	Busy signal (Status Bit 4)	
CA310	Least Significant Bit of address from CPU (byte steering bit)	1B5
CATN1/0	Console Attention flip-flop	10G5
CCC0	CC Bus - C Bit	7R4
CL070	Primary Power Failure Control line	14K7
CLDR0	Clear line for D Bus receivers	5K5
CLK0/1	Timer clock pulses (11 for character)	12L4
CLRA0	Clear line for cycle counter	5R7
CLRC0	Clear line for timing, flip-flop	5H8
CLRST0	Clear ST flip-flop	12E4
CMCR0	Clear MCR11:15	7C7
CMCR110 CMCR130:150	Clear lines for Machine Control Register	Sheet 7
CMD0	Command Control line, MPX channel	6N4
CMGA0	Command line for TTY controller	10N4
CMGB0	Command line for Display controller	10N5
D000:150	D Bus	Sheet 4
DA0	Data Available Control line, MPX channel	6N4
DAGA0	DA line for TTY controller	10N1

MNEMONICS	MEANING	SCHEMATIC LOCATION
DAGB0	DA line for Display controller	10N9
DBEN1	D Bus Enable	6G4
DCKH1	Clock for D Bus receivers high	6A5
DCKL1	Clock for D Bus receiver low	6B5
DD1/0	Device data signals from Schmidt Trigger receiving circuit	16E7
DFST1/0	Timing Control flip-flop, Detects DSTRT	5E5
DL00:070	Buffered D Bus	Sheet 8
DL00X	Strap to TTY address decoder	9E4
DMPF0	Data Memory Parity Fail (from MBC)	7E4
DR0	Data Request Control line, MPX channel	6H4
DR001:151	D Bus receivers	Sheet 6
DRGA0	DR line for TTY controller	10N2
DRGB0	DR line for Display controller	10N8
DRN1/0	Start Bit stage of Shift Register (controls transmit line in Write mode)	11M6
DSPLY0	Display controller interrupt line to CPU	10J8
DSTRT0	Start D Bus operations	5H9
DSYN1		5D6
DT1/0	Device Transmitting flip-flop (set when RCV loop starts the timer)	11G7
DTMG0	Delayed TMG signal	12C4
DU1	Output of Device Unavailable detector-Active for TTY in DEF/local modes	16J5
DX1	Serial data input to Shift Register (line data in Read mode/all ones in Write mode)	11B2
EBL1	Interrupt Enable flip-flop for TTY	9J6
EOC1/0	End of character (output of character counter)	12N6
ENSHA0 ENSHB0 ENSHC0	Enable signals for S Bus high	Sheet 2
ENSLA0 ENSLB0 ENSLC0	Enable signals for S Bus low	Sheet 3
ENT30	Enter Time period T3	5N2
EPF1/0	Early PPF Timer (1 millisecond)	14L2
ESNC0 ESN00	Complimentary pulsed signals from Display Console	10A5
EX1	Examine bit of TTY status	8J8
EXA0 EXB0	Auxiliary initialize inputs	14A3
FLSYN0	False SYNC signal (D Bus operation)	14K8
FPOW0	Decoded Power Down function	7C7

MNEMONICS	MEANING	SCHEMATIC LOCATION
FSEL 00:03	Function Select lines from CPU	Sheet 1
FSTP0	Stop function-terminates SHFT pulses	12M5
FTX1/0 FTY1/0	Displays controller SYNC generation flip-flops	Sheet 13
FWAIT1/0	Flip-flop for load Wait function	7E8
GACK0	Gate Acknowledge function	6G2
GADRS1	Gate ADRS line	6R3
GCC0	CC Bus - G Bit	7R2
GCMD1	Gate Command	6M3
GDA1	Gate Data Available line	6M3
GDHBH0 GDLBH0 GDLBC0 GDA0	Gating on D Bus signals	Sheet 4
GDIN1	Gate Data In	6K3
GDOUT1	Gate Data Out	6M3
GDR1	Gate Data Request	6H3
GLAB1	Gate LA and LB signals	13G4
GLITCH0	Start Glitch signal - clears TMG1	12B2
GP1/0	Gate POUT function	1K6
GPX0	POUT function finished signal	IN6
GSR1	Gate Status Request	6J3
GSTP1	Gate STP (test point)	15K8
GSTRT1	STRT0 gated with IOU decoded address	IN8
HW1/0	Halfword test line - MPX channel	5J2, 5K2
INCR1/0	Increment/Normal flip-flop	10D2
INIT0	INT key line from Console	14A3
INTR1	TTY interrupt flip-flop	12E8
IRLMP0 (only on Mod. 8/32)	Instruction Read Local Memory Parity Fail (from MBC)	7E3
KA KB	Cycle counter flip-flops	Sheet 5
KC0/1	Timing Control flip-flop, Control line timing	5F3, 5H4
KD1/0	Timing Control flip-flop Control line timing	5M6
KSIG0	Function code line from CPU	1B4
KSYN1/0	Timing Control flip-flop, SYN stretch	5H8
KT1/0	Cycle counter-Terminate flip-flop	5N6
KTM	Test point. Ground to kill Start Timer	14B5
KY	Johnson Counter flip-flops for address cycle	5L8
KX		5M8

MNEMONICS	MEANING	SCHEMATIC LOCATION
LB0	Signals controlling the loading of display registers	13J5
LA0		13J6
LCC0	CC Bus - L Bit	7R2
LDBR0/1	Load Buffer Register pulse (active in Read mode only)	8C7
LDWAIT0	Decoded Load Wait Indicator function	7C8
LESYN1/0	Timing Control flip-flop Detects leading edge of SYNC	5H2
MCR001:091	MCR straps	Sheet 2
MCR110:150	Machine Control Registers	Sheet 7
MFIN0	Module Finish line to CPU	7N8
MMF0	Machine Malfunction interrupt line to CPU	7G6
MSEL000:020	Module Select lines from CPU	1C8
MSIG0	Module Finish line to CPU - Tests the state of HW line	7N9
MSYN1	SYNC from Display or TTY controllers	11D8
MTA0/1	Master TTY Timer (440HZ Output)	12J3
MTB0/1		
MTC1	Timer clock counter (110HZ Output)	12H4
MTD1		
OV1/0	Overflow error flip-flop	8G8
PA0	Pulse output functions (test points)	Sheet 1
PB0		
PC0		
PD0		
PFDT0	Power Fail Detector output	14D3
PF1/0	Primary Power Fail flip-flop	14H5
POFF0	Power Off line from Console switch	14A3
POUT0	Pulse Out function	7C7
PPF0	Primary Power Fail interrupt line	14K6
RACK0	Receive Acknowledge interrupt signal	12F9
RDWDH1	Read-Write Data Halfword	6G4
RN	Negative side of RECEIVE loop	16H8
RP	Positive side of RECEIVE loop	16H6
RST0	Reset line for Display controller	10G3
S160:230	S Bus high	Sheet 2
S240:310	S Bus low	Sheet 3
SCC0	CC Bus - Strobe line	7R6
SCLR0/1	System initialize line MPX channel	15K2
SD001:071	Bi-Directional byte bus to Display Panel	Sheet 8
SELSH0/1	Select signal for S Bus high	2N1

MNEMONICS	MEANING	SCHEMATIC LOCATION
SELSL1	Select signal for S Bus low	3F2
SH10	Signals for sensing Display Console's Switch Register	13J7
SL00		13J8
SHFT1/0	Shift Register pulses, nine per character	12N4
SKT1	Set KT flip-flop	5N3
SMCR0	Sense MCR 00:15	7C7
SMFIN0	B Bus operation finished signal	IL9
SNGL0/1	Single mode flip-flop	10G8
SR0	Status Request Control line, MPX channel	6H4
SR001:071	Shift Register-eight data stages	Sheet 11
SRG0	SR for Display Panel	10N6
SRGA0	SR line for TTY controller	10N3
SRGB0	SR line for Display controller	10N7
SSGL1/0	SNGL key line from Display Console	10A8
ST0	Start idle Timer flip-flop	12E4
STC1	Start gating on S Bus (non-D Bus operation)	2H4
STCLK1	Clock for ST flip-flop	12C3
STD1	Start gating on S Bus (D Bus operation)	2H5
STES1	Set TESYN flip-flop	
STMA0	Start Timer	14F5
STMB0/1	Start Timer flip-flop	14G8
STP1	System Stop flip-flop	14N5
STP1A	Buffered STP1 (test point)	14N5
STPF1/0	Start Power Fail Timer latch	14H3
STPFR0	Start Power Fail routine	14F2
STRT0	Module Start line from CPU	1C7
STT1	Start display controller timer	13E3
SYN0	SYNC test line - MPX channel	5A5
SYN0	SYNC test line MPX channel	11G9
TACK0	Transmit Acknowledge interrupt signal	12N8
TB0	Delay Control line, flip-flop	5B4
TC1/0	Timing Control delay pulses	59B
TDU	Device Unavailable line from TTY	16H4
TERM1	Timing Control flip-flop, Detect trailing edge of SYNC	5E6
THW0	Decoded Test Halfword function	7C7
TMG0/1	Timing gate control flip-flop	12D1
TMGIA	Timing gate test point	12N1
TN	Negative side of SEND loop	16H1
TP	Positive side of SEND loop (TTY)	16H3

MNEMONICS	MEANING	SCHEMATIC LOCATION
TRNS0	Transmit signal to SEND loop	16F1
TX0/1	Display controller timer	13G2
TY0/1		13J3
VCC0	CC Bus - V Bit	7R4
WAIT1	WAIT light control	13J9
WRT1/0	Write mode execute flip-flop for TTY	12D3
WT1/0	Write mode storage flip-flop for TTY	9N7
XA1/0	Flip-flop for gating LA and LB	13F5
XC1/0	Flip-flop for gating SH, SL	13F7
XLC1/0	Line check flip-flop (checks for START glitches and break conditions)	11M7
XPF1/0	Power Fail stop timer	14L5
XRPA	Pull-Up resistor	13F5
XRPB	Pull-up resistor	5L7
XRPD	Pull-up resistor	9M3
XRPE	Pull-up resistor	7E8
XRPF	Pull-Up resistor	7F1

APPENDIX 1. MODULE 3 OPERATIONS

The single precision floating point circuits of the ALU, called the FALU and addressed as Module 3, become active when the FALU recognizes its address on the Control Bus, provided the proper strapping has been supplied through the optional Writable Control Store (WCS). When the FALU becomes active the CPU signals start (STRT), and the function to be implemented is determined from the Control Bus. For FALU functions, the ALU clock is enabled and a hardware sequence is entered to perform the required operation. The shift gates are used to shift the A Bus or the S Bus right or left back into the A latch and on to the A Bus again as determined by the ALU algorithms.

The register stacks of the processor CPU-C board contain 16 32 bit single precision floating point registers (FR0:F).(MSEL000. MSEL011.MSEL021) of the Module Select Bits in the micro-instruction select the FR registers. Table A-1 shows the functions performed by the FALU.

TABLE A-1. MODULE 3 (FLOATING POINT) OPERATION

F FIELD				MODULE 3 (FLOATING POINT)
0	0	0	0	Not used
0	0	0	1	Load
0	0	1	0	Subtract With Carry
0	0	1	1	Add With Carry
0	1	0	0	Not used
0	1	0	1	Compare
0	1	1	0	Not used
0	1	1	1	Not used
1	0	0	0	Subtract
1	0	0	1	Add
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	Compare and Equalize
1	1	0	1	Not used
1	1	1	0	Multiply
1	1	1	1	Divide

When Module 3 is operable, an additional ALU arithmetic state is designated as shown in Figure A-1 (Compare to state diagram, Figure 19).

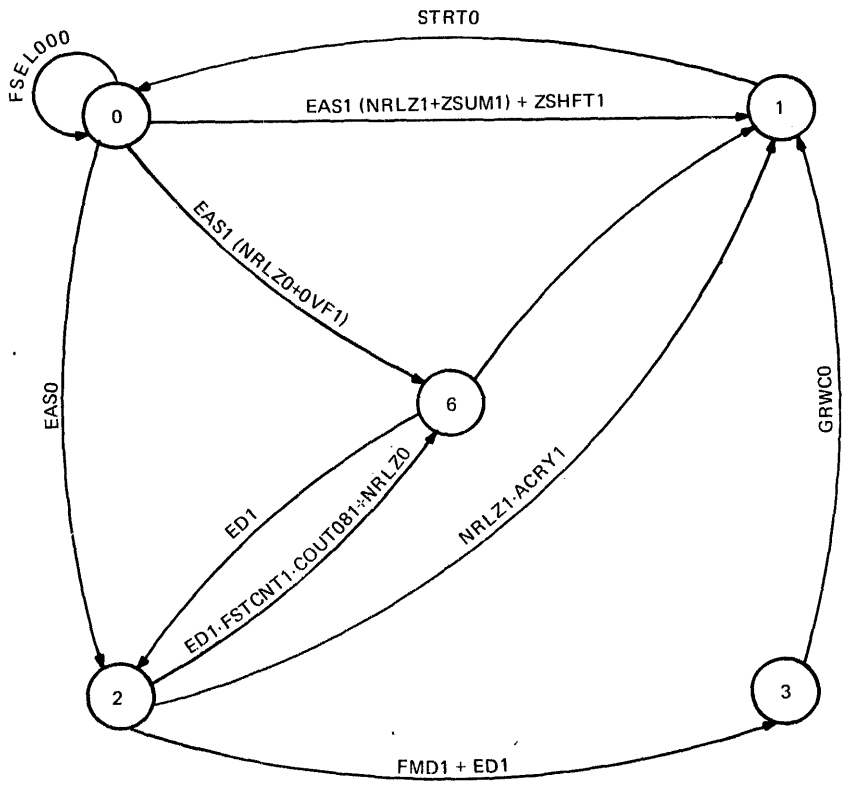


Figure A-1. ALU State Transitions, Including Module 3.

The logic determing the floating point state transitions are listed in Table A-2.

TABLE A-2. STATE REGISTER LOGIC, INCLUDING MODULE 3.

TRANSI-TION	ASA LOGIC	ASB LOGIC	ASC LOGIC	COMMENT
AS001 TO AS011	J = ZSHFT1 + EAS1·COUT080· (NRLZ1 + ZSUM1)			ABORT SHIFT IF SHIFT COUNT IS ZERO. FLT. PT. ADD/SUB. COMPLETE IF NO MANTISSA OVERFLOW AND RESULT IS NORMALIZED OR ZERO.
AS001 TO AS021		J = EAS0·AS001		UNCONDITIONAL TRANSFER IF NOT FLT. PT. ADD/SUB.
AS001 TO AS061		J = EAS1·(COUT081 + NRLZ0·ZSUM0)	J = EAS1·(COU081 + NRLZ0·ZSUM0)	FLT. PT. ADD/SUB. RESULTS IN MANTISSA OVERFLOW OR UN-NORMALIZED MANTISSA
AS021 TO AS011	J = ACRY1·NRLZ1	K = ACRY1·NRLZ1	J = ACRY1·NRLZ0 K = NRLZ1	SHIFT COMPLETE OR FLT. PT. MULT. COMPLETE AND NORMALIZED.
AS0Z1 TO AS031	J = ACRY1·NRLZ1	K = FMD0+ED0		FIX PT. MULT./DIV. COMPLETE. FLT. DIVIDE COMPLETE.
AS021 TO AS061		K = ACRY1·NRLZ1	J = NRLZ0·ACRY1+ ED1·COUT081· FSTCNT1 K = NRLZ1	FLT. MULT. RESULTS IN UN-NORMALIZED MANTISSA. FIRST ITERATION OF FLT. DIVIDE REVEALS DIVIDEND LESS THAN DIVISOR.
AS031 TO AS011		K = GRWC0·AS031		FIX MULT/DIVIDE–FIRST HALF OF RESULT WRITTEN INTO DESTINATION REGISTER. FLT. DIVIDE – MQ TRANSFERRED TO AL.
AS061 TO AS021			J = ED1·FSTCNT1	FLT. DIVIDE – DIVIDEND HAS BEEN MADE SMALLER THAN DIVISOR. CONTINUE DIVIDE.
AS061 TO AS011	J = AS061·NRLZ1		K = NRLZ1	FLT. PT. RESULT HAS BEEN NORMALIZED.
AS011 TO AS001	RESET = STRT1	RESET = STRT1	RESET = STRT1	RESET TO AS001 WHEN CPU REMOVES STRT1.

The floating point simple functions are Load (ELD), Subtract with Carry (ESWC), Add with Carry (EAWC), and Compare (EC). These instructions are floating point instructions only in the sense that they manipulate floating point data. The hardware implementation is identical for that of the fixed point instructions and more of the exponent hardware is used.

Compare and Equalize

The Compare and Equalize instruction is always performed prior to a floating point Add/Subtract. The instruction effectively aligns the exponents of the two operands by shifting the mantissa of the smaller operand.

To simplify the logic for determining the larger operand, B00 is inhibited (forced to a one) during AS001. The difference of the two operands is taken (A-B), and the BGTR flip-flop (6C2) is loaded with the information (SBGTR1) determining the larger operand. The logic for this determination (3D3) is:

$$SBGTR1 = A001 \oplus B001 \oplus S001$$

but since B001 = 1,

$$SBGRT1 = A000 \oplus S001$$

If the BGTR flip-flop is set, B is the larger operand and A is shifted, or if BGTR is reset, A is the larger operand and B is shifted. The exponential difference is computed simultaneously and this result becomes the hexadecimal shift count. However, if this shift count exceeds 5_{10}, the operation is abandoned as significance is shifted out of the mantissa, the result being zero. The four bit magnitude comparator (8J2) compares the exponent difference to 5_{10} and X0VF1 (8N4) determines if the shift count is less than 5_{10}. One additional problem occurs if the exponent of B is greater than the exponent of A. The difference results in a 2's complement number and does not reflect a true shift count. Should this occur, OCMP1 (8D7) is active and complements the difference and inhibits ACNT for one shift cycle in AS021, yielding the correct number of hexadecimal shifts.

During AS021, either the A or B Bus is inhibited (forced to all ones) and a subtraction is performed. The net result is to transfer the operand which is to be shifted into the AL register. Thereafter, the operand is shifted hexadecimally to the right according to the shift count. When the shift is complete (ACRY1), the transition is made to AS011 where the result is gated to the S Bus with the sign and exponent field zero filled. When the Add/Subtract instruction follows, the CPU always gates the larger operand onto the A Bus and the shifted operand to the B Bus.

The algorithm for Floating Point Compare and Equalize:

AS001
- SUM0 → 1
- BG001 → 1
- A△B
- A01:07△B01:07
- FXS05:07 → ACNT05:07
- if X0VF0, AS001 → AS021
- if X0VF1, AS001 → AS011

AS021
- if ACRY1, AS021 → AS011
- if FSTCNT1
  - if OCMPL1, ACNT → ACNT
  - if OCMPL0, ACNT Σ1 → ACNT
  - if BGTR1, A00:31 → AL00:31
  - if BGTR0, B00:31 → AL00:31
- if FSTCNT0
  - ACNT Σ1 → ACNT
  - 0 → AL08:11
  - AL08:27 → AL12:31

AS011
- if X0VF1, 0 → S00:31
- if X0VF0, 0 → S00:07, AL08:31 → S08:31
- MFIN → 1

Floating Point Add/Floating Point Subtract

One additional characteristic of floating point arithmetic beyond that discussed in the Compare and Equalize algorithm arises from floating point notation. The mantissa is represented by sign and magnitude. Positive numbers have a Sign bit equal to zero and negative numbers have a Sign bit equal to one. However, unlike fixed point notation, negative numbers are not represented in 2's complement format. Therefore, when performing an addition with unlike signs, a subtraction must be performed to obtain the true sum. Similarly, when performing a subtraction with unlike signs, to obtain a true difference an addition must be performed. This is accomplished by the FAXB1 address bit to the ALU ROM. The FAXB1 flip-flop (9N6) is set during AS021 of the Compare and Equalize instruction and the logic for this bit is A001 ⊕ B001.

In AS001, the mantissas of A and B are added/subtracted and the exponent of A is presented to the exponent up/down counters. If adding (SUM1), it is possible to overflow the resultant mantissa (COUT081) and a correction cycle is executed in AS061. If subtracting (SUM0), it is possible that the result may not be normalized and a normalize shift is executed in AS061. Should neither of these conditions arise, the transition to AS011 is direct and the result is gated to the CPU.

The algorithm for Floating Point Add is:

```
AS001   if FAXB0, SUM1→1, AΣB
        if FAXB1, SUM0→1, AΔB
        A01:07→XS01:07
        S00:31→AL00:31
        if NRLZ0·ZSUM0 + COUT081·SUM1, AS001→AS061
        if (NRLZ1+ZSUM1)·SUM1·COUTO80, AS001→AS011
AS061   if SUM0{ 0→AL28:31
               { AL12:31→AL08:27
               { XS01:07-1→XS01:07

        if SUM1{ 0→AL08:10
               { 1→AL11
               { AL08:27→AL12:31
               { XS01:1:07+1→XS01:07

        if NRLZ1, AS061→AS011
AS011   if ZSUM1, 0→S00:31
        if ZSUM0{ AL08:31→S08:31
                { XS01:07→S01:07
                { A00→S00
        MFIN→1
```

```
                    if M1   { S07:30→AL08:31
                              (A00 + B00)·ZSUM0→AL00
                              MQ00:30→MQ01:31
                              S31→MQ00

                    if M0   { AL08:30→AL09:31
                              0→AL08
                              MQ00:30→MQ01:31
                              AL31→MQ00

AS061                       AL12:31→AL08:27
                            0→AL28:31
                            (XSΔ1)→XS
                            if NRLZ1, AS061→AS011

AS011               if UFLO { AL08:31→S08:31
                              XS01:07→S01:07
                              A00⊕B00→S00

                    if UFL1, 0→S00:31
                    1→MFIN
```

Floating Point Divide

Floating Point Divide is implemented by continuously subtracting the mantissa of B from the mantissa of the shifted partial remainder (AL) to ascertain which is the larger. If the partial remainder proves to be the larger, the quotient digit (Q31) is set to a one and the left shifted difference is taken as the new partial remainder. If the partial remainder is less than the divisor, the partial remainder is shifted left and the cycle is repeated.

Since the mantissas are true magnitude, the larger mantissa is readily detected by COUT081. However, if significance is shifted out of the n^{th} partial remainder, the n+1 partial remainder is, by definition, larger than the divisor. Therefore, the true logic for the quotient digit is:

$$Q311 = COUT081 + AL071$$

where AL071 detects a one being shifted out of the partial remainder.

The exponent result is obtained by subtracting the divisor exponent (B01:07) from the dividend exponent (A01:07) and the sign bit is derived from A001 ⊕ B001.

On the first divide cycle, if COUT081 is detected, it is necessary to execute a correction cycle to be able to represent the results in 24-bits plus the sign. The mantissa (of the partial remainder) is shifted right one hexadecimal digit and the exponent is incremented. On the next clock, the ALU returns to AS021 and continues the divide iterations.

When the divide has been completed (ACRY1), the ALU goes to AS031, and gates MQ to the AL register and then goes to AS011.

The algorithm for Floating Point Divide is:

```
AS001               SUM0→1
                    A00:31→AL00:31
                    A01:07ΔB01:07→XS01:07
                    7(10)→ACNT
                    AS001→AS021
AS021               if ACRY1, AS021→AS011
                    if FSTCNT1·Q311, AS021→AS061
                    ACNTΣ1→ACNT
                    ALΔB
```

if Q311:
- 1→MQ31
- MQ01:31→MQ00:30
- 0→AL31
- AL01:31→AL00:30

if Q310:
- 0→MQ31
- MQ01:31→MQ00:30
- 0→AL31
- AL01:31→AL00:30

AS061
- XS01:07Σ1→XS01:07
- 0→AL08:10
- AL07→AL11
- AL08:27→AL12:31
- AS061→AS021

AS031
- MQ00:31→AL00:31
- AS031→AS011

AS011
- AL08:31→S08:31
- XS01:07→S01:07
- A00⊕B00→S00
- MFIN→1

Arithmetic Iterative Counter (ACNT01:05)

The iterative shifting of the ALU is controlled by a modulo 32 counter which is enabled during AS021. It is in AS021 that the iterative operations of shift and Multiply/Divide occur and this counter is used to determine completion of the operation and, therefore, the time at which transition to the next arithmetic state should occur. For floating point operations, the counter is used in two different modes as described below.

1. Floating Point Multiply/Divide

For these instructions, the counter is loaded with a count of 7_{10} to allow for seven fewer iterations (the size of the exponent field). For floating point Multiply, when the counter reaches a count of 30_{10} the transition is made from AS021 to AS011 if the result is normalized, or to AS061 if the result is not normalized. For floating point Divide, when the counter reaches a count of 31_{10}, the transition from AS021 to AS031 is made.

2. Compare and Equalize

This instruction is always performed prior to execution of a floating point Add/Subtract instruction. It is used to align the exponents of the two operands by shifting the mantissa of the lesser operand. The smaller operand is shifted right hexadecimally an amount determined by the difference of the two exponents. The shift count, therefore, is loaded from FXS051:071 which is the difference of the exponents. It is possible that this difference may result in a 2's complement number. Should this occur, the 1's complement of this result is loaded into the counter, and the counter is inhibited on the first count of AS021. This is accomplished by the logic at gate 09C03. If this difference should result in a shift count greater than 5_{10}, the operation is aborted since this would result in shifting significance out of the mantissa. Should this occur, a signal called X0VF1 forces a shift count of zero and the operation is aborted. When the shift is complete, the counter reaches a count of 31_{10}, and ACRY1 forces the transition from AS021 to AS011.

Arithmetic Condition Code

The ALU gates appropriate Condition Code flags to the CPU for all ALU functions. When the ALU senses its address and receives a start (STRT) it signals the CPU with SCC0 that a new Condition Code is available. Figure 18 (ALU Functional Block Diagram) shows that the ALU Condition Code circuits consist of combinational logic which determines the resultant condition of each instruction. These are latched in a register. The clock which latches the Condition Code is gated in one of two ways. For the simple functions (FSEL000), the clock results from STRT, delayed an appropriate amount of time to allow the ALU to complete its function. For complex functions (FSEL001), the clock is generated in AS011 at the conclusion of an instruction. The Condition Code is then gated onto the bus through a tri-state multiplexor. The representation of each flag is as follows.

1. VCC0 (Arithmetic Overflow).

The logic for this flag is shown on Sheet 3 (SVCC0). It is enabled for fixed point Add, Subtract, and Divide; and floating point Add, Subtract, Compare and Equalize, Multiply, and Divide. The flag is active for fixed-point Add/Subtract instructions when an overflow is determined by the logic:

$$ASIGN0 \cdot S001 \cdot (BG001 + SUM1) \oplus ASIGN1 \cdot S000 \cdot (BG001 \oplus \overline{SUM1}).$$

The V flag is active for fixed point Divide on the first iteration of the Divide if the quotient bit is determined to be a one. This condition is called a Divide Fault (DFLT) and indicates that the result cannot be contained in 31 bits plus sign. The V flag also sets for fixed point Divide at the end of the divide algorithm if the calculated sign of the quotient is incorrect. For floating point instructions, all mantissa overflow is correctable by shifting the mantissa and adjusting the exponent. Therefore, floating point overflow/underflow is a function of exponent arithmetic alone. The V flag is set for the following conditions:

$$0FL1 = AM011 \cdot (BG011 \oplus \overline{EM1}) \cdot FXS011 \oplus S0FL1$$
$$0FL1 = CAE1 \cdot X0VF1 + AM010 \cdot (BG011 \oplus EM1) \cdot FXS010 \oplus SUFL1$$

2. CCC0 (Carry).

The logic for this flag is shown on Sheet 2. It is enabled for fixed point Add/Subtract, Shifts, and Divide; and floating point Compare, and Compare and Equalize. For fixed point Add/Subtract the logic is SUM1 COUT001+SUM0 COUT000 respectively. For floating point Compare, the logic is essentially, SLCC0, and is used to signal the larger of the two numbers. The C flag is also active for fixed point Divide to signal a divide fault and for floating point Compare and Equalize to signal B as the greater operand (BGTR0). For Shift type instructions, the C flag is the state of the last bit to be shifted. This is selected by the eight to one (8/1) multiplexor whose select control lines are encoded to yield the proper bit for every type shift. The selected bit is then latched by the flip-flop shown at 2E2.

It should also be noted that the Module Signal (MSIG0) from the ALU is identical to CCC0.

3. LCC (Less Than Zero)

The L flag represents the sign of any arithmetic operation. For fullword fixed point operations it is the sign of the result and for halfword shifts it is the sign of Bit 16 (S161). For floating point operations, it is the sign of the floating point result except where exponent underflow occurs or if the floating point result is zero. For these cases the L flag is forced to the inactive state. For floating point compare the logic $[(A001 + B001) \oplus COUT000] \cdot ZSUM0$.

4. GCC0 (Greater Than Zero)

This flag logically represents the occurrence of not less than zero and results not equal to zero and not exponential underflow. This can be logically represented as follows:

$$GCC0 = LCC0 \cdot ZSUM0 \cdot UFL0$$

Arithmetic Elements and ROM Control (Sheets 9:17)

The heart of the ALU is built from the four bit arithmetic/logical elements (Perkin-Elmer Part Number 19-067) and a format ROM used to control them. Also used in conjunction with the ALU chips are a two level carry-look ahead scheme (Perkin-Elmer Part Number 19-068).

The ALU is esentially controlled by 256X4 bit ROM. FSEL001:031 and MSEL011 address the ROM and determine the required control for the given instruction. ASIGN1, BSIGN1, and FAXB1 provide needed additional information to insure correct control for fixed point Multiply/Divide and for floating point Add/Subtract. Shown in Table A-3 is a listing of ALU control for floating point and the respective operations as a function of the address bits. One additional control bit (ALOG1) is required to correctly specify logical operations from arithmetic operations. The logic for this gate (12L2) is:

MSEL010•FSEL000•FSEL011

and essentially decodes the logical operations as per the FSEL field.

There are two levels of gating beyond the ROM outputs on AM0D00:03. These are to provide two basic overide functions. The first is included for the Compare and Equalize instruction. The ROM is coded for a Subtract to obtain the difference of A and B. However, once we determine which is smaller, we wish to load the smaller mantissa into the A latch where it can be shifted. The bus which is not to be shifted is inhibited (forced to all one's) and the transfer into the A latch is accomplished by forcing a carry in and modifying AMOD00:03 to perform an addition. The gate which provides this over-ride to ROM control is located at 9H4.

The second override function provided is to transfer A to S. This is accomplished by XFR0 (12M5). The cases for which this is necessary are as follows.

1. In AS001 for shifts and Multiply/Divide (fixed and float) to transfer operand from the A Bus to the A latch.
2. In AS011 to transfer contents of A latch to the S Bus.
3. In AS031 in fixed point multiply to transfer contents of A latch to the S Bus.
4. In AS031 of divide (fixed and float) to transfer contents of A latch to S Bus under certain conditions (see divide algorithms).

TABLE A-3. ALU ROM CONTROL FOR FLOATING POINT

FAXB1	BSIGN1	ASIGN1	MSEL011	FSEL001	FSEL011	FSEL021	FSEL031	AMOD031	AMOD021	AMOD011	AMOD001	FUNCTION	COMMENTS
X	X	X	1	0	0	0	1	1	0	0	1	SUM1	FLT. PT. LOAD
X	X	X	1	0	0	1	0	0	1	1	0	SUM0	FLT. PT. SUB. WITH CARRY
X	X	X	1	0	0	1	1	1	0	0	1	SUM1	FLT. PT. ADD WITH CARRY
X	X	X	1	0	1	0	1	0	1	1	0	SUM0	COMPARE
0	X	X	1	1	0	0	0	0	1	1	0	SUM0	FLT. PT. SUB. – SIGNS ALIKE
1	X	X	1	1	0	0	0	1	0	0	1	SUM1	FLT. PT. SUB. – SIGNS DIFFER
0	X	X	1	1	0	0	1	1	0	0	1	SUM1	FLT. PT. ADD – SIGNS ALIKE
1	X	X	1	1	0	0	1	0	1	1	0	SUM0	FLT. PT. ADD – SIGNS DIFFER
X	X	X	1	1	1	0	0	0	1	1	0	SUM0	COMPARE AND EQUALIZE
X	X	X	1	1	1	1	0	1	0	0	1	SUM1	FLT. PT. MULTIPLY
X	X	X	1	1	1	1	1	0	1	1	0	SUM0	FLT. PT. DIVIDE

NOTE: SUM1 = SUM, SUM0 = DIFFERENCE

MQ Register

The Multiplier Quotient Register is used exclusively in Multiply/Divide instructions. It is comprised of eight MSI four bit shift registers which are capable of shifting left or right.

Control for the MQ registers is located at 7N4. The A Bus is always loaded into MQ in AS001 by forcing both SR1 and SL1 high. This is accomplished by clearing the Control flip-flop (7K4) with STRT1. For multiply, SR1 is active to perform right shifts and SL1 is inactive. The opposite is true for divide when shifts left are performed.

AL Register and Shift Multiplexors

The AL registers are comprised of eight MSI quad D type flip-flops with double rail output. They are used in all complex functions (FSEL001) as a holding register for shift type operations.

Shifts are performed by enabling one of four multiplexors depending on the type of shift to be performed. The multiplexor outputs are OR-tied together and perform the following types of shifts.

1. n: has S001:311 and MQ001:311 as inputs. Does not shift; used for transferring MQ or A Bus to AL register.

2. n+1: has S011:311 and AL021:311 as inputs. Performs left one shifts for Shift instructions and Divide instructions. End points are determined by AGL001 and AGL311 (Sheet 8).

3. n–1: has S001:301 and AL001:301 as inputs. Performs right one shifts for Shift instructions and Multiply instructions. End points are determined by AGR001 and SGR001 (Sheet 8).

4. n+4: has AL121:311 and AL081:271 as inputs. Shifts left hexadecimally (n+4) to normalize and shift right hexadecimally (n–4) to correct overflow conditions or for Compare and Equalize instruction.

Exponent Arithmetic

Exponential arithmetic is accomplished through the use of two 19-067 4-bit arithmetic/logic elements. The exponent fields (Bits 01:07) of A and B are either added to or subtracted from each other, depending upon the instruction. The result is loaded into an up-down counter, where the exponent may be incremented or decremented as required by post-normalization or overflow correction.

As previously mentioned (Section 3.2.4), in the Compare and Equalize instruction, the exponent difference may result in a 2's complement number and it was necessary to take the 1's complement of this for use as the shift count. This is accomplished by the Exclusive-OR gates connected to the ALU chips and the control signal OCMP1. The 4-bit magnitude comparator is used to determine if the magnitude of the exponent difference is greater than 5_{10}. Should this be the case, the Compare and Equalize instruction is aborted since significance would be shifted out of the mantissa. X0VF1 detects this case.

Perkin-Elmer uses excess 64 notation to express floating point numbers. As a result of an exponent addition or subtraction, the result becomes unbiased (i.e., the excess 64 is lost). To restore excess 64 notation to the exponent field in floating point Multiply/Divide, the most significant bit of the exponent field is complemented. This is accomplished by the Exclusive-OR gate whose logic is FXS011 $\oplus$ EMD1.

2 K B

WRITABLE CONTROL STORE

35-555F01A20
September 1975

METRIC

MODEL 8/32
WRITABLE CONTROL STORE
INSTALLATION SPECIFICATION

INTRODUCTION

The Writable Control Store (WCS) is an option which extends the flexibility of the user level Processor to that of the micro-machine. The WCS has the capability of storing and retrieving data within the control store, plus the capability of dynamically altering control store instructions. In effect, the micro-programmer has the full capability of the user level machine at micro-processor speeds.

The WCS offers 2KB of control store, sufficient to contain 512 instructions or some combination of instructions and data. It is contained on the 8/32 CPC Processor board and requires typically 7 Amperes of 5VDC for power.

This specification provides the necessary information for the installation of the 8/32 Writable Control Store (WCS) option.

PHYSICAL CHARACTERISTICS (35-555 Board also includes 8/32 CPC)

Dimensions – Board 381 mm x 381 mm (15" x 15")

Weight – 2.72 kilograms (16 pounds) approximately.

Power – 5VDC at 10 Amperes maximum

Hardware

- one additional power supply regardless of expansion.
- one 35-555F01 Board
- one 17-360 front edge ribbon cable
- one illegal instruction ROM on 8/32 CPB ROM.

UNPACKING

When the WCS option is shipped with a system, it is installed at the factory. All cables and printed circuit boards should be inspected to ensure proper seating.

INSTALLATION

Chassis

Slot 6 of the Basic Processor lower chassis is used for the 8/32 WCS option. The WCS is mounted on the 35-555F01 board (the 8/32 Processor CPC board).

Power

An additional power supply, regardless of configuration, has to be used to provide an extra 5VDC (P5) source for WCS. See Figure 1.

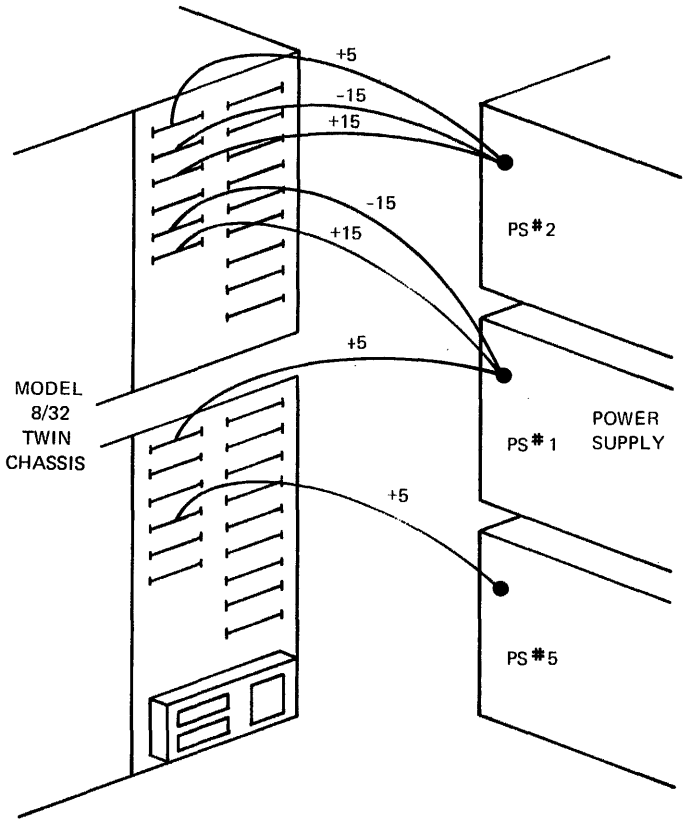


Figure 1. 8/32 Processor With WCS and/or DFU Power Wiring

Cabling

The 17-360 cable connects Connector 4 on the CPB and CPC Processor boards.

Strapping

Refer to the Writable Control Store Maintenance Specification, 35-555F01A21 for strapping details.

Testing

Upon completion of the installation, and before power is applied, all voltages should be checked for shorts between each other and ground. Proper operation of the WCS is tested by the execution of the WCS Test Progra,.. 06-192.

Other

Illegal instruction ROM, 19-084F43, on the 8/32 CPB board (35-537) at Location 00C must be replaced by 19-084F48.

2K WRITABLE CONTROL STORE

8KB

35-555F01R01A21
January 1978

METRIC

WRITABLE CONTROL STORE MAINTENANCE SPECIFICATION

2 kB

INTRODUCTION

The Writable Control Store (WCS) is an option which extends the flexibility of the user level Processor to that of the micro-machine. The WCS has the capability of storing and retrieving data within the control store, plus the capability of dynamically altering control store instructions. In effect, the micro-programmer has the full capability of the user level machine at micro-processor speeds.

The WCS offers 2KB of control store, sufficient to contain 512 instructions or some combination of instructions and data. It is contained on the unused half of the 8/32 CPC Processor board and requires typically 7 Amperes of 5VDC for power.

This specification describes the functional operation of the Model 8/32 Writable Control Store and provides information necessary for its maintenance. This specification references CPC Functional Schematic 35-555D08. Perkin-Elmer schematic title, drawing number, and sheet number are located in the lower right corner of each sheet. Each sheet is zoned alphabetically across the top and bottom margins and numerically down the side margins. These schematics are referenced throughout the block diagram and functional analysis text to correlate specific locations on the schematics to the text. When a specific location is referenced by the text, a number-letter-number is used to designate schematic sheet number, and zone location within the sheet. For example, schematic reference (3B5) is found on Sheet 3, at the intersection of Zone B and 5.

BLOCK DIAGRAM ANALYSIS

Data is stored in a 512 x 32 bit array subdivided into two pages, i.e., A and B. Each page stores 256 fullwords of data. Each page is further delineated as a high half which stores Data Bits CSD001:151, and a low half which stores Data Bits CSD161:311. Data to be written into the Writable Control Store is derived from the backpanel A Bus, buffered, and fanned out to Pages A and B. See Figure 1.

The address to be read (or written) is derived from the Control Store Address lines (CSA) 04:15 originating on the 8/32 CPB board. The four most significant address lines (CSA 04:07) are strapped to enable a selectable address range for the WCS. The eight least significant address lines are buffered directly as A0:A7, and select one out of 256 addresses within each page.

FUNCTIONAL SCHEMATIC ANALYSIS

Storage Device

The basic storage element used in the WCS is the 19-077 static bi-polar Random Access Memory (RAM) employing tri-state output, organized 256 words by one bit. It is intended for high speed memory applications where low input loading on chip address decoding, and high capacitive drive capability are required. See Table 1.

The three state output has the characteristic TTL totem pole output with active elements driving both the ONE and ZERO output voltage levels, plus the capability to disable both driving elements to a high impedence state when the device is not selected. The data output can then be tied to a common output bus which can be driven by only one active output or a passive pull-up.

The memory device (19-077) is addressed with the A0-A7 inputs which select one of 256 words. The chip is enabled by making all Memory Enables, Pins 3, 4, and 5 low. If any of the Memory Enables are high, the chip is in the high impedence state. If the Write Enable Pin 12 is high and the chip is enabled, the stored data (complement of data applied at input during write cycle) is read on the output pin. If the Write Enable Pin 12 is low and the chip is enabled, the data on the input pin is written into the addressed word.

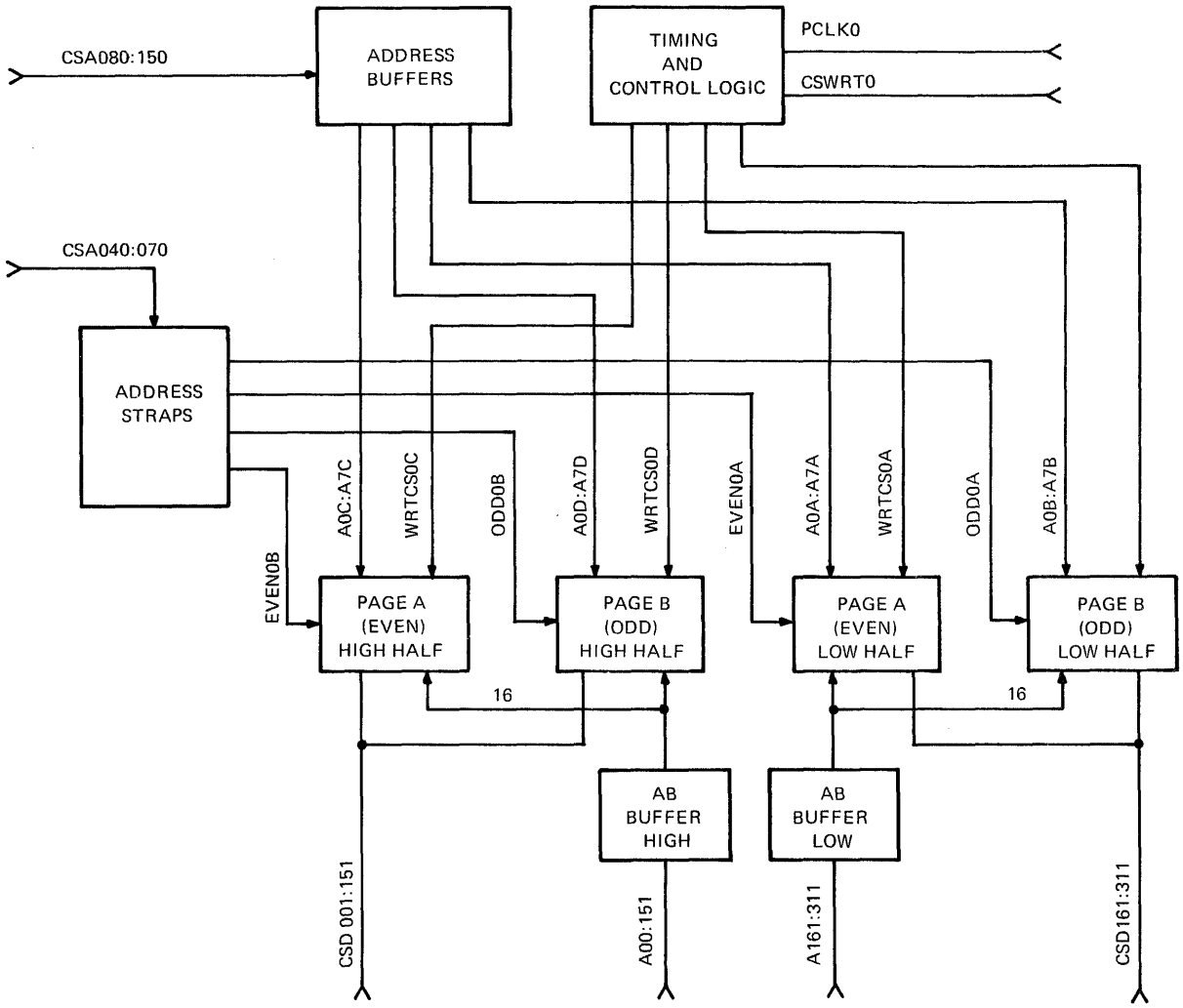


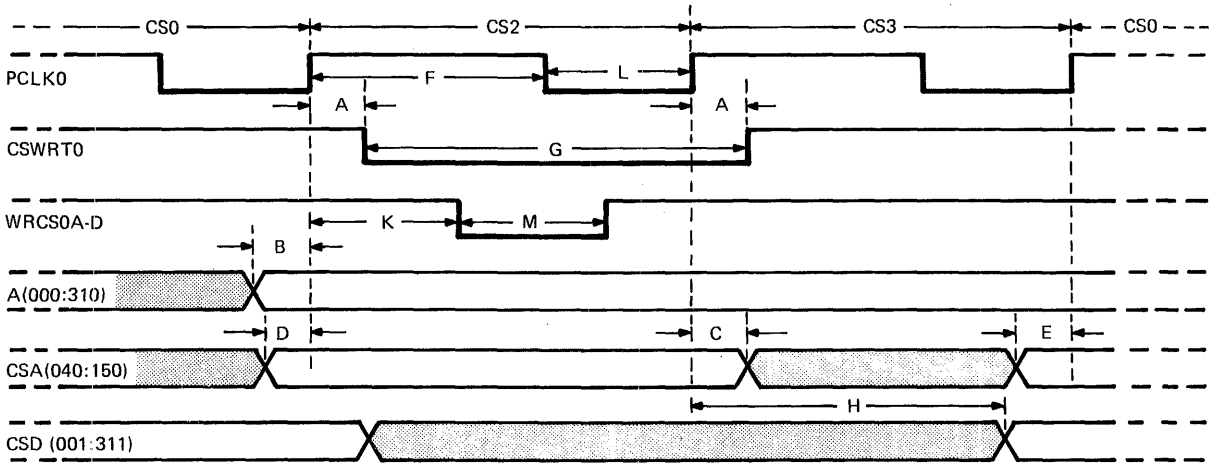
Figure 1. 8/32 WCS Block Diagram

TABLE 1. 19-077 MEMORY DEVICE TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
ALL LOW	LOW	WRITE	UNDEFINED
ALL LOW	HIGH	READ	COMPLIMENT OF WRITTEN DATA
ONE OR MORE HIGH	DON'T CARE	HOLD	HIGH IMPEDENCE STATE

Writing into WCS

Refer to Figure 2, Timing Diagram. During Control Store Write operation, the Processor traverses Processor Control States 0, 2, and 3. The Write instruction is decoded in Control State 0. The CPB deposits the WCS address on CSA 04:15 lines at least 10 nanoseconds before Control State 2 is entered. The CSA 070 determines which page is written into by activating either ODD0 or EVEN0 chip enable lines.



	MAX in ns	MIN in ns
A	24	8
B	/	10
C	58	8
D	/	10
E	/	10
F	/	95

	MAX in ns	MIN in ns
G	/	115
H	90	0
K	70	58
L	/	40
M	/	50

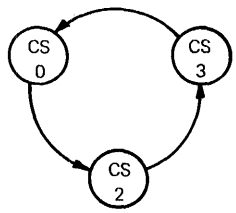


Figure 2. Control Store Write Operations

The CSA 04:06 are factory strapped to inhibit the chip enable lines for any address outside the X'800'–'9FF' range. The CSA 08:15 are buffered directly as A0:A7, and select one out of 256 addresses within each page. The CPB holds address lines static at least 10 nanoseconds after Control State 2 to 3 transition. The data to be written into WCS is deposited on the backpanel A Bus at least 10 nanoseconds before CS0→CS2 transition.

This data is buffered on the WCS board and applied simultaneously to both pages of the WCS. Data is held static throughout the CS2 state.

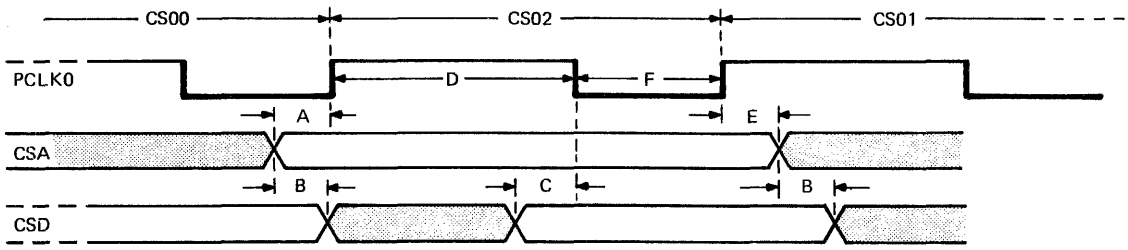
Writing of one 32-bit word is accomplished in Control State 2. Write operation is distinguished from a Read operation by CSWRT going active. This signal is used to derive Write enable pulses WRCS0A-D. The width of WRCS0 is guaranteed to be 50 nanoseconds minimum.

The 40 nanosecond delayed Processor Clock (PCLK0) is used to build the leading edge of WRCS0. This ensures that the switching noise on the leading edge of CSWRT signal is screened off. The trailing edge of WRCS0 is generated by the DPCLK0A signal (Processor Clock Delayed 20 nanoseconds).

Since PCLK0 is high (inactive) for 85 nanoseconds minimum, the width of WRCS0 is guaranteed to be 50 nanoseconds minimum. The DPCLK0A input also ensures that a sufficient data and address hold time is allowed after the trailing edge of WRCS0.

Control Store Read

Refer to Figure 3.



NOTE: CSWRT0 WILL STAY HIGH THRUOUT THE ENTIRE CS READ OPERATION

A = 10 ns MAX D = 95 ns MIN

B = 10 ns MIN E = 10 ns MIN

C = 10 ns MIN F = 40 ns MIN

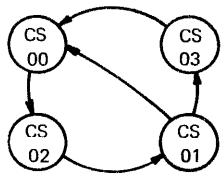


Figure 3. CPU/WCS Interface Timing Control Store Read Operations

The Read instruction is decoded in Control State 0. The CPB gates the address on the busses prior to entering Control State 2 as described in the section on writing into WCS. The CSWRT0 is held high throughout the Read instruction. During CS2, WCS deposits one 32-bit word on Control State Data bus (CSD) 001:311. The data on the bus must be settled at least 10 nanoseconds before the negative going edge of PCLK0 (see parameter C in Figure 3) which latches the data read from the WCS in the Processor Register Stacks.

WCS Strapping

Address strapping.

The 8/32 WCS responds to the Control Store addresses within the X'800-9FF' range.

NOTE

Strapping Address X'800 - 9FF' 21-25, 22-28,
23-30, 24-31, 46-25, 45-28, 44-30, 43-32.

ROUTINE MAINTENANCE

Routine maintenance consists of running the WCS Test Program 06-192.

35-663R01A20
June 1978

METRIC

MODEL 8/32
2K WRITABLE CONTROL STORE
INSTALLATION SPECIFICATION

INTRODUCTION

The Writable Control Store (WCS) option extends the flexibility of the user level processor to that of the micro-machine. The WCS has the capability of storing and retrieving data within the control store, plus the capability of dynamically altering control store instructions. In effect, the micro-programmer has the full capability of the user level machine at micro-processor speeds.

The WCS offers 8KB of control store, sufficient to contain 2048 instructions or some combination of instructions and data. It is contained on the 8/32 CPC Processor board and requires typically 10 Amperes of 5VDC for power.

This specification provides the necessary information for the installation of the 8/32 Writable Control Store (WCS) option.

PHYSICAL CHARACTERISTICS (35-663 Board also includes 8/32 CPC)

Dimensions - Board 381 mm x 381 mm (15" x 15")

Weight 2.72 kilograms (6 pounds) approximately

Power - 5VDC at 15 Amperes maximum

Hardware

- one additional power supply regardless of expansion.
- one 35-663F00 board
- one 17-360F01 front edge ribbon cable
- one illegal instruction ROM on 8/32 CPB ROM.

UNPACKING

When the WCS option is shipped with a system, it is installed at the factory. All cables and printed circuit boards should be inspected to ensure proper seating.

INSTALLATION

Chassis

Slot 6 of the lower chassis on a 356 mm (14") Basic Processor Twin Chassis is used for the 8/32 WCS option. The WCS is mounted on the 35-633F00 board (the 8/32 Processor CPC board).

Power

An additional power supply, regardless of configuration, has to be used to provide an extra 5VDC (P5) source for WCS. See Figure 1.

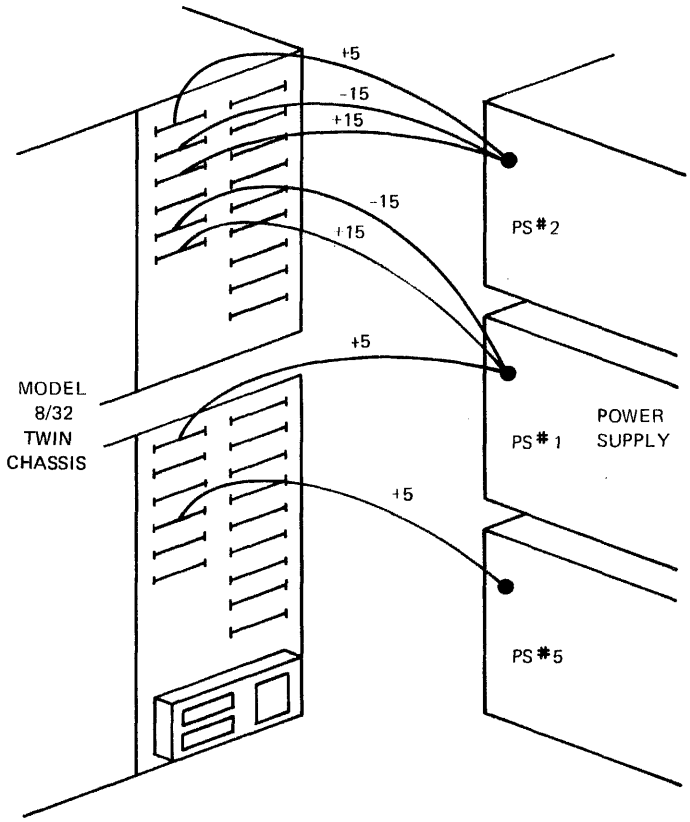


Figure 1. 8/32 Processor with WCS and/or DFU Power Wiring

Cabling

- The 17-360F01 cable connects Connector 4 on the CPB and CPC Processor boards.

Testing

Upon completion of the installation, and before power is applied, all voltages should be checked for shorts between each other and ground. Proper operation of the WCS is tested by the execution of the WCS Test Program, 06-192.

Other

- Illegal instruction ROM, 19-195F13, on the 8/32 CPB board (35-537F01) at location 00C must be replaced by 19-195F14.

35-663A21
October 1977

METRIC

MODEL 8/32
2K WRITABLE CONTROL STORE MAINTENANCE SPECIFICATION

INTRODUCTION

The Writable Control Store (WCS) is an option which extends the flexibility of the user level processor to that of the micro-machine. The WCS has the capability of storing and retrieving data within the control store, plus the capability of dynamically altering control store instructions. In effect, the micro-programmer has the full capability of the user level machine at micro-processor speeds.

The WCS offers 8KB of control store, sufficient to contain 2048 instructions or some combination of instructions and data. It is contained on the unused half of the 8/32 CPC Processor board and requires typically 10 Amperes of 5VDC for power.

This specification describes the functional operation of the Model 8/32 Writable Control Store and provides information necessary for its maintenance. This specification references CPC Functional Schematic 35-663D08. Perkin-Elmer schematic title, drawing number, and sheet number are located in the lower right corner of each sheet. Each sheet is zoned alphabetically across the top and bottom margins and numerically down the side margins. These schematics are referenced throughout the block diagram and functional analysis text to correlate specific locations on the schematics to the text. When a specific location is referenced by the text, a number-letter-number is used to designate schematic sheet number, and zone location within the sheet. For example, schematic reference (3B5) is found on Sheet 3, at the intersection of Zone B and 5.

BLOCK DIAGRAM ANALYSIS

Data is stored in a 2048 x 32 bit array subdivided into two pages, i.e., A and B. Each page stores 1024 fullwords of data. Each page is further delineated as a high half which stores Data Bits CSD001:151, and a low half which stores Data Bits CSD161:311. Data to be written into the Writable Control Store is derived from the backpanel A Bus, buffered, and fanned out to Pages A and B. See Figure 1.

The address to be read (or written) is derived from the Control Store Address (CSA) lines 04:15 originating on the 8/32 CPB board.

FUNCTIONAL SCHEMATIC ANALYSIS

Storage Device

The basic storage element used in the WCS is the 19-218 static bi-polar Random Access Memory (RAM) employing tri-state output, organized 1024 words by one bit. It is intended for high speed memory applications where low input loading on chip address decoding, and high capacitive drive capability are required. See Table 1.

The three state output has the characteristic TTL totem pole output with active elements driving both the ONE and ZERO output voltage levels, plus the capability to disable both driving elements to a high impedence state when the device is not selected. The data output can them be tied to a common output bus which can be driven by only one active output or a passive pull-up.

The memory device (19-218) is addressed with the A0-A9 inputs which select one of 1024 words. The chip is enabled by making the Memory Enable Pin 1 low. If the Memory Enable is high, the chip is in the high impedence state. If the Write Enable, Pin 14, is high and the chip is enabled, the stored data is read on the output pin. If the Write Enable, Pin 14, is low and the chip is enabled, the date on the input pin is written into the addressed word.

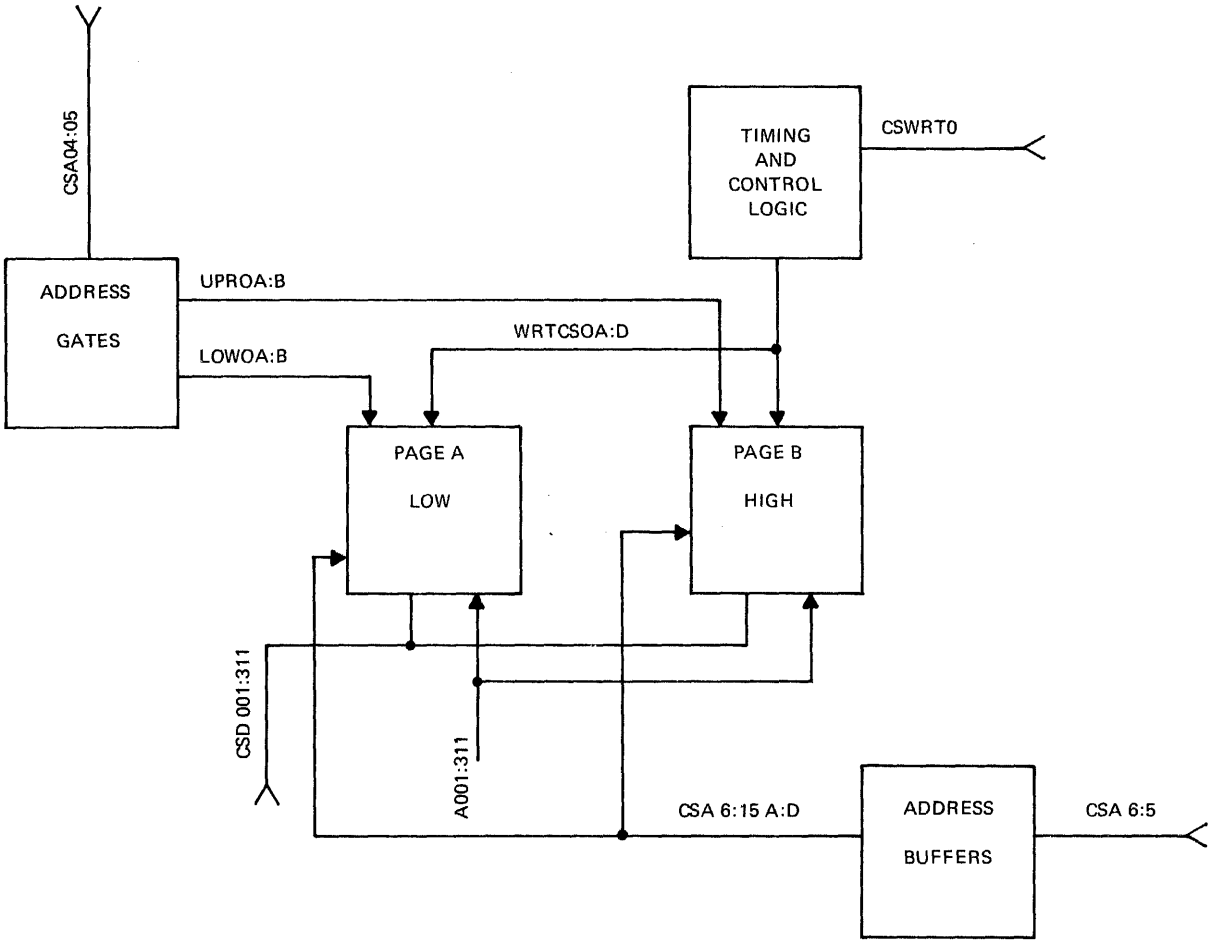


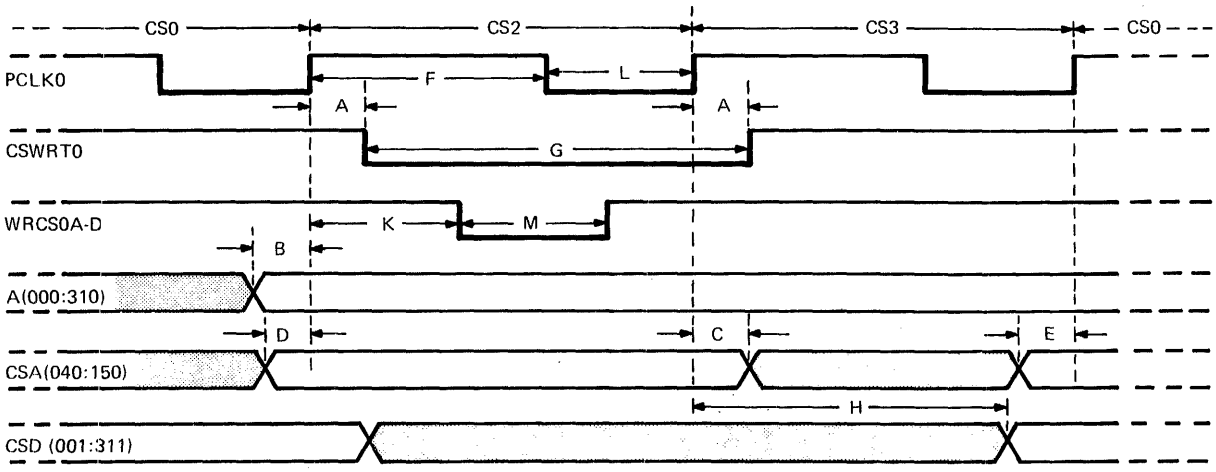
Figure 1. 8/32 WCS Block Diagram

TABLE 1. 19-218 MEMORY DEVICE TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
LOW	LOW	WRITE	UNDEFINED
LOW	HIGH	READ	WRITTEN DATA

Writing into WCS

Refer to Figure 2, Timing Diagram. During Control Store Write operation, the processor traverses Processor Control States 0, 2, and 3. The Write instruction is decoded in Control State 0. The CPB deposits the WCS address on CSA lines 04:15 at least 10 nanoseconds before Control State 2 is entered.



	MAX in ns	MIN in ns
A	24	8
B	/	10
C	58	8
D	/	10
E	/	10
F	/	85

	MAX in ns	MIN in ns
G	/	105
H	90	0
K	70	58
L	/	40
M	/	50

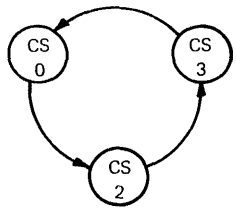


Figure 2. Control Store Write Operations

The WCS is inhibited for any address outside the X'800' - 'FFF' range. The CSA 06:15 are buffered directly as A0:A9, and select one of 1024 addresses within each page. The CPB holds address lines static at least 10 nanoseconds after Control State 2 to 3 transition. The data to be written into WCS is deposited on the backpanel A Bus at least 10 nanoseconds before CS0 CS2 transition.

This data is buffered on the WCS board and applied simultaneously to both pages of the WCS. Data is held static throughout the CS2 state.

Writing of one 32-bit word is accomplished in Control State 2. Write operation is distinguished from a Read operation by CSWRT going active. This signal is used to derive Write enable pulses WRCS0 A-D. The width of WRCS0 is guaranteed to be 50 nanoseconds minimum.

Since PCLK0 is high (inactive) for 85 nanoseconds minimum, the width of WRCS0 is guaranteed to be 50 nanoseconds minimum.

Control Store Read

Refer to Figure 3.

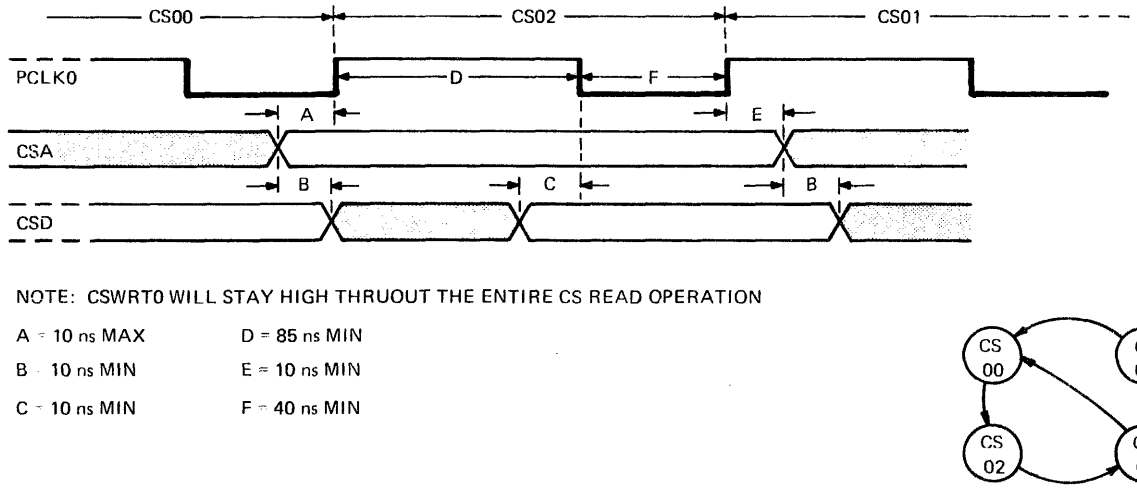


Figure 3. CPU/WCS Interface Timing Control Store Read Operations

The Read instruction is decoded in Control Store 0. The CPB gates the address on the busses prior to entering Control State 2 as described in the section on writing into WCS. The CSWRT0 is held high throughout the Read instruction. During CS2, WCS deposits one 32-bit word on Control State Data (CSD) bus 001:311. The data on the bus must be settled at least 10 nanoseconds before the negative going edge of PCLK0 (see parameter C in Figure 3), which latches the data read from the WCS in the Processor Register Stacks.

WCS Strapping

Address:

The 8/32 2K WCS responds to the control Store addresses within the X'800' - 'FFF'range.

ROUTINE MAINTENANCE

Routine maintenance consists of running the WCS Test Program 06-192.

MEMORY

METRIC

MODEL 8/32 MAIN MEMORY SYSTEM MAINTENANCE SPECIFICATION

1. INTRODUCTION

This specification applies to the Perkin-Elmer Model 8/32 Main Memory System components listed in Table 1.

TABLE 1. MODEL 8/32 MAIN MEMORY COMPONENTS

BOARD PART NO.	MNEMONIC	FUNCTION
35-534	LMI	LOCAL MEMORY INTERFACE
35-535	MBC	MEMORY BUS CONTROLLER

2. SCOPE

This specification describes the overall operation of the Model 8/32 Main Memory System consisting of one MBC and two LMI boards used in conjunction with the 32-206(02-409) 32 KB Memory Module or the 32-209(02-483) 750 ns 64 KB Memory Module. The Main Memory System interconnection to the CPA Bus and the Extended Direct Memory Access (EDMA) port are covered by this specification. The specification also provides a block diagram description, timing information, troubleshooting and maintenance, and a mnemonic list for the MBC and LMI.

3. SYSTEM BLOCK DIAGRAM

The basic organization of the Main Memory System is shown in Figure 1. Access to the memory system is made through two ports: The CPU port which interfaces with the CPA board, and the EDMA port which interfaces with the Extended Direct Memory Access Bus.

The Memory Bus Controller (MBC) board controls the two ports into the local memory and provides a third data path which enables the CPA to directly access remote memory located on the EDMA Bus. The MBC also maintains a cache memory of eight halfwords which is used to store instructions in a look-ahead fashion, and is equipped with circuits to resolve contention between the CPU port, EDMA port, and look-ahead cache for access to Local Memory. The MBC maintains the control logic for the EDMA Bus (QUE0, RPC0/TPC0, and SOT0 as described in Section 7).

The Local Memory Interface (LMI) board provides all signals necessary to control the Local Memory Modules (LMMs) and steers halfword data to the appropriate Memory Module bank for halfword operations. In addition, the LMI generates and checks parity, on systems so equipped.

3.1 Memory System Organization

The Model 8/32 Memory System is organized into a pyramid structure which places four Memory Module banks in parallel (see Figure 1). Note that each LMI controls two banks of Memory Modules, each 16 bits wide, which are accessed simultaneously to give a 32 bit wide fullword of data on each memory access cycle of an LMI. The MBC is connected via the 32-bit Local Memory Bus to two LMI boards, each of which controls half of the available memory.

The addressing structure of the memory system is such that the two halves of memory controlled by separate LMI boards are interleaved; i.e., successive fullwords are controlled by alternate LMIs. Looking at the address format (Figure 2), only 19 of 20 address bits are used by the memory system. Bit 17, the fullword bit, determines which of the two LMIs controls the requested address; Bit 18, the halfword bit, determines which of the two banks controlled by the LMI contains the requested halfword (used only for halfword operations). These bits are used only within each LMI to select the appropriate memory bank and Bits 0:16 are then sent to the memory bank to address the desired location within the selected bank. Thus, addresses in which Bits 17 and 18 are both zero, are found in the bank with interleaving address 00 (Figure 1), and similarly for the other three combinations of the two least significant bits.

The two important features of the Main Memory System organization are: 1. Fullword data paths, providing true fullword access capability; 2. Fullword interleaving, reducing the effective memory cycle time for accesses to subsequent fullword addresses.

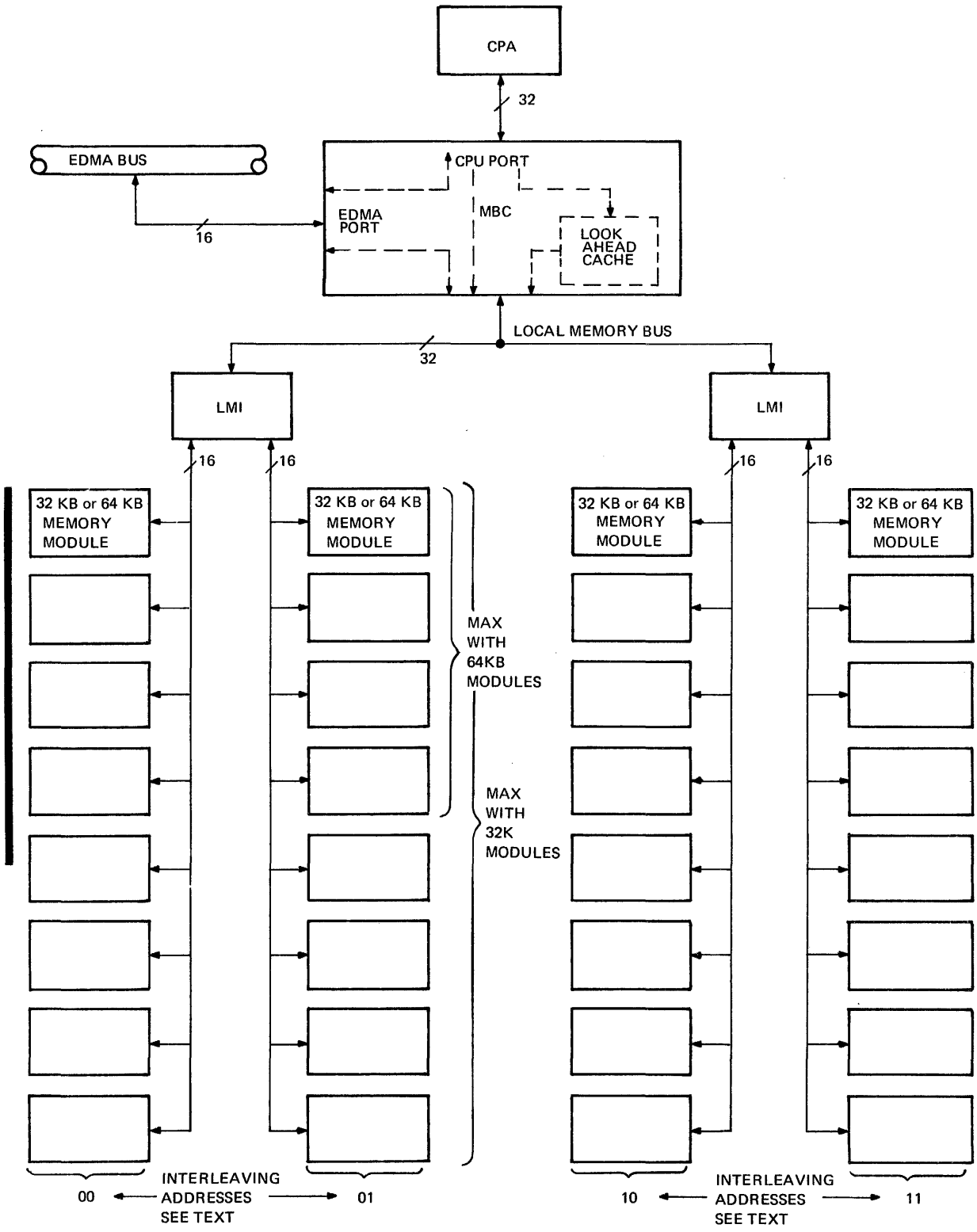


Figure 1. Model 8/32 Main Memory System Block Diagram

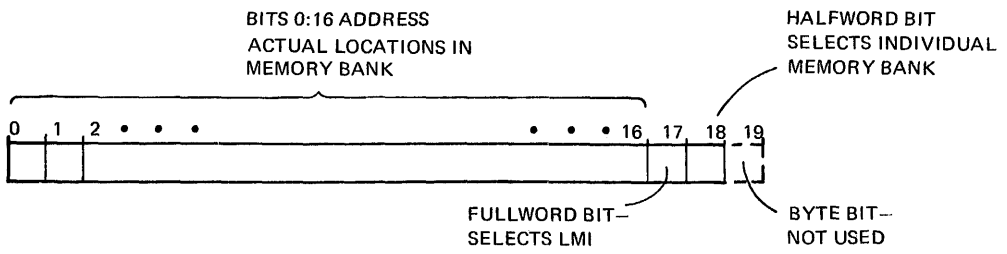


Figure 2. Address Format

4. MEMORY SYSTEM PHYSICAL DESCRIPTION AND INTERCONNECTION

The basic configuration for the Main Memory System consists of one MBC, two LMI boards, and four 32-206(02-409) 32KB or 32-209(02-483) 64KB 750 nanosecond cycle time Core Memory Modules with or without parity. These are arranged as shown in Figure 3. Expansion of memory capacity beyond the basic 128 KB with 32 KB memory modules or 256 KB with 64 KB modules respectively requires that Local Memory Modules in the basic chassis be removed and all Memory Modules be located in the Memory Expansion chassis with interconnection via back panel cables. Refer to the 8/32 Customer Installation Manual, 29-537, for details of memory expansion.

4.1 Memory Bus Controller

The MBC consists of one Perkin-Elmer standard size board which occupies upper chassis Slot 1. The MBC plugs into back panel Connectors 0 and 1 for power, ground, and CPU, EDMA and LMB interfaces. A backpanel waterfall cable from Connector 1 of the MBC slot to Connector 1 of the lower card file Slot 2 provides the interconnection of the EDMA Bus interface to the I/O slots.

4.2 Local Memory Interface, 8/32 and 8/32C

Each LMI board is one Perkin-Elmer standard size board which occupies upper chassis Slots 3 and 6. The LMI boards should not be interchanged, as each board is strapped differently. The LMI plugs into Connectors 0 and 1 for power, ground, and LMB and LMM interfaces.

4.3 Local Memory Interface, 8/32D

Each LMI board is one Perkin-Elmer standard size board which occupies upper chassis Slots 2 and 5. The LMI boards should not be interchanged, as each board is strapped differently. The LMI plugs into Connectors 0 and 1 for power, ground, and LMB and LMM interfaces.

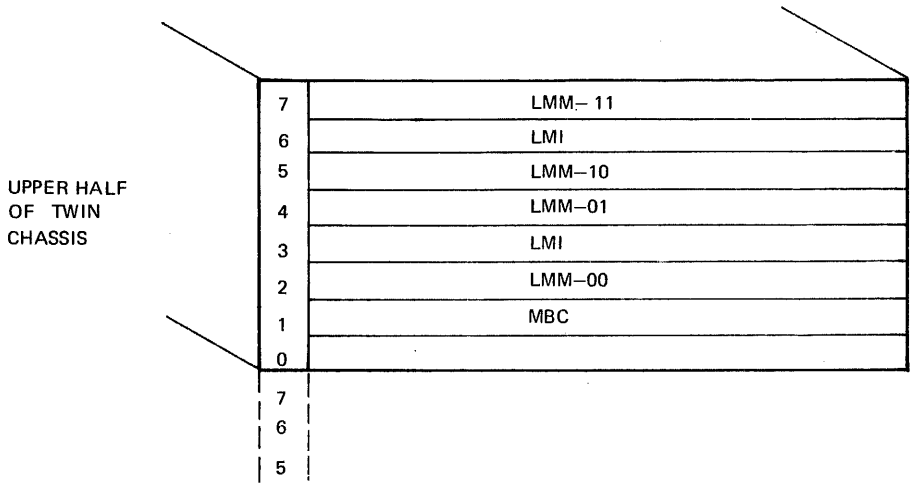
5. COMPATIBLE MEMORY MODULES

NOTE

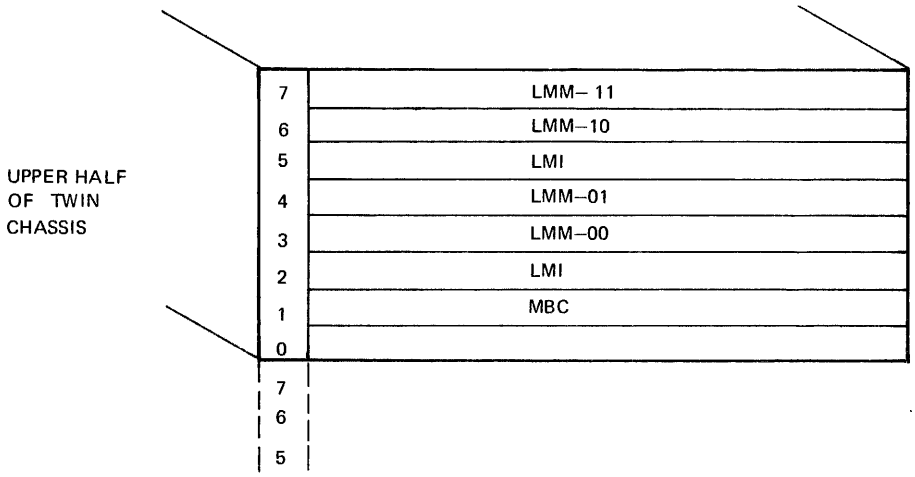
The descriptions in this section are not meant to limit future memory expansion to the types of Memory Modules specifically mentioned. Future development may result in additional compatible Memory Modules (for example, semi-conductor memories) which meet the same interface specifications and therefore can be accommodated.

The Main Memory System is designed to accommodate two different standard Perkin-Elmer modules within Local Memory as follows:

32-206 (02-409)	32 KB 750 nanosecond cycle time Module
32-209 (02-483)	64 KB 750 nanosecond cycle time Module



8/32 and 8/32C Main Memory System



8/32D Main Memory System

Figure 3. Basic Configuration

The standard configuration rules for the system are such that only one type of Memory Module may be used within Local Memory; i.e., mixing memory types is not permitted except by special configuration. Provisions have been made in the memory system design for special configurations where up to two pairs of SLMIs can be added to the LMB in addition to one pair of LMIs, with each pair accommodating a different type of standard Perkin-Elmer memory module. That is, each pair of LMIs is strapped to respond only to separate, contiguous blocks of memory address. Figure 4 shows a special configuration.

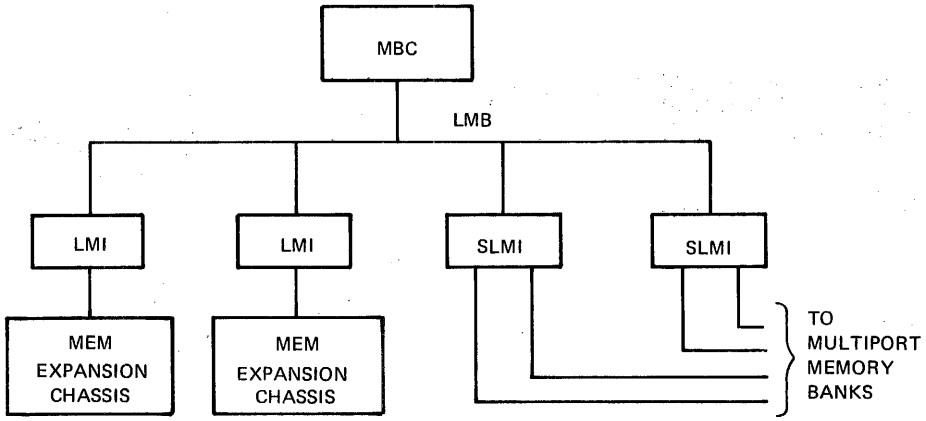


Figure 4. Example of a Memory System Special Configuration

6. CPU/MBC INTERFACE

The CPU/MBC interface between the MBC and CPA boards consist of the following lines:

MNEMONIC	NAME	DIRECTION
CA120:300	Control Address	CPA → MBC
CD000:310	Control Data	CPA ⇄ MBC
CMC000:020	Control Memory Control	CPA → MBC
CREQ0	Control Request	CPA → MBC
CRDY0	Control Ready	CPA ← MBC

Data and Code Lines

Address Lines (Control Address–CA120:300)

These lines transfer the 19-bit address from the CPA to the MBC for all CPU memory accesses.

Data Lines (Control Data–CD000:310)

The bi-direction Data Lines transfer data between CPA and MBC for all CPU memory accesses. Halfword data is always transferred on CD160:310.

Control Code Lines (Control Memory Control–CMC000:020)

The CMC lines carry a code from the CPA to the MBC indicating the type of memory access CPU is requesting. The CMC code is shown in Table 2.

TABLE 2. CMC CODE

CMC BIT			FUNCTION
000	010	020	
0	1	0	READ FULLWORD
0	0	0	INSTRUCTION READ
0	X	1	READ HALFWORD
1	0	0	WRITE FULLWORD
1	1	0	NO ACTION–NOT USED
1	0	1	WRITE HALFWORD
1	1	1	NO ACTION–NOT USED

Control Lines

CREQ0 — The Control Request line is pulsed low-active by CPA whenever the CPU is requesting a memory access.

CRDY0 — Control Ready is pulsed low-active by the MBC when data is valid during a read cycle, or when a write cycle no longer requires valid CMC code and data from the CPU.

One other control line, DMFP0, is transmitted from the MBC to the IOU board and is maintained low active whenever a memory error is detected from Local Memory or remote memory (on the EDMA Bus).

6.1 Types of CPU Memory Operations

The CPU can be serviced with five different types of memory operations as defined by the CMC code. Read fullword and write fullword are 32 bit data operations; read halfword and write halfword are 16 bit data operations. Instruction read appears at the CPU interface to be a halfword read. However, the MBC responds differently to the instruction read code as described in Section 11.3.

7. MBC/EDMA INTERFACE

The interface of the MBC with the Extended Direct Memory Access (EDMA) Bus provides high speed interconnection between the CPU and up to three remote memory systems, as well as between Local Memory and up to four EDMA Channel controllers (DMAC). These DMACs can include Extended Selector Channels (ESELCH) and custom EDMA controllers. In addition, the MBC interface supports the EDMA Bus control circuits.

The EDMA Bus control circuit maintained by the MBC consists of the following control lines:

QUE0 — The Queue pulse resolves contention for the bus by freezing the request status at its leading edge.

RPC0/TPC0 — Receive Priority Chain (RPC) and Transmit Priority Chain (TPC) are the low-active daisy-chain priority signal which select the highest priority requesting device captured by QUE0.

SOT0 — The negative going leading edge of Start of Transmit (SOT) enables the selected device to start transmission over the bus.

The remaining lines which comprise the MBC/EDMA interface are:

DMA Data Bus Lines

DMX120:150
DMA000:170 — The DMA Data Bus contains 22 lines that carry multiplexed address and command code, write data, and read data. Data Bus formats are shown in Figure 5.

Control Lines

XREQ0 — Common Request line pulled low by any memory or DMAC requesting service.

LMRQ0 — Local Memory Request Queued is pulled low by a DMAC when it is selected by RPC0, if it is requesting Local Memory.

LOAD0 — The negative going edge of Load gates the contents of the DMA Data Bus into the appropriate receiving register of a memory interface on DMAC to memory transfers.

ANS0 — The negative going edge of Answer Sync. loads the contents of the EDMA Data Bus into the appropriate receiving registers on memory to DMAC transfers.

EOT0 — End of Transmit is a high speed timing signal generated by the DMAC or memory at the end of its last data bus pulse. It signals the bus control circuits on the MBC that one device is finished with the bus and it may issue SOT0 to the next user if a request is queued and ready.

M0BZ0:M3BZ0 — There is one MxBZ0 (Memory Busy) line associated with each of the four memory systems connected to the bus (Local Memory plus three Remote Memories). MxBZ0 is pulled low by the active DMAC as soon as it receives the SOT0 pulse. It is released by the DMAC at the end of the address pulse but is held down by the memory until the memory is capable of receiving the next command.

BH0 — The Bus Hold line is pulled low by an immediate response memory interface and is held low until the answer is returned. This signals the bus control circuit on the MBC that no SOT0 signal can be generated to another device until the immediate response memory is finished with its cycle.

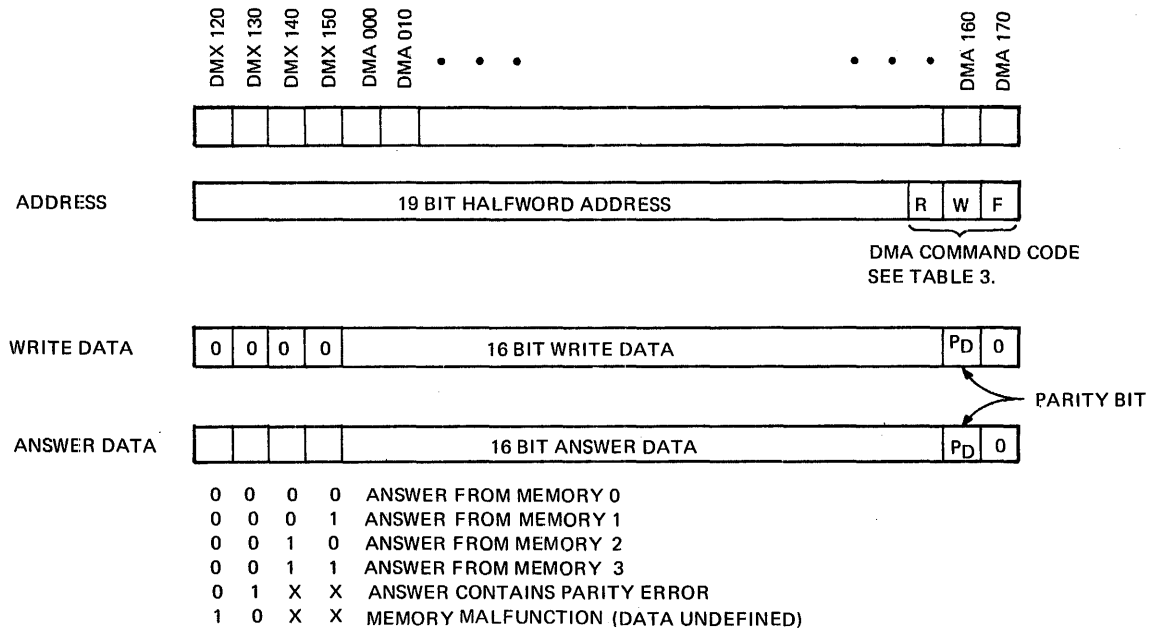


Figure 5. EDMA Data Bus Formats

7.1 EDMA Bus Control Logic

The EDMA Bus control logic is located on the MBC and is used to resolve contention of devices requesting service on the EDMA Bus, queue the selected device (QUE0), establish an order of priority of requesting devices (RPC0/TPC0), and issue a start command (SOT0), indicating that one device has the use of the bus and may begin transmission.

7.2 Types of EDMA Operations

Seven types of data transfer operations can occur over the EDMA Bus. Table 3 lists the operations and their identifying command codes which are transmitted on the R, W, and F bits of the EDMA Data Bus address format (DMA150, 160, and 170 respectively) in low active polarity (see Figure 5).

Read halfword and Write halfword are 16-bit data transfers. Read and Set halfword is a remote memory Read operation which, in addition to reading the data, causes the most significant bit of the data halfword in the remote memory to be set after the read is accomplished. Read fullword and Write fullword are 32-bit data transfers in which the data is sent over the EDMA Data Bus in separate 16-bit halfwords.

Burst read and Burst write are block transfer operations in which a single EDMA request initiates a block of continuous memory accesses to sequential fullword addresses.

TABLE 3. EDMA COMMAND CODE

R	W	F	FUNCTION
1	0	0	READ HALFWORD
0	1	0	WRITE HALFWORD
1	1	0	READ AND SET HALFWORD
1	0	1	READ FULLWORD
0	1	1	WRITE FULLWORD
1	1	1	READ BURST
0	0	1	WRITE BURST

8. MBC/LMI INTERFACE

The MBC/LMI interface consists of the following lines:

MNEMONIC	NAME	DIRECTION
LMB000:310	Local Memory Bus	MBC ⇄ LMI
LMRS0	Local Memory Request Service	MBC → LMI
LMDS0	Local Memory Data Strobe	MBC → LMI
LMRDY0	Local Memory Ready	MBC ← LMI
LMBSYA0, LMBSYB0, LMBSYC0	Local Memory Busy A, B, and C	LMI ⇄ LMI

Data Bus LMB000:310

These bidirectional lines are time-multiplexed to transfer address and control data to the LMI boards at the start of a memory cycle and later to transfer data between the MBC and LMI boards, as shown in Figure 6. Halfword data is always transferred on LMB160:310.

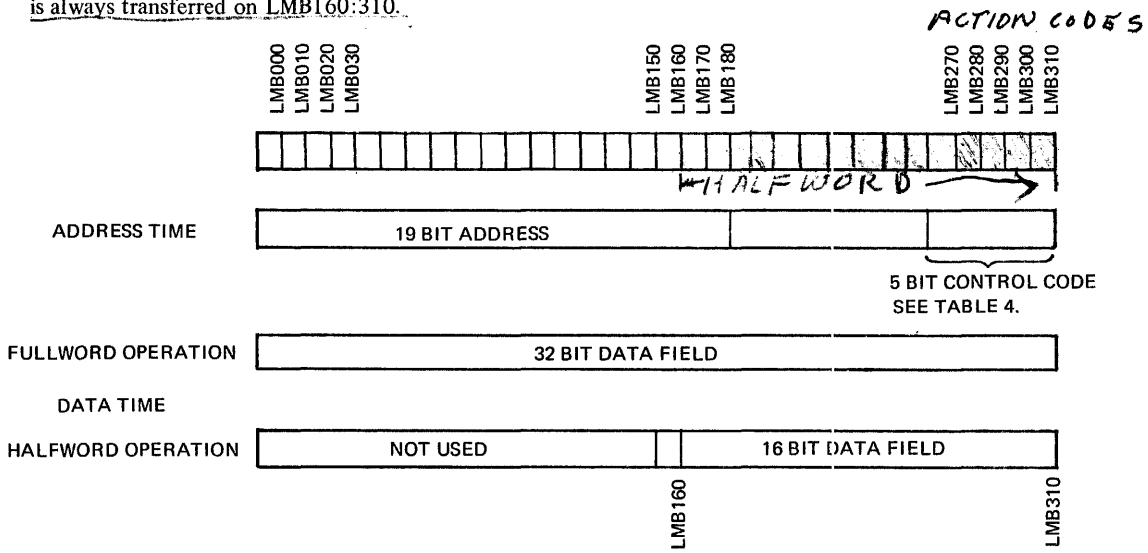


Figure 6. Local Memory Bus Formats

Control Lines

LMRS0 — Local Memory Request is made low-active when the MBC is requesting a memory cycle.

LMDS0 — The leading edge of Local Memory Data Strobe clocks write data into the LMI Memory Data Register during Write operations.

LMRDY0 — The Local Memory Ready pulse is maintained low active when an LMI begins the requested memory cycle and when data for a Read operation is valid on the LMB.

LMBSYB0, LMBSYC0 — Local Memory Busy A, B, and C communicate between LMI boards to synchronize their access cycles for an instruction Read operation.

8.1 Types of Memory Operations

Five types of data transfer operations can occur over the Local Memory Bus. Table 4 lists the operations and their identifying control codes. The control code is transmitted over LMB27:31 during address time (see Figure 6) with high-active polarity.

TABLE 4. LOCAL MEMORY CONTROL CODE

ACTION CODES

LMB27	LMB28	LMB29	LMB30	LMB31	FUNCTION
C001	C011	C021	EX1	SX1	
0	X	1	X	0	WRITE FULLWORD
1	0	1	X	0	READ FULLWORD (FROM CPA or DMA)
1	1	1	1	0	READ FULLWORD (FROM DMA in BURST)
0	1	0	X	0	WRITE HALFWORD
1	X	0	X	0	READ HALFWORD
1	1	1	0	0	INSTRUCTION READ (FROM CPA)
X	X	X	X	1	INSTRUCTION READ (FROM LOOK-AHEAD CACHE)

Write and Read fullword are 32-bit data transfer operations. Note that two codes exist for read fullword—the LMI responds identically to either code. Write and Read halfword are 16-bit data transfers over LMB16:31. An Instruction Read request causes both LMIs to respond with a fullword Read operation. This results in a double fullword Read operation, aligned on double fullword boundaries. The first 32-bits transmitted to the MBC contain the actual instruction halfword requested. 125 nanoseconds later, the second 32-bits of the aligned double fullword is transmitted by the other LMI. Both fullwords are stored in the look-ahead cache.

Note that there are two Instruction Read codes, depending on whether the CPU or the look-ahead cache initiated the request. The LMI boards respond identically to either code.

9. LMI/LMM INTERFACE

The LMI interface with the Local Memory Modules (LMMs) is defined by the following lines:

MNEMONIC	NAME	DIRECTION
MS000:160	Memory Sense Bus	LMI⇄LMM
MD000:160	Memory Data Bus	LMI⇄LMM
MAX060, MAX070, MA00:14(0)	Memory Address	LMI→LMM
ER0	Early Read	LMI→LMM
EWRT0	Even Halfword Write	LMI→LMM
OWRT0	Odd Halfword Write	LMI→LMM

Data Lines MS000:160 and MD000:16*

These two bidirectional data busses carry 16 bits + parity of read data and write data between an LMI and its two separate banks of memory. The MS Bus and associated memory bank handle the most significant (even) halfword in an aligned fullword, while the MD Bus and memory bank handle the least significant (odd) halfword (see Section 3). The two busses are then linked together within the LMI for a fullword of data (on fullword operations).

Address Lines MAX060, MAX070, MA00:14, (0)

These lines carry the 17-bit address from the LMI to both banks of memory. Contrary to their mnemonic designation, the LMI outputs high-active address information.

Control Lines

ER0	Early Read is a Memory Module control signal which initiates the readout phase of a core memory cycle.
INH0	Inhibit is a Memory Module control signal which initiates the restore/write phase of a core memory cycle.
EWRT0	Even Write is a Memory Module control signal which is maintained low-active when it is desired to write into the even-halfword bank of memory.
OWRT0	Odd Write is a Memory Module control signal which is maintained low active when it is desired to write into the odd-halfword bank of memory.

The Memory Module cycle is basically the same for any request type initiated by the MBC, the only difference is that one or both of EWRT0/OWRT0 are maintained low active if a Write operation is performed. It is important to remember that an LMI cycles two Memory Modules (even and odd halfword) for every access cycle, whether the request is for a halfword or fullword operation.

10. MBC BLOCK DIAGRAM DESCRIPTION (See Figure 7.)

1. The 19 CAXX0 lines from the CPA are the memory address lines. They are stored in 19 tracking latches, the CA ADDR Register.

2. The STK ADDR Register contains the 17-bit address of the four halfwords in the stack with the lowest double-fullword address. The STK A valid flip-flop indicates when this data is valid.

3. STK B Σ is a 16-bit adder that effectively adds 1 to the stack address register to provide the address of the four halfwords of data in the stack with a higher double-fullword address. The STK B valid flip-flop indicates when this data is valid.

4. The comparators, CEQL and CEQU compare the 17 most significant bits of the CA ADDR Register to the STK A and STK B data to determine if the address requested is contained in the stack.

5. The Control Memory Control (CMC) analysis block decodes the Instruction Read code, data read and write codes, and the null state code of the CMC bits.

6. The Memory Contention (MC) circuit resolves contention for the memory between the Processor, the EDMA Bus, and the look-ahead stack. In the case of more than one request to the memory, the Memory Contention (MC) circuit also sets priority. The EDMA Bus has highest priority, the Processor second, and the look-ahead stack lowest. This circuit enables the Local Memory Request Service signal (LMRS), holds the Local Memory Bus Busy state, and is reset by the Cycle Complete (CYCOM) signal.

7. The enabled LMRS logic generates LMRS with the appropriate delays and conditions.

8. The Cycle Complete (CYCOM) logic generation indicates that the present access to memory using the Local Memory Bus is completed.

9. Counter F (CTR F) keeps track of the number of Local Memory Readys (LMRDY) required from the LMI to steer the data and input to the CYCOM logic.

10. The Local Memory Bus (LMB) is a 32-bit bidirectional bus that sends and receives the LMI data to and from the LMIs.

* These bidirectional data busses should not be confused with the unidirectional MS and MD lines on the Memory Modules. The MS and MD lines of the Memory Module are wired together and the combination is then connected to either the LMI MS Bus or LMI MD Bus, as appropriate.

11. When the LMRS signal is sent to the LMIs, the LMB is used for address and control information. The LMB is driven by tri-state multiplexors at each end and received by STTL gates. The address information is low active on the bus while the control bits are high active. The first Local Memory Ready signal from the LMIs indicate that the address has been accepted and the memory cycle has started. The LMB is then used for the transfer of data. The data is high active on the LMB.

    The LMB tri-state multiplexor puts the address on the LMB either from the Processor (CAF), the EDMA (DAD), or from the stack request (STB). For Write operations to memory this multiplexor is also enabled and places either the Processor data (CD), or the EDMA data (DMF) on the LMB.

12. The Instruction Stack contains eight halfwords. It has separate Read and Write select lines. It is loaded four halfwords at a time, each time the Processor makes an Instruction Read memory access or each time the stack makes a look-ahead access. The four halfwords come in two 32 bit passes on the LMB. The Write select logic determines the stack address to be loaded and the CTR F logic creates the Load strobes. The Read select lines come directly from the three least significant bits of the address from the Processor, CAF. A tri-state multiplexor, CD B, places the data from the stack onto the CD lines to the Processor during an Instruction Read from an address in local memory.

13. Tri-state multiplexor CD A places data onto the CD Bus to the Processor during a data read from Local Memory or during a read from memory on the EDMA Bus.

14. The Address analysis logic looks at the address requested by the Processor on the CA lines and compares it to four sets of straps to determine if the address is contained in Local Memory, or in one of the three memories that can be placed on the EDMA Bus, or it is beyond the range of memory fitted in the particular machine. The outputs M0, M1, M2, M3, and GTUU (Greater Than Unused) indicate in what region the requested address lies. There are four straps in each set so the one megabyte of memory can be divided up with a resolution of 64 K bytes.

15. Tri-state buffer A places the CAF information on the DMT lines (to DMA transmitters) for Processor requests to memory on the EDMA Bus. Tri-state multiplexor, DMT A, places the data onto the DMT lines when the request is a write to external memory.

16. The DMA transceivers translate the TTL DMT levels into the EDMA Bus levels.

17. The LM data register stores the LM data for answers to EDMA requests from Local Memory.

18. The tri-state multiplexor, DMT B, places the correct half of the LM register onto the DMT lines for these reads.

19. The DXR and DMR lines are signals from the EDMA Receivers.

20. The DMA address register counter stores (and increments when necessary), the 19-bits of address information from the EDMA Bus during accesses to Local Memory.

21. The DMA CTRL register stores the three control bits.

22. The DMA data register is a 32-bit register that stores the data from the DMA Bus that is sent to Local Memory on a write, or stores the read data sent back to the Processor from external memory.

23. The DCOMP A and the DCOMP B circuits are comparators that signal when the EDMA Bus is Writing into memory over an address that is valid in the instruction look-ahead stack.

24. The CPA SEL logic requests the EDMA Bus for transfers to external memory and gets the CPA selected as the transmitting device on the EDMA.

25. CTR B generates the Load and End of Transmit (EOT) signals for the EDMA when CPA is communicating with external memory. It also helps create the signals for data steering and enabling.

26. CTR D receives Load signals from the EDMA Bus and creates the load register signals. It counts the loads and initiates action when required.

27. The Bus Control logic with signals from CTR A, handles the requests for the EDMA Bus and generates the Queue (QUE), Transmit Priority Chain (TPC), and Start of Transmit (SOT) for the bus.

28. The CRDY logic generates CRDY back to CPA at the end of the CPA access.

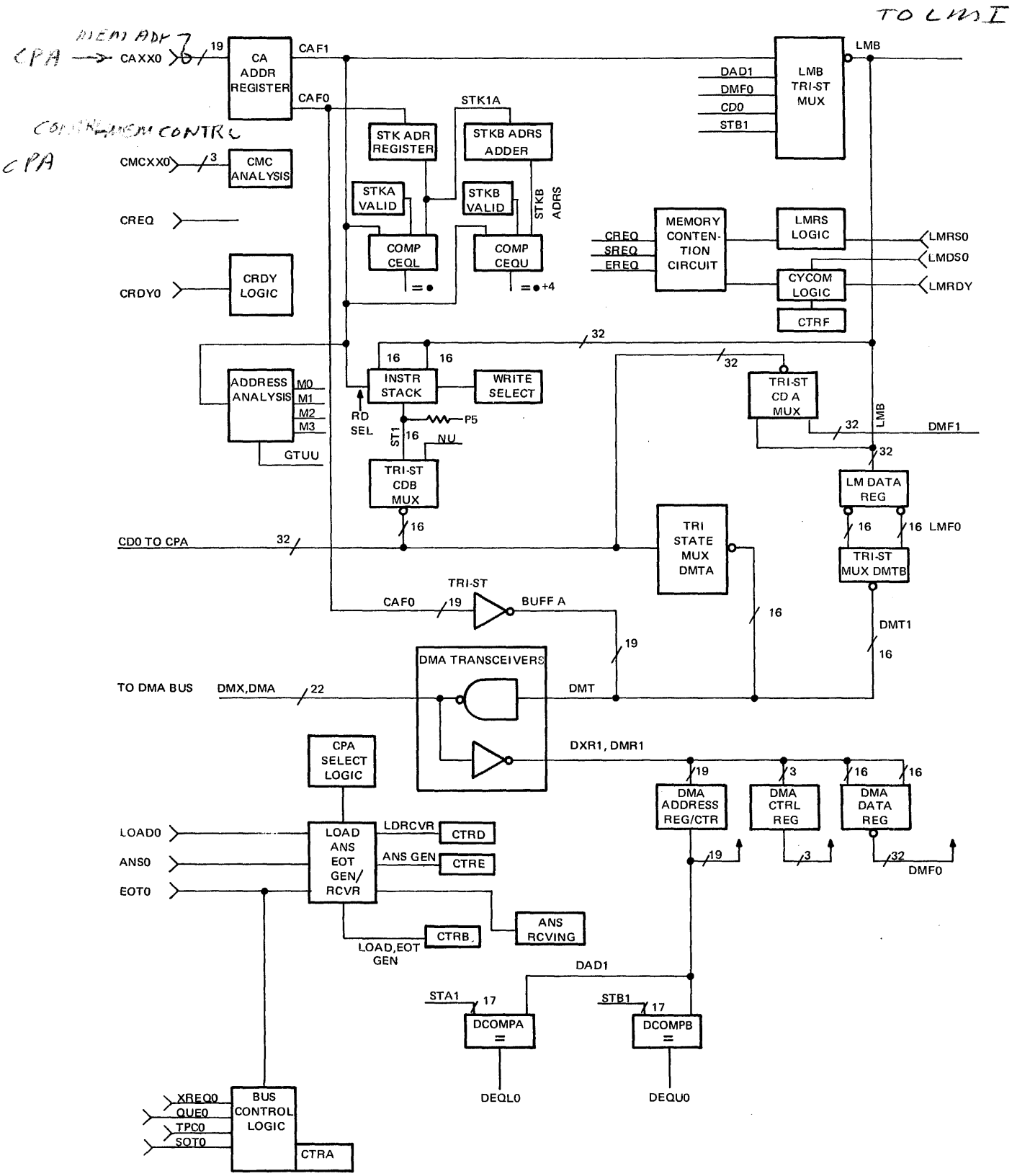


Figure 7. MBC Block Diagram

11. MEMORY BUS CONTROLLER (MBC) FUNCTIONAL DESCRIPTION

11.1 CPA to Local Memory Write Halfword of Fullword

11.1.1 Address Transfer Cycle. Refer to timing diagram Figure 8. The address bits from CPA come through tracking latches (Sheet 6) which are tracking because the CREQF (6F6) is still reset. The address is analyzed by the comparators (Sheet 9) and found to lie in the range of the Local Memory (Memory 0). The CMC bits (11H6) are also checked and it is found that this access is not an Instruction Read (IR).

The CREQ pulse is received from the CPA and stored in the CREQF (6F6). A delay line (14A7) is also started to give delayed signals equivalent to CREQF. The setting of CREQF freezes the address in the tracking latch and signals the start of the MBC response.

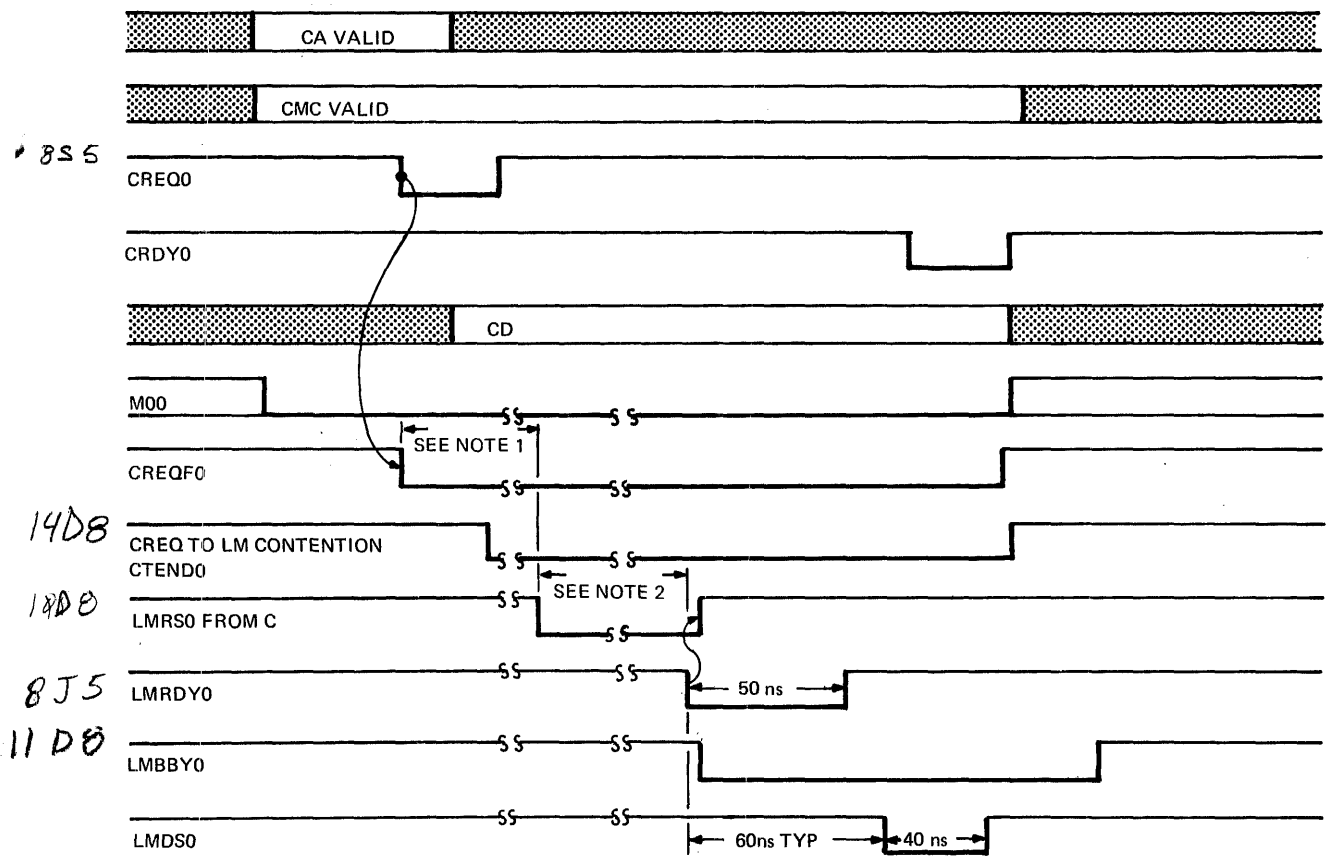
CTEND0 (13E8) is the input to the Memory Contention circuit and it is created from M01, IR0, CRQD001 (CRQD001 is CREQ delayed zero time), and no resetting signal. The CTEND0 signal is immediately sent when CREQ is received, the access is not an Instruction Read (IR0), and the address is in the range of Local Memory (M01).

The LMB multiplexors (Sheet 3) enable and select the CAFxx1 and CAFBxx1 signals with a low active signal on DATTM1 (13M9) and a high active signal of EFB0. DATTM1 is low active during address time except when the look-ahead stack is requesting to be filled from memory (SMX0 being low).

The address time ends when the Local Memory Bus Busy flip-flop is set. This occurs when the first Local Memory Ready is received from the LMIs. The command code is also sent on the LMB at the same time as the address. Bit 27 on the LMB (LMB270) is low at this time for write commands.

The AND-OR-Invert gate (13N7) creates Local Memory Request Service (LMRS). The CF1 and EF0 inputs indicate that the Processor (C) and not the EDMA (E) is in control of the memory. LMRS is turned off by LMBBY being set. The D35 is a delayed enable signal from the contention delay line and is discussed in the Memory Contention circuit.

Note in the timing diagram that the gap between CREQ to LM and the LMRS0 from C could be caused by another cycle presently in progress or a request from the EDMA Bus which has a higher priority. The gap between LMRS0 and LMRDY0 is caused by the LMI being addressed while still being busy from a previous access.



NOTE 1: This Delay depends on whether or not the Memory is busy with an EDMA or Stack Request.
NOTE 2: This Delay depends on whether or not the requested LMI is busy.

Figure 8. CPA → LM Write Timing Diagram

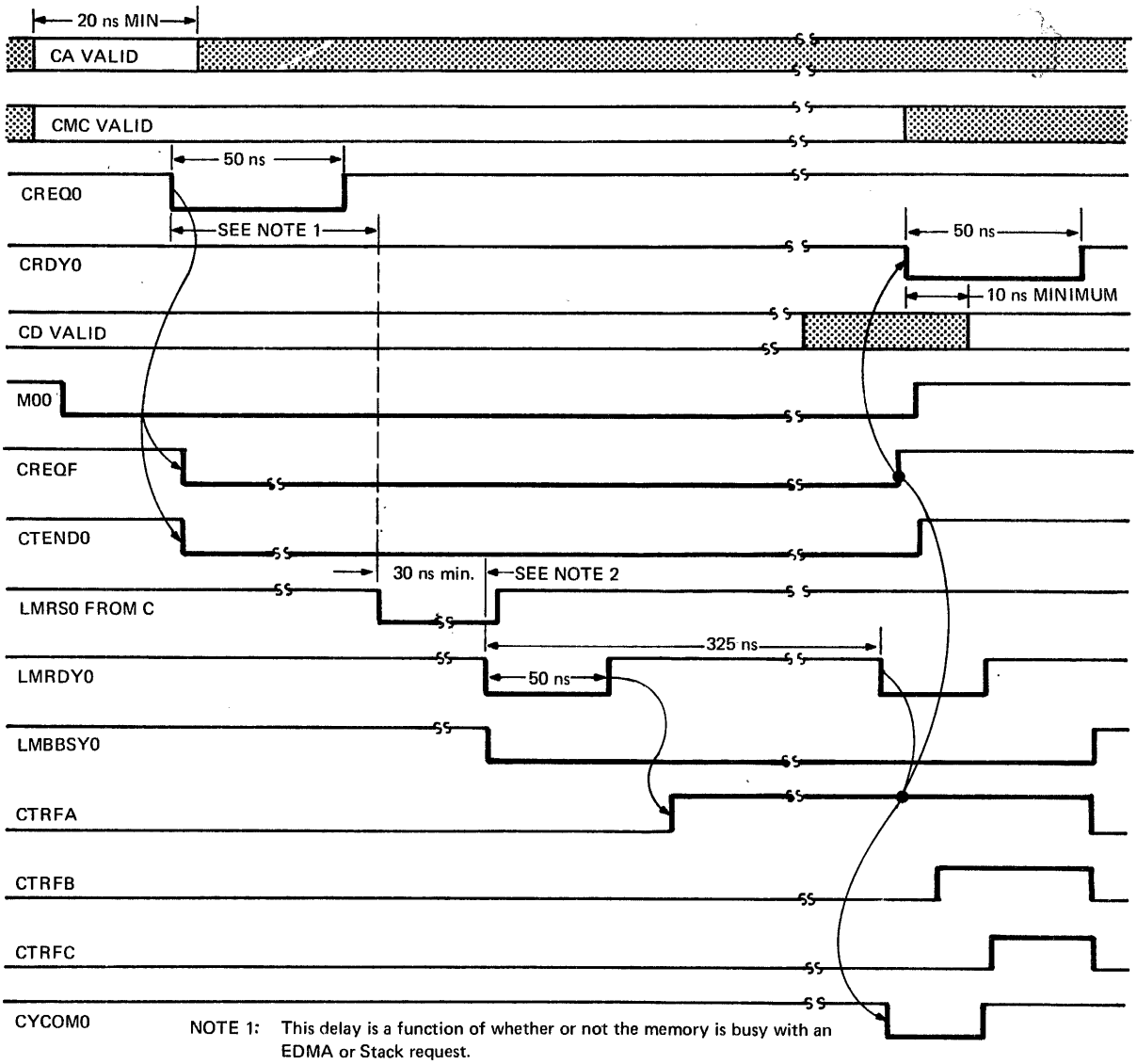
11.1.2 Data Transfer Cycle. During the LMRS signal, a delay line (11L9) is being loaded with a low active signal to generate the data strobes on the LMB and the Local Memory Data Strobe (LMDS).

The conditions necessary to load this delay line with a 0 are: 1. Not a stack request SMX0, 2. Local Memory Request Service (LMRS1), and 3. Data write command code as indicated by a 1 on LMB271. When LMRS is disabled (caused by the LMRDY signal from the LMI which sets the LMBBY flip-flop) the delay line (11L9) starts to reload with a 1 level. Meanwhile, DATTM1 (13L9) has gone high active because of LMBBY, causing WDTM0 (Write Data Time) to go low (11N7). Local Memory Data Strobe (LMDS) is also generated (11N5) by this delay line and occurs during WDTM.

The LMB multiplexors (Sheet 3) are switched at data time because the address enabling signal, DATTM1, goes high and the Write Data Time (WDTM0) signal goes low, enabling the CD lines onto the LMB and disabling the CAF lines. LMDS indicates the end of the cycle and Cycle Complete (CYCOM). CYCOM is generated in parallel on the AND-OR-Invert gate (11D8) by DA701 and DA400. Cycle Complete (CYCOM) resets the Memory Contention circuit. The ready signal to the Processor (CRDY) is generated by the AND-OR-Invert gate (14N8). LMDS causes CRDY through the gate (14K8) which is the OR of LMDS or Instruction Read ready from Local Memory (IRWRT – Instruction Read or Write). The CREQ flip-flop is reset in parallel by the same signal into the RCREQF circuit (14R5). There is no distinction made in the MBC between halfword and fullword accesses to Local Memory.

11.2 CPA to Local Memory Read Halfword or Fullword

11.2.1 Address Transfer Cycle. Refer to timing diagram Figure 9. This cycle is the same as for the data writes to Local Memory except that Bit 27 on the LMB (LMB271) is high at this time indicating a read command.



NOTE 1: This delay is a function of whether or not the memory is busy with an EDMA or Stack request.

NOTE 2: This delay is a function of whether or not Local Memory is busy.

Figure 9. CPA→LM Read Timing Diagram

11.2.2 Data Transfer Cycle. The edge of the first LMRDY signal from the LMI indicates that the address has been accepted and the data cycle follows. At this time the LMB multiplexors in the MBC are turned off waiting for the LMI to send back the data. This is accomplished by DATTM1 (13M9) going to the 1 state when LMBBY (13G9) is set.

Counter F, Stage A (CTF A) (11E4) is set on the trailing edge of LMRDY. The LMI sends another LMRDY when it has the data settled on the lines so Stage A of Counter F is used to differentiate between the first and the second LMRDY.

When the LMI sends data, it is placed on the CD lines through tri-state multiplexors (Sheet 4), CDA. At this time the Read Data (RDDAT0) signal is low (11H5). This is generated by the AND of CMC001 (11F5) and not an Instruction Read from Local Memory (STCD0) (11C5). (STCD0 – Stack to CD enable signal). RDDAT0 and STCD0 enables the multiplexors, and M00 (Memory Zero or Local Memory) or MB00 (Buffered Memory Zero) select the LMB lines.

Cycle Complete (CYCOM0) is generated by the second LMRDY when it is ANDed with CTF A and not an Instruction Read and not a Stack Access (SMX0) to memory (AND-OR-Invert gate) (11D8). CRDY is generated in parallel by CTFA1 (14N8), LMRDY (delayed by 5 nanoseconds extra), and the output of a flip-flop which indicates that the access was not an Instruction Read. The reset of the CREQF flip-flop is generated by CRDY (14R6).

11.3 CPA Instruction Read from Address in Local Memory

11.3.1 Instruction Valid in the Stack. The Control Address flip-flops (CAF) tracking latches are constantly being compared against the STA and STB signals. STA is the output of the register that stores the present base address of the data in the stack (Sheet 7). STB is the output of the adder (Sheet 7) that adds 1 to STA, giving the address of the data in the upper half of the stack. Note that there is no STB28 because this is the complement of STA28. This is the reason there are 17-bits of STA but only 16-bits of the adder are needed to add 1 to it.

The comparisons are done on Sheet 8. Bit 17 is handled in both cases by Exclusive OR gates (8H9). Even if the address compares in one of these two comparator circuits, other signals are needed to obtain an equal output. These signals are STKA, which indicates that the lower half of the stack is valid, STKB, which indicates that the upper half of the stack is valid; and SD200, which is a signal that permits the data in the stack to be loaded and settled from a stack access.

If either of these comparisons show up as equal by the time the CREQ signal reaches the 20 nanosecond tap on the CREQ delay line (14A7), then it is remembered in a cross coupled EQ1 flip-flop (14D7). EQ1, M01, IR1, and C0 (Instruction Read, and Processor not accessing memory) combine in an AND gate to become EQIRC0 (14G6). This combines with CRQD30 (CREQ delayed 30 nanoseconds) to form the CRDY back to the Processor (14M8). The equivalent of the Stack Ready (STKRDY) is generated two other places, once as the true signal (STKRDY1) (14G8) and once as the not signal at (STKRDY0) (14G7). These are used to load the STA register with the present base address of data in the stack (14J7) and to reset STKB (14L6) (indicator of the validity of the upper half of the stack) if the access is to the upper half of the stack, and generate a request to memory at the same time to refill the stack with a Set Stack Request (SSREQA) (14M6).

The data is delivered to the CD lines during this process from the stack (Sheet 5) through CD Multiplexor B, (Sheet 4). These multiplexors are enabled by a STCD0 signal (11C5). STCD0 is low whenever the Processor is doing an Instruction Read (IR) from Local Memory (M01).

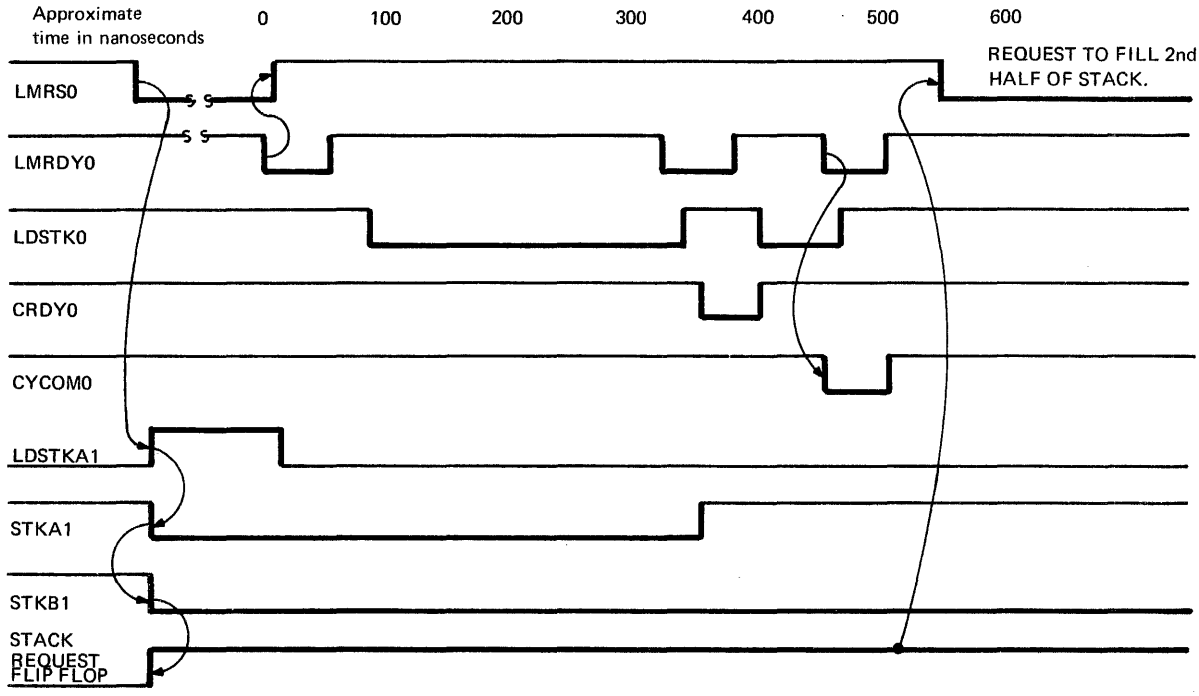
The correct word in the stack is addressed by the three least significant bits of the address.

11.3.2 Address Requested not in Stack or Stack not Valid. Refer to timing diagram Figure 10. If the comparators do not indicate an equal in either half of the stack and the address is in Local Memory (M0) then a request to Local Memory is made. This is accomplished with CTEND0 (13D8) created from not CEQL, not CEQU, M0, and not any other ready or complete presently being generated and the stack not being filled (SD500–Stack Delayed 50 nanoseconds).

The request and address transfer cycle to Local Memory is the same as for data reads or writes. The data cycle requires transferring two 32-bit words as follows. The second LMRDY from the LMIs indicates that the data fullword containing the requested halfword is on the LMB. This is enabled into the stack with the signal LDSTK0 (11C1). The delay line (11B2) creates the proper timing of this signal from the second LMRDY. CRDY (14R8) is generated at this time by the AND of CTFB1 and CTFC0. Counter F, Stage B is set during the second LMRDY and Counter F, Stage C is set at the trailing edge of the second LMRDY. Reset CREQF is generated in parallel by IRWRT0 (Instruction Read or Data Write) (14R6). Cycle Complete (CYCOM) is generated by the third LMRDY from the LMIs by the AND of Counter F Stage C (CTFC) and LMRDY at the AND-OR-Invert gate (11C8).

When the Processor has to go to Local Memory for an instruction, the STA register (Sheet 7) is loaded with the new base Address (LDSTA1) (14J7). The two flip-flops that indicate the valid state of the stack, STKA (14J4) and STKB (14L6), are both reset by C1LMRS0 (14 G5). There are three other signals that can reset these flip-flops through the clear input. These signals are System Clear (SCLR), writing into an address that is valid in the stack with a Write command from the EDMA Bus (DEQ), and writing into an address that is valid in the stack from the Processor (from CMC000, and C1 AND LMRS).

The STKA flip-flop is set again with the IRWRT signal (14H5) when ANDed with C1 (the Processor in charge of the Local Memory) and IR1 (a decode of the CMC bits that indicate an Instruction Read) (11H6). C1LMRS0 also sets the Stack Request flip-flop (13B5) to Local Memory to fill the upper half of the stack with another memory access.



NOTE 1: If Stack was valid but requested instruction is not in Stack, C1·LMRS0 will invalidate stack.

Figure 10. Instruction Read when Stack is Invalid or the Requested Instruction is not Currently in Stack

The data is written through the stack on an Instruction Read by controlling the Write select lines to the stack. These signals are STWB1 (14C1) and STWA1 (14E2). The S1 and SMX0 signals to this logic are from the Memory Contention circuit indicating when the stack is accessing memory. At this time however, since the Processor (C for CPA) is accessing memory, the stack is not. This leaves S1 low and SMX0 high. This gates the state of STA280 through to STWB1 and the state of CAF290 clocked into the flip-flop on the first LMRS.

Stage B of Counter F first enables the true side of the flip flop and then the complement side through to STWA1. Meanwhile STWB1 is directly the inverse of STA280 (14B2) and is actually the equivalent of Bit-28 of the control address from CPA. Recall that STA is the register that contains the base address of the data in the stack and it was just loaded with the present address being requested by CPA (LDSTA1) (14J7) so it reflects the present state of CAF28 for this Instruction Read.

For example, if CAF290 is high indicating a request to memory with an even fullword address, then the first data back from the memory is from the even fullword LMI. Stage B of Counter F (CTF B) is still low when this data is indicated valid by the second LMRDY, and STWA1 is low for the first data fullword and high for the second data fullword from memory.

11.4 Stack Control

– Stack request to memory
– Stack filled from memory
– Stack invalid-valid states

There are two ways that the stack may start a memory access. Since an Instruction Read from CPA fills the bottom half of an empty or invalid stack, a stack request is required to fill the upper half. The C1LMRS0 signal (14G5) is caused by a CPA request. It is generated when the Processor is making an Instruction Read request to Local Memory. The other signal that sets the Stack Request flip-flop (13C5) is SSREQA0 (14N6). This occurs whenever the CPA initiates an Instruction Read to an address in the upper half of the stack. STKB flip-flop is also reset at this time to indicate that this half of the stack is temporarily not valid. The leading edge of Stack Ready (STKRDY1) resets the STKB flip-flop if the address comparison was in the upper half of the stack as indicated by C address Equal to Upper half of stack (CEQU). Note that the lower and upper halves of the stack are defined by the address stored in STA register and not by the physical address in the stack. That is, at one instant of time the bottom half of the stack may be Addresses 0:3 and at another time the bottom half of the stack may be Addresses 4:7. (The data is not moved from one location in the stack to another. Only the STA Address register is reloaded.) The STKA flip-flop refers to validity of the data in the stack that is from the memory location indicated by the STA register, and the STKB flip-flop refers to validity of the data in the stack that is from a memory location indicated by the STB adders.

The address sent to the memory during the request from the stack is from the STB adders. This is put on the LMB multiplexors (Sheet 3) by a Stack Busy signal (SBSY0) 14C1). Note that LMB310 is high indicating a Stack request to memory. SBSY0 is low when the stack is accessing memory (S1) until the Local Memory Bus Busy flip-flop is set (LMBBY0) (indicating that the memory has accepted the address and the data transfer cycle is about to begin.

During the data cycle the LMIs pass back two 32-bit words of data the same as the Instruction Read to memory from the CPA. The Load Stack signal (LDSTK0) (11C1) is generated the same as for the Instruction Reads from CPA since the SXIR signal is the OR of Instruction Read from the CPA and Stack in control of the memory (11D6). Cycle Complete (CYCOM) (11F8) is from the third Local Memory Ready (LMRDY) as indicated by the state of Counter F Stage C (CTF C) the same as for Instruction Reads from CPA to memory.

The Write select lines to the stack to select the addresses that the data goes to are STWB and STWA (14A1) (the same as described in CPA Instruction Reads to memory). The fact that this memory access is from the stack looking ahead to fill the upper half, conditions these select lines. STWB1 is the complement of STA281 since the stack fills the upper half from the opposite double fullword address as the lower half. STWA1 is always low for the first 32-bit data word in a stack access because the even address fullword is always sent back first in a Stack request (recall in a CPA Instruction Read, the first fullword sent back is the one that contains the halfword that was requested and could be the even or the odd fullword). This is done by SMX0 (the signal that enables the Stack address onto the LMB through the LMB multiplexors) presetting the flip-flop (14B2).

The signal SD500 from the delay line (13K6) is used to permit the data to settle in the stack before permitting CPA to use it.

11.5 EDMA Bus Control Circuit (See Figure 11.)

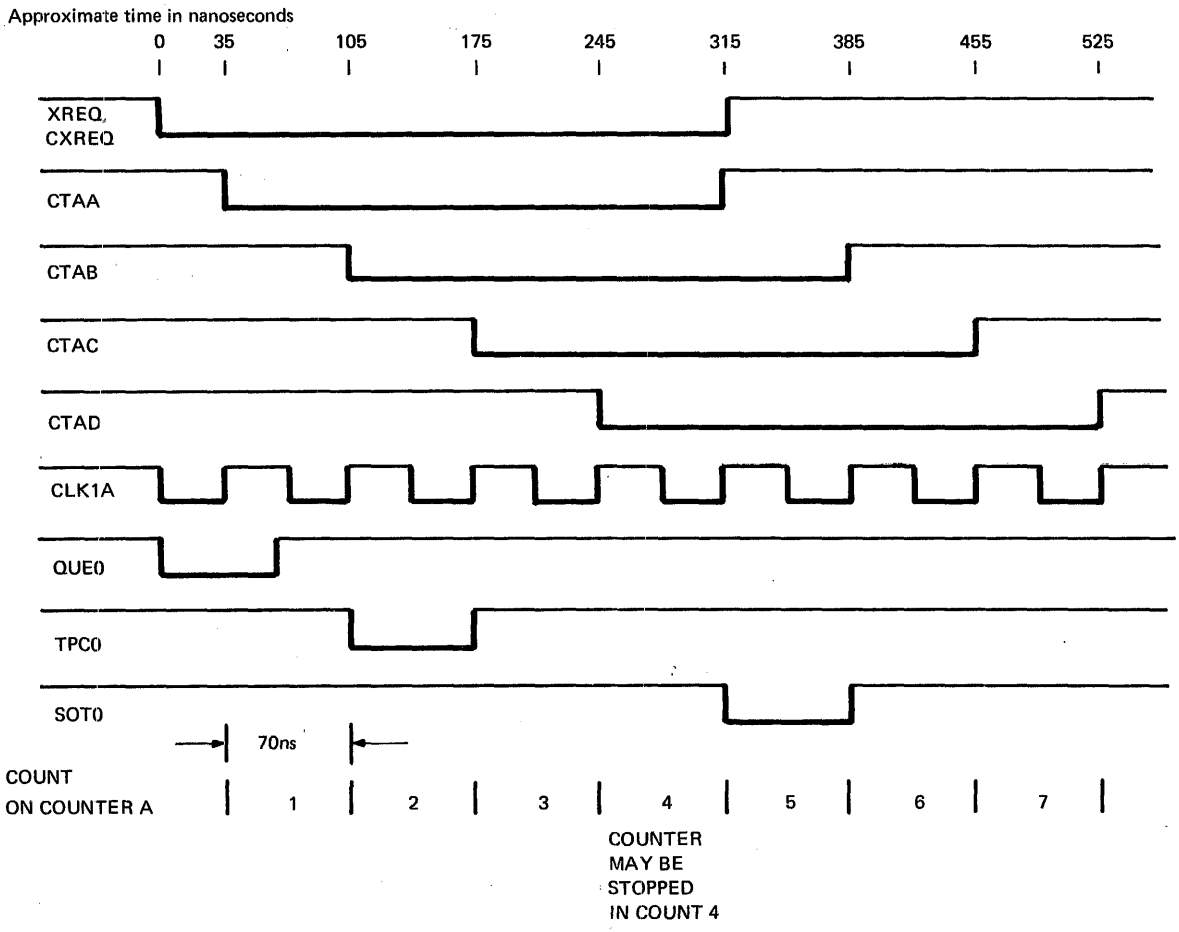


Figure 11. EDMA Bus Control

The EDMA Bus control circuit generates the QUE, Transmit Priority Chain (TPC), and Start of Transmit (SOT) signals to the bus. These signals are created from a 4-bit Johnson Counter which is labeled CTA (10H1). The counter can be stopped at either of two times by signals at the clock oscillator (10C1). At Count zero, Stage A and Stage D of the counter (CTAA and CTAD) are both high. At this time the counter is stopped unless there is a request from the EDMA Bus (XREQ) or a request for the bus from the Processor (CXREQ). This condition is the output of the four input NAND gate (10B1). When one of these requests arrives, the counter clock starts and immediately sends out a QUE0 (10N3). At Count two, the Transmit Priority Chain (TPC) (which is actually the beginning of the priority chain) is sent out (10R7). At Count 4, the counter can again be stopped (CTAA1 and CTAD1 both high) by the STHOLD1 signal (10K3). STHOLD1 is generated by the ORing of five signals. These signals are: 1. DMAACT0, which indicates that the DMA is presently transmitting data and another Start of Transmit (SOT) should not be sent at this time, 2. The Local Memory Request Received signal (LMRQR1) (which indicates that the device queued up is requesting Local Memory) is ANDed with EF0, which is the EDMA selected state of the Memory Contention circuit. This means that if the queued device is requesting Local Memory, Start of Transmit (SOT) is not sent until the EDMA has control of Local Memory in the Memory Contention circuit, 3. BH0 which is the Bus Hold signal indicating that a memory is still using the bus and will momentarily send back answers, 4. A delayed Bus Hold signal to inhibit false indications of Bus Hold being removed, or 5. EDMA Request and Burst Read (ERQBRD0) which indicates that when a Burst Read operation is occurring, another SOT should not be transmitted until the Burst Read access is completed.

Count 5 (CTA Stage B high and CTA Stage A low) (10L4) generates Start of Transmit (SOT0). SOT0 sets the DMAACT flip-flop indicating that the DMA is actively transmitting data at this time. End of Transmit or System Clear resets this flip-flop as the END0 signal (10M9).

11.6 CPA Select on EDMA Bus (See Figure 12.)

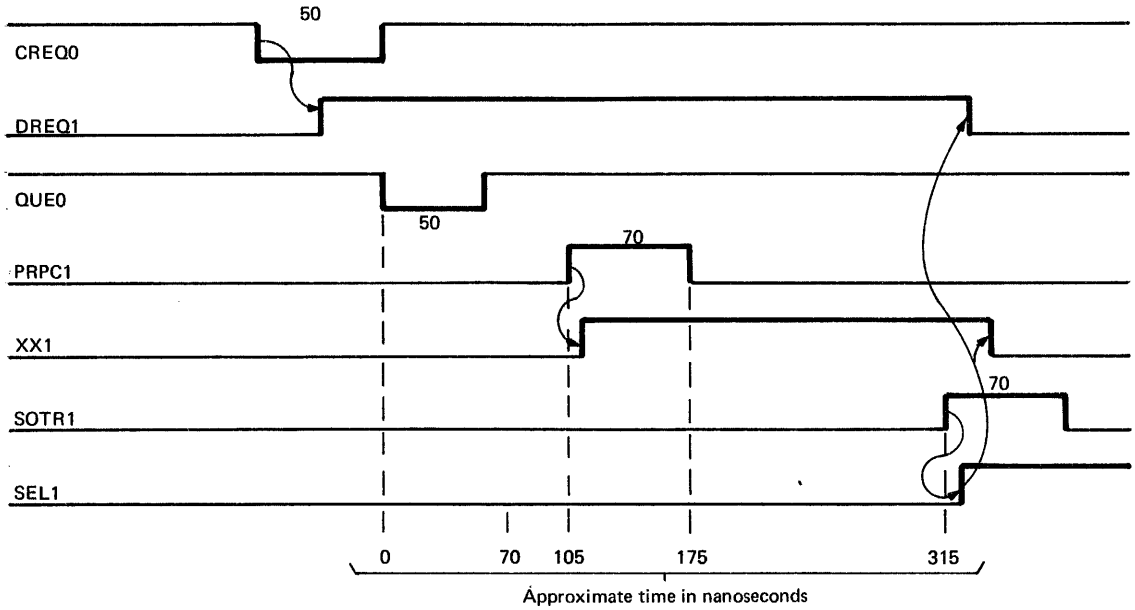


Figure 12. CPA Request to EDMA Bus

When CPA makes a request to the MBC for an address that is not in Local Memory, the address analysis logic indicates if the address is in Memory 1, 2, 3, or not in the system. This is done by the comparators (Sheet 9). The strapping on the comparators draws the division lines through the memory so that when an address (four most significant bits) is greater than one set of straps, but less or equal to the next set of straps, then the address is in that block of memory. When the address is found to be within the range of Memory 1, 2, or 3, the MBC goes out to the EDMA Bus for the access. The DREQ flip-flop (9L3) is set by a pulse when the address is not in the Local Memory addresses (M00) and less than the unequipped memory addresses (LTUU0). When the memory requested is no longer busy as determined by the AND-OR-Invert gate (9J5) then the CXREQ signal is sent to request the EDMA Bus and the SQUEF1 signal (9M5) sent to the select logic (Sheet 10).

The first Select Logic flip flop (10H6) is set on the leading edge of QUE0 when the SQUEF1 signal is present. This information is transmitted to the second flip flop on the trailing edge of QUE0. The leading edge of RPCR1 clocks the XX1 flip-flop (10K6) and the leading edge of Start of Transmit clocks this into the second Select Logic flip-flop (10N6) (SEL1).

When the SEL flip-flop (10N6) is set, the XX1 flip-flop is reset, and the DREQ flip-flop (9L3) is also reset. This ends the select sequence.

11.7 CPA Write to Remote Memory

When the Select (SEL) flip-flop is set, the delay line controlled clock at 10B3 is started. T00A is the output of this clock and it is counted in the 2-bit Johnson Counter, Counter B (CTBA and CTBB-Counter B, Stages A and B) (10E6). The LOADs and EOTs for these transfers are generated by Counter B (10F7).

The first operation is to transfer the address out to the EDMA Bus with a LOAD. Loads are generated whenever Counter B is not at zero by ANDing the CTB000 signal with the clock T00A signal (10F7). The End of Transmit (EOT) is generated with the first load if the operation is a read, with the second load if the operation is a half word write, and with the third load for a fullword write. The gate (10D7) looks at CMC001 to determine if the operation is a read, if it is, it enables the EOT signal. For halfword operations the counter is forced to skip Count 2 by the gates feeding the D input of CTBA (10D5). This gives the EOT with the second LOAD.

When the Select flip flop is set, the Control Address (CAF) and CMC bits are sent out to the EDMA Bus by turning on the tri-state buffers (Sheet 2), the transceiver at 5K2 and the transceivers on Sheet 2. The latter transceivers are also left on if the operation is a write, to transmit the data.

Note that the CMC bits are transmitted with the address but are modified in the case of an Instruction Read to be just a halfword read (2R8).

The signals that turn on these gates are DMCA0 to enable the addresses (10C7). This is the decode of Count 1 from Counter B. The signal that enables the transmitters is DMA Enable (DMENB0) (10E9) whenever Counter B is not in the zero state. There is another input to enable the transmitters called CTEA0 but this pertains to the EDMA Bus reading from Local Memory.

After the address has been transmitted with the first LOAD then the data is enabled onto the DMA Transmit (DMT) lines with the tri-state multiplexors (Sheet 2). These multiplexors are enabled by Counter B Stage B being set (Counts 2 or 3). This signal is CTBB0. If the command is a fullword write, the most significant half is transmitted first and the least significant half transmitted last. The select line to the multiplexors is from Counter B Stage A (CTBA0). Recall that for a halfword operation, Count 2 of Counter B is skipped and therefore only the least significant half is transmitted.

The ready signal to the CPA is generated by the trailing edge of the End of Transmit (11J4). Here the Enable End of Transmit signal is ANDed with CMC000 which indicates a write command and is used to set the DMRDYB flip-flop. The setting signal (DMRDYA1) and the output of the flip-flop (DMRDYB1) (Sheet 11) are ANDed (14J7) and after being ORed with other signals becomes CRDY (14S8). They also reset the CREQ flip-flop by creating the RCREQF signal (14S6).

11.8 CPA Read from Remote Memory

The request, select, and transfer of the address sequence is the same as for writes to remote memory. With the LOAD signal that transmits the address however, is also an End of Transmit (EOT). This is generated (10D7) by ANDing the CMC000 signal with State A of Counter B (CTBA1). CMC001 is high whenever there is a read command.

When the answers are returned with the data on the EDMA Bus there is a 2-bit code to indicate from which memory it was received. This code is decoded and ANDed with the address block decode from the address analysis block (Sheet 11). If there is a match between the decoded address and the requested address, the answers are used to load the two halves of the DMA Data Register (DMA flip-flops –DMF) (Sheet 1) with the Load Least Significant Half (LDLSH) and the Load Most Significant Half (LDMSH) signals (11N3). The flip-flop (11N2) is reset on Start of Transmit and is toggled on each answer. If the command is a fullword read, the first answer loads the most significant half of the register and the second answer loads the least significent half. In a halfword read, the answer counter is forced to load the least significant half first (since there will not be a second load) by the signal DMAFW0 (DMA fullword not).

The Ready signal to the CPA is from the DMRDYA1 and DMRDYB1 signals, the same as for remote memory writes. The source of these signals is the Load Least Significant Half signal (LDLSH) after checking to see that these answers were for the CPA request with the NAND gate (11K5). The conditions on this gate are C Request Delayed 60 nanoseconds (CRQD601) and DREQ0 (DMA Request having been reset by Select).

The DMA Write Data Buffers, DMF Data Register, are gated onto the CD lines during this operation through the multiplexors (Sheet 4). They are enabled by the RDDAT0 signal the same as a read from Local Memory but the multiplexor selects the DMF inputs with the M00 and the MB00 (these are the outputs of the address analysis block and they are high whenever the access is not to Local Memory).

11.9 EDMA Bus Write to Local Memory (See timing diagram Figure 13.)

Before the Start of Transmission (SOT0) is sent to the device that is queued on the EDMA Bus, it has sent back a Local Memory Request signal if it wanted Local Memory. This LMRQ0 signal is used to initiate a request to the Memory Contention circuit for EDMA control. SOT0 is not sent unless control has been granted to the EDMA Bus as indicated by the EF1 signal in the Memory Contention circuit (13H1). The memory request is not actually made yet. It is inhibited by the EHOLD0 signal. EHOLD0 does not go high until the Write Buffer is full (WRTBUF1) and Direct Memory Memory Control Bit 0 is high (DMMC000) (11M6).

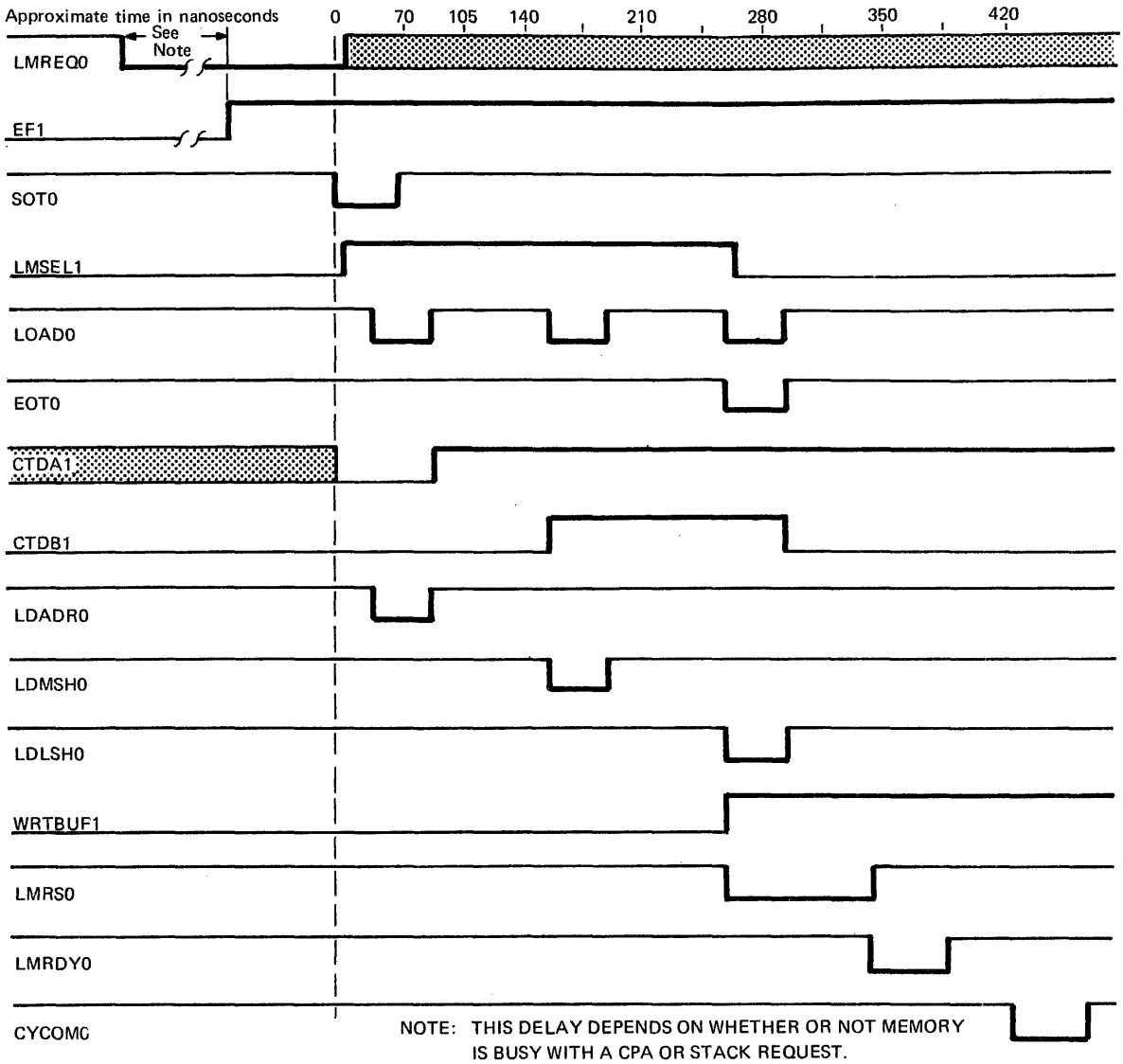


Figure 13. EDMA Bus Write to Local Memory

When LMRQR1 is high with Start of Transmission, the Local Memory Selected flip-flop is set (LMSEL) (12D6). The Start of Transmission (SOT0) initializes Counter D Stage A (CTD A), resets the Write Buffer Full flip-flop, and other flip-flops used.

Counter D keeps track of the loads being received so that the first load from the EDMA Bus loads the DMA Address Counter Register (Sheet 1). This register is loaded with a low on Address Finished (ADRFN1) (12H8) and a clock (CDMAD1) (11G9). The low on ADRFN1 is from Stage A of Counter D (CTD A) not being set yet. The clock signal is from the Load Address input (LDADR0) (11G9). This is generated (12C7) by the first load from the EDMA Bus after SOT0. At the trailing edge of this first load, CTD A is set and the Address cycle is finished. On the second load, a Load Most Significant Half (LDMSH) of the DMF Data Register (Sheet 1) is generated. This is the LDMSH0 signal (12H8) that is ORed (11M4) to actually load the register. Note that there is a load at the same time as the address load but it is of no significance because it is written over by the second one. The second load also toggles the Stage B flip-flop of Counter D (CTD B) (12F8). This enables the third load to set the Write Buffer Full flip-flop (WRTBUF) (12K8) and load the Least Significant Half (LDLSH) of the DMF Data Register with the LDLSH0 signal.

EHOLD0 (11M6) goes high now and the memory access is started. The EDMA Address register (DADxx) is put on the LMB by enabling the multiplexors (Sheet 3) with the DATTM1 signal as described in the CPA write to Local Memory, and selecting the DADxx inputs with the EFB0 signal from the Memory Contention circuit indicating that the EDMA is in control of the Local Memory Bus.

The remainder of the operation is the same as for CPA writes to Local Memory except that the data multiplexors to the LMB are selecting the DMF data inputs with the EFB0 signal. The Local Memory Data Strobe is generated in the same way.

The Local Memory Select flip-flop is reset with the End of Transmit signal but the operation is extended to the end of the cycle on the Local Memory Bus by the cross coupled flip-flop (13B2). This flip flop is set by LMSEL0, enabled to request memory with the DMA control bit that indicated a write, DMMC000, and reset with Cycle Complete (CYCOM). This flip-flop is another condition that delays Start of Transmit by holding the Bus Control counter with ERQWRT0 (10H3).

For halfword writes to Local Memory, Stage B of Counter D is held high by the DMMC021 signal being low. This is the control bit from the EDMA Bus, after it is stored in the register (1K8), that indicates a halfword operation when it is low. This control bit register was loaded at the same time as the address with the leading edge of LDDMC signal (12D7).

11.10 EDMA Bus Read from Local Memory (See Figure 14.)

When the LMRQ signal is sent on the EDMA Bus, the bus control circuit does not send SOT0 until the EDMA has control of the Local Memory Bus in the same manner as for an EDMA write to Local Memory.

SOT0 and LMRQ set the Local Memory Select flip-flop (12D5). The Address transfer cycle is the same as for the Write operation. The SOT0 signal initializes several circuits for the Read operation. These are the Read Buffer Full (RDBUFL) flip-flop (12C2) and the Counter E Stages A and B (12H3 and 12K4).

The gate (11K5) removes EHOLD0 when the ADRFN1 signal goes high. This occurs after the address is transferred to the DAD Registers. At this time the Read Buffer is also empty, reset by SOT0, and not in a Burst Read operation, and DMMC001 is high because it is a Read operation.

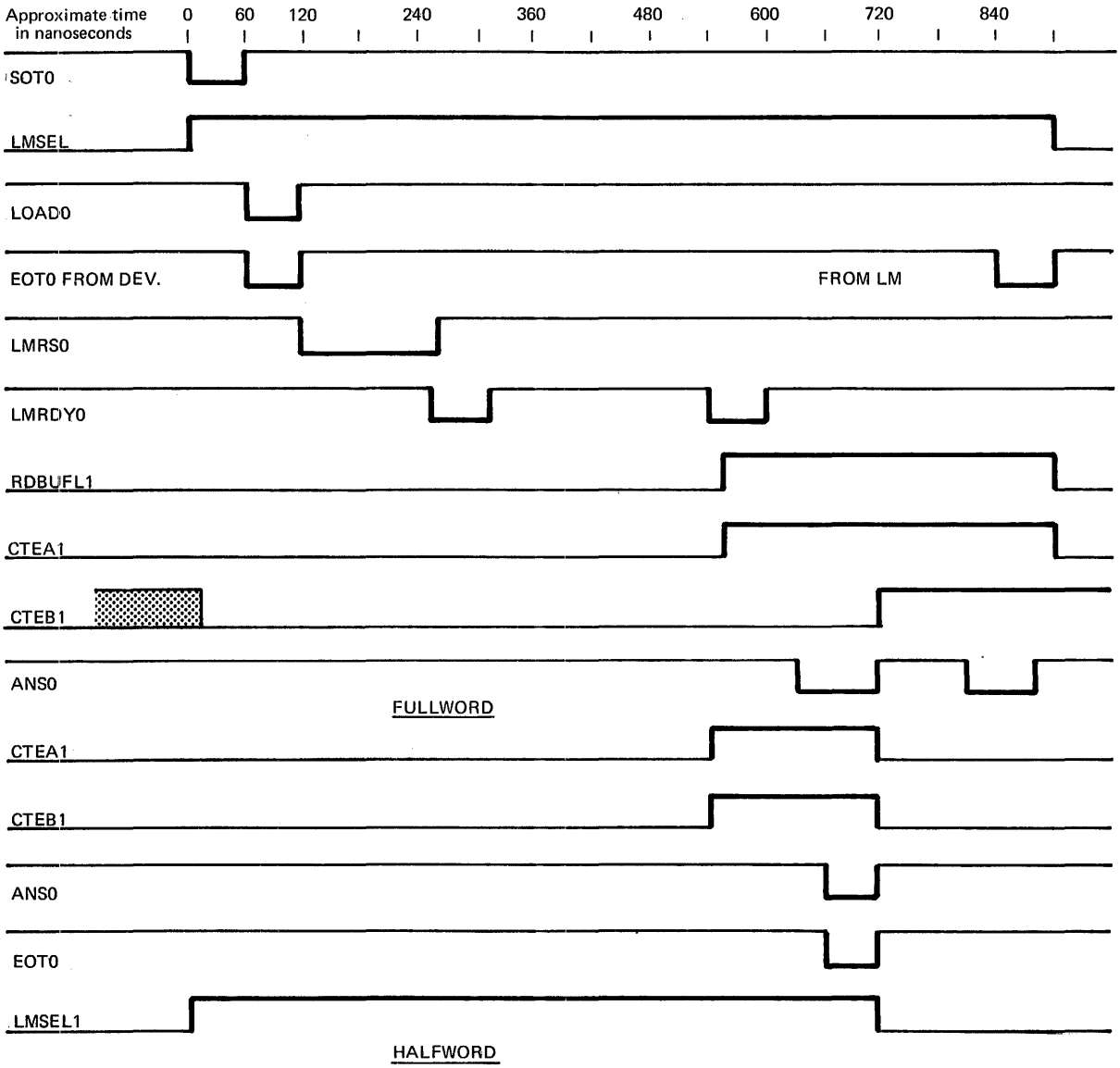


Figure 14. EDMA Bus Read from Load Memory

The memory operation of Local Memory Request Service (LMRS) and two Local Memory Readys (LMRDYs) continue as usual. The Cycle Complete (CYCOM) signal is generated as with any data read command. CYCOM0 (12B2) is ANDed with LMSEL to set the Read Buffer Full (RDBUFL). The other two inputs to the gate (12D2) are DMMC001 and RDYDAT1. These are the command bits, indicating a Read operation, and a Ready for Data signal respectively, that can be low only during Burst Read operations. This gate therefore starts the delay line controlled clock for Counter E (12H2). This circuit generates the Answers (ANSWT1) (12J2) and enables and steers the LMB register (LMF) (Sheet 2) onto the EDMA Bus. Note that Counter E Stage A enables the multiplexors (Sheet 2) and Counter E Stage B (CTE B) selects the most significant half of the LMB register first and the least significant half second. Meanwhile the EDMA transmitters (Sheet 2) are enabled with the DMA Enable signal (DMENB0). DMENB0 is generated (10E9) by the OR of Counter E Stage A (which is the controlling signal for reads at this time) or Counter B not being at Count 0 (see Sections 11.7 and 11.8).

This description has implied fullword transfers. For halfword operations, DMMC021 is low and the gate (12J3) causes Stage B of Counter E to be set on the first clock. This transfers just the least significant half of the data word.

The gates (12D4 and 12E4) generate End of Transmit (EOT0) along with the second ANS0 except when it is a Burst Read operation. This EOT0 resets LMSEL flip-flop (12D5) ending the cycle.

11.11 EDMA Bus Burst Write to Local Memory (See Figure 15.)

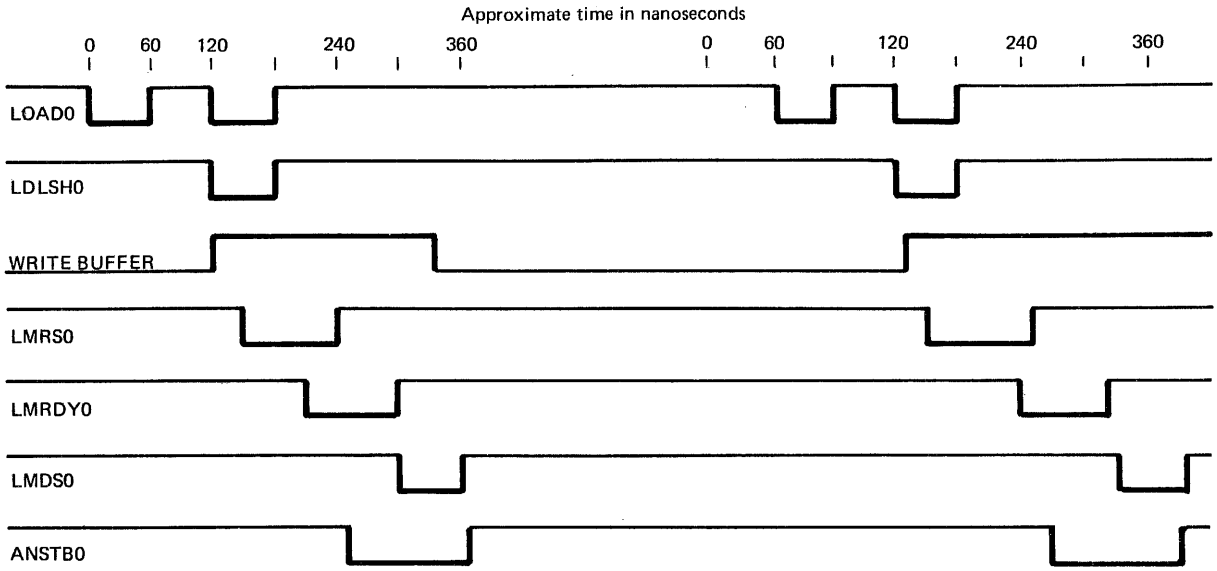


Figure 15. EDMA Burst Write to Local Memory

The Burst Write mode starts the same as the half or fullword write but continues on after the data is sent to memory.

The Burst Write mode to Local Memory operates by referring to the Write Buffer Full flip-flop (WRTBUF) (12K8). As the data is written out to Local Memory, ANSTB0 is generated (11M6) to signal the device that it may send more data. CYCOM0 resets WRTBUF when the Local Memory Data Strobe is sent out. WRTBUF is set when the LDLSH0 signal (12L8) loads the least significant half of the EDMA Data Register (DMF) (Sheet 1).

This operation continues with each CYCOM0 incrementing the EDMA address register counter (Sheet 1) with the CDMAD1 signal (11G9) until the device sends an EOT0.

11.12 EDMA Bus Burst Read from Local Memory

The Burst Read mode starts the same way as the half or fullword read. It does not send out an EOT0 with the ANS0 because of the gate at 12D5 that inhibits EOT0 when Burst Read (BRSTRD1) is decoded from the DMMC bits (12B1). The next memory access is made as soon as the Read Buffer is empty, by raising EHOLD0 (11N6) with the RDBUFL1 signal going low (11N5). The Read Buffer is emptied at the end of the data transfer to the bus.

The other controlling signal is RDYDAT1 (12D1). The flip-flop that enables this signal (12B3) is set by the LOAD0 as received from the EDMA Bus and reset as soon as CTE A is set. CTE A is Stage A of Counter E that generates the ANS0s to the EDMA Bus (12H3).

The gate (12D1) starts the clock for Counter E when the buffer is full, when the EDMA is ready for data, and when it is a Read operation (DMM001 being high). EHOLD0 is removed and the memory access started when the Read Buffer (12C2) is emptied. The operation continues until the device sends an EOT0. The MBC initiates an extra Read to Memory at this time, which is not used.

11.13 Memory Access Contention Control

Sheet 13 contains the Memory Access Contention Control logic. It handles requests from either of three inputs. These are EREQE1 (13C1), CTEND0 (13C3 and 13E8), and the Stack Request flip-flop (1305). EREQE1 is the request from the EDMA Bus and CTEND0 is the request from CPA.

These request signals are low active at the inputs to the first rank of flip-flops (Sheet 13). They also OR into the delay line (13F7). The 5 nanosecond tap on this delay line clocks the requests into the first rank of flip-flops and the 25 nanosecond tap clocks the requests into the second rank of flip-flops. It is at this second rank of flip-flops that the contention is resolved. If the EDMA or EF1 flip-flop is set it has control of the memory. The CF1 flip-flop indicates that CPA has control of the memory unless EF1 is also set. The bottom flip-flop is the Stack request flip-flop. It is the lowest priority and is reset if either the EDMA or CPA flip-flop is set.

The Stack Request flip-flop is set when CPA requests an instruction from the upper half of the stack (SSREQA0) or CPA has gone to memory for an instruction because it wasn't in the stack (CILMRS0).

CTEND0 is low (requesting the memory) when from top to bottom of the AND-OR-Invert gate (13D7) 1. ANDing M01, SD500, (CEQL0 or CEQU0), and CRQD201 – 50 nanoseconds after request to go to memory for Instruction Reads. 2. ANDing CRQD301, GTUU1, and CRQD001 – make a dummy access to memory that is not in this system configuration, to prevent Processor hang-up. 3. CI-feedback latch to store CTEND0 until CYCOM0, DMARDY0, or STKRDY0. 4. ANDing M01, IR0, and CRQD001 – Access to memory quickly if the request is to Local Memory and is not an Instruction Read.

EREQE1 is the OR of three EDMA Bus signals or states. From top to bottom (Sheet 12) they are: 1. LMREQR1 – Local Memory is Requested by the Queued device. 2. LMSEL and Burst Read code until the end of the next Cycle Complete (CYCOM). 3. LMSEL stored until next Cycle Complete and the DMMC bit that indicates a write command.

These requests are reset or at least removed during the Cycle Complete signal.

Local Memory Request Service (LMRS0) is generated at 13M7. The inputs to the AND-OR-invert gate are from top to bottom: 1. SS1 – Stack access after a delay to let the multiplexor settle. 2. Feedback to act as a flip-flop and store the request for timing elsewhere. 3. EF1 AND EHOLD0 – EDMA request and EDMA ready to access memory. 4. EF0 AND CF1 – EDMA not requesting, and CPA is requesting. The D35 signal is from the delay line at 13F7 to cover overlap of flip-flops, etc. The LMBBY0 (13F8) signal indicates that the first Ready signal has been received from the Local Memory and the address cycle is over.

12. LOCAL MEMORY INTERFACE (LMI) BLOCK DIAGRAM ANALYSIS

The LMI boards (two per system) control access to the Local Memory Modules (LMM) from the Memory Bank Controller (MBC) via the Local Memory Bus (LMB). Whenever a request is made by the MBC, the appropriate LMI sends address data and control signals to its Local Memory Modules (LMMs). Halfword and fullword data is steered to or from the LMMs according to the type of memory access. The LMI also contains the parity generation and check circuits for its LMMs.

12.1 LMI Block Diagram (See Figure 16.)

The LMI boards are idle until the Local Memory Request Signal (LMRS0) is generated by the MBC. The LMIs respond by performing a memory cycle. The memory cycle is the same for each type of memory access. They differ in the data steering required. The following steps outline a memory cycle.

1. Examine the address data on the LMB to determine which LMI should respond (refer to Section 3 on interleaved address organization).

2. Latch address and control data into registers of the correct LMI and indicate the start of the cycle by sending LMRDY0 to the MBC.

3. The LMI sends ER0 to its LMMs to begin the Read or Write cycle.

4. If the memory access is a Write operation, load data from the MBC into the write data register on the LMI, steer write data and WRT0 to the LMMs.

   If the memory access is a Read operation, accept data from LMMs and relay this data and LMRDY0 to the MBC.

5. Generate or check parity as required for the type of memory cycle. Indicate parity errors to Processor via DLMP0 and IRLMP0.

Note that if the memory access is an Instruction Read, both LMIs respond to the request (LMRS0) and each performs a memory cycle for its block of memory. This is explained in detail in Section 13.

The following paragraphs describe each functional block of Figure 16. Each block includes the pertaining schematic sheet number.

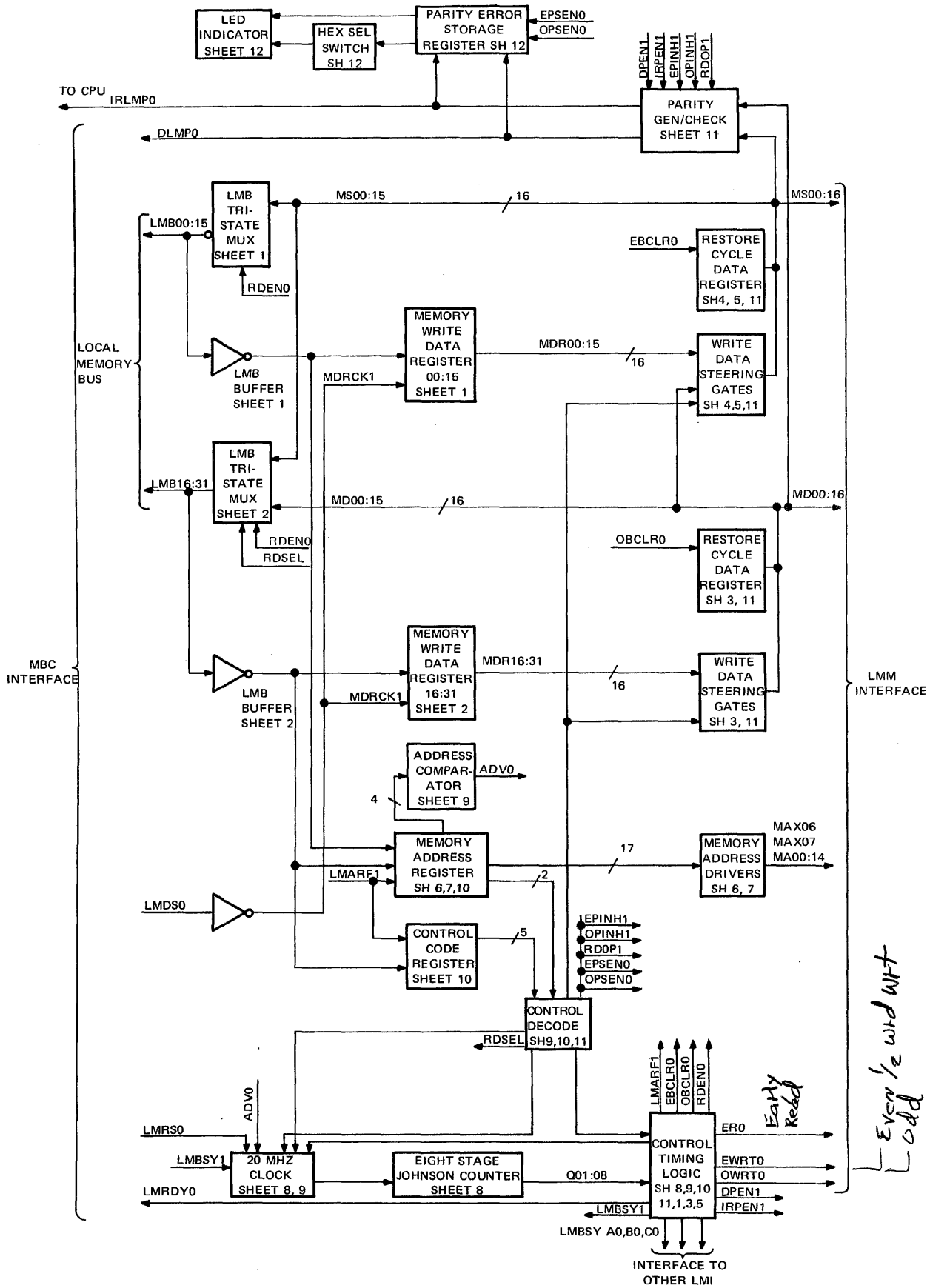


Figure 16. Local Memory Interface Functional Block Diagram

12.2 Local Memory Bus Tri-State Multiplexors

The LMI uses the LMB to transmit data from a memory Read operation to the MBC. These multiplexors serve as the LMB drivers for this function. The drivers are normally in a high-impedance state and are enabled for approximately 100 nanoseconds during a memory Read operation by RDEN0.

Note that this function is represented on the diagram as two blocks; one block drives LMB00:15, the other block drives LMB16:31. This shows the data steering function for halfword Read operations. LMB16:31 is used for transmitting all halfword format data between the MBC and LMI. These lines have two possible sources of halfword data (e.g., MS00:15 and MD00:15) corresponding to the most significant (even) halfword and the least significant (odd) halfword, respectively, within any given fullword. The correct selection of the source is made by RDSEL.

12.3 LMB Buffers

These serve to reduce the normalized load on each LMB line to one.

12.4 Memory Write Data Register

The Memory Write Data Register (MDR) receives data from the LMB for use in memory Write operations only. Data is strobed into the register by MDRCK1, which is the buffered and control gated back panel signal LMDS0. The MDR is shown divided into two blocks, and all data for halfword Write operations is stored in MDR16:31.

12.5 Read Data Register

The Read Data Register is used to store the memory module output data during a Read operation. This is required under two conditions; that is, during any Read operation, when the registers function as described previously, and during a halfword Write operation, when one LMM is being written into while the second is not. Recalling that two Local Memory Modules (LMMs) are cycled in parallel whenever the LMI is active, a halfword Write operation requires that the module which is not being written into be cycled through a Read operation, leaving its data unchanged.

The Read Data Registers are normally in a tracking mode and follow the data lines. They are latched by the EBCLR0 and OBCLR0 control signals when the Local Memory Module (LMM) output data becomes valid.

12.6 Write Data Steering Gates

This block steers data to the correct LMM during memory Write operations. Note that the steering gates for the even halfword (MS00:15) have two possible sources of data. MDR00:15 is selected for a fullword Write operation. MDR16:31 is selected if a halfword Write operation to the even halfword is required, since all halfword write data from the MBC is stored in MDR16:31. Write data steering is controlled by four signals called WTE00:03. All Write Data Steering Gates are disabled for memory Read operations.

12.7 Memory Address Register

The Memory Address Register (MAR) stores the 19-bit memory address provided by the MBC. The devices used in the MAR are the tracking latch type, permitting the address to be quickly relayed to the Local Memory Modules (LMMs). It should be noted that the MAR does not latch up an address unless that particular LMI is required to respond to it.

12.8 Memory Address Drivers

The Memory Address Drivers are high current devices used in conjunction with terminated memory address lines to provide good transmission characteristics on these lines. This becomes important in systems that have additional memory located in a separate chassis.

12.9 Control Code Register

The Control Code Register (CCR) works in the same way as the MAR, and is used to store the 5-bit control code that identifies the type of memory access to be made (see Section 8).

12.10 Address Comparator

The Address Comparator takes the four most significant bits of the address from the MAR and compares them against an upper and lower address limit for that LMI which is selected by a strapping feature. The address must be within the allowed limits for the comparator to generate ADV0, which allows the control clock to start a memory cycle.

12.11 Control Decode Logic

The Control Decode Logic accepts the 5-bit control code stored in the CCR, the two least significant bits of the address stored in the MAR, and generates all the combinatorial logic outputs required for LMI control. The more important signals are shown on the block diagram.

12.12 Clock

The Clock is a gated 20 MHZ square wave oscillator that provides the time base for operation of the LMI and control of the Local Memory Modules (LMMs). Operation of the clock is conditional on LMRS1, ADV1, STCLKA1, and STCLKB1 all being valid.

12.13 Counter

The Counter is an eight stage Johnson Counter driven by the 20 MHZ clock described previously. The outputs of its eight stages are decoded to provide directly the signal timing needed within the LMI and LMMs.

12.14 Control Timing Logic

The Control Timing Logic accepts the output from the Counter and Control Decode blocks as inputs and develops all time based control signals required by the LMI and the Local Memory Modules (LMMs). In addition, the Control Timing logic block controls the synchronization of two LMIs for the instruction read cycle. The important signals are shown on the block diagram.

12.15 Parity Generation and Check

The parity logic generates the parity bits during Write operations and checks for correct parity during Read operations. One parity bit is provided for each halfword of memory.

If a parity error is detected during a Read operation, the parity logic signals the Processor via IRLMP0 or DLMP0 (in Model 8/32), which indicates parity error in an Instruction Read, or parity error in a data read, respectively. These two signals are OR tied on the back panel and are called DMPF0 on Models 8/32C and 8/32D.

12.16 Parity Error Storage Register

During a parity fail indication (IRLMP0 or DLMP0), the Parity Error Storage Register determines which of the Local Memory Modules (LMMs) being accessed is the source of the parity error and sets a flag to identify that module. The parity error storage register can monitor up to 16 Local Memory Modules (LMMs), which is the maximum number that one LMI can accommodate.

12.17 Hexadecimal Selector Switch and LED Readout

These two blocks are used to read out the contents of the Parity Error Storage Register and determine which of the Local Memory Modules (LMMs) is the source of the parity errors received.

13. LMI DETAILED FUNCTIONAL AND TIMING DESCRIPTION

This section describes in detail the timing of all memory operations referencing Functional Schematics 35-534D08. The reader should be familiar with Sections 1 through 9 before reading this section. The timing given here is for a system using 750 nanoseconds cycle time with 32 KB memories, and assumes that the memory being accessed is not busy when the request is initiated. Timing differences required by other memory modules is explained in Section 13.5.

13.1 Fullword Write (See Figure 17.)

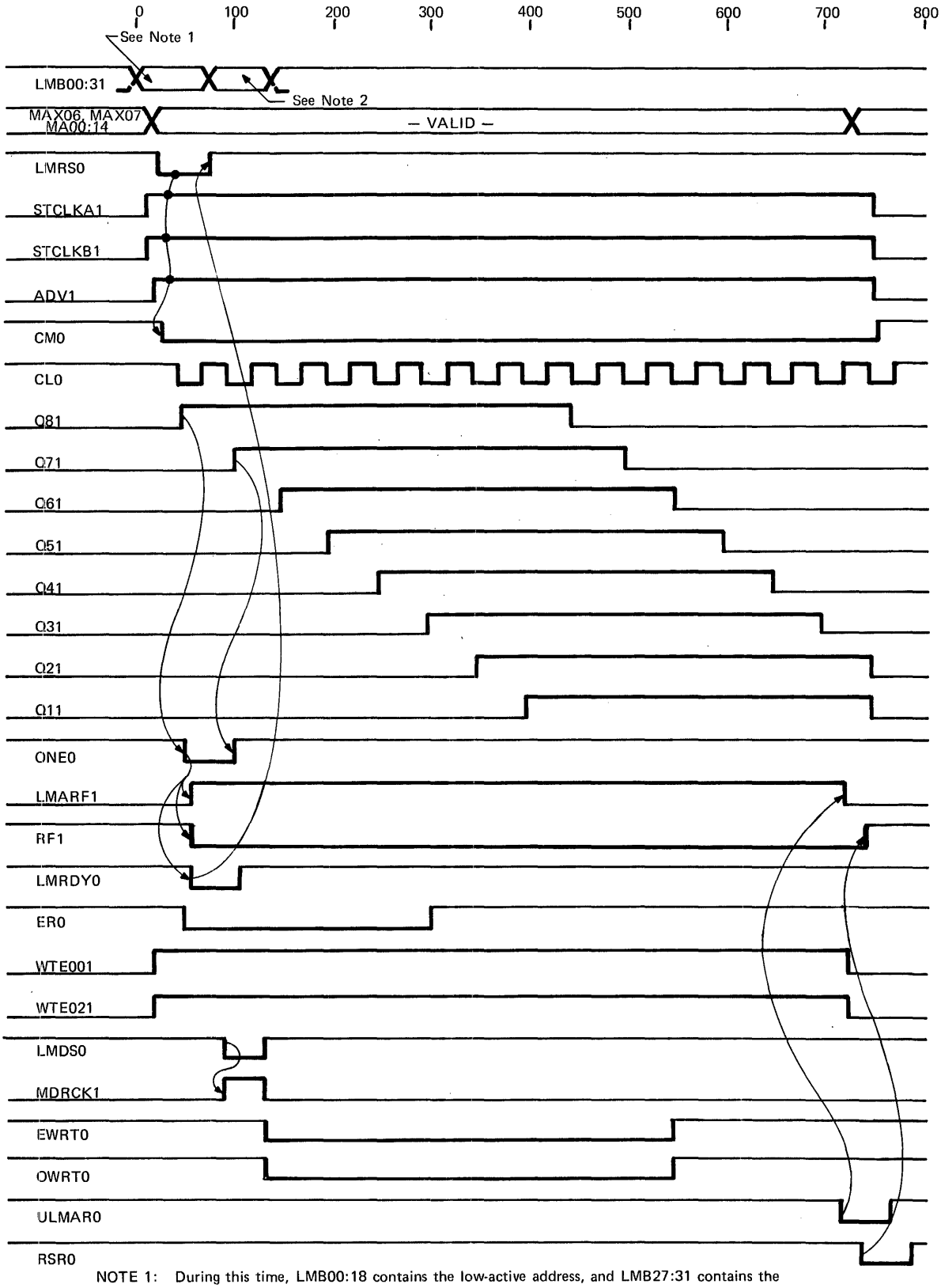
A fullword Write operation begins with address and control data being placed on the LMB by the MBC. The memory address, in low-active polarity, is placed on LMB Lines 00:18; while the 5-bit control code is placed on LMB27:31 in high-active polarity. LMB polarity is thus mixed at this time. Approximately 20 nanoseconds after the LMB data is valid, the MBC generates LMRS0 and holds it low waiting for the LMI to respond.

The 17 most significant bits of the memory address pass through the address tracking latches (Sheets 6 and 7) and are transmitted via the MA Bus to the Local Memory Modules (LMMs). The four most significant bits are also routed to the address comparator (9J3) where they are compared against the prewired upper and lower address limits for the LMI. If the ADRS is within limits, ADV0 (9R3) goes low, forcing ADV1 (8L3) high.

If Bit 18 of the 19-bit address is in the correct state, as determined by a strap at 10F8, FWD0 (10J8) goes low, forcing STCLKA1 (8K2) high. Bit 18 determines which of the two LMIs controls the fullword location desired, since the LMIs are interleaved on fullwords. The Control Decode Logic decodes INSRD1 (9C2) as low, since this is not an Instruction Read operation. This forces STCLKB1 (8K3) high.

Since the MBC is holding LMRS0 low, LMRS1 (8F1) is high, and LMRS1, STCLKA1, STCLKB1, and ADV1 sets CM0 (8N2) low. CM0 starts the clock running (8B5) and the buffered clock output CL0 (8C5) drives the eight stage Johnson Counter (Sheet 8), which is triggered by the clock's negative going edge.

Two features of the counter are: a self-start feedback decode (SSFB0) (8R5) which is used in conjunction with a complete decode of one counter state (9B2) to assure that the counter does not lock into an undesired sequence of states, and its modified interconnection of stages Q21 (8M6) and Q11 (8N6) which causes the counter to have only 15 states, instead of the normal 16 (see Timing Diagram, Figure 17).



NOTE 1: During this time, LMB00:18 contains the low-active address, and LMB27:31 contains the high-active control code.

NOTE 2: During this time, LMB00:31 contains 32 bits of high-active data.

Approximate time in nanoseconds

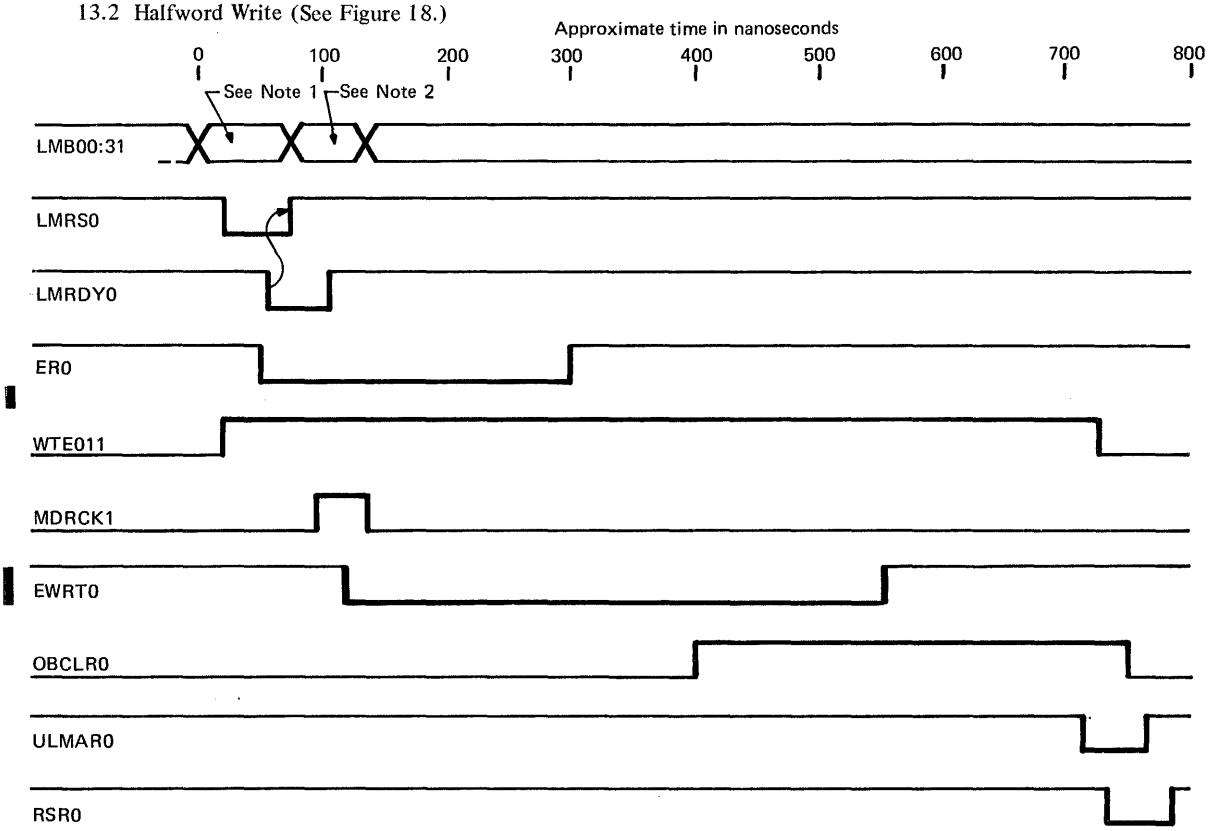
Figure 17. Fullword Write Timing

The first clock edge causes ONE0 (9F3) to be generated, which in turn sets LMARF1 (10C1) high and RF1 (8A2) low. LMARF1 latches the address and control data into the Memory Address Register (MAR) and Control Code Register (CCR) respectively. RF1 keeps STCLKA1, STCLKB1, and ADV1 high, while its complement, RF0 (8C2), latches the Local Memory Request flip-flop (8D2) in the high state. These insure that CM0 remains low-active for the duration of the memory cycle. In addition, ONE0 causes LMRDY0 (9K2) to be sent back to the MBC. Upon receipt of LMRDY0, the MBC releases LMRS0. The first clock edge also causes ER0 (8F9) to be sent to the Local Memory Modules (LMMs), thus beginning the memory access cycle.

The MBC places 32-bits of high active data on the LMB to be written into memory. It sends LMDS0 to the LMIs which becomes MDRCK1 (1R6) and strobes the data into the Memory Data Register (MDR00:31) (Sheets 2 and 3). In the interim, WTE001 (10L2) and WTE021 (10L3) go high, steering the data to the MS and MD Busses (Sheets 3, 4 and 5) and into the memory modules. Approximately 100 nanoseconds after the leading edge of ER0, EWRT0 (9G6), and OWRT0 (9G5) send the Local Memory Modules (LMMs) into the write mode. The LMMs accept the write data on the MD and MS busses and store it into the memory location.

After the write cycle is completed, ULMAR0 (9R8) unlatches the Memory Address Register (MAR) and the Control Code Register (CCR), allowing address and control data for a new memory cycle to be accepted. Approximately 20 nanoseconds later, RSR0 (9G1) resets RF1 high, which unlatches the Local Memory Request flip-flop and frees STCLKA1, STCLKB1 and ADV1 for a new cycle. The timing of RSR0 is such that CM0 goes high and disables the clock when the counter is in the clear (all low) state, thus leaving the control logic ready to begin another cycle.

13.2 Halfword Write (See Figure 18.)



NOTE 1: During this time, LMB00:18 contains the low-active address, and LMB2?.31 contains the high-active control code.

NOTE 2: During this time, LMB16:31 contains the 16 bits of high-active data.

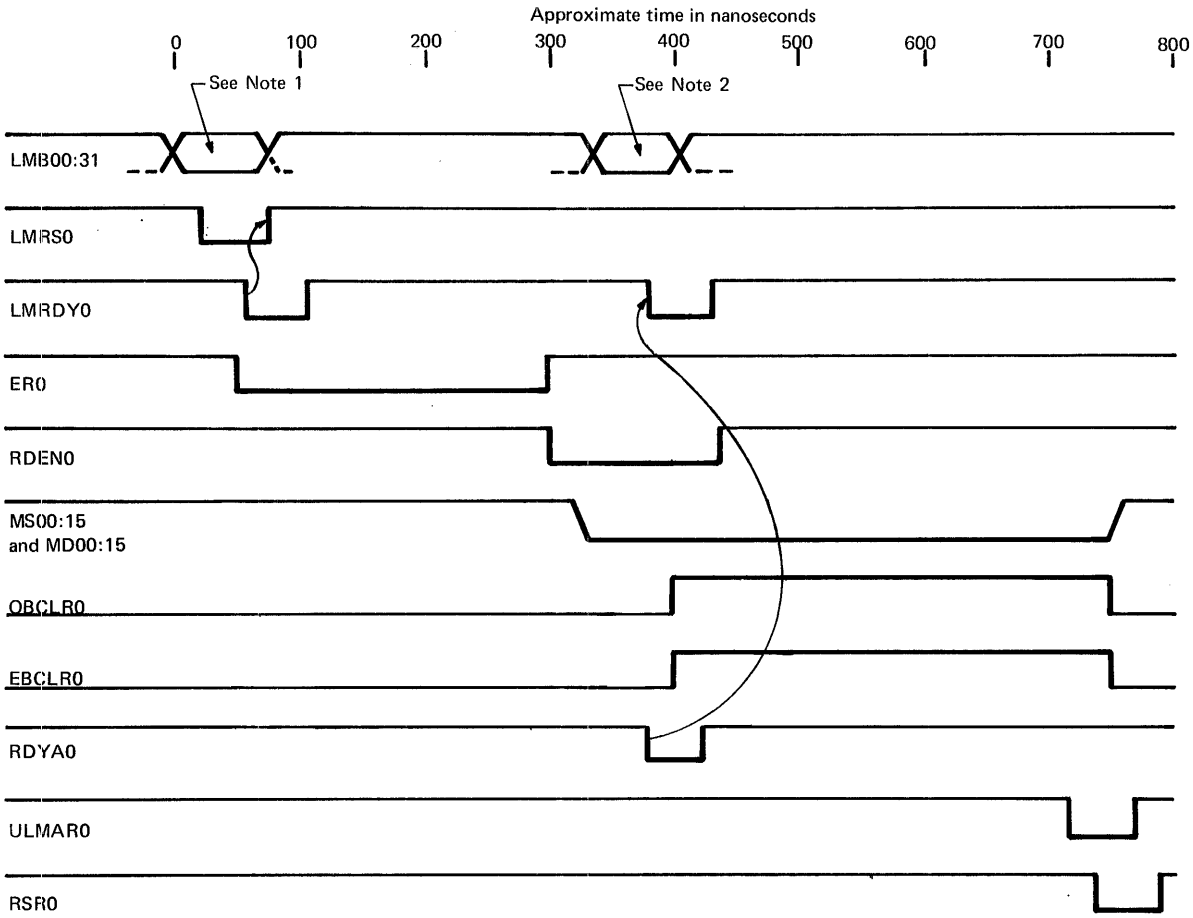
Figure 18. Halfword Write Timing (Most Significant Halfword)

The halfword Write operation is very similar to a fullword write; the difference is essentially in steering the halfword of data from the LMB to the appropriate Memory Module Bus (MS or MD) and restoring the data in the other unmodified halfword of the fullword actually being accessed. (A LMI board always accesses two Local Memory Modules in parallel. When a halfword operation is specified, the other, unused, halfword of the accessed location must remain unchanged.) This section describes a halfword write into the most significant (even) halfword. A least significant (odd) halfword write may be extrapolated directly from the description.

The halfword write cycle begins the same as a fullword write. The description in Section 13.1 up to and including the generation of ER0 applies here. After the receipt of LMRDY0, the MBC places the 16-bits of high-active data on LMB16:31 and sends LMDS0 which becomes MDRCK1(1R6) and strobes the data into MDR16:31 (Sheets 1 and 3). (All halfword data transmitted over the LMB is placed on LMB16:31.) WTE011 goes high and steers the data in MDR16:31 out to MS00:15 (Sheets 4 and 5). WTE001 and WTE021 remain low. Approximately 200 nanoseconds after the leading edge of ER0, EWRT0 (9G6) is generated, inhibiting the data currently stored in the most significant halfword from also being placed on MS00:15. Approximately 350 nanoseconds after the leading edge of ER0, OBCLR0 (3L8) goes high, allowing the data read out of the least significant halfword to be stored in the Restore Cycle Data Register flip flops of MD00:15 (Sheet 3).

After the write phase is completed, ULMAR0 (9R8) and RSR0 (9G1) reset the LMI for the start of another cycle as described in Section 13.1.

13.3 Fullword Read (See Figure 19.)



NOTE 1: During this time, LMB00:18 contains the low active address, and LMB27:31 contains the high-active control code.

NOTE 2: During this time, LMB00:31 contains 32 bits of high-active data.

Figure 19. Fullword Read Timing

The Fullword Read cycle begins like a fullword write. The description in Section 13.1, up to and including the generation of ER0, is applicable here. After the receipt of LMRDY0, the MBC releases the LMB and waits for the LMI to respond with data. Approximately 250 nanoseconds from the leading edge of ER0, RDEN0 (IA8) goes low active, enabling the 2:1 multiplexors which serve as LMB drivers (Sheets 1 and 2). RDSEL (10K5) is low, which steers MS00:15 onto LMB00:15 and MD00:15 onto LMB16:31 (Sheets 1 and 2). The output data from the Local Memory Modules (LMMs) appears on MS00:15 and MD00:15 no later than 275 nanoseconds from the edge of ER0, and is steered to the LMB as described previously. At 325 nanoseconds from ER0 another LMRDY0 pulse (9K2) is generated by RDYA0 (9G3) which indicates to the MBC that data is valid on the LMB. The Read/Write registers located on each LMM automatically provide the restore phase of the Read cycle.

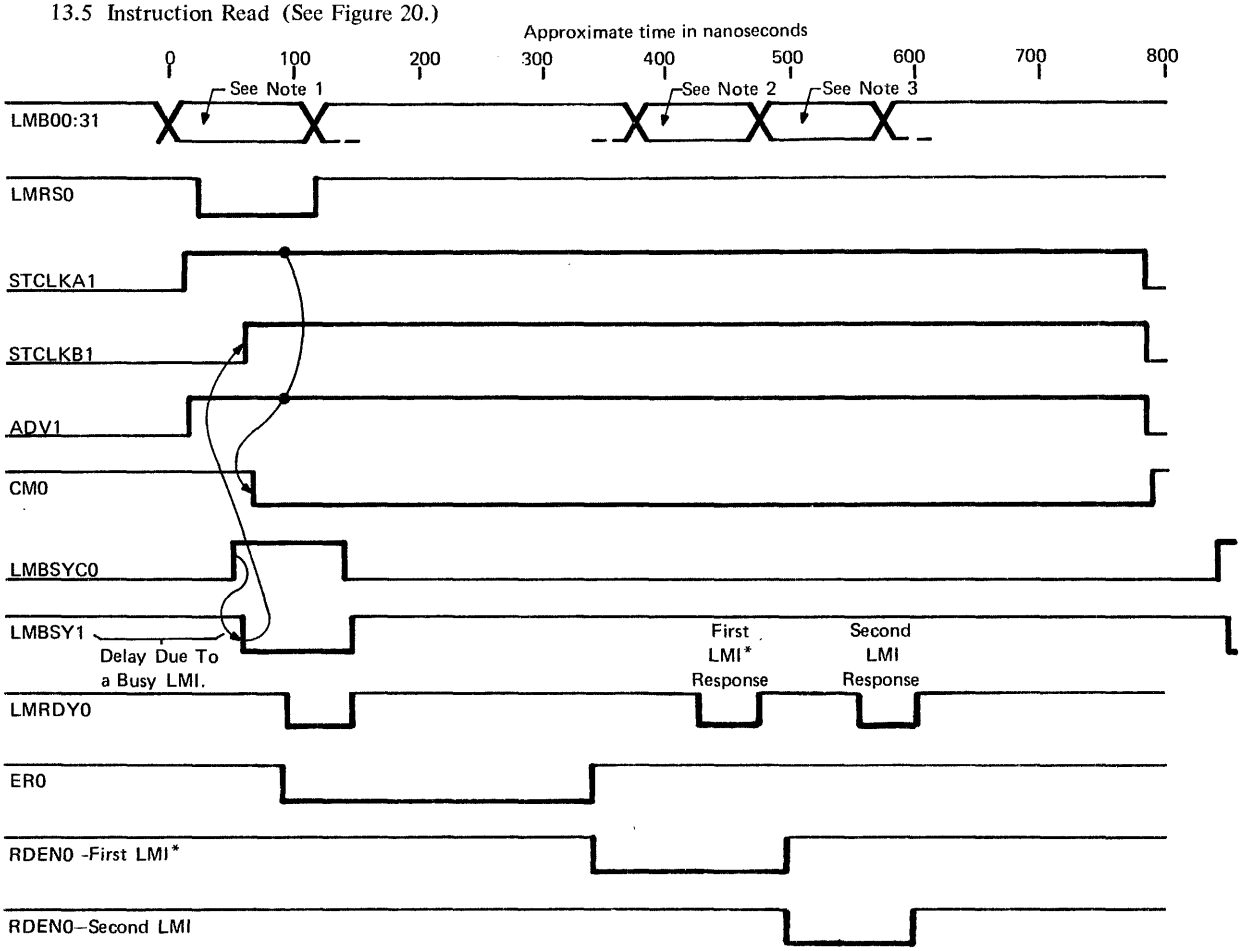
After the write phase is completed, ULMAR0 (9R8) and RSR0 (9G1) reset the LMI for the start of another cycle as described in Section 13.1.

13.4 Halfword Read

In all halfword Read operations, the requested halfword is placed on LMB16:31 (Sheet 2). A halfword read cycle to access the least significant (odd) halfword in a fullword is identical to the fullword read cycle described in Section 13.3. The MBC is this case only uses the data on LMB16:31.

In a halfword read cycle to access the most significant (even) halfword, RDSEL (10K5) is high. All other details of the cycle are identical to a fullword read (Section 13.3). The MBC in this case only uses the data on LMB16:31.

13.5 Instruction Read (See Figure 20.)



* The first LMI controls the address containing the instruction halfword requested by CPA.

Note 1: During this time, LMB00:18 contains the low active address, and LMB27:31 contains the high active control code

Note 2: During this time, LMB00:31 contains a fullword of data from the first LMI.*

Note 3: During this time, LMB00:31 contains a fullword of data from the second LMI.

Figure 20. Instruction Read Timing

The Instruction Read operation is a double fullword (64-bits) read, in which both LMI boards cycle in parallel and each sends a fullword over the LMB in sequence. Two important features of LMI operation during this type of request are: 1. Both LMI boards must be quiescent (i.e., not cycling) before the operation can begin, and 2. The first of the two fullwords of data sent to the MBC contains the instruction halfword requested by CPA.

This cycle begins with address and control data placed on LMB00:18 and LMB27:31 respectively, followed by LMRS0 from the MBC (see Section 13.1 for details). INSRD0 (9E2) goes low, forcing STCLKA1 (8K2) high. If the address is within range, ADVI (8L3) goes high. Since INSRDI (9C2) is high, STCLKB1 (8L3) does not go high unless LMBSY1 (9G8) is low. As shown in Figure 21, LMBSY1 does not go low unless LMBSYC0 (9H8) from both LMIs is high, indicating that both LMI boards are quiescent. This ensures that the LMI boards will cycle in parallel. When LMBSY1 goes low, STCLKB1 goes high. CM0 (8B5) is forced low and starts the clock, and each LMI begins a fullword Read operation.

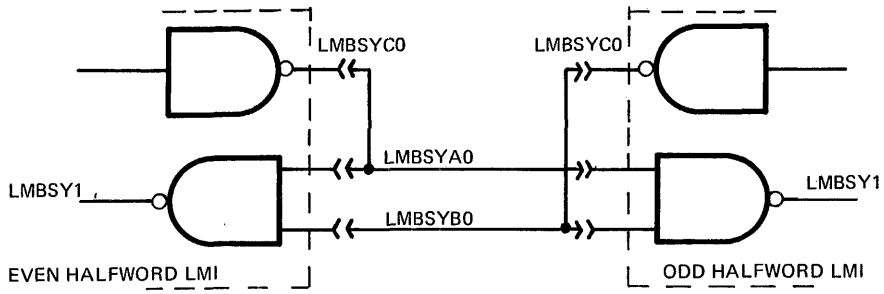


Figure 21. LMBSY1 Logic

The LMI that controls the address containing the instruction halfword requested by CPA completes a normal fullword read cycle as described in Section 13.3. Thus, RDEN0 (1A8) goes low 250 nanoseconds from the leading edge of ER0 (8F9). This is followed by a fullword of data not later than 275 nanoseconds from the leading edge of ER0, and LMRDY0 (9K2) generated by RDYA0 (9G3) logic 325 nanoseconds from the leading edge of ER0.

The other LMI also completes a fullword read cycle, but delays placing the data on the LMB as follows: data is received on MS00:15 and MD00:15 not later than 275 nanoseconds from the leading edge of ER0 as before, but RDEN0 does not go low until 400 nanoseconds from ER0, at which time the fullword of data is gated to the LMB (note that RDEN0 in the first LMI has gone high, disabling the outputs). This is followed by a LMRDY0 pulse at 450 nanoseconds from ER0, generated by RDYB0 logic (9E4). Data from each of the two LMI boards is received, a fullword at time, spaced by 125 nanoseconds.

13.6 Parity Generation and Checking

Parity bits MS160 and MD160, correspond to the most significant (even) halfword and least significant (odd) halfwords respectively. The parity bit is generated whenever its corresponding halfword is written. When a Write operation is initiated, the parity generator/checker integrated circuits (11C7) used for the halfwords being written into are enabled via EPINH1 (11D1) and/or OPINH1 (11C7) (e.g., on an even halfword write, only EPINH1 goes low and enable the I.Cs. The data on MS00:15 or MD00:15 generates EPGEN1 or OPGEN1 respectively, which is gated onto MSI60 or MDI60 by WTE031 (11H1) and written into memory. If the operation is only a halfword write, the parity bit of the other halfword that is accessed is read out of memory, latched into the open-collector flip-flop of that line (11J3 for MS160, 11K6 for MD160) and rewritten into memory.

In a Read operation, the parity bit for each halfword is read out of memory and latched into the open-collector flip-flops of MS160 and MD160. As with parity generation, only the parity generator/checker integrated circuits used for the halfwords being requested are enabled with EPINH1 and/or OPINH1. RDOP8 (I0H2) goes high, allowing the parity bit as well as the data bits to be checked. A parity error in one of the halfwords is indicated by EPERR0 (IIH4) or OPERR0 (IIG6). These are ORed to become PERR1 (IIJ4), which is then gated by either IRPEN1 (IIJ4) or DPEN1 (IIJ3) to become IRLMP0 (Instruction Read Parity Error) or DLMP0 (Data Read Parity Error) respectively. Both IRLMP0 and DLMP0 are 50 nanosecond pulses that occur approximately 400 nanoseconds from the leading edge of ER0.

14. MEMORY SYSTEM TEST FEATURES

14.1 Parity Error Source Indicator (LMI)

The Parity Error Source Indicator (Sheet 12) detects the occurrence of a parity error (DLMP0 or RLMP0) and sets a flag to indicate which of the 16 Memory Modules controlled by the LMI is the source of the data causing the parity failure. The occurrence of DLMP0 or IRLMP0 causes the flip-flop (12N1) to be set, lighting the LED (12R2). The control logic (Sheet 12) resolves the source of the parity error to the particular halfword (hence the particular Memory Module) from which the erroneous data was received. This causes EPSEN0 (12J6) or OPSEN0 (12J8) to go low, depending upon whether the error source was an even or odd halfword respectively. MPI (12J6) goes high if either DLMP0 or IRLMP0 are activated. When all three enable inputs on a 3 to 8 decoder (12K7) are activated, it decodes the three Most Significant Address Bits; ML001, MLX061, and MLX071 (12J6) and the corresponding PDXX0 (12L7) output goes low. This sets one of the 16 flag flip-flops (Sheet 12).

To find the source of an error, a Hexadecimal switch (12K4) is rotated so that its outputs select one input at a time to the two 8 to 1 multiplexors (12E3), which turns ON an LED (12J2) whenever the selected flag flip-flop is set. The Hexadecimal switch positions correspond to Memory Module locations as shown in Figure 22. The module that is the source of a parity error turns ON the LED (12J2) when the hexadecimal switch is at that module's position.

In a system using 64KB Memory Modules, a maximum of eight modules are connected to each LMI and the Hexadecimal switch positions correspond to Memory Modules as shown in Figure 23.

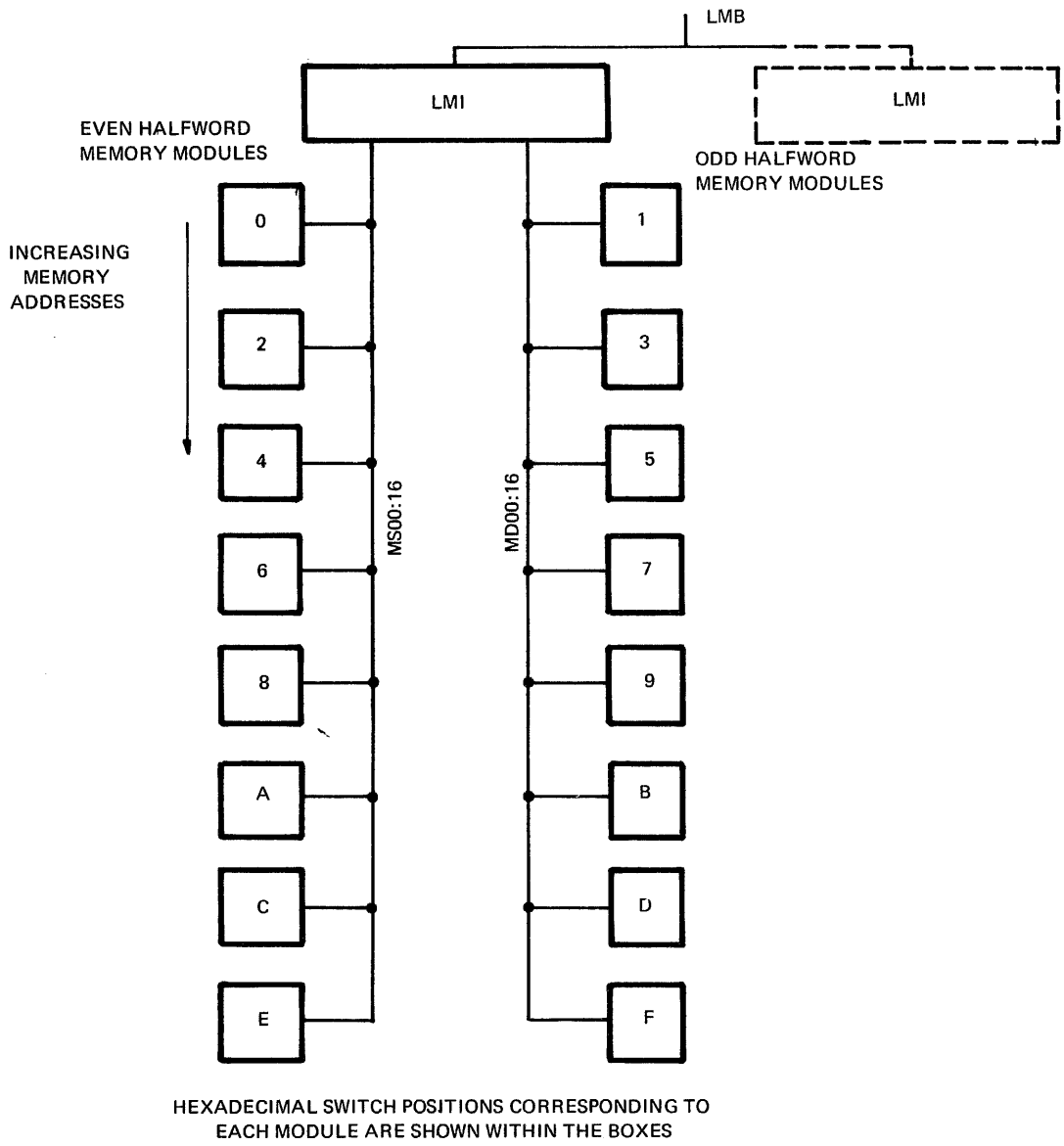
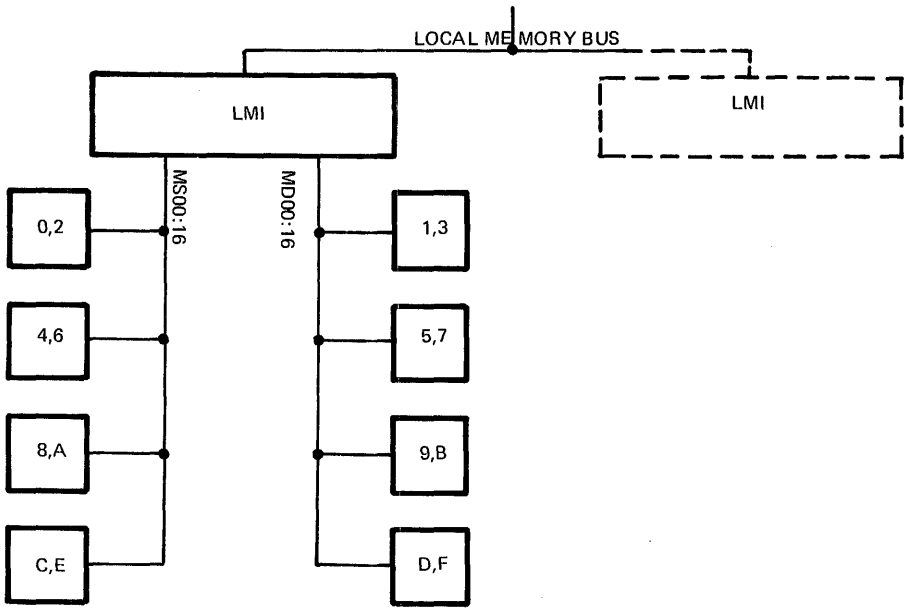


Figure 22. Parity Error Source Indicator — Hexadecimal Switch Positions for 32KB Modules



HEXADECIMAL SWITCH POSITIONS CORRESPONDING TO EACH MODULE ARE SHOWN WITHIN THE BOXES.

Figure 23. Parity Error Source Indicator – Hexadecimal Switch Positions for 64KB Memory Modules

14.2 Force Parity Error Strap (LMI)

A strap (11F5) is provided on the LMI which, when installed, causes the LMI to generate a parity error on each memory read cycle. The type of access (instruction or data read) determines whether IRLMP0 or DLMP0 is activated.

MEMORY SYSTEM TEST PROGRAMS

The following test programs are recommended to check the Memory System operation:

1. 06-156	Memory Test Program Parts 1, 2, and 3	This program checks all available memory in various ways, using only the CPU port of the MBC.
2. 06-159	System Exerciser	This program checks the EDMA port of the MBC and operates it in contention with the CPU port. This program requires an ESELCH.

16. TROUBLESHOOTING

16.1 Extender Board Operation

Use of the 28-015 Extender board allows convenient troubleshooting of the Model 8/32 Main Memory. It allows extended operation of the MBC or either LMI. To operate any board on the extender, the extender board must be plugged into the chassis slot corresponding to that board. Only one board should be extended from the chassis at a time.

NOTE

In order to operate the MBC on an extender a 35-597 Extender Board Terminator must be plugged into the spare slot of the extender board.

16.2 Troubleshooting Checks

If trouble develops and the memory system is suspect, the following checks are recommended:

1. Check for proper seating of all boards and cable connectors.
2. With the Power switch ON, measure P5, P16, and N16 on all memory chassis.
3. If parity errors are the source of the problem, check the LMI Parity Error Source Indicators to determine if the problem is isolated within a particular Memory Module, i.e., possibly a defective module.
4. Check for correct data and control (handshaking) between the MBC and the LMI boards. This usually isolates the problem to either the MBC or the LMI boards and Memory Modules.
5. If the problem only occurs for one particular state of the fullword address bit, it is associated only with the corresponding LMI and its memory modules. If, in addition, the problem is also restricted to one state of the halfword bit, then it is associated with only one LMI and one bank of memory modules (see Section 3).

16.3 Timing Adjustment

A timing adjustment is performed on all LMI boards at the factory to set the speed of the control logic clock. If the clock driver IC or the delay line in the clock circuit is replaced on an LMI board, the clock should be readjusted via the strap at board location 14D as follows (see schematic location 8C3):

1. Place a strap between Pins 14D05 and 14D15.
2. Place Processor in any memory access loop that continually cycles that LMI.
3. Measure clock period signal CL0 on Sheet 8D5 at the second clock pulse or later (not the first pulse) and adjust strap until the period is 49.5 to 51.5 nanoseconds.

17. INSTALLATION

Mechanical installation of Model 8/32 memories is covered by the 8/32 Customer Installation Manual, 29-526, and of the 8/32C and 8/32D memories by the 8/32C and 8/32D Customer Installation Manual, 29-537. After the equipment is mounted and connected, the following checks should be performed:

1. Unplug all Main Memory System boards (MBC, LMIs, and LMMs)
2. Adjust the power supply voltages as follows:

   P5 to +5.0 Volts
   P15 to + 16.5 Volts
   N15 to – 16.5 Volts
3. Power down and plug in all boards
4. Power up again and check voltages; readjust if necessary
5. Run Memory Test 06-156.

18. MAIN MEMORY SYSTEM MNEMONICS

The following lists provide a brief description of each mnemonic found in the memory system. The source of each signal on functional schematic 35-535D08 (MBC) and 35-534D08 (LMI), is also provided.

18.1 8/32 Memory Bus Controller (MBC) Functional Schematic 35-535D08.

MNEMONIC	MEANING	SCHEMATIC LOCATION
ADRFN1	Address cycle of EDMA transfer finished	12J9
ANS0	EDMA Bus Answer	5J2
ANSR1	Answer Received	5G1
ANSTB0	Answer signal to transmitters–B input	11N6
ANSWT1	Answer to EDMA bus transmitter	12J2
BRSTWRT1	Burst mode write decode of EDMA	11M6
BURSTRD1	Burst read decode of DMA control bits	12C1
C28EB0	CPA address Bit 28 equal to upper address in stack	8J8
CA120:300	Control Address lines from CPA	Sheet 6
CAF120:300	Control Address flip-flops address register zero output	Sheet6
CAF121:151	True side of Control Address flip-flops	Sheet 6
CCYCOM0	C Selected and Cycle Complete	13C6
CD000:310	Control Data lines to/from CPA	Sheet 4
CDMAD1	Clock DMA address register	11G9
CEQL0	CPA address equal to lower address in stack	8K9

MNEMONIC	MEANING	SCHEMATIC LOCATION
CEQU0	CPA address equal to upper address in stack	8R9
CF1/0	CPA select flip-flop in memory contention circuit	13F3
C1/0	CPA selected in memory contention circuit buffered	13K3
CILMRS0	CPA access to memory with instruction read and local memory request service	14G5
CLK1A	Clock to EDMA Bus control counter	10F1
CLK1B	Clock to counter B	10E6
CMC000:020	Control Memory control code from CPA	Sheet 11
CRDY0	C Ready signal to CPA	14S8
CREQ0	Control Request from CPA	6G6
CREQF 1/0	Control Request flip-flop	6A1
CRQD 001 101 201 301 501 601	CPA Request Delayed 00, 10, 20, etc. nanoseconds	Sheet 14
CTAA1	Counter A Stage A	10J2
CTAB1	Counter A Stage B	10N2
CTAC1	Counter A Stage C	10L2
CTBA1/0	Counter B Stage A	10E6
CTB000	Counter B not at count time zero	10C8
CTBB1/0	Counter B Stage B	10F6
CTDA1/0	Counter D Stage A	12G6
CTAD1/0	Counter A Stage D	10J1
CTDA1-LMSEL	Counter D Stage A and local memory selected	12H6
CTEA1/0	Counter E Stage A	12J3
CTEB1/0	Counter E Stage B	12L4
CTFA1	Counter F Stage A	11E4
CTFB1/0	Counter F Stage B	11G4
CTFC1/0	Counter F Stage C	11B4
CTFCLK	Counter F Clock	11C1
CTMOUT0	CPA Request Time out	14N2
CXREQ0	CPA Request to EDMA	9N5
CYCOMB0	Memory Cycle complete buffered	11G9
C28EA0	CPA address Bit 28 equal to lower address in stack Bit 28	8J9
D28EA0	DMA address Bit 28 equal to lower address in stack Bit 28	8E8
D28EB0	DMA address Bit 28 equal to upper address in stack Bit 28	8E9
D35	Memory contention request delayed 35 nanoseconds	13G6
DA000	Data strobe delay line output 00 nanoseconds	11K8
DA300	Data strobe delay line output 30 nanoseconds	11K8

MNEMONIC	MEANING	SCHEMATIC LOCATION
DA700	Data strobe delay line output 70 nanoseconds	11L8
DA400	Data strobe delay line output 40 nanoseconds	11L8
DAD121:301	DMA Address register counter	Sheet 1
DATTM1	Data Time on LMB	13M9
DB700	Delay line 70 nanosecond tap	12J1
DEQ0	DMA address equal to address in stack and DMA writing to memory	14H1
DEQL0	DMA address equal to lower address in stack	8C9
DEQU0	DMA address equal to upper address in stack	8G9
DLMPF0	Data Local Memory Parity Fail	14A3
DMAACT1/0	DMA Active	10J4
DMAFW0	Fullword access from CPA to EDMA	2M9
DMA160:170	EDMA Bus	1M9
DMARDY A/B	DMA Ready—creates CRDY	11M5
DMARY0	DMA RDY to CPA	14K8
DMCA0	DMA control address time	10C7
DMENB0	Enable DMA transmitters	10E9
DMF001:311	DMA Data Register flip-flops	Sheet 1
DMMC000:020	DMA Memory Control code	1K9
DMPF0	Data Memory Parity Fail (on Model 8/32); Data or Instruction Memory Parity Fail (on Models 8/32C and 8/32D	14C4
DMT001:171	Signals to DMA Transmitter	Sheet 2
DMX120:150	EDMA Bus lines	5L2
DPF1	Data Parity Fail	14C3
DREQ1/0	CPA request to EDMA Bus	9L4
DXR121:151	DMX signal out of receiver	Sheet 5
EFB0	EDMA flip-flop in memory contention circuit-buffered	13K2
EF1/0	EDMA selected flip-flop in memory contention circuit	13G1
EHOLD0	EDMA Hold memory access	11N6
ENB0	Enable memory busy on EDMA Bus	10N8
END0	End selected condition	10N9
ENEOT1	Enable End of Transmit	10F8
EOT0	End Of Transmit	12F4
EOT0	End Of Transmit	10G9
EQ1	CPA address equal to an address in stack	14E6
EQIRC0	Equal and instruction read and CPA not still accessing memory	14F6
EREQE1	EDMA request to memory contention circuit	13E1
ERQWRT0	EDMA request and write command	13C1
GTUU1	Greater Than Unused memory lower limit	9E2
GXX1	Combination of ready signals	14K2
IR 1/0	Instruction read decode of CMC bits	11H7
IRWRT0	Instruction read or data write—ready	14K8

MNEMONIC	MEANING	SCHEMATIC LOCATION
LDADR0	Load from EDMA Bus receiver	12E7
LDDMC1	Load DMA control bit register	12E7
LDLMF1	Load Local Memory flip flops–Data Register	11G9
LDLSH0	Load Least Significant Half of DMA Data Register	12K8
LDLSH1	Load Least Significant Half of DMA Data Register	11N3
LDMSH0	Load Most Significant Half of DMA Data Register	12J8
LDMSH1	Load Most Significant Half of DMA Data Register	11N4
LDSTA1	Load Stack address register STA	14K7
LDSTK0	Load Stack	11C1
LMB271	Local Memory Bus Bit-27	11J7
LMB000:316	Local Memory Bus signals to Local Memory Interface	Sheet 3
LMBBY1/0	Local Memory Bus Busy	13G8
LMDS0	Local Memory Data Strobe	11N5
LMF000:310	Local Memory Bus flip-flops Data Register	Sheet 2
LMRDY0	Local Memory Ready	11A7
LMREQ0	Local Memory Requested	10C4
LMRS0	Local Memory Request Service	13N8
LMSEL1/0	Local Memory Selected	12D5
LMTMOT0	Local Memory Time Out	14S4
LOAD0	EDMA Bus Load	5J2
LOADR1	Load Received	5G1
LOADT0	Load signal to EDMA transmitter	10F7
M00	Same as memory zero except local memory zero active	9G8
M01	Memory Zero, Local Memory One active	9G7
M1BZR0	Memory 1 Busy from EDMA Bus receivers	9J4
M2BZR0	Memory 2 Busy from EDMA Bus receivers	9J4
M3BZR0	Memory 3 Busy from EDMA Bus receivers	9J4
MB00	Same as memory zero except buffered zero active	9G7
MSTP0A:3A	Memory Address strapping upper address of each memory most significant bit	Sheet 9
MSTP0B:3B	Same as MSTP0A:3A except next MSB	Sheet 9
MSTP0C:3C	Same as MSTP0B:3B except next MSB	Sheet 9
MSTP0D:3D	Same as MSTP0C:3C except next MSB	Sheet 9
P5RB	P5 through Resistor B	1N7
P5RX	P5 through Resistor X	8H6
P5RY	P5 through Resistor Y	9A1
P5RZ	P5 through Resistor Z	12B3
QUE0	Queue	10N3
RDBUFL1/0	Read Buffer Full	12D2
RDDAT0	Read Data	11H5
RDYDAT	EDMA Ready for Data	12D1

MNEMONIC	MEANING	SCHEMATIC LOCATION
RPC1	Receive Priority Chain	10N1
RSREQ0	Reset stack request signal	13B6
S1	Stack selected in memory contention circuit	13M5
SBSY0	Stack Busy on LMB	14C1
SCLRB0	System Clear buffered	10H9
SD1	Stack select delayed	13M5
SEL1/0	Selected (CPA)	10N6
SLMSEL0	Set Local Memory Select flip flop	12D5
SOT0	Start Of Transmit	10M4
SPECIR1	Special instruction read stored signal	14K9
SMX0	Stack multiplexor control	13J4
SS1	Stack Selected	13M5
SSREQA0	Set Stack Request	14N6
ST161:311	Stack output data	Sheet 5
STA121:281	Stack Address register bottom of stack	Sheet 7
STA280	Stack Address register LSB	7N2
STB121:271	Stack Address - middle of stack	Sheet 7
STCD0	Stack to CD lines	11C5
STHOLD	Start of Transmit Hold	10K3
STKA1/0	Valid status of half of stack that contains upper address	14M6
STKRDY1	Stack Request Ready to CPA	14J8
STWA1	Stack Write Select A	14E2
STWB1	Stack Write Select B	14C1
SQUEF1	Set Queue flip-flop	9N5
SXIR	Stack multiplexor control or Instruction read	11D6
T00A	Time Zero from delay line	10A3
T80A	Time 80 nanoseconds delayed from delay line input	10B2
WDTM0	Write Data Time	11M7
WRTBUF1/0	Write Buffer Full	12L8
XREQ0	EDMA Bus request	10A1
XX1/0	Ready to be started	10L6

MNEMONIC	MEANING	SCHEMATIC LOCATION
ADV0	Output of comparators (Sheet 9) indicating that requested address is within block of memory controlled by this LMI.	9N3
C001:021	Buffered CMC bits from CPA which are part of the control code transmitted from the MBC to LMI boards indicating CPU requests to local memory.	Sheet 10
CL0	Clock Output–pulse train drives Johnson Counter on Sheet 11.	8C6
CL1	Complement of CL0, used to time RSR0 pulse.	8D5
CM0	Cycle Memory–enables the clock and is held low throughout the memory cycle.	8N1
DLMP0	This low-active pulse is generated when an LMI detects a parity error on any operation except instruction read.	11N8
EBCLR0	Even Buffer Clear–is normally low and is asserted high during a Read operation to latch data into the Restore Cycle Data Registers for the even (most significant) halfword.	5H8
EPERR0	Asserted low-active when a parity error is detected on a Read operation from the even halfword memory bank of an LMI.	11G4
EPINH1	High active to inhibit parity generator/checking logic for even halfword memory bank of an LMI.	11D1
ER0	Early Read control signal for local Memory Modules begin the memory cycle read phase.	8F9
EWRT0	Even Halfword Write–is asserted low-active when it is desired to write into an even-address halfword.	9G6
EX1/0	Bit 4 of MBC-LMI control code which indicates an EDMA request for local memory.	10C7
FW1/0	MAR output bit which selects the LMI controlling requested address.	10E8
FWD1/0	Strap-selected level function which is low-active when this LMI is selected by FW1/0.	10G8
HEX011:041	The output of a Hexadecimal rotary switch which select a particular PFxx1 line for display on an LED.	Sheet 12
HW1/0	MAR output bit which is the least significant address bit and is used to select one of the two halfword memory banks controlled by an LMI on halfword memory operations.	10H6
ID021	An intermediate combinatorial decode used in various functions.	10H3
ID030	An intermediate combinatorial decode used in various functions.	10L4
ID041	An intermediate logical decode signal used in various functions.	9F2
INH0	Inhibit control signal of Local Memory Modules begins the restore/write phase of a memory cycle.	8H2

MNEMONIC	MEANING	SCHEMATIC LOCATION
INSRD1	Combinatorial decode indicates access is an Instruction Read.	9C2
IRLMP0	This low-active pulse is generated when an LMI detects a parity error during an instruction Read operation.	11M4
LMARF1/0	Level signal which changes mode of memory address register and control code register between tracking and latched.	10C1
LMB000:310	32 Bit wide bidirectional Local Memory Bus used to transmit data and addresses between the MBC and LMI boards.	Sheets 1 and 2
LMBSY A0 B0 C0	Three control lines used to synchronize LMI cycles for an Instruction Read (double fullword read).	9G8
LMRDY0	Ready signal from LMI to MBC indicates that LMI has responded to request and is ready to accept write data, or that read data is valid on the LMB.	9K2
LMDS0	Local Memory Data Strobe-loads data transmitted from the MBC into the MDR.	
LMRS0	Request line from MBC–indicates that MBC is requesting the memory to cycle.	8D1
MA000:140	Memory Address bits–concatenated with MAX060 and MAX070 to form the address sent from the LMI to the memory modules.	Sheets 6 and 7
MAX060 and 070	Extended Memory Address bits–see MA000:14.	
MCLR0	Memory Clear–buffered System Clear which is sent to all Local Memory Modules.	8E7
MCR0A1	Timing pulse used to control signals only when 1 microsecond cycle time local Memory Modules are used.	11N1
MCR0B0	Timing pulse used to control signals only when 1 microsecond cycle time local Memory Modules are used.	9M8
MD000:160	Memory Data–is the bidirectional data bus which transmits data between the LMI and the least significant halfword (odd) bank of Local Memory Modules (LMMs).	Sheet 3
MDR001:311	Output of the Memory Data Register which store data for memory write operations only.	Sheets 3 and 4
ML000:010	Latched Memory Address bits–output of MAR.	6C7
MLX060 and 070	Latched Extended Memory Address bits. Output of the tracking latches used for the MAR.	Sheet 8
MP1	Memory Parity Fail–high active when either DLMP0 or IRLMP0 are asserted.	12L1
MS000:160	Memory Sense–is the bidirectional data bus which transmits data between the LMI and the most significant halfword (even) bank of memory modules.	Sheets 4 and 5
MSTRP0	Timing pulse used to control signals only when 1 microsecond cycle time Local Memory Modules are used.	9M9
NULMAR0	Used to unload memory address register and control code register at the end of the cycle for 750 nanoseconds cycle time memories.	9F1

MNEMONIC	MEANING	SCHEMATIC LOCATION
OBCLR0	Odd Buffer Clear—is normally low and is asserted high during a read operation to latch data into the Restore Cycle Data Registers for the odd (least significant) halfword.	3L8
ONE0	Decode of the first state of the counter (Sheet 8) used to initiate various memory cycle signals.	9F3
OPERR0	Asserted low-active when a parity error is detected on a Read operation from the odd halfword memory bank of an LMI.	11G6
OPINH1	High active to inhibit parity generation/checking logic for odd halfword memory bank of an LMI.	11D5
OWRT0	Odd Halfword Write—is asserted low-active when it is desired to write into an odd-address halfword.	9G5
PD000:150	Each of these decoder output lines correspond to one of the up to 16 local Memory Modules than an LMI can control. A line is asserted low-active when a parity error is detected on a Read operation to its corresponding memory module.	Sheet 12
PF001:151	The 16 outputs of the Parity Error Storage register. A line is set high active when a parity error is received from the Local Memory Module that particular flip flop represents.	Sheet 12
Q010:080	Output of Counter flip-flops stages 1 thru 8 (flip-flop Q outputs).	Sheet 8
Q011:081	Same as above but complemented (flip-flop Q outputs).	Sheet 8
RDEN0	Read Enable—goes low to activate the multiplexors/drivers of the LMB on Read operations.	1A8
RDOP1	This signal is asserted high-active on any type of Read operation.	10H2
RDSEL	Selects the correct data for placement on LMB16:31 at LMB2:1 multiplexors/driver (Sheet 2). RDSEL is high for an even halfword read and low for an odd halfword or fullword read.	10K6
RF0	Complement of RF1, Captures LMRS0 in tracking latch.	8C2
RSR0	Initializes the LMI at the end of a memory cycle.	9G1
SCLR0	System Clear	8A8
SSFB0	Counter Self-Start Feedback—insures counter does not remain in an undesired stable sequence of statues.	8R5
SX1/0	Bit 5 of MBC-LMI control code which indicates an Instruction Read initiated by the look-ahead cache on MBC.	10C5
ULMAR0	Pulse to Unlatch Memory Address register and control code register at the end of memory cycle.	9R8
WTE001	This data steering signal is asserted high-active for a halfword Write operation into the most significant (even) halfword.	10L2

MNEMONIC	MEANING	SCHEMATIC LOCATION
WTE011	This data steering signal is asserted high-active for a fullword Write operation.	10L4
WTE021	This data steering signal is high-active for a halfword write into the least significant (odd) halfword or for a fullword write.	10L3
WTE031	This signal is asserted high-active on all Write operations to enable the appropriate parity bit(s) to be written into memory.	11H1
XRPC	Pullup Resistor C	8N5
XRPD	Pullup Resistor D	12K3
XRPG	Pullup Resistor G	9E4

EXTENDED SELECTOR CHANNEL

02-328R04A20
September 1978

METRIC

M73-105
EXTENDED SELECTOR CHANNEL INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-328 Extended Selector Channel (ESELCH) (Product Number M73-105) in a Model 7/32 or 7/32C or 8/32, 8/32C, or 8/32D Processor System. The Extended Selector Channel is complete on one 35-508 printed circuit board.

2. PHYSICAL CHARACTERISTICS

2.1 Dimensions

381 mm x 381 mm (15" x 15")

2.2 Weight

1.134 kilograms (2.5 pounds) maximum

3. INSTALLATION

The ESELCH may be installed in any even numbered chassis slot (i.e., 0, 2, 4, or 6) of the Extended Direct Memory Access (EDMA) Bus. In a 7/32 or 7/32 C Processor, the EDMA Bus starts at either Slot 3 or Slot 7 of the Expansion back panel of the twin chassis. See 02-348A20, 7/32 or 7/32 C Memory Access Controller (MAC) Installation Specification for details. For a 8/32 Processor, the EDMA Bus starts at Slot 2 of the lower CPU chassis. The EDMA Bus can be extended to other Expansion chassis through cables but the bus length is limited to 2.438 meters (8 feet). Seven DMA devices (in addition to the MAC) may be installed on the EDMA Bus. The seven devices may all be ESELCHs with no extended memory interfaces or custom DMA devices.

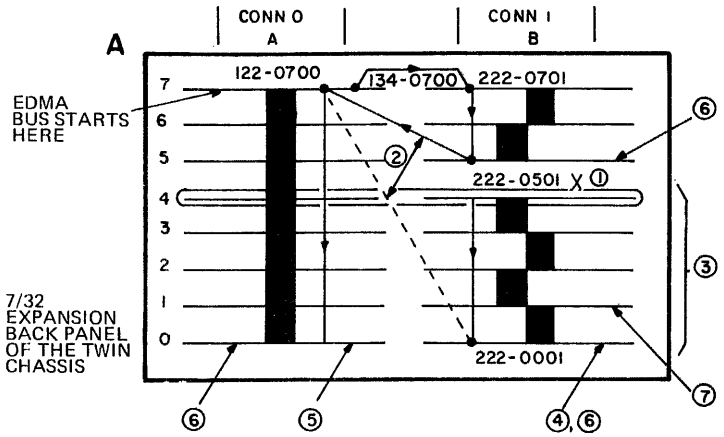
3.1 Back Panel Wiring

At the time of installation it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the ESELCH and the next higher numbered slot on the one (1) connector only. The Receive Acknowledge/Transmit Acknowledge (RACK0/TACK0) "daisy chain" wiring on the back panel is rerouted according to Figure 1A. The lower numbered card slots in the chassis become part of the private ESLECH Bus on the one (1) connector only.

To install an ESELCH in Slot 4:

1. Remove all wires from Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2 (see back panel map on Functional Schematic 02-328D08, Sheet 1).
2. Remove the wire between 222-0001 and 122-0700.
3. Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the zero (0) and one (1) connectors and RPC0/TPC0 jumper between Pins 137 and 237 on zero (0) connector of Slot 4.
4. Connect 122-0700 to 222-0501.

5. To install an ESELCH in any other even numbered slot of a twin or universal expansion chassis, a simular procedure is followed. Refer to Figure 1 (B, C, D, E, and F). When Expanding to a universal chassis only (Figures 1E, 1F), make the following changes:
Remove Wires: 128-0701-TEMP B
227-0701-TEMP A
Add: 128-0701 to 128-0601
227-0701 to 227-0601



NOTE: THE CIRCLED NUMBERS ON ILLUSTRATIONS A, B, C, D, E, AND F REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING INSTALLATION PROCEDURES.

TO INSTALL A SELECTOR CHANNEL IN SLOT 4 OF THE 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS

① CUT THE MULTIPLEXOR BUS.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

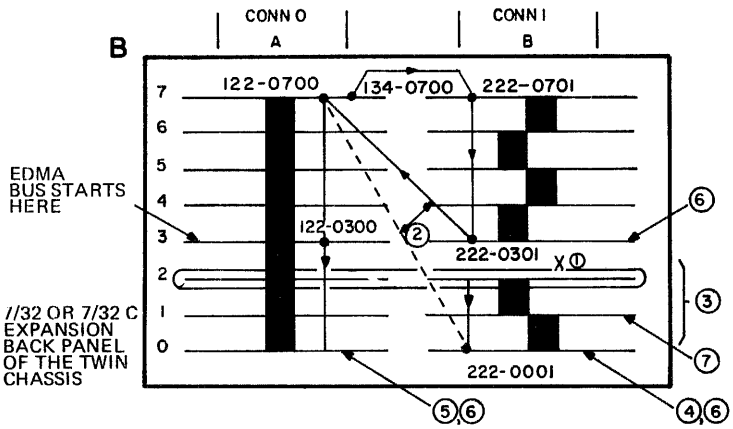
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN 1) SIDE ONLY ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE AND SLOTS 7, 6 AND 5 ON THE CONNECTOR ONE SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑦ INSTALL EDMA BUS TERMINATOR 35-548 HERE.



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS

① CUT THE MULTIPLEXOR BUS

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

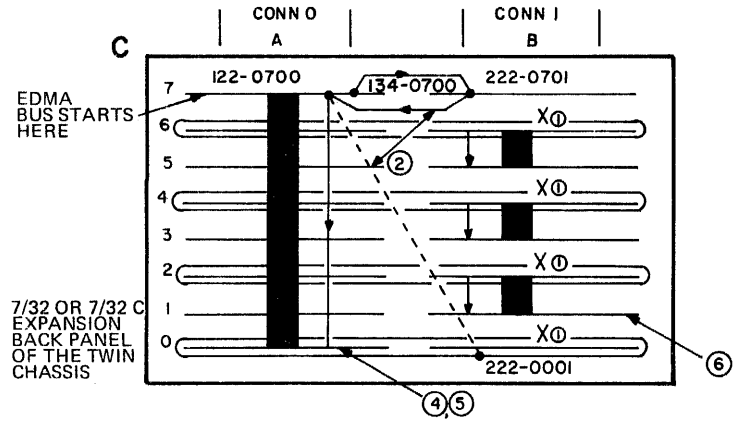
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑦ INSTALL EDMA BUS TERMINATOR 35-548 HERE.



TO INSTALL 4 SELECTOR CHANNELS (IN SLOTS 6, 4, 2, AND 0) OF THE 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS

① CUT THE MULTIPLEXOR BUS IN FOUR PLACES.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

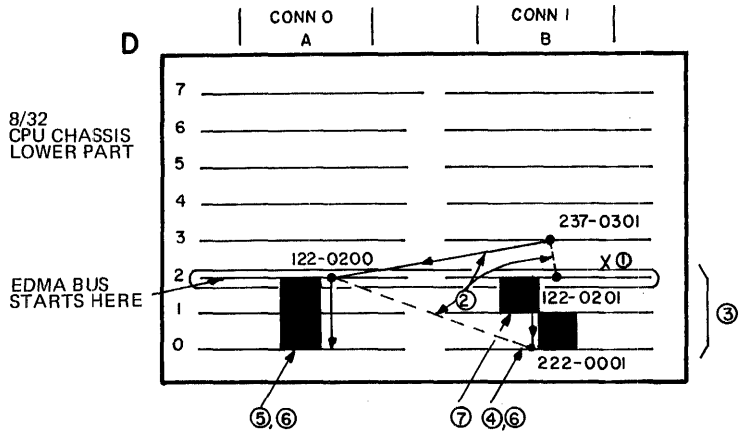
③ EACH SELCH EXCEPT THE ONE IN SLOT 0 HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 0, 1, 3, AND 5 ON CONNECTOR ONE (CONN1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

⑤ INSTALL I/O TERMINATOR 35-433R01 HERE.

⑥ INSTALL EDMA BUS TERMINATOR 35-548 HERE.

Figure 1. Backpanel Modifications



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE 8/32 CPU CHASSIS LOWER PART

① CUT THE MULTIPLEXOR BUS.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

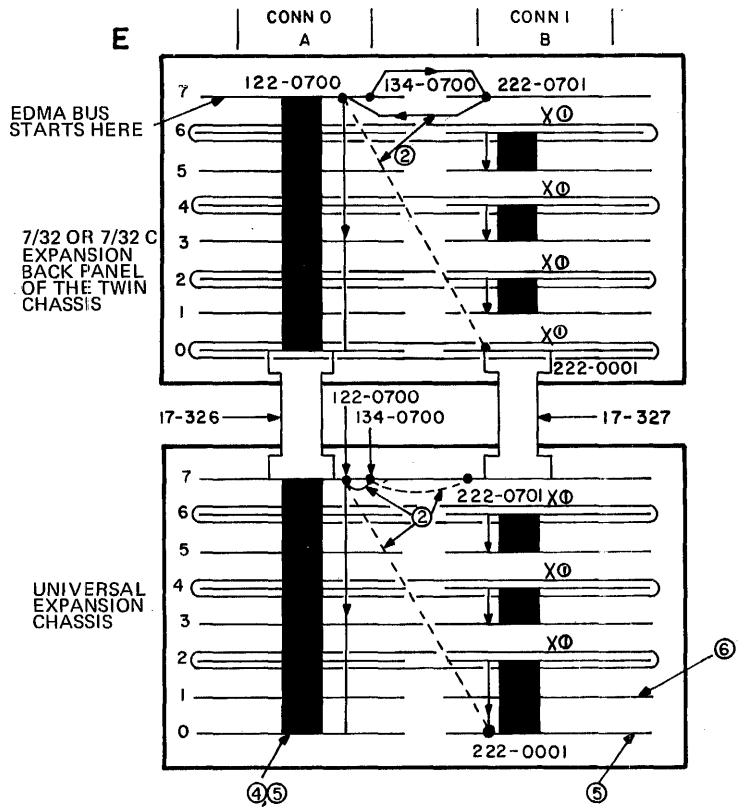
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑦ INSTALL EDMA BUS TERMINATOR 35-548 HERE.



TO INSTALL 7 SELECTOR CHANNELS IN SLOTS 6, 4, 2 AND 0 OF 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS AND 2, 4, 6 OF EXPANSION CHASSIS.

① CUT THE MULTIPLEXOR BUS IN 7 PLACES.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

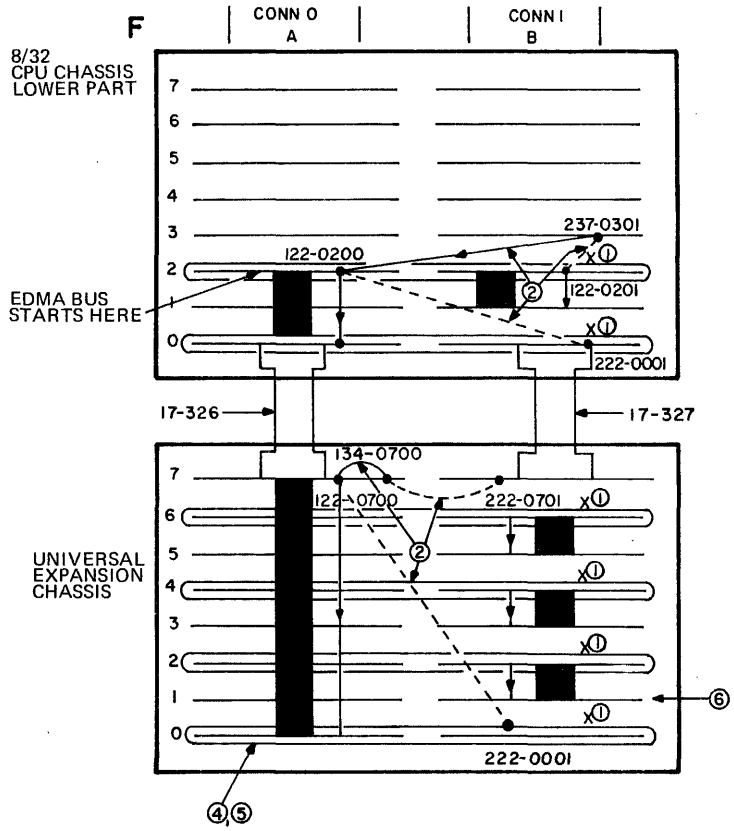
③ EACH SELCH EXCEPT THE ONE IN SLOT 2 OF UNIVERSAL EXPANSION CHASSIS HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 1, 3, AND 5 OF JUMBO CHASSIS AND 0, 3, 5 OF EXPANSION CHASSIS ON CONNECTOR ONE (CONN 1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

⑤ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑥ INSTALL EDMA BUS TERMINATOR 35-548 HERE.

Figure 1. Backpanel Modifications (Continued)



TO INSTALL 6 SELECTOR CHANNELS IN SLOTS 0 AND 2 OF THE 8/32 CPU LOWER CHASSIS AND 0, 2, 4, AND 6 OF THE UNIVERSAL EXPANSION CHASSIS.

① CUT THE MULTIPLEXOR BUS IN 6 PLACES.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPERS.

③ EACH SELCH, EXCEPT THE ONE IN SLOT 0 OF THE EXPANSION CHASSIS, HAS ONE SLOT AVAILABLE ON ITS PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 1 OF CPU LOWER CHASSIS AND 0, 1, 3, 5, OF THE EXPANSION CHASSIS ON THE CONNECTOR ONE (CONN 1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

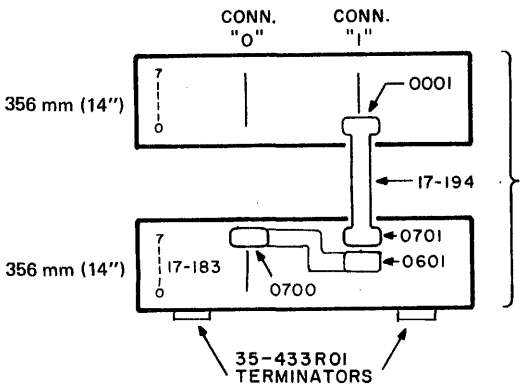
⑤ INSTALL I/O TERMINATOR 35-433R01 HERE.

⑥ INSTALL EDMA TERMINATOR 35-548 HERE.

Figure 1. Backpanel Modifications (Continued)

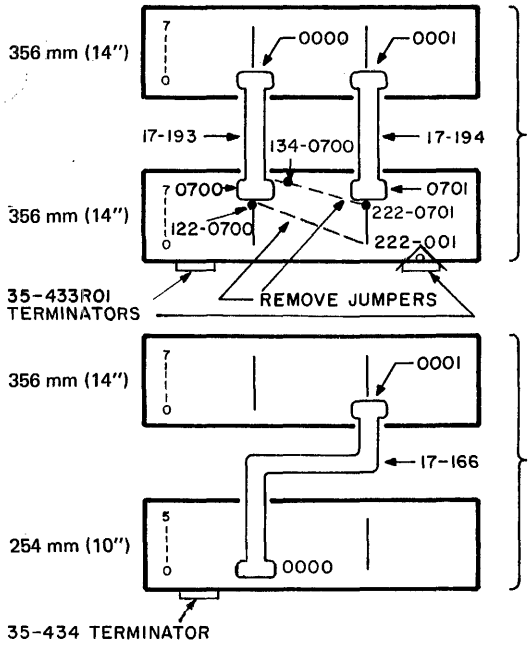
3.2 Cabling

The cabling necessary for the ESELCH depends on the systems physical configuration. When the ESELCH Bus does not extend outside the twin chassis, no cabling is required. When the ESELCH Bus must be extended to another chassis, a number of cable configurations can be used, see Figure 2. Care should be taken to minimize bus lengths and not exceed 762 mm (30") (three expansion chassis).



(A) CONNECTS TWO ADJACENT 356 mm (14") CHASSIS. THE PRIVATE SELCH BUS APPEARS AT BOTH CONNECTORS 0 AND 1 OF THE LOWER CHASSIS. NOTE THE DATA CHANNEL DOES NOT APPEAR IN THE LOWER CHASSIS.

Figure 2. Cabling



(B) USED TO CONNECT TWO ADJACENT 356 mm (14") CHASSIS. THE MULTIPLEXOR BUS APPEARS AT CONNECTOR 0, AND THE SELCH BUS APPEARS AT CONNECTOR 1. WHEN USING THIS CONFIGURATION, THE FOLLWOING WIRING CHANGES TO THE RACK0/TACK0 DAISY CHAIN MUST BE MADE TO THE LOWER CHASSIS: REMOVE 134-0700 TO 122-0701 AND 222-0001 TO 122-0700 AND ADD 134-0700 TO 122-0700.

(C) CONNECTS THE PRIVATE SELCH BUS TO A 254 mm (10") CHASSIS ONE OR TWO CHASSIS AWAY.

Figure 2. Cabling (Continued)

The termination of the 17-312 cable, at Slot 7 or Slot 3, on the Expansion back panel designates the start of the EDMA Bus. Refer to Figure 3. If any slot (on the one side) is to be used for an ESELCH, add contiguous wire straps as follows:

Slot 7	Slot 3
129 - 0701	129 - 0301
129 - 0601	129 - 0201
129 - 0501	129 - 0101
129 - 0401	129 - 0001
129 - 0301	
129 - 0201	
129 - 0101	
129 - 0001	

through the appropriate chassis.

4. ADDRESS STRAPPING

The preferred address of the ESELCH is X'0F0' (10 bit address). The controller is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-328D08.

5. STRAP OPTIONS FOR ADDRESS SPACE ALLOCATION

Address space allocation for the four memory banks is determined by strap options in the ESELCH. Each memory bank's address space must be zero or a multiple of 64K bytes up to a maximum of 1,024K bytes for a 8/32 Processor or a maximum of 256K bytes for a 7/32 or 7/32 C Processor. Address assignment must be contiguous and the four memory banks are assigned address space in ascending order.

On the ESELCH printed circuit board, there are two decoders, A03 and A04, which decode the extended address bits (four most significant address bits). Each output of the decoders allocates 64K bytes of memory. The 16 outputs with wire wrap stakes are marked 0:15. The four wire wrap stakes next to them are marked M00, M10, M20, and M30. These denote the four memory banks. The address space allocation should be strapped according to system configuration. All non-existent memory locations should be strapped to the stake marked NE (Non-Existent Memory). See Figure 4. Address Allocation

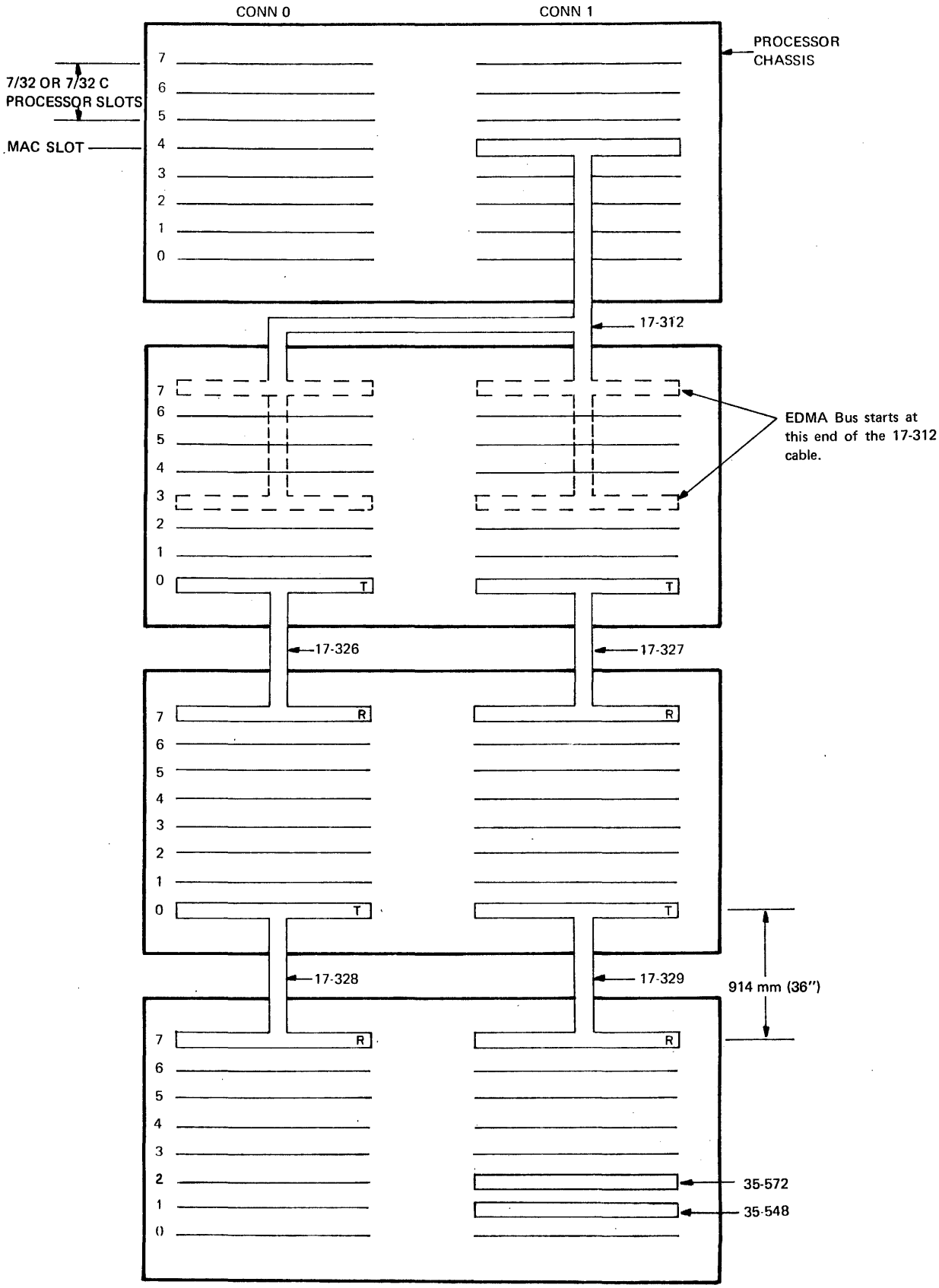


Figure 3. MAC Back Connections

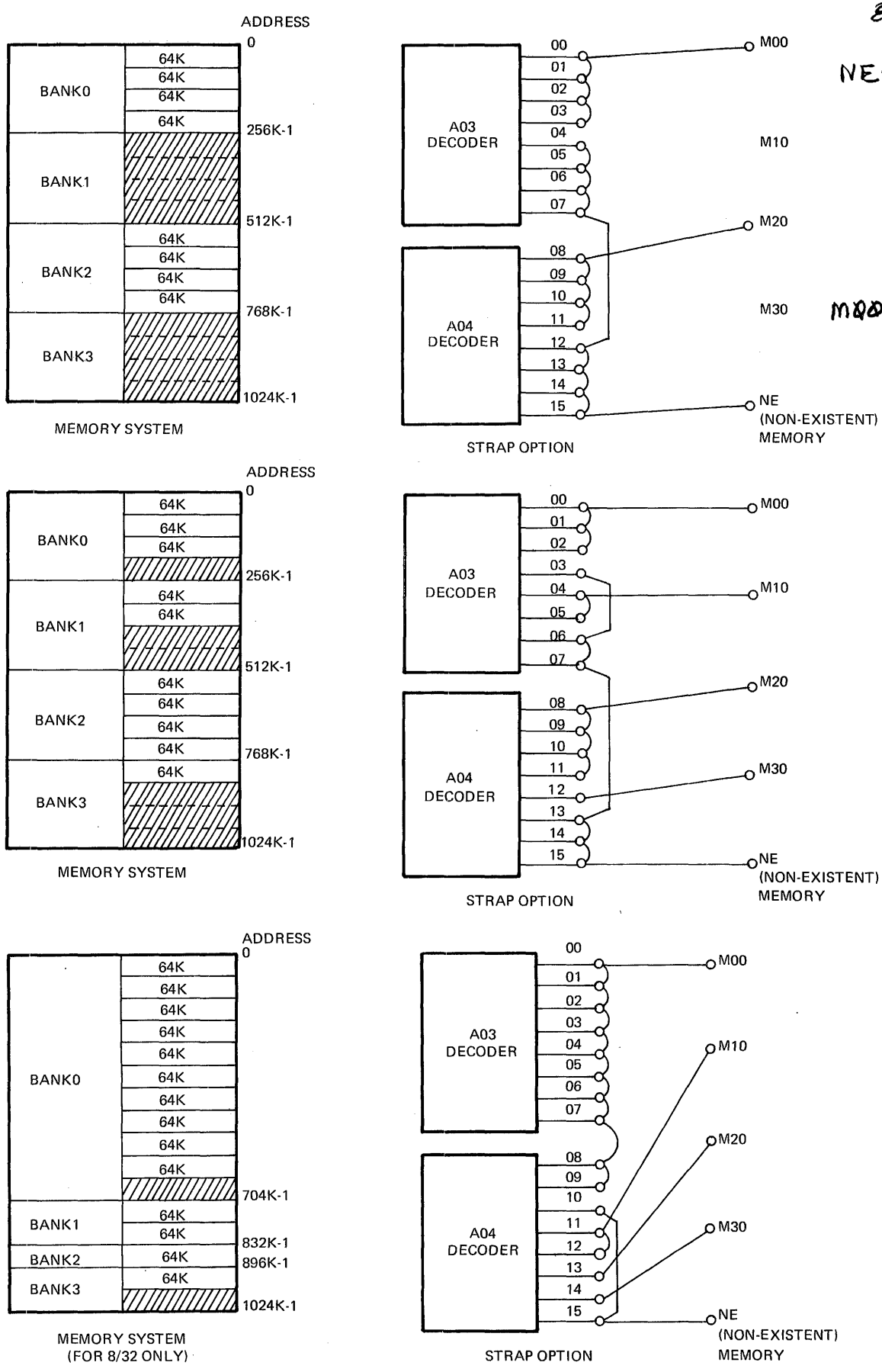


Figure 4. Address Allocation

6. INSTALLATION CHECKS

The ESELCH is factory tested using a special high speed device. Therefore, field checks are contingent upon the user having the appropriate hardware and software available with which to exercise the ESELCH. Test Program 06-161, shipped with the ESELCH, may be used if a Perkin-Elmer Magnetic Tape or a Removable Cartridge Disc system is installed on the ESELCH's private bus.

7. CONFIGURATION

The ESELCH may be installed in any chassis within the same system cabinet as the Processor. The total number of DMA devices must be seven or less. This includes ESELCHs, memory interfaces, or custom DMA devices using the Universal EDMA Bus Interface.

8. MODEL 7/32, MODEL 7/32 C, AND MODEL 8/32 STRAPPING

For use with the Model 7/32 and 7/32 C, strap E2 to E3 (M01 only).

For use with the Model 8/32, strap E2 to E1 (M01 only).

NOTE

If 35-508M01 ESELCH is used for a 7/32 or 7/32 C Processor, Strap E3 to E2. For an 8/32 Processor, Strap E1 to E2. If 35-508M00R12 ESELCH is used for 7/32 or 7/32 C Processor, Strap E3 to E2.

NOTE

The 35-508M01R02 (or higher) ESELCH is required for 8/32 Systems. The 35-508M00 or M01 may be used with 7/32 or 7/32 C Systems.

02-328R03A21
September 1978

METRIC

M73-105
EXTENDED SELECTOR CHANNEL MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-328 Extended Selector Channel (ESELCH) (Product Number M73-105) is a Direct Memory Access port which provides block data transfer between a device controller and memory. Once initiated, the transfer is independent of the Processor. The Processor sets up the device controller, loads the ESELCH with the starting and the final addresses of the memory block, specifies the type of operation (Read or Write), and issues a GO command. The ESELCH then handles the transfer without further direction by the Processor.

The Extended Selector Channel is complete on one printed circuit board and occupies one slot in a system chassis. The ESELCH provides the drivers, receivers, and termination resistors for the private ESELCH Bus. This bus originates at Connector One (1) of the ESELCH slot and extends to each lower numbered slot in the system chassis on the Connector One (1) side only. The private ESELCH Bus can be extended to other chassis, as required. For installation information, refer to the 02-328A20 Extended Selector Channel Installation Specification.

2. SCOPE

This specification describes the operation of the ESELCH in its various modes, i.e., Setup, Memory Read, Memory Write, and Termination. Where necessary, this specification references the Multiplexor Channel Bus and Extended Direct Memory Access Bus operations. These busses are described in detail in the Architectural and Product Line Standards, Extended Direct Memory Access Bus, Publication Number 43-005.

3. BLOCK DIAGRAM ANALYSIS

Refer to the ESELCH block diagram on Sheet 1 of Functional Schematic 02-328D08, and the ESELCH Flow Chart, Figure 1, during the following analysis. Before initiating a data transfer via the ESELCH, the device controller and the ESELCH must be set up. The set up procedure is implemented by the Processor via the Multiplexor Bus (MUX-Bus). When the ESELCH is in the idle mode, the MUX Bus is tied directly to the private ESELCH Bus through the ESELCH. This allows the Processor to communicate directly with any device on the private ESELCH Bus.

To prepare the ESELCH for data transfer, the Address Register (AR) and Auxiliary Address Register (AAR) must be loaded with the starting address in memory where the transfer is to begin, and the Final Address Register (FAR) must be loaded with the address of the last memory location to be accessed. These registers are loaded from the eight least significant Data Lines D080:150 by four or six consecutive Data Availables (DA) from the Processor.

The first two or three Data Availables load the starting address and the last two or three Data Availables load the final address. The Address Register is incremented by two after each halfword is transferred to/from the device. Data transfer is terminated when the Auxiliary Address Register is equal to the Final Address Register or when the Auxiliary Address Register increments past its maximum value, X'FFFFF'.

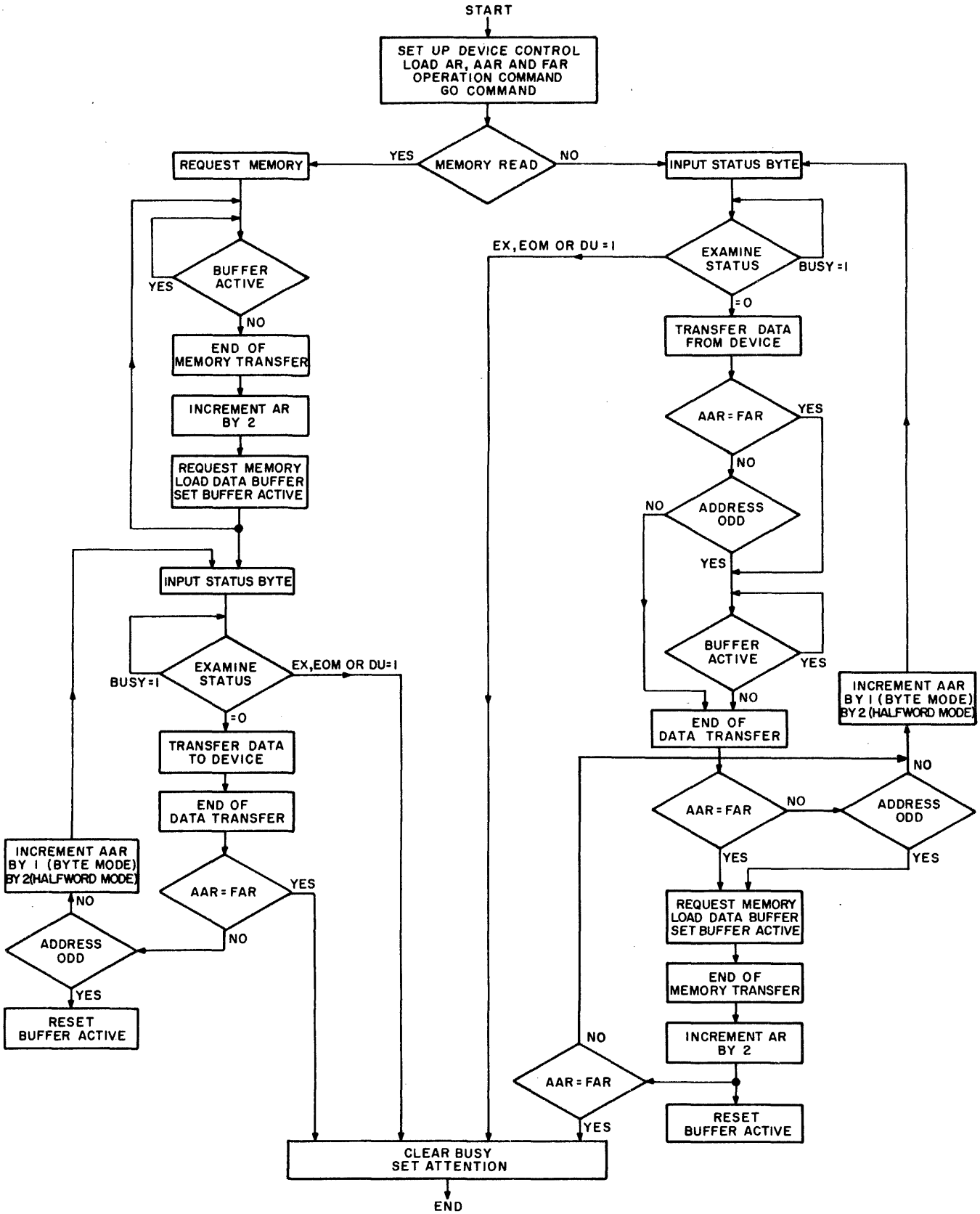


Figure 1. Flow Chart

Data transfer is begun by the Processor issuing a GO command to the ESELCH. Transfer to/from the device is now independent of the Processor. The GO command also prevents communication between the Processor and any device on the private ESELCH Bus until the transfer is terminated and the ESELCH is addressed.

Data transfer is controlled in the move data circuit by inspection of the four least significant bits of the status byte presented by the active device on the private ESELCH Bus. When any one of the three least significant bits are set (EX, EOM, or DU) the transfer is terminated. Bit 12 (Busy) regulates the rate of data transfer. In the Memory Read mode, the actual data transfer begins with a Memory Request (XREQ0) as soon as a GO command is issued. When the memory request is serviced by the Processor, the ESELCH EDMA Bus control circuit activated Select (SEL), which gates the contents of the Address Register onto the EDMA Bus. An Answer (ANS0) signal is then sent out by the Processor to gate a halfword of data from memory into the Data Register. At the termination of the memory transfer, the data is loaded from the Data Register to the Data Buffer and the Address Register is incremented.

Once the Data Buffer is loaded, data transfer to the device over Private Data Lines PD000:150 is initiated and, when applicable, a request is made to fetch the next halfword from memory. This cycle continues until either a match is detected between the contents of the Auxiliary Address Register and the contents of the Final Address Register, or until the transfer is aborted due to an error condition.

In the Memory Write mode, the data transfer sequence described previously for Memory Read mode is reversed. That is, two bytes of data are loaded into the Data Register from the device prior to a memory request and the data flow is from the device to the Data Register, Data Register to the Data Buffer, and finally to memory.

The branch gate circuit and the move data circuit control the flow of data between memory and the device. The branch gate circuit supervises the overall data flow, while the move data circuit performs the handshaking between the ESELCH and the active device on the private ESELCH Bus.

Upon termination of the data transfer, the program is notified via an interrupt and by the inactive state of the ESELCH Busy flip-flop which is presented to the program as Bit 12 of the ESELCH status byte. Extended Selector Channel Status and Command Byte Data is shown on Table 1.

TABLE 1. EXTENDED SELECTOR CHANNEL STATUS AND COMMAND BYTE DATA

BIT NUMBER	8	9	10	11	12	13	14	15
STATUS BYTE			MEMORY MAL-FUNCTION	MEMORY PARITY FAIL	BUSY			
COMMAND BYTE		EXTENDED ADDRESS READ	READ	GO	STOP	SELCH STATUS		

BUSY	This bit is set by command GO. It remains set while the ESELCH is in the process of transferring data. It is cleared by Initialize, Command STOP, normal termination, and error abortion. When this bit is cleared, an interrupt is generated.
MEMORY MALFUNCTION	This bit is set when the memory interface recognizes a malfunction. It is stored in the ESELCH for subsequent evaluation by the Processor, however, the transfer is not interrupted. It is cleared by Initialize or Command GO.
MEMORY PARITY FAIL	This bit is set when the memory interface recognizes a parity failure. It is stored in the ESELCH for subsequent evaluation by the Processor, however, the transfer is not interrupted. It is cleared by Initialize or Command GO.
READ	This command changes the mode of the ESELCH from Write to Read. In Read mode, data is transmitted from the active device on the ESELCH and written into memory. Whenever a data transmission has been completed, the ESELCH is placed in the Write mode. Each time a Read operation is required, a Read command must be issued.
GO	This command initiates a data transmission. This command can be issued at the same time the Read/Write mode is established.
STOP	This command halts any data transmission in progress, and initializes the ESELCH for starting a new operation. It should be given when the ESELCH terminates.
SELCH STATUS	When this bit is set, the ESELCH status is returned every time on an SR or SS instruction to the ESELCH. When reset, the current SELCH definition applies. (i.e., when the ESELCH is idle, the device status is returned with the BUSY bit forced to a zero. When the ESELCH is transferring data, only the BUSY bit is returned. The ESELCH becomes idle only after Initialize or any I/O instruction to the ESELCH is executed.)
EXTENDED ADDRESS READ	When this bit is set, the ESELCH returns a three byte final address to the Processor if RD or RDR followed by RH or RHR instructions are executed. The most significant byte is returned first. When this bit is reset, the ESELCH returns a two byte final address to the Processor if two successive RD or RDR instructions are executed. The most significant byte is returned first. Before issuing RD or RH instructions to read the final address, a Command STOP should be issued to insure that the ESELCH is in the initial state.

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

This section relates to Functional Schematic 02-328D08, Sheets 2 through 9. Note that in Perkin-Elmer functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 (D08). The last character (0) indicates that when D08 is active, the line is at a logical zero level.

4.2 ESELCH Control Circuit

In the idle mode (the ESELCH is in the idle mode after Initialize or any I/O instruction to the ESELCH is executed), the ESELCH Address (3M9), Busy (4E3), and Multiplexor-ESELCH (MSC) (4E4) flip-flops are reset and the private ESELCH Bus is tied directly to the Multiplexor Bus. This allows the Processor to communicate, via the Multiplexor Bus, with any device on the private ESELCH Bus. When data is transferring from the Processor to the device in the byte mode, DLG (2A3) is low. This disables the inputs to A168 and A156 transceivers (2B4 and 2B7). Data D080:150 (2A5 and 2A8) passes through A168, A156, and inverters at 2D3:2D9 and become DA081:151 (2E3:2E9). Since the ESELCH is idle, BSY1 (2H1) is low. This causes STROBE1, STROBE2, SELA and SELB of the A46, A47, A34, and A35 Multiplexors (2L4:2L9) to become active, thus DA081:DA151 can pass through these multiplexors. At this time DLG1A (2N3) is low because DLG1 (2N2) is low. This enables the A48 and A36 transceivers (2N4 and 2N7) and Data D081:151 passes through these transceivers and is sent to the device as PD080:150 (2N5:2N9).

When data is transferring from the device to the Processor, the selection lines of eight multiplexors at 3C4:3N4 are all inactive (zero is selected), thus PD081:151 can pass through these multiplexors and arrive at the input to transceivers A168 and A156. At this time DLG1 is high. This enables the transceivers and the data passes through as D080:150 to the Processor. Figure 2 shows the details of 19-118 transceivers.

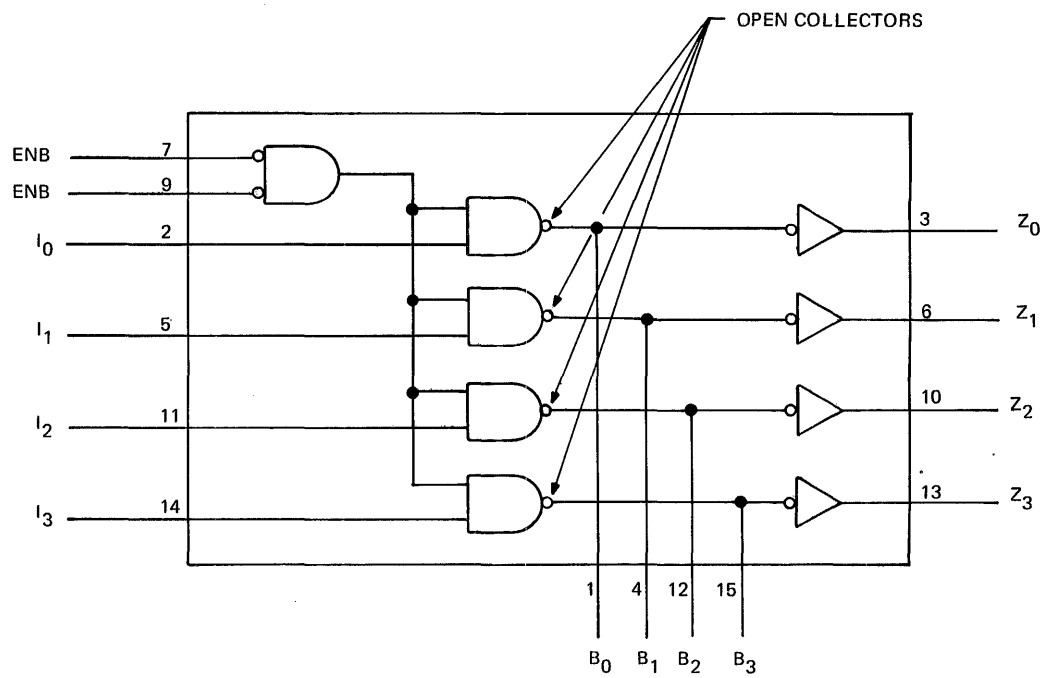


Figure 2. 19-118 Transceiver

To communicate with the ESELCH, it must first be addressed. The ESELCH Address (X'0F0' preferred) is placed on Data Lines D060:150 (2A5:2A8) and the Address control line is activated (ADRS0) (4K7). The ESELCH Address is decoded by the eight input NAND gate (2H6) and the Address flip-flop is set (3M9). The Address flip-flop set output (AD1) (3M8), when active, prevents the control signals on the MPX-Bus from passing onto the private ESELCH Bus by holding the Control Line Gate inactive (CLG1 and CLGA1) (2G2). SGAD0 (4M7) controls the Private Address (PADRS0) (4N7) such that when the ESELCH is being addressed, PADRS0 does not become active. This allows the ESELCH to be addressed without resetting the Address flip-flop on the active device on the private ESELCH Bus.

The loading of the Address Register (AR), Auxiliary Address Register (AAR), and the Final Address Register (FAR) is accomplished by four or six consecutive Data Availables (DAs) from the Processor. The Load/Unload Sequencer (6C3) controls the loading of these registers and the unloading of the Auxiliary Address Register. The Sequencer is set to its initial state by the termination of the last data transfer, a STOP command, or a System Clear (SCLR0) (3K9). The Address Registers on Sheet 6 (6F1:6F8) and the Final Address Registers (FX, FH, and FL) on Sheet 5 are connected as shown in Figure 3. If four consecutive Data Availables to the ESELCH (DAs) are executed by the Processor, the first DA loads DA081:151 into the Final Address Low Register (FL) and the second DA copies the contents of the FL Register into the Final Address High Register(FH) and a new DA081:151 is loaded into the FL Register and so on. After the fourth DA is executed, Bits 00:07 of the starting address are loaded in the Address High Register (AH) and Bits 08:15 of the starting address are loaded in the Address Low Register (AL). Bits 00:07 of the final address are loaded in the Final Address High (FH) Register and Bits 08:15 of the final address are loaded in the Final Address Low Register (FL). Counter A in the Load/Unload Sequencer is initially set at State 3 (0011). After four DAs are executed, Counter A is in State 7 (0111). At this time the D output of Counter A is still low. When Command GO is executed, NAND Gate C generates a Page Zero (PG00) signal to clear the Address Extended Register (AX) and the Final Address Extended Register (FX). The Command GO (3N6) generates a Set Auxiliary Address Register (SETAAR0) (3N6) to copy the starting address into the Auxiliary Address Register at 5B3:5N3. If six DAs to the ESELCH are executed by the Processor, the first four DAs act exactly the same way as before except that the fourth DA also generates a Load Final Address Extended (LFRX0) signal to load DA121:151 into Final Address Extended Register (FX). After the fifth DA is executed, the Extended, High, and Low Starting Address bits and the Extended, and High Final Address Bits are loaded in the AX, AH, AL, FH and FL Registers respectively. At this time, Counter A in the Load/Unload Sequencer is at State 8 (1000) and the D output is high. This inhibits any further data from loading into the AX, AH, and AL Registers. After the sixth DA is executed, the Extended Final Address bits in FH are thrown away and the High Final Address bits in the FL Register are copied into the FH Register and the Low Final Address bits are loaded into the FL Register. At this time all the address bits are loaded into the correct registers. The Command GO (3N6) generates a Set Auxiliary Address Register (SETAAR0) (3N6) to copy the starting address into the Auxiliary Address Register at 5B3:5N3.

If the Extended Address Read Command bit is reset, two Data Requests (DRs) are required to read back the final address from the Auxiliary Address Registers. Counter A145 (6C2) is initially set at State 3 (0011) and the C input of the A157 Decoder is low (6C4) because the A54 (6C7) flip-flop is reset by resetting the Extended Address Read Command bit. The first DR decodes State 3 of Counter A145 and activates the Unload Auxiliary Address Register High (UAARH0) (Sheet 6). Outputs from the Auxiliary Address Register (AAR041:111) (Sheet 3) pass through the Multiplexors at 3C4:3N4 and send the high bytes of the final address to the Processor. The second DR increments the counter to State 4 (100). Since input C of Decoder A157 (6C4) is set low, the zero state is decoded. It activates the UAARL0 and sends the low bytes of the final address to the Processor.

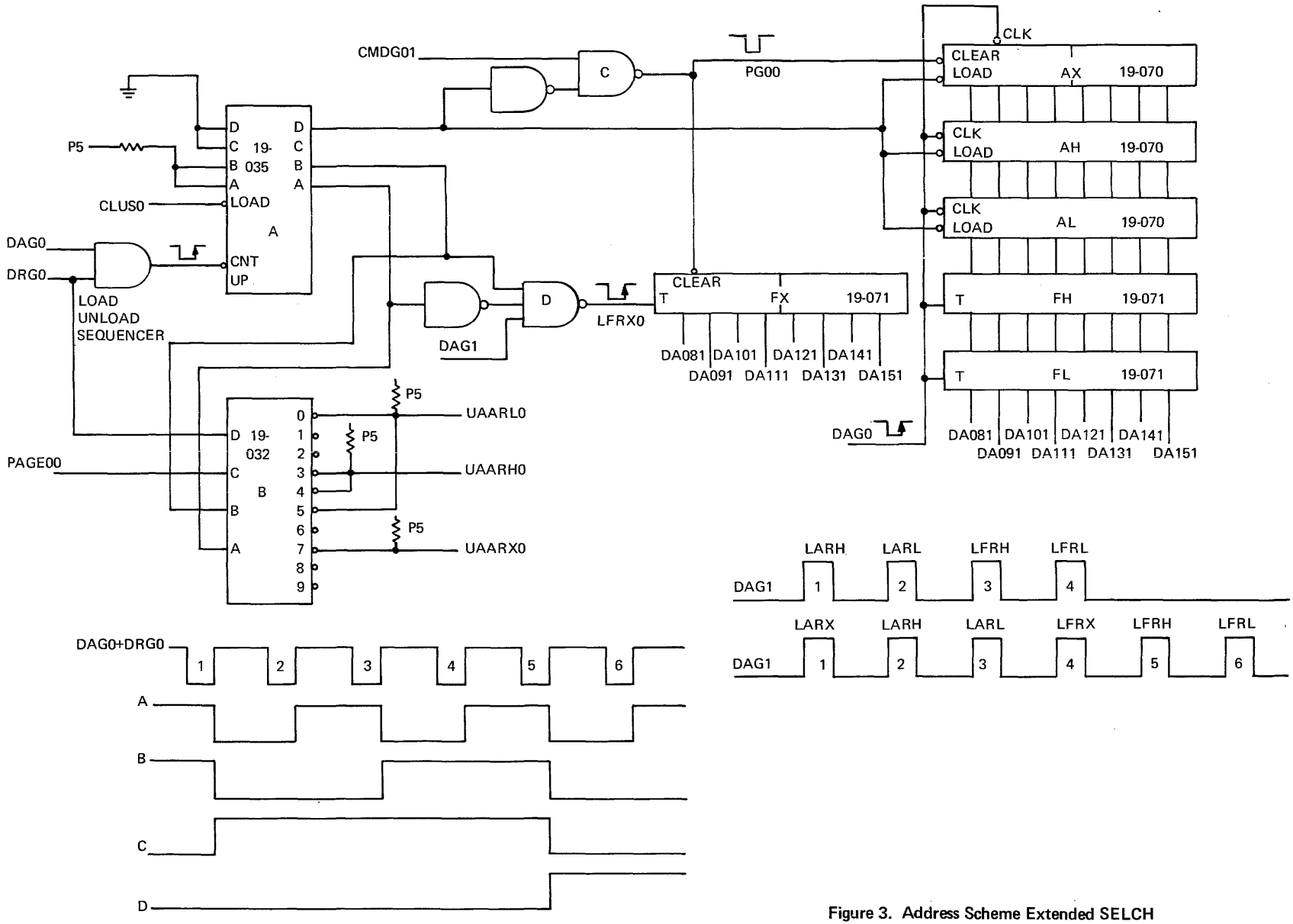


Figure 3. Address Scheme Extended SELCH

If the Extended Address Read Command bit is set, three Data Requests (DRs) are required to read back the final address from the Auxiliary Address Register. In this case, flip-flop A54 (6C7) is set and input C of Decoder A157 (6C4) is high. The remainder of the operation is the same as described previously.

If a Memory Write operation is desired, an Output command with Bit 10 set must be issued to set the Write flip-flop (4E6). Since the Write flip-flop is reset by the Data Available/ Requset Gate (DARG1) (4A6) whenever a DA or DR is sent to the ESELCH (set up procedure), no command is necessary to initiate a Memory Read operation.

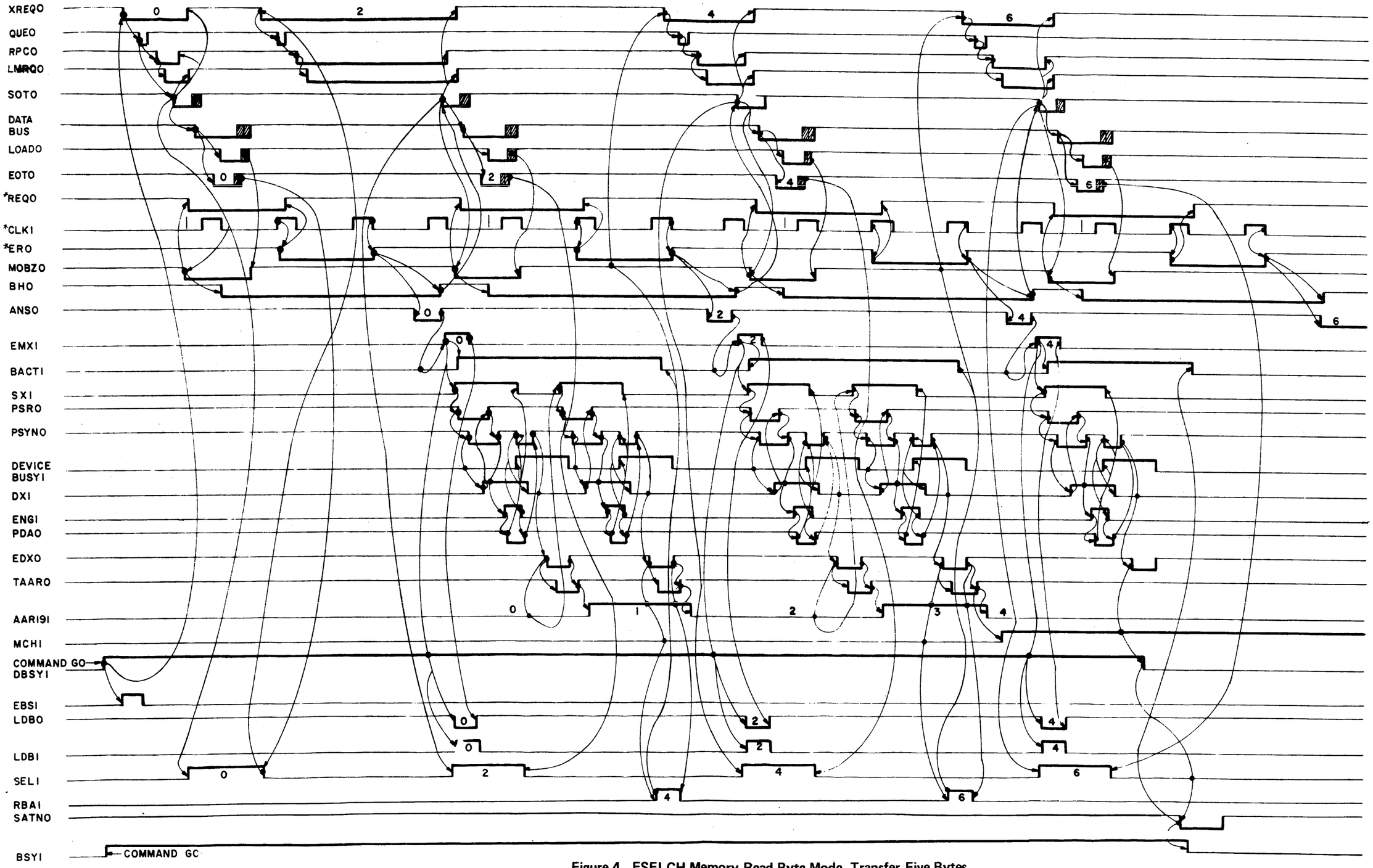
Data transfer commences with a GO command from the Processor, which is an Output command with Bit 11 set. The GO command sets both the BUSY (4E3) and MSC (4E4) flip-flops. The setting of the BUSY flip-flop causes an End of Busy Set pulse (EBS1) (4N3) to be generated. This pulse is generated from the falling edge of BSY0 (4F3), and is used by the branch gate circuit to initiate the transfer cycle. The busy latch circuit remains set until the ESELCH detects the termination of transfer and its state is presented to the program via Bit 12 of the Sense Status byte.

The Multiplexor ESELCH Control (MSC) flip-flop is reset by SCLR0A (4A5) or by addressing the ESELCH i.e., Set Gate active (SGAD1) (4A5), when the Busy flip-flop is reset. The resetting of the MSC flip-flop, MSC0 active, clears any pending interrupt in the ESELCH (8C5).

4.3 Extended Direct Memory Access Bus Control Circuit

Extended Direct Memory Access Bus Control timing relationships are shown in Figures 4 and 5 timing diagram for Memory Read Byte mode and Memory Write Byte mode respectively. An ESELCH request for memory is started by activating Set Request (XREQ0) (9M2). XREQ0 is activated by the branch gate circuit (8M1:8M8) when either the ESELCH bus has received a halfword of data from the device or, in the Memory Read mode, whenever the Memory Data Register (MDR) is available to accept the next halfword.

If the Select flip-flop (9G2) A62 is reset, the memory is not busy (M0BZ0:M3BZ0) (9F6) and if REQ1 (9M3) is active, XREQ0 is active. When the EDMA Bus receives the XREQ0, a Queue pulse (QUE0) (9A2) is sent to the ESELCH. The QUE0 pulse resolves contention for the bus by freezing the request status (9C2:9E2) It then sends a Receive Priority Chain pulse (RPC0) (9A3). The QUE0 pulse sets Contention flip-flop A39 (9E2) in all requesting devices. The highest priority queued device then captures the RPC0 pulse, sets the A62 flip-flop (9D2), and does not propagate the Transmit Priority Chain pulse (TPC0) (9H3) to the next device. If the ESELCH is requesting local memory, Local Memory Request Queued (LMRQ0) (9G1) is sent to the EDMA Bus at this time. If the EDMA Bus is not busy, a Start of Transmission pulse (SOT0) (9C9) is sent to the ESELCH. SOT0 then sets a Select flip-flop (9G2) which in turn removes XREQ0 and activates Memory Busy (MXBZ0) (9F6). Once the Select flip-flop is set, the SEL0 (9B7) enables the oscillator circuit (9D6) and the counter (9D8) starts counting. If it is in the Memory Read mode, Address MAX121:151 and MA001:151 (6G1:6G8) is presented to the EDMA Bus as DMX120:150 and DMA000:150 (6N1:6N7) and a Load (LOAD1) (9J8) signal strobes the address into the Processor. At the same time, an End of Transmission pulse (EOT1) (9L7) is sent to indicate to the EDMA Bus that the ESELCH has finished the transmission. EOT0A (9C4) fires a one-shot and resets the Select flip-flop and EDMA Bus control cycle is finished. In the Memory Write mode the operation is the same as in the Memory Read mode except that two consecutive LOAD1s (9J8) are sent. The first one is for the address and the second is for the data. Figure 6 shows the EDMA Bus control timing.



*IN PROCESSOR

Figure 4. ESELCH Memory Read Byte Mode, Transfer Five Bytes

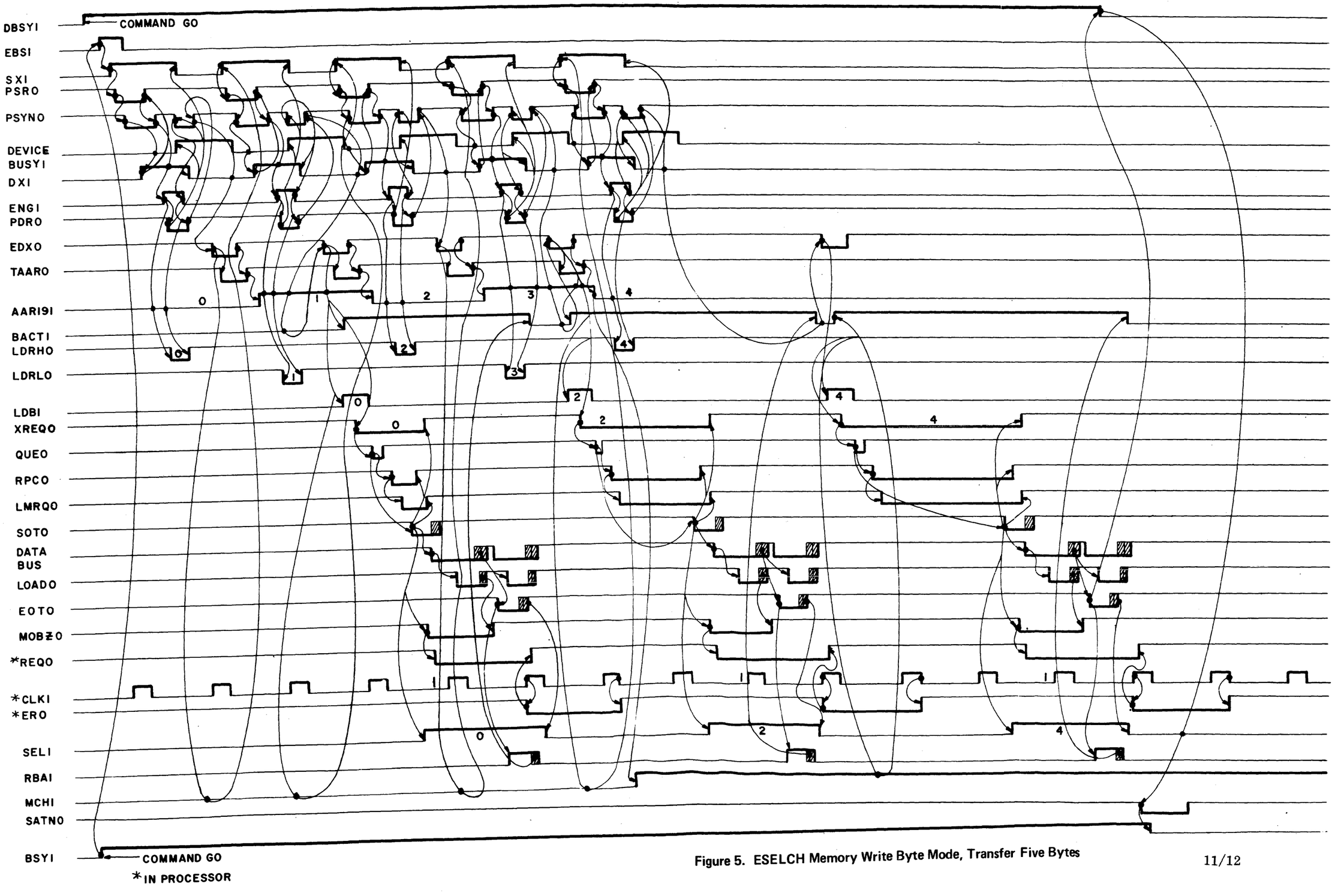
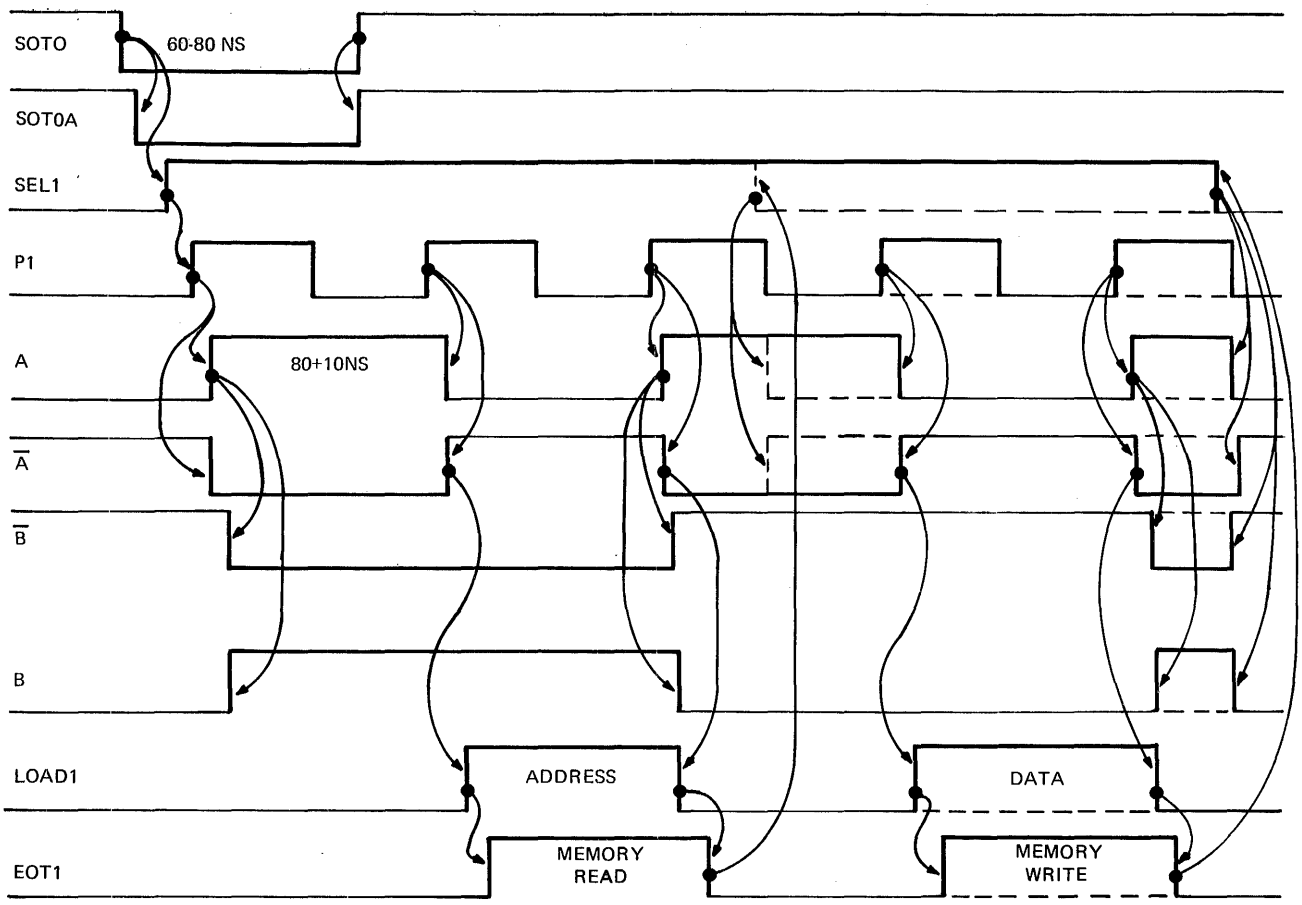


Figure 5. ESELCH Memory Write Byte Mode, Transfer Five Bytes



NOTE: DOTTED LINES FOR MEMORY READ

Figure 6. Extended Direct Memory Access (EDMA) Control Timing

4.4 Address Register and Auxiliary Address Register

The Address Register (6F1:6F8) and the Auxiliary Address Register (5B3:5N3) each consist of five four-bit counters. These registers are loaded by the Processor from Data Lines D080:150 (2A5 and 2A8), under control of the Load/Unload Sequencer (6C4) with the starting address from which the block transfers is to begin. The contents of the Address Register is gated onto the EDMA Bus Data Lines DMX120:150 and DMA000:150 (6N1:6N7) whenever the ESELCH is selected (SEL0A at 6L1 controls). The Address Register is incremented twice with each memory transfer by EOT0A and END0 (6D6). The Auxiliary Address Register (5B3:5N3) keeps track of the transfer between the ESELCH and device. This register is incremented, by one, for each byte of data transferred by Toggle Auxiliary Address Register (TAAR0)(5B1). When the transfer is in the Halfword mode, TARR0 is generated twice for each transfer. The outputs of the Auxiliary Address Register are used by the match circuit to determine the end of the data blocks. It's contents may be examined, via the program, by issuing two or three consecutive DRs to the ESELCH when the sequencer is initialized. In addition, AAR191 (4H8) is used in the Byte Transfer mode to determine whether the byte being transferred is odd or even, for byte steering. Carry Out from the most significant stage of the Auxiliary Address Register (5M1) terminates the transfer, clear Busy (4F1), when a transfer is attempted past the maximum address. This feature prevents 'wrap-around' in memory.

4.5 Final Address Register

The Final Address Register (FAR) is implemented by five quad latches (5B5:5N5). The register is loaded by SETAAR0 (5B1) when a GO command is executed. The outputs of this register are used exclusively by the match circuit to determine when the final address of the transfer is reached.

4.6 Memory Data Register and Data Buffer

The Memory Data Register (Sheet 7) is a 16-bit register composed of 16 edge triggered flip-flops. In the Memory Read mode, the data is toggled on the leading edge of Controlled Answer (CANS0) (7A9). During a Memory Write, data is toggled into the flip-flops on the trailing edge of the Load Data Register High (LDRH0) (7A9) or Load Data Register Low (LDRL0) (7H8).

As soon as the Memory Data Register is loaded, if the Data Buffer is empty as determined by the inactive state of the Buffer Active flip-flop (4G2), the contents of the Memory Data Register are loaded into the Data Buffer by Load Data Buffer (LDB1) (7A9). Information present in the Data Buffer is, in turn, either written into memory via EDMA Bus Data Lines DMA000:150 or sent to the device on Private Data Lines PD000:150.

4.7 Data Transfer Circuit

Refer to Figure 4 for Memory Read Byte mode timing diagram and Figure 5 for Memory Write Byte mode timing diagram. Both timing diagram show the timing of five byte transfer in the Byte mode.

A GO command to the ESELCH sets the Busy flip-flop (4E3) which generates the End of Busy Set pulse (EBS1) (4N3).

In the Memory Read mode, XREQ0 (9M2) is generated by Command GO (CMDG0) (9K4), thus a request for memory is initiated. When the halfword of data is present in the Memory Data Register, the End of Memory Transfer pulse (EMX1) (8L7) becomes active and the branch gate circuit once again requests memory and generates Set Status Transfer (SSX0) (8R4) and Load Data Buffer (LDB1) (9N8). These signals initiate the transfer to the device and load the Data Buffer respectively.

SSX0 sets the Status Request flip-flop (4C6) which activates the Private Status Request control line (PSR0) (4F6) to the active device on the private ESELCH Bus. This Status Request examines the four least significant bits of the status byte. If any of the three least significant bits (EX, EOM, or DU) are set, the transfer is terminated by resetting the Busy flip-flop (4E2). Assuming that each of these status bits remain reset for the remainder of this discussion. With Bit 12 (Busy) of the status byte reset, the Data Transfer flip-flop becomes set (4C8). Data transfer (DX0) (4D8) inhibits the generation of PSR0, which causes Private Sync (PSYN1) (4N4) from the device to become inactive. This enables Engage to go high (ENG1) (4G8), which allows the Private Data Available control line (PDA0) (4J6) to become active. The Private Data Available/Request signal (PDAR1) (4A6), generated whenever a Private Data Available (PDA0) or Private Data Request (PDR0) signal is active, clears the Status Request flip-flop. Upon receipt of Sync from the device, PSYN1 active, the Data Transfer flip-flop becomes reset and ENG1 goes low, disabling PDA0. When the Sync is removed by the device, an 80 nanosecond End of Data Transfer pulse is generated (EDX0) (4N9) which increments the Auxiliary Address Register and is used by the branch gate circuit to generate a SSX0 which starts the sequence again. When EDX0 and AAR191 are both active, Reset Buffer Active (RBA0) (8R3) is generated. It resets the Buffer Active flip-flop (4G2) and requests the memory again (9K4). This cycle continues until termination of the transfer is detected.

In the Memory Write mode, WT1 active (4F5), EBS1 (8K4) is used to generate SSX0, and the branch gate circuit directs the loading of a halfword of data into the Data Buffer before a memory request is made. The transfer of data from the device is the same as described in the Memory Read mode, except that ENG1 is used to generate the Private Data Request control line (PDR0) (4J5) rather than PDA0. Data from the device is loaded into the Memory Data Register on the trailing edge of either Load Data Register High (LDRH0) (4K8) or Load Data Register Low (LDRL0) (4J7), depending on which eight bits are being loaded. In the Halfword Transfer mode, both LDRH0 and LDRL0 are generated simultaneously. With WT1 active, the generation of EDX1 is delayed by activating the clear input to the one-shot (4L9) when the Buffer Active flip-flop is set (BACT1) (4G9), if either the transfer to the device is on an odd boundary or when a Match is detected (MCH0) (5H9). This prevents the reloading of the Data Buffer before the last halfword has been written into memory.

4.8 RACK0/TACK0 Contention Circuit

The ESELCH directs the propagation of the Acknowledge signal to lower priority devices on the Multiplexor Channel Bus as well as devices on the private ESELCH Bus. If the ESELCH Attention flip-flop (8C5) is set, the ESELCH captures the Receiver Acknowledge signal (RACK0) (8A4), places its device address on the data lines and returns Sync to the Processor, Attention Sync (ATSYN0) (8H3) active. If the Attention flip-flop is reset, RACK0 is propagated as either Private Transmit Acknowledge (PTACK0) (8G2) or Transmit Acknowledge (TACK0) (8G1). Since devices on the private ESELCH Bus have a higher interrupt priority than devices below the ESELCH on the MPX Bus; if the Private Attention line is active (PATN0) (8A3), PTACK0 is generated rather than TACK0. Note that when MSC1 is low (8C2), PATN0 is disabled so that a device on the private ESELCH Bus may not interrupt the Processor while the ESELCH is active.

4.9 Strap Options for Address Space Allocation

Address space allocation for the four memory banks is determined by strap options in the ESELCH. Each memory bank's address space must be zero or a multiple of 64K bytes up to a maximum memory capability of 1,024K bytes for the 8/32 Processor, a maximum of 256K bytes for the 7/32 or 7/32C Processor, or a maximum of 512K bytes for the 7/32C with the 35-527M02F01 Memory Access Controller. Address assignment must be contiguous and the four memory banks are assigned address space in ascending order.

In the ESELCH printed circuit board, there are two decoders, A03 and A04, (8C6, 8C7) which decode the extended address bits (four most significant address bits). Each output of the decoders allocates 64K bytes of memory. The 16 outputs with wire wrap stakes are marked 0:15. The four wire wrap stakes next to them are marked M00, M10, M20 and M30 (8D5, 8D8) denoting the four memory banks. The address space allocation should be strapped according to system configuration. All non-existent memory locations should be strapped to the stake marked NE (Non-Existent) Memory. See Figure 7 for details.

5. INSTALLATION CHECKS

Before attempting any maintenance or testing, insure that the necessary back panel modifications and ESELCH board option strapping have been made in accordance with the 02-328A20 ESELCH Installation Specification.

To insure a 2,000,000 Byte/Second transfer rate in the Halfword Transfer mode, it is necessary to limit the maximum delay between PDA0, PDR0, and PSR0 and the return of Sync from the device (PSYN0) to 50 nanoseconds. In addition, the EDMA Bus must have only one active MAC (i.e., the ESELCH), the device must be ready for the next byte of data, Busy status bit reset, whenever a Status Request (SR) is made. Field testing of this device is contingent upon the user having the appropriate software and hardware available with which to exercise the ESELCHs. Refer to Test Program Description 06-161 a configured requirements. There are no adjustments associated with this device.

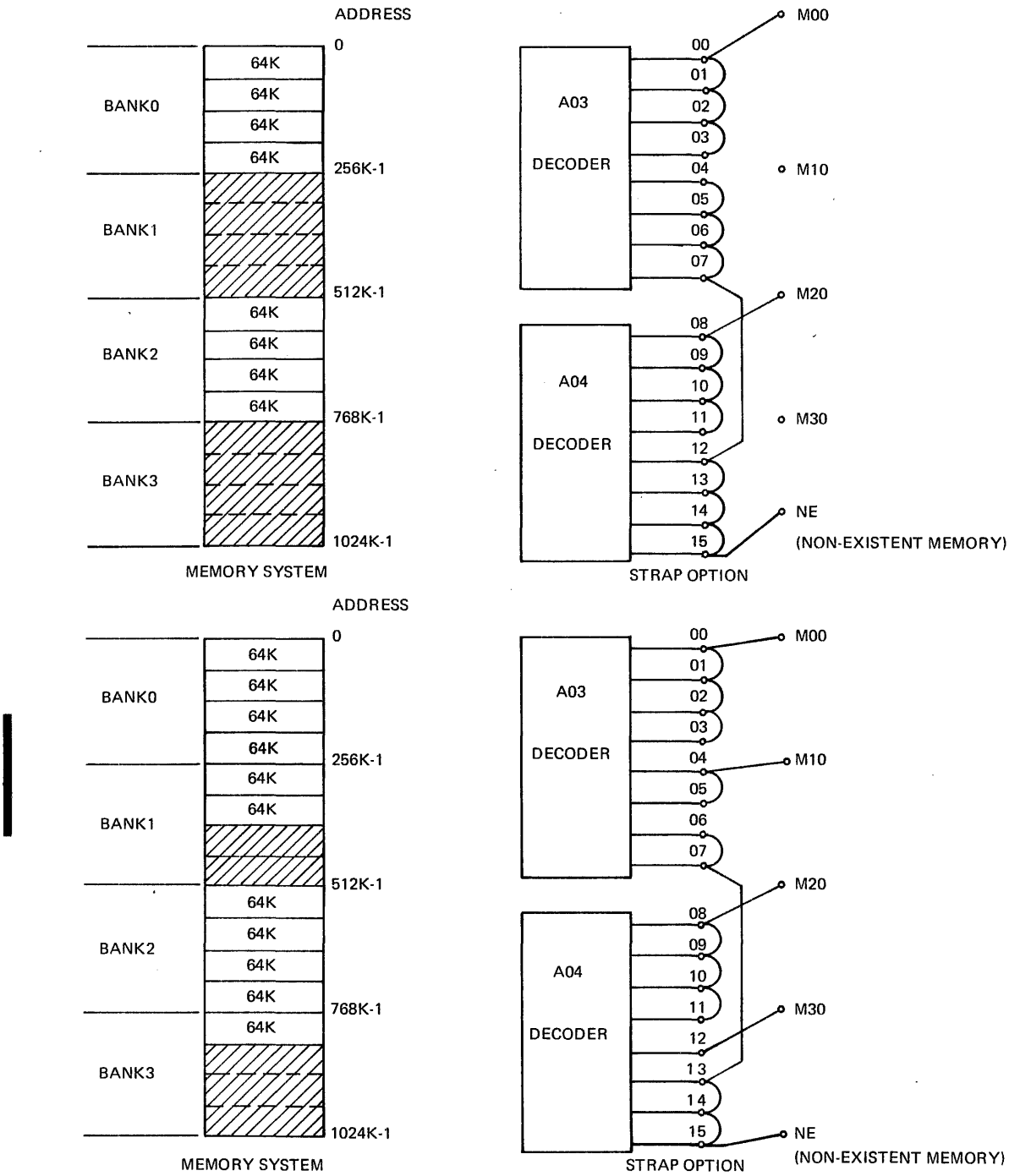


Figure 7. Address Allocation

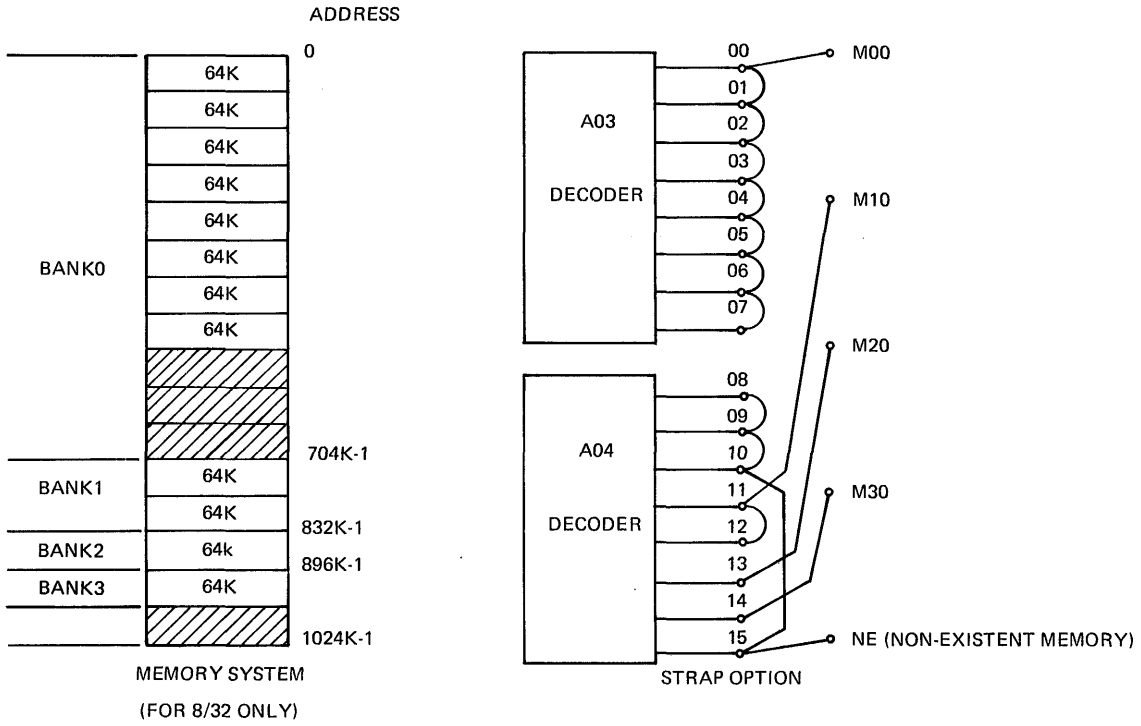


Figure 7. Address Allocation (Continued)

6. MNEMONICS

The following list provides a brief description of each mnemonic found in the ESELCH. The source of each signal on Functional Schematic 02-328D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AAR001:191	Outputs from the Auxiliary Address Register	5A6-5N6
AD1	Address-active when ESELCH is addressed	3N9
ADDA0	Address and Data Control-in Memory Read mode, LOAD0 strobes the address to the EDMA Bus. In Memory Write mode, the first LOAD0 strobes the address and the second LOAD0 strobes data to the EDMA Bus.	9J9
ADRS0	Address control line from MPX-Bus	4K7
ANS0	Answer control line-sends data from memory to ESELCH	6N9
ATN0	Attention-Attention to Processor	8E3
ATSYN0	Attention Sync-generated by an Acknowledge Attention from the Processor	8H3
BACT1	Buffer Active-indicates that valid data is present in the data buffer	4H1
BSY1	Busy-indicates data transferred in progress	4F3
CANS0	Controlled Answer-to insure that the answer is coming from the right memory.	8J6
CBSY0	Clear Busy-terminates transfer when a match or a non-existent memory is detected	8R5
CL070	Power Failure Clear	4K5
CLG1	Control Line Gate-gates private control lines	2G2
CLGA1	Control Line Gate-same as CLG1 except used to assure a 100 nanosecond delay between ADRS, CMD, DA, and the Data Lines	2G2
CLUS0	Clear Load/Unload Sequencer-clears sequencer	4F2
CMDGO0	Command GO-starts the whole sequence	4H4
CMD0	Command control line from MPX-Bus	4K6
CO0	Carry Out of the Auxiliary Address Register-Prevents memory wrap-around	5M1
D000:150	Data Lines from MPX-Bus	2A5-2A8 3A7-3A9
DA0	Data Available control line from MPX-Bus	4K6
DB001:151	Outputs from Data Buffer	7F1-7F8 7N1-7N8

MNEMONICS	MEANING	SCHEMATIC LOCATION
DBSY1:	Delayed Busy-to insure that the memory cycle is finished before sending out an interrupt	4L1
DLG1	Data Line Gate-gates data line and private data lines	2R2
DMA000:170	EDMA Bus Data Lines	6N2-6N9
DMX120:150	EDMA Bus Extended Data Lines	6N1
DR0	Data Request control line from MPX-Bus	4K5
DX1	Data Transfer-Data Transfer flip-flop	4D8
EBS1	End of Busy Set-signals the start of a ESELCH transfer	4N3
EDX0	End of Data Transfer-signals the end of a device transfer	4N9
EMX1	End of Memory Transfer-signals the end of a memory transfer	8L7
ENG1	Engage-gates either PDA0 or PDR0	4G8
EOT0	End of Transmission-to tell EDMA Bus that transmission is ended.	9L8
FH001:071	Final Address Register High-Final Address Bits 00:07	5G5-5K5
FL001:071	Final Address Register Low-Final Address Bits 08:15	5A5-5E5
GETBUS0	ESELCH gets the EDMA Bus in Memory Read mode	8J5
LDB1	Load Data Buffer-loads data into Data Buffer	8N8
LDRH	Load Data Register High-loads Data Bits 00:07	4K8
LDRL0	Load Data Register Low-loads Data Bits 08:15	4J7
LFRX0	Load Final Address Register Extended Bits 00:03	6D6
LMRQ0	Local Memory Request Queued	9G1
LOAD0	Load control line-loads Data or Address to EDMA Bus	6N9
M00:30	Memory Banks 0:3	8D6-8D8
M0BZ0:M3BZ0	Memory Busy	9F6
MA001:151	Memory Address Bits	6G3-6G7
MAX121:151	Extended Memory Address Bits	6G1
MCH1	Match-indicates a match between the Auxiliary Address Register and Final Address Register	5K9

MNEMONICS	MEANING	SCHEMATIC LOCATION
MMF1	Memory Malfunction	7K3
MSC1	Multiplexor-ESELCH Control flip-flop	4F5
PADRS0	Private Address control line to ESELCH Bus	4N7
PAGE01:11	Pages 01:11-encode M00:M30	8G6-8G7
PATN0	Private Attention from ESELCH Bus	8A3
PCL070	Power Failure Clear to ESELCH Bus	4N5
PCMD0	Private Command control line to ESELCH Bus	4N6
PD000:150	Private Data Lines-ESELCH Bus	2N5-2N9 3H7-3H9
PDA0	Private Data Available control line to ESELCH Bus	4J6
PDR0	Private Data Request control line to ESELCH Bus	4J5
PF1	Memory Parity Failure	7K4
PG00	Page Zero-indicates that four WDs are used to Set up Starting and Final Addresses, i.e., the Final Address is no greater than 64K Bytes.	6A1
PHW0	Private Halfword control line from ESELCH Bus	2D1
PSR0	Private Status Request control line to ESELCH Bus	4F6
PSYN0	Private Sync from the ESELCH Bus	4K4
PTACK0	Private Transmit Acknowledge to the ESELCH Bus	8H2
QUE0	Queue-to resolve contention for EDMA Bus	9A2
RACK0	Receive Acknowledge from MPX-Bus	8A4
RBA0	Reset Buffer Active-reset Buffer Active flip-flop	8R2
RBA0A	Controlled Reset Buffer Active-the leading edge clears the Buffer Active flip-flop in Memory Read mode and the trailing edge clears the Buffer Active flip-flop in the Memory Write mode.	8R3
RPC0	Receive Priority Chain from EDMA Bus	9A3
SATN0	Set Attention flip-flop	4N1
SBACT1	Set Buffer Active-set Buffer Active flip-flop	8R6
SCLR0	System Clear-initialize signal	3K9
SDX0	Set Data Transfer flip-flop-if no error status	4F1

MNEMONICS	MEANING	SCHEMATIC LOCATION
SEL1	Select-ESELCH gets the EDMA Bus	9H2
SELSTS1	Selch Status Command Bits	4C3
SETAAR0	Set Axuiliary Address Register	3R6
SGAD0	Set Gate-sets Address flip-flop	2J6
SOT0	Start of Transmission-to tell the ESELCH to start transmitting an address and data to the EDMA Bus	9C9
SR0	Status Request control line from MPX-Bus	4K4
SSX0	Set Status Transfer-sets the Status Request flip-flop	8R4
SX1	Status Transfer-Status Request flip-flop	4D6
SYN0	Sync to MPX-Bus	3R7
TAAR0	Toggle Auxiliary Address Register-increments Auxiliary Address Register	8N2
TACK0	Transmit Acknowledge-to lower priority device on the MPX Bus	8H1
TPC0	Transmit Priority Chain from EDMA Bus	9J3
UAARH0	Unload Auxiliary Address Register High-unload Auxiliary Address Register Bits 04:11	6D4
UAARL0	Unload Auxiliary Address Register Low-unload Auxiliary Address Register Bits 12:19	6D4
UAARX0	Unload Auxiliary Address Register Extended-unload Auxiliary Address Register Bits 00:03	6D5
WT1	Write flip-flop	4F5
XREQ0	Request-request EDMA Bus for service	9M2

DISPLAY PANEL

09-065R03A12
May 1978

METRIC

M71-102
HEXADECIMAL DISPLAY
INFORMATION SPECIFICATION

1. INTRODUCTION

The optional Hexadecimal Display Panel provides a means to manually control the Processor, interrogate and display various Processor registers and machine status, set and display Processor memory locations, and may be programmed as an I/O device by the user.

This specification describes the 09-065F02 Hexadecimal Display Panel (Product Number M71-102). It is also applicable to the 09-065F01 Binary Display Panel (Product Number M71-101), which is identical to the Hexadecimal Display Panel except for the omission of the hexadecimal indicators. The Hexadecimal Display Panel provides the following functions:

Displays five bytes of programmable digital information.

Registers and displays five hexadecimal digits of manually entered keyboard data.

Displays the WAIT and Power (PWR) indicators for the Processor.

Provides a 26 key control keyboard for manual input to the display.

Provides two bytes of unbuffered Switch Register data to the Processor.

Provides one byte of status to the Processor.

Provides a three position OFF-ON-LOCK key type switch capable of switching three separate power supply control lines.

Provides a control signal to the Processor that the display requires micro-program support.

2. GENERAL DESCRIPTION

A complete description of the operation of the Hexadecimal Display Panel is provided in the appropriate User's Manual. This specification describes the display from a maintenance view point. Figure 1 shows the Hexadecimal Display Panel.

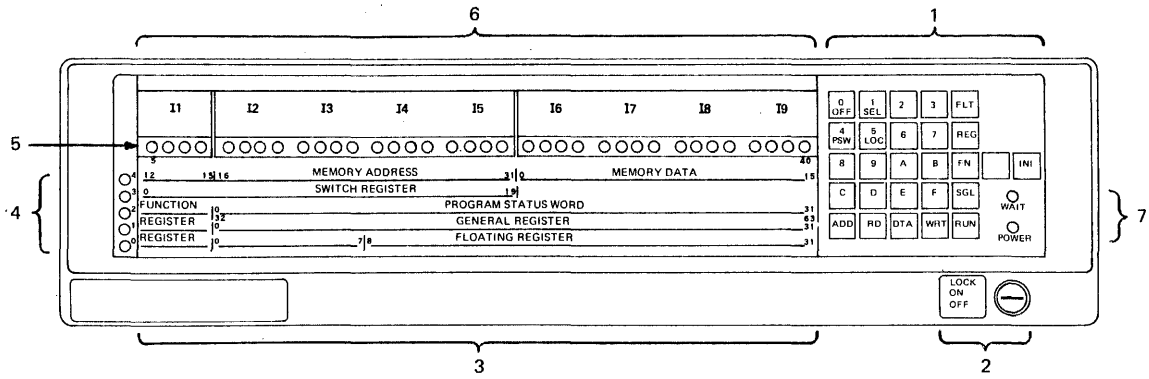


Figure 1. Hexadecimal Display Panel

Various parts of the Hexadecimal Display Panel in Figure 1 are numbered to correlate to the following descriptions.

1. Control Keyboard. The keyboard is the operators manual input to the Processor. The function of the specific keys are:

DTA — The function of the Data (DTA) key is to clear the Switch Register, connect the Switch Register to the display indicators, and enable hexadecimal data to be entered into the register. The Switch Register remains enabled and connected to the display indicators until any non-hexadecimal key other than DTA is depressed.

Hexadecimal Keys 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F supply data to the Switch Register when it is enabled, and the function number or register number for the Processor supported display (see Section 2.2).

ADD — The Address (ADD) key causes the Processor to read the five hexadecimal characters of the Switch Register, store them in the address portion of the Program Status Word (PSW), and display PSW 32:63 on the indicators.

RD — The Read (RD) key causes the Processor to read the memory location specified by the PSW, increment the PSW address by two, and display on the indicators the new address and the data read from memory.

WRT — Depressing the Write (WRT) key causes the data contained in the Switch Register to be written into the address specified by the PSW, the PSW to be incremented by two, and the new address and the data written to be displayed on the indicators.

FLT — Depressing the Floating-Point Register (FLT) key, followed by any hexadecimal key n, causes Floating-Point Register n to be displayed on the indicators.

REG — Depressing the Register (REG) key, followed by any hexadecimal key n, causes general register n to be displayed.

FN — Depressing the Function (FN) key, followed by any hexadecimal key n, causes the Processor to perform "Function n" as described in the appropriate User's Manual.

SGL — Depressing the Single Step (SGL) key causes the Processor to execute one user instruction and display the last register or function selected.

RUN — Depressing the Run (RUN) key causes the Processor to enter the Run mode at the address specified by the PSW.

INI — Depressing the Initialize (INI) key initializes the Processor.

SEL — Depress DTA, then 0 or F, for selection of Register Set 0 or 1 respectively. Then depress the Function (FN) Key followed by SEL to enable the selected register set to be displayed.

NOTE

The display requires support from the micro-program for all functions other than entering or displaying Switch Register data.

2. OFF-ON-LOCK Key Operated Locking Switch. This switch controls the power to the Processor and allows the keyboard to be completely disabled in the LOCK position.

3. Indicator Formats. These formats aid the user in interpreting the display indicators.

4. Format Selectors L0:4. Light Emitting Diode (LED) indicators L0:4 determine the format to be used to interpret display indicators L5:40.

5. Display Indicators L5:40. These LED indicators are used to display the PSW, general registers, etc., as described by the indicator formats.

6. Display Indicators I1:9. These indicators display the corresponding values displayed on L5:40 in the hexadecimal format.

7. WAIT and PWR. These indicators are illuminated when Processor is in the Wait state and Power is supplied to the Processor.

2.1 Switch Register Entries

When the operator is manipulating the Switch Register, there is no interaction between the display and the Processor. Data is entered into this register by first depressing the DTA key. This operation clears the Switch Register; connects the Switch Register to L5:24 of the display, and allows subsequent hexadecimal keyboard entries to be left shifted into the least significant digit of the resigter. The register is disconnected from the display and disabled when any non-hexadecimal key other than DTA is depressed. The register can be momentarily examined when it is disabled without affecting the Processor operation by depressing any hexadecimal key.

2.2 Processor Intervention

Depressing the following single keys causes the signals ESNC0 and ESNO0 to be complimentarily pulsed (ESNC0 is a positive going pulse):

ADD
RD
WRT
SGL
RUN

Depressing one of the following sequences of two keys causes a similar action:

FLT n (n is any hexadecimal digit)
REG n
FN n

3. FUNCTIONAL DIAGRAM ANALYSIS AND CIRCUIT DESCRIPTION

Refer to Figure 2. Hexadecimal Display Panel Block Diagram and Functional Schematic 09-065D08.

3.1 OFF-ON-LOCK Switch

This switch (2K1) controls power to the Processor by completing the circuit between CONT2 and CONT1 in the ON and LOCK positions. The switch is factory wired to provide one set of closures. This switch also provides a hard ground to the Processor as POFF0 in the OFF position which may be used as an early power down indication. When the switch is in the ON position, LP5 (2L1) is provided to the keyboard to enable the sensing of these switch closures.

3.2 Keyboard

The keyboard (Sheet 2) has a 5 x 5 switch array which is used to enter information to the Hexadecimal Display Panel logic, plus an Initialize (INI) key used to transmit this condition to the Processor (2G1). The keyboard is a self-contained unit and connects to the 35-520 logic board by 27 stakes, 00-1 through 26-1. These normally open switches are encoded by diode logic (Sheet 2) to form HEX01:31 (2B8) and FUN00:30 (2C8), plus a few additional control signals mentioned later in this description. The switches are designed to be high active when a switch is depressed by biasing all receiving gates low with a 220 ohm input resistor. A switch being depressed causes an input gate to go high by supplying LP5 through a current limiting resistor from the common input, Pin 0, if the OFF-ON-LOCK switch is in the ON position. There is no keyboard rollover protection and if more than one key is simultaneously depressed, the result is unspecified.

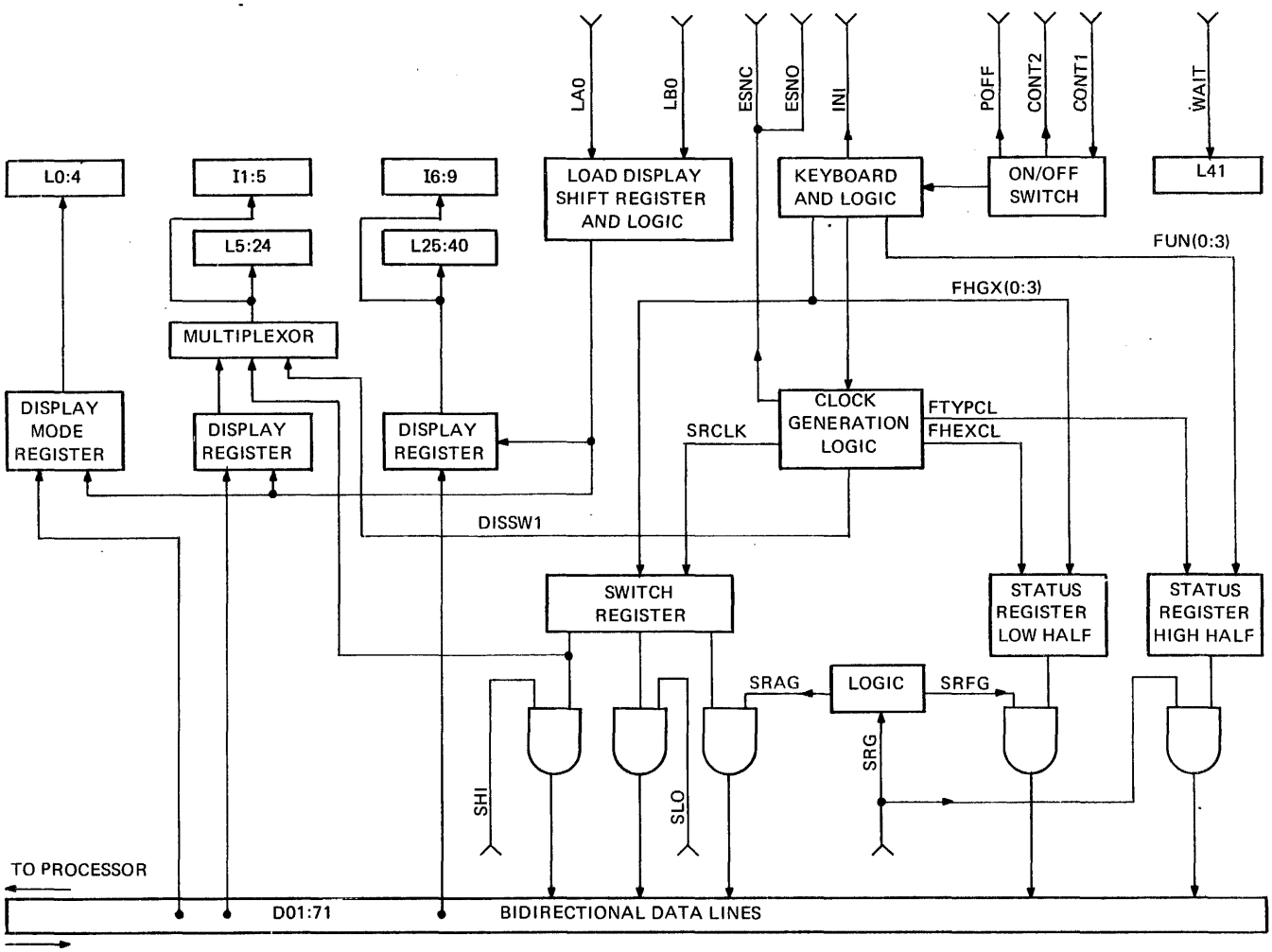


Figure 2. Hexadecimal Display Panel Block Diagram

3.3 Matrix Encoding

The diode matrix is encoded to drive signals HEX01:31 to the hexadecimal equivalent of the respective key 0:F (HEX31 is the LSB) when it is depressed. Depressing any function key other than DTA causes FUN00:30 to yield the codes specified by Table 1.

TABLE 1. FUNCTION KEY ENCODING (FUN00:30)

Key Depressed	FUN00	FUN10	FUN20	FUN30
SGL	0	1	1	1
RUN	1	1	1	1
WRT	1	1	0	1
RD	1	0	1	1
ADD	1	0	0	1
REG	0	1	1	0
FLT	0	1	0	0
FN	0	1	1	1

3.4 Clocking

Depressing any keyboard key other than DTA or INI generates one of three types of clocks used by the Hexadecimal Display Panel logic. This is accomplished by a positive transition of signal KEY1 (2F8) whenever one of these keys is depressed. The one shot triggered by this transition (2G8) is used to allow a one to two millisecond interval for switch bounce to subside before triggering the second one shot STRB1 (2K8) which is used to generate one of the three clocks. Since contact bounce is likely to retrigger these one shots when a key is released, the occurrence of signal KEY1 (any key depressed), HKEY1 (2F9 a hexadecimal key depressed), or FKEY1 (2H7 a function key depressed) being true in coincedence with the one shot is used to derive the clocks.

3.5 Switch Register Clocks

The Switch Register is enabled for clocking by depressing the DTA key. This is accomplished by direct clearing the Switch Register Enable flip-flop (SRENB) (2L6) when DTA is depressed and ANDing the zero output of the flip-flop plus HKEY1 and STRB1 to drive the Switch Register Clock (SRCLK0) (2M7). This clock is disabled by setting SRENB with the occurrence of FKEY1 when any function key is depressed.

3.6 Status Register Clocks

Two different clocks are used to load the status register. FTYPCL0 (2M8) is generated whenever any function key other than DTA is depressed and is used to load FUN00:30 into one half of the status register. The second clock FHEXCL0 (2N8) is generated whenever a hexadecimal key is depressed if the previously depressed key was FN, REG, or FLT. In this case, the hexadecimal input would be the register number or function number desired and FHEXCL0 is used to clock HEX01:31 into the second half of the status register.

3.7 Processor Intervention

The logic of the display signals the Processor that a response is necessary to a console function by signal ESNC0 (2R7) and its compliment ESNO0 (2R7). These signals are complimentarily pulsed whenever a function key other than DTA, FN, REG, or FLT is depressed, or whenever a hexadecimal key is depressed following FN, REG, or FLT (the occurrence of FHEXCL0).

3.8 Switch Register Loading

The Switch Register (4B1, 4D1, 4G1, 4J1, and 4M1) is loaded with a hexadecimal character with the occurrence of each SRCLK0 as mentioned previously. Data is entered into the least significant character (4B1) from the switches (HEX01:31) and left shifted through the register with each clock. The register is cleared whenever the DTA key is depressed.

3.9 Status Register

The status register is loaded in two parts as described previously. One half is loaded from FUN00:30 when a Function (FN) key is depressed by the occurrence of FTYPCL0. The least significant bit of this register is re-circulated on SGL or RUN and the second LSB is re-circulated on SSL to conform to the status codes indicated in Table 2. The second half of the register is loaded from HEX01:31 with the occurrence of FHEXCL0. These registers are initialized by SCLR0 from the Processor.

TABLE 2. STATUS CODES

KEY	DL1	DL2	DL3	DL4	DL5	DL6	DL7	DL0
SGL	1	U	X	X	X	X	X	X
INITIALIZE	U	U	U	U	U	U	O	U
RUN	0	0	0	X	X	X	X	X
WRT	0	0	1	U	U	U	U	U
RD	0	1	0	U	U	U	U	U
ADR	0	1	1	U	A_1	A_2	A_3	A_4
REG n	1	0	0	1	n_1	n_2	n_3	n_4
FLT n	1	0	1	1	n_1	n_2	n_3	n_4
FN n	1	0	0	0	n_1	n_2	n_3	n_4

A = Most significant hexadecimal digit of Switch Register
U = Unspecified
X = Unchanged
n = Hexadecimal digit associated with function (see Section 6)

The display status is presented to the Processor on the data lines (DL01:71) for the duration of time that control signal SRG0 is at a logical zero level. The data presented for status is in accordance with Table 2.

3.10 Display Register Loading

The Hexadecimal Display Panel registers and displays five bytes of data transmitted from the Processor. Two control signals are transmitted from the Processor to direct the loading of these registers. LA0 (2K5) is a low active pulse which signifies that data is available on bi-directional Data Lines D01:71 and it is to be loaded into the least significant byte of the display register. LA0 is used to initialize a four bit shift register (2M4) to 1000_2 which is used to load subsequent bytes, and generate a load pulse LA1 which is used to load the data into the LSB of the display register (2B6 and 3E6). Four subsequent LB0 pulses sent from the Processor gates data from D01:71 into successive bytes of the display register (3G6 and 3J6, 4C5 and 4E5, 4G5 and 4K5, 4N5 and 3N2). This is accomplished as each LB0 pulse is inverted and gated as LDB1, LDC1, LDD1 and LDE1 (2N4) respectively as controlled by the sequencing shift register (2M4) which is right shifted with each LB0 pulse.

3.11 Display Indicators

The two least significant bytes of the display register are gated directly to LEDs L25:40 and the hexadecimal indicators I6:9 (Sheet 3). LEDs L5:24 and hexadecimal indicators I1:5 are used to display either the most significant bytes of the display registers or the Switch Register. These sets of registers are selected through the 2:1 multiplexors (4C6, 4E6, 4H6, 4K6 and 4N6) as determined by the state of the DISSW1 (2N6). DISSW1 is high whenever the Switch Register is enabled (SRENB1) or a hexadecimal key is depressed (HKEY1).

3.12 Processor Inputs

Data is gated to the Processor in response to control signals SHI0, SLO0 or SRG0. SLO0 gates the two least significant digits of the Switch Register onto the bi-directional Data Lines D01:71 (4C3 and 4C4). SHI0 gates the next two Switch Register digits onto the bi-directional Data Lines D01:71 (4H3 and 4K3). SRG0 causes the status register bits to be gated (3D4) as per Table 2. Note that either the most significant Switch Register character is gated (4N3) if DL11 is low or the hexadecimal portion of the status register if DL11 is high (3H4).

4. PROCESSOR INTERFACING

4.1 Processor Connector

Signals from the display are terminated at a 26-080F06 type connector per the following list:

SIGNAL	PIN	SIGNAL	PIN	*X1-X4	PIN
D01	109	LA0	203	X1	207
D11	110	LB0	114	X2	211
D21	111	SHI0	200	X3	210
D31	112	SLO0	206	X4	209
D41	202	WAIT1	102		
D51	204	SRG0	113		
D61	205	ESNC0	103		
D71	208	ESNO0	104		
POFF0	105	INIT0	101		
CONT1	DB1-C1 & 214	SSGL1	106		
CONT2	DB1-C2	GND	100-3		
CONT3	DB-C3 & 213	GND	108		
SCLR0	107	GND	212	twisted with 114	
		GND	201	twisted with 203	

*X1-X4 A1-8 leads to front terminal strip of chassis.

4.2 Timing

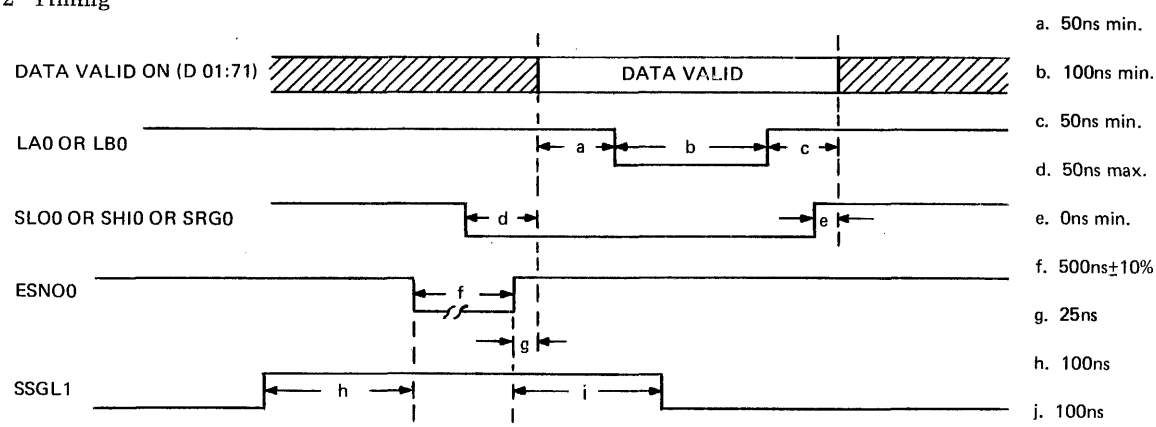


Figure 3. Hexadecimal Display Panel Timing

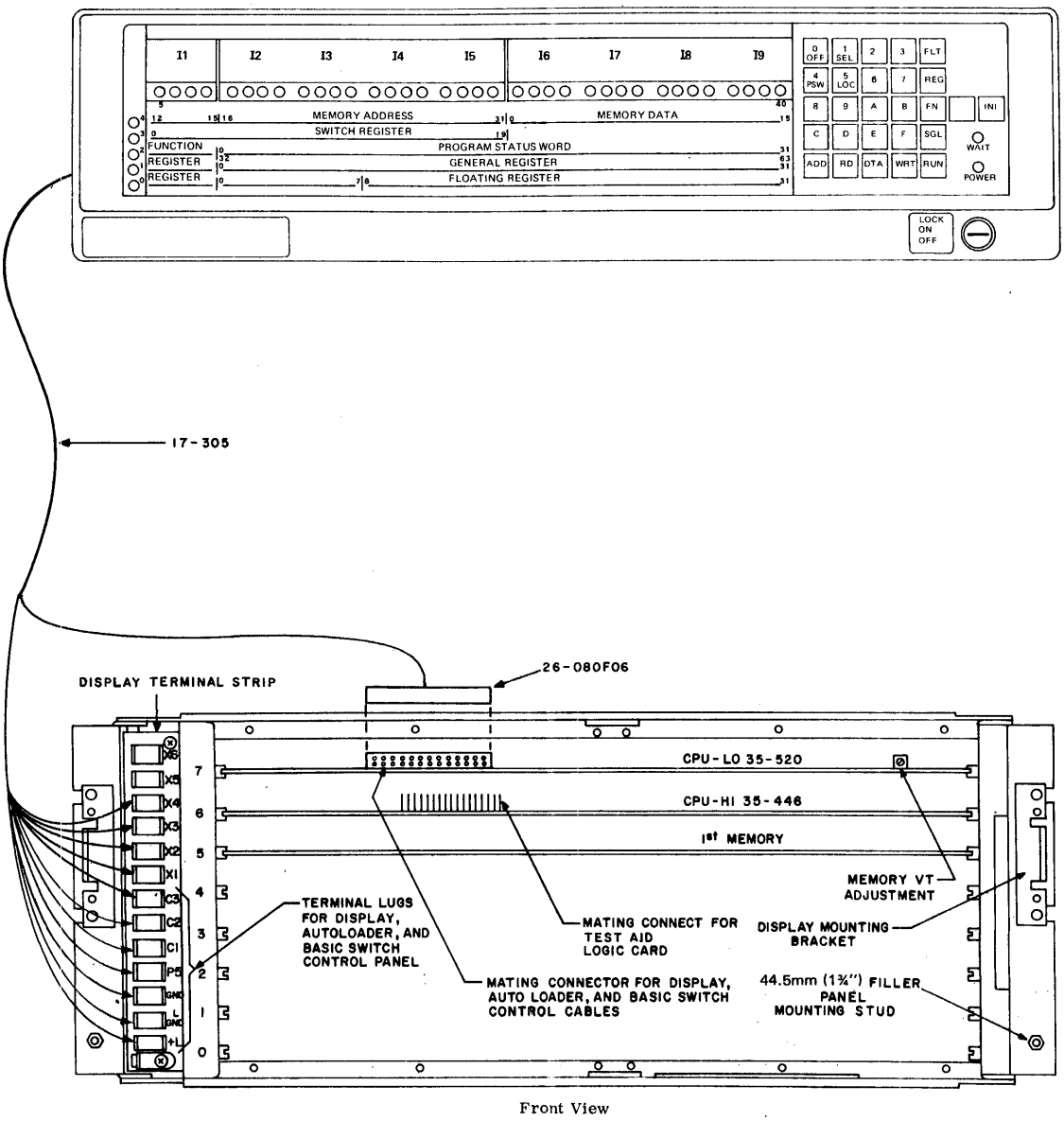
5. INSTALLATION PROCEDURE

The Hexadecimal Display Panel is connected to the Processor via a 17-305 cable. The 26-080F06 30-pin connector of the Hexadecimal Display Panel plugs into the mating connector as shown in Figures 4, 5 and 6.

CNTL1, CNTL2, P5, GND, LGND, +L jumpers go to corresponding lugs on the Processor chassis display terminal strip as shown in Figure 4.

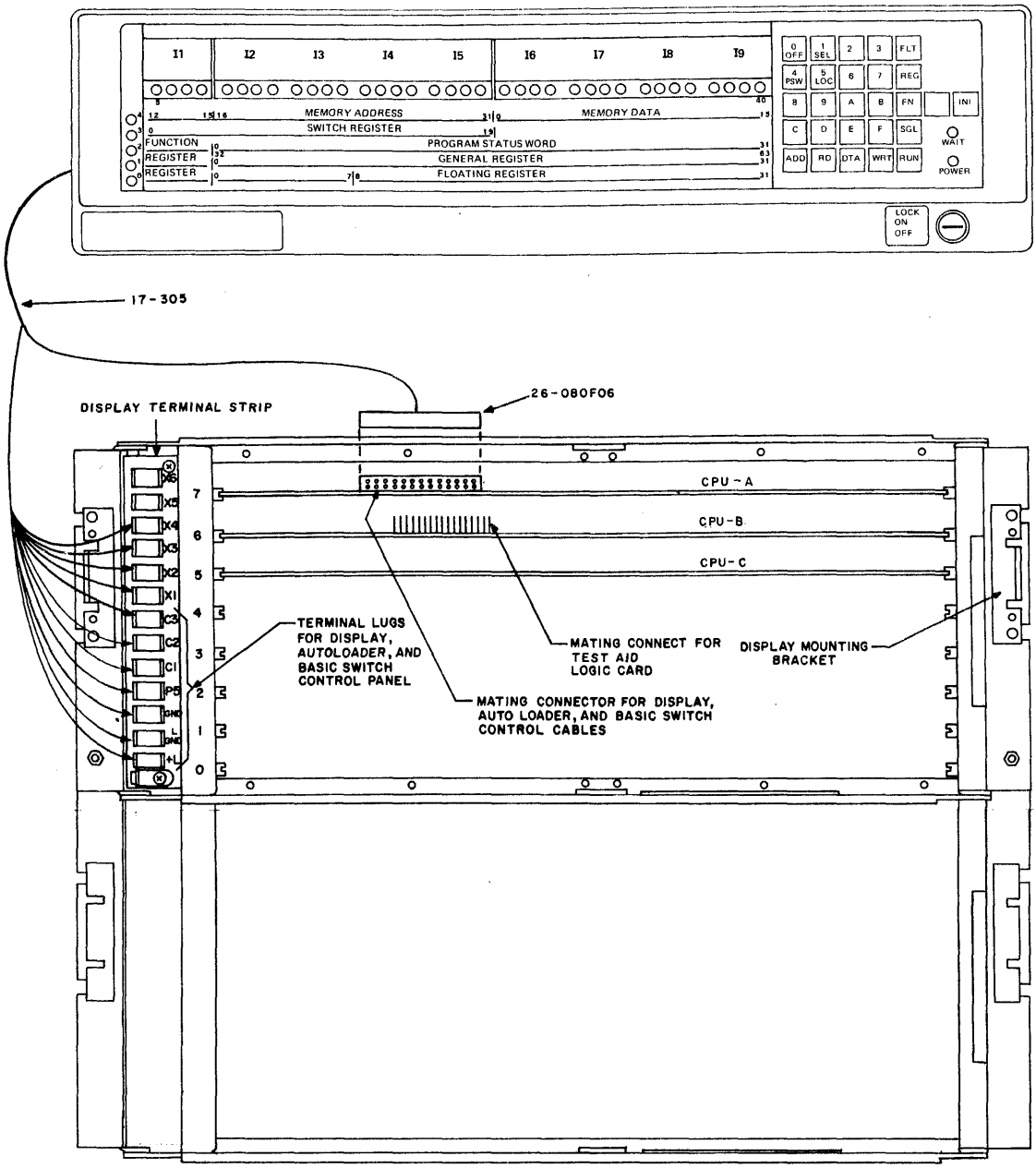
6. POWER

The Hexadecimal Display Panel draws its power from the P5 and +L lugs on the Processor chassis display terminal strip. See Figure 4.



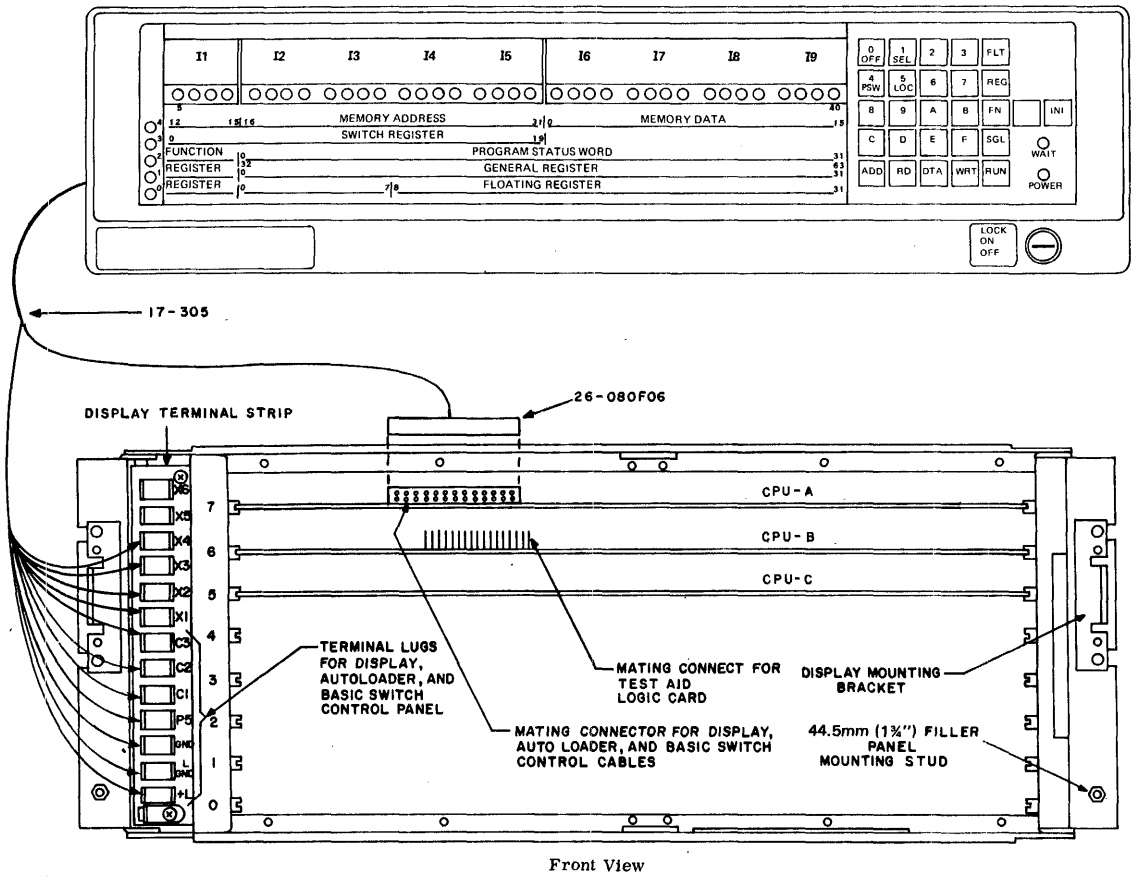
Front View

Figure 4. 7/16 Basic Display Installation



7/16 HSALU OR 7/32 TWIN CHASSIS INSTALLATION

Figure 5. Model 7/16 HSALU or 7/32 Installation



Front View

7/16 HSALU INSTALLATION

Figure 6. Model 7/16 HSALU Installation 7" Chassis

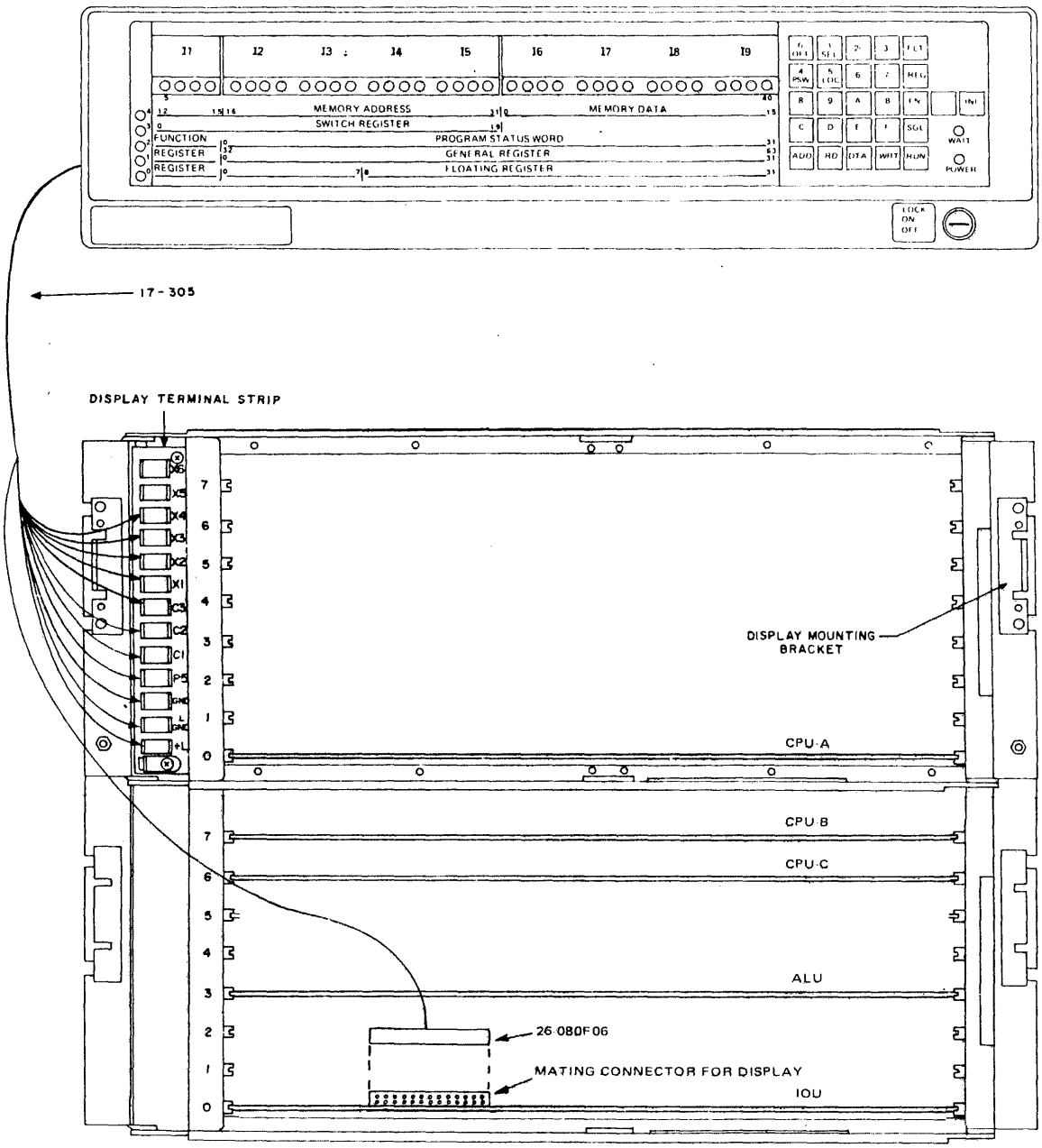


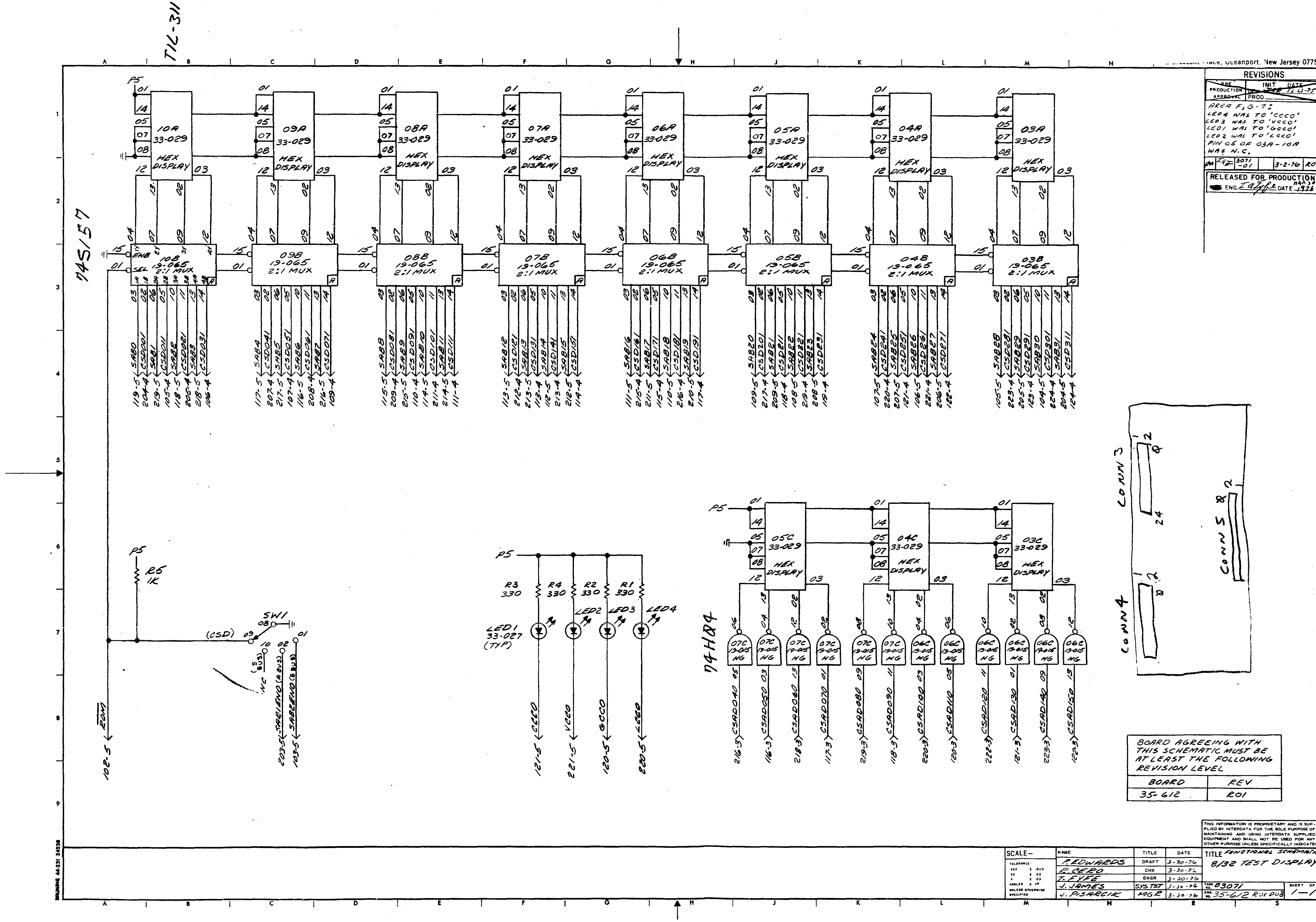
Figure 7. Model 8/32 Twin Chassis Installation

7. MNEMONICS

The following list provides a brief description of each mnemonic found in the Hexadecimal Display Panel. The source of each signal on Functional Schematic 09-065D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
CONT1	12 VAC to turn on power supply	2L1
CONT2	12 VAC to turn off power supply	2M1
DISSW1	Controls Display Multiplexors for L5:24	2R6
ESNC0	Execute switch normally open	2R7
ESNO0	Execute switch normally closed	2R7
FTYPCL0	Function type status register clock	2N7
FHEXCL0	Hexadecimal type status register clock	2N8
FUN00:30	Encoded functional keys	Sheet 2
HEX01:31	Encoded hexadecimal keys	Sheet 2
INIT0	Initialize Processor	2H2
LA0	Low active signal from Processor which initializes the loading sequence and loads the least significant byte of the Hexadecimal Display Panel	2K5
LB0	Low active signal from Processor used to control loading of display registers by generating LDB1, LDC1, LDD1, LDE1	2L5
LDB1	Load display registers	2R3
LDC1		2R4
LDD1		2R4
LDE1	Loads display mode register and most significant hexadecimal digit of the display	2R4
POFF0	Early power OFF failure	2K1
SCLR0	System Clear, initialize status registers	3J1
SDA0	DTA key depressed	2J2
SHI0	Switch Register high half gate command	2M2
SLO0	Switch Register low half gate command	2L3
SOR0	SGL or RUN keys depressed	2K2
SRAG1	Switch Register most significant hexadecimal digit gate command	2R2
SRCLK0	Switch Register clock	2M7
SRFG1	Status Register Function high half gate command	2R2
SRG1	Status Register low half gate command	2M2
SSL1	SGL key depressed	2J6
WAIT1	Wait light control	2M6

DRAWINGS



TIC-311
74S/57
74H04
Crescent Place, Oceanport, New Jersey 07757
REVISIONS
PRE PRODUCTION APPROVAL | INIT | DATE 12-23-75 | PROD
AREA F, G-7:
LED4 WAS TO 'CCCO'
LED3 WAS TO 'VCCO'
LED1 WAS TO 'GCCO'
LED2 WAS TO 'LCCO'
PIN 05 OF 03A-10A WAS N.C.
3071-01 | 3-2-76 | R01
RELEASED FOR PRODUCTION ENG. I a Fyfe DATE MAR 30 1976
P5
10A 33-029 HEX DISPLAY
09A 33-029 HEX DISPLAY
08A 33-029 HEX DISPLAY
07A 33-029 HEX DISPLAY
06A 33-029 HEX DISPLAY
05A 33-029 HEX DISPLAY
04A 33-029 HEX DISPLAY
03A 33-029 HEX DISPLAY
10B 19-065 2:1 MUX
09B 19-065 2:1 MUX
08B 19-065 2:1 MUX
07B 19-065 2:1 MUX
06B 19-065 2:1 MUX
05B 19-065 2:1 MUX
04B 19-065 2:1 MUX
03B 19-065 2:1 MUX
ENB SEL
SAB0 CSD001 SAB1 CSD011 SAB2 CSD021 SAB3 CSD031
119-5 204-4 219-5 105-4 118-5 205-4 218-5 106-4
SAB4 CSD041 SAB5 CSD051 SAB6 CSD061 SAB7 CSD071
117-5 207-4 217-5 107-4 116-5 208-4 216-5 109-4
SAB8 CSD081 SAB9 CSD091 SAB10 CSD101 SAB11 CSD111
115-5 209-4 215-5 110-4 114-5 211-4 214-5 111-4
SAB12 CSD121 SAB13 CSD131 SAB14 CSD141 SAB15 CSD151
113-5 212-4 213-5 113-4 112-5 213-4 212-5 114-4
SAB16 CSD161 SAB17 CSD171 SAB18 CSD181 SAB19 CSD191
111-5 215-4 211-5 115-4 110-5 216-4 210-5 117-4
SAB20 CSD201 SAB21 CSD211 SAB22 CSD221 SAB23 CSD231
109-5 217-4 209-5 118-4 108-5 219-4 208-5 119-4
SAB24 CSD241 SAB25 CSD251 SAB26 CSD261 SAB27 CSD271
107-5 220-4 207-5 121-4 106-5 221-4 206-5 122-4
SAB28 CSD281 SAB29 CSD291 SAB30 CSD301 SAB31 CSD311
105-5 223-4 205-5 123-4 104-5 224-4 204-5 124-4
R5 1K
SW1
(CSD)
(S BUS) NC
SAB1ENO (A BUS)
SAB2ENO (B BUS)
ROM
102-5
203-5
103-5
R3 330
R4 330
R2 330
R1 330
LED1 33-027 (TYP)
LED2
LED3
LED4
CCCO VCCO GCCO LCCO
121-5 221-5 120-5 220-5
05C 33-029 HEX DISPLAY
04C 33-029 HEX DISPLAY
03C 33-029 HEX DISPLAY
07C 19-015 HG
06C 19-015 HG
CSAD040 CSAD050 CSAD060 CSAD070 CSAD080 CSAD090 CSAD100 CSAD110 CSAD120 CSAD130 CSAD140 CSAD150
216-3 116-3 218-3 117-3 219-3 118-3 220-3 120-3 222-3 121-3 223-3 122-3
CONN 3
CONN 4
CONN 5
BOARD AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL
BOARD | REV
35-612 | R01
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.
SCALE–
TOLERANCE: .XXX ± .005 .XX ± .02 .X ± .03 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED
NAME | TITLE | DATE
P. EDWARDS | DRAFT | 3-30-76
R. CERO | CHK | 3-30-76
T. FYFE | ENGR | 3-30-76
J. JAMES | SYS TST | 3-30-76
J. PISARCIK | MGR | 3-30-76
TITLE FUNCTIONAL SCHEMATIC 8/32 TEST DISPLAY
TASK NO. 03071
DWG. NO. 35-612 R01 D08
SHEET 1 OF 1
BRUNING 44-231 24538

PERKIN-ELMER

BACK PANEL MAP

CONN.	TITLE	CPB		DCB		DFU		ALU		CONN.
	BD. LOC	AA07		AA06		AA05		AA04		
	TERM.	ROW		ROW		ROW		ROW		
	NO.	1	2	1	2	1	2	1	2	
1	41	P5	P5	P5	P5	P5	P5	P5	P5	1
	40	GND	GND	GND	GND	GND	GND	GND	GND	
	39	DSPYL1	PPFO							
	38	ATNO20	ATNO30							
	37	ATN000	ATN010							
	36	GND	GND	GND	GND	GND	GND	GND	GND	
	35	B300	B310	B300	B310	B300	B310	B300	B310	
	34	B280	B290	B280	B290	B280	B290	B280	B290	
	33	B260	B270	B260	B270	B260	B270	B260	B270	
	32	B240	B250	B240	B250	B240	B250	B240	B250	
	31	GND	GND	GND	GND	GND	GND	GND	GND	
	30	B220	B230	B220	B230	B220	B230	B220	B230	
	29	B200	B210	B200	B210	B200	B210	B200	B200	
	28	B180	B190	B180	B190	B180	B190	B180	B180	
	27	B160	B170	B160	B170	B160	B170	B160	B160	
	26	GND	GND	GND	GND	GND	GND	GND	GND	
	25	S300	S310	S300	S310	S300	S310	S300	S300	
	24	S280	S290	S280	S290	S280	S290	S280	S280	
	23	S260	S270	S260	S270	S260	S270	S260	S260	
	22	S240	S250	S240	S250	S240	S250	S240	S240	
	21	GND	GND	GND	GND	GND	GND	GND	GND	
	20	S220	S230	S220	S230	S220	S230	S220	S230	
	19	S200	S210	S200	S210	S200	S210	S200	S210	
	18	S180	S190	S180	S190	S180	S190	S180	S190	
	17	S160	S170	S160	S170	S160	S170	S160	S170	
	16	GND	GND	GND	GND	GND	GND	GND	GND	
	15	A300	A310	A300	A310	A300	A310	A300	A310	
	14	A280	A290	A280	A290	A280	A290	A280	A290	
	13	A260	A270	A260	A270	A260	A270	A260	A270	
	12	A240	A250	A240	A250	A240	A250	A240	A250	
	11	GND	GND	GND	GND	GND	GND	GND	GND	
	10	A220	A230	A220	A230	A220	A230	A220	A230	
	09	A200	A210	A200	A210	A200	A210	A200	A210	
	08	A180	A190	A180	A190	A180	A190	A180	A190	
	07	A160	A170	A160	A170	A160	A170	A160	A170	
	06	GND	GND	GND	GND	GND	GND	GND	GND	
	05	MMF0	PSW230							
	04									
	03	MSEL020	RWCO	MSEL020	RWCO	MSEL020	RWCO	MSEL020	RWCO	
	02	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	
	01	GND	MSIGO	GND	MSIGO	GND	MSIGO	GND	MSIGO	
	00	P5	P5	P5	P5	P5	P5	P5	P5	
		1	2	1	2	1	2	1	2	
	41	P5	P5	P5	P5	P5	P5	P5	P5	
	40	GND	KSIGO	GND	KSIGO	GND	KSIGO	GND	KSIGO	
	39	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	
	38	FSEL000	FSEL010	FSEL000	FSEL010	FSEL000	FSEL010	FSEL000	FSEL010	
	37	STRT0	MFINO	STRT0	MFINO	STRT0	MFINO	STRT0	MFINO	
	36	GND	GND	GND	GND	GND	GND	GND	GND	
	35	B140	B150	B140	B150	B140	B150	B140	B150	
	34	B120	B130	B120	B130	B120	B130	B120	B130	
	33	B100	B110	B100	B110	B100	B110	B100	B110	
	32	B080	B090	B080	B090	B080	B090	B080	B090	
	31	GND	GND	GND	GND	GND	GND	GND	GND	
	30	B060	B070	B060	B070	B060	B070	B060	B070	
	29	B040	B050	B040	B050	B040	B050	B040	B050	
	28	B020	B030	B020	B030	B020	B030	B020	B030	
	27	B000	B010	B000	B010	B000	B010	B000	B010	
	26	GND	GND	GND	GND	GND	GND	GND	GND	
	25	S140	S150	S140	S150	S140	S150	S140	S150	
	24	S120	S130	S120	S130	S120	S130	S120	S130	
	23	S100	S110	S100	S110	S100	S110	S100	S110	
	22	S080	S090	S080	S090	S080	S090	S080	S090	
	21	GND	GND	GND	GND	GND	GND	GND	GND	
0	20	S060	S070	S060	S070	S060	S070	S060	S070	0
	19	S040	S050	S040	S050	S040	S050	S040	S050	
	18	S020	S030	S020	S030	S020	S030	S020	S030	
	17	S000	S010	S000	S010	S000	S010	S000	S010	
	16	GND	GND	GND	GND	GND	GND	GND	GND	
	15	A140	A150	A140	A150	A140	A150	A140	A150	
	14	A120	A130	A120	A130	A120	A130	A120	A130	
	13	A100	A110	A100	A110	A100	A110	A100	A110	
	12	A080	A090	A080	A090	A080	A090	A080	A090	
	11	GND	GND	GND	GND	GND	GND	GND	GND	
	10	A060	A070	A060	A070	A060	A070	A060	A070	
	09	A040	A050	A040	A050	A040	A050	A040	A050	
	08	A020	A030	A020	A030	A020	A030	A020	A030	
	07	A000	A010	A000	A010	A000	A010	A000	A010	
	06	GND	GND	GND	GND	GND	GND	GND	GND	
	05	SCLR0	CCCO	SCLR0	CCCO	SCLR0	CCCO	SCLR0	CCCO	
	04	SCC0	VCCO	SCC0	VCCO	SCC0	VCCO	SCC0	VCCO	
	03	SCLR1	GCCO	SCLR1	GCCO	SCLR1	GCCO	SCLR1	GCCO	
	02	TKILLO	LCCO		LCCO		LCCO		LCCO	
	01	GND	GND	GND	GND	GND	GND	GND	GND	
	00	P5	P5	P5	P5	P5	P5	P5	P5	
		1	2	1	2	1	2	1	2	

CONN.	TITLE	IOU	I/O	I/O	I/O	CONN.
	BD. LOC.	AA03	AA02	AA01	AA00	
	TERM.	ROW	ROW	ROW	ROW	
	NO.	1 2	1 2	1 2	1 2	
1	41	P5 P5	P5 GND	P5 GND	P5 GND	1
	40	GND GND	GND GND	GND GND	GND GND	
	39	P15 PPFO				
	38	N15 DSPYLO				
	37	RACKO TACKO	DMAI70 DGND	DMAI70 DGND	DMAI70 DGND	
	36	GND GND	DMAI50 DMAI60	DMAI50 DMAI60	DMAI50 DMAI60	
	35	B300 B310	DMAI30 DMAI40	DMAI30 DMAI40	DMAI30 DMAI40	
	34	B280 B290	DGND DMAI20	DGND DMAI20	DGND DMAI20	
	33	B260 B270	DMAI10 DMAI00	DMAI10 DMAI00	DMAI10 DMAI00	
	32	B240 B250	DMA090 DMA080	DMA090 DMA080	DMA090 DMA080	
	31	GND GND	DMA070 DMA060	DMA070 DMA060	DMA070 DMA060	
	30	B220 B230	DMA050 DGND	DMA050 DGND	DMA050 DGND	
	29	B200 B210	DMA030 DMA040	DMA030 DMA040	DMA030 DMA040	
	28	B180 B190	DMA010 DMA020	DMA010 DMA020	DMA010 DMA020	
	27	B160 B170	DGND DMA000	DGND DMA000	DGND DMA000	
	26	GND GND	SCLR0 HWO	SCLR0 HWO	SCLR0 HWO	
	25	S300 S310			PATNO SREQO	
	24	S280 S290			XFER0 TERM0	
	23	S260 S270	SYNO ATNO	SYNO ATNO	SYNO ATNO	
	22	S240 S250	PACKO TACKO	CLO70 DA0	PACKO TACKO	
	21	GND GND	CLO70 DA0	DR0 CMD0	CLO70 DA0	
1	20	S220 S230	DR0 CMD0	SR0 ADR30	DR0 CMD0	1
	19	S200 S210	SR0 ADR30	DI40 DI50	SR0 ADR30	
	18	S180 S190	DI40 DI50	DI20 DI30	DI40 DI50	
	17	S160 S170	DI20 DI30	DI00 DI10	DI20 DI30	
	16	GND GND	DI00 DI10	DO80 DO90	DI00 DI10	
	15	A300 A310	DO80 DO90	DO60 DO70	DO80 DO90	
	14	A280 A290	DO60 DO70	DO40 DO50	DO60 DO70	
	13	A260 A270	DO40 DO50	DO20 DO30	DO40 DO50	
	12	A240 A250	DO20 DO30	DO00 DO10	DO20 DO30	
	11	GND GND	DO00 DO10		DO00 DO10	
	10	A220 A230	DMX140		DMX140	
	09	A200 A210	DMX150 DMX120	DMX150 DMX120	DMX150 DMX120	
	08	A180 A190	DMX130 DGND	DMX130 DGND	DMX130 DGND	
	07	A160 A170	M3B20 M2B20	M3B20 M2B20	M3B20 M2B20	
	06	GND GND	M1B20 M0B20	M1B20 M0B20	M1B20 M0B20	
	05	MMF0 * IRLMP0 *	LOAD0 AN50	LOAD0 AN50	LOAD0 AN50	
	04	MMEPF0 * DMPF0 *	LMEQO DGND	LMEQO DGND	LMEQO DGND	
	03	MSEL020	SOTO EOTO	SOTO EOTO	SOTO EOTO	
	02	MSEL000 MSEL010	XEEQO QUEO	XEEQO QUEO	XEEQO QUEO	
	01	GND MSIGO	GND GND	GND GND	GND GND	
	00	P5 P5	P5 GND	P5 GND	P5 GND	
		1 2	1 2	1 2	1 2	
	41	P5 P5	P5 GND	P5 GND	P5 GND	
	40	GND KSIGO	GND GND	GND GND	GND GND	
	39	FSEL020 FSEL030				
	38	FSEL000 FSEL010				
	37	STRT0 MFINO	RPCO TPCO	RPCO TPCO	RPCO TPCO	
	36	GND GND	DGND BHO	DGND BHO	DGND BHO	
	35					
	34	GND GND		↑	XRACKO	
	33					
	32	MAR310				
	31	GND GND				
	30	ACKO30				
	29	ACKO20				
	28	ACKO10 GND	PRPCO PRPCO	PRPCO PRPCO	PRPCO PRPCO	
	27	ACKO00 HWC				
	26	GND GND	SCLR0 HWO	SCLR0 HWO	SCLR0 HWO	
	25	GND GND			PATNO SREQO	
	24				XFER0 TERM0	
	23	SYNO ATNO	SYNO ATNO	SYNO ATNO	SYNO ATNO	
0	22	CLO70 DA0	PACKO TACKO	CLO70 DA0	PACKO TACKO	0
	21	GND GND	CLO70 DA0	CLO70 DA0	CLO70 DA0	
	20	DR0 CMD0	DR0 CMD0	DR0 CMD0	DR0 CMD0	
	19	SR0 ADR30	SR0 ADR30	SR0 ADR30	SR0 ADR30	
	18	DI40 DI50	DI40 DI50	DI40 DI50	DI40 DI50	
	17	DI20 DI30	DI20 DI30	DI20 DI30	DI20 DI30	
	16	GND GND	DI00 DI10	DI00 DI10	DI00 DI10	
	15	DI00 DI10	DO80 DO90	DO80 DO90	DO80 DO90	
	14	DO80 DO90	DO60 DO70	DO60 DO70	DO60 DO70	
	13	DO60 DO70	DO40 DO50	DO40 DO50	DO40 DO50	
	12	DO40 DO50	DO20 DO30	DO20 DO30	DO20 DO30	
	11	GND GND	DO00 DO10	DO00 DO10	DO00 DO10	
	10	DO20 DO30				
	09	DO00 DO10				
	08					
	07					
	06	GND GND				
	05	SCLR0 CCCO				
	04	SCC0 VCCO				
	03	SCLR1 GCCO				
	02	LCCO				
	01	GND GND	GND GND	GND GND	GND GND	
	00	P5 P5	P5 GND	P5 GND	P5 GND	
		1 2	1 2	1 2	1 2	

NOTES
1. BACKPANEL - 35-541
Ⓦ WIRE WRAP RUN

RELEASED FOR PRODUCTION — ENG. — DATE

PRE PRODUCTION APPROVAL — INIT — DATE — DEV — PROD

SHEET INDEX — REV. LEV. 5 3 3 5 — SHT NO. 1 2 3 4

SEE SHEET 4 FOR REVISION INFO.

NAME	TITLE	DATE
G. MELTON	DRAFT	6-10-74
G. J. HOMEFIELD	CHK	10-10-74
T. FYFE	ENGR	
S. MESSINA	DIR ENG	

TITLE 8/32 BACKPANEL LOWER

DWG 03053 — SHEET OF 1 4

01-078205D08

PERKIN ELMER

BACK PANEL MAP

CONN.	TITLE / BD LOC / TERM. NO.	LMM A07 ROW 1	LMM A07 ROW 2	LMI NOTE 2 A06 ROW 1	LMI NOTE 2 A06 ROW 2	LMM A05 ROW 1	LMM A05 ROW 2	LMM A04 ROW 1	LMM A04 ROW 2
1	41	PS	GND	PS	PS	PS	GND	PS	GND
	40	GND	GND	GND	GND	GND	GND	GND	GND
	39	PIS	PIS			PIS	PIS	PIS	PIS
	38	NIS	NIS			NIS	NIS	NIS	NIS
	37	MDI50	MDI60	MDI50	MDI60	MDI50	MDI60	MDI50	MDI60
	36	MDI30	MDI40	MDI30	MDI40	MDI30	MDI40	MDI30	MDI40
	35	MDI10	MDI20	MDI10	MDI20	MDI10	MDI20	MDI10	MDI20
	34	MDO90	MDI00	MDO90	MDI00	MDO90	MDI00	MDO90	MDI00
	33	MDO70	MDO80	MDO70	MDO80	MDO70	MDO80	MDO70	MDO80
	32	MDO50	MDO60	MDO50	MDO60	MDO50	MDO60	MDO50	MDO60
	31	MDO30	MDO40	MDO30	MDO40	MDO30	MDO40	MDO30	MDO40
	30	MDO10	MDO20	MDO10	MDO20	MDO10	MDO20	MDO10	MDO20
	29	GND	MDO00	GND	MDO00	GND	MDO00	GND	MDO00
	28	TEMPA ⊗	VT	WRTO	TEMP B ⊗	TEMPA ⊗	VT	WRTO	TEMP B ⊗
	27	WRTO	TEMP B ⊗	OWRTO		WRTO	TEMP B ⊗	WRTO	TEMP B ⊗
	26	GND	GND	GND	GND	GND	GND	GND	GND
	25	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310
	24	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290
	23	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270
	22	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250
	21	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230
	20	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210
	19	GND	GND	GND	GND	GND	GND	GND	GND
	18								
	17								
	16	GND	GND	GND	GND	GND	GND	GND	GND
	15								
	14								
	13								
	12								
	11	GND	GND	GND	GND	GND	GND	GND	GND
	10		MS000	EWRTO	MS000 ⊗	EWRTO	MS000		MS000
	09	MS010	MS020	MS010	MS020	MS010	MS020	MS010	MS020
	08	MS030	MS040	MS030	MS040	MS030	MS040	MS030	MS040
	07	MS050	MS060	MS050	MS060	MS050	MS060	MS050	MS060
	06	MS070	MS080	MS070	MS080	MS070	MS080	MS070	MS080
	05	MS090	MS100	MS090	MS100	MS090	MS100	MS090	MS100
	04	MS110	MS120	MS110	MS120	MS110	MS120	MS110	MS120
	03	MS130	MS140	MS130	MS140	MS130	MS140	MS130	MS140
	02	MS150	MS160	MS150	MS160	MS150	MS160	MS150	MS160
	01	GND	GND	GND	GND	GND	GND	GND	GND
	00	PS	GND	PS	PS	PS	GND	PS	GND
		1	2	1	2	1	2	1	2
0	41	PS	GND	PS	PS	PS	GND	PS	GND
	40	GND	GND	GND	GND	GND	GND	GND	GND
	39	LMBSYA0	LMBSYC0	LMBSYA0	LMBSYC0	LMBSYA0	LMBSYC0	LMBSYA0	LMBSYC0
	38	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMDS0
	37	LMBSYB0	LMRS0	LMBSYB0	LMRS0	LMBSYB0	LMRS0	LMBSYB0	LMRS0
	36	GND	GND	GND	GND	GND	GND	GND	GND
	35	DUA0	MBZ0	DUA0	MBZ0	DUA0	MBZ0	DUA0	MBZ0
	34	GND	GND	GND	GND	GND	GND	GND	GND
	33	MA130	MA140	MA130	MA140	MA130	MA140	MA130	MA140
	32	MA110	MA120	MA110	MA120	MA110	MA120	MA110	MA120
	31	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100
	30	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080
	29	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060
	28	GND	GND	GND	GND	GND	GND	GND	GND
	27	SCLR0		SCLR0		SCLR0		SCLR0	
	26	MCLR0	GND	MCLR0	GND	MCLR0	GND	MCLR0	GND
	25	GND	GND	GND	GND	GND	GND	GND	GND
	24	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190
	23	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170
	22	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150
	21	GND	GND	GND	GND	GND	GND	GND	GND
	20	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130
	19	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110
	18	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090
	17	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070
	16	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050
	15	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030
	14	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010
	13	GND	GND	GND	GND	GND	GND	GND	GND
	12	IRLMP0	DLMP0	IRLMP0	DLMP0	IRLMP0	DLMP0	IRLMP0	DLMP0
	11	GND	GND	GND	GND	GND	GND	GND	GND
	10	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040
	09	MA020		MA020		MA020		MA020	
	08	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070
	07	MA010		MA010		MA010		MA010	
	06	MA000		MA000	GND	MA000		MA000	
	05	PAR0		PAR0		PAR0		PAR0	
	04	INH0	ER0	INH0	ER0	INH0	ER0	INH0	ER0
	03		SPY		SPY		SPY		SPY
	02	PIS	NIS					PIS	NIS
	01	GND	GND	GND	GND	GND	GND	GND	GND
	00	PS	GND	PS	PS	PS	GND	PS	GND
		1	2	1	2	1	2	1	2

CONN.	TITLE / BD.LOC. / TERM. NO.	LMI (NOTE 2) A03 ROW 1	LMI (NOTE 2) A03 ROW 2	LMM A02 ROW 1	LMM A02 ROW 2	MBC A01 ROW 1	MBC A01 ROW 2	CPA A00 ROW 1	CPA A00 ROW 2
1	41	PS	PS	PS	GND	PS	PS	PS	PS
	40	GND	GND	GND	GND	GND	QUE0	GND	MSIG0
	39					DMA160	DMA170	B300	B310
	38					DMA140	DMA150	B280	B290
	37	MDI50	MDI60	MDI50	MDI60	DMA120	DMA130	B260	B270
	36	MDI30	MDI40	MDI30	MDI40	GND	GND	GND	GND
	35	MDI10	MDI20	MDI10	MDI20	DMA100	DMA110	B240	B250
	34	MDO90	MDI00	MDO90	MDI00	DMA080	DMA090	B220	B230
	33	MDO70	MDO80	MDO70	MDO80	DMA060	DMA070	B200	B210
	32	MDO50	MDO60	MDO50	MDO60	DMA040	DMA050	B180	B190
	31	MDO30	MDO40	MDO30	MDO40	DMA020	DMA030	B160	B170
	30	MDO10	MDO20	MDO10	MDO20	GND	GND	GND	GND
	29	GND	MDO00	GND	MDO00	DMAR000	DMAR010	S300	S310
	28	TEMPA ⊗	VT	TEMPA ⊗	VT	DMX140	DMX150	S280	S290
	27	0WRTO		WRTO	TEMP B ⊗	DMX120	DMX130	S260	S270
	26	GND	GND	GND	GND	GND	GND	GND	GND
	25	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	S240	S250
	24	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	S220	S230
	23	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	S200	S210
	22	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	S180	S190
	21	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	S160	S170
	20	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	GND	GND
	19	GND	GND	GND	GND	GND	CRDY0	GND	CRDY0
	18					CMC020	CREQ0	CMC020	CREQ0
	17					CMC000	CMC010	CMC000	CMC010
	16	GND	GND	GND	GND	GND	GND	GND	GND
	15					CD300	CD310	CD300	CD310
	14					CD280	CD290	CD280	CD290
	13					CD260	CD270	CD260	CD270
	12					CD240	CD250	CD240	CD250
	11	GND	GND	GND	GND	GND	GND	GND	GND
	10	EWRTO	MS000	EWRTO	MS000	CD220	CD230	CD220	CD230
	09	MS010	MS020	MS010	MS020	CD200	CD210	CD200	CD210
	08	MS030	MS040	MS030	MS040	CD180	CD190	CD180	CD190
	07	MS050	MS060	MS050	MS060	CD160	CD170	CD160	CD170
	06	MS070	MS080	MS070	MS080	GND	GND	GND	GND
	05	MS090	MS100	MS090	MS100	M3820	M2820	B140	B150
	04	MS110	MS120	MS110	MS120	M1820	M0820	B120	B130
	03	MS130	MS140	MS130	MS140	LOAD0	RNS0	B100	B110
	02	MS150	MS160	MS150	MS160	SOT0	EOT0	B080	B090
	01	GND	GND	GND	GND	GND	XREQ0	GND	B070
	00	PS	PS	PS	GND	PS	PS	PS	PS
		1	2	1	2	1	2	1	2
0	41	PS	PS	PS	GND	PS	PS	PS	PS
	40	GND	GND	GND	GND	GND	MTPC0 ⊗	GND	B060
	39	LMBSYA0	LMBSYC0	LMBSYA0	LMBSYC0	LMEQ0 ⊗	BH0 ⊗	B040	B050
	38	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMDS0	B020	B030
	37	LMBSYB0	LMRS0	LMBSYB0	LMRS0	PRPC0 ⊗	LMRS0	B000	B010
	36	GND	GND	GND	GND	GND	GND	GND	GND
	35	DUA0	MBZ0	DUA0	MBZ0	CD140	CD150	CD140	CD150
	34	GND	GND	GND	GND	CD120	CD130	CD120	CD130
	33	MA130	MA140	MA130	MA140	CD100	CD110	CD100	CD110
	32	MA110	MA120	MA110	MA120	CD080	CD090	CD080	CD090
	31	MA090	MA100	MA090	MA100	GND	GND	GND	GND
	30	MA070	MA080	MA070	MA080	CD060	CD070	CD060	CD070
	29	MA050	MA060	MA050	MA060	CD040	CD050	CD040	CD050
	28	GND	GND	GND	GND	CD020	CD030	CD020	CD030
	27	SCLR0		SCLR0		CD000	CD010	CD000	CD010
	26	MCLR0	GND	MCLR0	GND	GND	GND	GND	GND
	25	GND	GND	GND	GND	SCLR0	GND	SCLR0	GND
	24	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	S140	S150
	23	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	S120	S130
	22	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	S100	S110
	21	GND	GND	GND	GND	GND	GND	GND	GND
	20	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130		
	19	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	S080	S090
	18	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	S060	S070
	17	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	S040	S050
	16	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	S020	S030
	15	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	S000	S010
	14	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010		
	13	GND	GND	GND	GND	GND	GND	GND	GND
	12	IRLMP0	DLMP0	IRLMP0	DLMP0	CA300	DLMP0	CA300	MAR310 ⊗
	11	GND	GND	GND	GND	CA280	CA290	CA280	CA290
	10	MA030	MA040	MA030	MA040	CA260	CA270	CA260	CA270
	09	MA020		MA020		CA240	CA250	CA240	CA250
	08	MAX060	MAX070	MAX060	MAX070	CA220	CA230	CA220	CA230
	07	MA010		MA010		CA200	CA210	CA200	CA210
	06	MA000	GND	MA000		GND	GND	GND	GND
	05	PAR0		PAR0		CA180	CA190	CA180	CA190
	04	INH0	ER0	INH0	ER0	CA160	CA170	CA160	CA170
	03		SPY		SPY	CA140	CA150	CA140	CA150
	02	PIS	NIS			CA120	CA130	CA120	CA130
	01	GND	GND	GND	GND	GND	DMFP0 ⊗	GND	GND
	00	PS	PS	PS	GND	PS	PS	PS	PS
		1	2	1	2	1	2	1	2

NOTES
1. BACKPANEL — 35-540
⊗ WIRE WRAP RUNS
2. SLOT ASSIGNMENTS SHOWN FOR THE BASIC 128 KB MEMORY SYSTEM.

THE LMI BOARDS ARE RE-ASSIGNED WHEN THE SYSTEM IS EXPANDED WITH CORRESPONDING CHANGES IN MA, MD, & MS STRAPPING OPTIONS.

NAME	TITLE	DATE
G. MELTON	DRAFT	6-10-74
G.J. HOMEFIELD	CHK.	10-10-74
T. EVEE	ENGR	
S MESSINA	DIR ENG	

TITLE 8/32 BACK PANEL UPPER

TASK NO. 03053 DWG NO. 01-078 F03D08 SHEET OF 2 - 4

PERKIN-ELMER

BACK PANEL MAP

CONN.	TITLE BD. LOC. TERM. NO.	LMM 07 ROW 1	LMM 07 ROW 2	LMM 06 ROW 1	LMM 06 ROW 2	LMM 05 ROW 1	LMM 05 ROW 2	LMM 04 ROW 1	LMM 04 ROW 2	CONN.
1	41	PS	GND							1
	40	GND	GND							
	39	PI5	PI5							
	38	NI5	NI5							
	37	MD150	MD160							
	36	MD130	MD140							
	35	MD110	MD120							
	34	MD090	MD100							
	33	MD070	MD080							
	32	MD050	MD060							
	31	MD030	MD040							
	30	MD010	MD020							
	29		MD000							
	28	TEMPA	VT							
	27	WRTO	TEMPB							
	26	GND	GND							
	25	LM8300	LM8310							
	24	LM8280	LM8290							
	23	LM8260	LM8270							
	22	LM8240	LM8250							
	21	LM8220	LM8230							
	20	LM8200	LM8210							1
	19	GND	GND							
	18									
	17									
	16	GND	GND							
	15									
	14									
	13									
	12									
	11	GND	GND							
	10		MS000							
	09	MS010	MS020							
	08	MS030	MS040							
	07	MS050	MS060							
	06	MS070	MS080							
	05	MS090	MS100							
	04	MS110	MS120							
	03	MS130	MS140							
	02	MS150	MS160							
	01	GND	GND							
	00	PS	GND							
		1	2	1	2	1	2	1	2	
0	41	PS	GND							0
	40	GND	GND							
	39									
	38	LMRDY0	LMD50							
	37	LMBSY0	LMB50							
	36	GND	GND							
	35	DUA0	MB20							
	34	GND	GND							
	33	MA130	MA140							
	32	MA110	MA120							
	31	MA090	MA100							
	30	MA070	MA080							
	29	MA050	MA060							
	28	GND	GND							
	27	SCLR0								
	26	MCLR0	GND							
	25	GND	GND							
	24	LMB180	LMB190							
	23	LMB160	LMB170							
	22	LMB140	LMB150							
	21	GND	GND							
	20	LMB120	LMB130							
	19	LMB100	LMB110							
	18	LMB080	LMB090							
	17	LMB060	LMB070							
	16	LMB040	LMB050							
	15	LMB020	LMB030							
	14	LMB000	LMB010							
	13	GND	GND							
	12		LMP0							
	11	GND	GND							
	10	MA030	MA040							
	09	MA020								
	08	MAX060	MAX070							
	07	MA010								
	06	MA000								
	05	PAR0								
	04	INH0	ER0							
	03									
	02	PI5	NI5							
	01	GND	GND							
	00	PS	GND							
		1	2	1	2	1	2	1	2	

CONN.	TITLE BD. LOC. TERM. NO.	LMM 03 ROW 1	LMM 03 ROW 2	LMM 02 ROW 1	LMM 02 ROW 2	LMM 01 ROW 1	LMM 01 ROW 2	LMM 00 ROW 1	LMM 00 ROW 2	CONN.
1	41							PS	GND	1
	40							GND	GND	
	39							PI5	PI5	
	38							NI5	NI5	
	37							MD150	MD160	
	36							MD130	MD140	
	35							MD110	MD120	
	34							MD090	MD100	
	33							MD070	MD080	
	32							MD050	MD060	
	31							MD030	MD040	
	30							MD010	MD020	
	29								MD000	
	28							TEMPA	VT	
	27							WRTO	TEMPB	
	26							GND	GND	
	25							LM8300	LM8310	
	24							LM8280	LM8290	
	23							LM8260	LM8270	
	22							LM8240	LM8250	
	21							LM8220	LM8230	
	20							LM8200	LM8210	1
	19							GND	GND	
	18									
	17									
	16							GND	GND	
	15									
	14									
	13									
	12									
	11							GND	GND	
	10								MS000	
	09							MS010	MS020	
	08							MS030	MS040	
	07							MS050	MS060	
	06							MS070	MS080	
	05							MS090	MS100	
	04							MS110	MS120	
	03							MS130	MS140	
	02							MS150	MS160	
	01							GND	GND	
	00							PS	GND	
		1	2	1	2	1	2	1	2	
0	41							PS	GND	0
	40							GND	GND	
	39									
	38							LMRDY0	LMD50	
	37							LMBSY0	LMB50	
	36							GND	GND	
	35							DUA0	MB20	
	34							GND	GND	
	33							MA130	MA140	
	32							MA110	MA120	
	31							MA090	MA100	
	30							MA070	MA080	
	29							MA050	MA060	
	28							GND	GND	
	27							SCLR0		
	26							MCLR0	GND	
	25							GND	GND	
	24							LMB180	LMB190	
	23							LMB160	LMB170	
	22							LMB140	LMB150	
	21							GND	GND	
	20							LMB120	LMB130	
	19							LMB100	LMB110	
	18							LMB080	LMB090	
	17							LMB060	LMB070	
	16							LMB040	LMB050	
	15							LMB020	LMB030	
	14							LMB000	LMB010	
	13							GND	GND	
	12								LMP0	
	11							GND	GND	
	10							MA030	MA040	
	09							MA020		
	08							MAX060	MAX070	
	07							MA010		
	06							MA000		
	05							PAR0		
	04							INH0	ER0	
	03									
	02							PI5	NI5	
	01							GND	GND	
	00							PS	GND	
		1	2	1	2	1	2	1	2	

NOTES
1. BACKPANEL - 35-542

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE 8/32 BACKPANEL MEMORY EXP.

TASK NO. 03053 DWG NO. 01-078 R03 008 SHEET OF 3 - 4

PERKIN-ELMER
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

ADDED: "MSIGO" ON SHT. 2 TO CPA, PIN 240-1.					
S/H	KT	03088 43		3-24-75	R01
ADDED: SHT. 1 "PREQO" MNEMONIC TO PIN 128-0 & 228-0 SLOTS 00 THRU 02. SHT. 2 "LMBSYAO" TO PIN 139-0 SLOTS 02 THRU 07. "LMBSYCO" TO PIN 239-0 SLOTS 02 THRU 07. CHANGED: PIN 187-0 SLOT 01 WAS "LMBSYO", PIN 187-0 SLOTS 02 THRU 07 WERE LMBSYO.					
S/H	KT	03088 49		3-24-75	R02
ADDED: SHEET 4.					
S/H	KT	03088 52		3-24-76	R03
CONN 2 ROW 1 PIN 08 STRTIA WAS SRTI. CONN 3 ROW 2 PIN 16 CSA040 WAS CSAD041. CONN 3 ROW 1 PIN 16 CSA050 WAS CSAD051. REVISED SHTS 1 & 4.					
KR		4231	R	3-4-80	R04
SHT 1, AREA J5, ADDED "MMEPFO" TO 104-1. REVISED SHTS 1 & 4.					
KR		5304	MS	2-14-83	R05

CONN 5

	2	1
16	UIR300	UIR310
15	UIR280	UIR290
14	UIR260	UIR270
13	UIR240	UIR250
12	YD300	YD310
11	YD280	YD290
10	YS300	YS310
09	YS280	YS290
08	SX300	SX310
07	SX280	SX290
06	GND	ININTO
05	GND	MAIO
04	GND	IREQO
03	GND	DREQO
02	GND	PSW210
01	GND	GND
00	GND	PASS1A

CONN 2

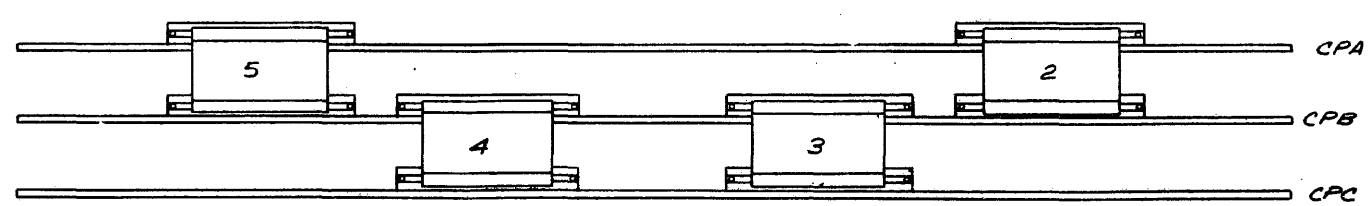
	2	1
16	MC020	MC030
15	MC000	MC010
14	GND	S2BO
13	GND	PCLKO
12	GND	JUTY1
11	GND	RX3DO
10	GND	SPARE
09	GND	CS000
08	GND	STRTIA
07	GND	GND
06	GND	GND
05	BSEL031	BSEL041
04	BSEL011	BSEL021
03	GND	BSEL001
02	SSEL031	SSEL041
01	SSEL011	SSEL021
00	GND	SSEL001

CONN 3

	2	1
24	GND	GND
23	CSAD141	GND
22	CSAD121	CSAD151
21	GND	CSAD131
20	CSAD101	CSAD111
19	CSAD081	GND
18	CSAD061	CSAD091
17	GND	CSAD071
16	CSA040	CSA050
15	GND	GND
14	GND	GND
13	GND	SPARE
12	GND	PCLKO
11	PSW251	SECLK1
10	PSW260	PSW270
09	GND	S2BO
08	ASEL031	ASEL041
07	ASEL011	ASEL021
06	GND	ASEL001
05	BSEL031	BSEL041
04	BSEL011	BSEL021
03	GND	BSEL001
02	SSEL031	SSEL041
01	SSEL011	SSEL021
00	GND	SSEL001

CONN 4

	2	1
24	CSD301	CSD311
23	CSD281	CSD291
22	GND	CSD271
21	CSD261	CSD251
20	CSD241	GND
19	CSD221	CSD231
18	GND	CSD211
17	CSD201	CSD191
16	CSD181	GND
15	CSD161	CSD171
14	GND	CSD151
13	CSD141	CSD131
12	CSD121	GND
11	CSD101	CSD111
10	GND	CSD091
09	CSD081	CSD071
08	CSD061	GND
07	CSD041	CSD051
06	GND	CSD031
05	CSD021	CSD011
04	CSD001	GND
03	GND	CSWPO
02	GND	INCLKO
01	GND	CLKO
00	GND	GND



SCALE–

NAME	TITLE	DATE
G. MELTON	DRAFT	2-14-75
	CHK	2-18-75
	ENGR	

TITLE: CPA/CPB, CPB/CPC FRONT END CABLING

03088

01-078 R05 D08 | 4-4

BACK PANEL MAP

CONN. 1

TERM. NO.	CPB AA07 Row 1	CPB AA07 Row 2	DCB AA06 Row 1	DCB AA06 Row 2	DFUB AA05 Row 1	DFUB AA05 Row 2	DFUA AA04 Row 1	DFUA AA04 Row 2	ALU AA03 Row 1	ALU AA03 Row 2	SPARE AA02 Row 1	SPARE AA02 Row 2	SPARE AA01 Row 1	SPARE AA01 Row 2	IOU AA00 Row 1	IOU AA00 Row 2
41	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5
40	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
39	DSPYL0	PPF0													P15	PPF0
38	ATN020	ATN030													N15	DSPYL0
37	ATN000	ATN010													RACK0	TACK0
36	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
35	B300	B310	B300	B310	B300	B310	B300	B310	B300	B310	B300	B310	B300	B310	B300	B310
34	B280	B290	B280	B290	B280	B290	B280	B290	B280	B290	B280	B290	B280	B290	B280	B290
33	B260	B270	B260	B270	B260	B270	B260	B270	B260	B270	B260	B270	B260	B270	B260	B270
32	B240	B250	B240	B250	B240	B250	B240	B250	B240	B250	B240	B250	B240	B250	B240	B250
31	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
30	B220	B230	B220	B230	B220	B230	B220	B230	B220	B230	B220	B230	B220	B230	B220	B230
29	B200	B210	B200	B210	B200	B210	B200	B210	B200	B210	B200	B210	B200	B210	B200	B210
28	B180	B190	B180	B190	B180	B190	B180	B190	B180	B190	B180	B190	B180	B190	B180	B190
27	B160	B170	B160	B170	B160	B170	B160	B170	B160	B170	B160	B170	B160	B170	B160	B170
26	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
25	S300	S310	S300	S310	S300	S310	S300	S310	S300	S310	S300	S310	S300	S310	S300	S310
24	S280	S290	S280	S290	S280	S290	S280	S290	S280	S290	S280	S290	S280	S290	S280	S290
23	S260	S270	S260	S270	S260	S270	S260	S270	S260	S270	S260	S270	S260	S270	S260	S270
22	S240	S250	S240	S250	S240	S250	S240	S250	S240	S250	S240	S250	S240	S250	S240	S250
21	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
20	S220	S230	S220	S230	S220	S230	S220	S230	S220	S230	S220	S230	S220	S230	S220	S230
19	S200	S210	S200	S210	S200	S210	S200	S210	S200	S210	S200	S210	S200	S210	S200	S210
18	S180	S190	S180	S190	S180	S190	S180	S190	S180	S190	S180	S190	S180	S190	S180	S190
17	S160	S170	S160	S170	S160	S170	S160	S170	S160	S170	S160	S170	S160	S170	S160	S170
16	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
15	A300	A310	A300	A310	A300	A310	A300	A310	A300	A310	A300	A310	A300	A310	A300	A310
14	A280	A290	A280	A290	A280	A290	A280	A290	A280	A290	A280	A290	A280	A290	A280	A290
13	A260	A270	A260	A270	A260	A270	A260	A270	A260	A270	A260	A270	A260	A270	A260	A270
12	A240	A250	A240	A250	A240	A250	A240	A250	A240	A250	A240	A250	A240	A250	A240	A250
11	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
10	A220	A230	A220	A230	A220	A230	A220	A230	A220	A230	A220	A230	A220	A230	A220	A230
09	A200	A210	A200	A210	A200	A210	A200	A210	A200	A210	A200	A210	A200	A210	A200	A210
08	A180	A190	A180	A190	A180	A190	A180	A190	A180	A190	A180	A190	A180	A190	A180	A190
07	A160	A170	A160	A170	A160	A170	A160	A170	A160	A170	A160	A170	A160	A170	A160	A170
06	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
05	MMF0	PSW230													MMF0	DMPF0
04															MMEPF0	FWINT0
03	MSEL020	RWC0	MSEL020	RWC0	MSEL020	RWC0	MSEL020	RWC0	MSEL020	RWC0	MSEL020	RWC0	MSEL020	RWC0	MSEL020	RWC0
02	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010
01	GND	MSIG0	GND	MSIG0	GND	MSIG0	GND	MSIG0	GND	MSIG0	GND	MSIG0	GND	MSIG0	GND	MSIG0
00	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5

CONN. 0

TERM. NO.	CPB Row 1	CPB Row 2	DCB Row 1	DCB Row 2	DFUB Row 1	DFUB Row 2	DFUA Row 1	DFUA Row 2	ALU Row 1	ALU Row 2	SPARE AA02 Row 1	SPARE AA02 Row 2	SPARE AA01 Row 1	SPARE AA01 Row 2	IOU Row 1	IOU Row 2
41	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5
40	GND	KSIG0	GND	KSIG0	GND	KSIG0	GND	KSIG0	GND	KSIG0	GND	KSIG0	GND	KSIG0	GND	KSIG0
39	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030
38	FSEL000	FSEL010	FSEL000	FSES010	FSEL000	FSEL010	FSEL000	FSEL010	FSEL000	FSEL010	FSEL000	FSEL010	FSEL000	FSEL010	FSEL000	FSEL010
37	STRT0	MFIN0	STRT0	MFIN0	STRT0	MFIN0	STRT0	MFIN0	STRT0	MFIN0	STRT0	MFIN0	STRT0	MFIN0	STRT0	MFIN0
36	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
35	B140	B150	B140	B150	B140	B150	B140	B150	B140	B150	B140	B150	B140	B150		RACK0
34	B120	B130	B120	B130	B120	B130	B120	B130	B120	B130	B120	B130	B120	B130	GND	GND
33	B100	B110	B100	B110	B100	B110	B100	B110	B100	B110	B100	B110	B100	B110		LMRQ0
32	B080	B090	B080	B090	B080	B090	B080	B090	B080	B090	B080	B090	B080	B090	MAR310	ATN0
31	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
30	B060	B070	B060	B070	B060	B070	B060	B070	B060	B070	B060	B070	B060	B070	ACK030	MTPC0
29	B040	B050	B040	B050	B040	B050	B040	B050	B040	B050	B040	B050	B040	B050	ACK020	PRPC0
28	B020	B030	B020	B030	B020	B030	B020	B030	B020	B030	B020	B030	B020	B030	ACK010	GND
27	B000	B010	B000	B010	B000	B010	B000	B010	B000	B010	B000	B010	B000	B010	ACK000	HW0
26	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
25	S140	S150	S140	S150	S140	S150	S140	S150	S140	S150	S140	S150	S140	S150	GND	GND
24	S120	S130	S120	S130	S120	S130	S120	S130	S120	S130	S120	S130	S120	S130		
23	S100	S110	S100	S110	S100	S110	S100	S110	S100	S110	S100	S110	S100	S110	SYN0	BH0
22	S080	S090	S080	S090	S080	S090	S080	S090	S080	S090	S080	S090	S080	S090	CL070	DA0
21	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
20	S060	S070	S060	S070	S060	S070	S060	S070	S060	S070	S060	S070	S060	S070	DE0	CMD0
19	S040	S050	S040	S050	S040	S050	S040	S050	S040	S050	S040	S050	S040	S050	SR0	ADRS0
18	S020	S030	S020	S030	S020	S030	S020	S030	S020	S030	S020	S030	S020	S030	D140	D150
17	S000	S010	S000	S010	S000	S010	S000	S010	S000	S010	S000	S010	S000	S010	D120	D130
16	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
15	A140	A150	A140	A150	A140	A150	A140	A150	A140	A150	A140	A150	A140	A150	D100	D110
14	A120	A130	A120	A130	A120	A130	A120	A130	A120	A130	A120	A130	A120	A130	D080	D090
13	A100	A110	A100	A110	A100	A110	A100	A110	A100	A110	A100	A110	A100	A110	D060	D070
12	A080	A090	A080	A090	A080	A090	A080	A090	A080	A090	A080	A090	A080	A090	D040	D050
11	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
10	A060	A070	A060	A070	A060	A070	A060	A070	A060	A070	A060	A070	A060	A070	D020	D030
09	A040	A050	A040	A050	A040	A050	A040	A050	A040	A050	A040	A050	A040	A050	D000	D010
08	A020	A030	A020	A030	A020	A030	A020	A030	A020	A030	A020	A030	A020	A030		
07	A000	A010	A000	A010	A000	A010	A000	A010	A000	A010	A000	A010	A000	A010		
06	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
05	SCLR0	CCC0	SCLR0	CCC0	SCLR0	CCC0	SCLR0	CCC0	SCLR0	CCC0	SCLR0	CCC0	SCLR0	CCC0	SCLR0	CCC0
04	SCC0	VCC0	SCC0	VCC0	SCC0	VCC0	SCC0	VCC0	SCC0	VCC0	SCC0	VCC0	SCC0	VCC0	SCC0	VCC0
03	SCLR1	GCC0	SCLR1	GCC0	SCLR1	GCC0	SCLR1	GCC0	SCLR1	GCC0	SCLR1	GCC0	SCLR1	GCC0	SCLR1	GCC0
02	TKILL0	LCC0		LCC0		LCC0		LCC0		LCC0		LCC0		LCC0		LCC0
01	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
00	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5

REVISIONS (CONT.)

REVISED SHTS 1 & 4. KR 4231 R 3-6-80 R03

ADDED "MMEPF0" TO IOU 104-1. REVISED SHT 1. KR 5304 MS 2-14-83 R04

AREA R5 TERM NO. 05 & 04 DMP0 WAS IRLMP0, FWINT0 WAS DMPF0 REVISED SHT 2 ALSO. GP 3537 3-16-78 R02

NOTES
1. BACKPANEL - 35-592.

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED THE REVISION LEVEL OF THE DOCUMENT

RELEASED FOR PRODUCTION ENG. DATE 2/4/76

SHEET INDEX				
REV. LEV.	4	1	-	2
SHT. NO.	1	2	3	4

PRE PRODUCTION APPROVAL — DEV, INIT, DATE 2/5/76

REVISED SHTS 1 & 4. AREA B1: DSPYL0 WAS DSPLY1. DELETED ALL REF TO WIRE WRAP RUNS. 4-6-76 R01

TITLE	NAME	DATE
DRAFT	B. GRAY	2-19-75
CHK	R. CERO	2-19-75
ENGR	G. WELLY	4-12-76
	R. BARKER	4-12-76
DIR ENG	S. MESSINA	4-12-76

TITLE (LOWER BACKPANEL) MODEL 8/32 C (W/DFU BACKPANEL)

TASK NO. 03150 — DWG NO. 01-098R04D08 — SHEET 1 OF 4

BACK PANEL MAP

Connector 1, board locations A07–A04

TERM. NO.	LMM A07 Row 1	LMM A07 Row 2	LMI (NOTE 2) A06 Row 1	LMI (NOTE 2) A06 Row 2	LMM A05 Row 1	LMM A05 Row 2	LMM A04 Row 1	LMM A04 Row 2
41	PS	GND	PS	PS	PS	GND	PS	GND
40	GND	GND	GND	GND	GND	GND	GND	GND
39	P15	P15			P15	P15	P15	P15
38	N15	N15			N15	N15	N15	N15
37	MD150	MD160	MD150	MD160	MD150	MD160	MD150	MD160
36	MD130	MD140	MD130	MD140	MD130	MD140	MD130	MD140
35	MD110	MD120	MD110	MD120	MD110	MD120	MD110	MD120
34	MD090	MD100	MD090	MD100	MD090	MD100	MD090	MD100
33	MD070	MD080	MD070	MD080	MD070	MD080	MD070	MD080
32	MD050	MD060	MD050	MD060	MD050	MD060	MD050	MD060
31	MD030	MD040	MD030	MD040	MD030	MD040	MD030	MD040
30	MD010	MD020	MD010	MD020	MD010	MD020	MD010	MD020
29	GND	MD000	GND	MD000	GND	MD000	GND	MD000
28	TEMPA ⊛	VT ⊛			TEMPA ⊛	VT ⊛	TEMPA ⊛	VT ⊛
27	WRTO	TEMP B ⊛	OWRTO		WRTO	TEMP B ⊛	WRTO	TEMP B ⊛
26	GND	GND	GND	GND	GND	GND	GND	GND
25	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310
24	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290
23	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270
22	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250
21	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230
20	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210
19	GND	GND	GND	GND	GND	GND	GND	GND
18								
17								
16	GND	GND	GND	GND	GND	GND	GND	GND
15								
14								
13								
12								
11	GND	GND	GND	GND	GND	GND	GND	GND
10		MS000	EWRTO	MS000	EWRTO	MS000		MS000
09	MS010	MS020	MS010	MS020	MS010	MS020	MS010	MS020
08	MS030	MS040	MS030	MS040	MS030	MS040	MS030	MS040
07	MS050	MS060	MS050	MS060	MS050	MS060	MS050	MS060
06	MS070	MS080	MS070	MS080	MS070	MS080	MS070	MS080
05	MS090	MS100	MS090	MS100	MS090	MS100	MS090	MS100
04	MS110	MS120	MS110	MS120	MS110	MS120	MS110	MS120
03	MS130	MS140	MS130	MS140	MS130	MS140	MS130	MS140
02	MS150	MS160	MS150	MS160	MS150	MS160	MS150	MS160
01	GND	GND	GND	GND	GND	GND	GND	GND
00	PS	GND	PS	PS	PS	GND	PS	GND

Connector 1, board locations A03–A00

TERM. NO.	LMI (NOTE 2) A03 Row 1	LMI (NOTE 2) A03 Row 2	LMM A02 Row 1	LMM A02 Row 2	MBC A01 Row 1	MBC A01 Row 2	CPA A00 Row 1	CPA A00 Row 2
41	PS	PS	PS	GND	PS	PS	PS	PS
40	GND	GND	GND	GND	GND	QUEO	GND	MSIGO
39					DMA160	DMA170	B300	B310
38					DMA140	DMA150	B280	B290
37	MD150	MD160	MD150	MD160	DMA120	DMA130	B260	B270
36	MD130	MD140	MD130	MD140	GND	GND	GND	GND
35	MD110	MD120	MD110	MD120	DMA100	DMA110	B240	B250
34	MD090	MD100	MD090	MD100	DMA080	DMA090	B220	B230
33	MD070	MD080	MD070	MD080	DMA060	DMA070	B200	B210
32	MD050	MD060	MD050	MD060	DMA040	DMA050	B180	B190
31	MD030	MD040	MD030	MD040	DMA020	DMA030	B160	B170
30	MD010	MD020	MD010	MD020	GND	GND	GND	GND
29	GND	MD000	GND	MD000	DMA000	DMA010	S300	S310
28			TEMPA ⊛	VT ⊛	DMX140	DMX150	S280	S290
27	OWRTO		WRTO	TEMP B ⊛	DMX120	DMX130	S260	S270
26	GND	GND	GND	GND	GND	GND	GND	GND
25	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	S240	S250
24	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	S220	S230
23	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	S200	S210
22	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	S180	S190
21	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	S160	S170
20	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	GND	GND
19	GND	GND	GND	GND	GND	CRDYO	GND	CRDYO
18					CMC020	CREQO	CMC020	CREQO
17					CMC000	CMC010	CMC000	CMC010
16	GND	GND	GND	GND	GND	GND	GND	GND
15					CD300	CD310	CD300	CD310
14					CD280	CD290	CD280	CD290
13					CD260	CD270	CD260	CD270
12					CD240	CD250	CD240	CD250
11	GND	GND	GND	GND	GND	GND	GND	GND
10	EWRTO	MS000	EWRTO	MS000	CD220	CD230	CD220	CD230
09	MS010	MS020	MS010	MS020	CD200	CD210	CD200	CD210
08	MS030	MS040	MS030	MS040	CD180	CD190	CD180	CD190
07	MS050	MS060	MS050	MS060	CD160	CD170	CD160	CD170
06	MS070	MS080	MS070	MS080	GND	GND	GND	GND
05	MS090	MS100	MS090	MS100	M3B20	M2B20	B140	B150
04	MS110	MS120	MS110	MS120	M1B20	M0B20	B120	B130
03	MS130	MS140	MS130	MS140	LOADO	ANSO	B100	B110
02	MS150	MS160	MS150	MS160	SOTO	EOTO	B080	B090
01	GND	GND	GND	GND	GND	XREQO	GND	B070
00	PS	PS	PS	GND	PS	PS	PS	PS

Connector 0, board locations A07–A04

TERM. NO.	A07 Row 1	A07 Row 2	A06 Row 1	A06 Row 2	A05 Row 1	A05 Row 2	A04 Row 1	A04 Row 2
41	PS	GND	PS	PS	PS	GND	PS	GND
40	GND	GND	GND	GND	GND	GND	GND	GND
39	LMBSYAO	LMBSYCO	LMBSYAO	LMBSYCO	LMBSYAO	LMBSYCO	LMBSYAO	LMBSYCO
38	LMRDYO	LMDSO	LMRDYO	LMDSO	LMRDYO	LMDSO	LMRDYO	LMDSO
37	LMBSYBO	LMRSO	LMBSYBO	LMRSO	LMBSYBO	LMRSO	LMBSYBO	LMRSO
36	GND	GND	GND	GND	GND	GND	GND	GND
35	DUAO	MB2O	DUAO	MB2O	DUAO	MB2O	DUAO	MB2O
34	GND	GND	GND	GND	GND	GND	GND	GND
33	MA130	MA140	MA130	MA140	MA130	MA140	MA130	MA140
32	MA110	MA120	MA110	MA120	MA110	MA120	MA110	MA120
31	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100
30	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080
29	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060
28	GND	GND	GND	GND	GND	GND	GND	GND
27	SCLRO		SCLRO		SCLRO		SCLRO	
26	MCLRO	GND	MCLRO	GND	MCLRO	GND	MCLRO	GND
25	GND	GND	GND	GND	GND	GND	GND	GND
24	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190
23	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170
22	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150
21	GND	GND	GND	GND	GND	GND	GND	GND
20	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130
19	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110
18	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090
17	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070
16	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050
15	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030
14	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010
13	GND	GND	GND	GND	GND	GND	GND	GND
12	IRLMPO	DLMPO	IRLMPO	DLMPO	IRLMPO	DLMPO	IRLMPO	DLMPO
11	GND	GND	GND	GND	GND	GND	GND	GND
10	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040
09	MA020		MA020		MA020		MA020	
08	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070
07	MA010		MA010		MA010		MA010	
06	MA000		MA000	GND	MA000		MA000	
05	PARO		PARO		PARO		PARO	
04	INHO	ERO	INHO	ERO	INHO	ERO	INHO	ERO
03		SPY		SPY		SPY		SPY
02	P15	N15					P15	N15
01	GND	GND	GND	GND	GND	GND	GND	GND
00	PS	GND	PS	PS	PS	GND	PS	GND

Connector 0, board locations A03–A00

TERM. NO.	A03 Row 1	A03 Row 2	A02 Row 1	A02 Row 2	A01 Row 1	A01 Row 2	A00 Row 1	A00 Row 2
41	PS	PS	PS	GND	PS	PS	PS	PS
40	GND	GND	GND	GND	GND	MTPCO ⊛	GND	B060
39	LMBSYAO	LMBSYCO	LMBSYAO	LMBSYCO	LMRQO ⊛	BHO ⊛	B040	B050
38	LMRDYO	LMDSO	LMRDYO	LMDSO	LMRDYO	LMDSO	B020	B030
37	LMBSYBO	LMRSO	LMBSYBO	LMRSO	PRPCO ⊛	LMRSO	B000	B010
36	GND	GND	GND	GND	GND	GND	GND	GND
35	DUAO	MB2O	DUAO	MB2O	CD140	CD150	CD140	CD150
34	GND	GND	GND	GND	CD120	CD130	CD120	CD130
33	MA130	MA140	MA130	MA140	CD100	CD110	CD100	CD110
32	MA110	MA120	MA110	MA120	CD080	CD090	CD080	CD090
31	MA090	MA100	MA090	MA100	GND	GND	GND	GND
30	MA070	MA080	MA070	MA080	CD060	CD070	CD060	CD070
29	MA050	MA060	MA050	MA060	CD040	CD050	CD040	CD050
28	GND	GND	GND	GND	CD020	CD030	CD020	CD030
27	SCLRO		SCLRO		CD000	CD010	CD000	CD010
26	MCLRO	GND	MCLRO	GND	GND	GND	GND	GND
25	GND	GND	GND	GND	SCLRO	GND	SCLRO	GND
24	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	S140	S150
23	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	S120	S130
22	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	S100	S110
21	GND	GND	GND	GND	GND	GND	GND	GND
20	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	FWINTO	
19	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	S080	S090
18	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	S060	S070
17	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	S040	S050
16	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	S020	S030
15	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	S000	S010
14	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010		
13	GND	GND	GND	GND	GND	GND	GND	GND
12	IRLMPO	DLMPO	IRLMPO	DLMPO	CA300	DLMPO	CA300	MAR310 ⊛
11	GND	GND	GND	GND	CA280	CA290	CA280	CA290
10	MA030	MA040	MA030	MA040	CA260	CA270	CA260	CA270
09	MA020		MA020		CA240	CA250	CA240	CA250
08	MAX060	MAX070	MAX060	MAX070	CA220	CA230	CA220	CA230
07	MA010		MA010		CA200	CA210	CA200	CA210
06	MA000	GND	MA000		GND	GND	GND	GND
05	PARO		PARO		CA180	CA190	CA180	CA190
04	INHO	ERO	INHO	ERO	CA160	CA170	CA160	CA170
03		SPY		SPY	CA140	CA150	CA140	CA150
02	P15	N15			CA120	CA130	CA120	CA130
01	GND	GND	GND	GND	GND	DMFPO ⊛	GND	GND
00	PS	PS	PS	GND	PS	PS	PS	PS

NOTES
1. BACKPANEL – 35-540
⊛ WIRE WRAP RUNS
2. SLOT ASSIGNMENTS SHOWN FOR THE BASIC 128 KB MEMORY SYSTEM

THE LMI BOARDS ARE RE-ASSIGNED WHEN THE SYSTEM IS EXPANDED WITH CORRESPONDING CHANGES IN MA, MD, & MS STRAPPING OPTIONS

REVISIONS
AREA N7-TERM NO 20 FWINTO WAS ADDED
GP 41 | 3537 | 3-16-78 | R01

NAME | TITLE | DATE
DRAFT
CHK
ENGR
DIR ENG

TITLE (UPPER BACKPANEL) MODEL 8/32 C (W/DFU BACKPANEL)
TASK NO. 03150
DWG NO. 01-098R01D08
SHEET 2 OF 4

PERKIN-ELMER

BACK PANEL MAP

CONN.	TITLE BD. LOC. TERM. NO.	LMM 07 ROW 1	LMM 07 ROW 2	LMM 06 ROW 1	LMM 06 ROW 2	LMM 05 ROW 1	LMM 05 ROW 2	LMM 04 ROW 1	LMM 04 ROW 2	CONN.	TITLE BD. LOC. TERM. NO.	LMM 03 ROW 1	LMM 03 ROW 2	LMM 02 ROW 1	LMM 02 ROW 2	LMM 01 ROW 1	LMM 01 ROW 2	LMM 00 ROW 1	LMM 00 ROW 2	TITLE BD. LOC. TERM NO.	CONN.
	41	PS	GND	PS	GND	PS	GND	PS	GND		41	PS	GND	PS	GND	PS	GND	PS	GND	41	
	40	GND	GND	GND	GND	GND	GND	GND	GND		40	GND	GND	GND	GND	GND	GND	GND	GND	40	
	39	P1S	P1S	P1S	P1S	P1S	P1S	P1S	P1S		39	P1S	P1S	P1S	P1S	P1S	P1S	P1S	P1S	39	
	38	N1S	N1S	N1S	N1S	N1S	N1S	N1S	N1S		38	N1S	N1S	N1S	N1S	N1S	N1S	N1S	N1S	38	
	37	MDI50	MDI60	MDI50	MDI60	MDI50	MDI60	MDI50	MDI60		37	MDI50	MDI60	MDI50	MDI60	MDI50	MDI60	MDI50	MDI60	37	
	36	MDI30	MDI40	MDI30	MDI40	MDI30	MDI40	MDI30	MDI40		36	MDI30	MDI40	MDI30	MDI40	MDI30	MDI40	MDI30	MDI40	36	
	35	MDI10	MDI20	MDI10	MDI20	MDI10	MDI20	MDI10	MDI20		35	MDI10	MDI20	MDI10	MDI20	MDI10	MDI20	MDI10	MDI20	35	
	34	MDO90	MDI00	MDO90	MDI00	MDO90	MDI00	MDO90	MDI00		34	MDO90	MDI00	MDO90	MDI00	MDO90	MDI00	MDO90	MDI00	34	
2	33	MDO70	MDO80	MDO70	MDO80	MDO70	MDO80	MDO70	MDO80		33	MDO70	MDO80	MDO70	MDO80	MDO70	MDO80	MDO70	MDO80	33	
	32	MDO50	MDO60	MDO50	MDO60	MDO50	MDO60	MDO50	MDO60		32	MDO50	MDO60	MDO50	MDO60	MDO50	MDO60	MDO50	MDO60	32	
	31	MDO30	MDO40	MDO30	MDO40	MDO30	MDO40	MDO30	MDO40		31	MDO30	MDO40	MDO30	MDO40	MDO30	MDO40	MDO30	MDO40	31	
	30	MDO10	MDO20	MDO10	MDO20	MDO10	MDO20	MDO10	MDO20		30	MDO10	MDO20	MDO10	MDO20	MDO10	MDO20	MDO10	MDO20	30	
	29		MDOOO		MDOOO		MDOOO		MDOOO		29		MDOOO		MDOOO		MDOOO		MDOOO	29	
	28	TEMPA	VT	TEMPA	VT	TEMPA	VT	TEMPA	VT		28	TEMPA	VT	TEMPA	VT	TEMPA	VT	TEMPA	VT	28	
	27	WRTO	TEMP B	WRTO	TEMP B	WRTO	TEMP B	WRTO	TEMP B		27	WRTO	TEMP B	WRTO	TEMP B	WRTO	TEMP B	WRTO	TEMP B	27	
	26	GND	GND	GND	GND	GND	GND	GND	GND		26	GND	GND	GND	GND	GND	GND	GND	GND	26	
	25	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310		25	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	25	
	24	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290		24	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	24	
	23	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270		23	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	23	
	22	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250		22	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	22	
1	21	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230		21	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	21	
	20	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	1	20	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	20	1
	19	GND	GND	GND	GND	GND	GND	GND	GND		19	GND	GND	GND	GND	GND	GND	GND	GND	19	
	18										18									18	
	17										17									17	
	16	GND	GND	GND	GND	GND	GND	GND	GND		16	GND	GND	GND	GND	GND	GND	GND	GND	16	
	15										15									15	
	14										14									14	
	13										13									13	
4	12										12									12	
	11	GND	GND	GND	GND	GND	GND	GND	GND		11	GND	GND	GND	GND	GND	GND	GND	GND	11	
	10		M5000		M5000		M3000		M8000		10		M5000		M5000		M5000		M5000	10	
	09	M3010	M3020	M5010	M5020	M3010	M8020	M3010	M8020		09	M3010	M3020	M5010	M3020	M3010	M3020	M3010	M8020	09	
	08	M3030	M5040	M5030	M5040	M3030	M3040	M3030	M5040		08	M3030	M5040	M5030	M5040	M3030	M5040	M3030	M3040	08	
	07	M3050	M5060	M3050	M5060	M3050	M5060	M3050	M8060		07	M3050	M5060	M3050	M5060	M3050	M5060	M3050	M5060	07	
	06	M3070	M5080	M3070	M5080	M3070	M3080	M3070	M8080		06	M3070	M5080	M3070	M5080	M3070	M3080	M5070	M5080	06	
	05	M3090	M5100	M3090	M5100	M3090	M5100	M3090	M8100		05	M3090	M5100	M3090	M5100	M3090	M5100	M3090	M8100	05	
	04	M3110	M3120	M3110	M3120	M3110	M3120	M3110	M3120		04	M3110	M3120	M3110	M3120	M3110	M3120	M3110	M3120	04	
	03	M3130	M3140	M3130	M3140	M3130	M3140	M3130	M3140		03	M3130	M3140	M3130	M3140	M3130	M3140	M3130	M3140	03	
	02	M3150	M3160	M3150	M3160	M3150	M3160	M3150	M3160		02	M3150	M3160	M3150	M3160	M3150	M3160	M3150	M3160	02	
	01	GND	GND	GND	GND	GND	GND	GND	GND		01	GND	GND	GND	GND	GND	GND	GND	GND	01	
	00	PS	GND	PS	GND	PS	GND	PS	GND		00	PS	GND	PS	GND	PS	GND	PS	GND	00	
		1	2	1	2	1	2	1	2			1	2	1	2	1	2	1	2		
	41	PS	GND	PS	GND	PS	GND	PS	GND		41	PS	GND	PS	GND	PS	GND	PS	GND	41	
	40	GND	GND	GND	GND	GND	GND	GND	GND		40	GND	GND	GND	GND	GND	GND	GND	GND	40	
	39										39									39	
	38	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMDS0		38	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMDS0	38	
	37	LMBSY0	LMBS0	LMBSY0	LMBS0	LMBSY0	LMBS0	LMBSY0	LMBS0		37	LMBSY0	LMBS0	LMBSY0	LMBS0	LMBSY0	LMBS0	LMBSY0	LMBS0	37	
	36	GND	GND	GND	GND	GND	GND	GND	GND		36	GND	GND	GND	GND	GND	GND	GND	GND	36	
	35	DUA0	MB20	DUA0	MB20	DUA0	MB20	DUA0	MB20		35	DUA0	MB20	DUA0	MB20	DUA0	MB20	DUA0	MB20	35	
	34	GND	GND	GND	GND	GND	GND	GND	GND		34	GND	GND	GND	GND	GND	GND	GND	GND	34	
	33	MA130	MA140	MA130	MA140	MA130	MA140	MA130	MA140		33	MA130	MA140	MA130	MA140	MA130	MA140	MA130	MA140	33	
	32	MA110	MA120	MA110	MA120	MA110	MA120	MA110	MA120		32	MA110	MA120	MA110	MA120	MA110	MA120	MA110	MA120	32	
	31	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100		31	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100	31	
	30	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080		30	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080	30	
	29	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060		29	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060	29	
	28	GND	GND	GND	GND	GND	GND	GND	GND		28	GND	GND	GND	GND	GND	GND	GND	GND	28	
	27	SCLR0		SCLR0		SCLR0		SCLR0			27	SCLR0		SCLR0		SCLR0		SCLR0		27	
	26	MCLR0	GND	MCLR0	GND	MCLR0	GND	MCLR0	GND		26	MCLR0	GND	MCLR0	GND	MCLR0	GND	MCLR0	GND	26	
	25	GND	GND	GND	GND	GND	GND	GND	GND		25	GND	GND	GND	GND	GND	GND	GND	GND	25	
	24	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190		24	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	24	
7	23	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170		23	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	23	
	22	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150		22	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	22	
	21	GND	GND	GND	GND	GND	GND	GND	GND		21	GND	GND	GND	GND	GND	GND	GND	GND	21	
0	20	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	0	20	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	20	0
	19	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110		19	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	19	
	18	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090		18	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	18	
	17	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070		17	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	17	
	16	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050		16	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	16	
	15	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030		15	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	15	
	14	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010		14	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010	14	
8	13	GND	GND	GND	GND	GND	GND	GND	GND		13	GND	GND	GND	GND	GND	GND	GND	GND	13	8
	12		LMP0		LMP0		LMP0		LMP0		12		LMP0		LMP0		LMP0		LMP0	12	
	11	GND	GND	GND	GND	GND	GND	GND	GND		11	GND	GND	GND	GND	GND	GND	GND	GND	11	
	10	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040		10	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040	10	
	09	MA020		MA020		MA020		MA020			09	MA020		MA020		MA020		MA020		09	
	08	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070		08	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070	08	
	07	MA010		MA010		MA010		MA010			07	MA010		MA010		MA010		MA010		07	
	06	MA000		MA000		MA000		MA000			06	MA000		MA000		MA000		MA000		06	
	05	PAR0		PAR0		PAR0		PAR0			05	PAR0		PAR0		PAR0		PAR0		05	
	04	INH0	ER0	INH0	ER0	INH0	ER0	INH0	ER0		04	INH0	ER0	INH0	ER0	INH0	ER0	INH0	ER0	04	
	03										03									03	
9	02	P1S	N1S	P1S	N1S	P1S	N1S	P1S	N1S		02	P1S	N1S	P1S	N1S	P1S	N1S	P1S	N1S	02	9
	01	GND	GND	GND	GND	GND	GND	GND	GND		01	GND	GND	GND	GND	GND	GND	GND	GND	01	
	00	PS	GND	PS	GND	PS	GND	PS	GND		00	PS	GND	PS	GND	PS	GND	PS	GND	00	
		1	2	1	2	1	2	1	2			1	2	1	2	1	2	1	2		

NOTES
1. BACKPANEL - 35-542

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE (MEMORY EXP) MODEL 8/32 C (W/DFU BACKPANEL)

TASK NO. 03150 SHEET OF 3 - 4

ENG NO. 01-098 D08

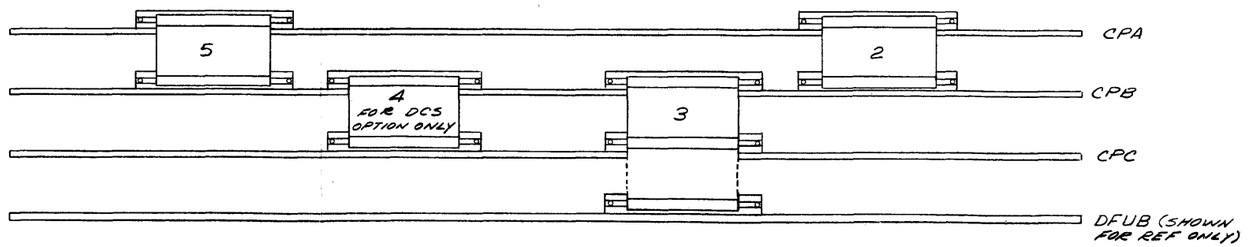
REVISIONS				
ON CABLE NUMBERED 4: ADDED "FOR DCS OPTION ONLY"; ON CABLE NUMBERED 3: DOTTED SECTION WAS SOLID. AREA E3: ADDED "(SHOWN FOR REF ONLY)."				
BC	03150		4-7-76	R01
EXTENSIVE CHANGES FOR R01 SEE MICRO-FILM COPY.				
KR	4231	R	3-6-80	R02

CONN 5		
	2	1
16	UIR300	UIR310
15	UIR280	UIR290
14	UIR260	UIR270
13	UIR240	UIR250
12	YD300	YD310
11	YD280	YD290
10	YS300	YS310
09	YS280	YS290
08	SX300	SX310
07	SX280	SX290
06	GND	ININTO
05	GND	MAIO
04	GND	IREQO
03	GND	DREQO
02	GND	PSW210
01	GND	GND
00	GND	PASSIA

CONN 2		
	2	1
16	MC020	MC030
15	MC000	MC010
14	GND	S2BO
13	GND	PCLKO
12	GND	JUTY1
11	GND	RX3DO
10	GND	SPARE
09	GND	CS000
08	GND	SRT1
07	GND	GND
06	GND	GND
05	BSEL031	BSEL041
04	BSEL011	BSEL021
03	GND	BSEL001
02	SSEL031	SSEL041
01	SSEL011	SSEL021
00	GND	SSEL001

CONN 3		
	2	1
24	GND	GND
23	CSA140A	GND
22	CSA120A	CSA150A
21	GND	CSA130A
20	CSA100A	CSA110A
19	CSA080A	GND
18	CSA060A	CSA090A
17	GND	CSA070A
16	CSA040A	CSA050A
15	GND	GND
14	GND	GND
13	GND	SPARE
12	GND	PCLKO
11	PSW251	SECLK1
10	PSW261	PSW271
09	GND	S2BO
08	ASEL031	ASEL041
07	ASEL011	ASEL021
06	GND	ASEL001
05	BSEL031	BSEL041
04	BSEL011	BSEL021
03	GND	BSEL001
02	SSEL031	SSEL041
01	SSEL011	SSEL021
00	GND	SSEL001

CONN 4		
	2	1
24	CSD301	CSD311
23	CSD281	CSD291
22	GND	CSD271
21	CSD261	CSD251
20	CSD241	GND
19	CSD221	CSD231
18	GND	CSD211
17	CSD201	CSD191
16	CSD181	GND
15	CSD161	CSD171
14	GND	CSD151
13	CSD141	CSD131
12	CSD121	GND
11	CSD101	CSD111
10	GND	CSD091
09	CSD081	CSD071
08	CSD061	GND
07	CSD041	CSD051
06	GND	CSD031
05	CSD021	CSD011
04	CSD001	GND
03	GND	CSWPO
02	GND	INCLKO
01	GND	CLKO
00	GND	GND



SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE
CPA/CPB, CPB/CPC/DFUB
FRONT END CABLING

TASK NO. 03150
DWG NO. 01-098E02D03
SHEET OF 4—4

BRUNING 44-231 2453B

BACK PANEL MAP

CONN.	TITLE	CPB	DCS	DFUB	DFUA	CONN.	TITLE	ALU	SPARE	SPARE	IOU	TITLE	CONN.
	BD. LOC	AA07	AA06	AA05	AA04		BD. LOC.	AA03	AA02	AA01	AA00	BD. LOC.	
	TERM.	ROW	ROW	ROW	ROW		TERM.	ROW	ROW	ROW	ROW	TERM	
	NO.	1 2	1 2	1 2	1 2		NO.	1 2	1 2	1 2	1 2	NO.	
	41	P5 P5	P5 P5	P5 P5	P5 P5		41	P5 P5	P5 P5	P5 P5	P5 P5	41	
	40	GND GND	GND GND	GND GND	GND GND		40	GND GND	GND GND	GND GND	GND GND	40	
	39	DSPYLO PPFO					39				PIS PPFO	39	
	38	ATNO20 ATNO30					38				NIS DSPYLO	38	
	37	ATNOOO ATNO10					37				RACKO TACKO	37	
	36	GND GND					36				GND GND	36	
	35	B300 B310					35				B300 B310	35	
	34	B280 B290					34				B280 B290	34	
2	33	B260 B270					33				B260 B270	33	2
	32	B240 B250					32				B240 B250	32	
	31	GND GND					31				GND GND	31	
	30	B220 B230					30				B220 B230	30	
	29	B200 B210					29				B200 B210	29	
	28	B180 B190					28				B180 B190	28	
	27	B160 B170					27				B160 B170	27	
	26	GND GND					26				GND GND	26	
	25	S300 S310					25				S300 S310	25	
	24	S280 S290					24				S280 S290	24	
	23	S260 S270					23				S260 S270	23	
3	22	S240 S250					22				S240 S250	22	3
1	21	GND GND				1	21	1			GND GND	21	1
	20	S220 S230					20				S220 S230	20	
	19	S200 S210					19				S200 S210	19	
	18	S180 S190					18				S180 S190	18	
	17	S160 S170					17				S160 S170	17	
	16	GND GND					16				GND GND	16	
	15	A300 A310					15				A300 A310	15	
	14	A280 A290					14				A280 A290	14	
	13	A260 A270					13				A260 A270	13	
4	12	A240 A250					12				A240 A250	12	4
	11	GND GND					11				GND GND	11	
	10	A220 A230					10				A220 A230	10	
	09	A200 A210					09				A200 A210	09	
	08	A180 A190					08				A180 A190	08	
	07	A160 A170					07				A160 A170	07	
	06	GND GND					06				GND GND	06	
	05	MMFO PSW230					05				MMFO IRLMPO	05	
	04						04				DMPFO	04	
	03	MSEL020 RWCO					03				MSEL020 RWCO	03	
5	02	MSEL000 MSEL010					02				MSEL000 MSEL010	02	5
	01	GND MSIGO					01				GND MSIGO	01	
	00	P5 P5					00				P5 P5	00	
		1 2	1 2	1 2	1 2			1 2	1 2	1 2	1 2		
	41	P5 P5					41				P5 P5	41	
	40	GND KSIGO					40				GND KSIGO	40	
	39	FSEL020 FSEL030					39				FSEL020 FSEL030	39	
	38	FSEL000 FSEL010					38				FSEL000 FSEL010	38	
	37	STRTO MFINO					37				STRTO MFINO	37	
	36	GND GND					36				GND GND	36	
	35	B140 B150					35			B140 B150	RACKO	35	
6	34	B120 B130					34			B120 B130	GND GND	34	6
	33	B100 B110					33			B100 B110	LMRQO	33	
	32	B080 B090					32			B080 B090	MAR310 ATNO	32	
	31	GND GND					31			GND GND	GND GND	31	
	30	B060 B070					30			B060 B070	ACKO30 MTPCO	30	
	29	B040 B050					29			B040 B050	ACKO20 PRPCO	29	
	28	B020 B030					28			B020 B030	ACKO10 GND	28	
	27	B000 B010					27			B000 B010	ACKOOO HWO	27	
	26	GND GND					26			GND GND	GND GND	26	
	25	S140 S150					25			S140 S150	GND GND	25	
	24	S120 S130					24			S120 S130		24	
7	23	S100 S110					23			S100 S110	SYNO BHO	23	7
	22	S080 S090				0	22	0		S080 S090	CLOTO DAO	22	
	21	GND GND					21			GND GND	GND GND	21	
0	20	S060 S070					20			S060 S070	DRO CMDO	20	0
	19	S040 S050					19			S040 S050	SRO ADR30	19	
	18	S020 S030					18			S020 S030	D140 D150	18	
	17	S000 S010					17			S000 S010	D120 D130	17	
	16	GND GND					16			GND GND	GND GND	16	
	15	A140 A150					15			A140 A150	D100 D110	15	
	14	A120 A130					14			A120 A130	D080 D090	14	
	13	A100 A110					13			A100 A110	D060 D070	13	
8	12	A080 A090					12			A080 A090	D040 D050	12	8
	11	GND GND					11			GND GND	GND GND	11	
	10	A060 A070					10			A060 A070	D020 D030	10	
	09	A040 A050					09			A040 A050	D000 D010	09	
	08	A020 A030					08			A020 A030		08	
	07	A000 A010					07			A000 A010		07	
	06	GND GND					06				GND GND	06	
	05	SCLRO CCCO					05				SCLRO CCCO	05	
	04	SCCO VCCO					04				SCCO VCCO	04	
9	03	SCLRI GCCO					03				SCLRI GCCO	03	9
	02	TKILLO LCCO					02				LCCO	02	
	01	GND GND					01				GND GND	01	
	00	P5 P5					00				P5 P5	00	
		1 2	1 2	1 2	1 2			1 2	1 2	1 2	1 2		

NOTES

1. BACKPANEL-35-592.

PRE PRODUCTION APPROVAL | INIT | DATE | DEV T.A.F. 1/27/78 | REV

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED THE REVISION LEVEL OF THE DOCUMENT

SHT.	REV. LEV				
INDEX	SHT. NO.	1	2	3	4

NAME	TITLE	DATE
C. MICHAELS	DRAFT	12-19-77
	CHK	
T. FYFE	ENGR	
R. BARKER		
L. PEZZI	DIR ENG	

TITLE (LOWER BACKPANEL) MODEL 8/32 C&D (W/DFU BACKPANEL)

TASK NO. 03017 | DWG NO. 01-103 D08 | SHEET OF 1 - 4

BACK PANEL MAP

CONN.	TITLE	LMM		LMM		LMI		LMM		CONN.
	BD LOC.	A07		A06		A05		A04		
	TERM.	ROW		ROW		ROW		ROW		
	NO.	1	2	1	2	1	2	1	2	
1	41	PS	GND	PS	GND	PS	PS	PS	GND	1
	40	GND	GND	GND	GND	GND	GND	GND	GND	
	39	PIS	PIS	PIS	PIS			PIS	PIS	
	38	NIS	NIS	NIS	NIS			NIS	NIS	
	37	MDI50	MDI60	MDI50	MDI60	MDI50	MDI60	MDI50	MDI60	
	36	MDI30	MDI40	MDI30	MDI40	MDI30	MDI40	MDI30	MDI40	
	35	MDI10	MDI20	MDI10	MDI20	MDI10	MDI20	MDI10	MDI20	
	34	MD090	MD100	MD090	MD100	MD090	MD100	MD090	MD100	
	33	MD070	MD080	MD070	MD080	MD070	MD080	MD070	MD080	
	32	MD050	MD060	MD050	MD060	MD050	MD060	MD050	MD060	
	31	MD030	MD040	MD030	MD040	MD030	MD040	MD030	MD040	
	30	MD010	MD020	MD010	MD020	MD010	MD020	MD010	MD020	
	29	GND	MD000	GND	MD000	GND	MD000	GND	MD000	
	28	TEMPA ⊛	VT ⊛			TEMPA ⊛	VT ⊛	TEMPA ⊛	VT ⊛	
	27	WRTO	TEMP B ⊛	OWRTO		WRTO	TEMP B ⊛	WRTO	TEMP B ⊛	
	26	GND	GND	GND	GND	GND	GND	GND	GND	
	25	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	
	24	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	
	23	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	
	22	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	
	21	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	
	20	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	
	19	GND	GND	GND	GND	GND	GND	GND	GND	
	18									
	17									
	16	GND	GND	GND	GND	GND	GND	GND	GND	
	15									
	14									
	13									
	12									
	11	GND	GND	GND	GND	GND	GND	GND	GND	
	10		MS000	EWRTO	MS000 ⊛	EWRTO	MS000		MS000	
	09	MS010	MS020	MS010	MS020	MS010	MS020	MS010	MS020	
	08	MS030	MS040	MS030	MS040	MS030	MS040	MS030	MS040	
	07	MS050	MS060	MS050	MS060	MS050	MS060	MS050	MS060	
	06	MS070	MS080	MS070	MS080	MS070	MS080	MS070	MS080	
	05	MS090	MS100	MS090	MS100	MS090	MS100	MS090	MS100	
	04	MS110	MS120	MS110	MS120	MS110	MS120	MS110	MS120	
	03	MS130	MS140	MS130	MS140	MS130	MS140	MS130	MS140	
	02	MS150	MS160	MS150	MS160	MS150	MS160	MS150	MS160	
	01	GND	GND	GND	GND	GND	GND	GND	GND	
	00	PS	GND	PS	GND	PS	PS	PS	GND	
		1	2	1	2	1	2	1	2	
0	41	PS	GND	PS	GND	PS	PS	PS	GND	0
	40	GND	GND	GND	GND	GND	GND	GND	GND	
	39	LMBSYA0	LMBSYC0	LMBSYA0	LMBSYC0	LMBSYA0	LMBSYC0	LMBSYA0	LMBSYC0	
	38	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMDS0	
	37	LMBSYB0	LMRS0	LMBSYB0	LMRS0	LMBSYB0	LMRS0	LMBSYB0	LMRS0	
	36	GND	GND	GND	GND	GND	GND	GND	GND	
	35	DURO	MB20	DURO	MB20	DURO	MB20	DURO	MB20	
	34	GND	GND	GND	GND	GND	GND	GND	GND	
	33	MAI30	MAI40	MAI30	MAI40	MAI30	MAI40	MAI30	MAI40	
	32	MAI10	MAI20	MAI10	MAI20	MAI10	MAI20	MAI10	MAI20	
	31	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100	
	30	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080	
	29	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060	
	28	GND	GND	GND	GND	GND	GND	GND	GND	
	27	SCLR0		SCLR0		SCLR0		SCLR0		
	26	MCLR0	GND	MCLR0	GND	MCLR0	GND	MCLR0	GND	
	25	GND	GND	GND	GND	GND	GND	GND	GND	
	24	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	
	23	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	
	22	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	
	21	GND	GND	GND	GND	GND	GND	GND	GND	
	20	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	
	19	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	
	18	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	
	17	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	
	16	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	
	15	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	
	14	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010	
	13	GND	GND	GND	GND	GND	GND	GND	GND	
	12	IRLMP0	DLMP0	IRLMP0	DLMP0	IRLMP0	DLMP0	IRLMP0	DLMP0	
	11	GND	GND	GND	GND	GND	GND	GND	GND	
	10	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040	
	09	MA020		MA020		MA020		MA020		
	08	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070	
	07	MA010		MA010		MA010		MA010		
	06	MA000		MA000	GND	MA000		MA000		
	05	PAR0		PAR0		PAR0		PAR0		
	04	INH0	ERO	INH0	ERO	INH0	ERO	INH0	ERO	
	03		SPY		SPY		SPY		SPY	
	02	PIS	NIS	PIS	NIS			PIS	NIS	
	01	GND	GND	GND	GND	GND	GND	GND	GND	
	00	PS	GND	PS	GND	PS	PS	PS	GND	
		1	2	1	2	1	2	1	2	

CONN.	TITLE	LMM		LMI		MBC		CPA		CONN.
	BD LOC.	A03		A02		A01		A00		
	TERM.	ROW		ROW		ROW		ROW		
	NO.	1	2	1	2	1	2	1	2	
1	41	PS	GND	PS	PS	PS	PS	PS	PS	1
	40	GND	GND	GND	GND	GND	QUE0	GND	MSIG0	
	39	PIS	PIS			DMA160	DMA170	B300	B310	
	38	NIS	NIS			DMA140	DMA150	B280	B290	
	37	MD150	MD160	MD150	MD160	DMA120	DMA130	B260	B270	
	36	MD130	MD140	MD130	MD140	GND	GND	GND	GND	
	35	MD110	MD120	MD110	MD120	DMA100	DMA110	B240	B250	
	34	MD090	MD100	MD090	MD100	DMA080	DMA090	B220	B230	
	33	MD070	MD080	MD070	MD080	DMA060	DMA070	B200	B210	
	32	MD050	MD060	MD050	MD060	DMA040	DMA050	B180	B190	
	31	MD030	MD040	MD030	MD040	DMA020	DMA030	B160	B170	
	30	MD010	MD020	MD010	MD020	GND	GND	GND	GND	
	29	GND	MD000	GND	MD000	DMA000	DMA010	S300	S310	
	28			TEMPA ⊛	VT ⊛	DMX140	DMX150	S280	S290	
	27	OWRTO		WRTO	TEMP B ⊛	DMX120	DMX130	S260	S270	
	26	GND	GND	GND	GND	GND	GND	GND	GND	
	25	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	S240	S250	
	24	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	S220	S230	
	23	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	S200	S210	
	22	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	S180	S190	
	21	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	S160	S170	
	20	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	GND	GND	
	19	GND	GND	GND	GND	GND	CRDY0	GND	CRDY0	
	18					CMC020	CEEQ0	CMC020	CEEQ0	
	17					CMC000	CMC070	CMC000	CMC070	
	16	GND	GND	GND	GND	GND	GND	GND	GND	
	15					CD300	CD310	CD300	CD310	
	14					CD280	CD290	CD280	CD290	
	13					CD260	CD270	CD260	CD270	
	12					CD240	CD250	CD240	CD250	
	11	GND	GND	GND	GND	GND	GND	GND	GND	
	10	EWRTO	MS000	EWRTO	MS000	CD220	CD230	CD220	CD230	
	09	MS010	MS020	MS010	MS020	CD200	CD210	CD200	CD210	
	08	MS030	MS040	MS030	MS040	CD180	CD190	CD180	CD190	
	07	MS050	MS060	MS050	MS060	CD160	CD170	CD160	CD170	
	06	MS070	MS080	MS070	MS080	GND	GND	GND	GND	
	05	MS090	MS100	MS090	MS100	MB810	M2820	B140	B150	
	04	MS110	MS120	MS110	MS120	MTB20	MTB820	B120	B130	
	03	MS130	MS140	MS130	MS140	LOAD0	RUN0	B100	B110	
	02	MS150	MS160	MS150	MS160	SOT0	EOT0	B080	B090	
	01	GND	GND	GND	GND	GND	XEEQ0	GND	B070	
	00	PS	GND	PS	PS	PS	PS	PS	PS	
		1	2	1	2	1	2	1	2	
0	41	PS	GND	PS	PS	PS	PS	PS	PS	0
	40	GND	GND	GND	GND	GND	MTPC0 ⊛	GND	B060	
	39	LMBSYA0	LMBSYC0	LMBSYA0	LMBSYC0	LMEQ0 ⊛	BH0 ⊛	B040	B050	
	38	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMD50	B020	B030	
	37	LMBSYB0	LMRS0	LMBSYB0	LMRS0	PRPC0 ⊛	LMR50	B000	B010	
	36	GND	GND	GND	GND	GND	GND	GND	GND	
	35	DURO	MB20	DURO	MB20	CD140	CD150	CD140	CD150	
	34	GND	GND	GND	GND	CD120	CD130	CD120	CD130	
	33	MAI30	MAI40	MAI30	MAI40	CD100	CD110	CD100	CD110	
	32	MAI10	MAI20	MAI10	MAI20	CD080	CD090	CD080	CD090	
	31	MA090	MA100	MA090	MA100	GND	GND	GND	GND	
	30	MA070	MA080	MA070	MA080	CD060	CD070	CD060	CD070	
	29	MA050	MA060	MA050	MA060	CD040	CD050	CD040	CD050	
	28	GND	GND	GND	GND	CD020	CD030	CD020	CD030	
	27	SCLR0		SCLR0		CD000	CD010	CD000	CD010	
	26	MCLR0	GND	MCLR0	GND	GND	GND	GND	GND	
	25	GND	GND	GND	GND	SCLR0	GND	SCLR0	GND	
	24	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	S140	S150	
	23	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	S120	S130	
	22	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	S100	S110	
	21	GND	GND	GND	GND	GND	GND	GND	GND	
	20	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130			
	19	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	S080	S090	
	18	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	S060	S070	
	17	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	S040	S050	
	16	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	S020	S030	
	15	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	S000	S010	
	14	LMB000	LMB010	LMB000	LMB010	LMB000	LMB070			
	13	GND	GND	GND	GND	GND	GND	GND	GND	
	12	IRLMP0	DLMP0	IRLMP0	DLMP0	CR300	DLMP0	CR300	MAR310 ⊛	
	11	GND	GND	GND	GND	CR280	CR290	CR280	CR290	
	10	MA090	MA040	MA030	MA040	CR260	CR270	CR260	CR270	
	09	MA020		MA020		CR240	CR250	CR240	CR250	
	08	MAX060	MAX070	MAX060	MAX070	CR220	CR230	CR220	CR230	
	07	MA010		MA010		CR200	CR210	CR200	CR210	
	06	MA000	GND	MA000		GND	GND	GND	GND	
	05	PAR0		PAR0		CR180	CR190	CR180	CR190	
	04	INH0	ERO	INH0	ERO	CR160	CR170	CR160	CR170	
	03		SPY		SPY	CR140	CR150	CR140	CR150	
	02	PS	NIS			CR120	CR130	CR120	CR130	
	01	GND	GND	GND	GND	GND	DMFP0 ⊛	GND	GND	
	00	PS	GND	PS	PS	PS	PS	PS	PS	
		1	2	1	2	1	2	1	2	

NOTES
1. BACKPANEL – 35-692
⊛ WIRE WRAP RUNS

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE 8/32 C&D BACKPANEL UPPER
TAB NO. 03017
DWG NO. 01-103 D08
SHEET 2 OF 4

BACK PANEL MAP

CONN.	TERM. NO.	LMM 07 ROW 1	LMM 07 ROW 2	LMM 06 ROW 1	LMM 06 ROW 2	LMM 05 ROW 1	LMM 05 ROW 2	LMM 04 ROW 1	LMM 04 ROW 2	CONN.	TERM. NO.	LMM 03 ROW 1	LMM 03 ROW 2	LMM 02 ROW 1	LMM 02 ROW 2	LMM 01 ROW 1	LMM 01 ROW 2	LMM 00 ROW 1	LMM 00 ROW 2	CONN.
	41	P5	GND								41							P5	GND	
	40	GND	GND								40							GND	GND	
	39	P15	P15								39							P15	P15	
	38	N15	N15								38							N15	N15	
	37	MD150	MD160								37							MD150	MD160	
	36	MD130	MD140								36							MD130	MD140	
	35	MD110	MD120								35							MD110	MD120	
	34	MD090	MD100								34							MD090	MD100	
	33	MD070	MD080								33							MD070	MD080	
	32	MD050	MD060								32							MD050	MD060	
	31	MD030	MD040								31							MD030	MD040	
	30	MD010	MD020								30							MD010	MD020	
	29		MD000								29								MD000	
	28	TEMPA	VT								28							TEMPA	VT	
	27	WRTO	TEMPB								27							WRTO	TEMPB	
	26	GND	GND								26							GND	GND	
	25	LMB300	LMB310								25							LMB300	LMB310	
	24	LMB280	LMB290								24							LMB280	LMB290	
	23	LMB260	LMB270								23							LMB260	LMB270	
	22	LMB240	LMB250								22							LMB240	LMB250	
1	21	LMB220	LMB230							1	21							LMB220	LMB230	
	20	LMB200	LMB210								20	1						LMB200	LMB210	1
	19	GND	GND								19							GND	GND	
	18										18									
	17										17									
	16	GND	GND								16							GND	GND	
	15										15									
	14										14									
	13										13									
	12										12									
	11	GND	GND								11							GND	GND	
	10		MS000								10								MS000	
	09	MS010	MS020								09							MS010	MS020	
	08	MS030	MS040								08							MS030	MS040	
	07	MS050	MS060								07							MS050	MS060	
	06	MS070	MS080								06							MS070	MS080	
	05	MS090	MS100								05							MS090	MS100	
	04	MS110	MS120								04							MS110	MS120	
	03	MS130	MS140								03							MS130	MS140	
	02	MS150	MS160								02							MS150	MS160	
	01	GND	GND								01							GND	GND	
	00	P5	GND								00							P5	GND	
		1	2	1	2	1	2	1	2			1	2	1	2	1	2	1	2	
	41	P5	GND								41							P5	GND	
	40	GND	GND								40							GND	GND	
	39										39									
	38	LMRDYO	LMDS0								38							LMRDYO	LMDS0	
	37	LMBSYO	LMBS0								37							LMBSYO	LMBS0	
	36	GND	GND								36							GND	GND	
	35	DUAO	MBZO								35							DUAO	MBZO	
	34	GND	GND								34							GND	GND	
	33	MA130	MA140								33							MA130	MA140	
	32	MA110	MA120								32							MA110	MA120	
	31	MA090	MA100								31							MA090	MA100	
	30	MA070	MA080								30							MA070	MA080	
	29	MA050	MA060								29							MA050	MA060	
	28	GND	GND								28							GND	GND	
	27	SCLRO									27							SCLRO		
	26	MCLRO	GND								26							MCLRO	GND	
	25	GND	GND								25							GND	GND	
	24	LMB180	LMB190								24							LMB180	LMB190	
	23	LMB160	LMB170								23							LMB160	LMB170	
	22	LMB140	LMB150								22							LMB140	LMB150	
	21	GND	GND								21							GND	GND	
0	20	LMB120	LMB130							0	20	0						LMB120	LMB130	0
	19	LMB100	LMB110								19							LMB100	LMB110	
	18	LMB080	LMB090								18							LMB080	LMB090	
	17	LMB060	LMB070								17							LMB060	LMB070	
	16	LMB040	LMB050								16							LMB040	LMB050	
	15	LMB020	LMB030								15							LMB020	LMB030	
	14	LMB000	LMB010								14							LMB000	LMB010	
	13	GND	GND								13							GND	GND	
	12		LMPO								12								LMPO	
	11	GND	GND								11							GND	GND	
	10	MA030	MA040								10							MA030	MA040	
	09	MA020									09							MA020		
	08	MAX060	MAX070								08							MAX060	MAX070	
	07	MA010									07							MA010		
	06	MA000									06							MA000		
	05	PARO									05							PARO		
	04	INHO	ERO								04							INHO	ERO	
	03										03									
	02	P15	N15								02							P15	N15	
	01	GND	GND								01							GND	GND	
	00	P5	GND								00							P5	GND	
		1	2	1	2	1	2	1	2			1	2	1	2	1	2	1	2	

NOTES
1. BACKPANEL - 35-542

NAME
DRAFT
CHK
ENGR
DIR ENG
DATE

TITLE (MEMORY EXP) MODEL 8132 C&D (W/DFU BACKPANEL)

TASK No. 03017
DWG No. 01-103 008
SHEET 3 OF 4

2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

CONN 5

	2	1
16	UIR300	UIR310
15	UIR280	UIR290
14	UIR260	UIR270
13	UIR240	UIR250
12	YD300	YD310
11	YD280	YD290
10	YS300	YS310
09	YS280	YS290
08	SX300	SX310
07	SX280	SX290
06	GND	ININTO
05	GND	MAIO
04	GND	IREQO
03	GND	DREQO
02	GND	PSW210
01	GND	GND
00	GND	PASS1A

CONN 2

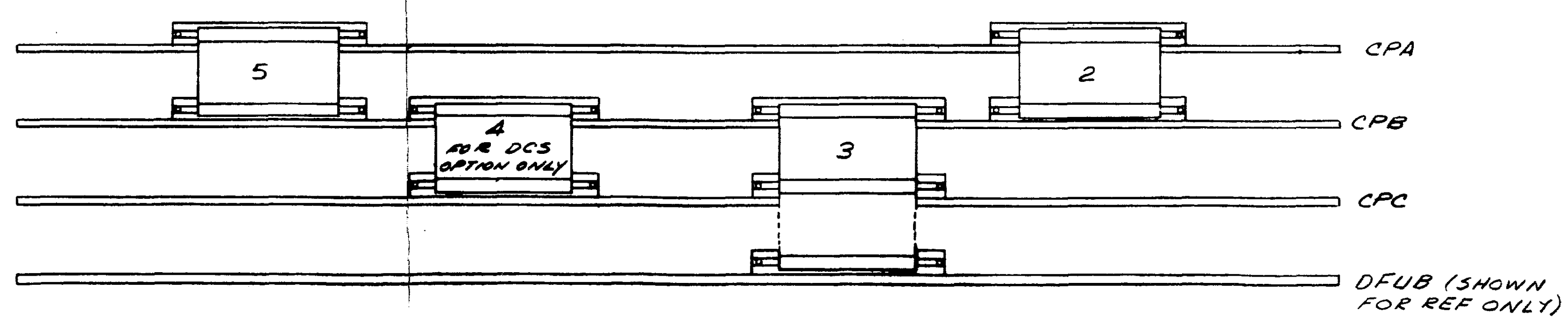
	2	1
16	MC020	MC030
15	MC000	MC010
14	GND	S2B0
13	GND	PCLKO
12	GND	JUTY1
11	GND	RX3D0
10	GND	SPARE
09	GND	CS000
08	GND	SRT1
07	GND	GND
06	GND	GND
05	BSEL031	BSEL041
04	BSEL011	BSEL021
03	GND	BSEL001
02	SSEL031	SSEL041
01	SSEL011	SSEL021
00	GND	SSEL001

CONN 3

	2	1
24	GND	GND
23	CSAD141	GND
22	CSAD121	CSAD151
21	GND	CSAD131
20	CSAD101	CSAD111
19	CSAD081	GND
18	CSAD061	CSAD091
17	GND	CSAD071
16	CSAD041	CSAD051
15	GND	GND
14	GND	GND
13	GND	SPARE
12	GND	PCLKO
11	PSW251	SECLK1
10	PSW260	PSW270
09	GND	S2B0
08	ASEL031	ASEL041
07	ASEL011	ASEL021
06	GND	ASEL001
05	BSEL031	BSEL041
04	BSEL011	BSEL021
03	GND	BSEL001
02	SSEL031	SSEL041
01	SSEL011	SSEL021
00	GND	SSEL001

CONN 4

	2	1
24	CSD301	CSD311
23	CSD281	CSD291
22	GND	CSD271
21	CSD261	CSD251
20	CSD241	GND
19	CSD221	CSD231
18	GND	CSD211
17	CSD201	CSD191
16	CSD181	GND
15	CSD161	CSD171
14	GND	CSD151
13	CSD141	CSD131
12	CSD121	GND
11	CSD101	CSD111
10	GND	CSD091
09	CSD081	CSD071
08	CSD061	GND
07	CSD041	CSD051
06	GND	CSD031
05	CSD021	CSD011
04	CSD001	GND
03	GND	CSWPO
02	GND	INCLKO
01	GND	CLKO
00	GND	GND



SCALE–

NAME | TITLE | DATE
DRAFT

TITLE
CPA/CPB, CPB/CPC/DFUB FRONT END CABLING

TASK NO. 03017
DWG NO. 01-103 D08

PERKIN ELMER

REVISIONS			
PRE PRODUCTION APPROVAL	DEV PROD	UNIT	DATE NOV 5 1979

RELEASED FOR PRODUCTION
MFG. ENG. ___ DATE ___

SEE MICROFILM FOR PREVIOUS REV LEVEL
REVISED SHTS 10 & 12

ME	BY	3832	M	1-22-79	R27

AREA E6 04D-06 WAS SIGNAL C011 W/LOCATOR 11A3 ADDED C011 w/ LOCATOR TO 04D-05. REVISED SHTS 1,2,3,4, 7, 10 & 12

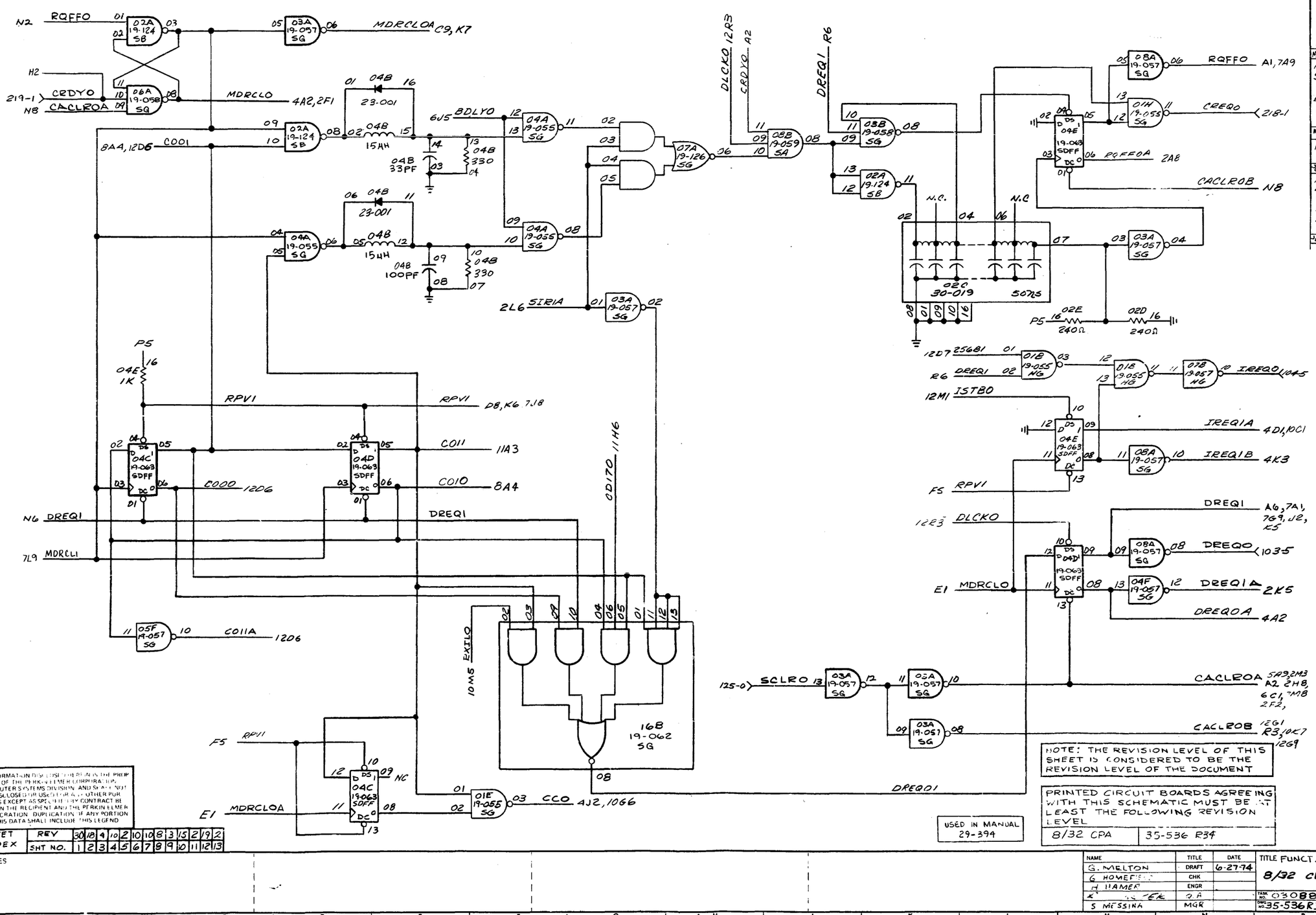
K	J	4231	R	3-4-80	R28

AREA N9 35-536 WAS R33 REVISED SHTS 1 & 10

J		4331	R	3-20-80	R29

AREA A2, ADDED CROSS REF LOC H2 TO 06A10, CRDYO. AREA H2, CROSS REF LOC FOR 08B11 WAS RPV1A, 2A5. REVISED SHTS 1 & 2.

		4536	E	12-11-80	R30



NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

8/32 CPA	35-536 R34

USED IN MANUAL 29-394

SHEET INDEX	REV	30	18	9	10	2	10	10	8	3	15	2	19	2
	SHT NO.	1	2	3	4	5	6	7	8	9	10	11	12	13

NOTES

NAME	TITLE	DATE
G. MELTON	DRAFT	6-27-74
G. HOMEFIELD	CHK	
H. HAMER	ENGR	
E. [illegible]	Q.A.	
S. MESSINA	MGR	

TITLE FUNCT. SCHEMATIC
8/32 CPA

TASK NO. 03088
DWG NO. 35-536R30 D08
SHEET OF 1 - 13

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
FOR PREVIOUS REV LEVELS SEE MICRO-FILM COPY. AREA L6 ADDED 7A6 TO SIRIA. AREA L7 REVERSED PINS 04 & 05 OF IC 12W AREA K7 RMVD 7A6 FROM SIRI. AREA R2 7L9 WAS 7L7 ON SDRI. AREA C7 REVERSED PINS 09 & 11 OF IC 12A.				
KR	4231	R	3-7-80	R17
AREA A5, DELETED RPVIA & CROSS REF LOC 1H1. (FROM 09B13)				
KV	45306	R	12-11-80	R18

from CPB

116-2 MC030

216-2 MC020

115-2 MC010

215-2 MC000

100-5 PASSIA — If "Ø" = Branch not occuring

09A 19-126 SG; 09B 19-126 SG; 09B 1K 16 P5; 16A 19-057 SG → PASS0A 12A1, 12A3

13E 19-057 SG → SMC031 C9

08A 19-057 SG → SMC011 C9

08A 19-057 SG → SMC000 → PSW210 102-5

15A 19058 SG; K9 ACLK1; 08B 19-059 SA; IC2 MDECLD; DS 14M 19-063 → N.C.; 01E 19-055 SG → IRB CACLR0A

CPC011 3F4 — INCR MAR by 4

CPC001 10K7 — INCR MLC by length of Last CMD

04F 19-057 SG → SMC000A H8, D7

04F 19-057 SG → SMC020A C9, D6

SMC001; SMC021; SMC030; SMC010; SMC020

Relocation & Prot enable → 07A 19-126 SG → SPROT1 7A5, 7C4, 8R3, 12A6, 12A9, 8F1

10A 19-055 SG; 04A 19-055 SG; P6 10A 1K 16

12D 19-116 4 TO 1 MUX

DATA R/W operation → DRDW1 12A2

IR1 7A6, 12A1, 10E4

IR1 — INSTRUCTION Read

IN7 7G7 DREQIA; 16A 19-057 SG; 00D 19-126 SG; 07B 19-057 SG → SDRDW1 6A4, 8A4; SDRDW0 8A4

7G2 8C1 SIRO; 05F 19-057 SG → SIRIA 1F4, 7A6

12B QUAD D FF 19-131 — INStruction Read — SIR1 4A3, 7J3, 12A6

FWWRTO 6J1, 11A4

J2 SMC000A

INF CACLR0A

Illegal Memory Data Write force mem Read

7L6 CDWO

12W 19-058 SG → CMC020 118-1

01A 19-055 SG; 12W 19-058 SG → CMC010 217-1

STAT0 7L8

10A 19-055 SG; 12W 19-058 SG → CMC000 117-1

CMC - mem CMD Bus to MBC

DATA Read

12C 19-116 SELB SELA STB1 STB2 OUTPUTS 4 TO 1 MUX

15D 19-131 QUAD D FF — CLK ACLK1 09; CLR B; IN8 CACLR0A

NC; RHO 04 F8; KB ACLK1 09

SDRO 12E2 — 2nd ½ word

SDRI 7L9, 4A2, 10E2

SRHO 12J8

SDWI 11A3, 7A4, 7H8, 7L8

SDWO AC3, 12L3 — Data Write

SSEL001 03; SSEL011; SSEL021; SSEL031; SSEL041; STRT0; 12C2; 101-2; 202-2; 102-2

16H 19-057 SG; 12A 19-129 3 TO 8 DECODER; LDMLC0 3A3, 3L5

LDMAR0 3B4, 3E1, 10G4, 10L3

J2 SMC020A; J2 SMC000A

13A 19-126 SG; 10B 19-062 SG

LDMDR0 4A1, 6G1

IN3 RQFF0A; 03D 19-063 DS DC; 4H3 CK1B; 6F6 XPU1

SLMDR0 4B4; SLMDR1 6G1

Rd half word → RHO M2

16A 19-058 SG

F2 SMC031; J2 SMC020A; C4 SMC000; 10A 19-055 SG; 15A 19-058 SG

109-2 CS000 control state "Ø"; 13E 19-057 SG

10K7, 3F4, 12A1 CS001; 4C1 CKIC; 14K 10-059 SA → ACLK1 C1

MCØØ:Ø3 Decode & Latching

NOTES

NAME	TITLE	DATE
G MELTON	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC 8/32 CPA

TASK NO. 03088; DWG NO. 35-536 R18 DOB; SHEET OF 2-13

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS			
DELETED: 19-117 @ 08E, 19-057 @ 07B, 19-055 @ 10D			
ADDED: MNEMONICS 'LDMRCKO @ B3, 'CSOO1 @ F4, 'C7K1 @ L8.			
9/4	JH	23088-31	2-3-75 R01
AREA B2: DELETED GATE 07B (19-057) AND RELATED CIRCUITRY WHICH SHOWED; 07B12 TO 07F09 CK0B. 07B13 TO 10D02 & MNEMONIC CK1A. MNEMONIC CLOCKO, & 330Ω & 470Ω RESISTORS WERE NOT SPECD. AREA E8: 09F 10 WAS TO 06F09 MNEMONIC C4 WAS NOT SPECD			
WS	GH	2698	12-16-75 R02
REVISED ALL REF'S TO SHT 9 AGAINST 09D, 08D, 07D, 06D, 06E & 07E			
PM	JJ	3094	1-24-77 R03
AREA A3 ADDED LOCATOR 441 TO SIGNAL CLOCKO.			
KR	JJ	4231	R 3-6-80 R04

NOTES

NAME	TITLE	DATE
G MELTON	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC

8/32 CPA

TASK NO. 03088

DRG NO. 35-536,804D08

SHEET OF 3-13

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
ADDED: 2-19-055 @02F-SHT LOC B2 & M1. CHANGED: 'MCLKO & 'MCLKOA WERE CONNECTED.	GN	03088-31	2-3-75	R01
ADDED: PSA MNEMONIC AT LOC B7 & H7.	GN	03088-48	3-5-75	R02
ADDED 2DB TO LDMDRO & 2AB TO CK1B SLMDRO WAS LDMRO	GN	03088 -55	3-27-75	R03
10C1 & 12A3 WENT TO 10J08	GN	03088 -72	4-22-75	R04
ADDED 10E4 TO CK1B	GN	2521	5-28-75	R05
AREA M3: CK1A WAS CROSS-REFERENCED TO 3B2	WS	2698	12-16-75	R06
REVISED ALL REF'S TO SHT 9 AGAINST 09K, 09J, 08K. 08J, 07K	PM	3094	1-24-77	R07
AREA H3 2H9 WAS ADDED 06M01, 07M01, 08M01, 09M01 AND 06501, 07501, 08501, 09501 WERE CONNECTED TO SLMDRO 2DB, AREA G5 ADDED SLMDR0A	GP	3242	7-29-77	R08
AREA C1, ADDED 08A, 19-057 SG, PIN 13 TO 10J-03. PIN 12 "CK1C" TO SHTS 269. 10C1 & 12A3. AREA M3, DELETED SHT LOC 2H8, ADDED 10G4. AREA H3, DELETED SHT. LOC. 10C1, 12A3, 10E4 & 2H9 FROM "CK1B" ADDED 6G2. AREA G4, SLMDR0A 6G4 WAS SPEC'D AS SLMDR0A 2F9.	WTA	4S 3551	5-23-78	R09
AREA B1 10J03 WAS CONNECTED TO CONNECT13-2. ADDED LOCATOR 3A3 TO SIGNAL CLOCKO.	KR	4231	3-6-80	R10

NOTES

NAME	TITLE	DATE
G. MELTON	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 CPA

TASK NO. 03088
ENG NO. 35-536 R10 D08

SHEET OF 4-13

BRUNING 44 231 16042

PERKIN ELMER

REVISIONS

AREA F9: 00D-03 WAS IR271. 00D-02 & 05 WAS 5IR1. 00D-04 WAS IR281. 00D-06 WAS TO 13W-019-02

PE	PM	03088-31		2-4-75	R01

CHANGED: 04F11 WAS CKOA' MNEMONIC.

PE	PM	03088-57		4-8-75	R02

215-1 CD310 11H2 — 00A 19-131 (4D) — 02 USR310 <110-5; 03 NC
115-1 CD300 11H2 — 05 2D — 07 USR300 <210-5; 06 NC
214-1 CD290 11H2 — 12 3D — 10 USR290 <109-5; 11 NC
114-1 CD280 11H1 — 13 4D — 15 USR280 <209-5; 14 NC
4N2 LDUIR0 — 09 CLK
6E5 XPU1 — 01 CLR

213-1 CD270 11H1 — 00B 19-131 (4D) — 02 UDR310 <112-5; 03 NC
113-1 CD260 11H1 — 05 — 07 UDR300 <212-5; 06 NC
212-1 CD250 11H5 — 12 — 10 UDR290 <111-5; 11 NC
112-1 CD240 11H4 — 13 — 15 UDR280 <211-5; 14 NC
09 CLK
01 CLR

210-1 CD230 11H4 — 00C 19-131 (4D) — 02 UIR310 <116-5; 03 UIR311 10A3
110-1 CD220 11H4 — 06 — 07 UIR300 <216-5; 06 UIR301 10A3
209-1 CD210 11H4 — 12 — 10 UIR290 <115-5; 11 UIR291 10A3
109-1 CD200 11H3 — 13 — 15 UIR280 <215-5; 14 UIR281 10A3
09 CLK
01 CLR

208-1 CD190 11H7 — 00C 19-131 (4D) — 02 UIR270 <114-5; 03 UIR271 10A3
108-1 CD180 11H6 — 05 — 07 UIR260 <214-5; 06 UIR261 10A3
207-1 CD170 11H6 — 12 — 10 UIR250 <113-5; 11 UIR251 10A4
107-1 CD160 11H6 — 13 — 15 UIR240 <213-5; 14 UIR241 10A4
09 CLK
01 CLR

7N8 ININTO — 01 — 02 — 13W 19-059 5A — 12
1N8 CACLR0A — 13

229-1 S310 — 10M 19-131 (4A) — 02 SR310 4A4; 03 SR311 3A6,3D1,13J7
129-1 S300 — 05 — 07 SR300 4A4; 06 SR301 3B6,3D1,13H7
228-1 S290 — 12 — 10 SR290 4B4; 11 SR291 3E1,13H7
128-1 S280 — 13 — 15 SR280 4B4; 14 SR281 3E1,13H7
09 CLK
6E4 XPU1 — 01 CLR

227-1 S270 — 10S 19-131 (4A) — 02 SR270 4C4; 03 SR271 3F5,13D7
127-1 S260 — 05 — 07 SR260 4C4; 06 SR261 3F5,13C7
225-1 S250 — 12 — 10 SR250 4C4; 11 SR251 3F5,13C7
125-1 S240 — 13 — 15 SR240 4C4; 14 SR241 3F5,13C7
09 CLK
01 CLR

2241 S230 — 10T 19-131 (4A) — 02 SR230 4D4; 03 SR231 3H5,13M4
124-1 S220 — 05 — 07 SR220 4D4; 06 SR221 3H5,13M4
223-1 S210 — 12 — 10 SR210 4E4; 11 SR211 13H5,13L4
123-1 S200 — 13 — 15 SR200 4E4; 14 SR201 3H5,13L4
09 CLK
01 CLR

222-1 5190 — 10W 19-131 (4A) — 02 SR190 4F4; 03 SR191 3K5,13G4
122-1 5180 — 05 — 07 SR180 4F4; 06 SR181 3K5,13G4
221-1 5170 — 12 — 10 SR170 4G4; 11 SR171 3K5,13F4
121-1 5160 — 13 — 15 SR160 4F4; 14 SR161 3K5,13F4
09 CLK
01 CLR

4A1 CLOCK0 — 11 — 04F 19-057 5G — 10

224-0 S150 — 04T 19-131 (4A) — 02 SR150 4H4; 03 SR151 3M5,13B4
124-0 S140 — 05 — 07 SR140 4H4; 06 SR141 3M5,13B4
223-0 S130 — 12 — 10 SR130 4H4; 11 SR131 3M5,13A4
123-0 S120 — 13 — 15 SR120 4H4; 14 SR121 3M5,13A4
09 CLK
6E5 XPU1 — 01 CLR

222-0 S110 — 04W 19-131 (4A) — 02 SR110 4J4; 03 SR111 13L1
122-0 S100 — 05 — 07 SR100 4J4; 06 SR101 13L1
219-0 S090 — 12 — 10 SR090 4K4; 11 SR091 13L1
119-0 S080 — 13 — 15 SR080 4K4; 14 SR081 13K1
09 CLK
01 CLR

218-0 S070 — 03T 19-131 (4A) — 02 SR070 4L4; 03 SR071 13G1
118-0 S060 — 05 — 07 SR060 4L4; 06 SR061 13F1
217-0 S050 — 12 — 10 SR050 4L4; 11 SR051 13F1
117-0 S040 — 13 — 15 SR040 4L4; 14 SR041 13F1
09 CLK
01 CLR

216-0 S030 — 03W 19-131 (4A) — 02 SR030 4M4; 03 SR031 13B1
116-0 S020 — 05 — 07 SR020 4M4; 06 SR021 13B1
215-0 S010 — 12 — 10 SR010 4N4; 11 SR011 13B1
115-0 S000 — 13 — 15 SR000 4N4; 14 SR001 13A1
09 CLK
01 CLR

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 CPA
TASK NO. 03088
DWG NO. 35-536 R02 D08
SHEET 5 OF 13

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
EXTENSIVE REVISIONS TO AREA B2, C9 FOR THESE AND PREVIOUS REV'S SEE VOID COPY IN FILES				
G.P.	11	3292	8-1-77	R09
AREA G2 & G3, ADDED 04F, 19-057 SG & 11T, 19-126 SG.				
WTA	A3	3551	5-23-78	R10

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

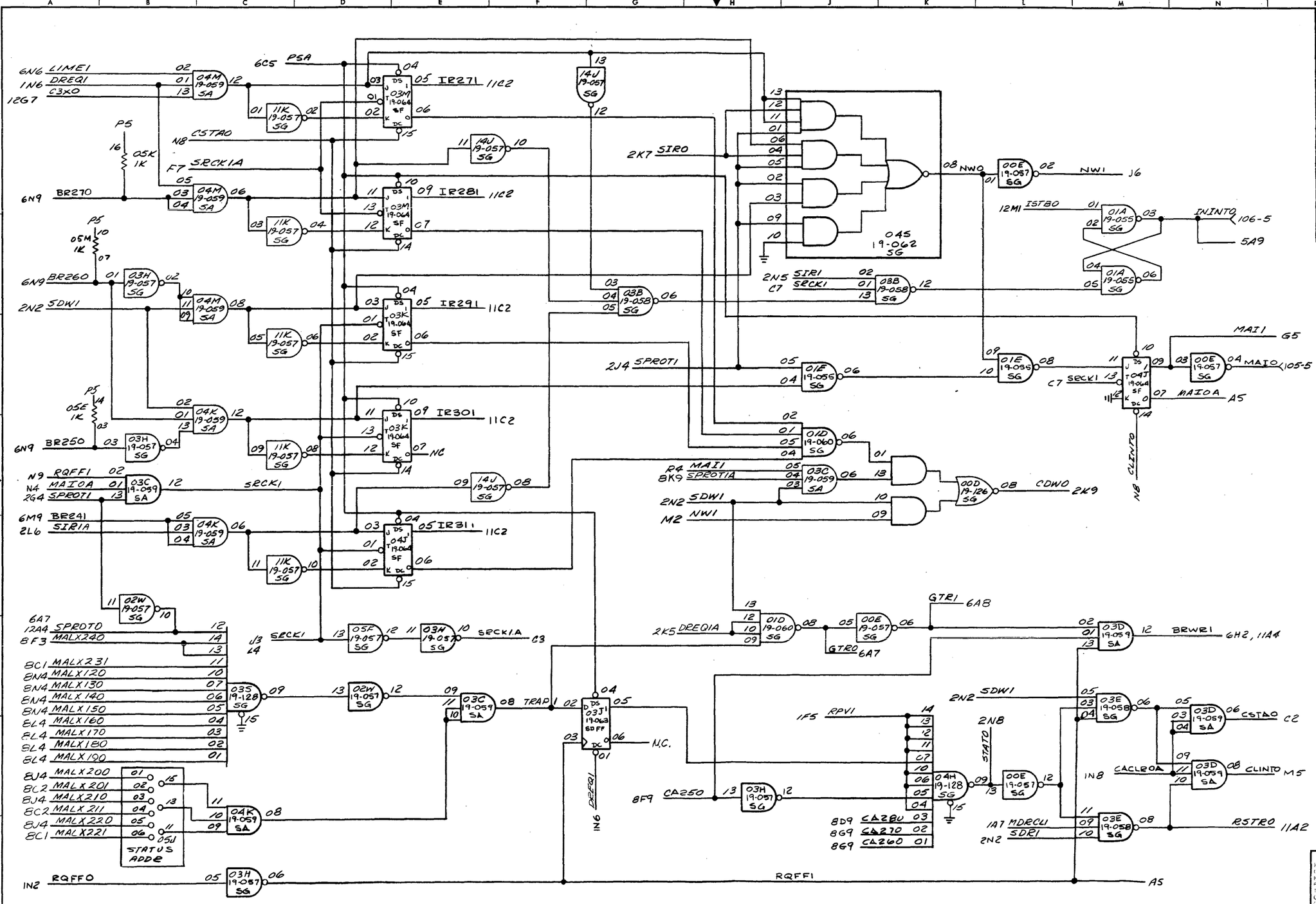
TITLE FUNCTIONAL SCHEMATIC
8/32 CPA

TASK NO. 03088 | DWG NO. 35-536 R10 008 | SHEET OF 6-13

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
EXTENSIVE CHANGES TO REV07, FOR REV08 AND PREVIOUS REVS SEE VOID COPY IN FILES				
GP	JJ	3242	8-1-77	R07
AREA A5, SHT LOC FOR "SPROTI" WAS 2J4. AREA A6, SIRI, 2K7 WAS SPECD AS SIRIA, 2N5. AREA B5: PIN 04 WAS NOT SPECD ON 03H.				
WTA	MS	3551	5-23-78	R08
AREA H5, 03C-04 & 05 WERE CONNECTED, SHT. LOC BK9 & SPROTIA WERE NOT SPEC'D.				
GP	JJ	3801	M 10-31-78	R09
AREA A6 SIGNAL SIRIA WITH LOCATOR 2L6 WAS SIRI W/ 2K7. AREA N7 6H2 WAS GD2				
KR	JJ	4231	R 3-7-80	R10



NOTES

NAME	TITLE	DATE	TITLE
G. MELTON	DRAFT		FUNCTIONAL SCHEMATIC 8/32 CPU
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03088
			DWG NO. 35-536 R10008
			SHEET OF 7-13

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
EXTENSIVE CHANGES TO REVOT, FOR REVOG AND PREVIOUS REVS SEE VUID COPY IN FILE 5.				
G.P	JV	3242 H	8-2-77	RD7
AREA J 9, 01A (19-056) WAS ADDED.				
GP	JV	3801	M	10-31-78	RD8

J4 MALX230 01 — 02W 19-057 SG — 02 MALX231 7A7
J4 MALX220 03 — 02W 19-057 SG — 04 MALX221 7A9
J4 MALX210 05 — 02W 19-057 SG — 06 MALX211 7A8
J4 MALX200 09 — 02W 19-057 SG — 08 MALX201 7A8

STRO 2J6 — 01B 19-055 SG

SPROT1 2J4

10C 19-066 2TO1 MUX — SEL, ENB, A; 4A 4B 3A 3B 2A 2B 1A 1B; 4Y 3Y 2Y 1Y
09C 19-066 2TO1 MUX
08C 19-066 2TO1 MUX
07C 19-066 2TO1 MUX
06C 19-066 2TO1 MUX

	A	B	Y
10C	SM2X281 9E9	SM2X291 9E9	MLC281 3D6
09C	SM2X241 9G9	SM2X251 9G9	MLC241 3H9
08C	SM2X201 9J9	SM2X211 9J9	MLC201 3J9
07C	SM2X161 9K9	SM2X171 9K9	MLC161 3K9
06C	SM2X121 9M9	SM2X131 9M9	MLC121 3M9

	A	B	Y
10C	SM2X301 9D9	SM2X311 9D9	MLC301 3D6
09C	SM2X261 9F9	SM2X271 9F9	MLC261 3H9
08C	SM2X221 9H9	SM2X231 9H9	MLC221 3J9
07C	SM2X181 9L9	SM2X191 9L9	MLC181 3K9
06C	SM2X141 9N9	SM2X151 9N9	MLC141 3M9

15E 19-126 SG — 256 SDRDWI 04, 10K3 RX2F1 05 — 06
Carry Commands — 1B3 C001, 1E6 C010, 255 SDRDWO — 03E 19-058 SG — 12
11K 19-057 SG — 13 — RX2P4-1 — 902

6A8 MALX280, MALX290, 6A8, MALX260, MALX270, 6A8
09 — 10 — 12 — 13 — 08 — 11 — 09F 19-125 S80
PROTQ — 7A7 MALX240

01K 330Ω PS

MALX200 6L9, A2, 7A8
MALX210 6L9, A2, 7A8
MALX220 6L9, A2, 7A9
MALX230 6L9, A1

MALX160 6L6, 7A8
MALX170 6L6, 7A8
MALX180 6L6, 7A8
MALX190 6L6, 7A8

MALX120 7A7
MALX130 7A7
MALX140 7A7
MALX150 7A7

02W 16 1K PS
04M 01 16 330Ω PS
02J 07 10 PS
02H 16
04 05E13
05 05E12 1K
02M 07 1K 10 PS
02K 16
06 05E11
07 05E10
02H
025 16 PS
07 02T 10
07 05T 10
01 05S 16

6L9 6L9 6L9 6L9 — BR200 BR210 BR220 BR230
6K9 6K9 6K9 6K9 — BR160 BR170 BR180 BR190
6H9 6H9 6H9 6H9 — BR120 BR130 BR140 BR150

05S 19-068 LOOK AHEAD CARRY GEN — Cn+x, Cn+y, Cn+z; P, G; Cn, G3 P3 G2 P2 G1 P1 G0 P0; NC
INPUTS 05S 19-067 4 BIT ALU — B3 A3 B2 A2 B1 A1 B0 A0; Cn; SEL IN; M; S3 S2 S1 S0
OUTPUTS — F3 F2 F1 F0; G; P; Cn+4; A=B
05K 19-067 4 BIT ALU
02H 19-067 4 BIT ALU
02K 19-067 4 BIT ALU
02S 19-067 4 BIT ALU

Effective Address =
CA = MLC+BR(MAC)+ Carries(2or4)
CA = Core Address

12G7 C3X1

111-0 CA280, 211-0 CA290, 112-0 CA300, 6K1
769
109-0 CA240, 209-0 CA250, 110-0 CA260, 210-0 CA270, 6A8, 7K9
107-0 CA200, 207-0 CA210, 108-0 CA220, 208-0 CA230
01A 19-055 SG — SPRDTA 7H5
104-0 CA160, 204-0 CA170, 105-0 CA180, 205-0 CA190
102-0 CA120, 202-0 CA130, 103-0 CA140, 203-0 CA150

NOTES

This sheet is SUM1X - See pg 20 - CPA Theory

NAME	TITLE	DATE
G. MELTON	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 CPU
TASK NO. 03088
DWG NO. 35-536RDBD08
SHEET OF 8-13

BRUNING 44-231 18042

PERKIN ELMER
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
REVISED & REDRAWN FOR CHANGES SEE VOID DWG. SEE 35-536 R02 D08 SHT 9
PM GV 3094 1-24-77 R03

11E 19-133 — A1 B1 A2 B2 A3 B3 A4 B4 — CO C4 — E1 E2 E3 E4 C

11F 19-133 4-BIT ADDER

11H 19-133 4-BIT ADDER

11J 19-133 4-BIT ADDER

11M 19-133 4-BIT ADDER

10K5 RX3F1

10H 19-065 2 TO 1 MUX — 1A 1B 2A 2B 3A 3B 4A 4B — 1Y 2Y 3Y 4Y

09H 19-065 2 TO 1 MUX

08H 19-065 2 TO 1 MUX

07H 19-065 2 TO 1 MUX

06H 19-065 2 TO 1 MUX

07B XRP1 P5 16 1K B9

06B 19-068 — P Cn+x Cn+y Cn+z G — Cn G3 P3 G2 P2 G1 P1 G0 P0

05C 19-067 4-BIT ALU — M S0 S1 S2 S3 Cn — A0 A1 A2 A3 CN+4 — F0 F1 F2 F3

05A 19-067 4-BIT ALU

14A 19-067 4-BIT ALU

11A 19-067 4-BIT ALU

11C 19-067 4-BIT ALU

RXIDOA 10M2 RXIDOB 10M2

D6 XRP1

SCALE—	NAME	TITLE	DATE
TOLERANCE XX ± .005, X ± .02, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	P.H. MARCUS	DRAFT	1-24-77
		CHK	
		ENGR	

TITLE
FUNCTIONAL SCHEMATIC
8/32 CPA

TASK NO. 03088
DRG. NO. 35-536 R03 D08
SHEET OF 9 —13

BRUNING 44-231 24538

PERKIN ELMER

4C1 CKIC
4H2 LDMDR1
1N6 IREQ1A
14E 19-126 SG
2N1 B2 SDRO
11J6 CD170
16H 19-057 SG
13C 19-060 SG
4N1 LDH0
15W 19-059 SA
E1 SDRO
14H 19-055 SG
RI1X0 12J8
5D5 UIR311
5D5 UIR301
5D6 UIR291
5D6 UIR281
5D7 UIR271
5D7 UIR261
5D8 UIR251
5D8 UIR241
14D 19-142 F41 256X 4 PROM
11J6 CD160
16H 19-057 SG
14C 19-058 SG
RI1021
RX0011
2N5 IR1
4M3 CK1A
12A2 SIRT1
12E 19-058 SG
RRSF1
16A 19-057 SG
M5 EXIL1
15B 19-055 SG
P5 13B 16.1K
2D7 LDMAR0
3C5 LDMRCK0
13B 19-063 SDFF
1F9 CC0
13B 19-063 SDFF
CACLE0B 1R8
12C 19-058 SG
14M 19-063 SDFF
RX1D0 12J8
NC
13B 19-063 SDFF
RX3F0
12J8 12G9 RX2F0
16C 19-130 SG
RX1D0B 9C7
RX1D0A 9C7
13B 19-063 SDFF
RX2F1
8A4, 9B1, 12G8
2D7 LDMAR0
16A 19-057 SG
15W 19-059 SA
JUTY1 112-2
00F 19-125 SB0
MS1G0 2A0-1
13B 19-063 SDFF
9C1 RX3F1
RX3EN1
14C 19-058 SG
RX3D0 111-2
15C 19-059 SA
RX1L0 F6, 1F8
13B 19-063 SDFF
INCR1 3D7
2F5 2G9 CPC001 C5001
15C 19-059 SA
INCR021 3D7

REVISIONS

AREA B1: REMOVED IREQ1A TO 13A-09 & 10. CK1A WAS TO 13A-13. LDMDR1 WAS TO 13A-01 13D-04 & 10 WAS TO 13A-08. AREA F1 & F3: 13C-10 & 14C-01 WERE N.C. AREA F1: 13C-13 WAS MDX011. AREA F5: 14C-13 WAS MDX001. AREA C3: 14D-12 WAS N.C. AREA H3: 13D-03 & 11 WAS TO 16A-02. 16A-01 WAS TO DD1. AREA J5: 13B-03 WAS TO LDMAR0. 13B-02 WAS TO 16A-04. 16A-03 WAS TO CK1A. AREA J6: 13B-10 WAS TO 13B-01, & 13. AREA L7: 15C-11 & 03 WERE TO INHMLC0 PIN 107-2 AREA J6: 13B-11 WAS TO 15B-06. 15B-05 WAS TO IR1. 15B-04 WAS TO DREQ1. AREA L2: 16C-05 & 13 & 14C-03 WERE RX001. 16A-09 WAS BMX5LB1 AREA N4: 15W-06 WAS MS1G0 PIN 240-1. 00F-03 WAS JUTY1 PIN 112-2

PC	03088-31		2-4-75	R01

CHANGED: 16A09 WAS 'BMXNB1' MNEMONIC.

GW	03088-50		3-6-75	R02

CHANGED: GATE @ 00F SHT LOC N4 WAS 19-056. 15B05 WAS CK1A

GW	03088-72		4-27-75	R04

16H WAS REPLACED BY 14H IN LOC D2

GW	03088-73		4-30-75	R05

ADDED GATE 10D TO LOC G4; 13B04 WAS 'DSTB0' TO 12M2

GW	2521	—	5-28-75	R06

AT LOC G5 GATE 12D WAS 10D; 12E12 WAS 10D06, 12E02 WAS 10D05; 10D04 'SIR1A'; 12E01 & 12B12 WAS NOT SPEC.

GW	2542	—	6-9-75	R07

AREA G2, 15W-09 & 15W-11 WERE REVERSED.

JC	2355	—	7-14-75	R08

AREA K4: CROSS REF 9B1 WAS ADDED TO RX2F1. CROSS REF 9C1 (RX3F1) WAS 9B2.

JC	2892	-	7-21-76	R09

AREA 10K5, 9C4 WAS 9C1 AREA 10M2, 9C7 WAS 9C6

PM	3094		1-24-77	R10

AREA F4, 12E-02 WAS SPEC'D AS MNEMONIC "CK1B" SHT. LOC 4H3. AREA C1, 15B-05 WAS SPEC'D AS "CK1B" SHT LOC, 4M3

WA	3551		5-23-78	R11

EXTENSIVE REVISION FOR PREVIOUS REV. SEE MICRO-FILM COPY

GP	3801	M	10-31-78	R12

AREA L3: DELETED 14C (19-058). AREA K-M1: ADDED 14C & 16M (19-063)

KR	3832	M	1-22-80	R13

AREA L2, 16C WAS 19-060 (2 PLACES).

KR	4231	R	3-6-80	R14

AREA C4, 14D WAS 19-084, 4-BIT ROM. AREA F2, 13C12 DESTINATION WAS 14C12

LW	4337	R	3-20-80	R15

NOTES

NAME	TITLE	DATE
G. MELTON	DRAFT	6-28-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCT. SCHEMATIC 8/32 CPU

TASK NO. 03088 DWG NO. 35-536215 D08 SHEET OF 10-13

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS
AREA C2: 11W-01 & 15 WAS TO 14W-08. 09W-01 & 15 WAS TO 15B-11 & 14W-11 14W-09 WAS RSTRI. 14W-10 & 15B-12 WAS CS001. 15B-13 WAS DWI. AREA C4: ADDED 13A. AREA D5 & D7: 11T-01 WAS MDR071, 11T-03 WAS MDR061, 11T-05 WAS MDR051, 11T-11 WAS MDR041, 11T-02 WAS SX310, 11T-04 WAS SX300, 11T-06 WAS SX290, 11T-10 WAS SX280. AREA C9: ADDED 11B,9
DS | WH | 03088-82 | 12-4-75 | P01
CHANGED: 15B12 WAS 'C001' MNEMONIC.
GH | WH | 03088-48 | 3-6-75 | P02

11W 19-134 HEX BUFF/INV.
- 02 NC
- 04 IR271 (7D1)
- 06 IR281 (7D2)
- 10 IR291 (7D4)
- 12 IR301 (7D5)
- 14 IR311 (7D6)
- 15 RSTRO (7R9)
- 03 NC
- 05 CD270 H1
- 07 CD280 H1
- 09 CD290 H2
- 11 CD300 H2
- 13 CD310 H2

09W 19-134 HEX BUFF/INV.
- 4C9 MDR261 02 → 03 CD260 K6, 4C4, 5A4
- 4C9 MDR271 04 → 05 CD270 K7, 4C4, 5A3, E1
- 4B9 MDR281 06 → 07 CD280 K3, 4B4, 5A3, E1
- 4B9 MDR291 10 → 09 CD290 K4, 4B4, 5A2, E2
- 439 MDR301 12 → 11 CD300 K4, 4A4, 5A2, E2
- 439 MDR311 14 → 13 CD310 K4, 4A4, 5A1, E2
- 01, 15

07W 19-134 HEX BUFF/INV.
- 4N9 MDR021 02
- 4M9 MDR031 04
- 4L9 MDR041 06
- 4L9 MDR051 10
- 4L9 MDR061 12
- 4L9 MDR071 14
- 01, 15
- 03 CD040 (129-0)
- 05 CD030 (228-0)
- 07 CD020 (128-0)
- 09 CD020 4N4
- 11 CD030 4M4
- 13 CD040 4L4
- CD050 4M4
- CD060 4L4
- CD070 4L4
- CD070 (230-0)
- CD060 (130-0)
- CD050 (229-0)

15B 19-055 5G: 2N2 SDWI → 13, 12 → 11 CDENO

139 19-126 5G: 1E5 CO11 → 09, 10; 7N7 BRWRI → 01; 2U7 EWWRTO → 13; → 08 CDXNO K5, 4U3

09T 19-134 HEX BUFF/INV.
- 4E9 MDR201 02
- 4E9 MDR211 04
- 4E9 MDR221 06
- 4E9 MDR231 10
- 4C9 MDR241 12
- 4C9 MDR251 14
- 01, 15
- 03 CD200 K9, 4E4, 5A6
- 05 CD210 K9, 4E4, 5A6
- 07 CD220 K6, 4D4, 5A5
- 09 CD230 K6, 4D4, 5A5
- 11 CD240 K6, 4C4, 5A4
- 13 CD250 K6, 4C4, 5A4

06W 19-134 HEX BUFF/INV
- H1 CD280
- H2 CD290
- H2 CD300
- H2 CD310
- 4N9 MDR001 12
- 4N9 MDR011 14
- 01, 15
- 03 MDX121 4H6, 6H6
- 05 MDX131 4H7, 6H6
- 07 MDX141 4H6, 6H6
- 09 MDX151 4H6, 6J6
- 11 CD000 4N4,
- 13 CD010 4N4,
- CD010 (227-0)
- CD000 (127-0)

D4 CDXNO

08W 19-134 HEX BUFF/INV.
- 4H9 MDR141 02
- 4H9 MDR151 04
- 4G9 MDR161 06
- 4G9 MDR171 10
- 4F9 MDR181 12
- 4F9 MDR191 14
- 01, 15
- CD140 (135-0)
- CD150 (235-0)
- 03 CD140 4H4
- 05 CD150 4H4
- 07 CD160 K8, 4F4, 5A8, 10D3
- 09 CD170 K8, 16G, 4G4, 5A8, 10D2
- 11 CD180 K8, 4F4, 5A7
- 13 CD190 K8, 4F4, 5A7

07T 19-134 HEX BUFF/INV.
- H4 CD220 02
- H4 CD230 04
- H4 CD240 06
- H5 CD250 10
- H1 CD260 12
- H1 CD270 14
- 01, 15
- 03 MDX061 4L6, A8, 6E6
- 05 MDX071 4L6, A8, 6E6
- 07 MDX081 4J6, 6G6
- 09 MDX091 4J7, 6G6
- 11 MDX101 4J6, 6G6
- 13 MDX111 4J6, 6G6

08T 19-134 HEX BUFF/INV
- 4K9 MDR081 02
- 4K9 MDR091 04
- 4K9 MDR101 06
- 4K9 MDR111 10
- 4H9 MDR121 12
- 4H9 MDR131 14
- 01, 15
- CD100 (133-0)
- CD090 (232-0)
- CD080 (132-0)
- 03 CD080 4K4
- 05 CD090 4K4
- 07 CD100 4J4
- 09 CD110 4J4
- 11 CD120 4H4
- 13 CD130 4H4
- CD130 (234-0)
- CD120 (134-0)
- CD110 (233-0)

06T 19-134 HEX BUFF/INV.
- H6 CD160 02
- H6 CD170 04
- H6 CD180 06
- H7 CD190 10
- H3 CD200 12
- H4 CD210 14
- 01, 15
- 03 MDX001 4M7
- 05 MDX011 4M6
- 07 MDX021 4M6
- 09 MDX031 4M6
- 11 MDX041 4L6, A9, 6E6
- 13 MDX051 4L7, A8, 6E6

115 19-131 SDF: N6 MDX071 04 → D 1 → 02 NC; N6 MDX061 05 → D 0 → 03 5X310 (108-5); MDX051 12 → D 1 → 07 NC; MDX041 13 → 0 → 06 5X300 (208-5); 10 NC; 11 5X290 (107-5); 15 NC; 14 5X280 (207-5); 4N1 LDH0 09 → CLK; 4A6 MARPU1 01 → CLR

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 CPA
TASK NO. 03088
DWG NO. 35-536R02D08
SHEET OF 11 - 13

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
EXTENSIVE CHANGES TO REV.15, FOR REV.14 AND PREVIOUS REV'S SEE VOID COPY IN FILES				
GP	JV	3242	12-27-77	R15
AREA B3, 15F-09 WAS SPEC'D AS MNEMONIC "CKIB", SHT. LOC. 4H3				
WTA	WS	3551	5-23-78	R16
AREA G3, 14E-3Q34 WAS REPOSITIONED FROM 0946				
GP	JV	3801	M 10-31-78	R17
AREA J8: 19-060, PIN 13 WAS 10N3.				
MR	JV	3832	M 1-22-78	R18
AREA A4 LOCATOR FOR SPCLI WAS R4.				
KR	JT	4231	R 3-7-80	R19

ISTBO 1K5, 7L2

STBO 4A3

SPCLI A4

SPROTO 6A1

P1BONO A4

P2ONI A4

P0BONI

GT1 6M2

GTO 6M2

C3X0 6A5, 9A1, 7A1

C3X1 6M2, 8L8

52B1A 13F1, 13A1, 13F4, 13L4

52B0

BMXNB1 13K7, 13E7, 13E1, 13J1, 13R1, 13D4, 13J4, 13R4

BMXSLB1 13D4, 13L7, 13F7, 13A7, 13J4

BMXNC1 13E4, 13L4, 13M7, 13B7, 13G7

BMXNA1 13B1, 13G1, 13L1, 13B4, 13G4, 13M4, 13D7, 13J7

BMXSLA1 13C1, 13M1, 13G5

DLCK0 1H1, 1K6

BIT16A 13D1, 13H1

BIT16B 13N1, 13C4, 13H4

RGENO H6

NOTES

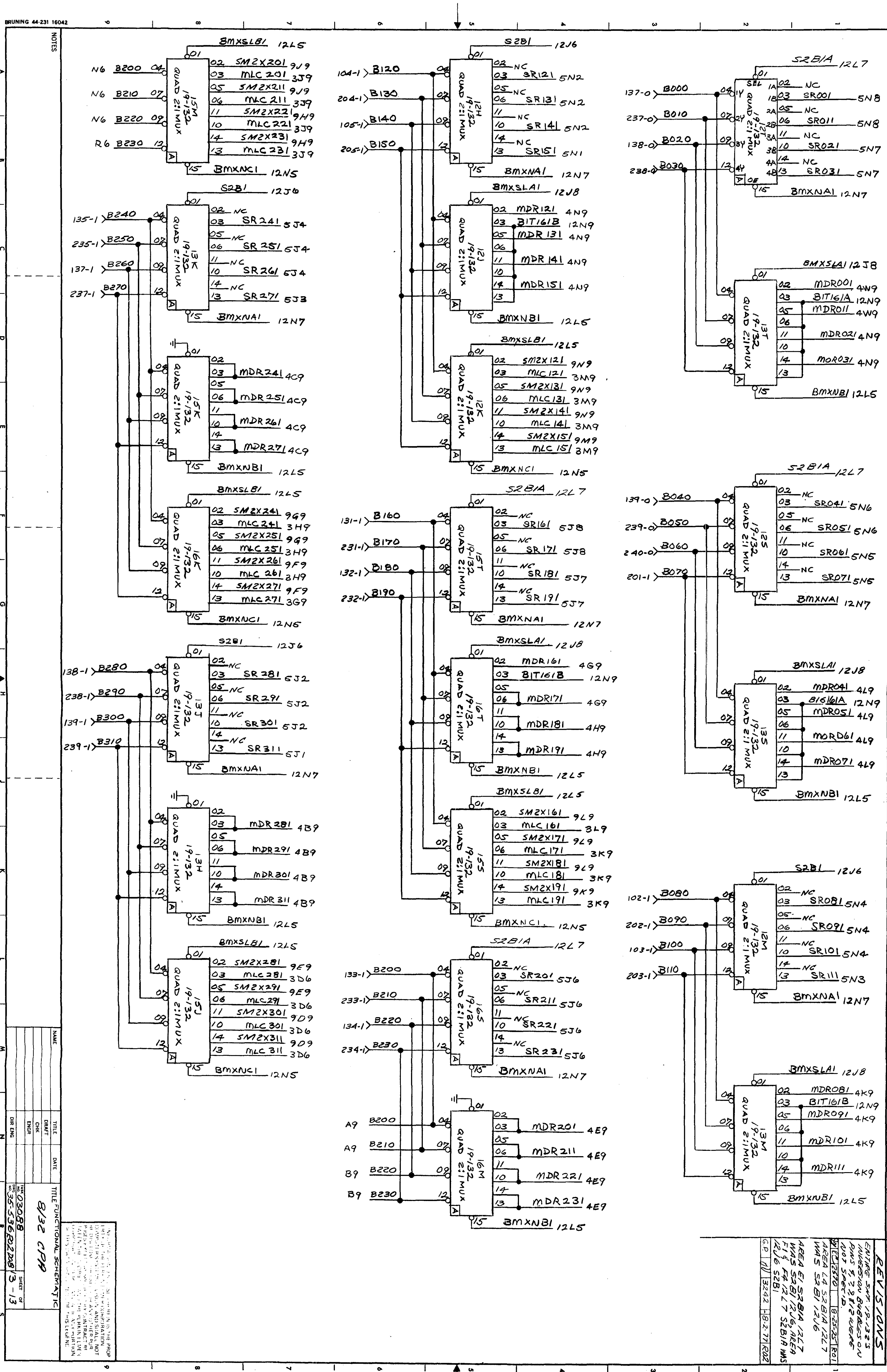
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC 8/32 CPA

TASK NO. 03088 ENG NO. 35-536R/9 D05

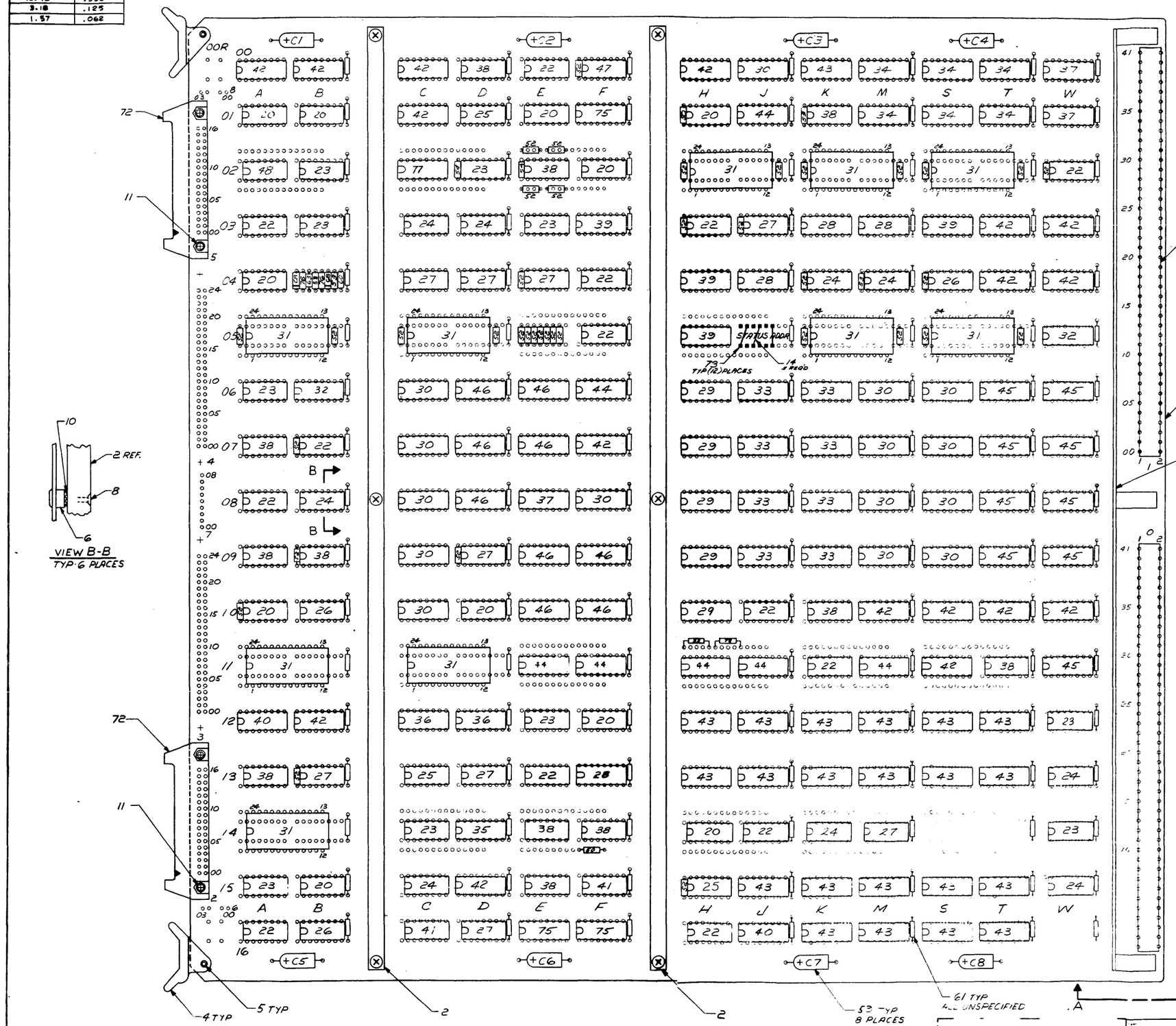
SHEET OF 12 - 13

BRUNING 44-231 16042



BRUNING 44-231 16042
NOTES
15M 19-132 QUAD 2:1 MUX
N6 B200 04, N6 B210 07, N6 B220 09, R6 B230 12
BMXSLB1 12L5
02 SM2X201 9J9
03 MLC201 3J9
05 SM2X211 9J9
06 MLC211 3J9
11 SM2X221 9H9
10 MLC221 3J9
14 SM2X231 9H9
13 MLC231 3J9
15 BMXNC1 12N5
12H 19-132 QUAD 2:1 MUX
104-1 B120, 204-1 B130, 105-1 B140, 205-1 B150
S2B1 12J6
02 NC
03 SR121 5N2
05 NC
06 SR131 5N2
11 NC
10 SR141 5N2
14 NC
13 SR151 5N1
15 BMXNA1 12N7
12T 19-132 QUAD 2:1 MUX
137-0 B000, 237-0 B010, 138-0 B020, 238-0 B030
S2B1A 12L7
02 NC
03 SR001 5N8
05 NC
06 SR011 5N8
11 NC
10 SR021 5N7
14 NC
13 SR031 5N7
15 BMXNA1 12N7
13K 19-132 QUAD 2:1 MUX
135-1 B240, 235-1 B250, 137-1 B260, 237-1 B270
S2B1 12J6
02 NC
03 SR241 5J4
05 NC
06 SR251 5J4
11 NC
10 SR261 5J4
14 NC
13 SR271 5J3
15 BMXNA1 12N7
12J 19-132 QUAD 2:1 MUX
BMXSLA1 12J8
02 MDR121 4N9
03 BIT161B 12N9
05 MDR131 4N9
11 MDR141 4N9
14 MDR151 4N9
15 BMXNB1 12L5
13T 19-132 QUAD 2:1 MUX
BMXSLA1 12J8
02 MDR001 4W9
03 BIT161A 12N9
05 MDR011 4W9
11 MDR021 4N9
14 MOR031 4N9
15 BMXNB1 12L5
15K 19-132 QUAD 2:1 MUX
03 MDR241 4C9
06 MDR251 4C9
10 MDR261 4C9
13 MDR271 4C9
15 BMXNB1 12L5
12K 19-132 QUAD 2:1 MUX
BMXSLB1 12L5
02 SM2X121 9N9
03 MLC121 3M9
05 SM2X131 9N9
06 MLC131 3M9
11 SM2X141 9N9
10 MLC141 3M9
14 SM2X151 9M9
13 MLC151 3M9
15 BMXNC1 12N5
16K 19-132 QUAD 2:1 MUX
BMXSLB1 12L5
02 SM2X241 9G9
03 MLC241 3H9
05 SM2X251 9G9
06 MLC251 3H9
11 SM2X261 9F9
10 MLC261 3H9
14 SM2X271 9F9
13 MLC271 3G9
15 BMXNC1 12N5
15T 19-132 QUAD 2:1 MUX
131-1 B160, 231-1 B170, 132-1 B180, 232-1 B190
S2B1A 12L7
02 NC
03 SR161 5J8
05 NC
06 SR171 5J8
11 NC
10 SR181 5J7
14 NC
13 SR191 5J7
15 BMXNA1 12N7
12S 19-132 QUAD 2:1 MUX
139-0 B040, 239-0 B050, 240-0 B060, 201-1 B070
S2B1A 12L7
02 NC
03 SR041 5N6
05 NC
06 SR051 5N6
11 NC
10 SR061 5N5
14 NC
13 SR071 5N5
15 BMXNA1 12N7
13J 19-132 QUAD 2:1 MUX
138-1 B280, 238-1 B290, 139-1 B300, 239-1 B310
S2B1 12J6
02 NC
03 SR281 5J2
05 NC
06 SR291 5J2
11 NC
10 SR301 5J2
14 NC
13 SR311 5J1
15 BMXNA1 12N7
16T 19-132 QUAD 2:1 MUX
BMXSLA1 12J8
02 MDR161 4G9
03 BIT161B 12N9
06 MDR171 4G9
10 MDR181 4H9
13 MDR191 4H9
15 BMXNB1 12L5
13S 19-132 QUAD 2:1 MUX
BMXSLA1 12J8
02 MDR041 4L9
03 BIT161A 12N9
05 MDR051 4L9
11 MORD61 4L9
14 MDR071 4L9
15 BMXNB1 12L5
13H 19-132 QUAD 2:1 MUX
03 MDR281 4B9
06 MDR291 4B9
10 MDR301 4B9
13 MDR311 4B9
15 BMXNB1 12L5
15S 19-132 QUAD 2:1 MUX
BMXSLB1 12L5
02 SM2X161 9L9
03 MLC161 3L9
05 SM2X171 9L9
06 MLC171 3K9
11 SM2X181 9L9
10 MLC181 3K9
14 SM2X191 9K9
13 MLC191 3K9
15 BMXNC1 12N5
12M 19-132 QUAD 2:1 MUX
102-1 B080, 202-1 B090, 103-1 B100, 203-1 B110
S2B1 12J6
02 NC
03 SR081 5N4
05 NC
06 SR091 5N4
11 NC
10 SR101 5N4
14 NC
13 SR111 5N3
15 BMXNA1 12N7
15J 19-132 QUAD 2:1 MUX
BMXSLB1 12L5
02 SM2X281 9E9
03 MLC281 3D6
05 SM2X291 9E9
06 MLC291 3D6
11 SM2X301 9D9
10 MLC301 3D6
14 SM2X311 9D9
13 MLC311 3D6
15 BMXNC1 12N5
16S 19-132 QUAD 2:1 MUX
133-1 B200, 233-1 B210, 134-1 B220, 234-1 B230
S2B1A 12L7
02 NC
03 SR201 5J6
05 NC
06 SR211 5J6
11 NC
10 SR221 5J6
14 NC
13 SR231 5J6
15 BMXNA1 12N7
13M 19-132 QUAD 2:1 MUX
BMXSLA1 12J8
02 MDR081 4K9
03 BIT161B 12N9
05 MDR091 4K9
11 MDR101 4K9
14 MDR111 4K9
15 BMXNB1 12L5
16M 19-132 QUAD 2:1 MUX
A9 B200, A9 B210, B9 B220, B9 B230
03 MDR201 4E9
06 MDR211 4E9
10 MDR221 4E9
13 MDR231 4E9
15 BMXNB1 12L5
PERKIN ELMER
REVISIONS
ENTIRE SHT 19-132S INVERSION BUBBLES ON PINS 5,7,9 & 12 WERE NOT SPEC'D. | 2570 | 8-25-75 | R01
AREA L4 S2B1A 12L7 WAS S2B1 12J6
AREA E1 S2B1A 12L7 WAS S2B1 12J6, AREA F1 & F4 12L7 S2B1A WAS 12J6 S2B1 | G.P. | 3242 | 8-2-77 | R02
NAME TITLE DRAFT CHK ENGR DIR ENG DATE
TITLE FUNCTIONAL SCHEMATIC
8/32 CPU
TASK NO. 03088
DWG NO. 35-536 R02 D08
SHEET 13 OF 13

MILLIMETER	INCH
13.46	.530
3.18	.125
1.57	.062



REVISIONS

THIS PRODUCTION RELEASE APPROVAL			

CHANGE 22-007 FOR IN USE TO 22-007 REV. 22-007 ADD IN USE TO 23-007 REV. OBSOLETE 30-013 FOR, 23-004 REF-007 FOR IN USE CHANGE: 30-011 IN DOC, 2-JAN ITEM IN USE ADD, 19-15 IN WR, NO 9.055 IN DWG / AN AND 19-057 IN AA

1		2330	6-6-75	

CHANGED: ITEM WAS ITEM 23, ITEM 661 6.5 @ LOC 48 WERE REVERSED.
ADDED: ITEM 22 @ 1/E, ITEMS 23 @ 2B, 1NH 2B @ 1BF, ITEM 38 @ 1AF.
DELETED: 1/E, 2B & 1BF.

	0007-01		9-24-75	

DELETED: 1 ITEM 661 1 ITEM 63.

	0008-01		10-7-75	

CHANGED: PAR WAS WAS ITEM 21.

	0009-01		2-3-76	

ADDED: 2 HOLES IN PAD 2SV, ITEM 18.

	0010-01		2-25-76	

AND REF. TO OTHER

			4-21-76	

ADDED ITEM 47 TO LOCATION

			4-28-76	

CHANGED ITEM 21 AT 2B ADD ITEM 77

	2509		4-30-76	

RELEASED FOR PRODUCTION

ADDED ITEM 80 TO CAB

	2507		5-28-76	

ADDED ITEM 23 TO 1BW

	2508		5-28-76	

CAB WAS ITEM 82

	2579		12-31-76	

ADDED ITEM 83 TO 2BB

	2620		1-28-77	

ADDED ITEMS 84 TO AREA 1H, LOC 16C ITEM SPEC'D WAS 23, LOC 15H ITEM SPECD WAS 41.

	2692		12-28-77	

MOVED ITEM 32 FROM LOC 2E AT LOC 1/E, 2.0 DIA ITEM

	2693		1-26-78	

LOCATION OF: ITEM 73 NOT SPEC'D

	2702		2-2-78	

CHANGED: ITEM 32, FROM AREA 1E TO AREA 2B, DELETED: ITEM 26, AREA 1/F DELETED: ITEM 29, AREA 1BE

	3012		1-19-77	

ADDED:
ITEM 24 TO AREA 1BK
ITEM 27 TO AREA 1BM
ITEM 53 TO AREA 2BK
AND 2BM

	3045		4-4-78	

CHANGED TO METRIC 5-4-78, GM.

REVISIONS CONT
ADDED ITEM 28 TO AREA 1/F.

	3350		10-13-78	

ITEM 3/F WAS 2B ITEM 38, AREA 2/F ADDED ITEM 50.

	3520		10-13-78	

COMPONENT	REF DESIGNATION

N. LIMPERT			
G. MINETELLI			
R. MANNES			
E. NIEDECK			
S. MESSER			

TITLE: ASSEMBLY PRINTED CIRCUIT MOD 8/32 CPR

	03088	
	-35-536 REV G	1-1

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

P5 16 — 03B 1K

33-032 05A: 01 NO, 02 NC, 04, 03, 12, 11, 09, 10 — 15 MB151, 14 MB141, 06 MB131, 07 MB121

06A 19-117 4 BIT MAG. COMP. (A)
- NC 02, A>B 03, A=B 04, A<B 10, A0 09, B0 12, A1 11, B1 13, A2 14, B2 15, A3 01, B3
- A>B 07 NC, A=B 06, A<B 05 NC
- 2B7 XRP1A
- 8N3 CSA151, 8N4 CSA141, 8N5 CSA131, 8N6 CSA121

07B 19-115 SA: 01/02 → 03 JB121 9E6; 04/05 → 06 JB131 9E7; 09/10 → 08 JB141 9E7; 12/13 → 11 JB151 9E7

33-032 04A: 01 NO, 02 NC, 04, 03, 12, 11, 09, 10 — 15 MB111, 14 MB101, 06 MB091, 07 MB081

08B 19-115 SA: 01/02 → 03 JB081 9E4; 04/05 → 06 JB091 9E4; 09/10 → 08 JB101 9E5; 12/13 → 11 JB111 9E5

07A 19-117 4 BIT MAG. COMP. (A)
- NC 02, 03, NC 04, 10, 09, 12, 11, 13, 14, 15, 01
- 07 NC, 06, 05 NC
- 8N7 CSA111, 8N9 CSA101, 9N6 CSA091, 9N8 CSA081

09B 19-115 SA: 01/02 → 03 JB041 9E2; 04/05 → 06 JB051 9E2; 09/10 → 08 JB061 9E2; 12/13 → 11 JB071 9E3

33-032 03A: 01 NO, 02 NC, 04, 03, 12, 11, 09, 10 — 15 MB071, 14 MB061, 06 MB051, 07 MB041

08A 19-117 4 BIT MAG. COMP. (A)
- NC 02, 03, NC 04, 10, 09, 12, 11, 13, 14, 15, 01
- 07 NC, 06, 05 NC
- 9N4 CSA071, 9N5 CSA061, 9N2 CSA051, 9N3 CSA041

03B 19-016 HG: 12/13 → 11 CNT1 9H8

JAM1

MNCLK1 09 — 03B 19-016 HG — 08 SETRLCO 14A3

13N3 CLK1B, 14M6 CS000 — 11C 19-058 SG: 05/04/03 → 06 XMTCH1

02B 19-015 HG: 01 ← SETRLCO; 02 SYNC (7P) → 101-7

02B 19-015 HG: 03 ← MTCH1; 04 → 12 01B 220 05 → 41 MTCH → P5 101-8 / 100-8 33-027

01A 33-032: 14 NC, 03, 15, 04 NO, 02, 01 NC — P5 12 02A 1K → 02A P5 14 2B7 XRP1A

00B 19-115 SA: 02/01 → 03; 04 02A P5 13; 05/04 → 06 FMTCH1

03B 19-016 HG: P5 16 02A 1K → SINO; 05/04 → 06

33-034 00R S1: 02 NO, NO 03 SINO; 01 NC, NS 04 SINC

03B 19-016 HG: P5 15 02A 1K → 02; 02/01 → 03 MNCLKO

13N4 CLK0, 14A4 SCLR0A — 00B 19-115 SA: 09/10 → 08

05 MTCH1 → 068 19-063 J-K FF (05 Q, 01 J, 02 K, 06 QC, 15): 04 Q → 05; 03 Q̄ → 06 NC; 01 QC

068 19-063 D FF (05 D, 02 Q, 06 Q̄, 01 DC): 03 D ← 06 NC; 04 Q → 05; 01 DC

068 19-063 D FF (05 D, 10 Q, 08 Q̄, 13 DC): 12 D ← 09 RUN1 NC; 11 Q̄ → 08 RUN0; 10 Q → 09 RUN1 NC; 13 DC

05, 04 → 048 19-126 SG: 06 KLCLK0 13H2

02, 03 →

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BEAT LEAST THE FOLLOWING REVISION LEVEL

8/32 CPB	35-537F00R22
8/32C CPB	35-537F01R07

USED IN MANUAL 29-394

REVISIONS

PRE PRODUCTION APPROVAL	INIT.	DATE
	DEV JSA	11/5/74
	PROD [illegible]	11/6/74

CHANGED: 06B04 WAS XRP1A; 06B02 WAS CONN TO 00B03; 06B02 WAS CONN TO 03B06; 06B01 WAS CONN TO 08B8.
REMOVED: 'JAM' LED & 'SNGL' LED & 220Ω RES @ 01B PINS 10 & 11; 2 GATES @ 02B OUTPUTS 08 & 06.
ADDED: GATE @ 03B OUTPUT 11 (CNT1).
CHANGED: ALL SHEETS EXCEPT 4 & 7 FROM R00 TO R01 REV.

GH/HH	03088-30	VB	1-21-75	R01
CHANGED: SHEETS 8 & 10 WERE R01. 09				
GH/HH	03088-30	VB	1-24-75	R02
CHANGED: REV OF SHTS 12 & 13 WERE R01.				
GH/HH	03088-24	VB	2-26-75	R03
CHANGED: REV OF SHT 14 WAS R01, SHT 12 WAS R02				
GH/HH	03088-57	VB	4-8-75	R04
REV LEV OF SHT 11 WAS R01				
GH/HH FJS	03088-20	VB	4-24-75	R05
REV LEV OF SHT 12 WAS R03				
GH/HH	03088-71	VB	4-28-75	R06

RELEASED [illegible] DATE 5/27/75

REV LEV OF SHT 1 WAS R06
" " " " 2 WAS R01
" " " " 3 WAS R01
REV LEV IN S9 WAS R06

GH/HH	2521	—	5-28-75	R07
REVISED SHT 13. 8/32 CPB, 35-537 WAS R10				
PE/HH	2576	—	7-18-75	R08
REVISED SHTS 2, 3, 12 & 13.				
JC/KC	2570	—	8-25-75	R09
REVISED SHTS 1, 9, 10 & 12 ADDED VAR FOI TO PCB TABLE				
JC/HH	2857		5-17-76	R10
REVISED SHTS 1, 13 & 14. 35-537 WAS R16, 35-537 FOI WAS R00.				
WS/HH	3151	—	5-11-77	R11
REVISED SHT'S 1 & 8. 35-537 WAS R19, 35-537 FOI WAS R04				
PM/HH	3471		2-1-78	R12
REVISED SHT. 14				
GS/HH	3531		5-22-78	R13
REVISED SHT. 12				
GS/HH	3694		5-22-78	R14
REVISED SHTS. 11 & 12. 35-537 R06 & FOI WERE R20 & R05.				
GP/HH	3800	M	11-1-78	R15
REVISED SHT 11				
CS	3792	A	4-3-79	R16

REVISIONS CONT'D IN AREA 9A.

SHEET INDEX																
SHT NO	1	2	3	4	5	6	7	8	9	10	11	12	13	14		
REV	17	3	3		1			3	3	3	4	8	5	5		

REVISED SHTS 1 & 9.

KP/KC	4231	R	3-7-80	R17

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	10-10-74
G.J. HOMEFIELD	CHK	11/5/74
D. ANKO	ENGR	
S. MESSINA	MGR	

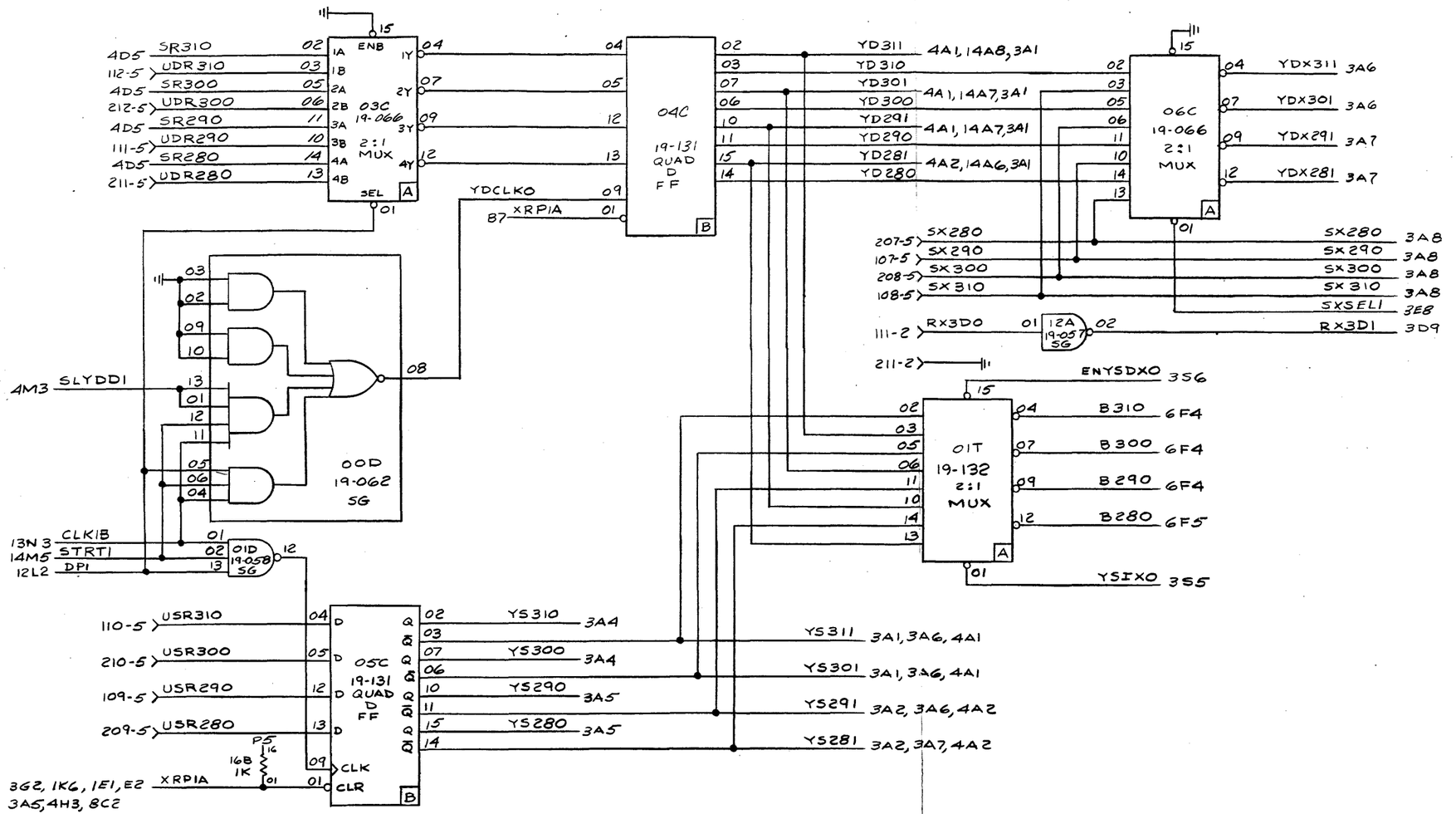
TITLE: FUNCTIONAL SCHEMATIC 8/32 CPB

DWG 03088 — SHEET 1 OF 14 — 35-537R11D08

BRUNING 44-231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISION			
CHANGED: 'DP1' LEAD @ 06C AS WAS 'DI'.			
G/H/KCD	03088-56	V1	4-21-75 R01
06C01 WENT TO 12A02 'SXSELI' WAS NOT SPEC			
GM WEN	2521	-	5-28-75 R02
AREA D2 & K2, 19-066-5 INVERSION BUBBLES ON PINS 9, 7, 2, 5, 12 WERE NOT SPEC'D. AREA K4, 19-132 INVERSION BUBBLES ON PINS 9, 7, 2, 5, 12 WERE NOT SPEC'D.			
GM KCD	2570	-	8-25-75 R03



P. EDWARDS
G. HOMEFIELD
S. MESSINA

10-12-74

FUNCTIONAL SCHEMATIC
8/32 CPB

03088
35-537 R03 D08 2 14

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

CHANGED: 19-0626 13F WAS 19-126 @ 14H.				
GM	DEN	03088-30	1-21-75	R01
ADDED GATE 12A TO LOC E6				
GM	DEN	2521	5-28-75	R02
AREA C1, C6, H2 & J6 19-0663; INVERSION BUBBLES ON PINS 4, 7, 9 & 12 WERE NOT SPECIFIED				
GM	DEN	2570	8-25-75	R03

NOTES

NAME	DATE	TITLE
E. ROE	10-11-74	FUNCTIONAL SCHEMATIC 8/32 CPB

03088-35-537R03D08 SHEET 3 OF 14

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

15C 19-066 2TO1 MUX
15B 19-065 2TO1 MUX
15A 19-071 HDFF
15T 19-066 2TO1 MUX
QUAD D FF 19-131
16B 19-063 SDFF
15W 19-063 SDFF
16W 19-063 SDFF
16T 19-124 SA
16A 19-059 SA
15J 19-060 SG
13J 19-055 SG
12A 19-057 SA
16S 19-057 SG
13S 19-058 SG
02K 19-059 SA
11M 19-059 SA
14S 19-062 SG
06W 19-134
06T 19-134
HEX BUFF/INV

YD311 YS311 YD301 YS301 YD291 YS291 YD281 YS281 2H1 2H5 2H1 2H6 2H1 2H6 2H2 2H6
R1R101 11C7
R1R100 R1R090 R1R080 R1R070 11C7 11C7 11C7 11C5
R1R090 R1R080 R1R071 R1R061 11C7 11C7 11C5 11C5
XS040 XS030 XS020 XS010
SSEL041 SSEL031 SSEL021 SSEL011 SSEL001
102-3 102-2 202-3 202-2 101-3 101-2 201-3 201-2 100-3 100-2
SLYDD1 2A3
SPSW1 G7, D6
XRP1A 2B7
CS001 14M6
CLK1A 13N4
SRCLK1 111-3
S280 S290 S300 S310 7M5 7M6 7M6 7M6
CLK1B 13N3
XRP1C 5A2, 11N3, 12M3
16W 1K P5
SR280 SR290 SR300 SR310
2B2 2B1 2B1 231
SPSW1 M3
CCCO 205-0
FLGCLK0 K9
VCCO 204-0
BCCO 203-0
LCCO 202-0
CFLG1 VFLG1 GFLG1 ZFLG1 LFLG1 14D5
XRP1C A5
CCCLK0 M7
SCLR0A 14A4
PSW281 PSW291 PSW301 PSW311 GPSWA0 14A6 14A7 14A7 14A8 3M3
A280 A290 A300 A310 114-1 214-1 115-1 215-1
SCCO 104-0
SPSW1 M3
SIRT1 14M5
CLK1A 13N4
ENFLG1 11R3
CCCLK0 G6
FLGCLK0 D6
PSWCLK1 5A2

NOTES

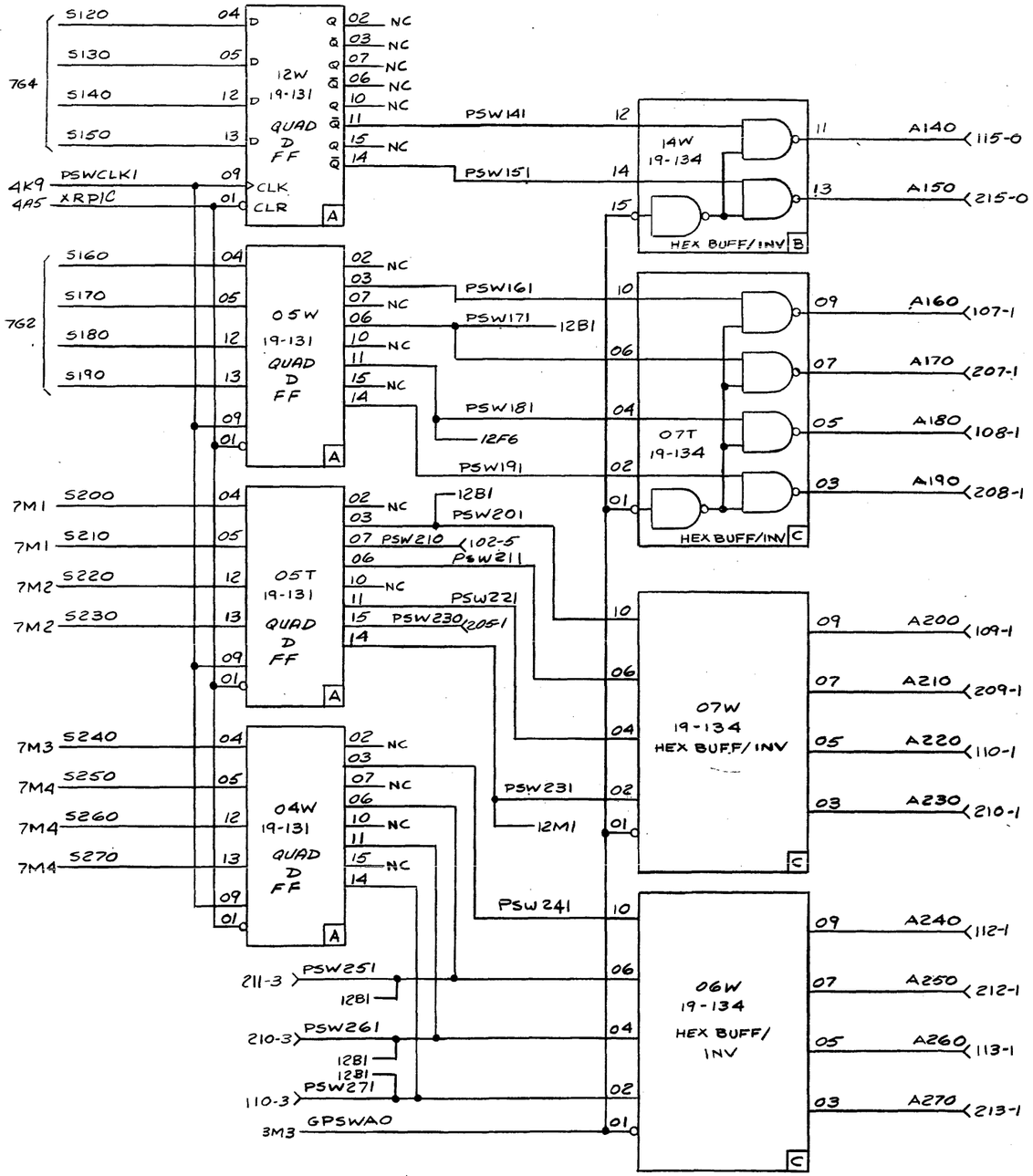
BRUNING 44-231 16042

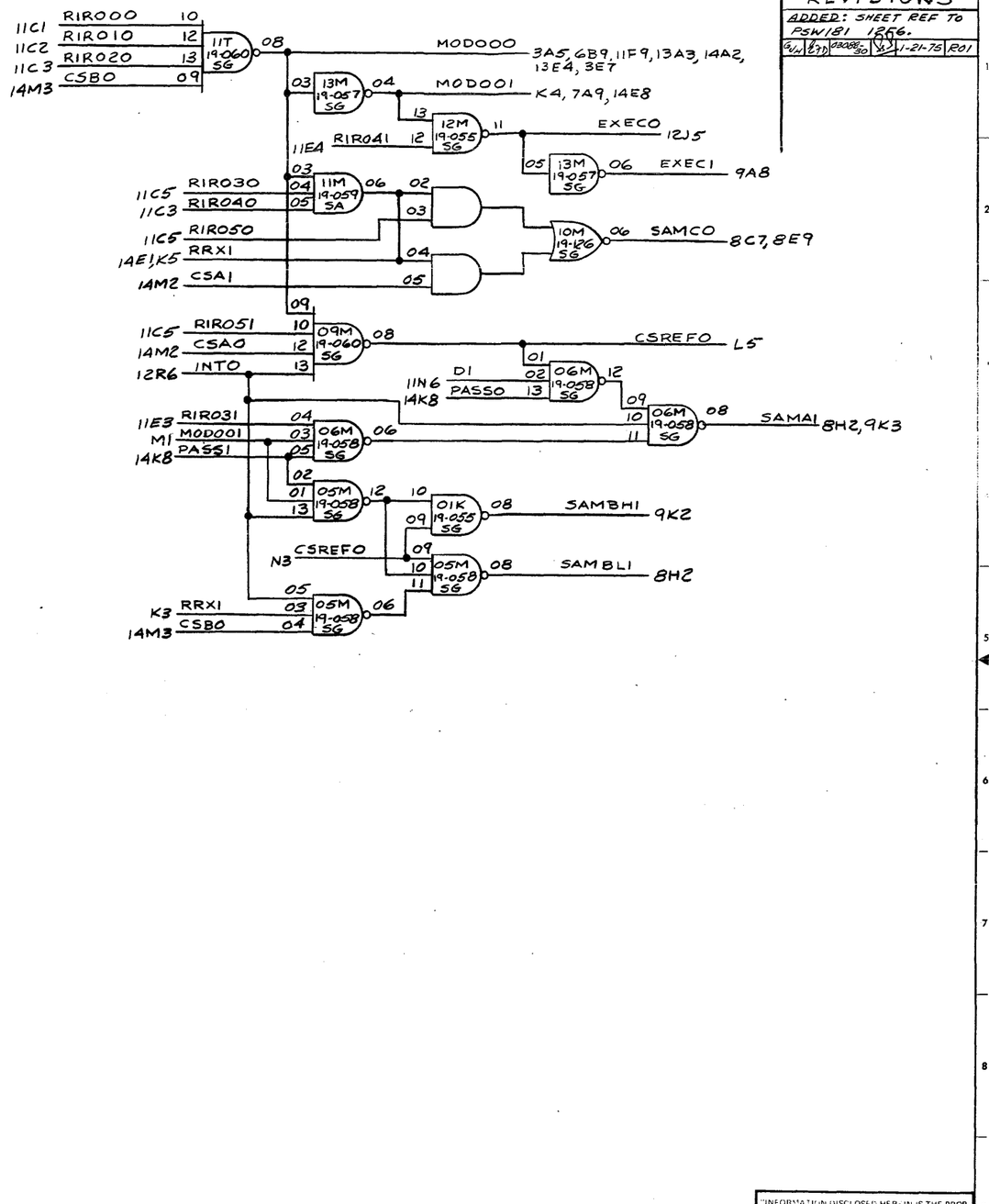
	NAME	DATE
DRAFT		
CHK		
ENGR		
DIR ENG		

TITLE FUNCT SCHEMATIC
M-8/32 CPB
DWG 03088
TAG 35-537 D08
SHEET 4 OF 14

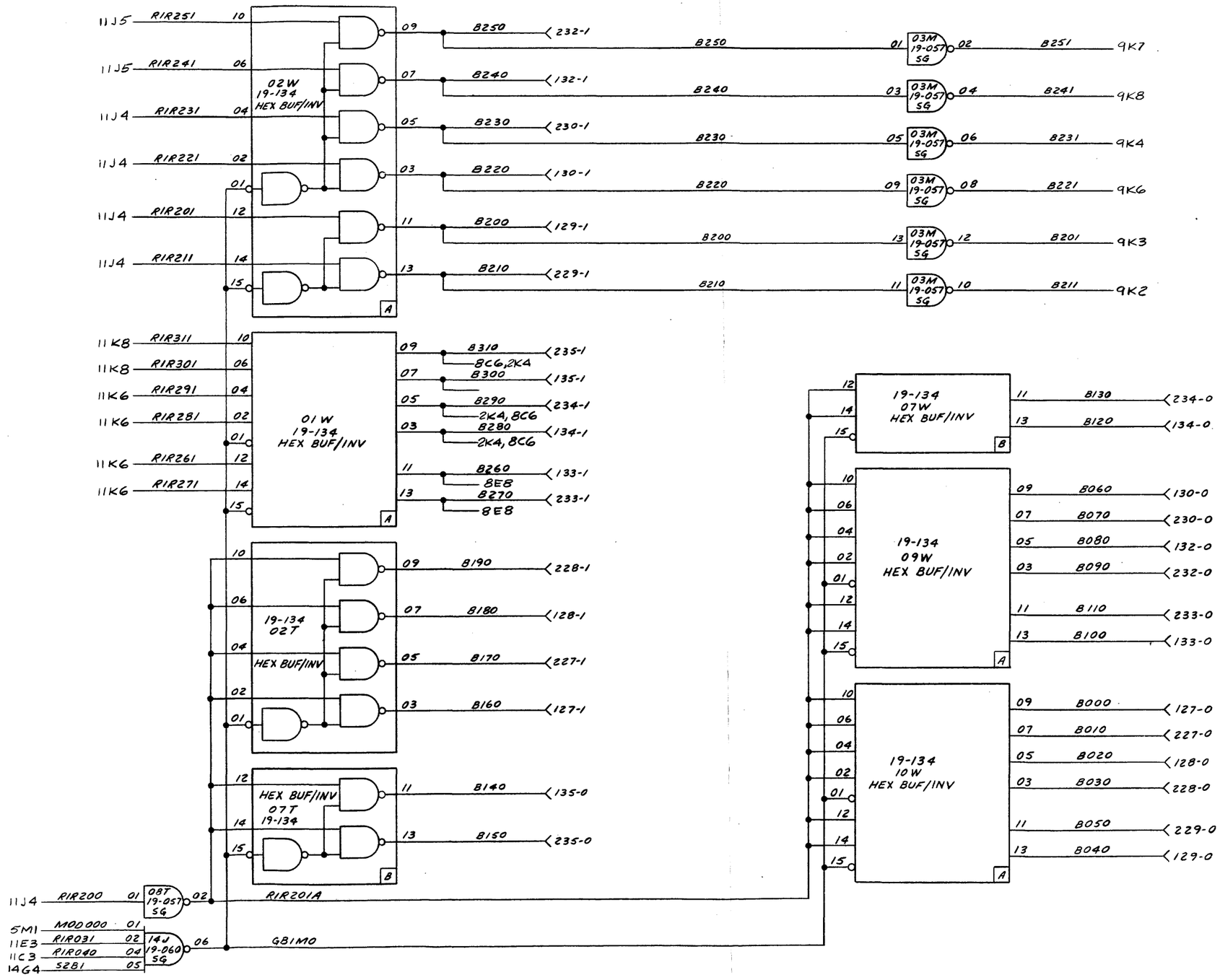
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
ADDED: SHEET REF TO PSW181 12F6.				
G.W.	8278	03088-30	1-21-75	R01





FUNCTIONAL SCHEMATIC
8/32 CPB
03088
35-537 R01 D08
5 14



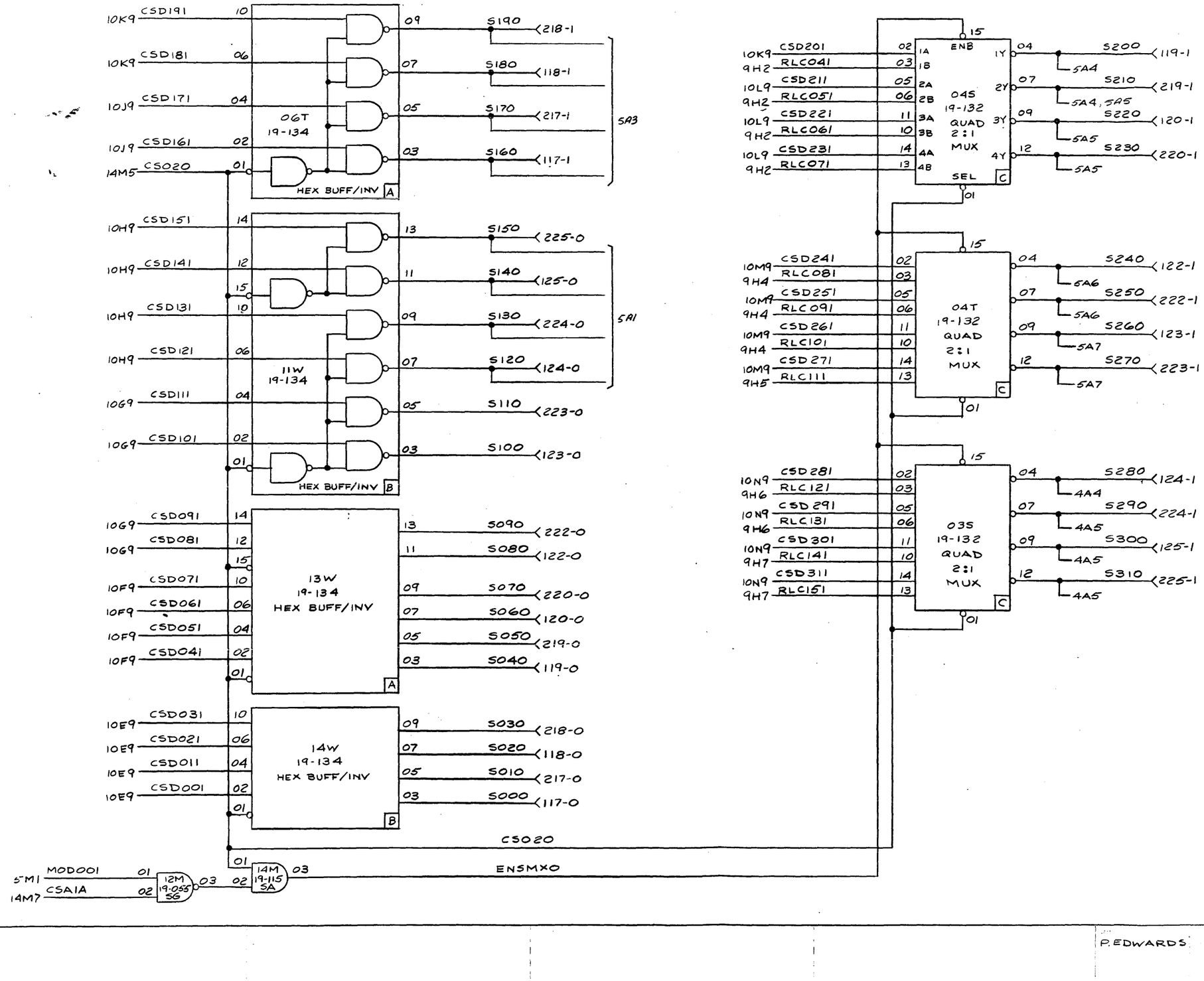
NOTES

DRAWN	J.R. BIELSKIE	DATE	10-11-74
TITLE	FUNCTIONAL SCHEMATIC 8/32 CPB		
	03088		
	35-5537 D08	SHEET	6-14

BRUNING 44-231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



NOTES:

P. EDWARDS

FUNCTIONAL SCHEMATIC
8/32 CPB
03088
35-537 D08 7 14

BRUNING 44 231 16042

REVISIONS				
CHANGED: SHEET REF ON TRAP130 WAS 12J4; TRAP120 WAS TRA120.				
C4	EJD	030285 SG	MS	1-21-75 R01
ADDED: 19-057@04D OUTPUTS ARE 'CSA100B' THRU 'CSA150B'.				
C4	EJD	030982 SG	MS	1-29-75 R02
AREA C4, 02C PINS 06, 10 AND 13 WERE NO CONN.				
PM	JW	3471		2-1-78 R03

12J4 TRAP150 → 01K 19-055 SG → 02E 19-059 SA

01C 19-066 2TO1 MUX
- 116-5 UIR310 (12J1) → 1A
- 12J4 TRAP140 → 1B
- 216-5 UIR300 (12J1) → 2A
- 12J4 TRAP130 → 2B
- 115-5 UIR290 (12J1) → 3A
- 12R5 TRAP120 → 3B
- 215-5 UIR280 (12J1) → 4A
- 2B7 XRP1A → 4B
- SEL ← 12R6 INT1
- 1Y → C1X141 → H3
- 2Y → C1X131 → H4
- 3Y → C1X121 → H5
- 4Y → C1X111 → H6

02C 19-066 2TO1 MUX
- 114-5 UIR270 (12J1) → 02
- 214-5 UIR260 (12J2) → 03
- 113-5 UIR250 (12J2) → 05
- 213-5 UIR240 (12J2) → 06
- SEL ← 12R6 INT1
- 04 → C1X101 → H8
- 07 → C1X091 → 9K6
- 09 → C1X081 → 9K8
- 12 → C1X071 → 9K4

01M 19-066 2TO1 MUX
- 11J7 RIR310 / 6F4 B310 → 02
- 11J7 RIR300 / 6F4 B300 → 05
- 11J7 RIR290 / 6F4 B290 → 11
- 11J7 RIR280 / 6F4 B280 → 14
- SEL ← 5N2 SAMC0
- 04 → C2X151 → H2
- 07 → C2X141 → H3
- 09 → C2X131 → H4
- 12 → C2X121 → H5

02M 19-066 2TO1 MUX
- 11J6 RIR270 / 6F5 B270 → 02
- 11J5 RIR260 / 6F5 B260 → 05
- NC → 11, 10, 14, 13
- SEL ← 5N2 SAMC0
- 04 → C1X101
- 07 → C2X101
- 09 → NC
- 12 → NC

1 02H
- 9H7 RLC151 → 06
- E5 C2X151 → 04
- 11J5 RIR251 → 03
- 5N4 SAMBL1 → STB1
- 5R4 SAMA1 → SELA
- STB2 ← 9H7 RLC141
- E2 C1X141 → 10
- E6 C2X141 → 11
- 11J5 RIR241 → 12, 13
- 07 → Y

2 19-116 4:1 MUX A
- 9H7 RLC141 → 10
- E2 C1X141 → 11
- E6 C2X141 → 12
- 11J5 RIR241 → 13
- 09 → Y

03H 19-116 4:1 MUX A
- 9H6 RLC131 → 06
- E2 C1X131 → 05
- E6 C2X131 → 04
- 11J4 RIR231 → 03
- SEL ← 5N4 SAMBL1, 5R4 SAMA1
- 9H6 RLC121 → 10
- E2 C1X121 → 11
- E6 C2X121 → 12
- 11J4 RIR221 → 13
- 07 → Y

02F 19-116 4:1 MUX A
- 9H5 RLC111 → 06
- E2 C1X111 → 05
- E6 C2X111 → 04
- 11J4 RIR211 → 03
- SEL ← 5N4 SAMBL1, 5R4 SAMA1
- 9H4 RLC101 → 10
- E3 C1X101 → 11
- E6 C2X101 → 12
- 11J4 RIR201 → 13
- 07 → Y

04D 19-057 SG
- 09 → 08 CSA150B → 10A9
- 11 → 10 CSA140B → 10A9
- 03 → 02 CSA130B → 10A9
- 07 → 06 CSA120B → 10A9
- 01 → 02 CSA100B → 10A9

04H 19-124 SG
- 01 → 03 CSA150 → 10B1
- 09 → 11 CSA120 → 10B1

09A 19-124 SG
- 01 → 03 CSA150A → 122-3
- 09 → 11 CSA120A → 222-3

04F 19-124 SG
- 01 → 03 CSA110 → 10B1
- 04 → 06 CSA100 → 10B2

10A 19-124 SG
- 01 → 03 CSA110A → 120-3
- 04 → 06 CSA100A → 220-3

CSA151 → 1E1
CSA141 → 1E2
CSA131 → 1E2
CSA121 → 1E2, 9B6
CSA111 → 1E4
CSA101 → 1E4, 9B4

NOTES:

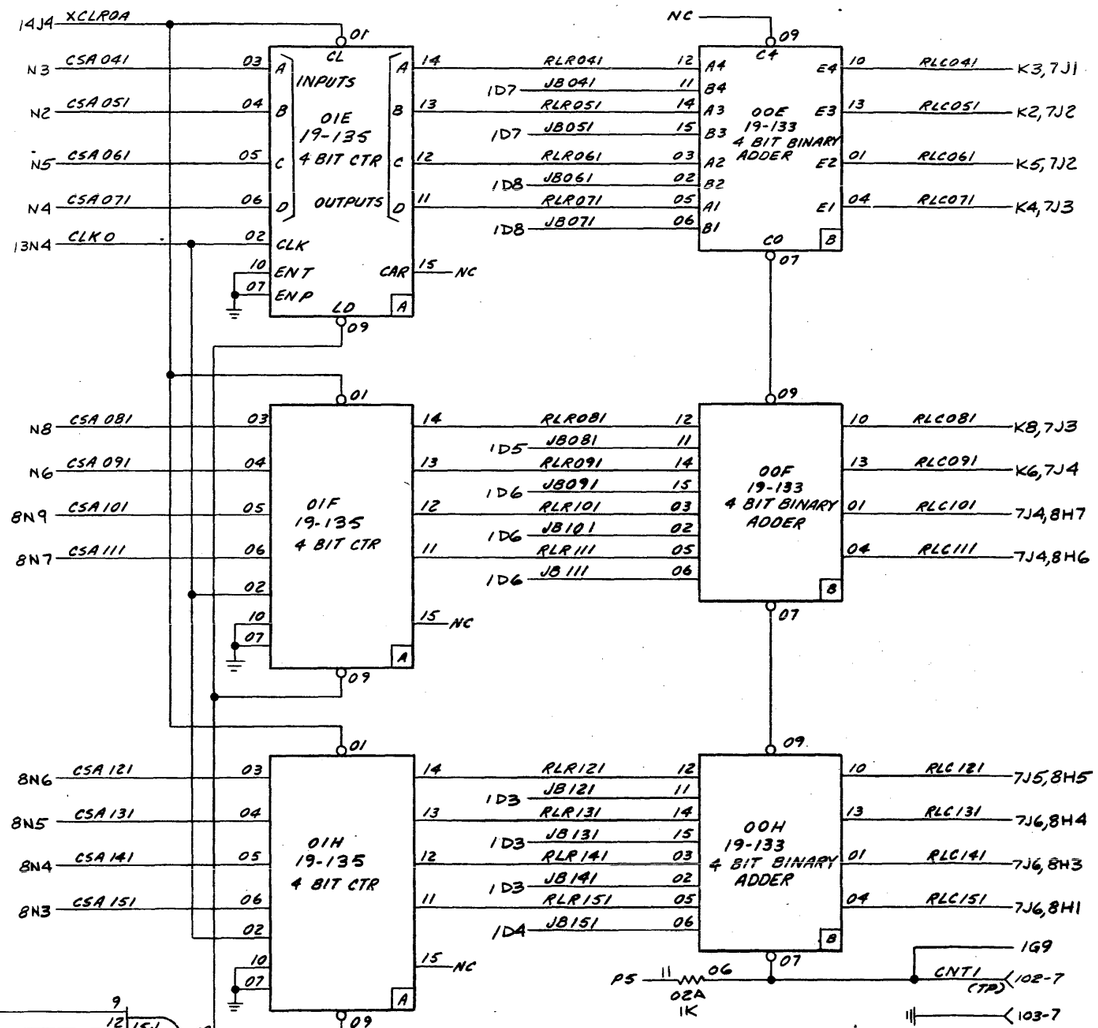
NAME	DATE
DRWN	
CHKD	
ENG	

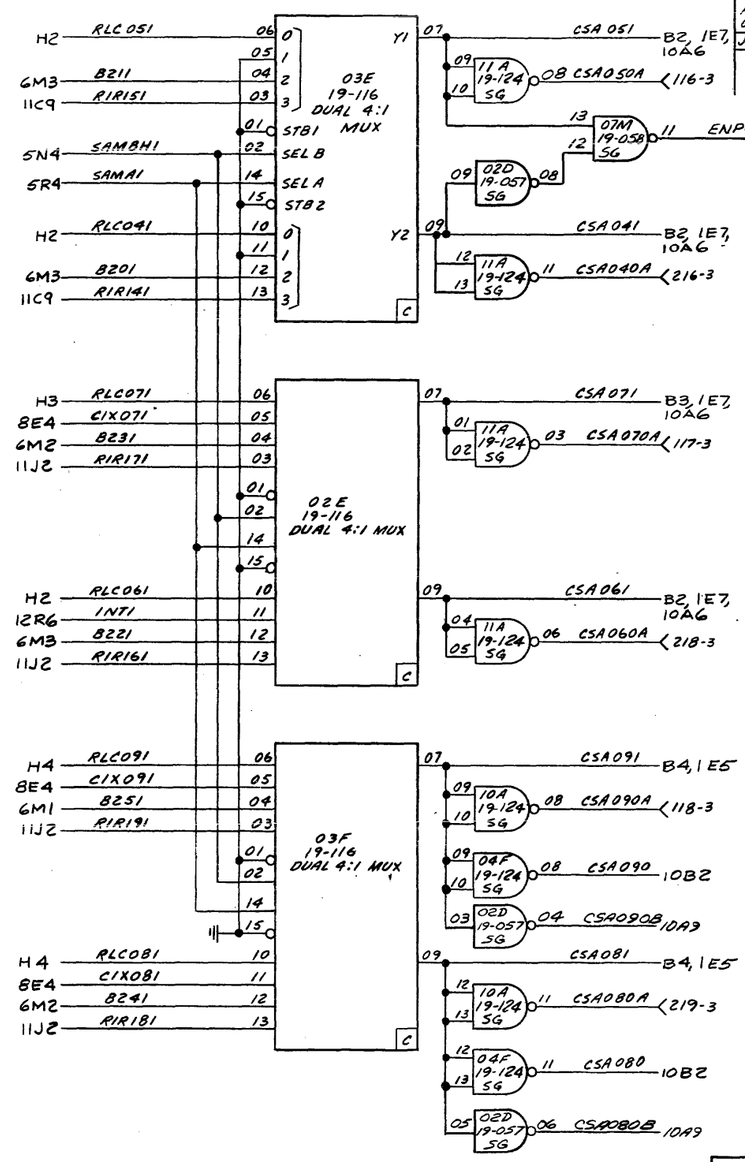
TITLE: FUNCT. SCHEMATIC M-8/32 CPB

03088 35-537 R03 D08 — SHEET 8 OF 14

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
CHANGED: CNT1 (TP) WAS ON PIN 10A-7; ADDED: SHEET REF TO CNT1 OF 1G9			
G/H	03088-30	1-21-76	R01
ADDED: GATE @ 02D-OUTPUT 'CSA090B', GATE @ 02D OUTPUT 'CSA080B'.			
J/H	A03088-40	1-23-76	R02
AREA N2, ADDED GATES 02D #07M, MNEM ENP450			
JC	J.S.P.	2857	5-17-76 R03





NOTES

NAME	TITLE	DATE	TITLE
J.R. BIELSKIE	DRAFT	10-11-74	FUNCTIONAL SCHEMATIC 8/32 CPB
	CHK		
	ENGR		
	SUP ENG		

03088 SHEET 9 OF 14

35-5-37R03D08

BRUNING 44-231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
ADDED: 'RDIS' MNEM. TO (TP) 103-6 & 4550Ω GND PIN 102-6.	6/14	1270	03088-30	V-21-75 R01
ADDED: 'CSA080B' THRU 'CSA150B' LEADS,	6/14	1270	03088-40	V-2975 R02
ADDED: F01 VARIATION TO ROM SYMBOLS (40) AND NOTE. CHANGED: 04E-11, 12J-13 #12J-14 WERE MNEM ENPG40. ADDED 12J-14 TO MNEM CSA071 ADDED 12J-13 TO MNEM ENP450	JC		2857	5-17-76 R03

8N2 CSA150
8N3 CSA140
8N4 CSA130
8N5 CSA120
8N6 CSA110
8N8 CSA100
9N7 CSA090
9N8 CSA080
9R2 ENP450

CSA071
ENP630
ENP620
ENP610
ENP600

RDIS (TP) 103-6
102-6

04F 16P5 1K

9N3 CSA041
9N2 CSA051
9N5 CSA061
9N4 CSA071

04E
19-129
3TO8 DECODER
G1 G2B G2A C B A SEL
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
07 N.C. 09 N.C. 10 N.C. 11 N.C. 12 13 14 15 ENPG00

9N9 CSA080B
9N7 CSA090B
8N9 CSA100B
8N7 CSA110B
8N9 CSA120B
8N5 CSA130B
8N3 CSA140B
8N1 CSA150B

12J	11J	10J	09J	08J	07J	06J	05J	HS ROM 1024-1279
12H	11H	10H	09H	08H	07H	06H	05H	HS ROM 768-1023
12F	11F	10F	09F	08F	07F	06F	05F	HS ROM 512-767
12E	11E	10E	09E	08E	07E	06E	05E	HS ROM 256-511
12D	11D	10D	09D	08D	07D	06D	05D	HS ROM 000-255

NOTES
*DENOTES ROM CHIPS USED ON 35-537F00
**DENOTES ROM CHIPS USED ON 35-537F01

NAME	TITLE	DATE
E. ROE	DRAFT	10-13-74
	CHK	
	ENGR	
	DIR ENG	

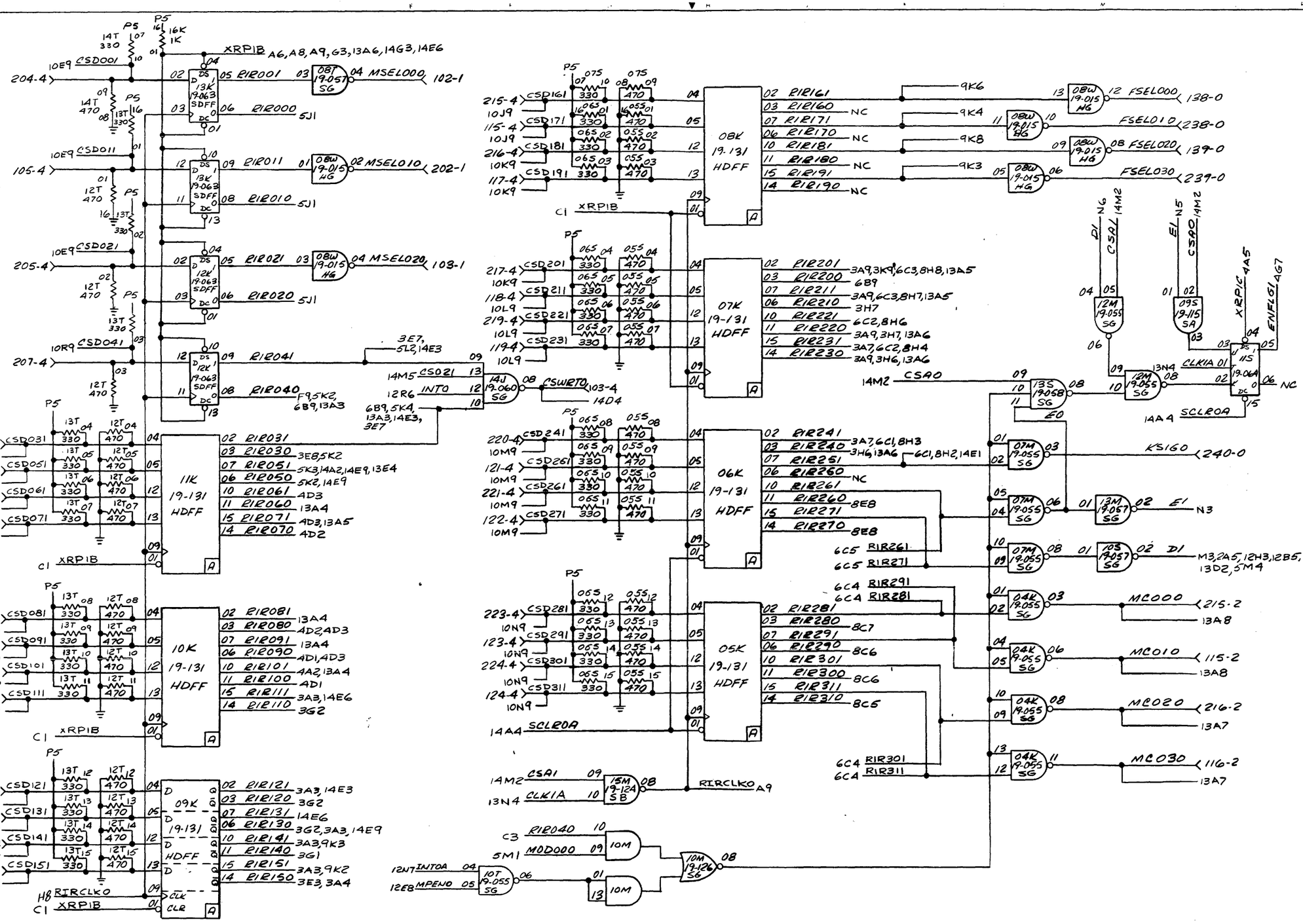
TITLE FUNCTIONAL SCHEMATIC 8/32 CPB
TASK NO. 03088
DWG NO. 35-537R03 D08
SHEET OF 10-14

BRUNING 44231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

ADDED: SHEET REF. TO CSWRTO-14D4; RIR041 & RIR031-3E7.				
CS	JW	03088-30	V3	11-21-75 R01
GATES 08W WERE 19-057				
CS	JW	03088	V3	12-24-75 R02
AREA F9 ADDED 19-055-09,05,06				
CP	JW	3800	M	11-1-78 R03
ALL 5S RESISTOR PACKS WERE 6S AND ALL 6S WERE 5S				
CS	JW	3792	R	4-4-79 R04



G. MELTON			FUNCT. SCHEMATIC M832 - CPB	
			03088	
			35-597 R04 008	11 14

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

CHANGED: PER MARKED PRINT IN ECR.				
GH	VH	03088-30	1-21-75	R01
ADDED: 19-059 @ SHT LOC L3, BD LOC 155.				
GH	GH	03088-54	3-26-75	R02
ADDED: 19-059 @ SHT LOC U8, BD LOC 155.				
GH	VH	03088-57	4-9-75	R03
EXTENSIVE CHANGES SEE ECR.				
SM	VH	03088-71	4-28-75	R04
AREA E2, K2, 13-0874'S INVERSION BUBBLES ON PINS 2, 10, 11, & 12 WERE NOT SHOWN				
SM	TC	2570	8-26-75	R05
AREA G1: ADDED 03D AND 00D TO 00C-19. 00C-14 WAS GROUND. ADDED VAR F01 TO 00C. AREA D1, 01S WAS 19-084 F77. AREA K1, 00C (19-142) WAS 19-084F76 ADDED VARIATION NOTE				
JC	VH	P. 2857	5-17-76	R06
AREA A9 & K2 NOTE 1 WAS NOT SPEC'D				
GS	VH	3694	5-22-78	R07
AREA N7, 19-057 05, 06 WAS ADDED. AREA N6 LOCATOR 13A2 WAS DELETED FROM 19-055-11, . AREA N6 LOCATOR 11E9 WAS DELETED FROM INTI. AREA E8 LOCATOR 11F9 WAS DELETED FROM INTENO.				
GP	VH	3800 M	11-1-78	R08

NOTES -
* DENOTES COMPONENTS USED ON 35-537F00
** DENOTES COMPONENTS USED ON 35-537F01

NOTE 1: WCS OPTION M8/32 USES 19-142 F64 IN LOC. 00C (SEE 02-440). M8/32 (CORD) USES 19-195 F14 IN LOC. 00C (SEE 02-540).

DRAWN: G. MELTON

TITLE: FUNCT. SCHEMATIC M-8/32 CPB

03-088
35-537 R08D08

12-19

DRAWING 44 231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

ADDED: DIODE @ 12B PINS 03 & 14, GATE @ LOC C3 IN LINE FROM 15F06 TO 14F12, GATE @ SMT LOC F5 TO PIN 13 ON 16D.
CHANGED: 15F01 WAS INTO, 15H04 WAS RIR230, 15H05 WAS RIR240.
G/A | [illegible] | 03088-30 | VB | 11-21-75 | R01

CHANGED: CAP. @ 12B WAS 220PF, 15E16 WAS CONNECTED TO 15D13.
ADDED: 100PF CAP. @ LOC 14C.
G/A | [illegible] | 03088-32 | VB | 3-26-75 | R02

AREA LG: 15E-13 WAS TO 14E-15
PE | KM | 2576 | - | 7-18-75 | R03

AREA C9, 19-129 INVERSION BUBBLES ON PINS 7, 9 & 10-15 WERE NOT SHOWN.
A | C | 2570 | - | 8-26-75 | F04

AREA D2: 19F-05 WAS TO MNE. CS011, CROSS-REF TO 14M4
05 | 27 | 3157 | - | 5-11-77 | A05

NOTES:

NAME	TITLE	DATE
E. ROE	DRAFT	10-12-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32
CPB
03088
35-537 ROSD08
SHEET 13 OF 14

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
ADDED: 19-115 @ 14M, SHT. LOC E4, 109-3 CONN TO S2B0A NET, 19-057 @ 02D-SHT LOC K8; CHANGED: MPENO WAS TRAP120
GJ/KP 03088-30 MS 1-21-75 R01
ADDED RESISTOR AT LOC. B1
GM KP 03088-37 MS 4-8-75 R02
AREA M2: ADDED 13D2 TO MNE. CSA1. AREA M4: DELETED 13D2 & 13E7 FROM CS011.
WS MM 3537 5-11-77 R03
AREA G5: DELETED INVERTING BUBBLE FROM PIN 05 OF 02J.
GS MM 3531 5-22-78 R04
AREA A7 & A8 SIGNALS YD281, YD291, YD301, & YD311 CROSS REF 2H2 WAS 1H2.
KR KP 4231 R 3-7-80 R05

NOTES

NAME	TITLE	DATE
PEDWARDS	DRAFT	
	CHK	
	ENGN	
	DIR ENG	

TITLE **FUNCTIONAL SCHEMATIC**
8/32 CPB

PROJ NO 03088
DWG NO 35-537 R05 D08
SHEET OF 14 14

BRUNING 44-231 16042

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530

SEE TABLE

VIEW B-B
TYP 6 PLACES

PARTIAL VIEW A-A
TYP 3 PLACES

METRIC

TABLE

F01	ASSEMBLY AS SHOWN
F00	ASSEMBLY AS SHOWN LESS ITEM 92 IN LOCATION 000
VARIATION	DESCRIPTION

COMPONENT	REF DESIGNATION

REVISIONS

PRE PRODUCTION APPROVAL	DEV PROD	INIT'L	DATE

ADDED: ITEM 103 TO POS 01A, 03A, 04A, 05A; ITEM 21 POS 02D; ITEM 25 POS 13J; ITEM 118 POS CONN 7 & CONN 8; ITEM 103 POS 12B PLUS 03B & 14. DELETED: 2-ITEM 91 & POS 01B PLUS 811, 7 & 10.

7/10	03000-30	10-22-76	E01	
ADDED ITEM 21 TO LOCATION 040				
5/11	03000-30	1-24-77	E02	
ADDED: ITEM 83 @ LOC 183, ITEM 101 @ LOC 18C.				
5/13	03000-30	3-16-78	E03	
ADDED RESISTOR TO LOC. 14C; -4K16				
5/11	03000-30	4-8-75	E04	
ADDED STRAPS FROM 03001 TO 03003 & 03001 TO 03004				
5/11	03000-30	4-8-75	E05	
28W WAS ITEM 81				
5/15	03000-30	4-24-75	E06	
ADDED CARD AND HARDWARE TO 15.				
5/16	03000-30	4-28-75	E07	

RELEASED FOR PRODUCTION
MFG ENG. DATE 5/1/75

055 WAS ITEM 96
063 WAS ITEM 85

2	MA6820	8-28-75	E08

LED NEAR I/C SOCK A01 WAS AS FOLLOWS
03000 (113)

4/11	2886	10-29-75	E09

ADDED RESISTOR AT 000 FOR VARIATION F01 ADD STRAP BETWEEN 030-04 & 040-05

4/11	2857	5-14-76	E10

ADDED ITEM 105'S TO LOCATION 030

6/11	2907	8-5-76	E11

LOC 00G ADDED I/C SOCKET ITEM 104

METRIC DIM VIEW A-A & TABLE ADDED.

GPW	3448	3-30-81	E12

DELETED ITEM 104 FROM LOC 00C. ADDED PICTURE OF ITEM 109 TO ZC 000, A01, A03 - A05

11	4597	6-23-81	E13

	NAME	TITLE	DATE
	W. LIMPERT	DRAFT	10/31/74
	G. HOLMFIELD	CHK	
	S. MESSINA	ENGR	
	E. ZACHESKE	QA	
	S. MESSINA	MGR	

TITLE: ASSEMBLY PRINTED CIRCUIT MOD 8/38 CPU

03000

35-537473 03 1-1

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
PRE PRODUCTION APPROVAL	DEV PRODUCT	INIT	DATE NOV 5 1974

CHANGED: SHEETS 3, 4, & 5 WERE R00 REV.
GS/MK | 03088-38 | 1-24-75 | R01

ADDED: SHEETS 6-9; REF TO SHT 8 ON '0000' THRU 'A310' LEADS.
GS/MK | 03088-39 | 1-27-75 | R02

CHANGED: SHEETS 4 & 5 WERE R01 REV.
GS/MK | 03088-41 | 1-27-75 | R03

CHANGED: SHEETS 4 & 5 WERE R02 REV
GS/MK | 03088-56 | 4-10-75 | R04

RELEASED FOR PRODUCTION
ENG [illegible] DATE 5/14/75

REV LEV OF SHT 5 WAS R03 REV LEV OF DOS LOC 59 WAS R00, REV LEV OF CPC WAS R06
GS/MK | 2506 | - | 5-27-75 | R05

ENTIRE SHT 3 19-077's INVERSION BUBBLES PIN 6, WAS NOT SHOWN. REVISED SHTS 1, 2, 6&7.
KR | 2570 | - | 8-25-75 | R06

REVISED SHT. 8
MS | 2688 | - | 12-12-75 | R07

REVISED SHTS 1 & 8 ADDED MANUAL REF. THIS SHT. AREA R7.
GS/MK | 3587 | 5-23-78 | R08

REVISED SHTS 1 & 5. AREA 59. 35-555 WAS R08. 35-555 F01 WAS R04.
KR | 4279 | MS | 2-28-80 | R09

REVISED SHTS 1, 2, 4, 5, & 9. AREA A1 PSW261A W/LOCATOR 5N5 WAS PSW260A W/LOCATOR 5N6. AREA A2 PSW271A W/LOCATOR 5N7 WAS PSW270A W/LOCATOR 5N8.
KR | 4231 | R | 3-10-80 | RID

REVISED SHTS 1, 3 & 5.
KR/MH | 4953 | MS | 4-19-82 | R11

REVISED SHTS 1 & 8
MH | 5105 | R | 7-7-82 | R12

4L7 AAD030
4L5 AAD040
4L1 AAD051
5N5 PSW261A
5N7 PSW271A
4L8 AAD020
4F6 AAD000
4F5 AAD010
4L3 ASTKNO
5H5 WCLK0A

3D1 SB001 — 00W — DATAIN — DATAOUT — 8H1 A000 — 107-0
3D1 SB011 — 00T — 8H1 A010 — 207-0
3D2 SB021 — 00S — 8H1 A020 — 108-0
3D2 SB031 — 00M — 8H2 A030 — 208-0
3D3 SB041 — 00K — 8H2 A040 — 109-0
3D4 SB051 — 00J — 8H3 A050 — 209-0
3D4 SB061 — 01W — 8H3 A060 — 110-0
3D4 SB071 — 01T — 8H3 A070 — 210-0
3D5 SB081 — 01S — 8H4 A080 — 112-0
3D6 SB091 — 01M — 8H4 A090 — 212-0
3D6 SB101 — 01K — 8H4 A100 — 113-0
3D6 SB111 — 01J — 8H5 A110 — 213-0
3D7 SB121 — 03S — 8H5 A120 — 114-0
3D8 SB131 — 03M — 8H6 A130 — 214-0
3D8 SB141 — 04S — 8H6 A140 — 115-0
3D8 SB151 — 04M — 8H6 A150 — 215-0
3J1 SB161 — 08W — 8K1 A160 — 107-1
3J1 SB171 — 08T — 8K1 A170 — 207-1
3J2 SB181 — 08S — 8K2 A180 — 108-1
3J2 SB191 — 08M — 8K2 A190 — 208-1
3J3 SB201 — 08K — 8K2 A200 — 109-1
3J4 SB211 — 09W — 8K3 A210 — 209-1
3J4 SB221 — 09T — 8K3 A220 — 110-1
3J4 SB231 — 09S — 8K3 A230 — 210-1
3J5 SB241 — 09M — 8K4 A240 — 112-1
3J6 SB251 — 09K — 8K4 A250 — 212-1
3J6 SB261 — 10W — 8K5 A260 — 113-1
3J6 SB271 — 10T — 8K5 A270 — 213-1
3J7 SB281 — 10S — 8K5 A280 — 114-1
3J8 SB291 — 10M — 8K6 A290 — 214-1
3J8 SB301 — 10K — 8K6 A300 — 115-1
3J8 SB311 — 11W — 8K7 A310 — 215-1

All 19-077 256-BIT MEM; WE; DATAOUT; A; 06

USED IN MANUAL 29-394

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

8/32 CPC	35-555 R11
8/32 CPC w/ DCS	35-555 F01 R09

SHEET INDEX	REV	12	2	2	4	7	1	1	3	1
	SHT NO.	1	2	3	4	5	6	7	8	9

NOTES

NAME	TITLE	DATE
G. MELTON	DRAFT	10-15-74
G.J. HOMEFIELD	CHK	1-23-75
E. DeANGELO	ENGR	
R. BARKER	G.M.	
R.E. JONES	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC 8/32 CPC
TASK NO 23088
DWG NO 35-555R12D08
SHEET OF 1 - 9

BRUNING 44-231 15042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
GATE SWT. 19-077'S, INVERSION BUBBLE ON PIN 6, WAS NOT SHOWN.			
W	2570	—	8-25-25 R01
AREA A1 PSW2618 WAS PSW2608. AREA A2 PSW2718 WAS PSW2708 AREA M9 LOCATOR 235-1 WAS 236-1.			
KR	4231	R	3-7-80 R02

4L8 BAD030
4L6 BAD040
4L2 BAD051
5N6 PSW2618
5N8 PSW2718
4F9 BAD020
4F8 BAD000
4F4 BAD010
4L4 BSTKN0
5H5 WCLK0

3D1 SB001 — 04K 19-077 256-BIT MEM — DATA IN / DATA OUT / ME1 / ME2 / ME3 / WE — 127-0 B000
3D1 SB011 — 05W 19-077 256 BIT MEM — 227-0 B010
3D2 SB021 — 05T 19-077 256 BIT MEM — 128-0 B020
3D2 SB031 — 05S 19-077 256 BIT MEM — 228-0 B030
3D3 SB041 — 05M 19-077 256 BIT MEM — 129-0 B040
3D4 SB051 — 05K 19-077 256 BIT MEM — 229-0 B050
3D4 SB061 — 06W 19-077 256 BIT MEM — 130-0 B060
3D4 SB071 — 06T 19-077 256 BIT MEM — 230-0 B070

3D5 SB081 — 06S 19-077 256 BIT MEM — 132-0 B080
3D6 SB091 — 06M 19-077 256 BIT MEM — 232-0 B090
3D6 SB101 — 06K 19-077 256 BIT MEM — 133-0 B100
3D6 SB111 — 07W 19-077 256 BIT MEM — 233-0 B110
3D7 SB121 — 07T 19-077 256 BIT MEM — 134-0 B120
3D8 SB131 — 07S 19-077 256 BIT MEM — 234-0 B130
3D8 SB141 — 07M 19-077 256 BIT MEM — 135-0 B140
3D8 SB151 — 07K 19-077 256BIT MEM — 235-0 B150

3J1 SB161 — 13S 19-077 256 BIT MEM — 127-1 B160
3J1 SB171 — 14W 19-077 256 BIT MEM — 227-1 B170
3J2 SB181 — 14T 19-077 256 BIT MEM — 128-1 B180
3J2 SB191 — 14S 19-077 256 BIT MEM — 228-1 B190
3J3 SB201 — 14M 19-077 256 BIT MEM — 129-1 B200
3J4 SB211 — 14K 19-077 256 BIT MEM — 229-1 B210
3J4 SB221 — 15W 19-077 256 BIT MEM — 130-1 B220
3J4 SB231 — 15T 19-077 256 BIT MEM — 230-1 B230

3J5 SB241 — 15S 19-077 256 BIT MEM — 132-1 B240
3J6 SB251 — 15M 19-077 256 BIT MEM — 232-1 B250
3J6 SB261 — 15K 19-077 256 BIT MEM — 133-1 B260
3J6 SB271 — 16W 19-077 256 BIT MEM — 233-1 B270
3J7 SB281 — 16T 19-077 256 BIT MEM — 134-1 B280
3J8 SB291 — 16S 19-077 256 BIT MEM — 234-1 B290
3J8 SB301 — 16M 19-077 256 BIT MEM — 135-1 B300
3J8 SB311 — 16K 19-077 256 BIT MEM — 235-1 B310

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 CPC
23088
35-555202 D08 SHEET 2 OF 9

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
CHANGED: MNEMONIC SCLK1 WAS SCLK1.				
4/M	MA	03088-28	MS	1-23-82 R01
AREA L9, ADDED IC 10F & 10J.				
KR	4953	MS	4-19-82	R02 K

117-0 S000 04 1D 1Q 02 NC
1Q̄ 03 SB001 1C1, 2C1
217-0 S010 05 2D 03W 19-131 QUAD D FF 2Q 07 NC
2Q̄ 06 SB011 1E1, 2E1
118-0 S020 12 3D 3Q 10 NC
3Q̄ 11 SB021 1F1, 2F1
218-0 S030 13 4D 4Q 15 NC
4Q̄ 14 SB031 1G1, 2G1
5U3 SCLK1 09 CLK
P5 16 10J 1K 01 CLR A

119-0 S040 04 02 NC
03 SB041 1J1, 2J1
219-0 S050 05 07 NC
06 SB051 1K1, 2K1
120-0 S060 12 03T 19-131 QUAD D FF 10 NC
11 SB061 1L1, 2L1
220-0 S070 13 15 NC
14 SB071 1N1, 2N1
09
01 A

122-0 S080 04 02 NC
03 SB081 1C3, 2C3
222-0 S090 05 04W 19-131 QUAD D FF 07 NC
06 SB091 1E3, 2E3
123-0 S100 12 10 NC
11 SB101 1F3, 2F3
223-0 S110 13 15 NC
14 SB111 1G3, 2G3
09
01 A

124-0 S120 04 02 NC
03 SB121 1J3, 2J3
224-0 S130 05 04T 19-131 QUAD D FF 07 NC
06 SB131 1K3, 2K3
125-0 S140 12 10 NC
11 SB141 1L3, 2L3
225-0 S150 13 15 NC
14 SB151 1N3, 2N3
09
01 A

117-1 S160 04 02 NC
03 SB161 1C5, 2C5
217-1 S170 05 12W 19-131 QUAD D FF 07 NC
06 SB171 1E5, 2E5
118-1 S180 12 10 NC
11 SB181 1F5, 2F5
218-1 S190 13 15 NC
14 SB191 1G5, 2G5
09
01 A

119-1 S200 04 02 NC
03 SB201 1J5, 2J5
219-1 S210 05 12T 19-131 QUAD D FF 07 NC
06 SB211 1K5, 2K5
120-1 S220 12 10 NC
11 SB221 1L5, 2L5
220-1 S230 13 15 NC
14 SB231 1N5, 2N5
09
01 A

122-1 S240 04 02 NC
03 SB241 1C7, 2C7
222-1 S250 05 13W 19-131 QUAD D FF 07 NC
06 SB251 1E7, 2E7
123-1 S260 12 10 NC
11 SB261 1F7, 2F7
223-1 S270 13 15 NC
14 SB271 1G7, 2G7
09
01 A

124-1 S280 04 02 NC
03 SB281 1J7, 2J7
224-1 S290 05 13T 19-131 QUAD D FF 07 NC
06 SB291 1K7, 2K7
125-1 S300 12 10 NC
11 SB301 1L7, 2L7
225-1 S310 13 15 NC
14 SB311 1N7, 2N7
09
01 A

P5 16 11M 1K
111-3 SRCLK1
5G2 SCLR0A
10J 19-057 5G
11K 19-116
11M 19-063
10F 19-065
ENB SEL
102-1 MSEL000
202-1 MSEL010
103-1 MSEL020
5H2 WSELIA
NC

M37X1 4A1
S37X1 4A2
M7X1 5G7
S7X1 5G6

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 CPC
TASK NO. 03088
DWG NO. 35-555 R02 D08
SHEET 3 OF 9

BRUNING 44-231 15042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
CHANGED: MNEMONIC 'SODD041' WAS 'SSEL041'; ADDED: GATE @ SHT LOC B8-19-055 @ 08H; 19-126 @ 01H SHT LOC F4; DELETED: 2-33-035 SWITCHES @ 16A & 16B				
4½	MW	03088-28	1-23-75	R01
ADDED: PES ON 'PSW25I' LEAD, @ 11H, PINS 01 & 16.				
5½	MW	03088-41	1-23-75	R02
WSELO WENT TO SL4 WSELIA, WSELOA & WSELI WENT TO SL3				
6½	[illegible]	03088 -56	4-10-75	R03
AREA L1 LOCATOR 1A1 WAS 2A1. AREA L2 LOCATOR 2A1 WAS 1A1. AREA E4 01H-09 & 01H-10 WERE REVERSED.				
KR	77	4231	3-7-80	R04

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC

DWG NO. 03088 REV 35-555 R04D08 SHEET 4 OF 9

ERUWING 44-231 10042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

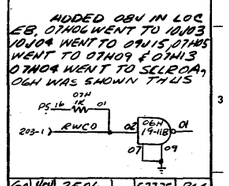
REVISIONS

CHANGED: 13K10 WAS CONN TO 'M7X1 NET; 13K8 WAS CONN TO BKLO NET,
DELETED: 19-057 GATE ON 'PCLKO' NET,
ADDED: GATE @ LOC 12K 19-055; GATE @ LOC 10J 19-057; GATE @ LOC 08H 19-056.
GW | MK | 03088-28 | SS | 1-23-75 | R01

ADDED: 1K PULL-UP @ LOC 11H ON 'PSW260.
GW | MK | 03088-41 | SS | 1-23-75 | R02

DELETED IC 09H, 19057
ADDED 1, 12J, 19-064
GW | GD | 03088 -SS | MK | 4-10-75 | R03

ADDED 08J IN LOC E8. 07H0L WENT TO 10J03 10J04 WENT TO 09J15, 07H05 WENT TO 07H09 & 07H13 07H04 WENT TO SCLR0A, 06H WAS SHOWN THUS



GW | MGH | 2506 | – | 5-27-75 | R04

AREA B8 10N15 WAS CONNECTED 10J01. 10H05 WAS CONNECTED TO 10J03 10H03 & 10H12 WERE N.C.
KR | W | 4279 | MS | 2-28-80 | R05

AREA N5 PSW261A WAS PSW260A. AREA N6 RSW 261B WAS PSW260B. AREA N7 PSW 271A WAS PSW270A. AREA N8 PSW 271B WAS PSW270B. AREA G7 PSW261 WAS PSW260. AREA G9 PSW 271 WAS PSW270.
KR | W | 4231 | R | 3-10-80 | R06

AREA H2 ADDED 3K9 TO WSELIA.
KR | W | 4933 | MS | 4-19-82 | R07

NOTES

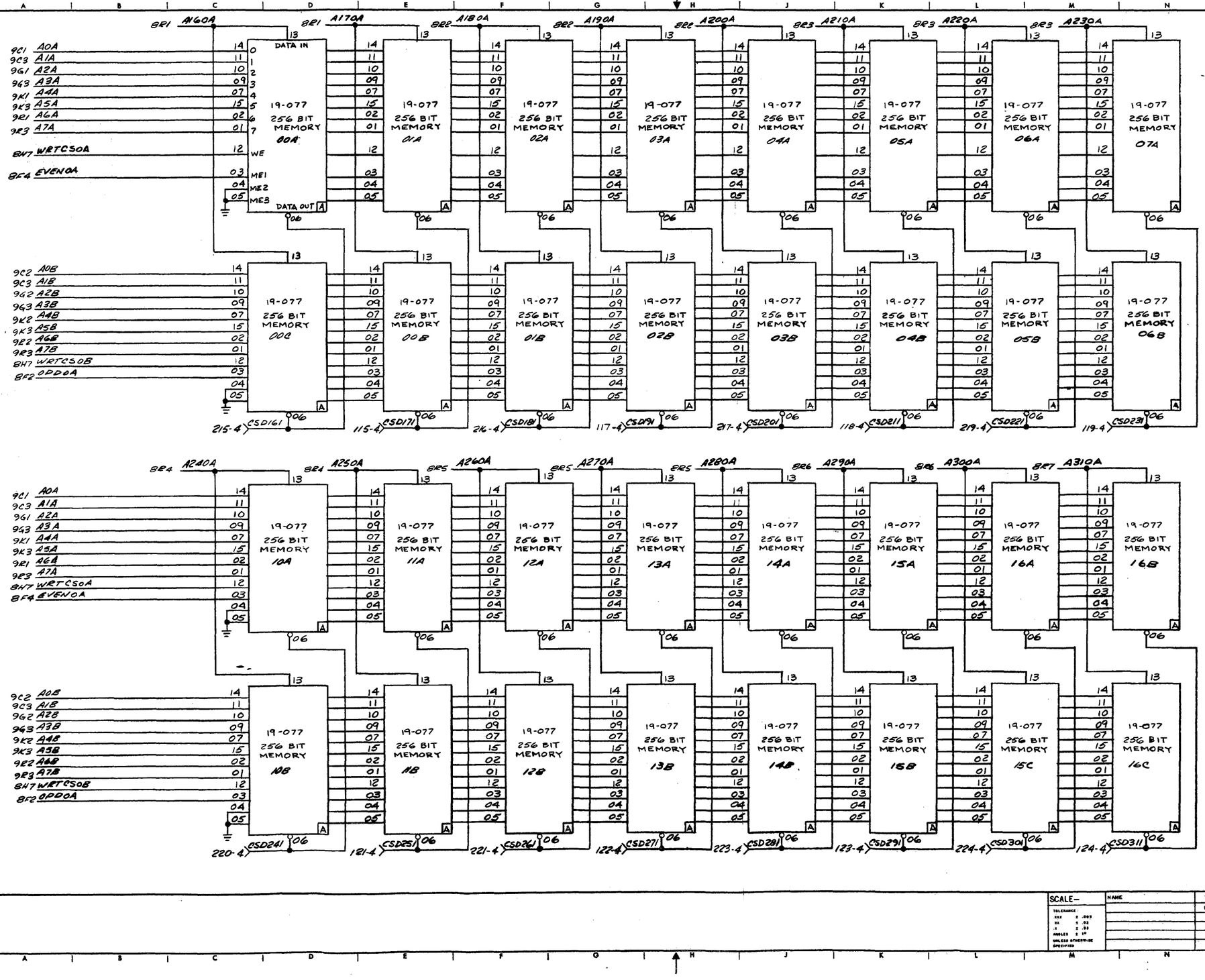
NAME P. EDWARDS

TITLE FUNCTIONAL SCHEMATIC
8132 CPC
03088
35-5557007008 5 9

BRUNING 44 231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



SCALE—

TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

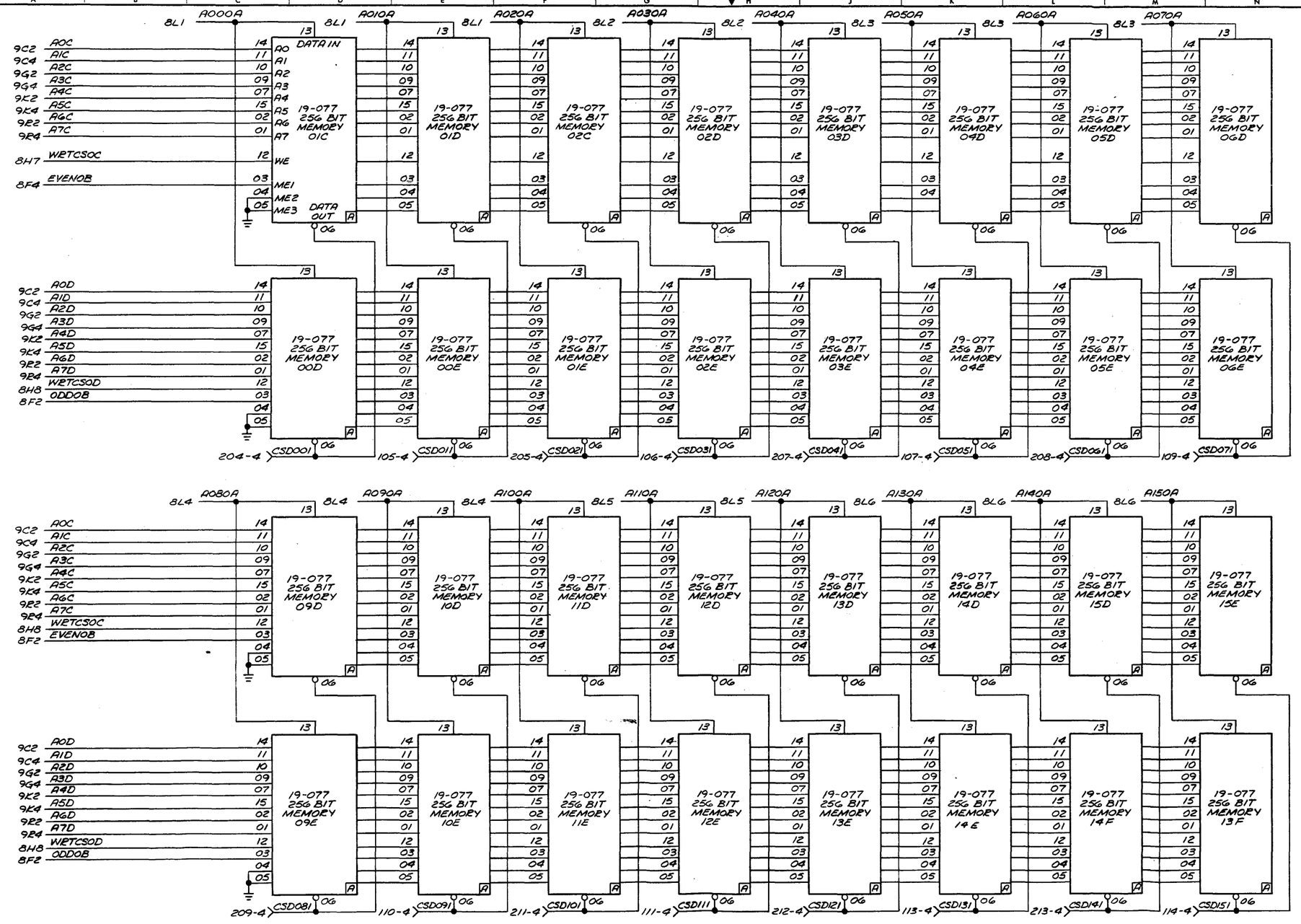
TITLE
FUNCTIONAL SCHEMATIC
MEM/32 CPC
(DCS OPTION)

TASK NO. 03088
DWG. NO. 35-535 D08
SHEET 6 OF 9

BRUNING 44-231 24539

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
ENTIRE SHT 19-077'S INVERSION BUBBLE ON PIN 6 WAS NOT SPEC'D				
SH	REV	2570	—	8-25-75



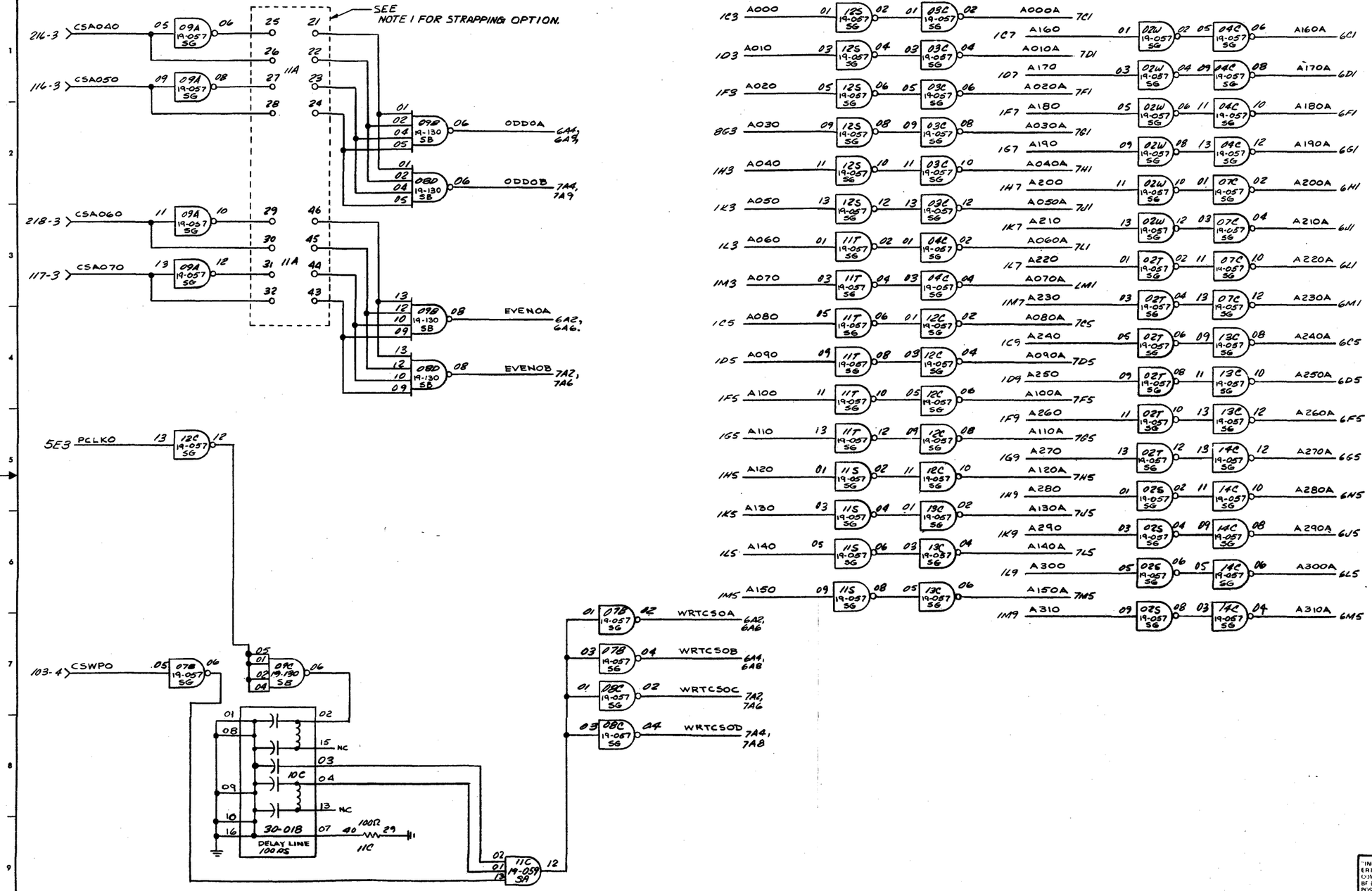
SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE
FUNCTIONAL SCHEMATIC
M8/32 CPC
(DCS OPTION)

TASK NO. 03088
DWG NO. 35-555 B01 D08
SHEET OF 7 — 9

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
FOR PREVIOUS INFO. SEE VOIDED COPY 35-555 R00 008			
WS	WA 2688	12-12-75	R01
AREA C1-C4: STRAPPING OPTION BRACKET WAS NOT SPEC'D. AREA A9: NOTE 1 WAS NOT SPEC'D			
GS	WA 3587	5-23-78	R02
AREA E2-E4 ALL 08D & 09B GATES WERE 19-060 (4 PLCS)			
JLV	WA 5105	7-7-82	R03



NOTES:
1. STRAPPING ADDRESS X'800-9FF'
21-25, 22-28, 23-30, 24-31,
46-25, 45-28, 44-30, 43-32

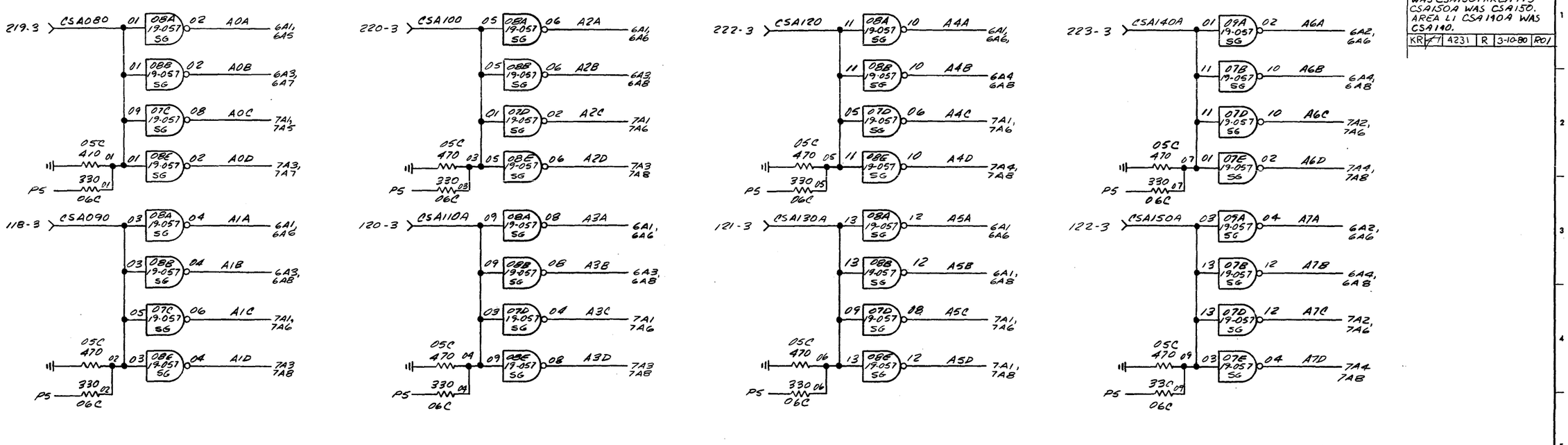
SCALE—	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE: FUNCTIONAL SCHEMATIC MB/32 CPC (DCS OPTION)
TAPE NO. 03088
DWG NO. 35-555 R3 D08
SHEET OF 8—9

BRUNING 44-231 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
AREA E3 CSA110A WAS CSA110. AREA H3 CSA130A WAS CSA130. AREA M3 CSA150A WAS CSA150. AREA L1 CSA190A WAS CSA190.
KR 4231 R 3-10-80 R01



SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

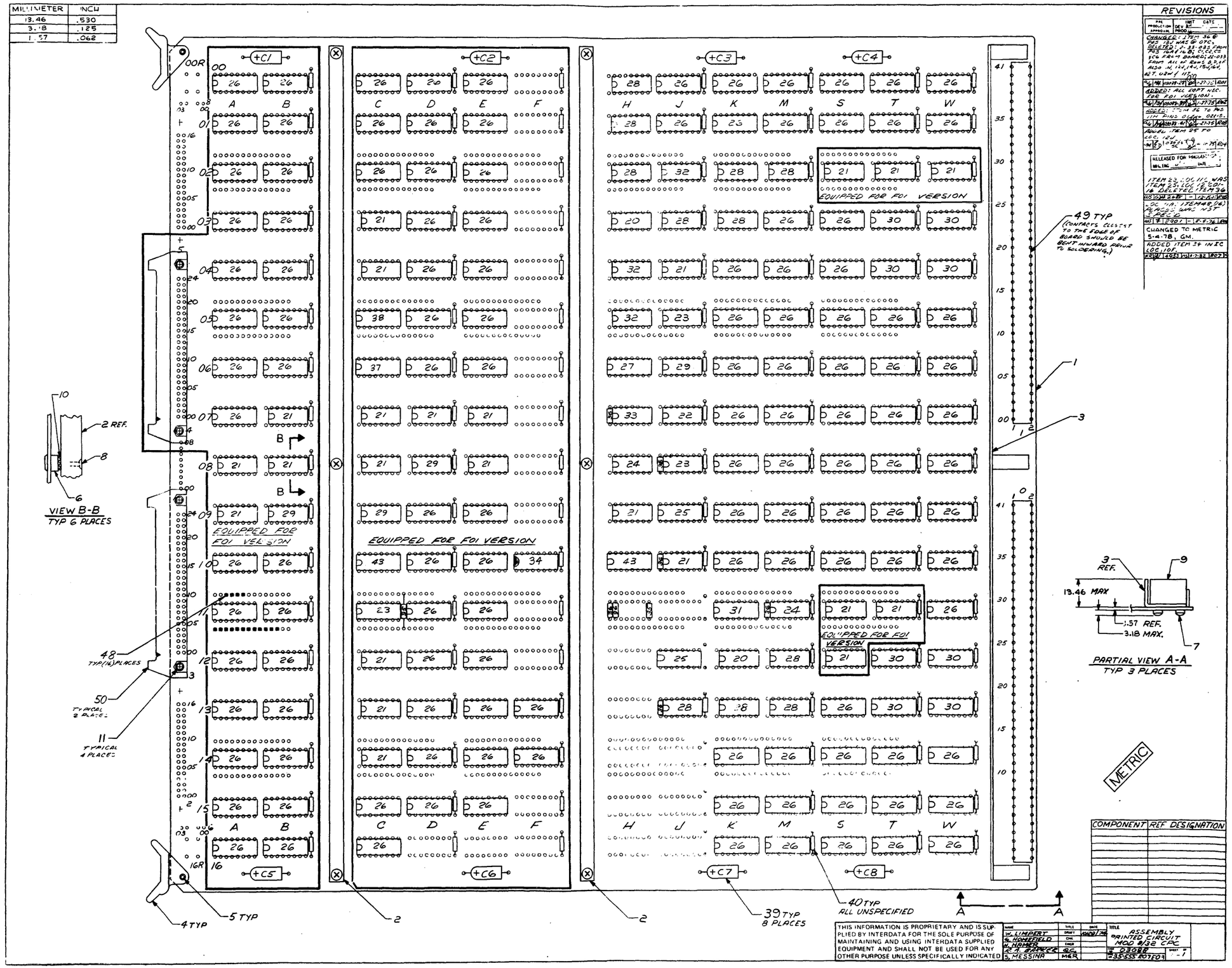
TITLE
FUNCTIONAL SCHEMATIC
M8/32 CPC
(DCS OPTION)

TASK NO. 03088
DWG NO. 35-555R01 D08
SHEET 9 OF 9

BRUNING 44-231 24538

Group Net [illegible] Board

MILLIMETER	INCH
13.46	.530
3.18	.125
1.57	.062



REVISIONS

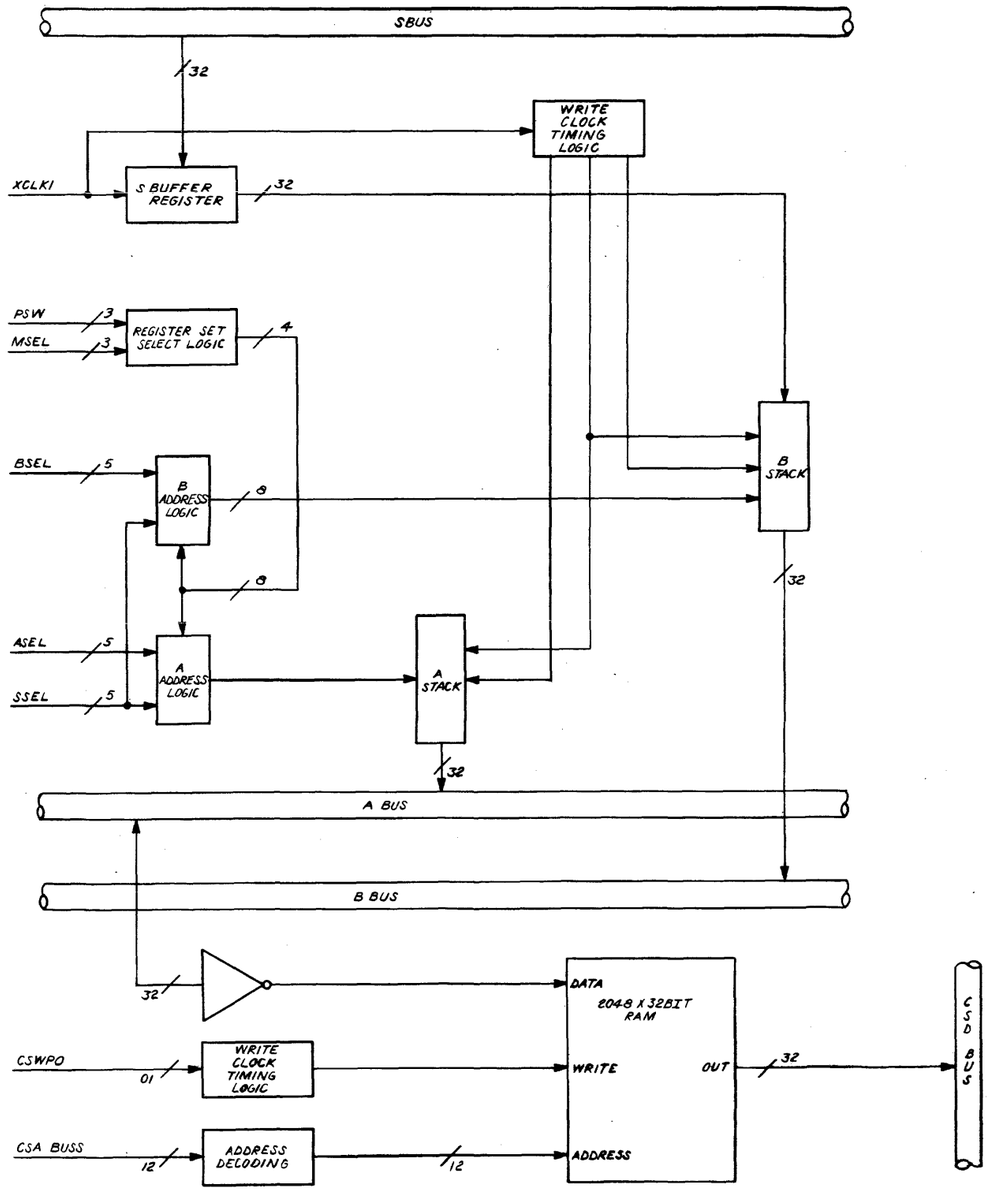
PRE PRODUCTION APPROVAL	DEV PROD	INIT	DATE

CHANGED: 1.750 TO 6 TPC 184 WAS 6 OTC).
DELETED: 2-22-033 FROM PCB ITEM 28, 0.C.C.C. 2 CR FROM BOARDS 21-033 FROM ALL 10 BDS & R.P.F. ALSO N, 140, 141, 150, 161 RET. U2W / 11-7-75
ADDED: ALL EQPT NEC. FOR FOI VERSION.
ADDED: ITEM 32 TO BDS WITH FOI3 OPTION. 001-5.
ADDED: ITEM 25 TO LOG 184
RELEASED FOR MANUFACTURING
ITEM 23, LOG 176 WAS ITEM 23, LOG 175 EQU. 16 DELETED ITEM 36
ADDED ITEM 37 (1 PER BD) TO LOG 176
CHANGED TO METRIC 5-4-78, GM.
ADDED ITEM 39 IN LOG 176

COMPONENT	REF DESIGNATION

NAME	TITLE	DATE
W. LIMPERT	DRAFT	6/6/78
G. HOMEFIELD	CHK	
W. HOPPER	ENGR	
A. BARRICK	QC	
S. MESSINA	MGR	

TITLE: ASSEMBLY PRINTED CIRCUIT MOD 832 CPC
03088-35555 REV E03
SHEET 1 OF 1



CONN	TERM. NO.	CABLE CONNECTOR MAP ROW 2	CABLE CONNECTOR MAP ROW 1	BACK PANEL MAP ROW 1	BACK PANEL MAP ROW 2	TERM. NO.	CONN
5	16			P5	P5	41	1
	15			GRD		40	
	14					39	
	13					38	
	12					37	
	11			GRD	GRD	36	
	10			B300	B310	35	
	09			B280	B290	34	
	08			B260	B270	33	
	07			B240	B250	32	
	06					31	
	05			B220	B230	30	
	04			B200	B210	29	
	03			B180	B190	28	
	02			B160	B170	27	
	01			GRD	GRD	26	
	00			S300	S310	25	
				S280	S290	24	
				S260	S270	23	
4	24	CSD301	CSD311	S240	S250	22	
	23	CSD281	CSD291			21	
	22	GRD	CSD271	S220	S230	20	
	21	CSD261	CSD251	S200	S210	19	
	20	CSD241	GRD	S180	S190	18	
	19	CSD221	CSD231	S160	S170	17	
	18	GRD	CSD211	GRD	GRD	16	
	17	CSD201	CSD191	A300	A310	15	
	16	CSD181	GRD	A280	A290	14	
	15	CSD161	CSD171	A260	A270	13	
	14	GRD	CSD151	A240	A250	12	
	13	CSD141	CSD131	GRD	GRD	11	
	12	CSD121	GRD	A220	A230	10	
	11	CSD101	CSD111	A200	A210	09	
	10	GRD	CSD091	A180	A190	08	
	09	CSD081	CSD071	A160	A170	07	
	08	CSD061	GRD	GRD	GRD	06	
	07	CSD041	CSD051			05	
	06	GRD	CSD031			04	
	05	CSD021	CSD011	MSEL020	RWC0	03	
	04	CSD001	GRD	MSEL000	MSEL010	02	
	03	GRD	CSWP0	GRD		01	
	02	GRD		P5	P5	00	
	01	GRD	GRD				
	00	GRD	GRD	P5	P5	41	
				GRD		40	
						39	
						38	
				STRT0		37	
3	24	GRD	GRD	GRD	GRD	36	0
	23	CSA140	GRD	B140	B150	35	
	22	CSA120	CSA150	B120	B130	34	
	21	GRD	CSA130	B100	B110	33	
	20	CSA100	CSA110	B080	B090	32	
	19	CSA080	GRD	GRD	GRD	31	
	18	CSA060	CSA090	B060	B070	30	
	17	GRD	CSA070	B040	B050	29	
	16	CSA040	CSA050	B020	B030	28	
	15	GRD	GRD	B000	B010	27	
	14	GRD	GRD	GRD	GRD	26	
	13	GRD	GRD	S140	S150	25	
	12	GRD	PCLK0	S120	S130	24	
	11	PSW251	SRCLK1	S100	S110	23	
	10	PSW261	PSW271	S080	S090	22	
	09	GRD	S280	GRD	GRD	21	
	08	ASEL031	ASEL041	S060	S070	20	
	07	ASEL011	ASEL021	S040	S050	19	
	06	GRD	ASEL001	S020	S030	18	
	05	BSEL031	BSEL041	S000	S010	17	
	04	BSEL011	BSEL021			16	
	03	GRD	BSEL001	A140	A150	15	
	02	SSEL031	SSEL041	A120	A130	14	
	01	SSEL011	SSEL021	A100	A110	13	
	00	GRD	SSEL001	A080	A090	12	
						11	
				A060	A070	10	
	16			A040	A050	09	
	15			A020	A030	08	
	14			A000	A010	07	
	13			GRD	GRD	06	
	12			SCLR0		05	
	11					04	
	10					03	
	09					02	
2	08			GRD		01	
	07			P5	P5	00	
	06						
	05						
	04						
	03						
	02						
	01						
	00						

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	BH	8/11/77
PROD		

SHTS. 1-10 HAVE BEEN REVISED. WCS WIRE DOES ON ALL SHTS. P5 FOR ROW 1,2 WERE NOT SHOWN PIN 26 WAS PIN 260

FOR 5.0 WCS REV 220

AS	BH	MS&E	11-1-77	R01

RELEASED FOR PRODUCTION
PROD. ENG. BH DATE 2/24/78

REVISED SHTS 1 & 6. AREA S9 35-663 WAS R01

KR	4279	MS	2-28-80	R02

AREA S9, 35-663 WAS R04, REVISED SHTS 1, 4 & 6.

KR	4953	MS	4-19-82	R03

BOARD	REV LEVEL
35-663	R06

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

REVISION	3	1	1	2	1	3	1	1	1	1
SHEET	1	2	3	4	5	6	7	8	9	10

SCALE —

	NAME	TITLE	DATE
	C. MICHAELS	DRAFT	7/20/77
	W. LIMPERT	CHK	7/29/77
	B. HAGERMAN	ENGR	2/24/78
	R.A. BARKER	Q.C.	2/24/78
	N. LEMONDE	MGR.	2/24/78

TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC W/2K WCS

ASY NO. 03838 SHEET OF 1 — 10

DWG NO. 35-663R03 D08

BRUNING 44-231 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

RESISTOR PACK 11J IN AREA D8 WAS NOT SHOWN. IN AREA B1 PSW261A WAS PSW260A IN AREA A2 PSW271A WAS PSW270A			
B	SHEET	11-1-77	201

5L7 AAD030
5L5 AAD040
5L1 AAD051
6N6 PSW261A
6N8 PSW271A
5L8 AAD020
5F6 AAD000
5F5 AAD010
5L3 ASTKNO
6H5 WCLK0A

4D1 SB001 — 00W 19-077 256-BIT MEM — 9H1 10T-0 A000
4D1 SB011 — 00T 19-077 256BIT MEM — 9H1 207-0 A010
4D2 SB021 — 00S 19-077 256-BIT MEM — 9H1 108-0 A020
4D2 SB031 — 00M 19-077 256-BIT MEM — 9H2 208-0 A030
4D3 SB041 — 00K 19-077 256-BIT MEM — 9H2 109-0 A040
4D4 SB051 — 00V 19-077 256-BIT MEM — 9H3 209-0 A050
4D4 SB061 — 01W 19-077 256-BIT MEM — 9H3 110-0 A060
4D4 SB071 — 01T 19-077 256-BIT MEM — 9H3 210-0 A070

4D5 SB081 — 01S 19-077 256-BIT MEM — 9H4 112-0 A080
4D6 SB091 — 01M 19-077 256-BIT MEM — 9H4 212-0 A090
4D6 SB101 — 01K 19-077 256-BIT MEM — 9H4 113-0 A100
4D6 SB111 — 01V 19-077 256-BIT MEM — 9H5 213-0 A110
4D7 SB121 — 03S 19-077 256-BIT MEM — 9H5 114-0 A120
4D8 SB131 — 03M 19-077 256-BIT MEM — 9H6 214-0 A130
4D8 SB141 — 04S 19-077 256-BIT MEM — 9H6 115-0 A140
4D8 SB151 — 04M 19-077 256-BIT MEM — 9H6 215-0 A150

4J1 SB161 — 08W 19-077 256-BIT MEM — 9K1 107-1 A160
4J1 SB171 — 08T 19-077 256-BIT MEM — 9K1 207-1 A170
4J2 SB181 — 08S 19-077 256-BIT MEM — 9K2 108-1 A180
4J2 SB191 — 08M 19-077 256-BIT MEM — 9K2 208-1 A190
4J3 SB201 — 08K 19-077 256-BIT MEM — 9K2 109-1 A200
4J4 SB211 — 09W 19-077 256-BIT MEM — 9K3 209-1 A210
4J4 SB221 — 09T 19-077 256-BIT MEM — 9K3 110-1 A220
4J4 SB231 — 09S 19-077 256-BIT MEM — 9K3 210-1 A230

4J5 SB241 — 09M 19-077 256-BIT MEM — 9K4 112-1 A240
4J6 SB251 — 09K 19-077 256-BIT MEM — 9K4 212-1 A250
4J6 SB261 — 10W 19-077 256-BIT MEM — 9K5 113-1 A260
4J6 SB271 — 10T 19-077 256-BIT MEM — 9K5 213-1 A270
4J7 SB281 — 10S 19-077 256-BIT MEM — 9K5 114-1 A280
4J8 SB291 — 10M 19-077 256-BIT MEM — 9K6 214-1 A290
4J8 SB301 — 10K 19-077 256-BIT MEM — 9K6 115-1 A300
4J8 SB311 — 11W 19-077 256-BIT MEM — 9K7 215-1 A310

11J 21-025 F03 RESISTOR MODULES
08 N.C.
13 N.C.
14 N.C.
15 N.C.
16 PS

NOTES

NAME	TITLE	DATE
P.CARD	DRAFT	7-8-77
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC W/2K WCS
TASK NO. 0.3828
DWG NO. 35-663R01 D08
SHEET 2 OF 10

BRUNING 44-231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
RESISTOR PACK 16J IN AREA 2B WAS NOT SHOWN IN AREA A1 PSW 26 IB WAS PSW 26 OB IN AREA A2 PSW 27 IB WAS PSW 27 OA			
BY	PCN	DATE	ECO
	3462	VI-1-77	201

5L8 BAD030
5L6 BAD040
5L2 BAD051
6N5 PSW26IB
6N7 PSW27IB
5F9 BAD020
5F8 BAD000
5F4 BAD010
5L4 BSTKNO
6H5 WCLKO

4D1 SB001 — 04K 19-077 256-BIT MEM — DATA IN — WE — DATA OUT A — 06 — 127-0 B000
4D1 SB011 — 05W 19-077 256 BIT MEM — A — 06 — 227-0 B010
4D2 SB021 — 05T 19-077 256 BIT MEM — A — 06 — 128-0 B020
4D2 SB031 — 05S 19-077 256 BIT MEM — A — 06 — 228-0 B030
4D3 SB041 — 05M 19-077 256 BIT MEM — A — 06 — 129-0 B040
4D4 SB051 — 05K 19-077 256 BIT MEM — A — 06 — 229-0 B050
4D4 SB061 — 06W 19-077 256 BIT MEM — A — 06 — 130-0 B060
4D4 SB071 — 06T 19-077 256 BIT MEM — A — 06 — 230-0 B070

4D5 SB081 — 06S 19-077 256 BIT MEM — A — 06 — 132-0 B080
4D6 SB091 — 06M 19-077 256 BIT MEM — A — 06 — 232-0 B090
4D6 SB101 — 06K 19-077 256 BIT MEM — A — 06 — 133-0 B100
4D6 SB111 — 07W 19-077 256 BIT MEM — A — 06 — 233-0 B110
4D7 SB121 — 07T 19-077 256 BIT MEM — A — 06 — 134-0 B120
4D8 SB131 — 07S 19-077 256 BIT MEM — A — 06 — 234-0 B130
4D8 SB141 — 07M 19-077 256 BIT MEM — A — 06 — 135-0 B140
4D8 SB151 — 07K 19-077 256BIT MEM — A — 06 — 235-0 B150

4J1 SB161 — 13S 19-077 256 BIT MEM — A — 06 — 127-1 B160
4J1 SB171 — 14W 19-077 256 BIT MEM — A — 06 — 227-1 B170
4J2 SB181 — 14T 19-077 256 BIT MEM — A — 06 — 128-1 B180
4J2 SB191 — 14S 19-077 256 BIT MEM — A — 06 — 228-1 B190
4J3 SB201 — 14M 19-077 256 BIT MEM — A — 06 — 129-1 B200
4J4 SB211 — 14K 19-077 256 BIT MEM — A — 06 — 229-1 B210
4J4 SB221 — 15W 19-077 256 BIT MEM — A — 06 — 130-1 B220
4J4 SB231 — 15T 19-077 256 BIT MEM — A — 06 — 230-1 B230

4J5 SB241 — 15S 19-077 256 BIT MEM — A — 06 — 132-1 B240
4J6 SB251 — 15M 19-077 256 BIT MEM — A — 06 — 232-1 B250
4J6 SB261 — 15K 19-077 256 BIT MEM — A — 06 — 133-1 B260
4J6 SB271 — 16W 19-077 256 BIT MEM — A — 06 — 233-1 B270
4J7 SB281 — 16T 19-077 256 BIT MEM — A — 06 — 134-1 B280
4J8 SB291 — 16S 19-077 256 BIT MEM — A — 06 — 234-1 B290
4J8 SB301 — 16M 19-077 256 BIT MEM — A — 06 — 135-1 B300
4J8 SB311 — 16K 19-077 256 BIT MEM — A — 06 — 235-1 B310

16J 21-025 F03 RESISTOR MODULE
09 — 180Ω 1/4W — +08
08 NC
13 NC
14 NC
15 NC
16 P5

DRAWN: F. CARD — 7/8/77

TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC W/2K WCS
03898
35-663R01 D08
SHEET OF 3-10

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

IN AREA A7 PIN 11 FOR IC U.K. WAS NOT SHOWN				
125	[illegible]	3462	11-1-77	R01
AREA L9, ADDED 10F & 10V.				
KR	[illegible]	4953	MS 4-19-82	R02

03W 19-131 QUAD D FF
117-0 S000 04 1D 1Q 02 NC
1Q̄ 03 SB001 2C1, 3C1
217-0 S010 05 2D 2Q 07 NC
2Q̄ 06 SB011 2E1, 3E1
118-0 S020 12 3D 3Q 10 NC
3Q̄ 11 SB021 2F1, 3F1
218-0 S030 13 4D 4Q 15 NC
4Q̄ 14 SB031 2G1, 3G1
6U3 SCLK1 09 CLK
P5 16 10J 1K 1 01 CLR A

03T 19-131 QUAD D FF
119-0 S040 04 1D 1Q 02 NC
1Q̄ 03 SB041 2J1, 3J1
219-0 S050 05 2D 2Q 07 NC
2Q̄ 06 SB051 2K1, 3K1
120-0 S060 12 3D 3Q 10 NC
3Q̄ 11 SB061 2L1, 3L1
220-0 S070 13 4D 4Q 15 NC
4Q̄ 14 SB071 2N1, 3N1
09 01 A

04W 19-131 QUAD D FF
122-0 S080 04 1D 1Q 02 NC
1Q̄ 03 SB081 2C3, 3C3
222-0 S090 05 2D 2Q 07 NC
2Q̄ 06 SB091 2E3, 3E3
123-0 S100 12 3D 3Q 10 NC
3Q̄ 11 SB101 2F3, 3F3
223-0 S110 13 4D 4Q 15 NC
4Q̄ 14 SB111 2G3, 3G3
09 01 A

04T 19-131 QUAD D FF
124-0 S120 04 1D 1Q 02 NC
1Q̄ 03 SB121 2J3, 3J3
224-0 S130 05 2D 2Q 07 NC
2Q̄ 06 SB131 2K3, 3K3
125-0 S140 12 3D 3Q 10 NC
3Q̄ 11 SB141 2L3, 3L3
225-0 S150 13 4D 4Q 15 NC
4Q̄ 14 SB151 2N3, 3N3
09 01 A

12W 19-131 QUAD D FF
117-1 S160 04 1D 1Q 02 NC
1Q̄ 03 SB161 2C5, 3C5
217-1 S170 05 2D 2Q 07 NC
2Q̄ 06 SB171 2E5, 3E5
118-1 S180 12 3D 3Q 10 NC
3Q̄ 11 SB181 2F5, 3F5
218-1 S190 13 4D 4Q 15 NC
4Q̄ 14 SB191 2G5, 3G5
09 01 A

12T 19-131 QUAD D FF
119-1 S200 04 1D 1Q 02 NC
1Q̄ 03 SB201 2J5, 3J5
219-1 S210 05 2D 2Q 07 NC
2Q̄ 06 SB211 2K5, 3K5
120-1 S220 12 3D 3Q 10 NC
3Q̄ 11 SB221 2L5, 3L5
220-1 S230 13 4D 4Q 15 NC
4Q̄ 14 SB231 2N5, 3N5
09 01 A

13W 19-131 QUAD D FF
122-1 S240 04 1D 1Q 02 NC
1Q̄ 03 SB241 2C7, 3C7
222-1 S250 05 2D 2Q 07 NC
2Q̄ 06 SB251 2E7, 3E7
123-1 S260 12 3D 3Q 10 NC
3Q̄ 11 SB261 2F7, 3F7
223-1 S270 13 4D 4Q 15 NC
4Q̄ 14 SB271 2G7, 3G7
09 01 A

13T 19-131 QUAD D FF
124-1 S280 04 1D 1Q 02 NC
1Q̄ 03 SB281 2J7, 3J7
224-1 S290 05 2D 2Q 07 NC
2Q̄ 06 SB291 2K7, 3K7
125-1 S300 12 3D 3Q 10 NC
3Q̄ 11 SB301 2L7, 3L7
225-1 S310 13 4D 4Q 15 NC
4Q̄ 14 SB311 2N7, 3N7
09 01 A

P5 16 11M 1K 1
11K 19-116 SELECTOR
1A 1B 1C 1D 2A 2B 2C 2D STB1 SELB SELA STB2
1Y 2Y
10J 19-057 5G
M37X1 5A1
S37X1 5A2
11M 19-063 DS DC
M7X1 6G7
S7X1 6G6
111-3 SRCLK1
6G2 SCLR0A
10F 19-065 ENB SEL
1A 1B 2A 2B 3A 3B 4A 4B 1y 2y 3y 4y
NC NC NC
102-1 MSEL000
202-1 MSEL010
103-1 MSEL020
6H2 WSELIA
10J 19-057 5B

NOTES

NAME	TITLE	DATE
P. CARD	DRAFT	7/8/77
	CHK	
	ENGR	
	DIR ENG	

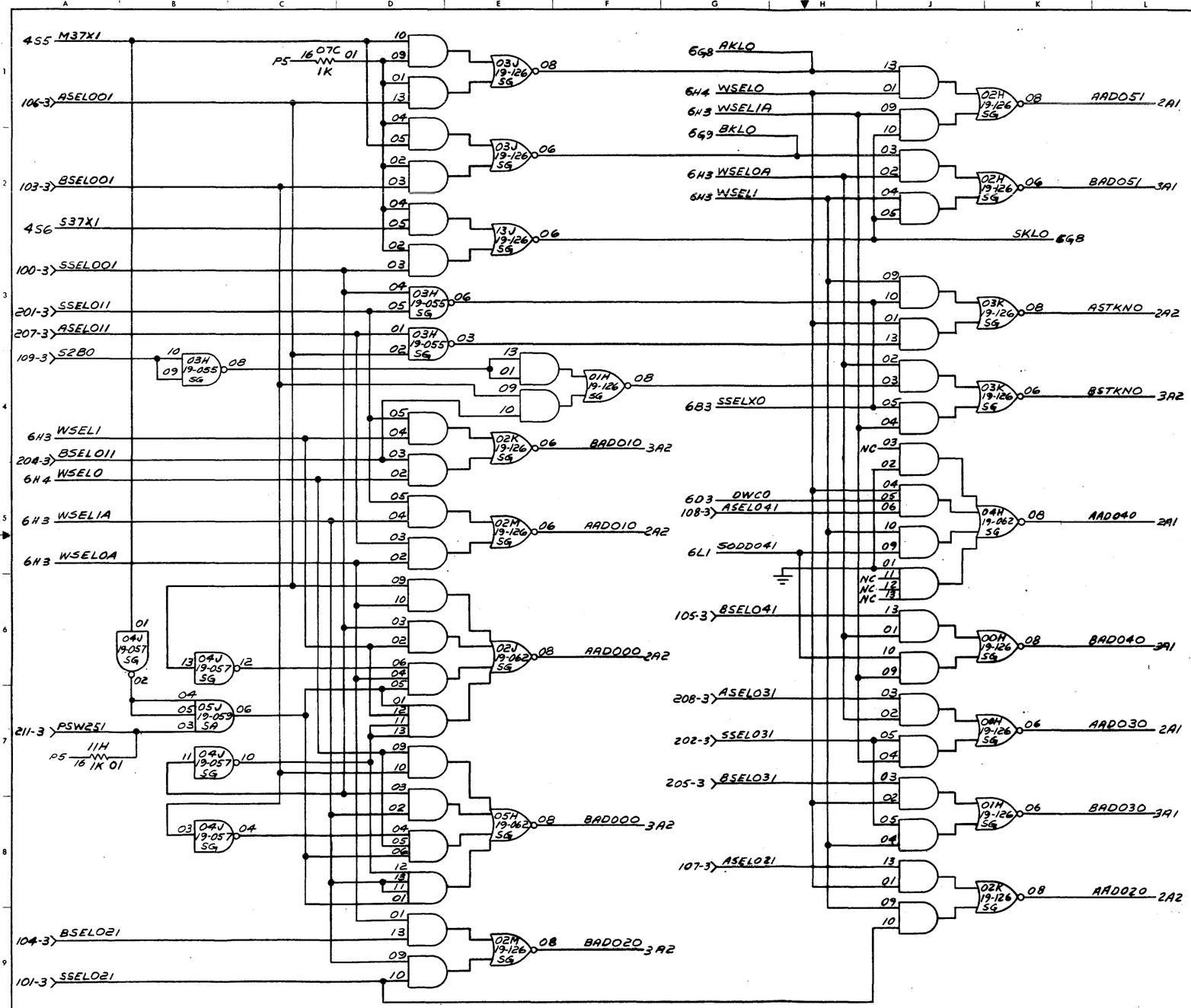
TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC W/12K WCS
TASK NO. 0389Z
DWG NO. 35-663R02 D08
SHEET 4 OF 10

BRUNING 44-231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

DESIGNATION FOR AADO51 WAS 3A1. DESIGNATION FOR BADO51 WAS 2A1			
BS		SEE SHEET 2	11-1-77



NOTES

BRUNING 44 211 16042

P. CARD	7/6/77	TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC W/2K WCS
		038908
		35-663R01 DO8 5-10

PERKIN ELMER

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

IN AREA 66 PSW26.1 WAS PSW26.0
IN AREA 69 PSW27.1 WAS PSW27.0
IN AREA 175 PSW26.1B WAS PSW26.0B
IN AREA 176 PSW26.1B WAS PSW26.0B
IN AREA 177 PSW27.1B WAS PSW27.0B
IN AREA 178 PSW26.1B WAS PSW26.0B

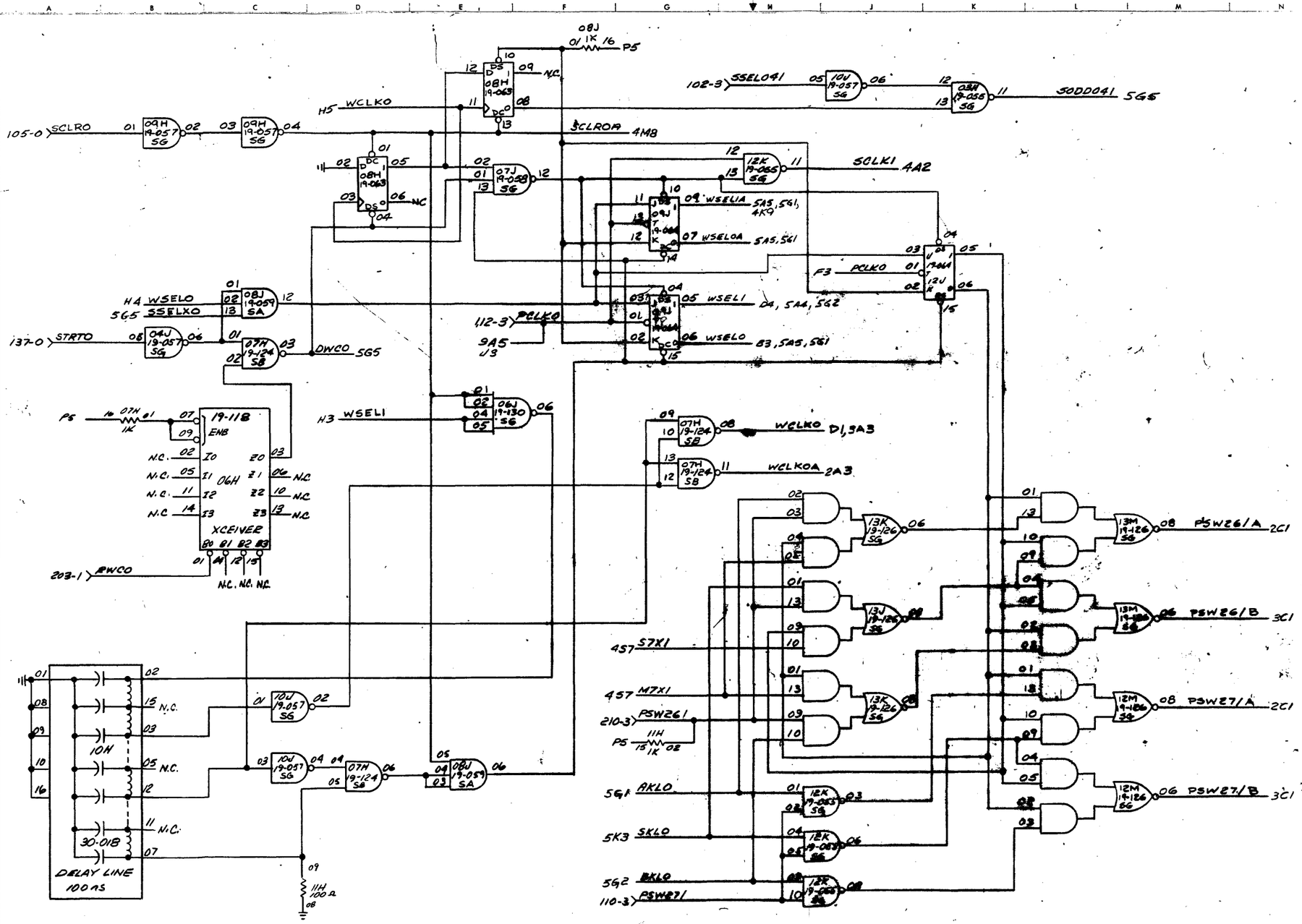
231	A	9462	11-1-77

AREA B8 10H15 WAS CONNECTED TO 10J01. 10H05 WAS CONNECTED TO 10J03. 10H03 & 10H12 WERE N.C.

KR	4279	MS	2-28-80	R02

AREA H2 ADDED 4K9 TO WSELIA.

KR	4953	PS	4-19-82	R03



NOTES

NAME	DATE
P. CARD	7/8/77

TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC W/2K WCS

0.3858
35-663R03 D03 6-10

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS					
	TITLE WCS WAS DCS				
825	9A	3962		11-1-77	B01

9C6 A001A — DATA IN — 19-218 1024 BIT MEMORY 01C — DATA OUT A — 07
9C6 A011A — 19-218 1024 BIT MEMORY 01D — A — 07
9C7 A021A — 19-218 1024 BIT MEMORY 02C — A — 07
9C7 A031A — 19-218 1024 BIT MEMORY 02D — A — 07
9C8 A041A — 19-218 1024 BIT MEMORY 03D — A — 07
9C8 A051A — 19-218 1024 BIT MEMORY 04D — A — 07
9C9 A061A — 19-218 1024 BIT MEMORY 05D — A — 07
9C9 A071A — 19-218 1024 BIT MEMORY 06D — A — 07

10D2	A0C	02	0
10D4	A1C	03	1
10D6	A2C	04	2
10D8	A3C	05	3
10H2	A4C	06	4
10H4	A5C	09	5
10H6	A6C	10	6
10H8	A7C	11	7
10N2	A8C	12	8
10N4	A9C	13	9
9E2	LOWOB	01	E/W
9H6	WETCSOC	14	

9D3 A0D — 19-218 1024 BIT MEMORY 00D — A — 07
9D5 A1D — 19-218 1024 BIT MEMORY 00E — A — 07
9D7 A2D — 19-218 1024 BIT MEMORY 01E — A — 07
9D9 A3D — 19-218 1024 BIT MEMORY 02E — A — 07
10H3 A4D — 19-218 1024 BIT MEMORY 03E — A — 07
10H5 A5D — 19-218 1024 BIT MEMORY 04E — A — 07
10H7 A6D — 19-218 1024 BIT MEMORY 05E — A — 07
10H9 A7D — 19-218 1024 BIT MEMORY 06E — A — 07
10N3 A8D — 15
10N5 A9D — 15
9E1 UPROB — 01
9H6 WETCSOD — 14

204-4 CSD001 — 105-4 CSD011 — 205-4 CSD021 — 106-4 CSD031 — 207-4 CSD041 — 107-4 CSD051 — 208-4 CSD061 — 109-4 CSD071

9H7 A081A — 19-218 1024 BIT MEMORY 09D — A — 07
9H8 A091A — 19-218 1024 BIT MEMORY 10D — A — 07
9H9 A101A — 19-218 1024 BIT MEMORY 11D — A — 07
9H9 A111A — 19-218 1024 BIT MEMORY 12D — A — 07
9M1 A121A — 19-218 1024 BIT MEMORY 13D — A — 07
9M1 A131A — 19-218 1024 BIT MEMORY 14D — A — 07
9M2 A141A — 19-218 1024 BIT MEMORY 15D — A — 07
9M2 A151A — 19-218 1024 BIT MEMORY 15E — A — 07

10D2	A0C	02	0
10D4	A1C	03	1
10D6	A2C	04	2
10D8	A3C	05	3
10H2	A4C	06	4
10H4	A5C	09	5
10H6	A6C	10	6
10H8	A7C	11	7
10N2	A8C	12	8
10N4	A9C	13	9
9E2	LOWOB	01	E/W
9H6	WRTCSOC	14	

10D3 A0D — 19-218 1024 BIT MEMORY 09E — A — 07
10D5 A1D — 19-218 1024 BIT MEMORY 10E — A — 07
10D7 A2D — 19-218 1024 BIT MEMORY 11E — A — 07
10D9 A3D — 19-218 1024 BIT MEMORY 12E — A — 07
10H3 A4D — 19-218 1024 BIT MEMORY 13E — A — 07
10H5 A5D — 19-218 1024 BIT MEMORY 14E — A — 07
10H7 A6D — 19-218 1024 BIT MEMORY 14F — A — 07
10H9 A7D — 19-218 1024 BIT MEMORY 13F — A — 07
10N3 A8D — 15
10N5 A9D — 15
9E1 UPROB — 01
9H6 WRTCSOD — 14

209-4 CSD081 — 110-4 CSD091 — 211-4 CSD101 — 111-4 CSD111 — 212-4 CSD121 — 113-4 CSD131 — 213-4 CSD141 — 114-4 CSD151

SCALE— | TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
P. CARD	DRAFT	7/8/77
	CHK	
	ENGR	

TITLE: FUNCTIONAL SCHEMATIC B/32 CPC W/2E W/CS
TASK NO. 03828 — SHEET OF 7—10
DWG NO. 35-662301 D08

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
IN TITLE	WCS WAS DCS		
105 [illegible] 3962		VI-1-77	ROI

9M3 A161A
9M3 A171A
9M4 A181A
9M4 A191A
9M4 A201A
9M5 A211A
9M5 A221A
9M6 A231A

10D1 A0A
10D3 A1A
10D5 A2A
10D7 A3A
10H1 A4A
10H3 A5A
10H5 A6A
10H7 A7A
10N1 A8A
10N3 A9A
9E2 LOWOA
9H5 WRTCSOA

10D2 A0B
10D4 A1B
10D6 A2B
10D8 A3B
10H2 A4B
10H4 A5B
10H6 A6B
10H8 A7B
10N2 A8B
10N4 A9B
9E1 UPPOA
9H6 WRTCSOB

DATA IN
DATA OUT
19-218 1024 BIT MEMORY 00A
19-218 1024 BIT MEMORY 01A
19-218 1024 BIT MEMORY 02A
19-218 1024 BIT MEMORY 03A
19-218 1024 BIT MEMORY 04A
19-218 1024 BIT MEMORY 05A
19-218 1024 BIT MEMORY 06A
19-218 1024 BIT MEMORY 07A
19-218 1024 BIT MEMORY 00C
19-218 1024 BIT MEMORY 00B
19-218 1024 BIT MEMORY 01B
19-218 1024 BIT MEMORY 02B
19-218 1024 BIT MEMORY 03B
19-218 1024 BIT MEMORY 04B
19-218 1024 BIT MEMORY 05B
19-218 1024 BIT MEMORY 06B

215-4 CSD161
115-4 CSD171
216-4 CSD181
117-4 CSD191
217-4 CSD201
118-4 CSD211
219-4 CSD221
119-4 CSD231

9M6 A241A
9M6 A251A
9M7 A261A
9M7 A271A
9M8 A281A
9M8 A291A
9M9 A301A
9M8 A311A

19-218 1024 BIT MEMORY 10A
19-218 1024 BIT MEMORY 11A
19-218 1024 BIT MEMORY 12A
19-218 1024 BIT MEMORY 13A
19-218 1024 BIT MEMORY 14A
19-218 1024 BIT MEMORY 15A
19-218 1024 BIT MEMORY 16A
19-218 1024 BIT MEMORY 16B
19-218 1024 BIT MEMORY 10B
19-218 1024 BIT MEMORY 11B
19-218 1024 BIT MEMORY 12B
19-218 1024 BIT MEMORY 13B
19-218 1024 BIT MEMORY 14B
19-218 1024 BIT MEMORY 15B
19-218 1024 BIT MEMORY 15C
19-218 1024 BIT MEMORY 16C

220-4 CSD241
121-4 CSD251
221-4 CSD261
122-4 CSD271
223-4 CSD281
123-4 CSD291
224-4 CSD301
124-4 CSD311

SCALE—	NAME	TITLE	DATE
TOLERANCE .XXX ± .005 .XX ± .02 .X ± .06 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	P. CARD	DRAFT	7/8/77
		CHK	
		ENGR	

TITLE
FUNCTIONAL SCHEMATIC
8/32 CPC W/ 2K WCS

DWG NO. 03898
DWG NO. 35-663R01 D08
SHEET OF 8—10

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA D6 PINS 09 & 08 WERE 22 & 07 RESPECTIVELY				
125	JR	9662	11-1-77	E01

216-3 CSA040 05 09A 19-057 SG 06
P5 16 06C 330 12 12 05C 470 16
116-3 CSA050 09 09A 19-057 SG 08
P5 06 330 13 13 05C 470
01 09B 19-124 SB 03 UPR0A 8A4, 8A9
02
04 09B 19-124 SB 06 UPR0B 7A4, 7A9
05
09 09B 19-124 SB 08 LOW0A 8A2, 8A7
10
12 09B 19-124 SB 11 LOW0B 7A2, 7A7
13

103-4 CSWP0 05 07B 19-057 SG 06
05
01 09C 19-130 SB 06
02
04
02
01
08
09
10
16
10C 30-018 DELAY LINE 100NS
15 NC
03 NC
14 NC
04 NC
13 NC
05 NC
12 NC
06 NC
11 NC
07 09 11C 100 08
09 13C 19-057 SG 08
01
02 12C 19-059 SA 12 WRTCS1
13
01 08A 19-057 SG 02 WRTCS0A 8A2, 8A7
01 08B 19-057 SG 02 WRTCS0B 8A4, 8A9
09 07C 19-057 SG 08 WRTCS0C 7A2, 7A7
01 08E 19-057 SG 02 WRTCS0D 7A4, 7A9

2C3 A000 01 12S 19-057 SG 02 A001A 7B1
2D3 A010 03 12S 19-057 SG 04 A011A 7D1
2F3 A020 05 12S 19-057 SG 06 A021A 7E1
2G3 A030 09 12S 19-057 SG 08 A031A 7F1
2H3 A040 11 12S 19-057 SG 10 A041A 7H1
2K3 A050 13 12S 19-057 SG 12 A051A 7J1
2L3 A060 01 11T 19-057 SG 02 A061A 7L1
2M3 A070 03 11T 19-057 SG 04 A071A 7M1

2C5 A080 05 11T 19-057 SG 06 A081A 7B5
2D5 A090 09 11T 19-057 SG 08 A091A 7D5
2F5 A100 11 11T 19-057 SG 10 A101A 7E5
2G5 A110 13 11T 19-057 SG 12 A111A 7F5

2H5 A120 01 11S 19-057 SG 02 A121A 7H5
2K5 A130 03 11S 19-057 SG 04 A131A 7J5
2L5 A140 05 11S 19-057 SG 06 A141A 7L5
2M5 A150 09 11S 19-057 SG 08 A151A 7M5
2C7 A160 01 02W 19-057 SG 02 A161A 8B1
2D7 A170 03 02W 19-057 SG 04 A171A 8D1
2F7 A180 05 02W 19-057 SG 06 A181A 8E1
2G7 A190 09 02W 19-057 SG 08 A191A 8F1
2H7 A200 11 02W 19-057 SG 10 A201A 8H1
2K7 A210 13 02W 19-057 SG 12 A211A 8J1
2L7 A220 01 02T 19-057 SG 02 A221A 8L1
2M7 A230 03 02T 19-057 SG 04 A231A 8M1
2C9 A240 05 02T 19-057 SG 05 A241A 8B5
2D9 A250 09 02T 19-057 SG 08 A251A 8D5
2F9 A260 11 02T 19-057 SG 10 A261A 8E5
2G9 A270 13 02T 19-057 SG 12 A271A F5
2H9 A280 01 02S 19-057 SG 02 A281A 8H5
2K9 A290 03 02S 19-057 SG 04 A291A 8J5
2L9 A300 05 02S 19-057 SG 06 A301A 8L5
2M9 A310 09 02S 19-057 SG 08 A311A 8M5

SCALE—	NAME	TITLE	DATE	TITLE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	P. CARD	DRAFT	7/8/77	FUNCTIONAL SCHEMATIC 8/32 CPC W/2K WCS
		CHK		
		ENGR		
		TASK NO. 03895		SHEET OF 9 —10
		DWG NO. 35-663R01 D08		

PERKIN ELMER
Oceanport, N.J. 07757

REVISIONS				
LTR	TITLE	WCS WAS	DCS	
AB	[illegible]		11-1-77	PDI

218-3 CSA060
- 01 09A 19-057 SG 02 — A0A — 8A1, 8A6
- 11 07B 19-057 SG 10 — A0B — 8A3, 8A8
- 05C 07 — 470 — 11 07D 19-057 SG 10 — A0C — 7A1, 7A6
- P5 — 06C 07 — 330 — 01 07E 19-057 SG 02 — A0D — 7A3, 7A8

117-3 CSA070
- 03 14C 19-057 SG 04 — A1A — 8A1, 8A6
- 05 14C 19-057 SG 06 — A1B — 8A3, 8A8
- 05C 10 — 470 — 09 14C 19-057 SG 08 — A1C — 7A1, 7A6
- P5 — 06C 10 — 330 — 11 14C 19-057 SG 10 — A1D — 7A3, 7A8

219-3 CSA080
- 01 07C 19-057 SG 02 — A2A — 8A1, 8A6
- 03 07C 19-057 SG 04 — A2B — 8A3, 8A8
- 05C 01 — 470 — 11 07C 19-057 SG 10 — A2C — 7A1, 7A6
- P5 — 06C 01 — 330 — 13 07C 19-057 SG 12 — A2D — 7A3, 7A8

118-3 CSA090
- 03 09A 19-057 SG 04 — A3A — 8A1, 8A6
- 13 07B 19-057 SG 12 — A3B — 8A4, 8A8
- 05C 09 — 470 — 13 07D 19-057 SG 12 — A3C — 7A1, 7A6
- P5 — 06C 09 — 330 — 03 07E 19-057 SG 04 — A3D — 7A4, 7A8

220-3 CSA100
- 11 08A 19-057 SG 10 — A4A — 8A2, 8A6
- 11 08B 19-057 SG 10 — A4B — 8A4, 8A8
- 05C 05 — 470 — 05 07D 19-057 SG 06 — A4C — 7A2, 7A6
- P5 — 06C 05 — 330 — 11 08E 19-057 SG 10 — A4D — 7A4, 7A8

120-3 CSA110
- 09 08A 19-057 SG 08 — A5A — 8A2, 8A6
- 09 08B 19-057 SG 08 — A5B — 8A4, 8A8
- 05C 04 — 470 — 03 07D 19-057 SG 04 — A5C — 7A2, 7A6
- P5 — 06C 04 — 330 — 09 08E 19-057 SG 08 — A5D — 7A4, 7A8

222-3 CSA120
- 05 08A 19-057 SG 06 — A6A — 8A2, 8A6
- 05 08B 19-057 SG 06 — A6B — 8A4, 8A8
- 05C 03 — 470 — 01 07D 19-057 SG 02 — A6C — 7A2, 7A6
- P5 — 06C 03 — 330 — 05 08E 19-057 SG 06 — A6D — 7A4, 7A8

121-3 CSA130
- 03 08A 19-057 SG 04 — A7A — 8A2, 8A6
- 03 08B 19-057 SG 04 — A7B — 8A4, 8A8
- 05C 02 — 470 — 05 07C 19-057 SG 06 — A7C — 7A2, 7A6
- P5 — 06C 02 — 330 — 03 08E 19-057 SG 04 — A7D — 7A4, 7A8

223-3 CSA140
- 01 07B 19-057 SG 02 — A8A — 8A2, 8A6
- 03 07B 19-057 SG 04 — A8B — 8A4, 8A9
- 05C 11 — 470 — 01 08C 19-057 SG 02 — A8C — 7A2, 7A6
- P5 — 06C 11 — 330 — 03 08C 19-057 SG 04 — A8D — 7A4, 7A9

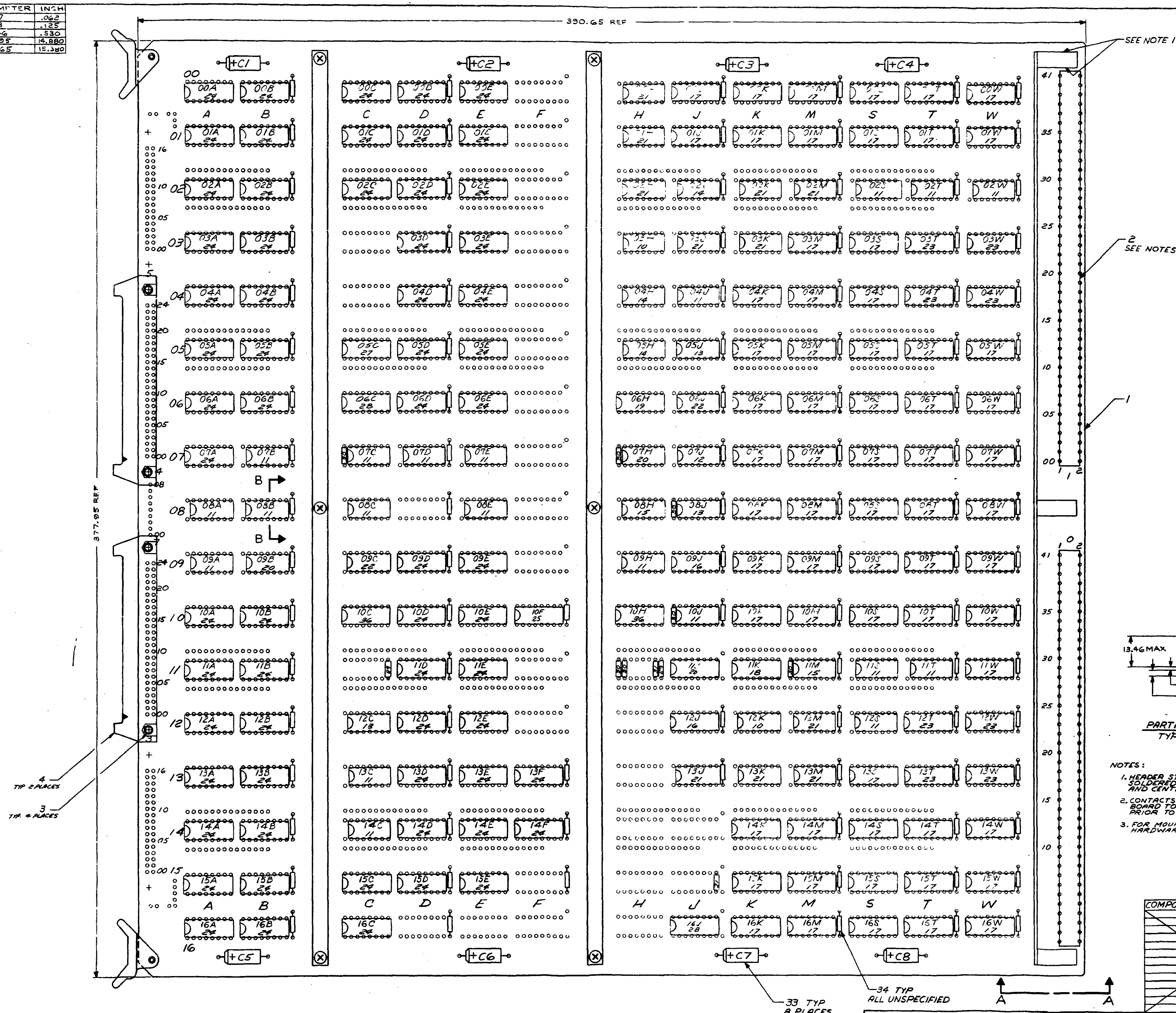
122-3 CSA150
- 13 08A 19-057 SG 12 — A9A — 8A2, 8A7
- 13 08B 19-057 SG 12 — A9B — 8A4, 8A9
- 05C 06 — 470 — 09 07D 19-057 SG 08 — A9C — 7A2, 7A7
- P5 — 06C — 330 — 13 08E 19-057 SG 12 — A9D — 7A4, 7A9

P5
- + C1-C8 15uF 20V
- 0.1uF 101 REQ'D

SEE SHEET 1 CONNECTOR MAP FOR P5 & GRD PINS

SCALE—	NAME	TITLE	DATE	TITLE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	P. CARD	DRAFT	7/8/77	FUNCTIONAL SCHEMATIC 8/32 CPC W/ 2K WCS
		CHK		
		ENGR		
				TASK NO. 03898 SHEET OF
				DWG NO. 35-GG3R01 D08 10 — 10

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530
377.95	14.880
390.65	15.380



REVISIONS

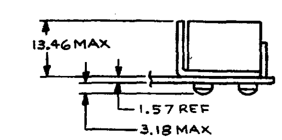
PRE PRODUCTION APPROVAL	INIT DATE DEV PROD

RESISTORS BETWEEN 15J-08 & 15J-09 AND HH-07 [illegible] WERE [illegible]. RESISTOR PACK [illegible] WERE [illegible]. RESISTOR BETWEEN 11C-08 11C-09 WAS LOCATED AT 11C-07 & 11C-10. [illegible] 11-4-77 R01

CHANGED HOLES IN CONNECTORS 2 & 5 AS PER ECR 3607 — 2-24-78 R02

RELEASED FOR PRODUCTION

ADDED [illegible] ADDED ITEM 34 [illegible] — 4953 — 4-7-82 R03



PARTIAL VIEW A-A
TYP 3 PLACES

NOTES:

1. HEADER STIFFENER TO BE SOLDERED TO GND BUS AT 2 ENDS AND CENTER (APP SIDE).
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
3. FOR MOUNTING OF STANDARD HARDWARE SEE 16-642 D12.

METRIC

COMPONENT	REF DESIGNATION

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

NAME	TITLE	DATE
J. HELWATY	DRAFT	7-28-77
W. LIMPERT	CHK	8-5-77
[illegible]	ENGR	2-24-78
R.A. BARKER	Q.C.	2-24-78
N. LEMONDE	MGR.	2-24-78

TITLE ASSEMBLY MULTI-WIRE 8/32 CPC W/2K WCS
03098 — 35-663 [illegible] E03 — SHEET 1-1

* See 8/32 MICRO INSTRUCTION MANUAL PUB# 29-438 Pg 7-8

PERKIN-ELMER

Function select Lines from CPU

138-0 FSEL000 01 07M 19-015 HG 02 — FSEL001 — 2E2, 3C3, 7A7
01 07F 19-057 SG 02 FSL000A — 5A4, 5J5, 6G1
238-0 FSEL010 03 07M 19-015 HG 04 — FSEL011 — 2E2, 3C2, 4B2, 6J1, 7A5
03 07F 19-057 SG 04 FSL010A — 6H1
139-0 FSEL020 05 07M 19-015 HG 06 — FSEL021 — 2E2, 3C2, 4B2, 6J1, 7A5
05 07F 19-057 SG 06 FSL020A — 6G1, 6H1
239-0 FSEL030 09 07M 19-015 HG 08 — FSEL031 — 2E2, 3C2, 4B2, 5B5, 6K1, 7A8, 7K7
09 07F 19-057 SG 08 FSL030A — 5A4, 6A1, 6H1, 7G7, H1
240-0 KSIGO 11 07M 19015 HG 10 — KSIGI — 2E3, 3C2, 4B2, 7A8
11 07F 19-057 SG 10 KSIGOA — 6G1
set's for I/O OP'S (Q)
132-0 CA 3I0 13 07M 19-015 HG 12 — CA3I1 — 2E3, 3C2, 4B2
13 07F 19-057 SG 12 CA3IOA — NC

Pulse output Lines

G4 FSL030A 01 11D 19-015 HG 02 06 1.5μh 11 — 12D — 10 12D 470Ω 07 — 09 12D 220 PF 08 — 03 11D 19015 HG 04 OFSL030 — 7G7

387 B28I 01 00C 19-101 B 02 03 — PA0 (TP) — 100-4
386 B29I 04 00C 19-101 B 05 06 — PB0 (TP) — 101-4
386 B30I 10 00C 19-101 B 09 08 — PC0 (TP) — 102-4
387 B3II 13 00C 19-101 B 12 11 — PD0 (TP) — 103-4

TEST PULSES 1,22 NS

(TOU) GND — 104-4, 112-4, 118-4
10G5 SCATNO — 105-4
14A3 MMEPFO — 107-4, 104-1
14A3 EXBO — 108-4
14A7 KTM — 109-4
14N5 STPIA — 110-4
15K8 GSTPI — 111-4
207-3 LSU — 113-4
14A3 XI — 114-4
211-3 X2 — 115-4
210-3 X3 — 116-4
209-3 X4 — 117-4
5K5 KAI — 119-4
5K4 KBI — 120-4
5H6 KDI — 121-4

P5 16 03E 12.7K — 06 03E 220PF 11 — G01
15 14 — 02E — 01 02 — 13 04 — 19-042 ONE SHOT 1.1μS — 03
7D7 POUTO
13F5 XRPA

04 05 N.C.
02 D DS 03E 19-089 HDFF C DC 01 — 06 GPX0 7H8

T 2 / 1 0 1 / 0 1 2 / 0 1 4

Module Select Lines from CPU

137-0 STRTO — 14B7 7A6
102-1 MSELOOO 01
103-1 MSELO20 02
202-1 MSELO1O
06S 19-055 SG 03 — 02 03 04 05 06 09 10 11 12 13 01 — 08 GSTRTI 2C4, 5E9, 7A7, 7N7
07S 19-062 SG

Made Pulse 7 Wide 1,2

REVISIONS

PRE PRODUCTION APPROVAL	UNIT DEV PROD	DATE

GATE 05H OUTPUT 8, CAP 220PF, RES 470, INDUCTOR MOVED TO SHT 7, DELETED GATE 01K OUTPUT 8, — G M C.J.S 03088-18 — 4-24-75 R01
CHANGED PER MARKED PRINTS. — C.J.S 03088-19 — 4-17-75 R02
ADDED 7N7 TO G8 FSEL030A, 7K7 WAS ADDED TO FSEL031, G4 — C.J.S 03088-29 — 4-18-75 R03
CHANGED: SHEETS 2 & 3. — C.J.S 03088-32 — 4-14-75 R04
CHANGED: SHEET 5 WAS REV. 3. REV: OF BOARD WAS R05. — F.J.S 03088-36 — 4-20-75 R05
CHANGED: SHT 3 & 5 WAS R03, — F.J.S 03088-38 — 4-21-75 R06
SHT 7 WAS R03 — C.J.S 03088-52 — 4-8-75 R07
ADDED 11D AT LOC J1 & M1 AND RESISTOR AT M1, CAP AT L1. CHANGED SHEETS 2 & 14 WERE R02 13 & 4 WERE R00, 3 & 7 WERE R04 & 15 WAS R03 WAS R01 — C.J.S 03088-65 — 4-15-75 R08
CHANGED, SHT 16 WAS R01, SHT 14 WAS R03 SHT 12 WAS R01 — C.J.S 03088-68 — 4-18-75 R09
07M WAS 19-057 REV LEV OF SHT 7 WAS R05 — C.J.S 03088-70 — 4-28-75 R10
REV LEV OF SHT 15 WAS 2 " " " " 14 WAS 4 — C.J.S 03088-75 — 5-2-75 R11
CHANGED: REV OF SHEET 14 WAS 5. — F.J.S 03088-79 — 6-9-75 R12
RELEASED FOR PRODUCTION — ENG. APPR. — DATE 5/12/75
AREA M3, REV LEVEL WAS 35-539 REV. CHG. SHTS 2 & 14. — K.C 2572 — 7-10-75 R13
REVISED SHT 2&6. — K.C 2570 — 8-25-75 R14
REVISED SHTS 1, 5 & 16 AREA J1 & M1, J1 WAS SHEET 19-052, AREA M1, J2D 06-11 15μh, WAS 9.7μh, AREA J1, J2D 08-09 220 PF WAS 1000 PF. AREA R9, 35-539 B16 WAS R15. — K.C 2603 — 9-9-75 R15
REVISED SHTS 4, 6 & 9. REV LEV OF 35-539 WAS R16 — W.S WR2 2890 — 1-15-76 R16
REVISED SHTS 1, 2 & 14. 35-539 WAS R17. — K.C 2752 — 7-14-76 R17
REVISED SHTS 1, 5 & 14 35-539 REV LEV WAS R18 — W.S W 3129 — 3-2-77 R18
REVISED SHTS 1, 2, 3, 5, 6, 7 & 9, 35-539 REV LEV WAS R19. — W.S W 2980 — 3-2-77 R19
REVISED SHTS 1, 2 & 6, 35-539 REV LEV WAS R20 — W.S 3195 — 3-16-77 R20

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

8/32-IOU	35-539R29

(CONT LOWER LEFT)

USED IN MANUAL 29-399

SHEET INDEX	REV	29	6	6	3	8	5	11		4	1		3	2	14	6	4
	SHT NO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

REVISIONS CONT.
REVISED SHT 14 35-539 REV LEVEL WAS R20 — GP W 3267 — 10-12-77 R21
REVISED SHT 7, 35-539 WAS R21. MANUAL NO. ADDED — GP W 3709 M 10-11-78 R24
GP W 3537 — 3-16-78 R22
REVISED SHTS 5, 35-539 WAS R22. — GP W 3797 M 10-11-78 R23
REVISED SHTS 2 & 7, 35-539 WAS R23. — M2 W 3858 M 1-23-79 R26

REVISIONS MADE TO SHT. 15 — M2 W 3872 M 1-22-79 R25
REVISIONS TO SHTS. 9 & 14 — VT W 4543 MS 2-19-81 R28
REVISED SHTS 1, 7, 14, 15, & 16. — KR W 4231 R 3-10-80 R27
REVISED SHTS 1, 5, & 7 — KR W 5304 MS 2-14-83 R29

AREA M5, "MMEPFO" WAS "EXAO" ADDED CONNECTION FROM "107-4" TO "104-1". REVISED SHTS 1 & 14

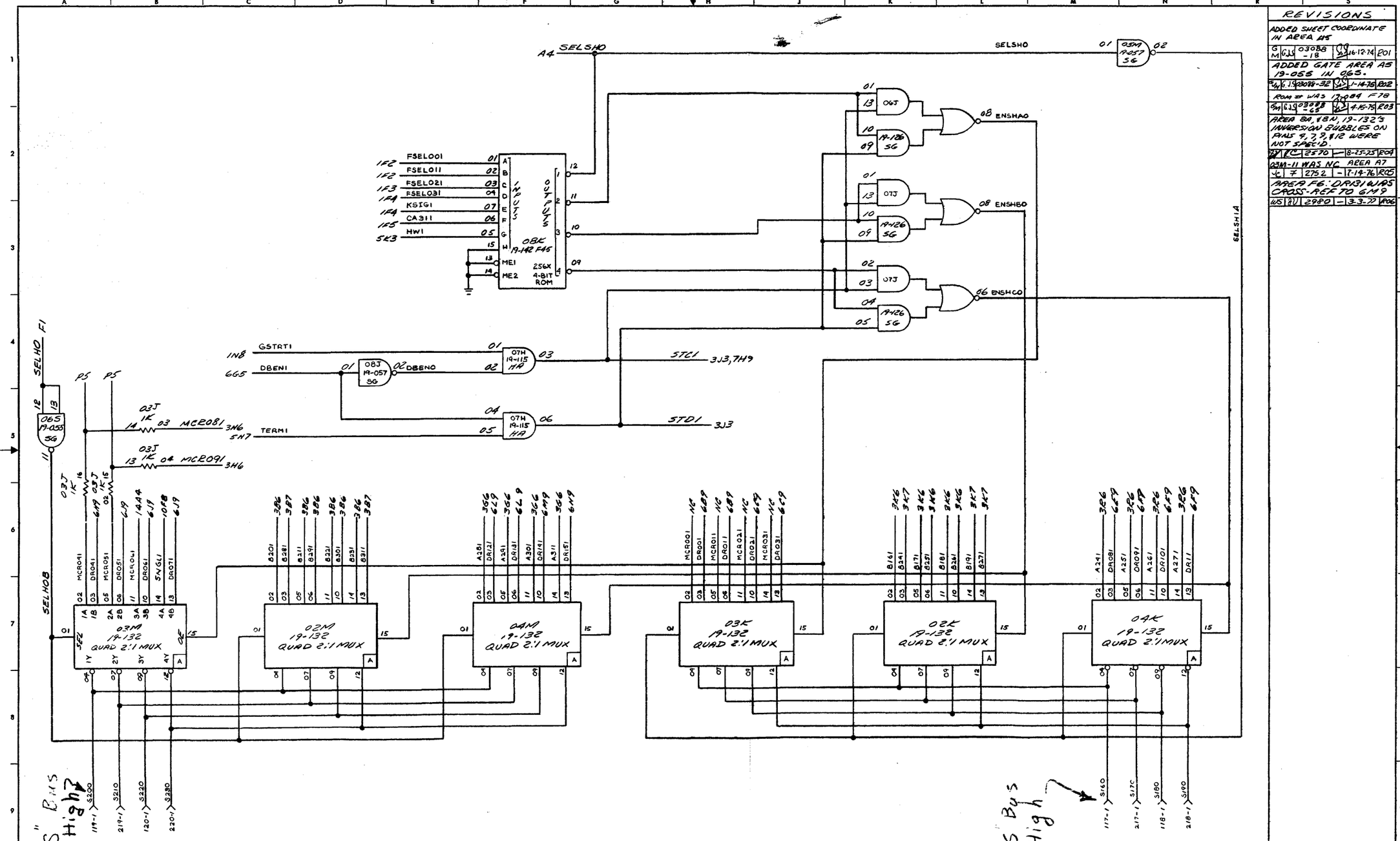
NAME	TITLE	DATE
J. CITRON	DRAFT	9-6-74
G.J. HOMEFIELD	CHK	10-15-74
G. SYROVY	ENGR	11-1-74
S.C. MESSINA	MGR	
R.A. BARKER		

TITLE FUNCTIONAL SCHEMATIC M8/32-IOU
TASK NO. 03088 DWG NO. 35-539R29D08 SHEET OF 1-16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS			
ADDED SHEET COORDINATE IN AREA A5			
G M	GJJ	03088 -18	16-12-74 R01
ADDED GATE AREA A5 19-055 IN 065.			
G M	GJJ	03088-32	1-14-75 R02
ROM # WAS 17-084 F78			
G M	GJJ	03088 -25	4-15-75 R03
AREA 8A, 8N, 19-132'S INVERSION BUBBLES ON PINS 4, 7, 9 & 12 WERE NOT SPEC'D.			
[illegible]	RC	2570	8-25-75 R04
03M-11 WAS NC AREA A7			
JC	7	2752	7-14-76 R05
AREA F6. DRI31 WAS CROSS-REF TO 6M9			
WS	RV	2980	3-3-77 R06



NOTES

NAME	TITLE	DATE
C CUTLER	DRAFT	8-7-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32-10U

TASK NO. 03088
DWG NO. 35-539 R06 008
SHEET OF 2-16

BRUNING 44-231 16042

PERKIN-ELMER

A164: A31Q - "A" BUS CONT
B164: B31Q - "B" BUS CONT

REVISIONS				
ADDED: NEW SHEET LOCATIONS IN AREA M2				
C/M	C.J.	03088-18	6-12-74	R01
ADDED: I19-134 TO AREA D1				
C/M	K.J.S	03088-29	7-9-74	R02
ADDED: 19-057 GATE 08J, LOC E19				
C/M	K.J.S	03088-32	7-24-74	R03
ADDED: GATE 19-055 @ SHT LOC B1, BOARD LOC 14H.				
C/M	K.J.S	03088-38	11-27-74	R04
ROM # WAS 19-082F79				
C/M	K.J.S	03088-65	4-15-75	R05
AREA 01: DELETED GATES AT 12S. DELETED 1K RESISTOR AT 10S016. FOR DREV. REV INFO SEE VOYAGER M1-M4, M-CORY 35-539 008, SHT 3, R05.				
WJS	JJ	2980	3-3-77	R06

NAME	TITLE	DATE
C.CUTLER	DRAFT	8-12-74
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC M8/32-IOU

TASK NO. 03088 SHEET OF 3-16
DWG NO. 35-539 R06 008

NOTES

BRUNING 44-231 16042

PERKIN-ELMER

D BUS 7

REVISIONS				
ROM # WAS 19-089 FBD				
GM	V-1C	03088-65	4-15-75	R01
AREA A9: 19M(21-025 F02) RELOTED CIRCUITRY WAS NOT SPEC'D.				
WS	1A	2994	5-12-76	R02
AREA C2, 08M-19-142 WERE CONNECTED TO GROUND				
GP	1	13799	M	10-11-78 R03

08M 19-142 FA7 4 BIT ROM

11T 19-134 HEX BUF/INV

11S 19-134 HEX BUFF/INV

11M 19-134 HEX BUFF/INV

11K 19-134 HEX BUFF/INV

13S 19-134 HEX BUFF/INV

13T 19-134 HEX BUFF/INV

13M 330Ω 21-025F03

13M 470Ω 21-025F02

"D" BUS

"INFORMATION DISCLOSED HEREIN IS THE PROPERTY OF THE PERKIN ELMER CORPORATION COMPUTER SYSTEMS DIVISION, AND SHALL NOT BE DISCLOSED OR USED FOR ANY OTHER PURPOSES EXCEPT AS SPECIFIED BY CONTRACT BETWEEN THE RECIPIENT AND THE PERKIN ELMER CORPORATION. DUPLICATION OF ANY PORTION OF THIS DATA SHALL INCLUDE THIS LEGEND

NAME	TITLE	DATE
C. CUTLER	DRAFT	8-9-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MB/32-10U
TASK NO. 03088
DWG NO. 35-539 R03 008
SHEET 4 OF 16

NOTES

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
CHANGED PER MARKED PRINTS.				
G/H	G.J.S	03088-19	12-17-74	R02
7K7 WAS 7K3 ON KT1, N5. XRPE WAS FLSYNO, 14K9 CORDINATE				
G/H	G.J.S	03088-29	8-7-75	R03
CHANGED: 19-130 IN POS 12J WAS 19-061.				
G/H	G.J.S	03088-36	11-20-75	R04
AREA H,J&K3, CIRCUITRY BETWEEN 11E-09&03F-06 WAS NOT STARTED				
SY	K.C	2665	8-28-78	EO5
AREA B5: DELETED 06T -01, 02, & 03 WHICH WAS TO HAVE SYNO & XSYNO. AREA A8: ADDED 09J, 06T 1K RESISTOR BETWEEN 09J-01, 16, & RELATED CIRCUITRY. AREA K-3 & B7: 08S WAS SPEC'D AS A 19-118 SG. AREA G8: 12E-07 WAS NC, 12E-09 WAS TO AS. AREA B6: RESISTOR AT 08T WAS 180Ω.				
WS	VT	3129	3-2-77	R06
AREA L2: 09E-05 WAS TO HAVE 1 RPE, CROSS-REF TO 7E8.				
WS	VT	2980	3-3-77	R07
EXTENSIVE CHANGES IN AREAS K2 & B7 FOR PREVIOUS REV LEVELS SEE R07 MICRO-FILM				
VT		4543	2-19-81	R08

NOTES

NAME	TITLE	DATE
C. CUTLER	DRAFT	8-19-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC

M8/32-IOU

TASK NO. 03088 SHEET OF 5-16

DWG NO. 35-539 R08 008

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS			
AREA D2, 19-129 WAS SHOWN REVERSED.			
RC	2570	8-25-75	R01
AREA N1, DRC1 WAS RC1. CORDN SK3 WAS SE7.			
RC	2605	9-9-75	R02
AREAS C4, H4 & J4: REVISED CROSS-REF. TO REFLECT NEW LOCATIONS ON SHT 4			
SK	2894	5-12-76	R03
AREA P1-9: ADDED GATE 06F & RELATED CIRCUITRY. 09M-02 WAS N.C.; 09M-03 WAS TO DR131, CROSS REF. TO 2F6, 3F6, & 7J3.			
SK	2980	3-3-77	R04
AREA H5: ADDED 2 330Ω RESISTORS BETWEEN OPT-02, 15 & OPT-01, 16. AREA N5: ADDED 3 330Ω RESISTORS BETWEEN OPT-01, 16, OPT-01, 16 & 10M-01, 16			
SK	3195	5-16-77	R05

NOTES

NAME	TITLE	DATE
G. MELTON	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC

M8/32-10U

TASK NO 03088

DWG NO 35-539 E025008

SHEET OF 6-16

BRUNING 44-231 18042

PERKIN ELMER

IOU - CONDITION codes to "C" BUS

REVISIONS
ADDED GATE 05H OUTPUT B, GATE 06F OUTPUT, 12,470 RES., 220PF CAP, & 4.7μH INDUCTOR. ADDED MNEMONIC STFO TO J8 AND DSTRTO IN PLACE OF XRPF AND STMBO IN PLACE OF STFO.
G M J.S 03088 -18 — 6-12-74 — R01
CHANGED PER MARKED PRINTS
G M J.S 03088 -19 — 8-12-74 — R02
ADDED TO 14H TO SHEET. 05F09 WAS GOING TO 05F09 NOW TO GSTRT1. 07J10 WAS GOING TO 09F09 NOW TO SCC1. 05F08 NOW GOES TO 14H09, 13E09 IS NOW INFINO WAS KTO. 08E03 WAS GOING TO 08E04 RESISTOR GOING TO 04F15 WAS 10K
G M J.S 03088 -29 — 9-9-75 — R03
09T WAS 19-056
M J.S 03088 -37 — 4-8-75 — R04
14N02 WENT TO FSEL030A ADDED 19-036 TO LOC. M4
G M J.S 03088 -65 — 4-15-75 — R05
13J04 WENT TO 13J05
G M J.S 03088 -70 — 4-23-75 — R06
PAGE P8: DELETED CROSS-REF TO SL7 FROM XRPE PAGE J3: DR13I WAS CROSS-REF TO 6M9.
M S W 2980 -13-3-77 R07
AREA E3 MNEMONIC DMPFO WAS IRLMPO AREA E4 MNEMONIC FWINTO WAS DMPFO
GP JJ 3537 3-16-78 R08
AREA K6 ADDED LOC 4B3
GP JJ 3799 M 10-11-78 R09
AREA G1 08J PINS 02 & 03 WERE REVERSED. AREA G3 06K PINS 02 & 03 WERE REVERSED.
KR JJ 4231 R 3-10-80 R10
AREA E8, DELETED 5J3 FROM SIGNAL XRPE
VT DW 4543 MS 2-19-81 R11

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	9-13-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONING SCHEMATIC

M8/32-IOU

TASK NO. 03088 — DWG NO. 35-539 R11 D08 — SHEET OF 7-16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS

MS NIBBLE TO Display Console

LS NIBBLE TO Display Console LAQ IS XFER STROBE ONPG 13-16

ATSYNO 12N9

4K9 D080 — 14K 19-016 HG — DL001 9D7, 9D4, 10B3, 11B1

4K9 D090 — 10K 19-015 HG — DL011 9D8, 10A3, 11B2

4J9 D100 — 10M 19-015 HG — DL021 9D6, 11B2

4J9 D110 — 10M 19-015 HG — DL031 9D7, 11B2

4H9 D120 — 10M 19-015 HG — DL041 9D7, 11B4

4H9 D130 — 10M 19-015 HG — DL051 9D8, 11B4

4G9 D140 — 10M 19-015 HG — DL061 9F3, 11B4

4G9 D150 — 10M 19-015 HG — DL071 9F5, 11B4

03H 19-015 HG — DL000 9D6

03H 19-015 HG — DL010 9D6, 9B3

03H 19-015 HG — DL020 9B3

10E 19-015 HG — DL030 9B3

10E 19-015 HG — DL040 9B3

10E 19-015 HG — DL050 9B4

DL060 9F4

DL070 9F3

00H 19-134 HEX BUFF/INV — 10N9 DAGB0

02H 19-134 HEX BUFF/INV

12K 19-134 HEX BUFF/INV

12M 19-134 HEX BUFF/INV

13S 19-134 HEX BUFF/INV — 16J5 DU1, 10N3 GRGAO

12K 19-134 HEX BUFF/INV — HB 0V1, 12D1 BRK1

12M 19-134 HEX BUFF/INV — 12E7 BSY1, C7 EX1

1345 FTXO

D080 4K9, D090 4K9, D100 4J9, D110 4J9

D120 4H9, D130 4H9, D140 4G9, D150 4G9

FB LDBRO — 03H 19-015 HG — LDBR1 11F2

12D1 TMGO, 11M7 XLC1 — 02F 19-016 HG — 03H 19-015 HG — BRK1 — BRKO

xEPD 9M3

04E 19-089 D FF — BA1 — 12D6 WRTO, 12N6 EOC1 — 02F 19-016 HG — BA0 12A7

04E 19-089 PS DC — 0V1 J7, 0V0 — C7 LDBRO

13H 19-016 HG — EX1

10N2 DRGAO, 10N4 CMGAO, 15M4 SCLROA — 01F 19-024 HA

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC

M8/32-IOU

TASK NO. 03088 — DWG NO. 35-539 — SHEET 008 OF 8-16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS			
CHANGED PER MARKED PRINTS			
GMK	03088-19	8-12-74	R01
GATES 03D PIN WAS 19-016. FLIPFLOPS AT 08B&00F PIN WAS 19-089.			
JK	2572	7-10-75	R02
AREA B2; MNEMONICS D0606,D070 WERE CROSS-REF. TO ARG			
MB	2844	5-13-76	R03
AREA N3; ADDED 14G2 TO XRPD'			
MB	3858	1-23-79	R04

P/O 12T
19-134
HEX BUFF/INV

E4 DL00X 12 → 11 D0B0 4K9
7E8 XRPE 14 → 13 D1A0 4G9
12M9 ATSYNO 15

4S6 D060 01
4S6 D070 02
8D3 DL010 03
8D4 DL020 04
8D5 DL030 05
8D5 DL040 06
8D6 DL050 11 → 12
11J 19-050 MG → 08 → 05 02J 19-015 MG → 06

8C6 DL061 02
8E7 DL070 04
E2 DL00X 05
05E 19-025 MG → 06 A1

8C2 DL001 09 (x'082') → 10
11 (x'002') 03J

12 → 13
8D6 DL060 09
8C6 DL071 10
05E 19-025 MG → 08 B1 10C3

ADR51 10C3 01 → 02 07G 19-016 MG → 03 ADSYNA0 11B7

6B5 ADR50 01 → 02 02J 19-015 MG

05 → 04 07G 19-016 MG → 06 ADSYNB0 10C7 11B7

XRPD 5N5,7K7,7M6, 14G2
02 04 05 ADA1 10L1
03 05D 19089 DC 06 NC
01

04E 1K 16 P5

12 10 09 ADB1 10L9
05D 19089
11 DC 08 NC
13 SCLR0B 15N3

XRPA 13F5
12 10 09 EBL1 12EB
00F 19063 DC 11 08 NC
13 SCLR0A 15M4

8D2 DL000 04
8D3 DL010 05
03D 19-055 MG → 06 → 09
10 03D 19-055 MG → 08

10N4 CMGA0 03
02J 19-015 MG → 04

8C2 DL001 01
8C3 DL011 02
03D 19-055 MG → 03

02 04 05 ARM1 12A8
00F 19063 DC 03 06 NC
01

CMGA1

8C4 DL031 03 → 04 05 BLK1 NC
01 02D 19064 KDC 02 06 BLK0 16B3
15

8C4 DL041 11 → 10 09 WT1 12A5
13 02D 19064 KDC 12 07 WT0 12A6
14

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8132-10U
TASK NO. 03088
DWG NO. 35-539 ROA 008
SHEET OF 9-16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
CHANGED PER MARKED PRINTS				
M	KJG	03088-19	KJG	8-12-74	R01

NS CMGBO 01 068 19-015 HG 02 — CMGB1 12 072 19-016 HG 11
13F5 XRPA
8C3 DLO11 — 03 DS 03C 19-064 01 — 05 INCR1 NC
8C2 DLOO1 — 02 K DC 0 — 06 INCRO 05 — 9N4 BI 03 — 9J2 ADRS1 04 — 07D 19-017 HG 06
15 — 05 — 03 — 04 — 01F 19-024 HA 06 RST0 13D8
15N3 SCLR0B
09 — 11 — 10 — 07D 19-017 HG 08
103-3 ESNC0
10 — 07C 19-016 HG 08 — 09
03 — 06B 19-015 HG 04
104-3 ESN00
02 — DS 0 1D 19-089 DC 0 — 04 — 05 CATN1 3J6 — 03 — 06 CATN0 — 01
P5 16 00D 1K — SCATN0 1M5
P5 15M4 SCLR0A 02 — 00K 19-115 HA 03
9L4 ADSYNB0 01
16 01D 2.2K
106-3 SSGL1 29 01C 18Ω 40 — SSGL1
12 — 10 — DS 0 1D 19-089 DC 0 — 09 SNGL1 2B6 — 11 — 08 SNGL0
05 — 00K 19-115 HA 04 — 06 DSPLY0 (238-1
39 01C 1000 PF 30
SCLR0A — 15M4

6N5 DA0 03 10K 19-015 HG 04 DA1
6E6 DR0 05 10K 19-015 HG 06 DR1
6N5 SR0 09 10K 19-015 HG 08 SR1
6N5 CMD0 11 10K 19-015 HG 10 CMD1

12D1 TMG0 01 — 9N3 ADA1 02 — 07D 19-017 HG 12 DAGA0 11N7, 11A5, 11A8, 12A2
02 — 01 — 06C 19-016 HG 03 DRGA0 8A9, 11K5, 11B8
05 — 04 — 06C 19-016 HG 06 SRGA0 8J6, 11A7
09 — 10 — 06C 19-016 HG 08 CMGA0 8A9 9D3, 11B8
13 — 12 — 06C 19-016 HG 11 CMGB0 A1, 11B8
02 — 01 — 06C 19-016 HG 03 SRG0 (113-3
05 — 04 — 06C 19-016 HG 06 SRGB0 13B2
09 — 10 — 06C 19-016 HG 08 DRGB0 13A3
9N4 ADB1 12 — 13 — 06D 19-016 HG 11 DAGB0 8E2, 13A2

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32-IOU
TASK NO. 03088
DWG NO. 35-539 R01 000
SHEET OF 10-16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS

13C 19-030 4 BIT SHIFT REG

13D 19-030 4 BIT SHIFT REG

14C 19-030 4 BIT SHIFT REG

14D 19-030 4 BIT SHIFT REG

P/O 12S 19-134 HEX BUF/INV

P/O 12T 19-134 HEX BUF/INV

P/O 00M 19-134 HEX BUF/INV

13H 19-016 HG

06B 19-015 HG

05K 19-025 HA

01H 19-050 HG

09D 19-016 HG

06T 19-036 HPO

08C 19-115 HA

DPS1 09C 19-089

DPS1 09C 19-089

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC

M8/32-IOU

TASK NO. 03088

DWG NO. 35-539 008

SHEET OF 11-16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS			
CHANGED PER MARKED PRINTS			
GM/LS	03088-19	8-12-74	R01
CHANGED 07802 TO DTMG1, 04D GATES WERE 19-016, 078 GATES WERE 19-016			
GM/GJS	03088-68	4-18-75	R02
FLIP-FLOPS AT 08B, PIN WAS 19-089. GATES 09D, P/N WAS 19-055.			
MCR	2572	7-10-75	R03

13B 1K P5

TMG1H (TP) 14R04

10L1,8G7,AA TMG0

10N1 DAGA0

N6 EOCO

GLITCH0

N4 SHFT1

11N7 DTI

16E7 DDI

11M8 XLC0

16E8 DDO

STCLK1

DTMG0

01 TMG0

9N7 WTI

9N8 WTO

WRT1 A6

WRT0 A7,8B8,11A2

16C5 DTMG1

05 WRT1

06 WRT0

8E9 BA0

BSY0

BSY1 8J8

OFBSY0

K5, 11F3 XRPC

P5 13E 1K

CLEST0 R3

11E7 STO

11E7,16B2 TMG1

XRPB 5L8

MTC1

MTA0

MTB0

MTB1

15N3 SCLR0B

CLEST0 E4

CLK1

CLK0 J6

SHFT0 11K6

SHFT1 A2,11B2

FSTPD

L4 CLK0

CNT UP

CNT DWN

LD 4 BIT CNTR

CL

CAR

BOR

T01

EOC1 8B9

EOC0 A2,11E9

ATN0 (232-0

ATN1

ATSYN0 N9

9J7 ARM1

INTR1

9J6 EBL1

RACK0 (237-1

RACK1

DRACK1

GATN0

GATN1

TACK0 (237-1

ATSYN0 A8,8A1,9E2, 11A7

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32-IOU

TASK NO. 03088
DWG NO 35-539 R03 008
SHEET OF 12-16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS					
00E12 WAS GOING TO 00E10					
	WJS	03088-68		18-75	R02

00J 47PF 00J 6.8K
00J 100PF 00J 6.8K
01E 1K
P5
F5
01J
19-0A2
ONE SHOT 100NS
ONE SHOT 200NS
05C 19-017 HG
06B 19-015 HG
02J 19-015 HG
10E 19-015 HG
00E 19-089
00D 19-101 B
01C 19-089
10N7 SRGB0
10N9 DAGB0
10N8 DRGB0
7G1 XRDF
STT1
TXO
TY1
DAGB1, F4
XRPA
FTY1
FTY0
FTX1
FTX0
NC
11A7
DAGB0
DAGB1
GLAB1
K3
XRPA
N3, 1H6, 9J6, 10A2, 19H5, 14J5
XA1
XA0
DRGB1
XC1
XC0
RST0
1063
LB0
LA0
114-3
203-3
SH10
SL00
200-3
206-3
7F9 FWAIT0
WAIT1
102-3
8J5, 11A7

Disp Reg Load Control Signals

SW Reg Sense Signals

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32-10U
TASK NO. 0-3068
DWG NO. 35-539 R02 008
SHEET OF 13-16

BRUNING 44.231 16042

PERKIN ELMER

REVISIONS			
CHANGED PER MARKED PRINTS			
GM KJS	03088-19	8-12-74	R01
ADDED 301 TO FLSYN1			
GM KJS	03088-29	4-9-75	R02
ADDED 714 TO PF1 04B12 WAS PDFFO ADDED 07A TO LOC. B2 04A AT LOC M8 WERE 19-016			
GM KJS	03088-65	4-15-75	R03
GATES 07B WERE 19-016			
GM KJS	03088-68	4-18-75	R04
ADDED DIODE TO 08A07 CHANGED VALUE OF CAP AT 08A06 TO 1MF DELETED STPFO FROM 05C09. ADDED 04F AT L3, ADDED 1 AF AT K3 & 01F AT N9			
GM KJS	03088-75	5-2-75	R05
ADDED: SHT LOC ET 19-115 @ P05 03F.			
GM KJS	03088-79	5-9-75	R06
GATE 03D PIN WAS 19-016.			
JC	2372	2-10-76	R07
AREA A4 - ADDED OFF PAGE NMAN MCR061 TO EXISTING CIRCUIT.			
JC	2752	7-14-76	R08
AREA B2: ADDED 3 1K RESISTORS & RE-LATED CIRCUITRY.			
WS AV	3129	3-2-77	R09
AREA X8: ADDED CROSS-REF TO FLSYNO FROM SL7.			
WS AV	2980	3-3-77	R10
AREA C2, RESISTOR 03B WAS 47K. AREA B2, RESISTOR 07A WAS ADDED TO P5. AREA B3, RESISTOR 04A WAS ADDED TO P5. AREA E2, CAPACITOR 05A WAS ADDED TO GND.			
GP AV	3267	10-12-77	R11
AREA G2: 19-064 WAS 19-124 AREA N4: REMOVED BUBBLE FROM 01F-08			
MR AV	3358	M 1-23-79	R12
AREA E3 ADDED 20-001 TO 03B TWO PLACES.			
KR 77	4231	R 3-10-80	R13

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC

M 8/32 - IOU

TASK NO. 03088

DWG NO 35-539 E/3 008

SHEET OF 14-16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
CHANGED PER MARKED PRINTS				
G.P.	03088 -19		8/12/74	R01
REVERSED THE POLARITY OF DIODES 01B BETWEEN PINS 09 & 08, AND 07 & 10. 04C AT LOC 23 WAS 19-016 (NAND), 04C01 & 02 - CONN. 04C05 & 04 - RES. AT 03A07 WAS 470, DIODE OF #0808 WAS 23-001. 03A06 WAS 47Ω.				
G.P.	03088 -66		4-15-75	R02
03A07 WAS 47Ω RES. 03A11 WAS 160Ω RES.				
G.P.	03088 -95		5-2-75	R03
EXTENSIVE REVISIONS FOR PREVIOUS LEVEL SEE MICROFILM COPY IN FILES.				
G.P.	3787	M	10-11-78	R04
AREA CG: RESISTOR 00A-12.05 WAS 10K. ADDED 1 μf CAP & .1 μf CAP				
M.E.	3872	M	1-22-79	R05
AREAS ES, F9, & JA ADDED 20-012 TO 02B-Q2, 02B-Q3, & 02B-Q4. AREA KS ADDED 20-001 TO 02B-Q1.				
K.R.	4231	R	3-10-80	R06

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32-10U

TAB NO. 03088
DWG NO. 35-539 R06 008
SHEET OF 15-16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
CHANGED PER MARKED PRINTS				
GM	JJS	03088 -19	8-12-74	R01
ADDED ALL OF THE CIRCUITRY COMING OFF OF TMG1				
GM	JJS	03088 -68	4-18-75	R02
AREA C3 & B5, 110 WAS SHOWN AS 19-057.				
GM	RC	2605	9-2-75	R03
EXTENSIVE CHANGES FOR R03 SEE MICRO-FILM COPY.				
KR	ST	4231	R	3-10-80	R04

DRNO 09
DTO 10 12C 19-018 HG 08
TMG1 12 13
11N16 11H7 12F5

118 19-036 HPD
01 02 03 TRNSO

10A 23-001 08 09
TN 122-2
10A 100Ω 07 10
10A 23-001 11 06
P5 10A 23-001 16

102-2 SEND LOOP 204-2

SMD − +

DTI 01 02 12C 19-018 HG 06
DDO 04
BLKO 05
11J7 E8 9N7

05 PISA 10A 1K 15 02
TP 220-2
10A 1K 14 03
10A 1K 13 04
12 10A 23-001 05

TDU 121-2 103-2

110 19-015 HG 05 06
15 4.7μh 02 120

09 110 19-015 HG 08 DTMG1 12A6
14 470 12D 03
13 12D 220PF 04

09A 4.7K 07 10
09A 23-001 08 09
09A 23-001 11 06
09A 4.7K 05 12
02 01 09A 20-001 03 DU1 8J6
P5 16 10B 4.7K
09A 2.2μF 40 29
13 04 09A 4.7K

09B 1500 15 02
03,15C4 PISA
09B 1500 14 03
13 04 09B 1K
EP 120-2 104-2

13 10C 19-015 HG 12
11 10C 19-015 HG 10
01 02 10B 19-016 HG 03 DD1 11G9,12A3
04 05 10B 19-016 HG 06 DDO B3, 11A2,12A3

09A 30 2.2μF 39
07 09B 180 10
P5 16 09B 23-001
09 08 09B 23-001

09B 2.2K 12 05
09B 100 06 11
EN 221-2 203-2

RECEIVE LOOP

LB
TD

GND 222-2
TTY GND 202-2

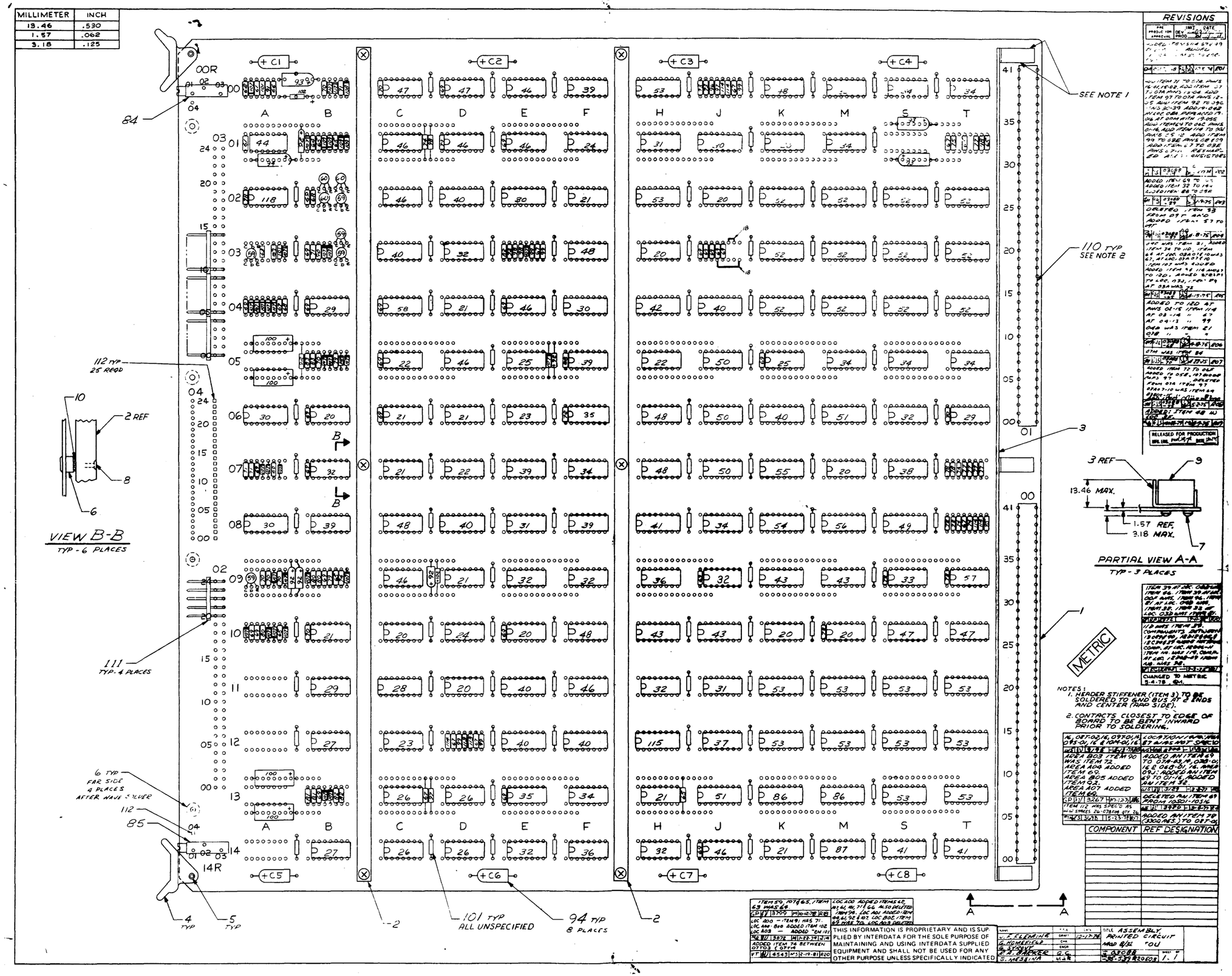
NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32-IOU
TASK NO. 03088
DWG NO. 35-539 R09008
SHEET OF 15-16

BRUNING 44-231 16042

MILLIMETER	INCH
13.46	.530
1.57	.062
3.18	.125



VIEW B-B
TYP - 6 PLACES

PARTIAL VIEW A-A
TYP - 3 PLACES

NOTES:
1. HEADER STIFFENER (ITEM 3) TO BE SOLDERED TO GND BUS AT 2 ENDS AND CENTER (TOP SIDE).
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

COMPONENT	REF DESIGNATION

REVISIONS

PRODUCTION APPROVAL	DEV PROD	DATE
	03	3-7

MODEL REVISING STEP 99
FIRST ALWAYS
ADD ITEM 97 TO C2A ADDS
16.01 FEED ADD ITEM 97
TO C2A ADDS 1.5 C4 ADD
ITEM 97 TO C2A ADDS 12-
05 ALL ITEM 98 TO 99C
AND 30-39 ADD 19.062
AT LOC C2A ADDS 57.7
C4A AT C2A WITH 19.055
ALL ITEMS 49 TO C4C ADDS
0.16 ADD ITEM 118 TO 99C
ADDS 2.5 ADD ITEM
99 TO C8E ADDS 28.559
ADD ITEM 97 TO C3E
ADDS 2.11 REMARK
ED ALL SHEETS

04	18	03 C8B	4-17-74	002

ADDED ITEM 69 TO
ADDED ITEM 32 TO 184
ADJ ITEM 48 TO 99E

05	19	03 C4B	9-25-74	A03

DELETED ITEM 93
FROM C1A ADDS
ADDED ITEM 97 TO
C4F

06	20	03 C2B	4-8-75	004

C4C WAS ITEM 21, ADDED
ITEM 78 TO 110 ITEM
69 AT C8C OBA01 WAS
63, AT C8C 01A TO
ITEM 107 WAS ADDED
ADDED ITEM 118 AND 97
TO C2D, ADDED 57.811
TO C8C, 03A, ITEM 84
AT 03A WAS 24

07	21	03 C2B	4-15-75	A05

ADDED TO 120 AT
AREA 04-15 ITEM 114
AT 03-14 " 67
AT 04-13 " 99
DASH WAS ITEM 21
03B " "

08	22	03 C2B	4-8-76	006

03A WAS ITEM 84

09	23	03 C2B	7-27-76	007

ADD ITEM 72 TO C4C
ADDED 19.058, 101.008
AND 97 DELETED
FROM 01A ITEM 97
03A 7-10 WAS ITEM 69

10	24	03 C2B	12-2-76	A06

ADDED ITEM 48 AT
LOC 46.

11	25	03 C2B	4-28-77	007

RELEASED FOR PRODUCTION

ITEM 39 AT LOC. C8B ADDS
ITEM 96, ITEM 39 AT
C8A ADDS ITEM 96, ITEM
81 AT LOC. C4B ADDS
ITEM 39, ITEM 39 AT
LOC. C3B ADDS ITEM 81.

12	26	03 C2B	12-5-77	010

1/2 DATE 1/80 ITEM 39
COMMENTS, ON ITEM
39 ADDS 90, ITEM 96
ADDS 81, ITEM 81 ADDS
COMP. AT LOC. 1800 AND
ITEM 90 ADDS 118, COMP.
AT LOC. 12 ADDS 118 ITEM
118 ADDS 39.

13	27	03 C2B	12-5-77	010

CHANGED TO METRIC
5-4-78 SM

COMPONENT	REF DESIGNATION
16 DIP-02/16, 09701/A	LOC 1700 AT 4.00, ITEM
018-01, 16 A 1049-01/16	87 ADDS NOT SPECIFIED
GP 13/7 3278	4-78 Mod 2000 FOR 1/80
AREA B03 ITEM 90	ADDED AN ITEM 69
WAS ITEM 72,	TO C2A AS IN 018-01
AREA A04 ADDED	16, 040-01, 16, AREA
ITEM 69,	095, ADDED AN ITEM
AREA B05 ADDED	69 TO C2A, ADDED
ITEM 92,	AN ITEM 36.
AREA A07 ADDED	4/31/78 3789
ITEM 60.	
GP 13/7 3267 Mm 12-7-78	DELETED AN ITEM 69
ITEM 112 WAS SPEED AS	FROM 10201-1016
MM 61 3078 115-33-78	4/31/78 3790
MM 61 3078 115-33-78	ADDED AN ITEM 78
	(300 MS) TO 017-01

ITEM 59, 107 65, ITEM 63 WAS 64	LOC A00 ADDED ITEMS 62, 80, 61, 70, 66, ALSO DELETED
GP 13/7 3759 MM 10-12-78 RB	ITEM 98, LOC A01 ADDED ITEM 99, 61, 92 & 107, LOC B02, ITEM 69 TO 98, 72 & LOC C03 DELETED
LOC A00 — ITEM 9, WAS 71, LOC A00 B00 ADDED ITEM 102	
LOC A03 — ADDED "DM 10"	
16 W 3078 MM 11-22-79 JM	
ADDED ITEM 74 BETWEEN 07703 & 07778	
VT 13 4543 MS 2-19-81 RDO	

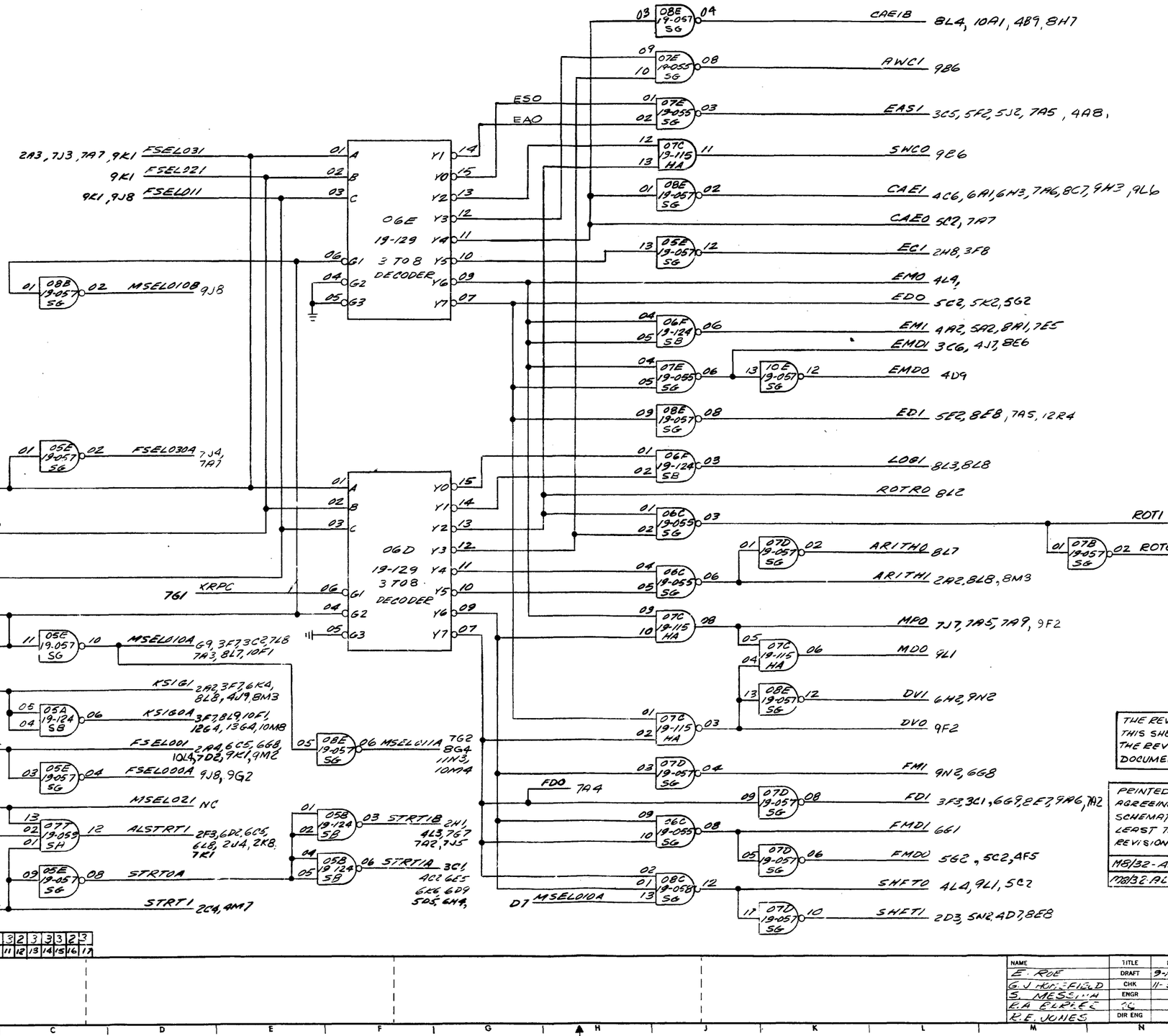
NAME		DATE
V. F. FLEMING	DRAFT	10-17-74
G. HOMEFIELD	CHK	
G. STOWE	ENGR	
C. F. BARKER	Q.C.	
S. MESSINA	MGR	

TITLE ASSEMBLY PRINTED CIRCUIT MOD 8/32 TOU

07088

SIZE D — 8-537220608 — SHEET 1 OF 1

PERKIN ELMER



THE REVISION LEVEL OF THIS SHEET IS CONSIDERED THE REV LEVEL OF THIS DOCUMENT.

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

M8/32-ALU	35-538R16
M8/32-ALU	35-538F0/R12

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	ACM	11-5-74
PROD		

KS1G0A AT D7 WAS GOING TO 05E06. ADDED 7G2 TO MSEL011A AT G8 ADDED 8M3 TO ARITH1 L6.

6M | ED | 030888-22 | 1-24-75 | R01

CHANGED: SHT 6 WAS R01 REV.

6M | ED | 030888-25 | 2-27-75 | R02

CHANGED SHTS 2, 4 & 8 TO R02, SHT 6 TO R03

6M | ED | 030888-8 | 4-8-75 | R03

RELEASED FOR PRODUCTION

REV LEV OF SHT 4 WAS R01 " " " " / " R03 " " " " 5 " R01 " " " " 7 " R01 " " " " 6 " R03 " " " P.C. BOARD REF IN LOC. RG WAS R03

6M | WN | 2524 | 5-29-75 | R04

REVISED SHT. 2. 8/32 ALU, 35-538, WAS R06

PE | WN | 2576 | 1-18-76 | R05

REVISED SHT. 14. CHANGED REV LEV OF SHT 14 WAS R01

WTA | JF | 2939 | 9-7-76 | R06

REVISED SHTS 2 & 9. 8/32 ALU, 35-538 WAS R07 M8/32 ALU 35-538 ALL R06

WS | JF | 3017 | 10-4-76 | R07

REVISED SHT 2. REV. LEV. OF M8/32-ALU & M8/32 ALU WAS R06, R04

PM | WN | 3170 | 4-5-77 | R08

REVISED SHT 2 REV LEVEL OF M8/32-ALU & M8/32-ALU (FC1) WAS R09 & R05 RESP.

GP | JJ | 3260 | 5-5-77 | R09

AREA B5 ADDED MANUAL TABLE. AREA R9 35-538 WAS R10 & 35-538F01 WAS R06 REVISED SHT'S 4, & 10 THRU 17.

PM | DJ | 3507 | 3-15-78 | R10

REVISED SHT 6, AREA R9 35-538 & 35-538F01 WERE R11 & R07 RESP.

GP | JJ | 3723 | 8-7-78 | R11

REVISED SHT 9

GP | JJ | 3769 | R | 10-16-78 | R12

AREA M7 ADDED 9F2 TO MP0 " L8 " " " DV0 AREA N9 35-538 & 35-538 F01 WERE R12 & R04

BP | DJ | 3932 | R | 5-29-79 | R13

AREA D8 SIGNAL FSEL000A CROSS REF WERE 9J8, 7N2, 9G2 AREA R9 35-538 WAS R14, 35-538 F01 WAS R10. REVISED SHT 9. AREA D8 ADDED 10L4 TO FSEL001

KR | DJ | 4132 | M | 8-30-79 | R14

AREA G9 LOCATOR 6H9 WASN'T CLEARLY WRITTEN. REVISED SHTS 1, 3, 6, 7, 15, 17

KR | DJ | 4231 | R | 3-4-80 | R15

REVISED 1, 11, 13

JAT | DJ | 4652 | M | 4-6-81 | R16

SHEET INDEX	REV	16	6	2	3	2	7	3	2	6	2	3	2	3	3	3	2	3
	SHT NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	9-16-74
G. J. HUNSFIELD	CHK	11-5-74
S. MESSINA	ENGR	
R. A. ELPLEE	PE	
R. E. JONES	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC M8/32 - ALU

TASK NO. 0.2.0.3.8 | SHEET OF 1 / 17

DWG NO. 35-538 R16 D08

BRUNING 44-231 16042

Oceanport N J 07757

REVISIONS

ADDED DIODE RESISTOR CAPACITOR & COIL TO 09B08 & 09N01 & 02 IN AREA 5C, CCCLKO WAS GOING TO E3, 07U15 WAS GOING TO 06U15. 07K06 WAS GOING TO GATEEC1 3F7, 07K10 & 05 WERE GOING TO 05H12, 09F13 WAS GOING TO 07E12 & 05H05. 05H06 & 04 WERE NC, 09E10 WAS GOING TO BGTR0 & 02. 07E12 WAS CCLKO. ADD OCTO 09E10

GM	KD	03088 -22		1-24-75	ECN

CCCO WAS MSIGO
MSIGO WAS CCCO
07W WAS 19-056
07E12 WENT TO 05H04
05H12 WENT TO CCCLKO
05H06 WENT TO 07K05

PM	KD	03088 -27	KD	4-8-75	ECO2

AREA C6: CAP 04A WAS 100 PF.

EC	PM	2576	-	7-18-75	R03

AREA M2: 08T-03, 06, 10 & 13 WERE NC. 08T-01 WAS TO GND.

WS		3019	-	10-14-76	R04

AREA F5, ADDED 05M, 100pF
30-018, 04 WAS N.C.
AREA F6, 30-018, 13 WAS N.C,
30-018, 05 WENT TO 09F-13,
30-018, 12 WENT TO 07K-05

PM	KD	3170		4-25-77	R05

AREA E6:
05H 04 DELETED CAP. 05H 100pfs.
05H 13 WAS CONNECTED TO 09F 13.
05H 05 WAS CONNECTED TO 07K 05.
05H 12 WAS N.C.

G.P	KD	3260	-	8-5-77	R06

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	9-18-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32 ALU

TASK NO. 03088
DWG NO. 35-538 R06 D08
SHEET OF 2-17

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
ADDED BSO TO 08M04 DELETE IC 19-057 09E IN AREA F6. ADD 19-127 IN SAME SPOT & ADD 19-058 AT E5, 09M05 WAS GOING TO 09H02, ADD GATE 01C AT D7, OBJ09 WENT TO 09M06 AND GATE EC1 2N8, OBJ10 WAS EC1 1L3 ADDED GATE 19-115 TO F8.
GMD 03088 -22 MS 1-24-79 R01
AREA J7 08J WAS 19-082-SG0.
KR 4231 R 3-10-80 R02

6F8 FSTCNT1 13
7H4 SAPO 02
6N6 ACLK1 01
10D 19-058 SG 12
12D 19-055 SG 04 05 06
12D 19-058 SG 04 03 06
1L8 FDI
1F9 STRTIA
DFLT0 2G6
DFLT1 NC
AF2 0FLI
07M 19-082 SG0
07M 16 330Ω P5
08M 19-057 SG 01 02
1D7 MSELO10A
5K8 AS001
9L9 ALOG0
09E 19-053 SA 12
6E3 AXB1
10K4 S001
09M 19-127 XOR 03
BS0 B7
1L8 FDI
10L4 ESUM0
SBGTR1 6C1
2H7 GATECC1
08K 19-082 SG0
10C1 BG001
9L4 SUM1
09K 19-027 XOR 06
7A3 AS1GN0
08M 19-057 SG 05 06
SVCC0 2H3
1L2 EAS1
1D5 FSELO30A
6D1 BGTR1
10B 19-058 SG 06
A6S UFLI
10L4 ESUM0
6E3 AS1GN1
1L2 EAS1
1L4 EMD1
6E3 AXB1
09H 19-126 SG 06
01 02 00D 19-127 XOES 03
X:S1GN1 10L2
10L4 ESUM0
4F6 UFLO
1F8 MSELD1
09E 19-053 SA 06
AK4 S1G1
1D7 KS1G1
08J 19-062 SG
SLCC0 2H2
SBCC0 2H1
10L4 ESUM0
4F6 UFLO
10D 19-058 SG 06
G4 AS1GN0
F3 BS0
01C 19-055 SG 06
09M 19-127 XOR 06
9F9 COUT000
09J 19-115 SA 11
10L4 EC1

NOTES

NAME	TITLE	DATE	TITLE
E. ROE	DRAFT	9-14-78	FUNCTIONAL SCHEMATIC M8/32 ALU
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03088
			DWG NO. 35-538 R02 D08
			SHEET OF 3 -17

BRUNING 44-231 16042

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

ADDED 10H4 TO 13D12 13D02 WAS SOFLO BJ7 NOW HAS ADDED 01C & 05E. 11E09 WENT TO 11E10, 06K05 WAS KSIG1 107. ADDED IC GATE TO LOCATION U9			
GM	03088-22	1-24-75	R01
ADDED FSX010 TO 10E02 07W WAS 19-056			
GM	03086-57	4-8-75	R02
AREA F1 REMOVED 10H4 FROM OFL1. AREA F2 10J4 WAS 7J2.			
PM	3507	3-15-78	R03

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MB/32 ALU

TASK NO. 03088
DWG NO. 35-538 R03 D08
SHEET OF 9-17

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IC GATE 11D AT LOC. 2J WAS 13C, 19-058.				
SM	SD	03088-22	5-23-75	E01
07A05 ADDED AS01 TO SMT 7C8, 07A09 ADDED ASB1 TO 7C8.				
SM	VEN	2522	5-23-75	E02

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32 ALU

TASK NO 03088
DWG NO 36-538 FUNDOB
SHEET OF 5-17

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division

REVISIONS

ADDED STRAP BETWEEN PINS 100-7 & 101-7 AT 5C. PINS " " WERE ADDED 16C14 WENT TO 16C15

DELETE R 15A 09-08, 14A13 14A09, 12A09, 10 F11 AND 15A09 WERE CONNECTED. 1C GATE 15B WAS ADDED BETWEEN 14A06 & 12D04. 14A06 & 11 WERE NC. ADD TAP 103-6 TO 12A09

GM	KD	03088-28	1-24-75	R01

CHANGED: DEL. LINE @ 10C 14A WAS 30-031, 100Ω RES ON PIN 14A14 WAS 51Ω.

GM	KD	03088-25	1-29-75	R02

07W WAS 19-056, ADDED NOMA TO 14A12.

GM	KD	03088 - 28	MB 4-8-75	R03

15C14, 7D8 WAS 7A7

BM	WCH	2522	— 5-29-75	R04

AREA H5 14A-08 WAS CONNECTED TO 15B-13.

GP	GV	3723	8-7-78	R05

AREA E3 ADDED 9GI TO ASIGNI

BP	GV	3932	M 5-22-79	R06

AREA E3 SIGNAL ASIGNI LOOKED LIKE AGIGNI. AREA F9 LOCATOR 7F9 WAS NOT SPEC'D ON SIGNAL FSTCNTO.

KR	GV	4231	R	3-6-80	R07

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

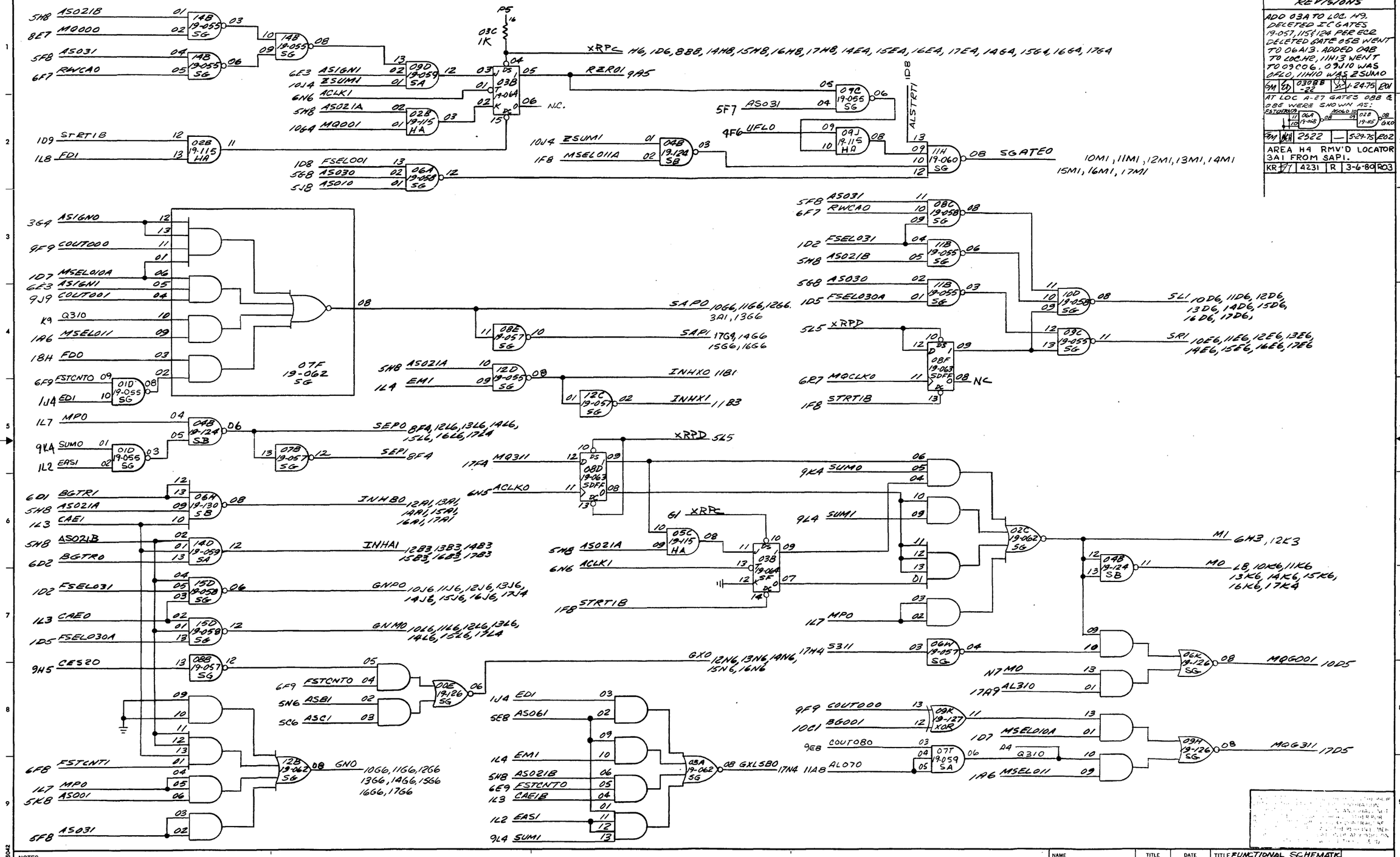
TITLE FUNCTIONAL SCHEMATIC
M 8/32 ALU

TASK NO. 02088
DWG NO. 35-539 R07D08
SHEET OF 6 - 11

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
ADD 03A TO LOC. H9. DELETED IC GATES 19-057, 115 & 124 PER ECR. DELETED GATE 05B WENT TO 06A13. ADDED 04B TO LOC. H2, 11H13 WENT TO 09C06. 09J10 WAS OFLO, 11H10 WAS ZSUMO
SM / ST / 030888 -22 / — / 4-24-75 / E01
AT LOC A-E7 GATES 08B & 08C WERE SHOWN AS: 5370/2109 — 06A 19-058 — 08B 19-055 — 08 GXO
SM / JKH / 2522 / — / 5-29-75 / E02
AREA H4 RMV'D LOCATOR 3A1 FROM SAPI.
KR / ST / 4231 / R / 3-6-80 / R03



NOTES

NAME	TITLE	DATE	TITLE: FUNCTIONAL SCHEMATIC
E. ROE	DRAFT	9-18-74	M8/32 ALU
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03088 — SHEET OF 7-17 — DWG NO. 25-538 803 D08

BRUNING 44-231 16042

Computer Systems Division
Oceanport N J 07757

REVISIONS
03W01 WAS XRPC, 03W09 WAS AS020. ADDED GATES 19-126 19-057 & 055 AT LOC NAME F3
GM 6D 03088-22 SJ 1-24-75 E01
09S02 WAS GOING TO 06W12, ADDED IC 07T TO LOC. R4, ADDED 000 TO LOC. F6
GM 6D 03088-57 MB 4-8-75 E02

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32 ALU

TASK NO. 03088 SHEET OF 8-17
DWG NO. 35-538 R02 D08

BRUNING 44-231 16042

PERKIN-ELMER
Computer Systems Division

REVISIONS					
ADDED 2J3 ON TO 2L060					
GM	KD	03088-22		5-24-78	E01
ADDED TO 04D06 CE520					
GM	KD	2522	-	5-29-75	R02
AREA M8: ADDED 2R2 TO 7L06, 1.					
WS	F	3019	-	10-19-76	R03
AREA J2, 05D WAS 19-087.					
GP	WI	3769	R	10-16-78	R04
AREA J2, 05D-01 WAS BSIGNI & TERMINATED AT GE3. 05D-02 WAS ASIGNI & TERMINATED AT GE3. AREA G2 GATES 01C & 02A ASSOC'D CONNECTIONS WERE NOT SPEC'D.					
BP	AV	3932	M	5-23-79	R05
AREA FGH2 ADDED CHIP 00D TO 02A-10 WHICH WAS CONN TO 02A-01 & 02. & 02A-09					
KR	AV	4132	M	8-30-79	R06

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32 ALU

TASK NO. 03088
DWG NO. 35-538 E06 D08
SHEET 9 OF 17

BRUNING 44-231 16042

REVISIONS

DELETED R AT U1, DELETED GATE 19-115 AT G1, SETZAO WENT TO 11G4. ADDED R'S TO L7. ADDED GATE 13W AND RESISTORS, 12T & 11T TO LOC 14. 13T01 WENT TO MSEL011A. ADDED GATE 02B TO M4. ADDED I C's 19-057, 19-056, 19-124 AT LOC M7 & R8. ADDED RESISTOR AT R8. ICs WERE 19-056 AT LOC H11, 2 & 3

PM		03088 -22		1-24-75	R01

EXTENSIVE CHG'S MADE FOR CHG'S SEE R01 MICRO-FILM

PM		3507		3-15-78	R02

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCT. SCHEMATIC M8/32 ALU

TASK 03088 DWG 35-538R02D08 SHEET OF 10-17

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
ADDED RESISTORS AT L7, 13A01 WAS MSEC01IA SETZA0 WENT TO 10G4 I.C.'s AT LOC U1,2&3 WERE 19-056			
BM	03088-22	11-24-75	R01
AREA K9 MNEMONIC ZSUM1A WAS ZSUM1.			
BM	3507	3-15-78	R02
AREA D2 - AM0D031 WAS AM0D031 AM0D021 WAS AM0D121. AM0D011 WAS AM0D111 AM0D001 WAS AM0D101			
JAT	9V	4652	M2 4-6-81 R03

7H4 INHX0 — 129-0 B040 — 229-0 B050 — 130-0 B060 — 230-0 B070 — 7H5 INHX1 — 109-0 A040 — 209-0 A050 — 110-0 A060 — 210-0 A070 — ASELA0B 8R6 — BA2 BA3 BA3 BA3 — BG041 BG051 BG061 BG071 BA2 — 16W 19-066 2TO1 MUX — 9J7 AM0D031 — 9J7 AM0D021 — 9K7 AM0D011 — 9K7 AM0D001 — 14K 19-067 4 BIT ALU — F3 F2 F1 F0 A=B Cq+4 — GO41 9C4 — PO41 9C4 — 10G7 SETZA0 — 12M 19-125 SBO — ZSUM1A 10J4 — SGATZD 7H2 — 8L4 XS041 — 8L4 XS051 — 8L3 XS061 — 8L3 XS071 — 13M 19-132 QUAD 2:1 MUX — S040 119-0 — S050 219-0 — S060 120-0 — S070 220-0 — XSSEL1 10N4 — ANB ALOG1 9E8 COUTOB0 — XRPB 6F3 — 16M A 19-072 4 BIT L/R SHIFT REG — MQ031 12D5 — MQ061 NC — MQ051 NC — MQ041 10R5 — S071 12A6 — S061 NC — S051 NC — S041 10A6 — AS030 5G8 — SRI 7N4 — GMO 7E7 — SAPO 7H4 — ALO81 12A9 — S081 12A4 — GNPO 7E7 — 1MO 7N7 — ALO31 10A9 — S031 10H4 — GNMO 7E7 — 16K 19-132 QUAD 2:1 MUX — 15K 19-132 QUAD 2:1 MUX — 13K 19-132 QUAD 2:1 MUX — P5 — 08 14M 09 — 12M 16 — 07 14M 10 — 14K 16 — 470Ω — 6N4 ALCLKA0 09 — 15M7 19-131 QUAD D FF — 1 0 1 0 1 0 1 0 — 7K9 8L7 ALO70 — NC ALO60 — ALO71 12R4 — ALO61 NC — ALO51 NC — ALO41 10H6

NOTES

NAME		TITLE	DATE
		DRAFT	
		CHK	
		ENGR	
		DIR ENG	

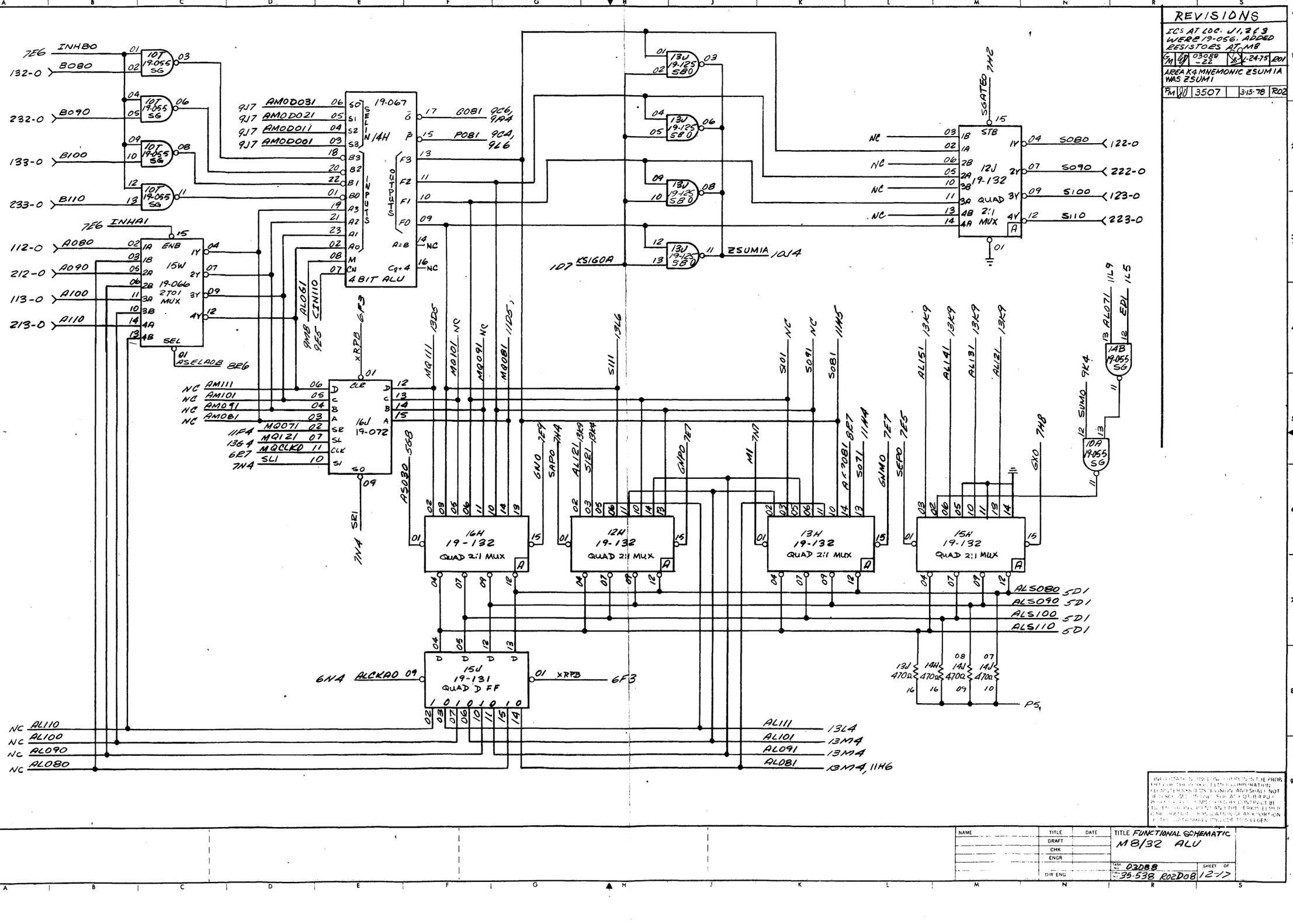
TITLE FUNCTIONAL SCHEMATIC
M8/32 ALU
TASK NO. 03088
DWG NO. 35-538 P03 D08
SHEET OF 11-17

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

ICs AT LOC. J1, 2 & 3 WERE 19-056. ADDED RESISTORS AT M8				
SM	VJ	03088 -22	2-24-75	E01
AREA K4 MNEMONIC ZSUM1A WAS ZSUM1				
SM	VJ	3507	3-15-78	R02



NOTES

BRUNING 44-231 16042

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32 ALU

TASK NO. 03088 SHEET OF
DWG NO. 35-538 R02D08 12-17

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
ICS AT 10B, 11, 2F & WERE 19-056. ADDED RESISTORS AT N18				
SM	03088 -22		1-24-79	2DW
AREA K4 MNEMONIC ZSUMIA WAS ZSUMIA. AREA K4 ADDED RES. 11T & 12T				
PM	3507		3-15-78	R02
AREA D2: AMOD001 WAS AMOD007				
JAT	4652	MS	4-6-81	208

7E6 INNIBO
134-0 B120
234-0 B130
135-0 B140
235-0 B150
09W 19-055 SG
7E6 INHAI
114-0 A120
214-0 A130
115-0 A140
215-0 A150
14W 19-066 2TO1 MUX
ENB
SEL
01 ASELA08 8F6
9J7 AMOD031
9J7 AMOD021
9J7 AMOD011
9J7 AMOD001
19-067 14E
SELIN INPUTS
OUTPUTS
A=B
C2+4
4 BIT ALU
17 G121 → 9C6, 9A3
15 P121 → 9C3, 9C6
ALOG1
9H8 9E5 SIN150
6F3 XRPB
NC AM151
NC AM141
NC AM131
NC AM121
12F4 MQ111
14G4 MQ161
6R7 MQCLKO
7N4 SR1
4 BIT L/R SHIFT REG
19-072 16F
MQ151 14D5
MQ141
MQ131
MQ121 12D5
7N4 SR1
ASO30 5G8
GNO 12F5
SAPO 7N4
AL15L 14H5
S151 14L6
GNPO 7E7
MO 7N7
S111 12F4
GNMO 7E7
SEPO 7E5
S141 NC
S131 NC
S121 12H6
AL191 14K9
AL181
AL171
AL161
AL151
AL141
AL131
AL121
AL111
AL101
AL091
AL081
GXO 7H8
16E 19-132 QUAD 2:1 MUX
12E 19-132 QUAD 2:1 MUX
13E 19-132 QUAD 2:1 MUX.
15E 19-132 QUAD 2:1 MUX
16F 19-131 QUAD DFF
6N4 ALCLKAO 09
01 XRPB → 6F3
13F 19-125 SBD
1D7 KSIGOA.
ZSUMIA 10J4
P5
12T 01 100Ω
11T 08 150Ω
7H2 SCATEO
12F 19-132 QUAD 2:1 MUX
NC
S120 → 12A-0
S130 → 22A-0
S140 → 12B-0
S150 → 22B-0
13F 470Ω 14E 470Ω 14F 470Ω 14F 470Ω → P5
8L9, 5D2 AL150
AL140
AL130
AL120
AL151 → 12L4, 14L4
AL141 → 12M4, 14M4
AL131 → 12M4, 14M4
AL121 → 12N6, 12M4, 14M4

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M832 ALU
TASK NO 03088
DWG NO 35-538 R03 D08
SHEET OF 13 17

BRUNING 44 231 16042

REVISIONS

	ICs AT LOC U1,2&3 WERE 19-056, ADDED RESISTORS TO AREA M8, 01E13 WENT TO AL191.			
FM	03088 -22		6-24-75	R01
	RESISTOR 03F 470Ω IN AREA M8 WAS 00E 470Ω			
WA	7 2934	-	9-7-76	R02
	AREA K4 MNEMONIC ΣSUMIB WAS ΣSUMI			
PM	3507		3-15-78	R03

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

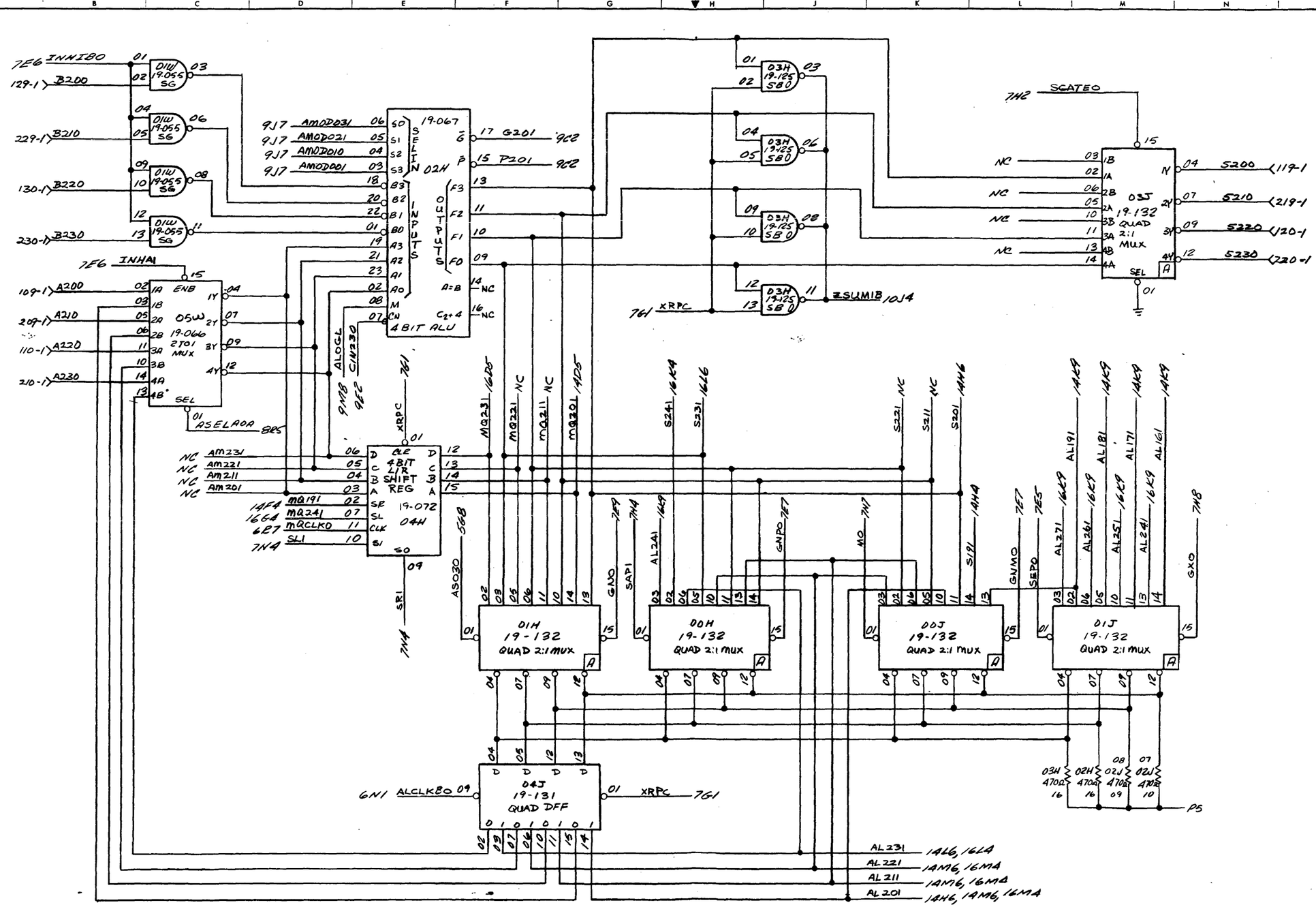
TITLE FUNCTIONAL SCHEMATIC
M8/32 ALU

TASK NO. 03088 SHEET OF
DWG NO. 35-538 R03 D08 14-17

BRUNING 44-231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
ADDED RESISTORS IN LOC M8, ICS IN LOC U1, 2 & 3 WERE 19-056				
PM	LD	03088 -22	SCN-2475	E01
AREA K4 MNEMONIC ZSUMIB WAS ZSUMI				
PM	DT	3507	3-15-78	R02
AREA E6 RMV'D BUBBLE FROM 09H-09.				
KR	AT	4231	R 3-10-80	R03



NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32 ALU

DWG NO 03088
REV 35-538R03D08
SHEET OF 15-17

BRUNING 44-231 16042

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

ICs AT LOC. U1, 2 & 3 WERE 19-056, RESISTOR ADDED AT M8.				
SM	SD	03088 -22	11-24-75	R01
AREA K4 MNEMONIC ZSUM1B WAS ZSUM1.				
PM	DV	3507	3-15-78	R02

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NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32 ALU

TASK NO. 03088 SHEET OF
DWG NO. 35-538 R02 D08 16 17

BRUNING 44 231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
ICs AT J1, 2 & 3 WERE 19-059. ADDED 2 RESISTORS AT J4.
PM | GD | 030888-22 | 11-24-78 | R01
AREA K4 MNEMONIC ZSUM1B WAS ZSUM1, 04S WAS 180Ω & 05S WAS 220Ω.
PM | 3507 | 3-15-78 | R02
AREA K8 RMV'D LOCATOR 7L8 FROM SIGNAL AL311.
KR | 4231 | R | 3-6-80 | R03

INHB0 7E6
B280 134-1
B290 234-1
B300 135-1
B310 235-1
00W 19-055 SG
4D8
INHA1 7E6
4D7
A280 114-1
A290 214-1
A300 115-1
A310 215-1
19-066 2T01 MUX
ENB
04N
ALOG1 CH310
9N8 9B9
XRPC 761
05S
AM311 889
AM301 888
AM291 888
AM281 888
MQ271 16FA
MQG311 7L8
MQCLK0 6L7
SLI 7N4
19-072 4BIT LTR SHIFT REG
SR1 7N4
AS030 5G8
AMOD031 9J7
AMOD021 9J7
AMOD011 9J7
AMOD001 9J7
BG281
BG291
BG301
BG311
19-067 02S
SEL IN
3-STATE OUTPUTS
4-BIT ALU
G 17 G281 9C1
P 15 P281 9C2
F0 13
F1 11
F2 10
F3 09
A=B 14 NC
Cn+4 16 NC
Cn 07
M 08
A0 02
A1 23
A2 21
A3 19
B0 01
B1 22
B2 20
B3 18
761 XRPC
04S 19-125 SB 0
ZSUM1B 10J4
7A2 SGATE0
STB 02W
19-132 QUAD 2:1 MUX
SEL A
NC
S280 124-1
S290 224-1
S300 125-1
S310 225-1
P5
04S 100Ω
05S 150Ω
470 00T
470 01T
470 00W
470 01W
MQ031 MQ021 MQ011 MQ001
GXLSB0 7H8
035 19-132 QUAD 2:1 MUX
015 19-132 QUAD 2:1 MUX
005 19-132 QUAD 2:1 MUX
037 19-132 QUAD 2:1 MUX
04T 19-131 QUAD D FF
ALCLK B0 6N1
XRPC 761
AL310 7M8,8L2,8L9
AL311 2A1,16L6
AL301 16M6
AL291 16M6
AL281 16N6,16M6
GND0 7E7
SAP1 7H4
AGL811 8H8
S811 7L8
MO 7H7
S801 NC
S291 NC
S281 16M6
S271 16M4
GNM0 7E7
SEP0 7E5
AL271 16K9
AL261 16K9
AL251 16K9
AL241 16K9

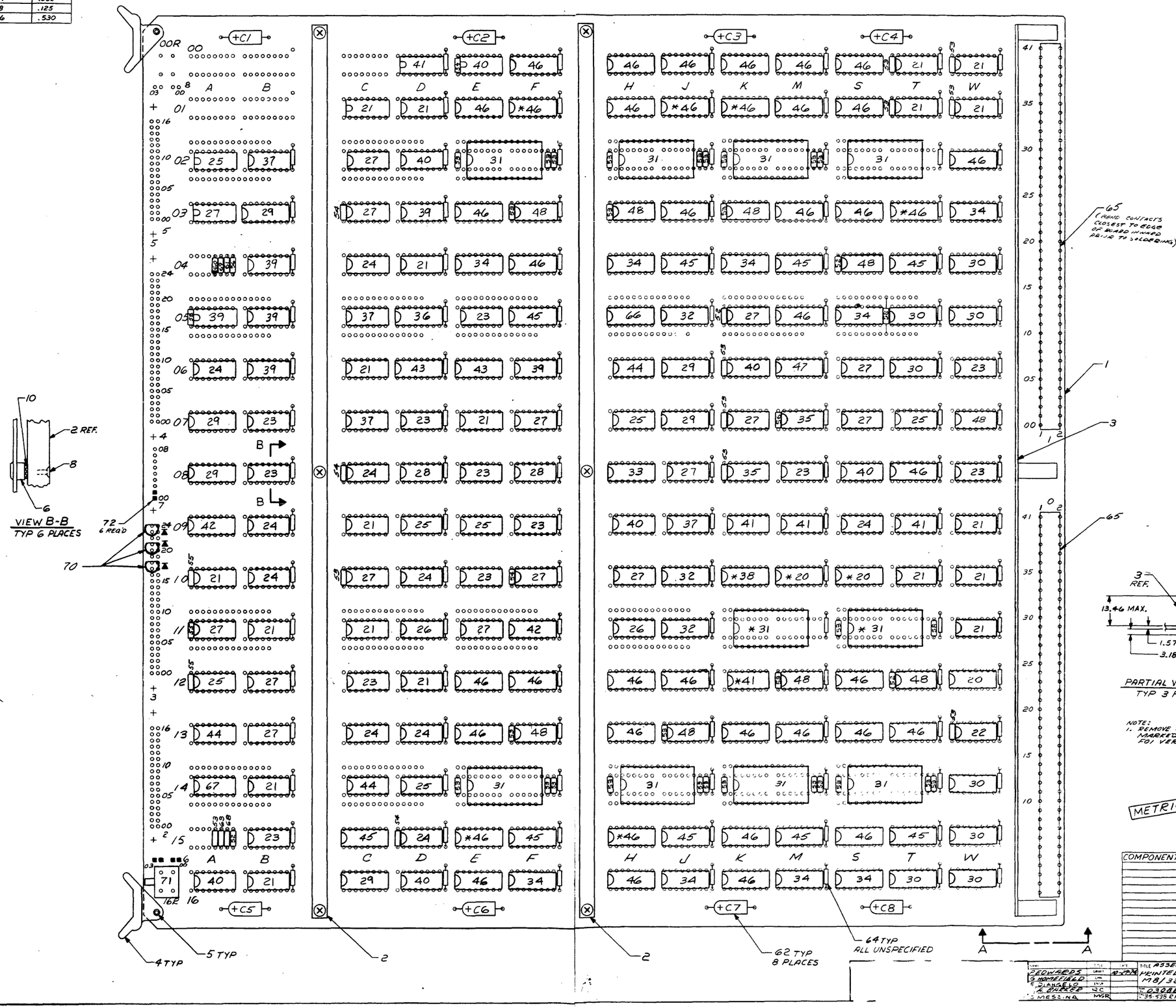
NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MB/32 ALU
TASK NO. 03088
DWG NO. 35-538R03D08
SHEET 7 OF 17

BRUNING 44-231 16042

MILLIMETER	INCH.
1.57	.062
3.18	.125
13.46	.530



REVISIONS

PRE PRODUCTION APPROVAL		REV	INIT	DATE	
		PROD			

CHANGES TO EXTENSIVE ECR INFORMATION SEE ECR.

PM	FJ	03208 -53	DS	1-25-75	RM

CHANGED: RESISTOR ITEM 67 FROM 15A MAS ITEM 57.

PM	FJ	W448-25	DS	1-25-75	RM

DELETE ITEM #3 FROM QTY ADDED FROM #8 TO 32W, ADDED ITEM 72 TO 06-C

PM	FJ	03208 -53	DS	4-8-75	RM

ADDED: NOTE 1 FOR FOI VERSION.

PM	FJ	W448-26	DS	4-8-75	RM

RELEASED FOR PRODUCTI.
MFG ENG. [illegible] DATE 5-[illegible]

ADDED ITEM 40 TO 00E

PM	BR	C522	-	6-27-76	RM

CHANGED ITEM 40 (DDE) 16 PINS WAS 16 PINS

PM	FJ	2934	-	9-7-76	ROA

ADDED 1.27 BETWEEN 03430 AND 03435.

PM	FJ	3170	-	9-26-77	RO7

AREA 10S DELETED CAS ITEM 73.

ID	JT	3266	-	10-5-77	RO8

ADDED METRIC TABLE. CHANGED DIM'S ON VIEW A-A TO METRIC. AREA 02A ADDED ITEM 25. AREA'S 04S & 14T ITEM 52 WAS ITEM 55. AREA'S 05S & 11T ITEM 58 WAS ITEM 58 (SHIFTED POS)

PM	FJ	3507	-	3-15-78	RO9

LOC 00E-01A,16 ADDED RES. ITEM #54.

KR	FJ	4132	-	8-30-78	R10

TC #32 (10 PLACES) WERE SHOWN AS EG PINS.

JM	FJ	W-[illegible]	RB	2-7-80	R11

EDWARDS	UNIT	SIZE	TITLE ASSEMBLY PRINTED CIRCUIT M8/32 - ALU
DANGELO	LTR	A	
BURKE	SC	DWG NO 03088	
MESS-NA	MGR	[illegible] 535 535 611 503	SHEET 1 OF 1

COMPONENT	REF DESIGNATION

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

DMA WRITE DATA BUFFERS

DMA CONTROL BITS FROM DMA 15:17

DMA 16 AND 17 TRANSCEIVERS

DMA ADDRESS COUNTER REGISTER

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION.

8/32 MBC — 35-535R25

USED IN MANUAL 29-394

NOTE: THIS REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

CONTINUED BELOW

RELEASED FOR PRODUCTION — ENG. — PROD.

35-535 P.C. BOARD REF IN AREA 59 WAS R05
REV LEV OF SHT 1 WAS R05
" " " " 9 WAS R02
" " " " 12 WAS R03
" " " " 10 WAS R03

AREA 59, 35-535 WAS R09. CHG. SHT 6, REV LEVEL WAS R01. CHG. SHT 13, REV LEVEL WAS R03.

REVISED SHT 9.

AREA 59, 35-535 WAS R10. CHG. SHT. 10.

REVISED SHTS 9 & 10, SUPPLEMENTARY INFO TABLE 8/32 MBC WAS R11

REVISED SHT 11, SUPPLEMENTARY INFO TABLE 8/32 MBC WAS R13

REVISED SHTS 9 THRU 13. SUPPLEMENTARY INFO TABLE 8/32 MBC WAS R14

REVISED SHTS 11, 12, & 13. TABLE 8/32 MBC WAS R15

REVISED SHT 13, TABLE 8/32 MBC WAS R16

REVISED SHTS 11 & 13 8/32 MBC WAS R18

REVISED SHTS 1, 9, 10, 11, 12 & 13. 35-535 REV LEV WAS R18.

REVISED SHT'S 12, 13 & 14. 8/32 MBC WAS REV LEV R21

SHEET INDEX														
REVLEVEL	24	1	1	1	2	3	6	10	11	9	13	8		
SHEET NO.	1	2	3	4	5	6	7	8	9	C	11	12	13	14

NOTES

REVISED SHTS 1 & 14
4979 | R | 4-29-82 | R24

REVISED SHT 10. ADDED MANUAL REF THIS SHT. AREA 59.
3531 | 5-23-78 | R22

REVISED SHTS 1, 10, & 14
LI 9007-06 | R | 10-22-80 | R23

REVISED SHTS 11/12/13 & 14. 35-535 WAS R23.
3476 | 12-23-77 | R20

REVISED SHT. 8, 35-535 WAS R24.
3420 | 2-17-78 | R21

REVISIONS (CONTD)
REVISED SHTS 1, 11 & 13. 35-535 WAS R22.
3772 | 5-10-77 | R19

REVISED SHT 13.
3186 | 7-4-77 | R19

REVISIONS

PRE PRODUCTION APPROVAL	INIT DATE
DEV	2ST NOV 6.74
PROD	Dec 11-5-74

REVISED PER ECO ON INDICATED SHEETS

03088-27 | 1-27-75 | R01

ADDED 03E TO M6 LMREQRI WAS NC
00512 WENT TO 00515
ADDED 00511 & 14 WENT TO PSRB, 00510 WAS NC

03088-42 | 2-7-75 | R02

CHANGED: SHT 12 WAS R02 REVISION.

03088-46 | 2-10-75 | R03

CHANGED: SHT 1 WAS R03
SHT. 5 WAS R00, SHT 9 WAS R01, SHTS. 10, 11, 13 & 14 WERE R02

03088-56 | 4-16-75 | R04

REV LEV OF SHT 11 WAS R03
" " " " 14 " R03

03088-74 | 6-1-75 | R05

2526 | — | 5-30-75 | R06

2575 | — | 7-18-75 | R07

2570 | — | 8-26-75 | R08

2601 | — | 9-9-75 | R09

2662 | — | 10-30-75 | R10

2663 | — | 10-30-75 | R11

2727 | 8-1-76 | R12

2758 | — | 3-12-76 | R13

2808 | — | 4-8-76 | R14

2840 | 5-10-76 | R15

3107 | — | 3-7-77 | R16

3176 | 4-21-77 | R17

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	10-14-74
G.J. HOMEFIELD	CHK	
T. FYFE	ENGR	
S. MESSINA	MGR	
R.A. BARKER	QC	

TITLE: FUNCTIONAL SCHEMATIC 8/32 MBC

TASK NO. 03088 | SHEET OF 1-14

DWG NO. 35-535 R24 D08

BRUNING 44 231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS					
CHANGED: 01M10 WAS CMC000 MNEMONIC.					
01/1	JP	03088-66	JK	4-17-75	201

03H 19-131 QUAD-D FLIP FLOP (CLR, CLK; 1D 1Q 2D 2Q 3D 3Q 4D 4Q)
02J 19-131 QUAD-D FLIP FLOP
01J 19-131 QUAD-D FLIP FLOP
00J 19-131 QUAD-D FLIP-FLOP
03J 19-131 QUAD-D FLIP FLOP
02K 19-131 QUAD-D FLIP FLOP
01K 19-131 QUAD-D FLIP FLOP
00K 19-131 QUAD-D FLIP FLOP

03T 19-132 QUAD 2:1 MUX (SEL, ENB; 1Y 2Y 3Y 4Y)
02T 19-132 QUAD 2:1 MUX
01T 19-132 QUAD 2:1 MUX
00T A/B 19-132 EN QUAD 2:1 MUX
03M 19-132 QUAD 2:1 MUX
02S 19-132 QUAD 2:1 MUX
01S 19-132 QUAD 2:1 MUX
00M A/B 19-132 EN QUAD 2:1 MUX

03W 19-118 QUAD BUS XCEIVER (ENB, SEL; IO I1 I2 I3; BO B1 B2 B3)
02W 19-118 QUAD BUS XCEIVER
01W 19-118 QUAD BUS XCEIVER
00W 19-118 QUAD BUS XCEIVER

03K 19-134 HEX BUFF/INV
02M 19-134 HEX BUFF/INV
01M 19-134 HEX BUFF/INV

08M 19-055 SG

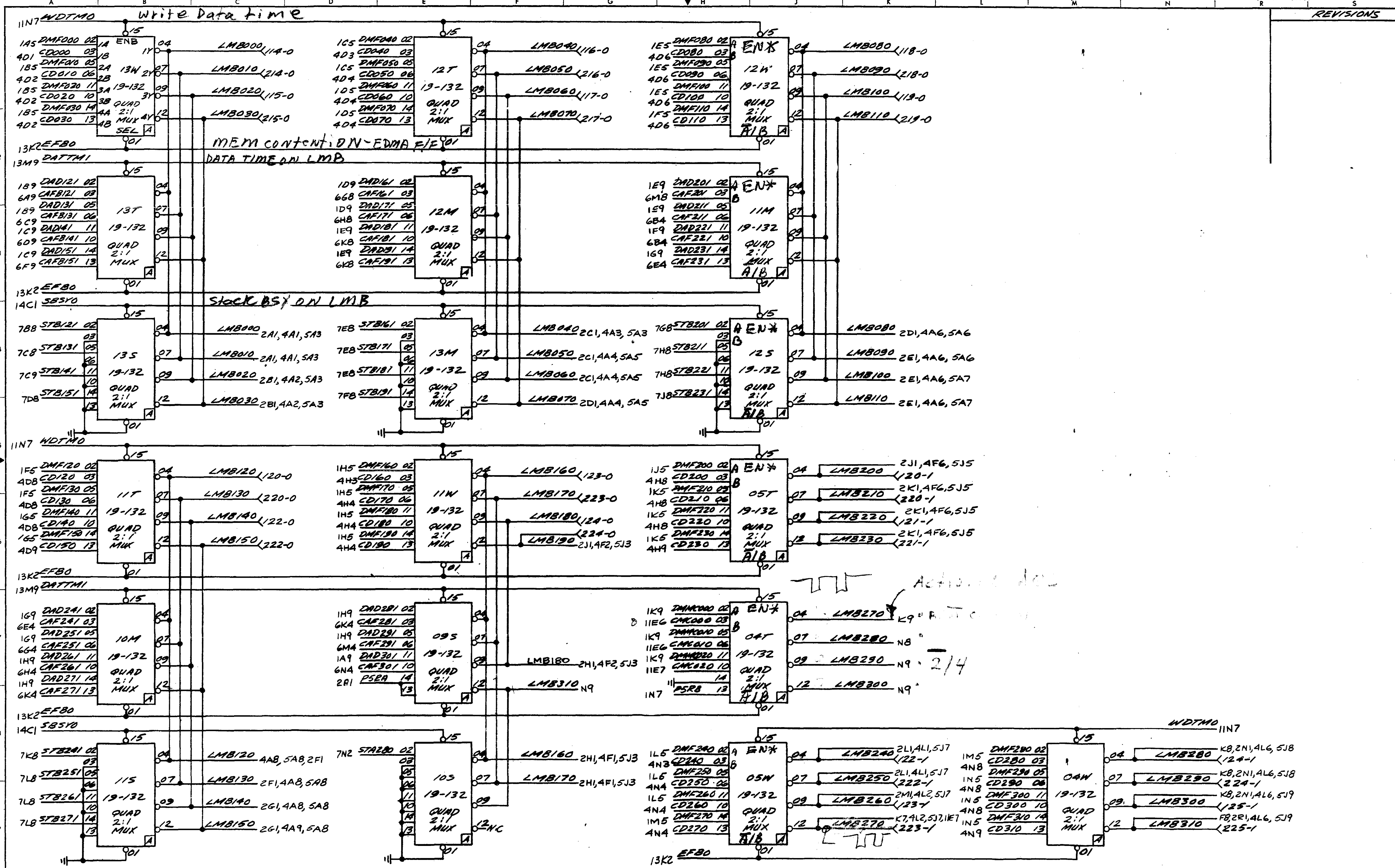
NOTES

NAME

TITLE FUNCT SCHEMATIC
8/32 MBC
03088
35-535-R01 D08 2 14

BRUNING 44 731 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757



NOTES

BRUNING 44 231 16042

NAME	TITLE	DATE
E. RoE	DRAFT	10-15-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32
MBC

03088
35-535 D08
SHEET 3 OF 14

REVISIONS			
ENTIRE SHT. 19-1323 INVERSION BUBBLES ON PINS 4, 7, 9, 12 WERE NOT SHOWN.			
27	MC	2370	8-26-75	R01

11H6 RDDATO

10W 19-132 QUAD 2:1 MUX (ENB, SEL)

3C4 LMB000	02	1A	04 1Y CD000 → 127-0 (2H5,3A1)
1A5 DMF001	03	1B	
3C4 LMB010	05	2A	07 2Y CD010 → 227-0 (2H5,3A1)
1B5 DMF011	06	2B	
3C4 LMB020	11	3A	09 3Y CD020 → 128-0 (2H5,3A1)
1B5 DMF021	10	3B	
3C5 LMB030	14	4A	12 4Y CD030 → 228-0 (2J5,3A2)
1B5 DMF031	13	4B	

MB00

10T 19-132 QUAD 2:1 MUX (RDDATO)

3F4 LMB040	02		04 CD040 → 129-0 (2K5,3D1)
1C5 DMF041	03		
3F4 LMB050	05		07 CD050 → 229-0 (2K5,3D1)
1C5 DMF051	06		
3F4 LMB060	11		09 CD060 → 130-0 (2K5,3D1)
1C5 DMF061	10		
3F5 LMB070	14		12 CD070 → 230-0 (2K5,3D2)
1D5 DMF071	13		

MB00

09W 19-132 QUAD 2:1 MUX (RDDATO)

3K4 LMB080	02		04 CD080 → 132-0 (2L5,3H1)
1D5 DMF081	03		
3K4 LMB090	05		07 CD090 → 232-0 (2L5,3H1)
1E5 DMF091	06		
3K4 LMB100	11		09 CD100 → 133-0 (2M5,3H1)
1E5 DMF101	10		
3K5 LMB110	14		12 CD110 → 233-0 (2M5,3H2)
1E5 DMF111	13		

MB00

09T 19-132 QUAD 2:1 MUX (RDDATO)

3C8 LMB120	02		04 CD120 → 134-0 (2N5,3A5)
1F5 DMF121	03		
3C9 LMB130	05		07 CD130 → 234-0 (2N5,3A6)
1F5 DMF131	06		
3C9 LMB140	11		09 CD140 → 135-0 (2N5,3A6)
1G5 DMF141	10		
3C9 LMB150	14		12 CD150 → 235-0 (2R5,3A6)
1G5 DMF151	13		

9G8 MB00

07W 19-132 QUAD 2:1 MUX

3F8 LMB160	02		04 CD160 → 107-1
1G5 DMF161	03		
3F8 LMB170	05		07 CD170 → 207-1
1H5 DMF171	06		
3F8 LMB180	11		09 CD180 → 108-1
1H5 DMF181	10		
3F6 LMB190	14		12 CD190 → 208-1
1H5 DMF191	13		

9G8 M00

07T 19-132 QUAD 2:1 MUX (STCDO)

5E3 ST161	02		04 CD160 → 2H5,3D5
	03		
5E3 ST171	05		07 CD170 → 2H5,3D6
	06		
5E3 ST181	11		09 CD180 → 2H5,3D6
	10		
5E3 ST191	14		12 CD190 → 2J5,3D6
	13		

07S 19-132 QUAD 2:1 MUX

3K5 LMB200	02		04 CD 200 → 109-1
1J5 DMF201	03		
3K6 LMB210	05		07 CD 210 → 209-1
1J5 DMF211	06		
3K6 LMB220	11		09 CD 220 → 110-1
1K5 DMF221	10		
3K6 LMB230	14		12 CD230 → 210-1
1K5 DMF231	13		

M00

11C5 STCDO

07M 19-132 QUAD 2:1 MUX

5E3 ST 201	02		04 CD200 → 2J5,3H5
	03		
5E3 ST 211	05		07 CD210 → 2K5,3H6
	06		
5D3 ST 221	11		09 CD220 → 2K5,3H6
	10		
5D3 ST 231	14		12 CD230 → 2K5,3H6
	13		

06W 19-132 QUAD 2:1 MUX

3K8 LMB240	02		04 CD240 → 112-1
1L5 DMF241	03		
3K9 LMB250	05		07 CD250 → 212-1
1L5 DMF251	06		
3K9 LMB260	11		09 CD260 → 113-1
1L5 DMF261	10		
3K9 LMB270	14		12 CD270 → 213-1
1M5 DMF 271	13		

M00

06T 19-132 QUAD 2:1 MUX (STCDO)

5E3 ST241	02		04 CD240 → 2L5,3H8
	03		
5E3 ST251	05		07 CD250 → 2L5,3H9
	06		
5F3 ST261	11		09 CD260 → 2M5,3H9
	10		
5F3 ST271	14		12 CD270 → 2M5,3M9
	13		

06S 19-132 QUAD 2:1 MUX

3N8 LMB280	02		04 CD280 → 114-1
1M5 DMF281	03		
3N9 LMB290	05		07 CD290 → 214-1
1N5 DMF291	06		
3N9 LMB300	11		09 CD300 → 115-1
1N5 DMF301	10		
3N9 LMB310	14		12 CD310 → 215-1
1N5 DMF311	13		

M00

06M 19-132 QUAD 2:1 MUX

5F3 ST 281	02		04 CD280 → 2N5,3L8
	03		
5F3 ST 291	05		07 CD290 → 2N5,3L9
	06		
5F3 ST 301	11		09 CD300 → 2N5,3L9
	10		
5N9 ST 311	14		12 CD310 → 2R5,3L9
	13		

NOTES

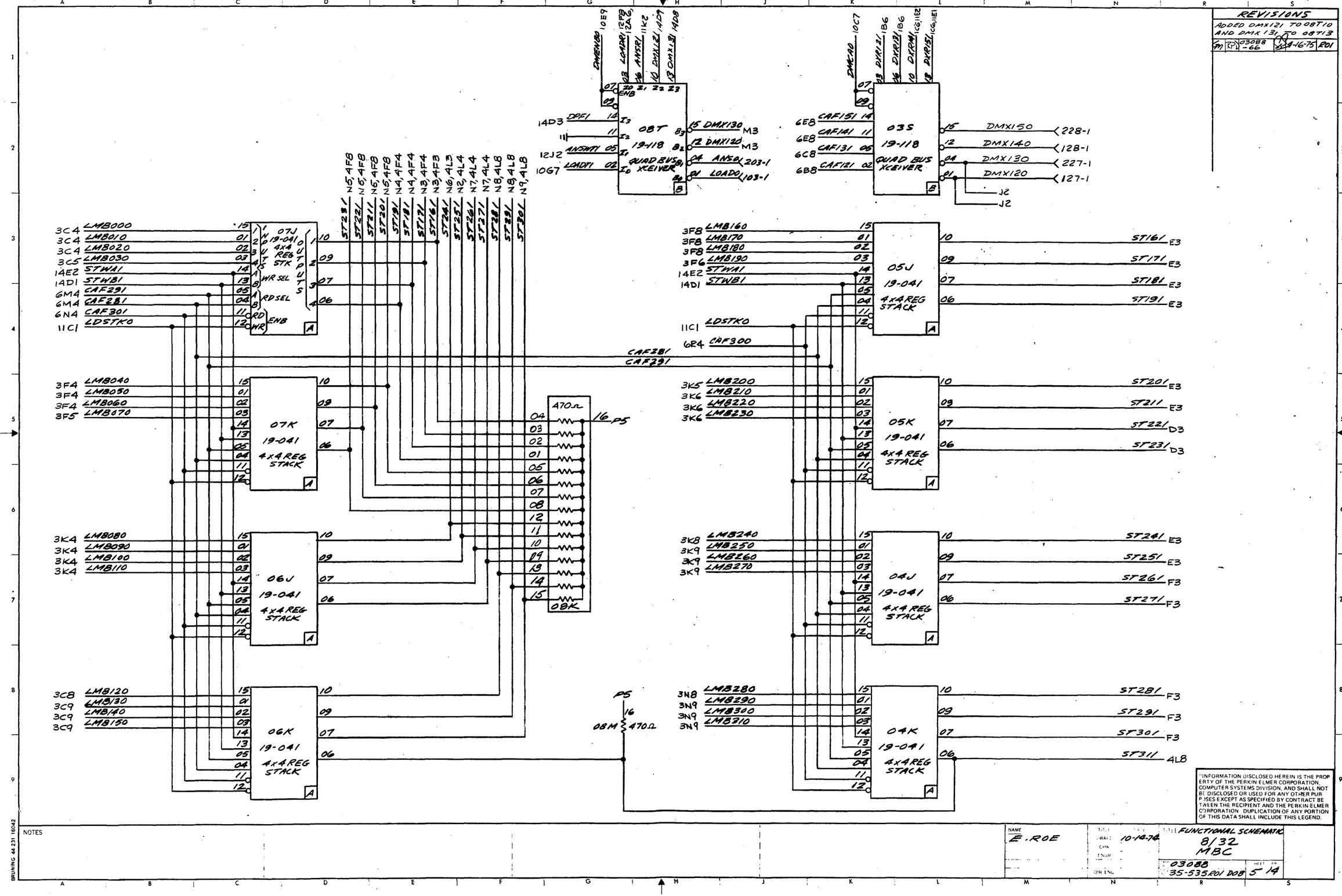
NAME	TITLE	DATE
TERRY PINGITORE	DRAFT	10-15-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCT. SCHEMATIC M 8/32 MBC

TASK NO. 03088 | DWG NO. 35-535-01008 | SHEET OF 4-14

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
ADDED DMX121 TO 08T10 AND DMX131 TO 08T13				
BY	CK'D	03088-66	9-16-75	R01



NOTES

NAME	DATE	TITLE
E. ROE	DRAFT 10-14-74	FUNCTIONAL SCHEMATIC 8/32 MBC
	CHK ENGR	03088 35-535.201 D08
	DIR ENG	SHEET OF 5 14

BRUNING 44 231 16042

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J 07757

REVISIONS
ADDED IC'S 19-055 IN LOC. C&D 5. OBF12 WENT TO CRDYO. CREQFO WAS REMOVED FROM (15T, 15W 14S, 14T, 14W, 16M, 16S, 16T 16W, 15S PINS @ 4 & 10)
6 AM 03088 -27 X 1-27-75 EDI
AREA A3, OBJ GATE WAS NOT SPEC'D. AREA N7, 15S-08 WAS CONN TO MNEM CAF210. 15S-10 & 15S-09 WAS CONN. TO GND. 15S-01 & 15S-13 WAS CONN. TO MNEM. CAF 211.
7 AM 2375 — 7-18-75 EDI

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	10-11-74
	CHK	
	ENGR	
	SR ENG	

TITLE FUNCTIONAL SCHEMATICS
8/32 MBC

03088
35-535-E00D08

SHEET OF
6-19

BRUNING 44-231 16042

PERKIN-ELMER

REVISIONS

PSR8 IN7
LOSTAL 14K8
CAF120 6A8
CAF130 6D8
CAF140 6D8
CAF150 6F8
CAF160 6F8
CAF170 6J8
CAF180 6J8
CAF190 6L8
CAF200 6L8
CAF210 6N4
CAF220 6C4
CAF230 6D4
CAF240 6F4
CAF250 6F4
CAF260 6J4
CAF270 6J4
CAF280 6L4
STA280 3D8, 8H8, 8D8, 14A1

16J 19-131 QUAD D FF
15J 19-131 QUAD D FF
14J 19-131 QUAD D FF
13J 19-131 QUAD D FF
12H 19-063 SDFF

STA151 8A7, 8H7
STA141 8A7, 8H7
STA131 8A7, 8H7
STA121 8A8, 8H8
STA191 8A6, 8H6
STA181 8A6, 8H6
STA171 8A5, 8H5
STA161 8A5, 8H5
STA231 8A3, 8H3
STA221 8A3, 8H3
STA211 8A4, 8H4
STA201 8A4, 8H4
STA271 8A1, 8H1
STA261 8A2, 8H2
STA251 8A2, 8H2
STA241 8A2, 8H2

16H 19-133 4 BIT ADDER
15H 19-133 4 BIT ADDER
14H 19-133 4 BIT ADDER
13H 19-133 4 BIT ADDER

STA281 8H9, 8D9, 14A1

STB121 3A4, 8E8, 8L8
STB131 3A4, 8E7, 8L7
STB141 3A4, 8E7, 8L7
STB151 3A4, 8E7, 8L7
STB161 3D4, 8E6, 8L6
STB171 3D4, 8E6, 8L6
STB181 3D4, 8E5, 8L5
STB191 3D4, 8E5, 8L5
STB201 3H4, 8E4, 8L4
STB211 3H4, 8E4, 8L4
STB221 3H4, 8E3, 8L3
STB231 3H4, 8E3, 8L3
STB241 3A8, 8E2, 8L2
STB251 3A8, 8E2, 8L2
STB261 3A9, 8E2, 8L2
STB271 3A9, 8E1, 8L1

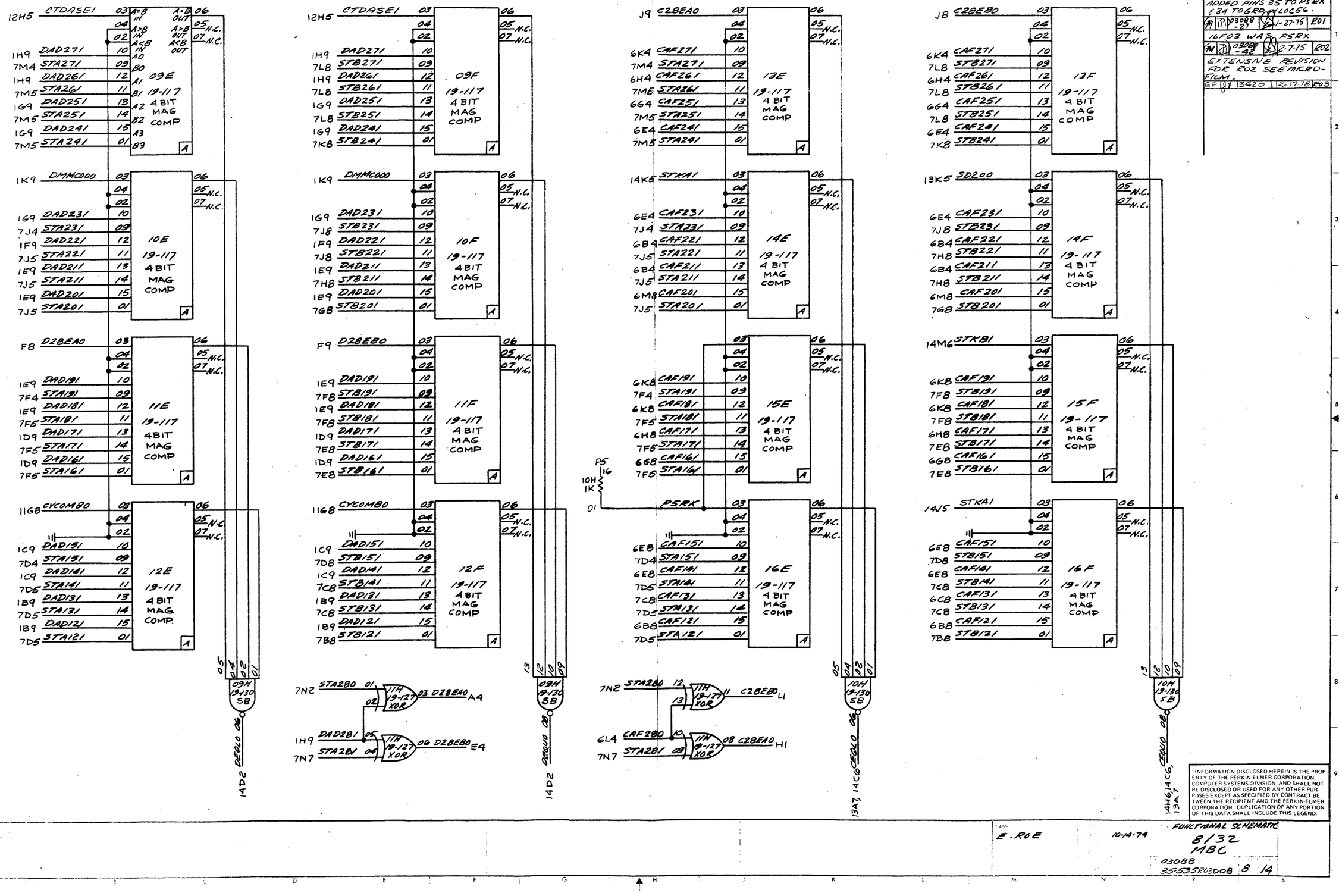
NOTES

NAME	TITLE	DATE	TITLE
J.R. BIELSKIE	DRAFT	10-15-74	FUNCTIONAL SCHEMATIC 8/32 MBC
	CHK		
	ENGR		
	DIR ENG		
			03088
			35-535 008
			SHEET 7 OF 14

BRUNING 44231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
ADDED PINS 35 TO PSRX E34 TO GRD. @ LOC 66.			
M	03088-27	11-27-75	R01
16F03 WAS PSRX			
M	03088-42	2-7-75	R02
EXTENSIVE REVISION FOR R02 SEE MICROFILM.			
GP	13420	2-17-78	R03



E. ROE 10-14-74

FUNCTIONAL SCHEMATIC
8/32 MBC
03088
35-535R03D08 8 14

PERKIN-ELMER

Local Memory Range Limit Comparators

REVISIONS

REMOVED SELO FROM 04H13 AND A2D11			
SM RP	03088-27	L-27-75	E01
IN LOC. G3, DAV 19-118 PIN 10 WAS 11 AND PIN 11 WAS 10 ADDED 11K1 TO P5RY			
SM RP	03088-26	4-16-75	R02
VALUE OF CAP. 04F WAS 220 PF, IN LOC K6			
SM VEA	2526	- 5-30-75	R03
AREA H6 05H-PINS 11, 12, 13 & 01 WERE TO SEL1. AREA N3 ADDED CROSS-REF. TO H6			
WS VM	2662	- 10-30-75	R04
AREA L4, MNEM. RXXO WAS NOT SPEC'D.			
SM MLZ	2727	- 2-29-76	R05
AREA K5: ADDED A DIODE (23-001) TO 05E-35, 39.			
WS VM	3107	- 5-5-77	R06

P5RY

11K1, 10D5, 10N5

34 33 32 31 30 — MSTP3D, MSTP3C, MSTP3B, MSTP3A

06F 19-117 4 BIT MAG COMP (A) — A<B IN, A=B IN, A>B IN, A0, B0, A1, B1, A2, B2, A3, B3; A<B OUT, A=B OUT, A>B OUT; N.C.; 1388

07F 19-117 4 BIT MAG COMP (A) — N.C.

29 28 27 26 — MSTP2D, MSTP2C, MSTP2B, MSTP2A

06H 19-117 4 BIT MAG COMP (A) — N.C.

25 24 23 22 — 6F9 CAFB15 MSTP1D; 6D9 CAFB14 MSTP1C; 6C9 CAFB13 MSTP1B; 6A9 CAFB12 MSTP1A

07H 19-117 4 BIT MAG COMP (A) — N.C.

21 33 32 31 — 6E8 CAF15 MSTP0D; 6E8 CAF14 MSTP0C; 6C8 CAF13 MSTP0B; 6B8 CAF12 MSTP0A

08H 1K, 16 P5

06E 16 1K P5 — STRAP FOR P5

14D8 CRQD1301 — 08U 19-057 SG — 02

14D7 CRQD2201 LTUU1 M00 — 02F 19-130 SB — 06

08W 19-118 QUAD BUS XCVR SEL — ENB, I3, I2, I1, I0, B3, B2, B1, B0, Z3, Z2, Z1, Z0, N.C.

11F2 M21, 11F2 M11, 11F3 M31

M3BZO 105-1; M2BZO 205-1; M1BZO 104-1

ENBO 10N8

selected CPH

10N6 SELO; 10L9 SCLEBO — 02D 19-116 HA

10L6 EXXO

DREQ01

M3BZRI, M2BZRI, M1BZRI — 05H 19-062 SG

N3 DREQO

05E 35 39 23-001; 05H 15 µH; 04F 1000 pF; 05F 330

DREQO 11J5, 14N1, H6 — EDMA RQST + to EDMA BUS

04F 19-115 HA — SQUEF1 10G5 — set QUE F/F

08H 19-055 SG — CXREQO 10A1 — CCPH RQST TO EDMA

M01 11A5, 14E6, 13A7, 13A9

13 09D 19-057 SG 12 — M800 4A9; M00 4F2

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	10-15-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC 8/32 MBC

03088 35-535 R06 D08

SHEET OF 9-14

BRUNING 44231 16042

PERKIN ELMER

All 3 ins high stops osc(clk)

DELAY LINE 30-019 00H 50nS

DELAY LINE 30-018 00C 100nS

REVISIONS
REPLACED T70A WITH T80A, LOC.C2 — SM — 03088-27 — 1-27-75 — R01
EXTENSIVE CHANGES SEE ECR SMT 4 — SM — 03088-42 — 2-7-75 — R02
03F03 WAS CTACI, 03F04 WAS CTA80 — SM — 03088-66 — 4-16-75 — R03

REVISIONS CONT'D
ADDED RES 118 TO 11809; 07011 WAS SOTRI; 03E03 WAS T00A; DELETED CROSS REF TO B6 FROM 02B01; GATE 03D AT 10C B6 WAS 00B 19-058; 02811 WENT TO SELO, 02810 WENT TO T80A; 02809 WAS XX0, DELETED XX0 FROM 07D06; 02B08 WENT TO 01E01 ADDED T10A TO 00C15 — SM — 2526 — - — 5-30-75 — R04
AREA C&D1, 02F-09 WAS CONN. TO 02F-10, AND WAS TIED TO 00H-05. 00H-11 & 13 WERE SHOWN "N.C." — RC — 2601 — 9-4-75 — R05
AREA N5 SELI WAS TO 966 — WS — 2662 — 10-30-75 — R06
AREA E4, DELETED GATE 02H. GATE 02H-03 WAS CONN. TO 01H-12, 02H-01 WAS EFO(13H2), 02H-02 WAS LMREQ1(1H3); AREA L6, 02D-01 WAS CONN. TO SELO. — DH — 2727 — 3-12-76 — R07
AREA 09: 08H-02 WAS TO 08H03. ADDED CONN. TO ANST80(11H6) — WS — 3107 — 3-5-76 — R08
AREA 65: SHT LOC. 9N5 BY SIG. 'SQUEF1' WAS SPEC'D 3NS — GS — 3531 — 5-23-78 — R09
IN AREA M2 DELETED CTACI AND L8. IN AREA J4 DELETED 14E4 FROM DMAACTO. IN AREA J4 DELETED L7 FROM CTABI. IN AREA L7 CTABI, CROSS REF. WAS RI. IN AREA H1 & H2 00F 4Q, 3Q, 2Q, & 1Q WERE 4B, 3B, 2B, & 1B — VT — LI 9007-06 — R — 10-22-80 — R10

NOTES

NAME	TITLE	DATE	TITLE
TERRY PINGITORE	DRAFT	10-16-74	FUNCTIONAL SCHEMATIC 8/32 MBC
	CHK		
	ENGR		
	PROJ ENG		03088 — SHEET OF — 35-535 R10 D08 — 10-14

BRUNING 44 231 16042

PERKIN-ELMER

REVISIONS				
19-057 IC GATES WERE ADDED TO G6C (9K & 11B) 11B 19-057 WAS ADDED TO G8 SMXO WENT TO 14M5, OLD PIN 11 & 03 WERE LMRDY80 00808 WENT TO LMRDY80 05815, 03, 13, & 05 WERE NC. 06C05, 05804 WENT TO DA811, 05807 WENT TO 06C 09				
1	03088 -22		6-27-75	R01
DELETED CROSS REF 12M9 FROM CYCOMO AND ADDED 4F7 TO CYCOMO				
2	03088 -22		7-7-75	R02
ADDED 16D AT LOC. M1, 04E03 WAS M11, 04E11 WAS M21, ADDED RESISTORS 05B AT LOC. F6 & 7 DELAY LINE WAS 30-019 01D05 WAS CMC000 ADDED U5 & 2M9 TO CMC8000. DELETED FROM CMC000 H6, J5, 10E6, 14D1, 8M9, DELETED FROM 04D10 AND CMC020 14D1. ADDED CROSS REF 14C9 LDLO AND LDMO 14C9, 12D1 WENT TO 14M8				
3	03088 -22		8-6-75	R03
08J WAS GOING TO 05 A13, DA800 WAS DA700				
4	03088 -22		9-1-75	R04
AREA G2 04E PIN 05 WAS TO 04E PIN 10 & 03E PIN 12				
WS	VHM	2663	-	10-30-75 R05
AREA F9, MNEM, 60YCMO WAS SPEC'D AS CYCOMO.				
2A	VHM	2727	-	12-29-76 R06
AREA F9, MNEM, ERSTO WAS SPEC'D AS CYCOMO.				
2A	VHM	2758	-	12-29-76 R07
AREA C7, MNEM SD600 WAS CONNECTED TO SMXO (AREA B6)				
JC	VRB	2840	-	5-10-76 R08
AREA M7: 06A-04 WAS TO 11NE (LMSEL1, CROSS-REF TO 12E5. AREA E8: 08A-01 WAS TO 07B-09 (ERSTO) CROSS-REF TO 13B3. AREA N6: ADDED CROSS-REF 10D9 TO ANSTBO				
WS	VJ	3107	-	3-5-77 R09
AREA 11F4: ADDED 13J9 TO CTFA1; AREA 11C8: ADDED 13J9 TO TO LMRY01. AREA H8: CYCOMBO WAS REF. TO 13J9.				
WS	VJ	3172	-	5-10-77 R10
AREA F9: "RDYDOS1" A7 WAS "CYCOM1" 13A6, 12A2. "RDBUFLO" 12D2 WAS "EFI" 13K1.				
GS	VJ	3476	-	12-22-77 R11

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

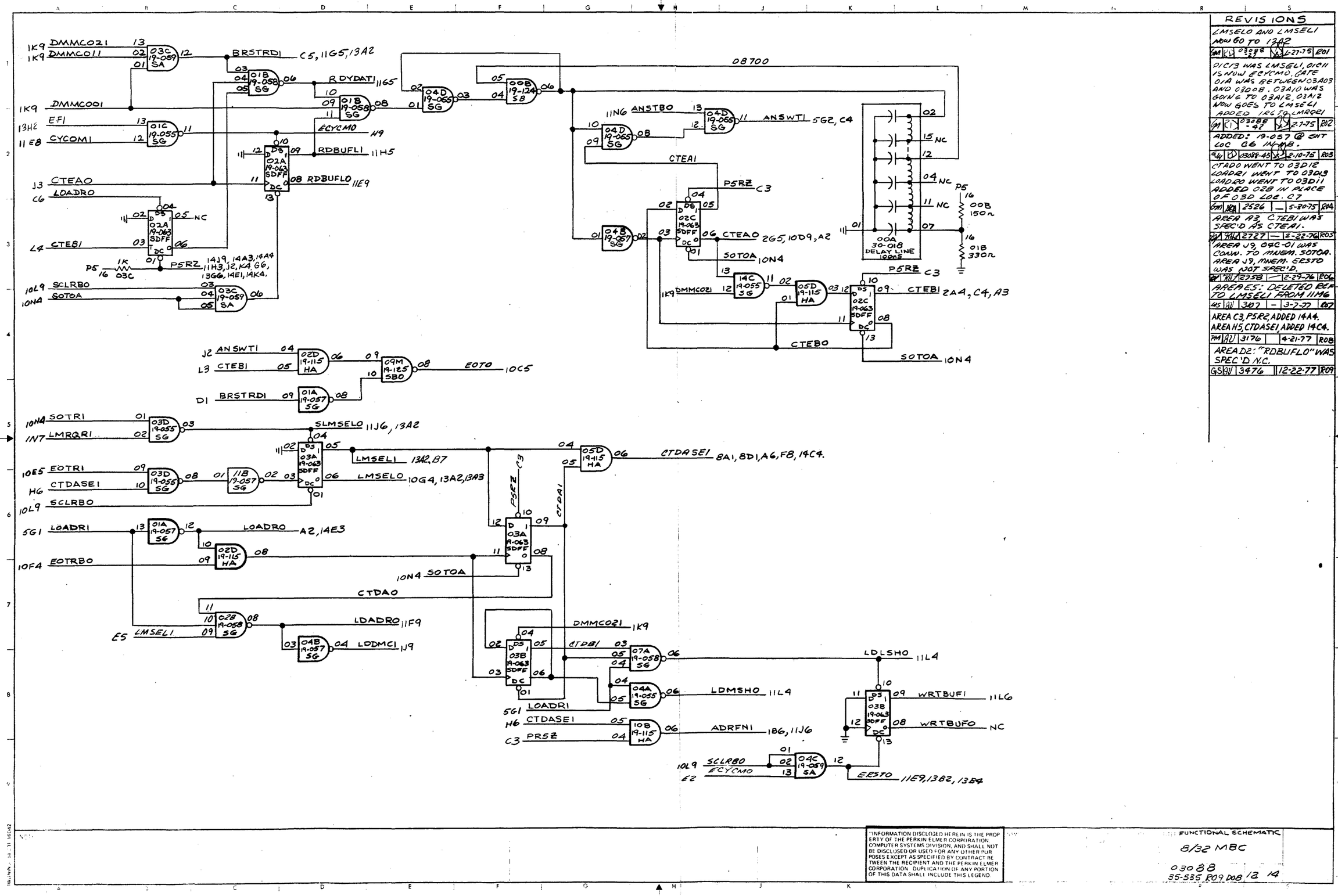
TITLE: FUNCTIONAL SCHEMATIC 8/32 M8C

TASK NO. 03088 CONF NO. 35-535R11 008

SHEET 11 OF 14

BRUNING 44-231 16042

PERKIN-ELMER



REVISIONS

LMSEL0 AND LMSEL1 NOW GO TO 13A2				
PM	KJ	03088-42	1-27-75	R01
01C13 WAS LMSEL1, 01C11 IS NOW ECYCMO. GATE 01A WAS BETWEEN 03A03 AND 03D08. 03A10 WAS GOING TO 03A12, 03A12 NOW GOES TO LMSEL1 ADDED 14C13 LMRQR1				
PM	KJ	03088-42	2-7-75	R02
ADDED: 19-057 @ SHT LOC C6 14 MB.				
GM	KJ	03088-45	2-10-75	R03
CTADO WENT TO 03D12 LOADR1 WENT TO 03D13 LOADR0 WENT TO 03D11 ADDED 02B IN PLACE OF 03D LOC. C7				
GM	MB	2526	—	5-30-75	R04A
AREA A3 CTEBI WAS SPEC'D AS CTEAI.				
GM	MB	2727	—	12-22-76	R05
AREA J9, 07C-01 WAS CONN. TO MNEM. SOTOA. AREA J9, MNEM. ERSTO WAS NOT SPEC'D.				
GM	MB	2758	—	12-29-76	R06
AREA E5: DELETED REF TO LMSEL1 FROM 11M6				
GS	MB	3107	—	3-2-77	R07
AREA C3, P5R2 ADDED 14A4. AREA H5, CTDASE1 ADDED 14C4.				
PM	MB	3176		4-21-77	R08
AREA D2: "RDBUFLO" WAS SPEC'D N.C.				
GS	MB	3476		12-22-77	R09

FUNCTIONAL SCHEMATIC

8/32 MBC

03088

35-535 R09 D08 12 14

PERKIN ELMER

Memory Control Logic

IF stuck low ONE DMA at Power up Check XREQ for Low, also this is read

EREQE1

EDMA b

EFBO

K9,E4

EFI

12A2, 11L6, 14A4

EFBO 3H9, 3A2, 3A3, 3A6, 3A8

CI A7, B8, 14G4, 14L9, 14H9, 11A7, 14C6, 14M5

CO 14C6

CFI K9

CPA

CFO E4

EREQRDO A1 10G4

CTENDO E8

CTENDO 08 C3

CCYCOMO 14E8, 14L8

CYCOMO 11E8

CYCOMBO 11H8

LMBBYO

LMBBYI 11A4, 14A4

LMRSO 237-0

11E7, 14A5, H8, 14H9

PSRZ 12C3

DATTMI 11L7, 3A2

SMXO

SSI K7

SSO A6,

SD200 BL3

SD500 A7

SD600 11C7

13A 30-018 DELAY LINE 100nS

12A 30-019 DELAY LINE 50ns

14D 19-062 SG

155 19-126

IN7 LMREQRI

D3 EREQRDO

1K9 DMMC000

LMSELO

B4, 12J3 ERSTO

B3 ERSTO

SLMSELO03

A2, 12D5

14N7 SSREQRO

14G7 CILMRSO

14M6 RSREQO

L6 SD1

11E8 CYCOM1

L3 C1

9G7 M01

J5 SD500

8K9 CEQLO

8R9 CEQUO

14D7 CRQD201

14D8 CRQD301

9E2 GTUU1

14C7 CRQD001

14E9 NO MEM1

14G8 STKRDYO

14K8 DMARDYO

11E8 CYCOMO

9G7 M01

11H6 IRO

14C7 CRQD001

K8, 14A1, LMBBYO

11B2 EDYD100

K9 SD35

N8 LMRSO

N5 SSI

E9 LMBBYO

11N6 EHOLDO

H2 DEFI

GG D35

H2 EFO

J4 CFI

J4 SMXO

11B8 LMRDY1

11F4 CTFA1

REVISIONS

IC. GATE 11D/N LOC J2 WAS 19-055, 12A WAS 30-018, 11C/3 WENT TO CYCOMOB. OBF02 WENT TO LMRDYB0, OBF01 WENT TO LMBBY0, 04C06 NOW GOES TO NO MEM1. ADDED IC GATES 01C, 00B, 01A AND 02B IN LOC. B3 & 4 & C3. 02B02 WENT TO LMSELO, 09C05 WENT TO CYCOM0

GM	KD	03088-27	11-27-75	R01

ADD 1E/L TO LMRQRO REMOVE 10A4 FROM EFI ADD 12A2 TO EFI ADD 10C4 TO EREQRDO 02B03 WENT TO 04B06

GM	KD	03088-92	12-7-75	R02

NOME:1 WAS 14B4
13A03 WAS SD200, 13A13 WAS SD500

GM	KD	03088-66	12-22-75	R03

AREA E2, 19-057 WAS SHOWN THUS:

CTENDO 11 12B (9057) 10 TO → 15A-10

AREA J7, GATE 12B WAS OBJ. ADDED 155.

GM	KM	2375	1-17-75	R04

AREA B3, B8B, MNEM, ECYCM0 WAS SPEC'D AS CYCOM0. AREA L8, MNEM DEFI WAS SPEC'D AS EFI. AREA J1, 11D COMP WAS NOT SPEC'D, EFO 10J6 DELETED

GM	KM	2727	2-29-76	R05

AREA B3 & B9, MNEM, ERSTO WAS SPEC'D AS ECYCM0.

GM	KM	2758	3-1-76	R06

AREA J1: RESISTOR LOC. BTWN. 11C29 & 11C25 WAS 330Ω, CAP. BTWN 11C30 & 11C31 (GND) WAS 100 PF. "11C" LOCATIONS WERE 11D (8) PLACES

WS	LC	2803	4-8-76	R07

AREA K6, ADDED MNEM SD600 AND 13A-5 AND CAPACITOR

JC	KB	2840	5-10-76	R08

AREA K1: ADDED 11C6 TO EFI. AREA B3: DELETED 11C9 FROM ERSTO. AREA K9, OBE-05 WAS TO 11E9

WS	GV	3107	3-7-77	R09

AREA H2, EFI, ADDED 14A9.
AREA G9, LMBBY1, ADDED 14A4.
AREA L2, EFBO, DELETED 14A4.

FM	GV	3176	4-21-77	R10

AREA K9. ADDED GATE 02H & RELATED CIRCUITRY. AREA J1 DELETED DIODE (23-001) AT 11C-39, 35. RESISTOR (470Ω) AT 11C-29, 25 WAS TO 11D-13. FOR PREV. REV INFO SEE VOIDED COPY 35-535 D08, SHT 13, R10.

WS	JV	3172	5-10-77	R11

ON IC. 15 S, PN 09 WAS 03, ALSO REMOVED BUBBLES.

GM	GV	3186	7-4-77	R12

AREA J2: DELETED 11E9 FROM "EFI"

GS	GV	3476	12-22-77	R13

NOTES

NAME	TITLE	DATE
J.R BIELSKIE	DRAFT	10-17-74
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC 8/32 MBC

ASM 03088 SHEET OF

ASY 35-535 R13 D08 13 -14

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS			
ADDED 19-062 IN LOC. R6 PIN NOS OF NAP IN MS WERE 09 & 13 TO GRD, RESISTOR IN MS 09 & 08 TO GRD., 11D IN L6 WAS 19-055. ADD 19-057 IN L9, 08B06 WAS LMRDY1 12C09 WAS CMC000, IRWRT1 WAS IRWRT0 ADDED 11K JUMPER & IC 09M IN LOC C4. 08D-13 WAS EF1, 13D1 WAS CMC000, 13D02 WAS CMC010, 13D13 WAS CMC020			
PM	03088-87	L-27-75	R01
ADDED BCC TO STKAI			
PM	03088-97	L2-7-75	R02
ADDED 11H2 TO CRQD101 09M05 WAS NOMEM1 ADDED 15D, 08M AND 11D TO AREA 9C, D, E, F, G & M. 08B13 WAS IR1			
GS	03088-66	L-22-76	R03
ADDED RDYDS1 TO LOC. N9			
PM	03088-78	L1-7-77	R04
AREA B4 ADDED 16D-063. AREA B4, 09M 19-125, 12 DELETED EFBO & CROSS REF 13L2. AREA C4, CTDASE1, 12H5 WAS LMSEL1, 1226.			
PM	3176	4-21-77	R05
AREA N9: 11A7 WAS 11C7 TO "RDYDS1"			
GS	3476	12-23-77	R06

REVISIONS CONT.			
IN AREA M7 SSREQA0 WAS SSEQA0			
VT	LI 9007-06	R	10-22-80 R07

"INFORMATION DISCLOSED HEREIN IS THE PROPERTY OF THE PERKIN ELMER CORPORATION COMPUTER SYSTEMS DIVISION AND SHALL NOT BE DISCLOSED OR USED FOR ANY OTHER PURPOSES EXCEPT AS SPECIFIED BY CONTRACT BETWEEN THE RECIPIENT AND THE PERKIN ELMER CORPORATION. DUPLICATION OF ANY PORTION OF THIS DATA SHALL INCLUDE THIS LEGEND.

FUNCTIONAL SCHEMATIC

8/32 MBC

03088

35-535R07 D08 14 14

MILLIMETER	INCH
13.46	.530
3.18	.125
1.57	.062

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV -VE	7/25/77
	PROD -VE	11-11-77

OSC WAS ISM 75 ADDED ITEM 84 TO 130 AND ITEM 83 TO 18.

	27378	CM1		

CHANGED: REF ITEM 60 @ LOC 23 WHERE IS LOC 62 WAS.

			4-10-78	AM2

ADDED 12 ITP LOCATIONS 15 I.D., ADDED 3 REF. TO LOC. 65, ITEM 47

	27982		4-14-78	AM3

RELEASED FOR PRODUCTION
MFG ENG. Fred Fyke DATE 5-12-78

ADDED ITEM 47 TO LOC 118.

	28586		5-30-78	AM4

ADDED ITEM 42 & 65 TO LOC 11C 11D

	28762		8-1-78	AM5

LOC 11C ITEM 47 WAS SPECD 25, ITEM 49 WAS SPECD 25, ITEM 47

	29628		8-8-78	AM6

ITEM 76 (23) PLACES WAS NOT SPECD

	32707		12-15-78	AM7

ADDED AM7/ITEM 65 TO LOC 05E35-39

	31072		2-27-79	AM8

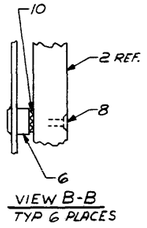
LOC 11C DELETED ON ITEM(S) 25, 47 & 49. ITEM(S) AM5 35, 39

	3278		5-10-79	AM9

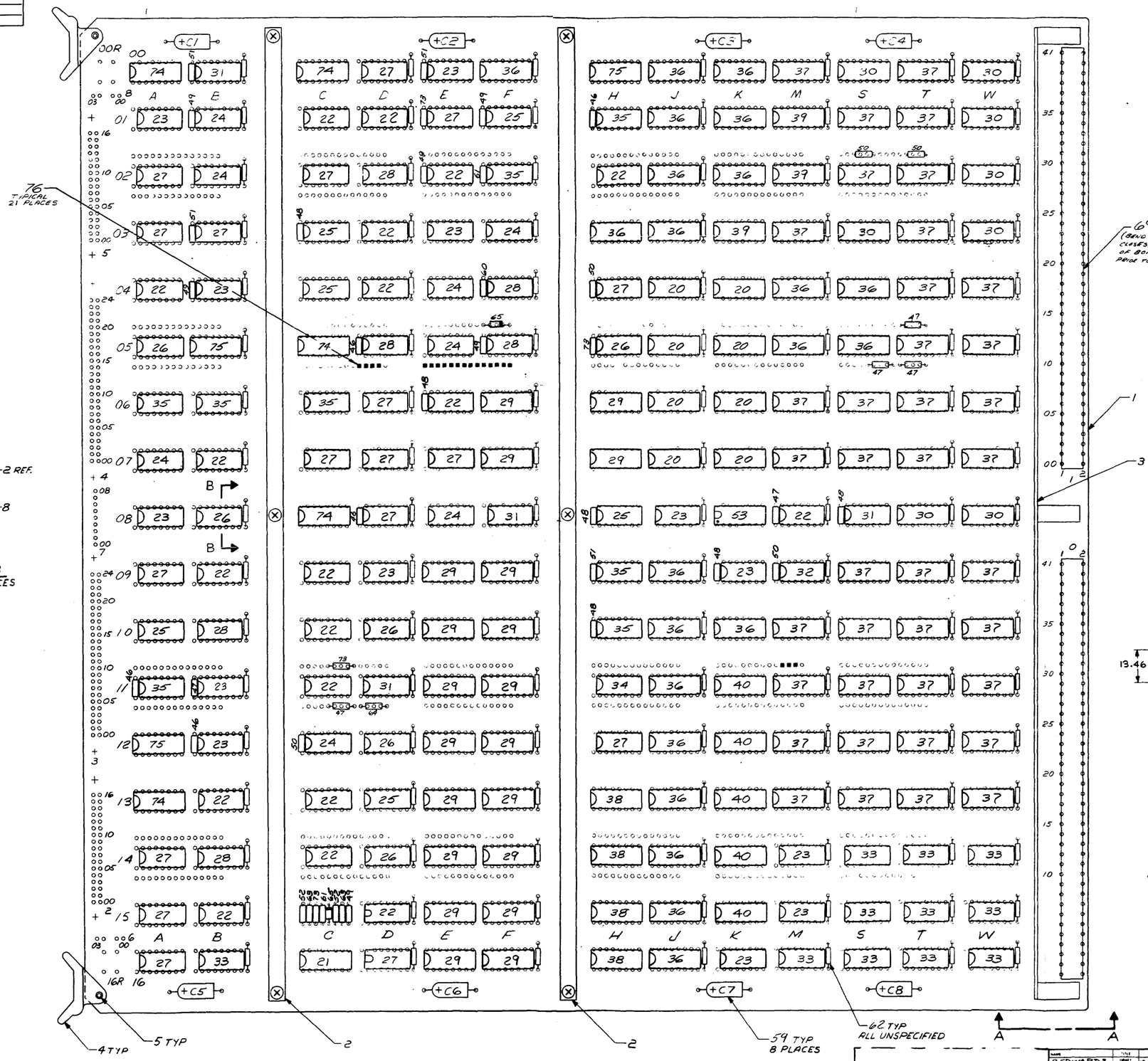
ADD 11C PINS 34 & 35 WERE STAKES. ITEM 76 QTY WAS 23

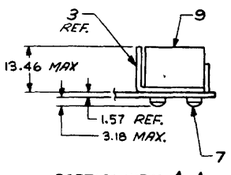
	34420		2-13-80	AM10

CHANGED TO METRIC 5-4-78, GM.



VIEW B-B
TYP 6 PLACES





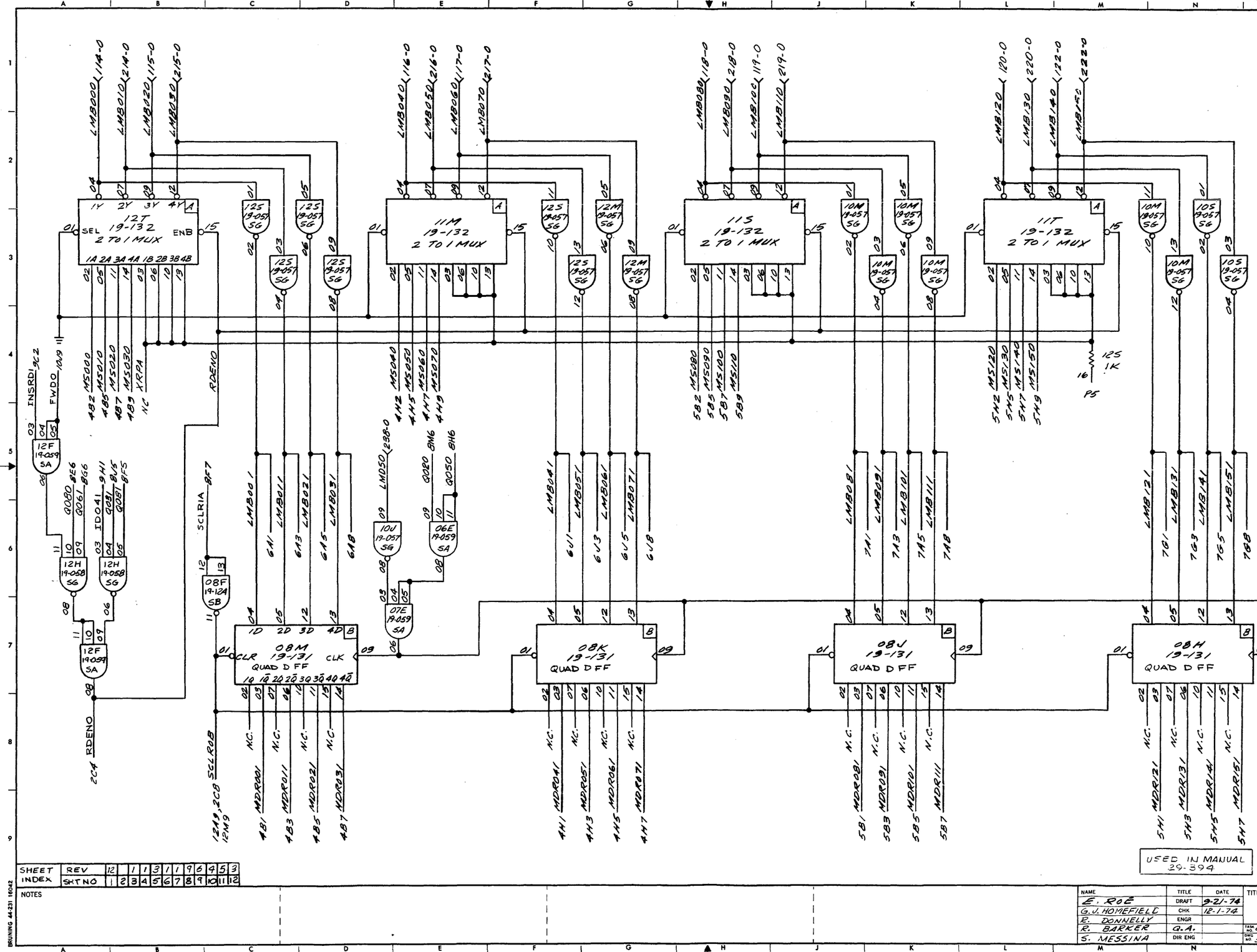
PARTIAL VIEW A-A
TYP 3 PLACES

METRIC

COMPONENT	REF DESIGNATION

NAME	TITLE	DATE	TITLE ASSEMBLY PRINTED CIRCUIT M8/32 - MBC
P.EDWARDS	DRAFT	10-30-79	
G.DOSFIELD	CHK		
S.TSE	ENGR		
A.A.BRANDT	QC		SIZE D
J.E.MESSINA	MGR		7030 REV
			7-35-5540-603 SHT 1 OF 1

PERKIN ELMER



REVISIONS

PRE PRODUCTION APPROVAL	DEV PROD	REF.	DATE
		1100	12/74

REVISED SHEETS 1,3 THRU 12 PER MARKED PRINTS				
JRB	KT	03088-17	11-27-74	R01
SHEET 8 WAS R01 REV.				
GM	KT	03088-25	1-16-75	R02
SHEET 8 WAS R02 REV. SHEETS 9 & 11 WERE R01 REV. CHANGED: MNEMONICS Q010, Q011, Q031, Q071 WERE Q10, Q11, Q31, Q71 RESP. SHEETS 5, 10, 11, & 12 WERE R01.				
GM	KT	03088-33	1-16-75	R03
SHEET 8 WAS R03 REV. SHEET 9 WAS R02 REV.				
GM	KT	03088-35	1-16-75	R04
CHANGED: AREA AS Q080 WAS Q011, Q061 WAS Q071 & Q081 WAS Q010 SHEET REV WERE: SHT.5 WAS R02, SHT 8 WAS R04, SHT. 11 WAS R02, ADDED: 19-059 GATES @ SHT. LOC. C7 & E6, POS 07E & 06E.				
GM	KT	03088-44	3-17-75	R05
CHANGED SHT 12 WAS R02 SHT 8 WAS R05				
GM	KT	03088-63	4-11-75	R06
RELEASED FOR PRINT INC.			5/14/75	
REVISED SHEETS 8 & 9 8/32 LMI 35-534 WAS R07				
VC	JRB	2891	5-11-76	R07
REVISED SHTS 1, 9, 10 & 11. 35-534 WAS R08				
WS	VV	3119	5-11-77	R08
REVISED SHTS 9 & 10 35-534 WAS R11 MANUAL TABLE ADDED				
GP	JL	3537	3-16-78	R09
REVISED SHTS 1 & 11. AREA 59 35-534 WAS R13.				
KR	KT	4250	MS 2-19-79	R10
REVISE SHT'S 1 & 8.				
KR	KT	4231	R 3-17-80	R11
AREA 59; 35-534 WAS R14 REVISED SHTS 1 & 8				
JLV	VV	14637	M 3-16-81	R12

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL	
8/32 LMI	35-534 R15

SHEET INDEX	REV	12	1	1	3	1	1	9	6	4	5	3
	SHT NO	1	2	3	4	5	6	7	8	9	10	11	12

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	9-21-74
G.J. HOMEFIELD	CHK	12-1-74
R. DONNELLY	ENGR	
R. BARKER	Q.A.	
S. MESSINA	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 LMI

TASK NO. 03088 | SHEET OF 1 - 12
DWG NO. 35-534 R12 D08

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS

10T 19-132 2 TO 1 MUX

03M 19-132 2 TO 1 MUX

03S 19-132 2 TO 1 MUX

03T 19-132 2 TO 1 MUX

07H 19-131 QUAD D FF

07F 19-131 QUAD D FF

06F 19-131 QUAD D FF

05F 19-131 QUAD D FF

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 LMI

TASK NO. 03088
DWG NO. 35-534 D08

SHEET 2 OF 12

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS			
REVISED PER MARKED PRINT			
JRB	03088-17	11-27-74	R01

2C9 MDR161 — 02M 19-125 SBO — 02T 220Ω 16 P5 — MD000 (229-1) — 330Ω 02T
2A4,11A5 MD000 — 03J 19-055 SG — 483 XRPM — P5 03J 16 1K
2C9 MDR171 — 02M 19-125 SBO — 02T 220Ω 15 P5 — MD010 (130-1) — 330Ω 02T
2A4,11A5 MD010 — 01K 19-057 SG
2D9 MDR181 — 01M 19-125 SBO — 02T 220Ω 14 P5 — MD020 (230-1) — 330Ω 02T
2B4,11A5 MD020 — 01K 19-057 SG
2D9 MDR191 — 01M 19-125 SBO — 00T 220Ω 16 P5 — MD030 (131-1) — 330Ω 01T
10L3 WTE021
L8 OBCLRO
2B4,11A6 MD030 — 01K 19-057 SG

2F9 MDR201 — 00M 19-125 SBO — 00T 220Ω 15 P5 — MD040 (231-1) — 330Ω 01T
2E4,11A6 MD040 — 01K 19-057 SG
2G9 MDR211 — 00M 19-125 SBO — 00T 220Ω 14 P5 — MD050 (132-1) — 330Ω 01T
2E4,11A6 MD050 — 01K 19-057 SG
2G9 MDR221 — 00K 19-125 SBO — 00T 220Ω 13 P5 — MD060 (232-1) — 330Ω 01T
2E4,11A6 MD060 — 01K 19-057 SG
2G9 MDR231 — 00K 19-125 SBO — 00T 220Ω 12 P5 — MD070 (133-1) — 330Ω 01T
10L3 WTE021
L8 OBCLRO
2E4,11A6 MD070 — 02J 19-057 SG

2J9 MDR241 — 02K 19-125 SBO — 00T 220Ω 11 P5 — MD080 (233-1) — 330Ω 01T
2H4,11A7 MD080 — 01J 19-057 SG
5F1 MQ21 — 06C 19-055 SG — 10L3 WTE020 — 04E 19-124 SB
2K9 MDR261 — 02K 19-125 SBO — 00T 220Ω 10 P5 — MD090 (134-1) — 330Ω 01T
2H4,11A7 MD090 — 01J 19-057 SG
2K9 MDR261 — 00J 19-125 SBO — 00S 220Ω P5 — MD100 (234-1) — 330Ω 01S
2H4,11A7 MD100 — 01J 19-057 SG
2K9 MDR271 — 00J 19-125 SBO — 00S 220Ω 15 P5 — MD110 (135-1) — 330Ω 01S
WTE021
L8 OBCLRO
2H4,11A7 MD110 — 01J 19-057 SG

2N9 MDR281 — 00H 19-125 SBO — 00S 220Ω 14 P5 — MD120 (235-1) — 330Ω 01S
2L4,11A7 MD120 — 01J 19-057 SG
2N9 MDR291 — 00H 19-125 SBO — 00S 220Ω 13 P5 — MD130 (136-1) — 330Ω 01S
2L4,11A8 MD130 — 01H 19-057 SG
2N9 MDR301 — 02J 19-125 SBO — 00S 220Ω 12 P5 — MD140 (236-1) — 330Ω 01S
2L4,11A8 MD140 — 01H 19-057 SG
2N9 MDR311 — 02J 19-125 SBO — 00S 220Ω 11 P5 — MD150 (137-1) — 330Ω 01S
10L3 WTE021
11G5,H8,E8,A8 OBCLRO
2L4,11A8 MD150 — 01H 19-057 SG

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 LMI
TASK NO. 03088
ENG NO. 35534 R01 D08
SHEET OF 3 -12

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
REVISED PER MARKED PRINT				
JRG	03088-17	JS	11-27-74	R01

1C9 MDR001 → 04M 19-125 SBO (10, 09 → 08) → 04T 16 220Ω P5 MS000 ⟨210-1; 11 → 04T 06 330Ω

2C9 MDR161 → 04M 19-125 SBO (04, 05 → 06)

13, 12 → 04M 19-125 SBO → 11

1A4,11A1,2B4 MS000 → 03V 19-055 SG (M → 06)

3A3 XRPM → 05

1C9 MDR011 → 04M 19-125 SBO (01, 02 → 03) → 02 04T 15 220Ω P5 MS010 ⟨109-1; 10 → 04T 07 330Ω

2C9 MDR171 → 04R 19-125 SBO (13, 12 → 11)

10, 09 → 04R 19-125 SBO → 08

1A4, 2B4,11A2 MS010 → 05R 19-057 SG (11 → 10)

1D9 MDR021 → 04R 19-125 SBO (01, 02 → 03) → 03 04T 14 220Ω P5 MS020 ⟨209-1; 09 → 04T 08 330Ω

2D9 MDR181 → 04R 19-125 SBO (04, 05 → 06)

13, 12 → 05M 19-125 SBO → 11

1B4,2B4,11A2 MS020 → 05R 19-057 SG (09 → 08)

1D9 MDR031 → 05M 19-125 SBO (10, 09 → 08) → 05T 16 220Ω P5 MS030 ⟨108-1; 15 → 06T 02 330Ω

10L2 WTE001

2D9 MDR191 → 05M 19-125 SBO (04, 05 → 06)

10L4 WTE011

5H8 EBCLR0 → 01

02 → 05M 19-125 SBO → 03

1B4,2B4,11A2 MS030 → 05R 19-057 SG (05 → 06)

1F9 MDR041 → 06M 19-125 SBO (13, 12 → 11) → 02 05T 15 220Ω P5 MS040 ⟨208-1; 14 → 06T 03 330Ω

2F9 MDR201 → 06M 19-125 SBO (10, 09 → 08)

04, 05 → 06M 19-125 SBO → 06

1E4,2E4,11A2 MS040 → 06R 19-057 SG (08 → 08)

1G9 MDR051 → 06M 19-125 SBO (01, 02 → 03) → 03 05T 14 220Ω P5 MS050 ⟨107-1; 13 → 06T 04 330Ω

2G9 MDR211 → 07M 19-125 SBO (13, 12 → 11)

10, 09 → 07M 19-125 SBO → 08

1E4, 2E4, 11A2 MS050 → 06R 19-057 SG (05 → 06)

1G9 MDR061 → 07M 19-125 SBO (04, 05 → 06) → 04 05T 13 220Ω P5 MS060 ⟨207-1; 12 → 06T 05 330Ω

2G9 MDR221 → 07M 19-125 SBO (01, 02 → 03)

01, 02 → 07R 19-125 SBO → 03

1E4,2E4,11A2 MS060 → 06R 19-057 SG (03 → 04)

1G9 MDR071 → 07R 19-125 SBO (04, 05 → 06) → 05 05T 12 220Ω P5 MS070 ⟨106-1; 11 → 06T 06 330Ω

10L2 WTE001

2G9 MDR231 → 07R 19-125 SBO (10, 09 → 08)

10L4 WTE011

5H8 EBCLR0 → 13

12 → 07R 19-125 SBO → 11

1E4, 2E4, 11A2 MS070 → 06R 19-057 SG (01 → 02)

NOTES

NAME	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC
E.ROE	DRAFT	9-26-74	8/32 LMI
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03088 SHEET OF 4-12
			DWG NO. 35-534R01D08

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
REVISED PER MARKED PRINT				
JR	03088-17		11-27-74	R01
CHANGED: MNEMONIC Q020 WAS Q59				
	03088-33		1-16-75	R02
CHANGED: 01801 WAS Q020 MNEMONIC.				
	03088-44		3-17-75	R03

1J9 MDR081 — 07J 19-125 SBO — 05T 220Ω PS — MS080 — 330Ω 06T — <206-1
1OL2 WTE001
2J9 MDR241
1OL4 WTE011
H8 EBCLRO
9M9 MSTRP0
8N6 Q010 — 01B 19-055 SG — 3J2 — MQ21 — 1OL3 WTE000 — 1OL5 WTE010 — 07D 19-058 SG — 08F 19-124 SB
1H4,2H4,11A3 MS080 — 06K 19-057 SG

1K9 MDR091 — 07J 19-125 SBO — 05T 220Ω PS — MS090 — 330Ω 06T — <105-1
2K9 MDR251 — 06J 19-125 SBO
1H4,2H4,11A3 MS090 — 05K 19-057 SG

1K9 MDR101 — 06J 19-125 SBO — 05S 220Ω PS — MS100 — 330Ω 06S — <205-1
2K9 MDR261 — 06J 19-125 SBO — 06H 19-125 SBO
1H4,2J4,11A3 MS100 — 06K 19-057 SG

1K9 MDR111 — 06H 19-125 SBO — 05S 220Ω PS — MS110 — 330Ω 06S — <104-1
2K9 MDR271 — 06H 19-125 SBO
1H4,2J4,11A3 MS110 — 05K 19-057 SG

1N9 MDR121 — 05J 19-125 SBO — 05S 220Ω PS — MS120 — 330Ω 06S — <204-1
1OL2 WTE001
2N9 MDR281 — 05J 19-125 SBO
1L4,2L4,11A4 MS120 — 05K 19-057 SG

1N9 MDR131 — 05J 19-125 SBO — 05S 220Ω PS — MS130 — 330Ω 06S — <103-1
2N9 MDR291 — 04J 19-125 SBO
1L4,2M4,11A4 MS130 — 05H 19-057 SG

1N9 MDR141 — 04J 19-125 SBO — 05S 220Ω PS — MS140 — 330Ω 06S — <203-1
2N9 MDR301 — 04J 19-125 SBO — 04H 19-125 SBO
1L4,2M4,11A4 MS140 — 05H 19-057 SG

1N9 MDR151 — 04H 19-125 SBO — 05S 220Ω PS — MS150 — 330Ω 06S — <102-1
2N9 MDR311 — 04H 19-125 SBO
WTE011
11F3,4H8,4B8,B2 EBCLRO — 04H 19-125 SBO
1L4,2M4,11A4 MS150 — 05H 19-057 SG

FUNCTIONAL SCHEMATIC
8/32 LMI
03088
35-534R03D08 5 12

PERKIN ELMER

REVISIONS				
REVISED PER MARKED PRINT				
JRB	RDD	03088-17		11-27-74	R01

1C6 LMB001 — 05, 04, 03, 02 — 14H 19-126 SG — 06 — 10, 09, 13, 12 — 14M 19-130 SG — 08 — MAX060 <108-0

9J3 MLX060 — 01 — 14J 19-057 SG — 02 — MLX061 — 12J7

1C6 LMB011 — 09, 10, 13, 01 — 14H 19-126 SG — 08 — 02, 01, 05, 04 — 14M 19-130 SG — 06 — MAX070 <208-0

9J3 MLX070 — 03 — 14J 19-057 SG — 04 — MLX071 — 12J7

1D6 LMB021 — 05, 04, 03, 02 — 13H 19-126 SG — 06 — 10, 09, 13, 12 — 14S 19-130 SG — 08 — MA000 <106-0

9J3 ML000 — 05 — 14J 19-057 SG — 06 — ML001 — 12J6

1D6 LMB031 — 09, 10, 13, 01 — 13H 19-126 SG — 08 — 02, 01, 05, 04 — 14S 19-130 SG — 06 — MA010 <107-0

01 — 13M 19-057 SG — 02

9J3 ML010 — 13 — 14J 19-057 SG — 12

10C2 LMARF1

1F6 LMB041 — 05, 04, 03, 02 — 13J 19-126 SG — 06 — 10, 09, 13, 12 — 14T 19-130 SG — 08 — MA020 <109-0

11 — 14J 19-057 SG — 10

1G6 LMB051 — 09, 10, 13, 01 — 13J 19-126 SG — 08 — 02, 01, 05, 04 — 14T 19-130 SG — 06 — MA030 <110-0

09 — 14J 19-057 SG — 08

1G6 LMB061 — 05, 04, 03, 02 — 14K 19-126 SG — 06 — 02, 01, 05, 04 — 13T 19-130 SG — 06 — MA040 <210-0

01 — 12M 19-057 SG — 02

1G6 LMB071 — 09, 10, 13, 01 — 14K 19-126 SG — 08 — 02, 01, 05, 04 — 08S 19-130 SG — 06 — MA050 <129-0

09 — 13M 19-057 SG — 08

03 — 12M 19-057 SG — 04

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 LMI

TASK NO. 03088
DWG NO. 35-534R01D08
SHEET 6 OF 12

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
REVISED PER MARKED PRINT				
REV	BY	03088-17		11-27-74 R01

1K6 LMB081

13K 19-126 SG

13M 19-057 SG

12M 19-057 SG

085 19-130 SG — 08 MA060 ⟨229-0

1K6 LMB091

13K 19-126 SG

12M 19-057 SG

097 19-130 SG — 06 MA070 ⟨130-0

1K6 LMB101

12K 19-126 SG

12J 19-057 SG

09T 19-130 SG — 08 MA080 ⟨230-0

1K6 LMB111

12K 19-126 SG

10C2 LMARF1

12J 19-057 SG

07S 19-130 SG — 06 MA090 ⟨131-0

1N6 LMB121

11J 19-126 SG

12J 19-057 SG

13M 19-057 SG

07S 19-130 SG — 08 MA100 ⟨231-0

1N6 LMB131

11J 19-126 SG

12J 19-057 SG

087 19-130 SG — 06 MA110 ⟨132-0

1N6 LMB141

11K 19-126 SG

12J 19-057 SG

08T 19-130 SG — 08 MA120 ⟨232-0

1R6 LMB151

11K 19-126 SG

10C2 LMARF1

12J 19-057 SG

07T 19-130 SG — 06 MA130 ⟨133-0

10C2 LMARF1

10J 19-057 SG

10K 19-126 SG

07T 19-130 SG — 08 MA140 ⟨233-0

2C6 LMB161

NOTES ADRS IS 0 ASSERTED ON LMB

NAME	TITLE	DATE
B GRAY	DRAFT	9-25-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC 8/32 LM I

TASK NO 03088

DWG NO 35-534 R01 D08

SHEET OF 7-12

PERKIN ELMER

REVISIONS				
REVISED PER MARKED PRINT				
VR6	03088-17		11-26-74	R01
DELETED 10PF CAP. LOC 14D CONN. TO 13D08, CHANGED IC IN LOC 13D WAS 30-051-2175 DEL. LINE, RES. AT 13D PIN 39&30 WAS 51Ω 1/8 WATT.				
	03088-25		1-16-75	R02
ADDED: MNEMONICS TO THE FOLLOWING OUTPUTS: 10K08, 12E08, 10H03, 12H12, 12E06, CHANGED: MNEMONICS Q010 - Q080 WERE Q10-Q80, Q011 - Q081 WERE Q11-Q81				
	03088-33		1-16-75	R03
DELETED: 9D4 REF @ Q080; 9D4 REF @ Q071; 9H1 REF @ Q021; ADDED: 9D4 REF @ Q070 & Q061; 9L1 REF @ Q021.				
	03088-35		1-16-75	R04
CHANGED: SHEET CROSS-REFERENCES TO INCORPORATE OTHER CHANGES.				
	03088-44		3-17-75	R05
ADDED LOC. 12J1 TO RFO & LOC 12H7 TO RFI				
	03088-63		5-11-76	R06
AREA H3-H4 NOTE: ADD STRAP.... 1MS. WAS AS FOLLOWS: ADD STRAP FOR 32KB OMIT FOR 64KB.				
KR	4231	R	3-17-80	R08
AREA C4; "07,01" WAS "01" AREA D4: 13C39 WAS CONN. WITH 14DIA. & 13D13				
	4637	M	3-16-81	R09

AREA K5, Q091 REMOVED REF LOCATION 9G5

AREA REF LOCATION 9G5

9G1 RSRO
F8 SCLROA
12H7, J2 RFI
9F3 ONBO
237-0 LMRS0
12J1
LMRS1
E8 XRPB
K5 Q041
INH0
104-0
14D SEE NOTE1
13D 30-041 2275 DELAY LINE
07,01
13C 100Ω
09E 30-019 DELAY LINE 50ns
ADD STRAP FOR 750NS OMIT FOR 1μS
09C
750ns: PINS 06 AND 10
1MS: PINS 07 AND 10
11H
Q020 M7
Q081 F5
P5
1K 12D
1K 08E
10F 180
10F 220
1K 09D
1K 08S
105 1K
085 1K
N2 CMO
F7 SCLRIA
CL1
CL0
9F1
R5 SGFB0
N5 Q011
SGFB0
XRPC 9A1
Q011 9D4,9A2,D6
Q010 5E1
9E2 LNSRDO
10J9 FWDO
A2 RFI
9N3 ADU0
9C2 INSRDI
9G8 LMBSY1
L1 XRPF
11R1 MCR0A1
9E4 XRPG
11K1, J3 XRPF
CMO A5
STCLKA1
ADV1
STCLKB1
STCLKC1
750ns: 2 AND 13
1μs: 4 AND 13
11H
L8 QA0
L6 Q030
L8 QA0
IB5, J8 Q031
F7 SCLRIA
MCLR0 126-0
SCLRIA A6, IC5, H8
SCLR0A A1, 10A1
127-0 SCLRO
F2 XRPB
F5 Q081
L6 Q030
ERO 204-0
J4 Q031
QA1 9A2
QA0 L4, H4
SSFB0 D5
Q071 9J8, 11G4
Q061 9C5, 9D4
Q051 11K2
Q041 F3 11L3
Q021 9K2 9K7
Q080 IA5, 9A1, 9A8, 9J8, 11G4
Q070 9A1, 9D3, 9D4
Q060 9A1, 13C8, 11K2
Q050 IE5, 9A1
9H1 Q040
Q030 9A2, L4, 9D4, E9
Q020 IE5, 9A9, E4
12M8, 9C3, 9C5, 9D4
IA5, 9C5, 9D4
IE4, IB5, 9C3, 12M8,

NOTES
1. NOMINAL STRAPPING PINS 05 TO 14. FINAL STRAPPING TO BE DETERMINED IN TEST.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCT SCHEMATIC 8/32 LMI

TASK NO. 03088 SHEET 8 OF 12
DWG NO. 35-534 R09 D08

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS

REVISED PER MARKED PRINT			
JRB (RP)	03088-17	11-2674	R01
ADDED MNEMONICS TO THE FOLLOWING OUTPUTS; 10H08, 07C06, CHANGED: TAP ON 09F DELAY LINE WAS 06; MNEMONICS - Q010-Q080 WERE Q10-Q80; Q011-Q081 WERE Q11-Q81; C0D1-C021 WERE C01-C21.			
GL (JL)	03088-33	1-16-75	R02
CHANGED: LOC E4 ON 07C PINS 01 & 02 WERE Q080 & Q071; PIN 09E13 WAS Q41; PIN 10H08 WAS CONN TO 10U13. ADDED: LOC N7,8 - @ 14C A 30-019; @ 13C PINS 29 & 40 A 100Ω RES; @ 14A - 19-124 GATE OUTPUT PIN 08.			
GL (RP)	03088-35	1-16-75	R03
AREA D5: 07D-01, 07D-04 WERE ON MNEM Q041			
JC JRB	2841	5-11-76	R04
AREA H3: ADDED GATE 09D & RELATED CIRCUITRY. AREA N3: ADDED GATE 13M & RELATED CIRCUITRY. AREA C3: REVISED CIRCUITRY PER ECN# 3119. FOR PREV. REV. INFO SEE VOIDED COPY 35-534 D08, SHT 9, R04.			
WS AH	3179	5-11-77	R05
AREA G3 - 09D-08-11 AND RELATED CIRCUITRY WAS DELETED FROM ME			
GP JH	3537	3-16-78	R06

NOTES
1. UPPER ADDRESS LIMIT STRAP (0 ASSERTED) PIN 14 MOST SIGNIFICANT, SEE INSTALLATION SPEC. FOR STRAPPING DETAILS.
2. LOWER ADDRESS LIMIT STRAP (0 ASSERTED) PIN 14 MOST SIGNIFICANT, SEE INSTALLATION SPEC FOR STRAPPING DETAILS

BRUNING 44-231 16042

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 LMI

TASK NO. 03088
DWG NO. 35-534 R06 D08
SHEET 9 OF 12

PERKIN ELMER

REVISIONS				
REVISED PER MARKED PRINT				
JRB	PD	03088-17		11-26-74 R01
CHANGED: MNEMONICS C000-C020 WERE C00-C20, C001-C021 WERE C01-C21				
4/4	PD	03088-33		1-16-75 R02
AREAS F6, F7. ADDED CROSS-REF 9G3 TO MNEMONICS SXO REXO, RESA				
GS	JT	3179		5-17-77 R03
AREA F6-LOCATOR 9G3 WAS DELETED FROM SXO, LOCATOR 12E7 WAS 11E7. AREA F7-LOCATOR 9G3 WAS DELETED FROM EXO. AREA F7				
GP	JT	3537		13-1678 R04

9R8 ULMARO
8F8 SCLROA
08E 19-060 SG
01B 19-055 SG
LMARFO A2, A3, A4, A7
04F 08F 19-124 SB
9F3 ONEO
LMARF1 6A9, 7A8, 7G8, 7N4

2K6 LMB271
E1 LMARFO
00F 19-126 SG
C001 GG, 12E7, 9A3
01H 19-057 SG
C000

2N6 LMB281
E1 LMARFO
00F 19-126 SG
9A3, 9A7 C011
01H 19-057 SG
C010

2N6 LMB291
E1 LMARFO
01F 19-126 SG
9A3 C021
02F 19-057 SG
C020 12E7, 11A1, 11A7

2N6 LMB311
03F 19-126 SG
5X1
02F 19-057 SG
5XO 9B3, 11A1, 11A7, 12E7

2C6 LMB181
04F 19-126 SG
05H 19-057 SG
MWO 9A6, 12F7, 11A6
HW1 12F9, 11A1

2N6 LMB301
E1 LMARFO
01F 19-126 SG
EX1
02F 19-057 SG
EXO 9A3

2C6 LMB171
04F 19-126 SG
FWO
05H 19-057 SG
FW1
EVEN LMI: 03 AND 07
ODD LMI: 03 AND 05
2H
FWDO
03F 19-126 SG
FWD1 9D3
FWDO 1A4, 8J2, 9D4

9L6, 9A5 ID010
03E 19-055 SG
RDOP1 9D2, 12D7, 11A5, 11A8, 11F3
02E 19-058 SG
03D 19-059 SA
ID021 9A6, 11F1
03E 19-055 SG
ID030 9A5
04E 19-124 SB
WTE001 AB8, 4H8, 5B1, 5H1
02F 19-057 SG
WTE000 5G2, 11F1
WTE021 3A8, 3E8, 3H8, 3L8
WTE020 3J3
WTE011 4B8, 4H8, 5B1, 5H8
02E 19-058 SG
WTE010 5G2
05E 19-060 SG
02F 19-057 SG
RDSEL 2A4

NOTES

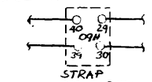
BRUNING 44-231 16042

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 LMI
TASK NO 03088
DWG NO 35534 RA008
SHEET OF 10-2

PERKIN ELMER

REVISIONS				
REVISED PER MARKED PRINT				
A	RR	03088-17	MB	11-24-74 R01
ADDED: MNEMONICS TO THE FOLLOWING OUTPUTS; 02C12, 05C08, 07E12, 07E08. CHANGED: MNEMONICS; CO20, Q081, Q011, Q060, Q051 WERE Q28, Q81, Q11, Q60 RESP.				
B	RR	03088-33	MB	1-16-75 R02
CHANGED: SHT LOC G4; Q080 WAS Q081, Q071 WAS Q011.				
C	RR	03088-44	MB	3-17-75 R03
LOC. G3: OGE-04 WAS TO MAKE IUS, ROO, CROSS-REF TO 8F8.				
WS	JJ	3/79	-	5-10-77 R04
AREA L4 WAS AS SHOWN BELOW:				
KR	JT	4250	MB	2-24-80 R05



NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC 8/32 LMI

TASK NO 03088 DWG NO 35-534 R05 D08 SHEET OF 11-12

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
REVISED PER MARKED PRINT				
PCB	03088-17	MB	11-26-74	R01
CHANGED: MNEMONICS; C001, C020 WERE C01 & C02 RESP.				
PCB	03088-33		1-16-75	R02
02801 WENT TO 02802 05A05 & 04 WERE CONN 06805 & 04 " "				
PCB	03088-03		4-11-75	R03

PARITY ERROR DETECT

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

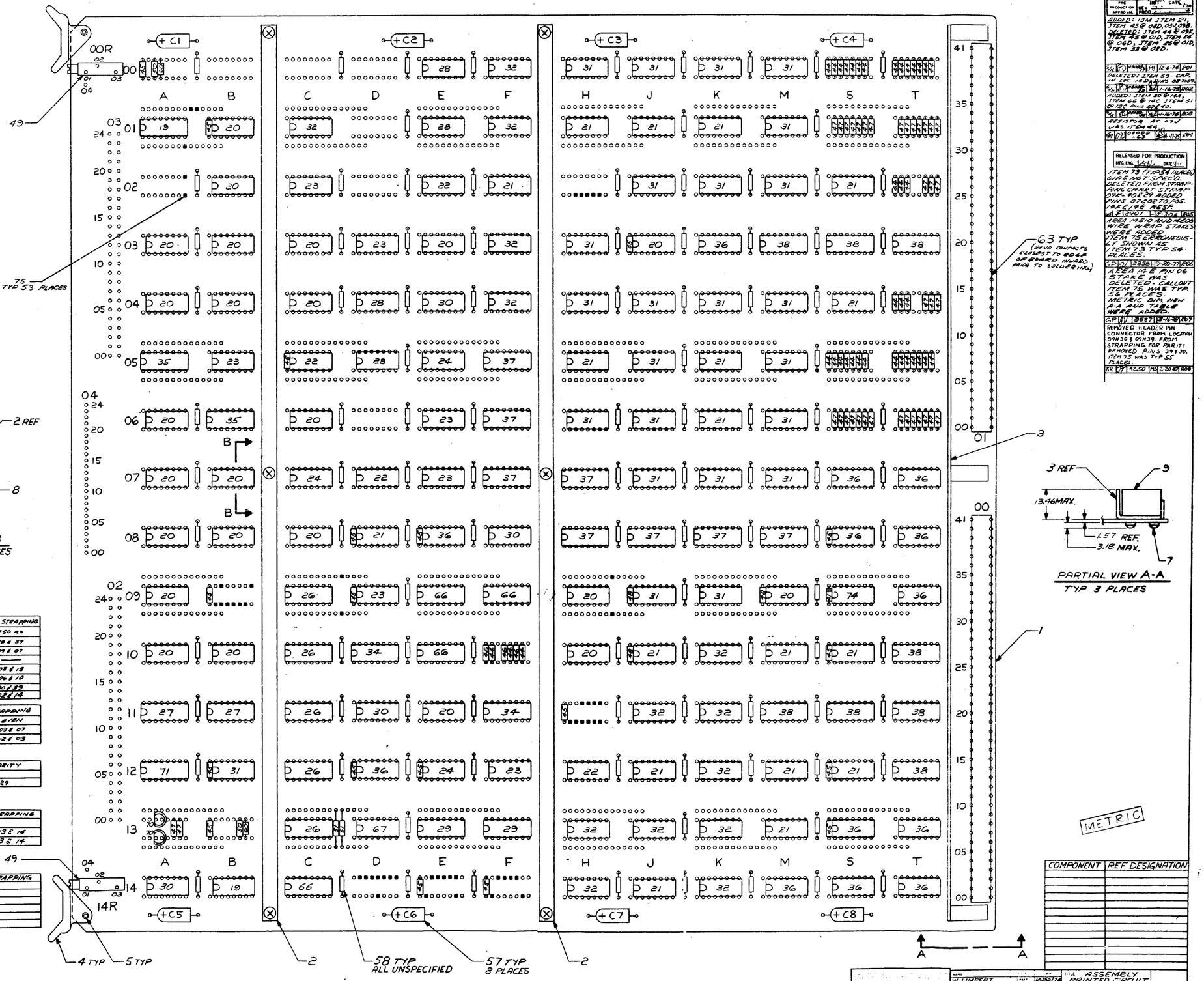
TITLE FUNCTIONAL SCHEMATIC
8/32 LMI

TASK NO 03088
DWG NO 35-5341 R03 D08

SHEET OF 12-12

BRUNING 44-231 16042

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530



1st & 750 nS 32KB STRAPPING		
POS.	1st	750 nS
01A	28 & 40	28 & 39
09B	01 & 06	04 & 07
	—	—
11N	04 & 13	03 & 13
11N	01 & 10	06 & 10
09C	30 / 39	30 / 39
09B	03 / 14	02 / 14

ODD & EVEN STRAPPING		
POS.	ODD	EVEN
02N	03 & 05	03 & 07
11N	12 & 05	12 & 03

STRAPPING FOR PARITY	
POS.	PINS
09H	40 AND 29

ADDRESS LIMIT STRAPPING	
POS.	PINS
14F	02, 07, 11, 12, 13 & 14
14E	02, 07, 11, 12, 13 & 14

64 KB MODULE STRAPPING	
01A	28 & 40
09B	03 & 06
09K	40 & 29
11H	04 & 13
11H	07 & 10
09B	03 & 14

REVISIONS

PRE PRODUCTION APPROVAL	INIT.	DATE
DEV		
PROD		

ADDED: 13M ITEM 21, ITEM 45 @ 04D, 09L09B. DELETED: ITEM 44 @ 09E, ITEM 45 @ 01D, 11M & @ 06D; ITEM 25 @ 01D, ITEM 33 @ 02D.

W	KD	PRODUCTION	MB	12-6-74 B01

DELETED: ITEM 53. CAP, .1M 10% 100 VOLTS OR MORE.

W	LP	PRODUCTION	MB	1-16-75 B02

ADDED: ITEM 80 @ 14A; ITEM 66 @ 14C & ITEM 51 @ 13C PINS 39 & 40.

W	KD	PRODUCTION	MB	1-16-75 B03

RESISTOR AT 09J WAS ITEM 44

SW	MD	030008 -03	MB	4-11-75 B04

RELEASED FOR PRODUCTION
MFG ENG. [illegible] DATE 4-11

ITEM 79 (TYP 54 PLACES) WAS NOT SPECIFIED. DELETED FROM STRAPPING CHART. STRAP 09K-40 & 29 ADDED. PINS 07 & 08 TO BE DELETED FROM RESPECTIVE AREA.

GP	MD	2907	8-3-76	B05

AREA 14E10 AND 14C06 WIRE WRAP STAKES WERE ADDED. ITEM 75 ERRONEOUSLY SHOWN AS ITEM 73 TYP 54 PLACES.

GP	MD	3358	10-20-77	B06

AREA 14E PIN 06 STAKE WAS DELETED. CALLOUT ITEM 75 WAS TYP 55 PLACES. METRIC DIM WHEN A-A AND TABLE WERE ADDED.

GP	MD	3537	8-12-78	B07

REMOVED HEADER PIN CONNECTOR FROM LOCATION 09N30 & 09N39. FROM STRAPPING FOR PARITY REMOVED PINS 39 & 30, ITEM 75 WAS TYP 55 PLACES.

KR	MD	42.50	MB	2-20-79 B08

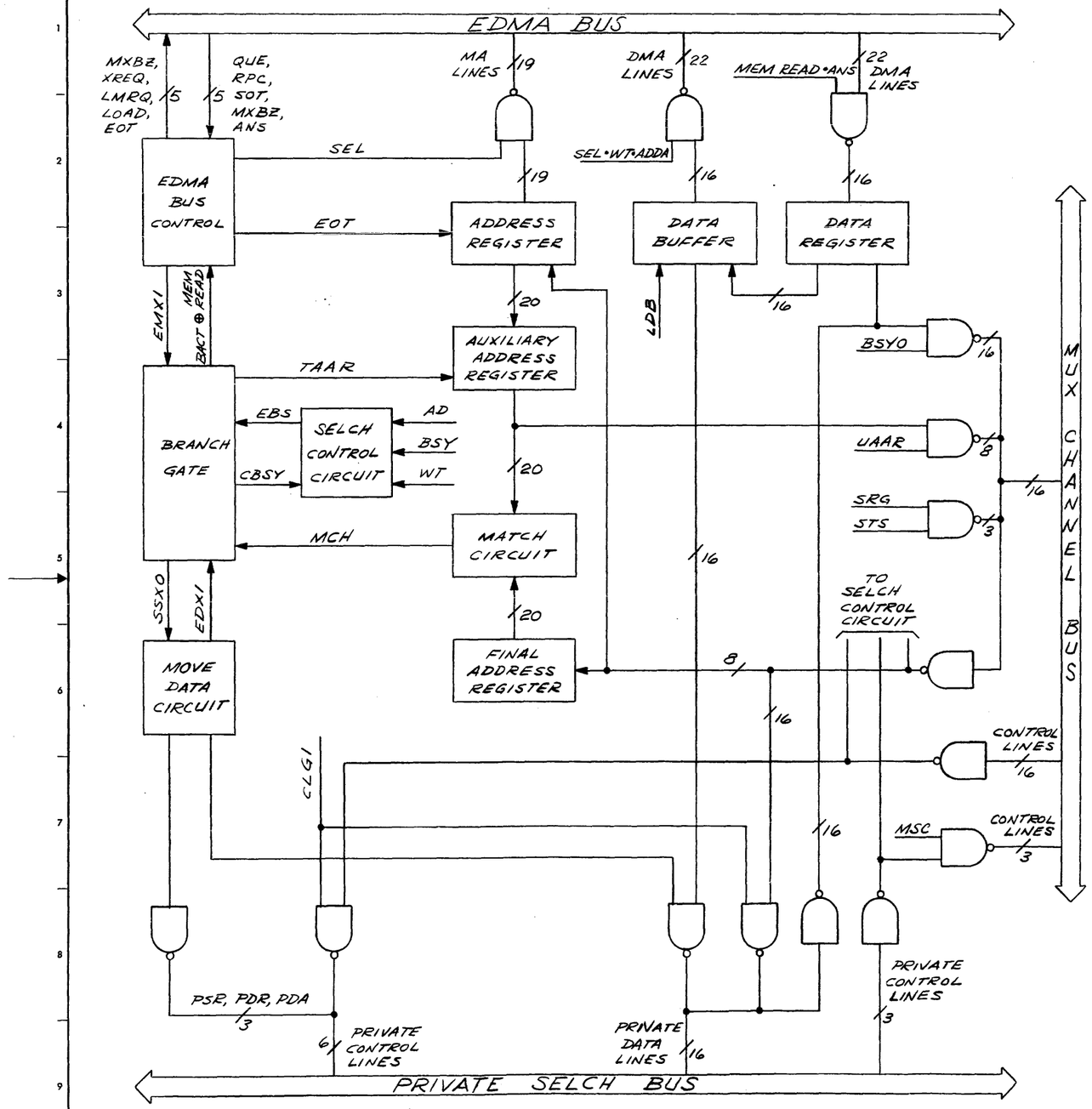
COMPONENT	REF DESIGNATION

DRAWN	W. LIMPERT	PART	10100176
ENGR	S. HOMEFIELD	DATE	12-6-74
CHK	S. CONNELLY	ENGR	
APPROVED		Q.C.	
	S. MESSINA	MFG.	

TITLE: ASSEMBLY PRINTED CIRCUIT MOD 8/32 CMI

SIZE D 030088 REV -35-53 & PREFOS

SHEET 1 OF 1



BACK PANEL MAP

ESELCH			CONN NO
ROW 1	TERM.NO.	ROW 2	
P5	41	GND	
GND	40	GND	
	39		
	38		
DMA170	37	DGND	
DMA150	36	DMA160	
DMA130	35	DMA140	
DGND	34	DMA120	
DMA110	33	DMA100	
DMA090	32	DMA080	
DMA070	31	DMA060	
DMA050	30	DGND	
DMA030	29	DMA040	
DMA010	28	DMA020	
DGND	27	DMA000	
SCLR0	26	PHW0	
	25		
	24		
PSYN0	23	PATN0	
	22	PTACK0	
PCL070	21	PDA0	
PDR0	20	PCMD0	
PSR0	19	PADRS0	1
PDI40	18	PDI50	
PDI20	17	PDI30	
PDI00	16	PDI10	
PDO80	15	PDO90	
PDO60	14	PDO70	
PDO40	13	PDO50	
PDO20	12	PDO30	
PDO00	11	PDO10	
	10	DMX140	
DMX150	09	DMX120	
DMX130	08	DGND	
M3B20	07	M2B20	
M1B20	06	M0B20	
LOAD0	05	ANS0	
LMRQ0	04	DGND	
SOT0	03	EOT0	
XREQ0	02	QUE0	
GND	01	GND	
P5	00	GND	
1	TERM.NO.	2	CONN.
P5	41	GND	
GND	40	GND	
	39		
	38		
RPC0	37	TPC0	
DGND	36	BH0	
	35		
	34		
	33		
	32		
	31		
	30		
	29		
	28		
	27		
SCLR0	26	HW0	
	25		
	24		
SYN0	23	ATN0	
RACK0	22	TACK0	0
CL070	21	DA0	
DR0	20	CMD0	
SR0	19	ADRS0	
DI40	18	DI50	
DI20	17	DI30	
DI00	16	DI10	
DO80	15	DO90	
DO60	14	DO70	
DO40	13	DO50	
DO20	12	DO30	
DO00	11	DO10	
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
GND	01	GND	
P5	00	GND	
1	TERM.NO.	2	CONN.

TEST POINTS

DESIG.	MNEMONIC	SHT. LOC.
A	ADIA	3N9
B	DXIA	4F8
C	MSCOA	4J5
D	BSYIB	4J3
E	SELIA	9K2
F	WTIA	4J6
G	SXIA	4F7

PRINTED CIRCUIT BOARD AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

ESELCH	35-508	M01 R08

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

SHEET INDEX	REV.	08	04	-	04	-	-	-	04	04
	SHT.	1	2	3	4	5	6	7	8	9

REVISIONS

RELEASED FOR PRODUCTION ENG. J. F. DATE 4/9/75

REVISED SHTS 2, 4, 8, & 9 ESELCH, 35508 M01, WAS R00					
PE	RC	2577	B	7-28-75	R01
REVISED SHTS 2&9, E SELCH, 35-508 M01 WAS R01					
AS	RC	2659	-	11-12-75	R02
REVISED SHTS 2&9, E SELCH, 35-508 M01 WAS R02					
AS	VA	2792	-	3-25-76	E03
REVISED SHT 9, E SELCH, 35-508 M01 WAS R03					
AS	RC	2825	-	5-11-76	R04
REVISED SHTS 2, 4 AND 8. 35-508 M01 WAS R04.					
GM	7	2908		7-7-76	R05
REVISED SHT. 4. 35-508 M01 WAS R05					
GM	7	2879	-	7-9-76	R06
REVISED SHT. 4. 35-508 WAS R06					
GM	7	2909	-	7-9-76	R07
REVISED SHTS. 2 AND 8 35-508 WAS 207.					
GP	WJ	3349		11-11-77	R08

NOTES

NAME	TITLE	DATE
J. F. FLEMING	DRAFT	4-1-75
R. CERO	CHK	4-11-75
J. YANG	ENGR	4-11-75
R. A. BARKER	Q.C.	4-17-75
D. FRANK-STARKEY	DES.	3-19-75

TITLE SCHEMATIC EXTENDED SELECTOR CHANNEL

TASK NO. 03055 DWG NO. 02-3508 M01 R08

SHEET OF 1-9

BRUNING 44-231 16042

REVISIONS			
AREA B1: CONNECTED A82-06,08,11, A82-02, & R38 TO MB20. AREA D1: CONNECTED A83-01, A82-07, R39, & R40 TO DMB20. A82-11 WAS NC			
PR	KC 2577	7-28-75	R01
AREA B1: A83-11,08&06 WERE REF TO 9L6 (MB20) AREA D1 A83-01 & 02 WERE REF TO 9J4 (DMB20)			
MR	KC 2659	11-12-75	R02
ADDED COORDINATE TO PHW0A (4G7) AT LOC G2			
MR	F 2908	7-7-76	R03
AREA 2L1 - A39 PIN 10 WAS CONNECTED TO BSYOA PIN 04			
GP	KC 3349	11-11-77	R04

NOTES
1. PREFERRED ADDRESS X'F0'.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: EXTENDED SELECTOR CHANNEL

TASK NO. 03055
DWG NO. 02-328M01 R04 D0E
SHEET OF 2 - 9

BRUNING 44-231 16042

REVISIONS

A131 19-118 QUAD BUS XCEIVER (SEE SH.1)

A130 19-118 QUAD BUS XCEIVER (SEE SH.1)

A107 19-118 QUAD BUS XCEIVER (SEE SH.1)

A106 19-118 QUAD BUS XCEIVER (SEE SH.1)

A79 19-069 8 TO 1 MUX

A91 19-069 8 TO 1 MUX

A103 19-069 8 TO 1 MUX

A115 19-069 8 TO 1 MUX

A127 19-069 8 TO 1 MUX

A139 19-069 8 TO 1 MUX

A151 19-069 8 TO 1 MUX

A163 19-069 8 TO 1 MUX

A94 19-065 2 TO 1 MUX

A119 19-065 2 TO 1 MUX

A118 19-065 2 TO 1 MUX

DATA LINES 00-07

PRIVATE DATA LINES 00-07

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: EXTENDED SELECTOR CHANNEL

TASK NO. 03055

DWG NO. 02-328M01 D08

SHEET OF 1-9

BRUNING 44-231 16042

REVISIONS				
AREA E1: A111-09 WAS CBSYO. A111-08 WAS TO A134-01. AREA G1: ADDED A170. AREA K1: A87-03 WAS CBSYO.				
PR	2577		7-28-75	R01
A125-04 WAS WT1. ADDED GATE A171 AT LOC. H7.				
SM	2908	-	7-7-76	R02
A134-02 WENT TO WT1(G)				
SM	2879	-	7-9-76	R03
A66-05 WENT TO PSYNIA				
SM	2909	-	7-9-76	R04

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

NOTES

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	

TITLE: EXTENDED SELECTOR CHANNEL

03055 02-328M-1R04D08 4-9

REVISIONS

AUXILIARY ADDRESS REGISTER

FINAL ADDRESS REGISTER

MATCH CIRCUIT

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: EXTENDED SELECTOR CHANNEL

TASK NO. 03055

DWG NO. 02-328M01 D08

SHEET OF 5-9

REVISIONS

LOAD/UNLOAD SEQUENCER

LOAD/UNLOAD SEQUENCER

ADDRESS REGISTER

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: EXTENDED SELECTOR CHANNEL

TASK NO. 03055 SHEET OF 6-9

DWG NO. 02-328M01 D08

BRUNING 44-231 16042

A59 19-038 4 TO 1 MUX
A71 19-038 4 TO 1 MUX
A35 19-038 4 TO 1 MUX
A47 19-038 4 TO 1 MUX
A46 19-071 HDFF
A23 19-065 2 TO 1 MUX
A11 19-065 2 TO 1 MUX
A22 19-071 HDFF
A10 19-071 HDFF
A32 19-071 HDFF
A126 19-089 HDFF
A114 19-024 HA
A111 19-015 HG
A101 19-016 HG
A451 19-027 T L O
A331 19-027 T L O
A211 19-027 T L O
A091 19-027 T L O
R65 1K
R2 1K

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE EXTENDED SELECTOR CHANNEL

TASK NO. 03055
ENG NO. 02-328M01 008
SHEET OF 7-9

BURROUGHS 44-231 16042

REVISIONS			
AREA 55: CBSYO DELETED 4K1 (CROSS REF)			
PE WC	2577	7-30-75	R01
AREA 88: A140 WAS SPEC'D AS 19-055			
WS WC	2792	3-25-76	R02
R50 WAS 3.3K (LOC B3)			
AM T	2908	7-7-76	R03
AREA F1, A172 WAS ADDED AREA F2, A148 - SINTO-F1 WAS ADDED TO PIN 03.			
GP WC	3349	11-11-77	R04

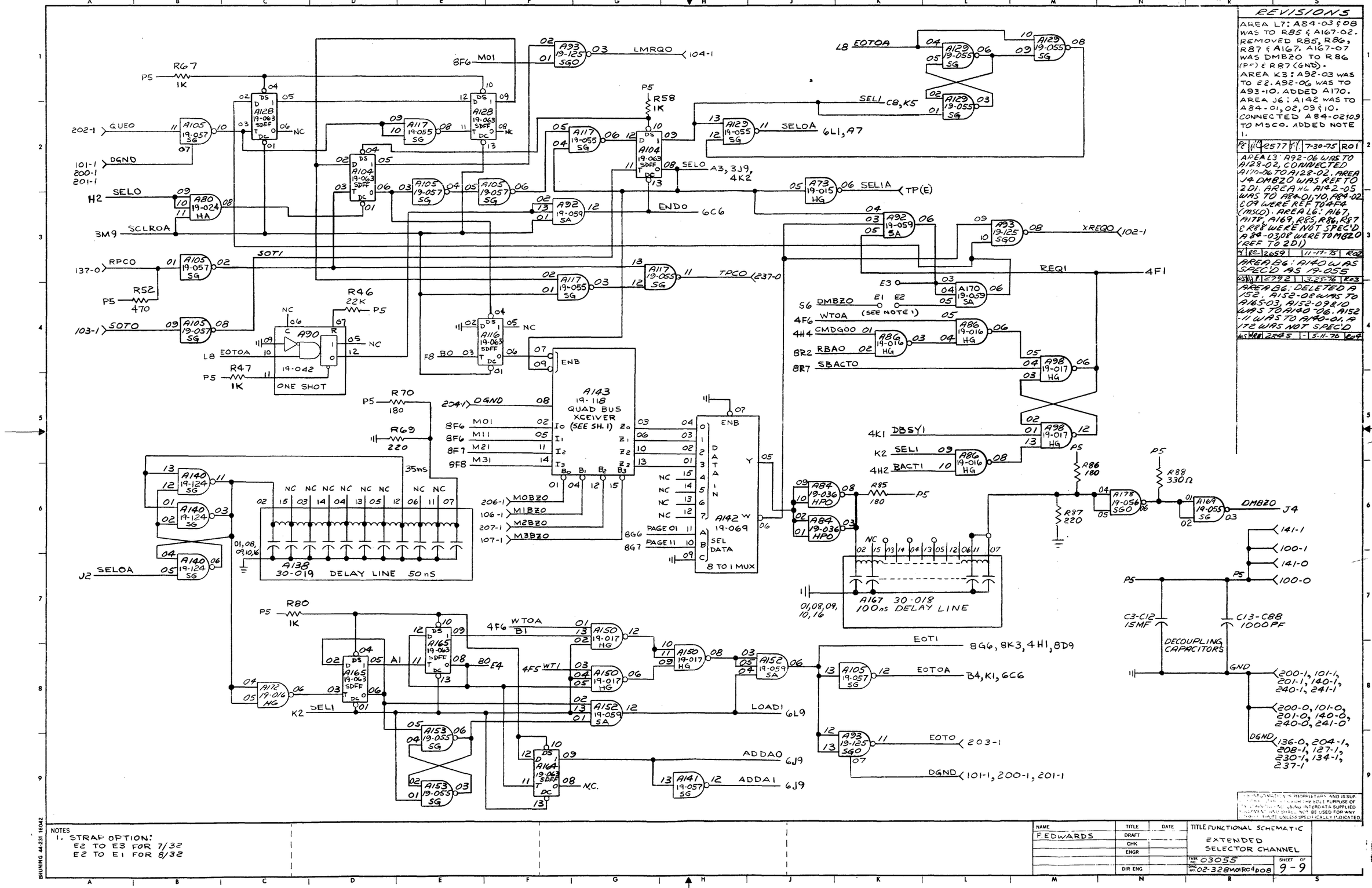
NAME	TITLE	DATE
EDWARDS	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNTIONAL SCHEMATIC
EXTENDED SELECTOR CHANNEL

TASK NO 03055 | DWG NO 02-328M01R04 DOB | SHEET OF 8-9

NOTES

BRUNING 44-231 16042


REVISIONS
AREA L7: A84-03 & 08 WAS TO R85 & A167-02. REMOVED R85, R86, R87 & A167. A167-07 WAS DMB20 TO R86 (P5) & RR7 (GND). AREA K3: A92-03 WAS TO E2. A92-06 WAS TO A93-10. ADDED A170. AREA J6: A142 WAS TO A84-01, 02, 09 & 10. CONNECTED A84-02 09 TO MSCO. ADDED NOTE 1.
PC 2577 BY 7-30-75 R01
AREA L3: A92-06 WAS TO A128-02, CONNECTED A110-06 TO A128-02. AREA J4 DMB20 WAS REF TO 2D1. AREA H6 A142-05 WAS TO A84-01, 10, A84-02 & 09 WERE REF TO 4F4 (MSCO). AREA L6: A167, A178, A169, R85, R86, R87 & R88 WERE NOT SPECD. A84-03, 08 WERE TO DMB20 (REF TO 2D1)
PC 2659 11-19-75 R02
AREA B6: A140 WAS SPECD AS 19-055
PC 2792 3-25-76 R03
AREA B6: DELETED A152. A152-08 WAS TO A165-03, A152-09 & 10 WAS TO A140-06. A152-11 WAS TO A140-01. A172 WAS NOT SPECD
PC 2845 5-11-76 R04
R67 1K
R58 1K
R46 22K
R52 470
R47 1K
R70 180
R69 220
R80 1K
R85 180
R86 180
R87 220
R88 330Ω
A105 19-057 SG
A117 19-055 SG
A128 19-063 SDFF
A104 19-063 SDFF
A116 19-063 SDFF
A165 19-063 SDFF
A164 19-063 SDFF
A80 19-024 HA
A92 19-059 SA
A93 19-125 SGO
A129 19-055 SG
A73 19-015 HG
A170 19-059 SA
A86 19-016 HG
A98 19-017 HG
A84 19-036 HPO
A178 19-056 SGO
A169 19-055 SG
A90 19-042 ONE SHOT
A143 19-118 QUAD BUS XCEIVER
A142 19-069 8 TO 1 MUX
A140 19-124 SG
A138 30-019 DELAY LINE 50nS
A167 30-018 100nS DELAY LINE
A172 19-016 HG
A150 19-017 HG
A152 19-059 SA
A153 19-055 SG
A141 19-057 SG
QUEO
DGND
SELO
SCLROA
RPCO
SOTO
SOT1
EOTOA
SELI
SELOA
ENDO
SELIA
TP(E)
XREQO
REQ1
4F1
TPCO
DMBZO
WTOA
CMDQ00
RBAO
SBACTO
DBSY1
BACT1
LMRQO
M01
M11
M21
M31
M0BZO
M1BZO
M2BZO
M3BZO
WTOA B1
WT1
BO
A1
LOAD1
ADDA0
ADDA1
EOTO
EOTI
ENB
DATA IN
SEL DATA
J2
J4
C3-C12 15MF
C13-C88 1000PF
DECOUPLING CAPACITORS
GND
DGND
35nS
NOTES
1. STRAP OPTION:
E2 TO E3 FOR 7/32
E2 TO E1 FOR 8/32
NAME P. EDWARDS
TITLE DRAFT
CHK
ENGR
DIR ENG
DATE
TITLE FUNCTIONAL SCHEMATIC
EXTENDED SELECTOR CHANNEL
TASK NO. 03055
DWG NO. 02-328M01RC4D08
SHEET 9 OF 9
BRUNING 44-231 16042

REVISIONS			
RELEASED FOR PRODUCTION			
MFG ENG.		DATE	
REMOVED R85 (NEAR A160 ITEM 49), R86 (R87 (NEAR A168) ITEM 49 (44 RESP. AND A167 ITEM 63. REMOVED STRAPS FROM E1 TO E4 (EE TO EG. ADDED STRAPS (1) THRU (4) REVISED TO SHOW ROZ COPPER.			
A	DC-A5772	B	10-30-78 BD1
REROUTED STRAPS 2 ADDED STRAPS 5,6&7, ADDED PADS & VIAS, RELOCATED E1, E2, E4, ADDED R90 & R91, ADDED & REVISED CIRCUITRY TO REFLECT NEW ARTWORK			
B	DC-A5772	-	11-17-78 AM
ADDED CAPS C870 AS ITEM 29, DELETED C76 (ITEM 57) WERE NOT SPECD			
C	12792	-	3-27-79 BB
REVISED CIRCUITRY TO REFLECT NEW ARTWORK. STRAPS WERE NOT SPECD			
D	12792	B	5-11-79 BB
PAD WAS ITEM 61, STRAPS 10 (11 WERE NOT SPECIFIED. REVISED CIRCUITRY TO REFLECT NEW ARTWORK			
E	12908	-	7-8-79 BB
REVISED CIRCUITRY TO REFLECT NEW ARTWORK			
F	2879	-	7-8-79 BB
REVISED CIRCUITRY TO REFLECT NEW ARTWORK & E.C.			
G	12908	-	7-8-79 BB
REVISED CIRCUITRY TO REFLECT R88 NETWORK, ADDED STRAPS 12, 13, 14			
H	13949	-	10-26-79 BB

SEE NOTE 1

GO SEE NOTE 2

APP SIDE

61 TYP. 72 PLACES

VIEW B-B

57 TYP. 76 PLACES C13 THRU C88 N.L UNSPECIFIED

11 TYP. PLACES

1.38

2.50

65 REF

3 REF

9

.530 MAX

.062 REF.

.125 MAX.

7

PARTIAL VIEW A-A

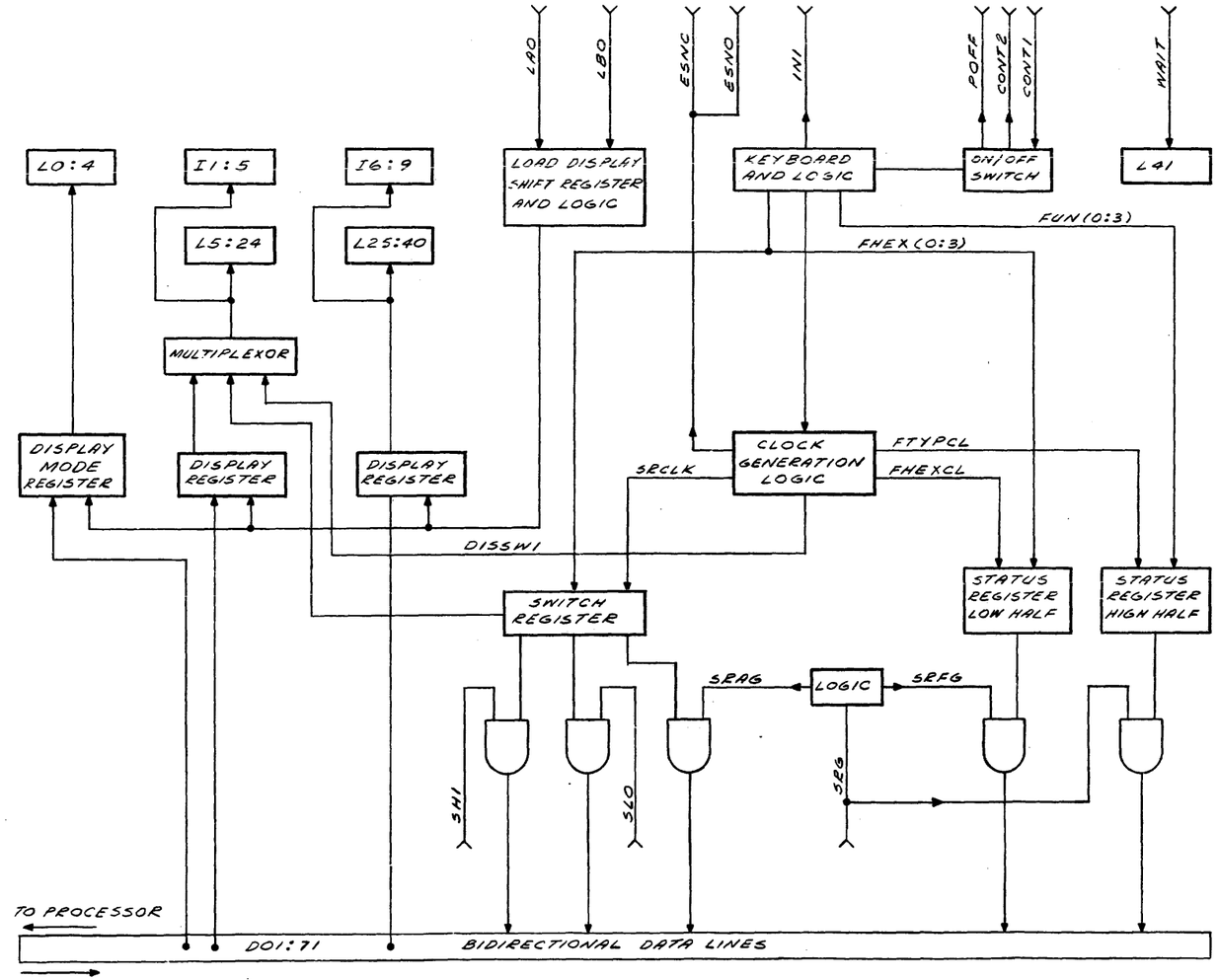
NOTES:
1. HEADER STIFFENER (ITEM 3) TO BE SOLDERED TO GND BUS AT 2 ENDS AND CENTER (APP. SIDE).
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BEND INWARD PRIOR TO SOLDERING.

65 ADD TAPE AS SHOWN & WRAP EDGES AROUND STIFFENER

COMPONENT	REF DESIGNATION
INT CKT	A02-A12, A14-A63, A65-A109, A111-A166 AND A173, A175-A180
CAPACITOR	C1-C75, C77-C88
RESISTOR	A1-R88
STRAPS	14 REQ'D

VALUE	TOL	DATE	TITLE
1 PROT	DRAFT	3/22/78	ASSEMBLY
2 CERO	CHK	3/24/78	INTERFACE REGULATOR
3 TRNG	ENGR	4/11/78	CHANNEL (8 BAUD)
4 SUPER	C	4/17/78	SIZE DWG NO
TOLER	UNLESS OTHERWISE SPECIFIED		

8-01



BLOCK DIAGRAM

CONN-3		
TERM	ROW 1	ROW 2
00	GND	SHIO
01	INITO	GND
02	WAIT1	D41
03	ESNCO	LAO
04	ESNOO	D51
05	POFFO	D61
06	SSGL1	SLOO
07	SCLRO	
08	GND	D71
09	DO1	
10	D11	
11	D21	
12	D31	GND
13	SRGO	CONT3
14	LBO	

REVISIONS

RELEASED FOR PRODUCTION MFG ENGR [illegible] DATE 2/14/74			
REVISED SHTS 2 & 3			
VLSI	2323	-	1-31-75 R01
REVISED SHTS 2 & 3			
WS	7	2635	- 12-10-75 R02
REVISED SHT 2			
GPD		3590	2-15-78 R03

REVISION LEVEL OF THIS SHEET IS CONSIDERED THE REVISION LEVEL OF THE DOCUMENT

35-519F02 R06	HEXADECIMAL DISPLAY

SHEET INDEX				
REV	3	2	0	
SHT	2	3	4	

NOTES

NAME	TITLE	DATE
H. MATTER	DRAFT	1-28-74
H. MATTER	CHK	1-28-74
S. MESSINA	ENGR	1-31-74
L. JOHMANN	TEST	1-31-74
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC HEXADECIMAL DISPLAY

TASK NO. 03081
DWG NO. 09-065 R03 D08
SHEET 1 OF 4

BRUNING 44-231 16042

REVISIONS				
AREA L1: CONNECTIONS 21, 22, 923 WERE DIRECTY CONNECTED TO 1W, 5W, & 9W RESP. CROSS REF ALL CONN 3 PIN NOS. TO SHEET 3. AREA G8: C7 WAS 4.7uF. C8 WAS 15uF				
PC	WK	2323	/	1-31-75	R01
AREA K1: ADDED JUMPER BETWEEN POINTS 03 & 05 AREA L6-L8, A61 02-04 WERE TO A61 10 & 13				
WS	F	2635	/	12-10-75	R02
AREA R5 R42 WAS 150Ω				
GP	JV	3590		12-15-78	R03

NOTES
1. L0 THRU L42 ARE 33-027

NAME	TITLE	DATE
P. EDWARDS	DRAFT	12-5-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
HEXADECIMAL DISPLAY

TASK NO 03081
DRG NO 09-065 03 D08
SHEET OF 2 - 4

REVISIONS				
AREA A1-A4, B1-B4: ADDED CROSS REF. FROM SHT. 2.				
PE	VGH	2323	—	1-31-75 R01
AREA B2. ADDED SCLRO REF. FROM SHT 2				
WS	JK	2635	—	12-11-75 R02

DBI-C3 CONT3
213-3 TP
214-3 TP
DBI-C2 23 CONT2 2J1
DBI-C1 CONT1 2L2
106-3 14 SSGLI 2J6
107-3 9 SCLRO J1, 2J6
105-3 22 POFFO 2J1
101-3 12 INITO 2H1
103-3 15 ESNCO 2S7
104-3 16 ESNOO 2S7
113-3 17 SRGO 2L2
102-3 10 WAITI 2M5
206-3 18 SLOO 2L3
200-3 20 SHIO 2L3
114-3 19 LBO 2L5
203-3 13 LAO 2K5
208-3 D71 4
205-3 D61 3
204-3 D51 2
202-3 D41 1
112-3 D31 8
111-3 D21 7
110-3 D11 6
109-3 D01 5
2L3 XRPI
2L4 LAI

FUN00 2D9
FUN10 2C9
SSLO 2G7
FUN20 2C9
SORO 2K7
FUN30 2D9
FTYPCLO 2N7
SCLRO J1
SORI 2J7
SSLI 2G7
HEX01 2B9
HEX11 2B9
HEX21 2A9
HEX31 2A9
FHEXCLO 2N8
SCLRO B2
R78 1K P5 E1

A46 19-071
A56 19-071
A57 19-043 HGO
A45 19-036 HPO
A35 19-036 HPO
R81 1K P5
R80 1K P5

2M2 FROO1
2M2 FROOO
2M2 SRGI
2R2 SRFG1

A1 19-071
A8 19-109 HGO
L1 L2 L3 L4
R2 R3 R4 R7 150
LP5
LAOA 2N5
LDE1 2R4

P5
R64 R63 R65 R62 R61 R60 R59 R58 330 (TYP.)
R68 R69 R70 R71 R72 R73 R74 R75 470 (TYP.)

D71 4A4
D61 4A4
D51 4A4
D41 4A4
D31 4A4
D21 4A4
D11 4A4
D01 4A4

2R4 LDBI
R79 1K P5

A26 4 BIT SHIFT REG. 19-030
A25 19-030 4 BIT SHIFT REG.
A24 19-030 4 BIT SHIFT REG.
A23 19-030 4 BIT SHIFT REG
SHR SHL SER IN MODE CONT

A7 19-109 HGO
A6 19-109 HGO
A5 19-109 HGO
L40 L39 L38 L37
L36 L35 L34 L33
L32 L31 L30 L29
L28 L27 L26 L25
R38 R39 R41 R40 150
R34 R35 R37 R36 150
R30 R31 R33 R32 150
R26 R27 R29 R28 150
LP5 4A8

A17 33-029 HEX DISPLAY
A16 33-029 HEX DISPLAY
A15 33-029 HEX DISPLAY
A14 33-029 HEX DISPLAY

LP5 — L GND
33MF, 10V
C1 & C2

P5 — GND
33MF, 10V
C3 TO C6

P5 — L GND
0.1MF, 30V
C10 TO C14

P5 — GND
0.1MF, 30V
C15 TO C39

DECOUPLING CAPACITORS

NOTES

NAME	TITLE	DATE	TITLE FUNTIONAL SCHEMATIC
P EDWARDS	DRAFT	12-3-73	HEXADECIMAL DISPLAY
	CHK		
	ENGR		
	DIR ENG		TASK NO 03081 ENG NO 09-065R02 D08 SHEET OF 3-4

BRUNING 44-231 16042

REVISIONS

2B9 HEX01
2B9 HEX11
2A9 HEX21
2A9 HEX31
2M7 SRCLKO
2H2 SDAO
2N3 SL01
2N2 SHI1
2R2 SRAS1
3R4 D71
3R4 D61
3R5 D51
3R5 D41
3R5 D31
3R5 D21
3R5 D11
3R5 D01
2R4 LDC1
LDD1 2R4
LDE1 2R3
XRP1 2L3
3L8 LP5
DISSWI 2N6

SW161 SW171 SW181 SW191
SW121 SW131 SW141 SW151
SW081 SW091 SW101 SW111
SW041 SW051 SW061 SW071
SW001 SW011 SW021 SW031

A55 A54 A53 A52 A51 — 19-071 (D 1, CLK 09, CLR 01)

A44 A43 A42 A41 A40 — 19-036 HPO / HGO

A34 A33 A32 A31 A30 — 19-030 4 BIT SHIFT REG

A22 A21 A20 A19 A18 — 19-053 2:1 MUX. (ENB 15, SEL 01)

A5 A4 A3 A2 A8 — 19-109 HGO

L24 L23 L22 L21 L20 L19 L18 L17 L16 L15 L14 L13 L12 L11 L10 L9 L8 L7 L6 L5

R23 R24 R25 R22 R19 R18 R20 R21 R16 R15 R14 R17 R12 R11 R10 R13 R8 R9 R6 R5 — 150

A13 A12 A11 A10 A9 — 33-029 HEX DISPLAY (LP5)

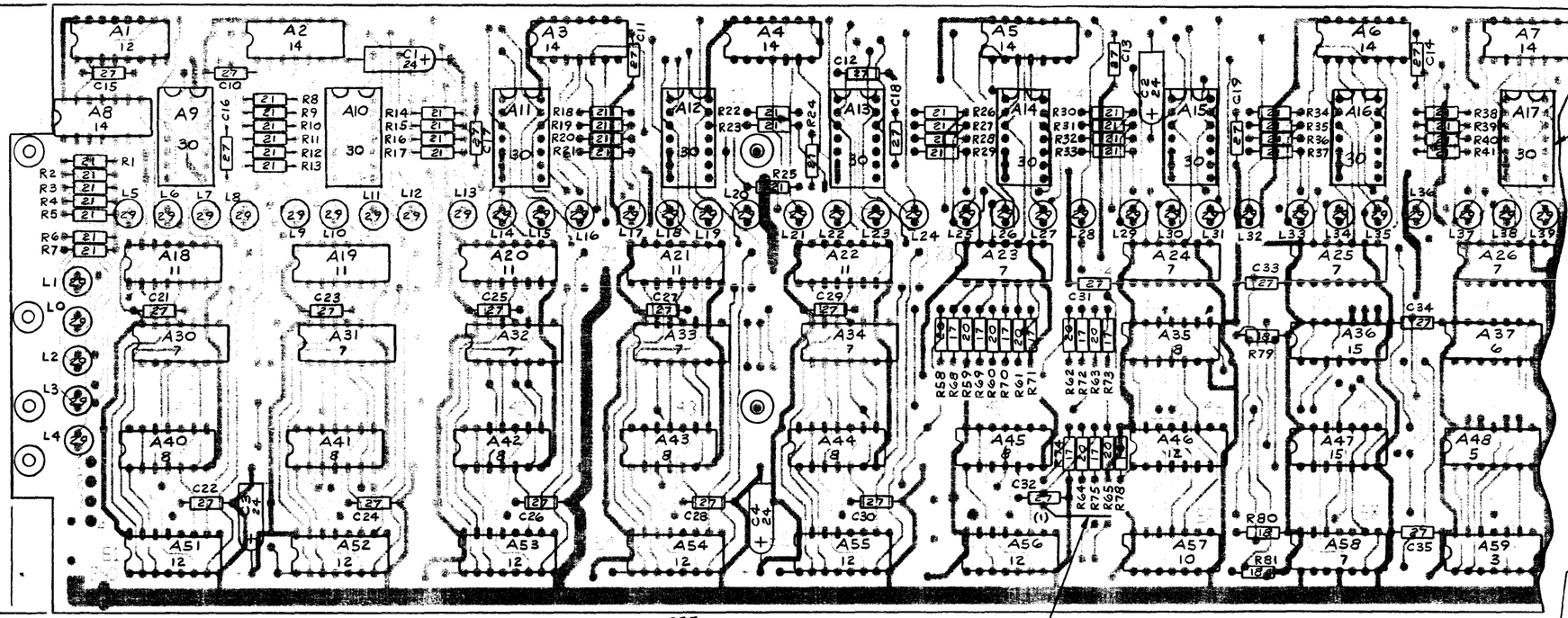
NOTES

NAME	TITLE	DATE
P.EDWARDS	DRAFT	12-3-73
	CHK	
	ENGR	
	DIR ENG	

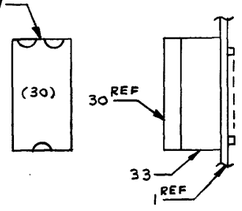
TITLE FUNCTIONAL SCHEMATIC HEXADECIMAL DISPLAY

TASK NO. 03081 DWG NO. 09-065 D08 SHEET OF 4-4

BRUNING 44-231 16042



DISPLAY TO BE INSERTED IN SOCKET WITH NOTCHES AS SHOWN



DETAIL A
FOR USE ON F02 ONLY

MILLIMETER	INCH
116.84	4.60
443.74	17.47

F02	AS SHOWN
F01	LESS ITEMS 30 & 33
VARIATION INFORMATION	

NOTES:
1. UNSPECIFIED COMPONENTS ARE ITEM 28.

REVISIONS

RELEASED FOR PRODUCTION
MFG. ENG. MB DATE 3-20-74

REVISED TO REFLECT R02 COPPER

DE	GEH	2152		4-15-74	R01

CHANGED ORIENTATION NOTE FOR LEDS. DID NOT SPC. FLAT SIDE

GM	GEH	2074	GM	5-28-74	R02

REVISED R86, WAS IN HORIZONTAL POSITION AREA - A27

9A	GEH	2261	-	9-5-74	R03

REVISED CIRCUITRY TO REFLECT NEW COPPER. STRAP #1 WAS NOT SPEC'D.

WS	FF	2635	-	12-11-75	R04

REVISED CIRCUITRY TO REFLECT R05 COPPER. R42 WAS ITEM 21, 150 Ω.

GP	JV	3590		2-16-78	R05

CHANGED TO METRIC 4-28-78 G.S.

P. EDWARDS	DRFT	1-16-74	ASSEMBLY, PRT. CKT. HEXIDECIMAL DISPLAY
H. MATTER	CHK	19 FEB 74	
S. MESSINA	ENG	2-15-74	03081
S. MESSINA	MGR	2-15-74	35-519 R05 D03 1-1

NOTES

NAME	TITLE	DATE
J. NESTOR	DRAFT	6-12-74
R.E. CERO	CHK	6-17-74
P.E. MALAS	ENG	7-31-74
H. E. [illegible]	PC	7-31-74
[illegible]	MGR.	7-31-74

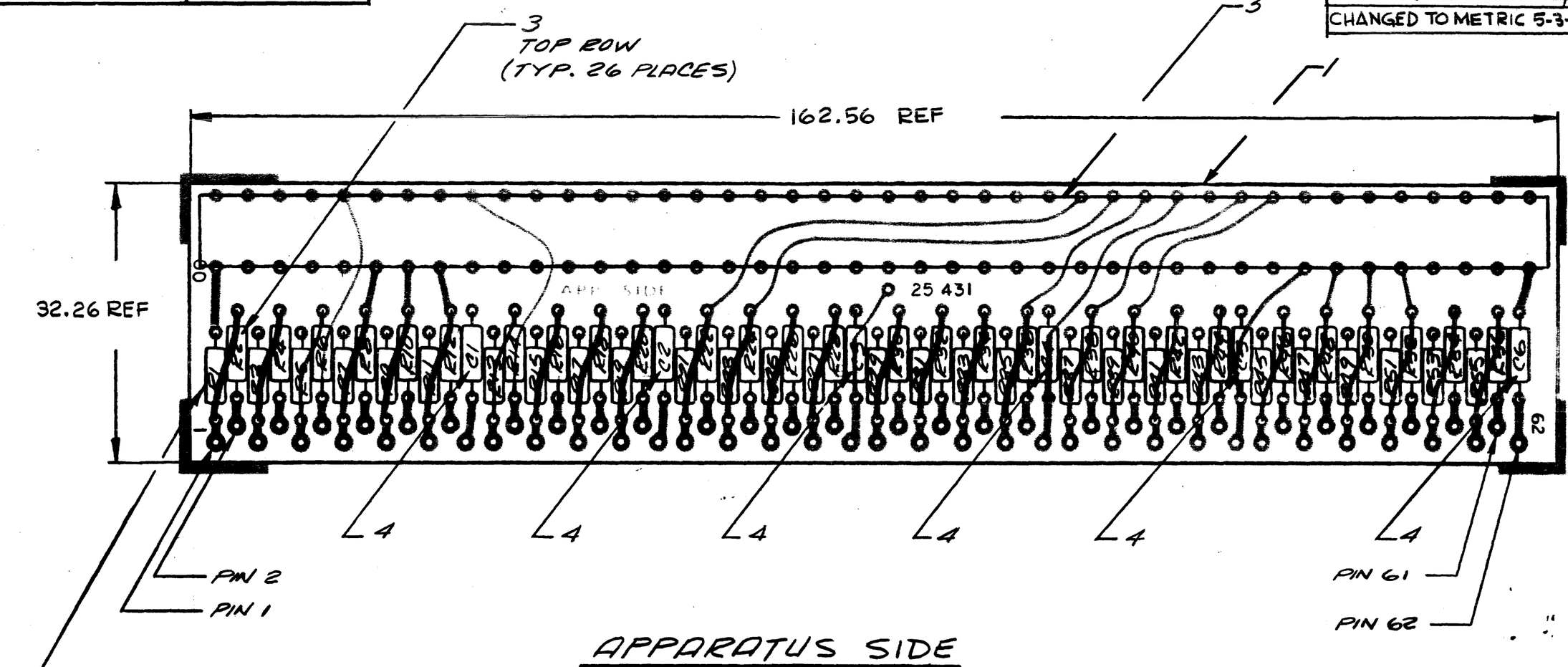
TITLE: FUNCT. SCHEMATIC DMA TERMINATOR BUS SIDE

TASK NO. 13047 DWG NO. 30-548 108 SHEET 1 OF 1

Transcribed 7/31/74
D.E. 6-14
Check. 6-14

MILLIMETER	INCH
162.56	6.40
32.26	1.27

PRE PRODUCTION APPROVAL	INIT DATE DEV ~~DUE 6-74~~ PROD. Week 6-14-74
RELEASED FOR PRODUCTION MFG. ENG. [signature] DATE 7/31/74	
CHANGED TO METRIC 5-3-78, GM	



APPARATUS SIDE

METRIC

NOTES

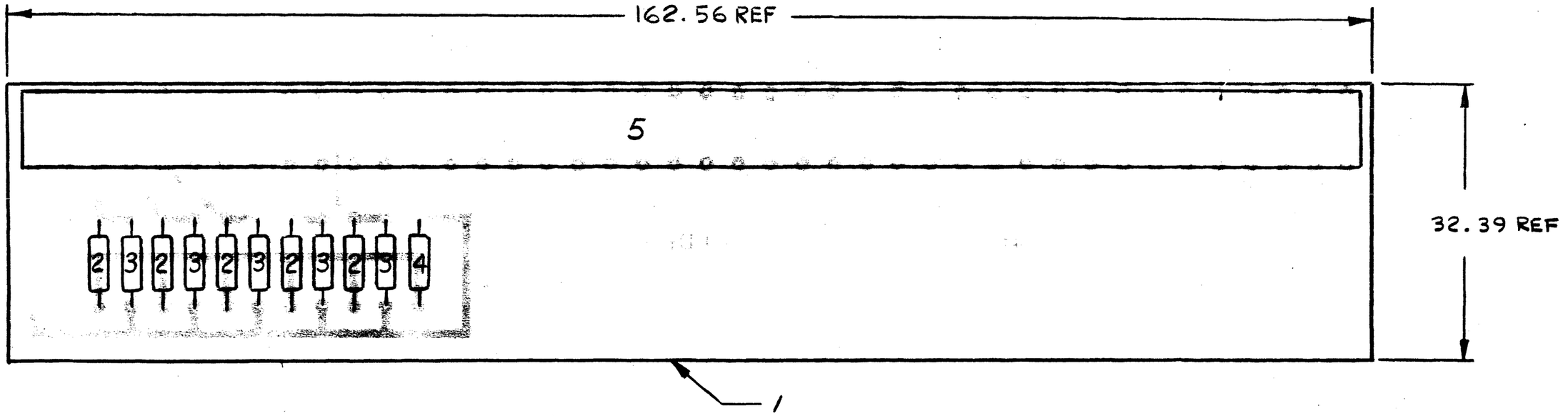
NAME	TITLE	DATE
G. MELTON	DRAFT	6-6-74
P.F. CERO	CHK	6-14-74
P. BALAS PD	ENGR	7-3-74
H ROSS	Q.C.	7-31-74
D. FRANKENBERGER	MGR	7-31-74

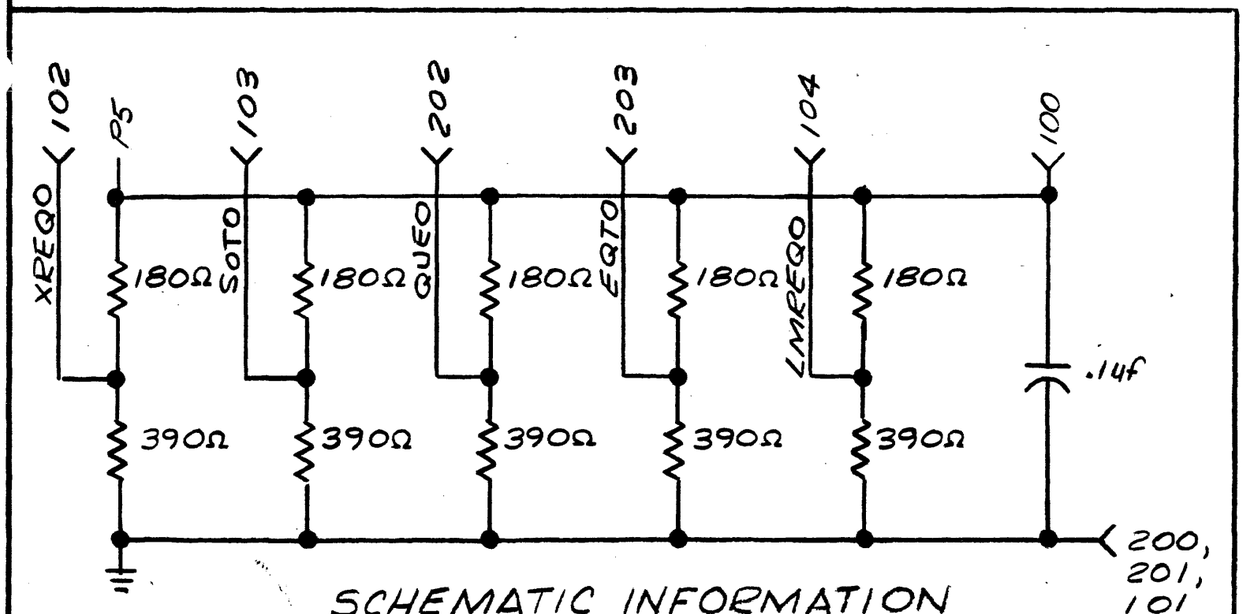
TITLE P.C. ASSEMBLEY
DMA TERM
BUS SIDE

TASK NO. 03047

DWG. NO. 35-548 803

SHEET 1 OF 1





SCHEMATIC INFORMATION

MILLIMETER	INCH
162.56	6.40
32.39	1.275

METRIC

REVISIONS

	INIT	DATE
PRE PRODUCTION	DEV	1-30-75
APPROVAL	PROD. NB	12-20-74

RELEASED FOR PRODUCTION
MFG. ENG. E. Ponzio DATE 3-5-75

CHANGED TO METRIC
5-3-78, GM.

NOTES:

NAME	TITLE	DATE
G. MELTON	DRAFT	11-12-74
H. MATTER	CHK	12-20-74
D. FRANKENBERGER	ENGR	3-5-75
R.A. BARKER	QC	3-5-75
	DIR ENG	

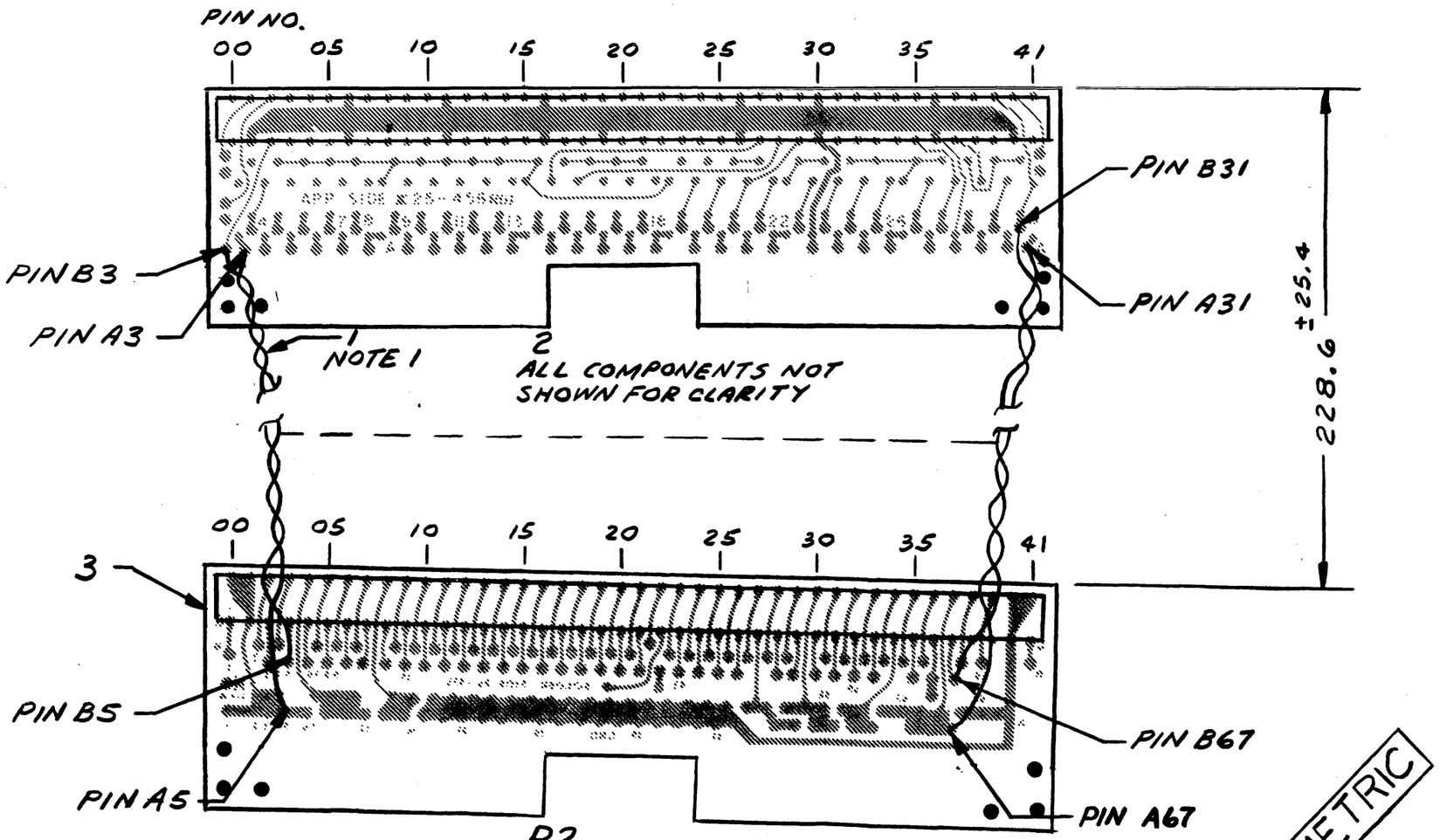
TITLE P.C. ASSEMBLY
TERMINATOR BOARD
7/32

TASK NO. 05132
DWG NO. 35-572 B03

SHEET OF 1 - 1

MILLIMETER	INCH
228.6 ± 25.4	9.00 ± 1.00

P1
APPARATUS SIDE



P2
(COPPER SHOWN IS SOLDER SIDE)
APPARATUS SIDE

METRIC

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	T.A. FYFE	
PROD	V. GUPTA	

RELEASED FOR PRODUCTION
MFG. ENG. V. Gupta DATE 5-2-75

CHANGE TO METRIC
5-3-78 GM

EXTENSIVE CHANGES FOR ROO
SEE PREVIOUS MICRO-FILM COPY.

KR	4009	R	10-4-79	ROI

NOTES
1. MAINTAIN 3 TWISTS PER INCH (MIN) ON ALL TIP WIRES. INSULATION PORTION OF ALL WIRES MUST ENTER TURRET HOLE & NOT EXTEND BEYOND SOLDER SIDE OF P.C. BOARD.

SCALE—

TOLERANCE:
.XXX ± .005
.XX ± .02
.X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	9-25-74
G. HOMEFIELD	CHK	2-3-75
T. FYFE	ENGR	5-2-75
R.A. BARKER	QC	5-2-75
S. MESSINA	MGR	5-2-75

TITLE
CABLE ASSEMBLY
DMA/MBC

TASK NO. 03088
DWG. NO. 17-336 R01 B03
SHEET OF 1 — 1

2 Crescert Place, Oceanport, New Jersey 07757

REVISIONS

	UNIT	DATE
PRE PRODUCTION APPROVAL	DEV G.J.S	11/26/74
	PROD	

RELEASED FOR PRODUCTION
DATE 3/4/75

P5

100-0
200-0
141-0
202-0 RM1 01 330 16 — 01 RM2 16
203-0 RM1 02 330 — 15 RM2
102-0 RM1 03 330 — 14 RM2
103-0 RM1 04 330 — 13 RM2
208-0 RM1 05 330 — 12 RM2
109-0 RM1 06 330 — 11 RM2
108-0 RM1 07 330 — 10 RM2
209-0 RM1 08 330 — 09 RM2
107-0 RM1 09 330 — 08 RM2
210-0 RM1 10 330 — 02 RM2
105-0 RM1 11 330 — 06 RM2
104-0 RM1 12 330 — 05 RM2
207-0 RM1 13 330 — 04 RM2
205-0 RM1 14 330 — 07 RM2
204-0 RM1 15 330 — 03 RM2
110-0 RM3 01 330 16 — 15 RM4 16
112-0 RM3 02 330 — 14 RM4
212-0 RM3 03 330 — 13 RM4
213-0 RM3 04 330 — 12 RM4
101-0
201-0
106-0
206-0

C1 0.1 μF

115-0 RM3 05 330 — 11 RM4
117-0 RM3 06 330 — 10 RM4
118-0 RM3 07 330 — 09 RM4
119-0 RM3 08 330 — 08 RM4
219-0 RM3 09 330 — 07 RM4
218-0 RM3 10 330 — 06 RM4
217-0 RM3 11 330 — 05 RM4
215-0 RM3 12 330 — 04 RM4
214-0 RM3 13 330 — 03 RM4
114-0 RM3 14 330 — 02 RM4
113-0 RM3 15 330 — 01 RM4
122-0 RM5 01 330 16 — 01 RM6 16
120-0 RM5 02 330 — 15 RM6
220-0 RM5 03 330 — 11 RM6
123-0 RM5 04 330 — 14 RM6
222-0 RM5 05 330 — 13 RM6
225-0 RM5 06 330 — 12 RM6
128-0 RM5 07 330 — 10 RM6
229-0 RM5 08 330 — 09 RM6

GND

129-0 RM5 09 330 — 08 RM6
228-0 RM5 10 330 — 07 RM6
227-0 RM5 11 330 — 06 RM6
224-0 RM5 12 330 — 05 RM6
125-0 RM5 13 330 — 04 RM6
223-0 RM5 14 330 — 03 RM6
124-0 RM5 15 330 — 02 RM6
130-0 RM7 01 330 16 — 09 RM8 16
230-0 RM7 02 330 — 06 RM8
132-0 RM7 03 330 — 07 RM8
133-0 RM7 04 330 — 08 RM8
237-0 RM7 09 330 — 05 RM8
235-0 RM7 10 330 — 11 RM8
234-0 RM7 11 330 — 10 RM8
233-0 RM7 12 330 — 04 RM8
135-0 RM7 13 330 — 03 RM8
232-0 RM7 14 330 — 02 RM8
134-0 RM7 15 330 — 01 RM8
209-1 RM9 05 330 16 — 04 RM10 16

C2 0.1 μF

P5

107-1 RM9 06 330 — 03 RM10
109-1 RM9 07 330 — 14 RM10
110-1 RM9 08 330 — 15 RM10
108-1 RM9 10 330 — 01 RM10
210-1 RM9 11 330 — 02 RM10
201-1 RM9 12 330 — 08 RM10
203-1 RM9 13 330 — 07 RM10
207-1 RM9 14 330 — 06 RM10
208-1 RM9 15 330 — 05 RM10
214-1 RM11 01 330 16 — 05 RM12 16
120-1 RM11 02 330 — 15 RM12
219-1 RM11 03 330 — 14 RM12
119-1 RM11 04 330 — 13 RM12
117-1 RM11 05 330 — 12 RM12
215-1 RM11 06 330 — 11 RM12
114-1 RM11 07 330 — 10 RM12
212-1 RM11 08 330 — 09 RM12
112-1 RM11 09 330 — 08 RM12
113-1 RM11 10 330 — 07 RM12

GND

C3 0.1 μF

213-1 RM11 11 330 — 06 RM12
115-1 RM11 12 330 — 04 RM12
217-1 RM11 13 330 — 03 RM12
218-1 RM11 14 330 — 02 RM12
118-1 RM11 15 330 — 01 RM12
125-1 RM13 01 330 16 — 05 RM14 16
229-1 RM13 02 330 — 15 RM14
228-1 RM13 03 330 — 14 RM14
227-1 RM13 04 330 — 13 RM14
124-1 RM13 05 330 — 12 RM14
220-1 RM13 06 330 — 11 RM14
122-1 RM13 07 330 — 10 RM14
222-1 RM13 08 330 — 09 RM14
123-1 RM13 09 330 — 08 RM14
223-1 RM13 10 330 — 07 RM14
224-1 RM13 11 330 — 06 RM14
225-1 RM13 12 330 — 04 RM14
127-1 RM13 13 330 — 03 RM14
128-1 RM13 14 330 — 02 RM14

101-1, 106-1, 206-1,
111-1, 211-1, 116-1,
216-1, 136-0, 140-0,
236-0, 111-0, 211-0,
116-0, 216-0, 121-0
221-0, 226-0,
126-0, 231-0,
131-0, 121-1, 126-1,
221-1, 226-1, 131-1,
136-1, 140-1, 231-1,
236-1, 240-1

GND

P5

241-0
141-1
241-1
100-1
200-1
129-1 RM13 15 330 — 01 RM14
137-1 RM15 01 330 16 — 05 RM16 16
237-1 RM15 02 330 — 15 RM16
235-1 RM15 03 330 — 14 RM16
135-1 RM15 04 330 — 13 RM16
232-1 RM15 05 330 — 12 RM16
230-1 RM15 06 330 — 11 RM16
132-1 RM15 07 330 — 10 RM16
133-1 RM15 08 330 — 09 RM16
134-1 RM15 09 330 — 08 RM16
233-1 RM15 10 330 — 07 RM16
234-1 RM15 11 330 — 06 RM16
138-1 RM15 12 330 — 04 RM16
238-1 RM15 13 330 — 03 RM16
130-1 RM15 14 330 — 02 RM16
239-1 RM15 15 330 — 01 RM16

GND

NOTES:
1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE 470Ω.

	NAME	TITLE	DATE
SCALE – ~	J.R GIELSKIE	DRAFT	11-11-74
TOLERANCE .XXX ± .001, .XX ± .02, .X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	G.J.HOMEFIELD	CHK	
	G. SYROVY	ENGR	
	P.A. BARKER	QC.	
	S. MESSINA	MGR.	

TITLE FUNCTIONAL SCHEMATIC TERMINATOR BOARD
M8/32

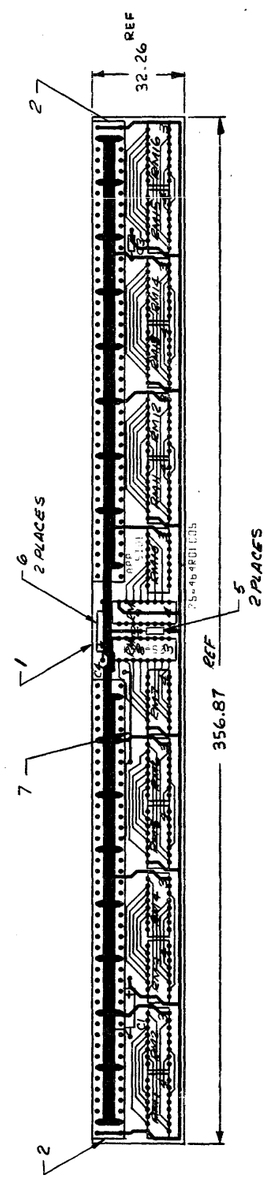
TASK NO. 03088 — SHEET OF 1 — 1
DWG. NO. 35-569 008

BRUNING 44-231 24538

REVISIONS			
REDRAWN FOR REDESIGN SEE VOIDED COPY.			
GM	9-4-26 03088	5-20-75	R01

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE _____

CHANGED TO METRIC
5-3-78 GM.



MILLIMETER	INCH
32.26	1.27
356.87	14.05

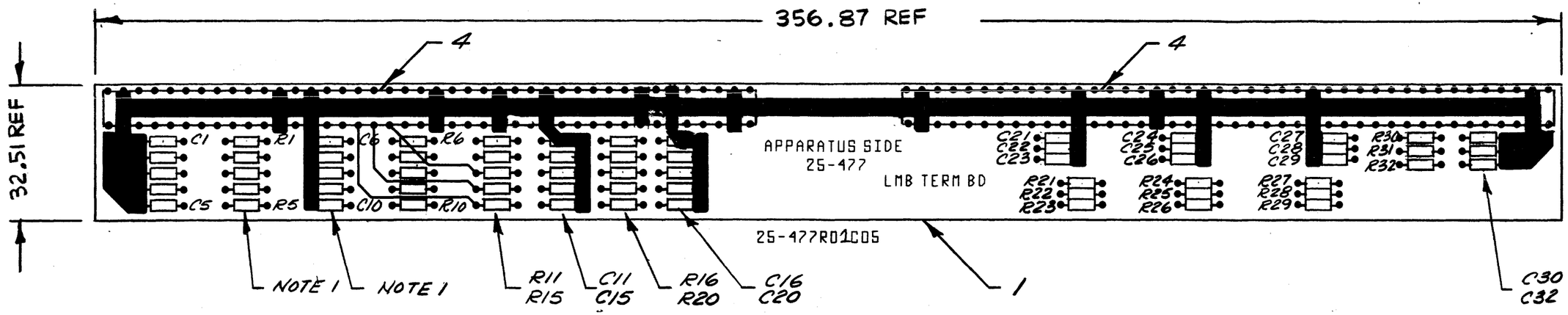
METRIC

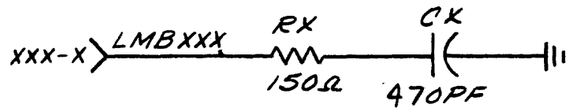
TOLERANCE:
.XXX ± .005
.XX ± .02
.X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE	TITLE
G. MELTON	DRAFT	1-20-75	PRINTED CIRCUIT ASSY
G.J. HOMEFIELD	CHK	2-9-75	TERMINATOR BOARD
G. STROVY	ENGR	5-2-75	M8/32
E.A. BARKER	QC	5-2-75	SIZE 03088 SHEET OF
S. MESSINA	DIR ENG	5-2-75	SCALE 36-369 REV C03 1-1

MILLIMETER	INCH
32.51	1.28
356.87	14.05

REVISIONS				
REVISED PER R01 COPPER				
EC PAH	2720	-	6-23-76	R01
CHANGED TO METRIC 5-3-78, GM.				





SCHEMATIC (SEE TABLE A)

TABLE A

MNEMONIC	PIN NO.	R(X)	C(X)
LMB000	114-0	R5	C5
LMB010	214-0	R1	C1
LMB020	115-0	R10	C10
LMB030	215-0	R2	C2
LMB040	116-0	R15	C15
LMB050	216-0	R3	C3
LMB060	117-0	R14	C14
LMB070	217-0	R4	C4
LMB080	118-0	R13	C13
LMB090	218-0	R9	C9
LMB100	119-0	R8	C8
LMB110	219-0	R7	C7
LMB120	120-0	R6	C6
LMB130	220-0	R19	C19
LMB140	122-0	R12	C12
LMB150	222-0	R18	C18

TABLE A (CONT.)

MNEMONIC	PIN NO.	R(X)	C(X)
LMB160	123-0	R11	C11
LMB170	223-0	R17	C17
LMB180	124-0	R20	C20
LMB190	224-0	R16	C16
LMB200	120-1	R24	C24
LMB210	220-1	R21	C21
LMB220	121-1	R25	C25
LMB230	221-1	R22	C22
LMB240	122-1	R26	C26
LMB250	222-1	R23	C23
LMB260	123-1	R29	C29
LMB270	223-1	R32	C32
LMB280	124-1	R28	C28
LMB290	224-1	R31	C31
LMB300	125-1	R27	C27
LMB310	225-1	R30	C30

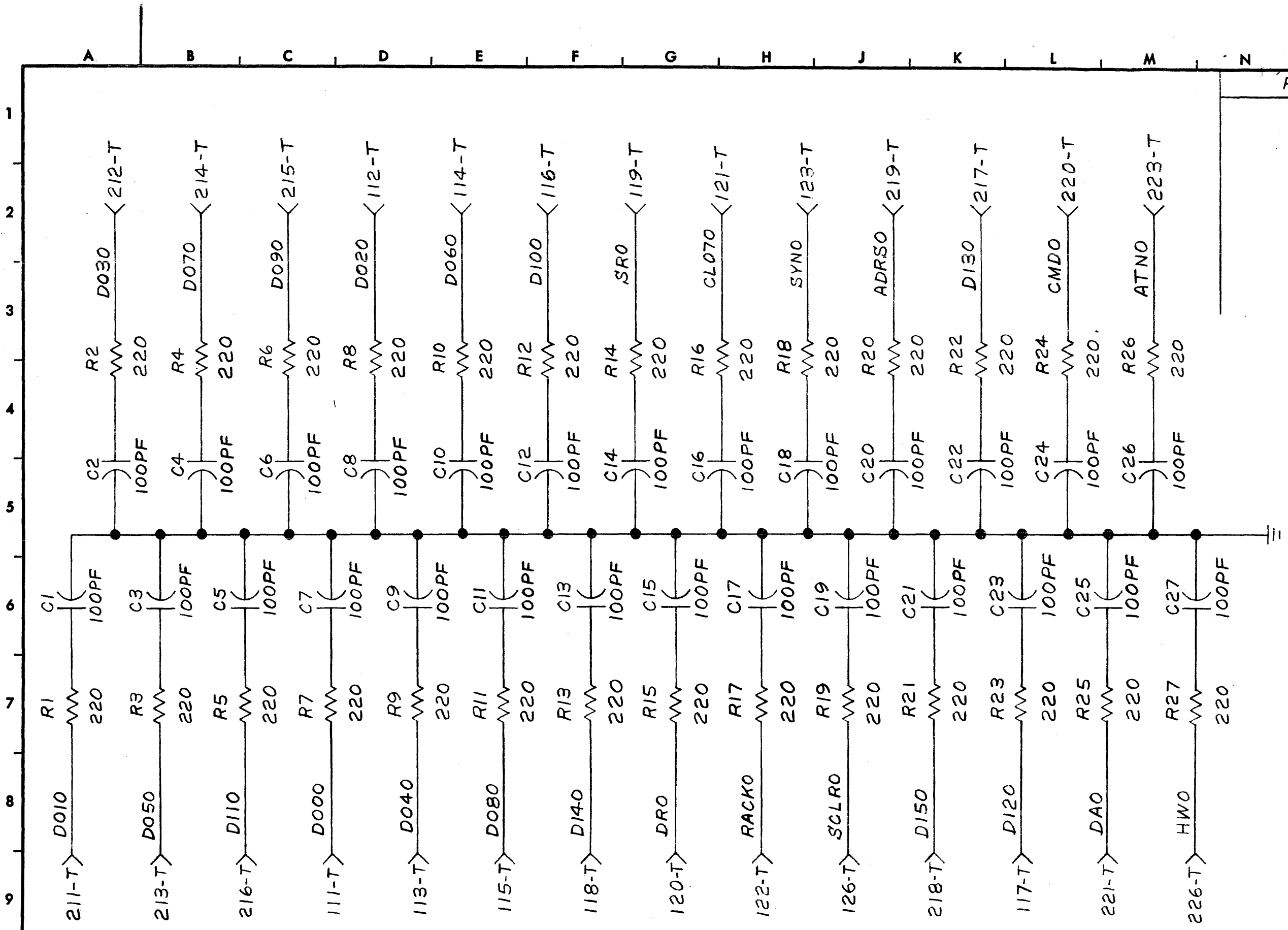
PRE PRODUCTION APPROVAL	INIT	DATE
DEV	[illegible]	3/14
PROD	VB	3/14

RELEASED FOR PRODUCTION
MFG. ENG. [illegible] DATE 5/12/78

METRIC

NOTES:
1. ALL "R" DESIGNATED COMPONENTS ARE ITEM 2 AND "C" DESIGNATED COMPONENTS ARE ITEM 3.

NAME	TITLE	DATE	TITLE
—	DRAFT	3-13-75	ASSY, PRINTED CKT LMB TERMINATOR
G. J. HOMEFIELD	CHK	3-13-75	
R. DONNELLY	ENGR		
			TASK NO. 03088 / SHEET OF
	DIR ENG		DWG NO. 35-578R01 B03 / 1-1



REVISIONS

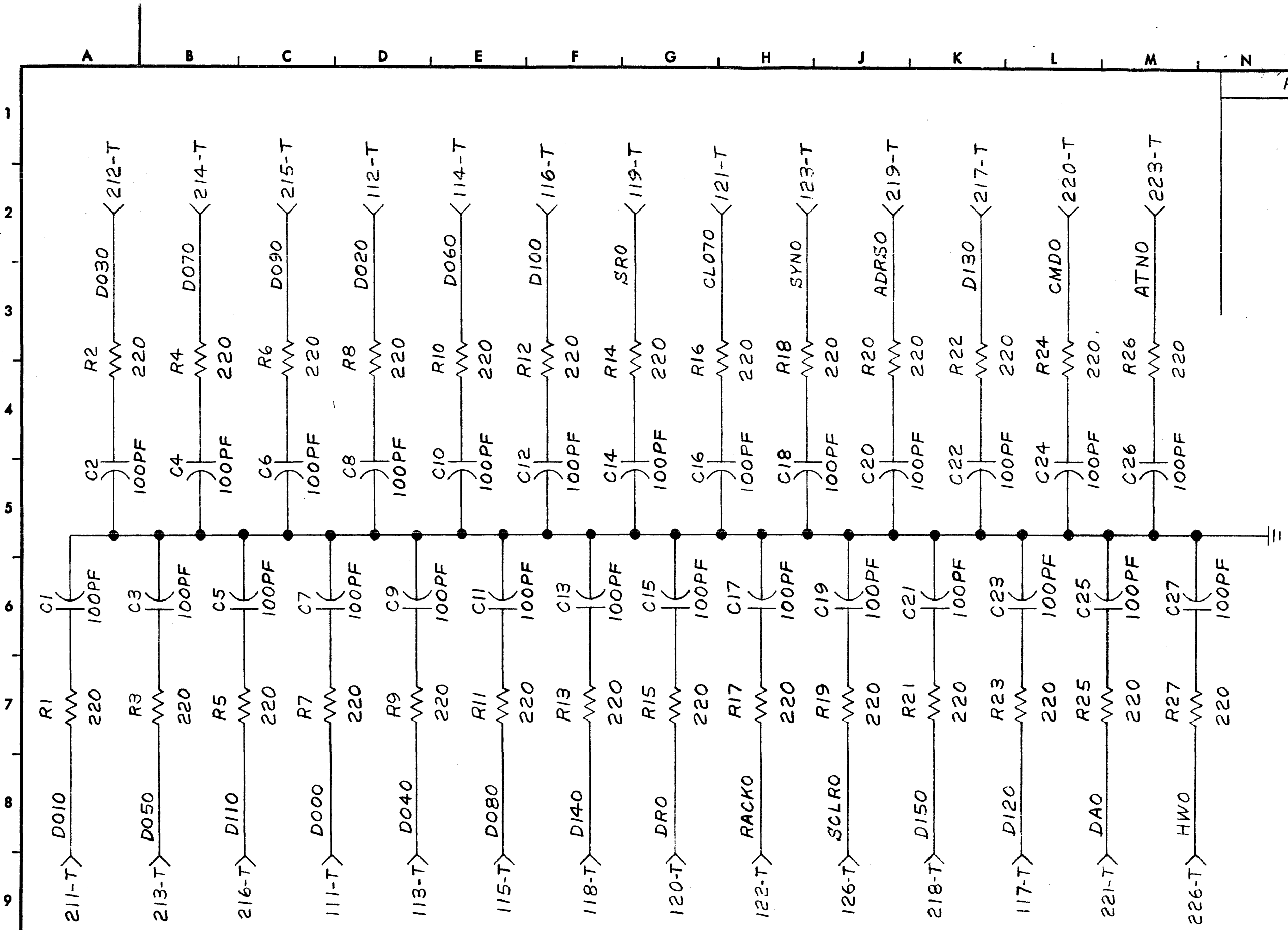
DF 9-31-73
[illegible] 9-20-73
[signature] 11/20/73

NOTES

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	9-12-73
H. MATTER	CHK	9-21-73
D. FRANKENBERGER	ENG	9-25-73
N. MASI	SYS TEST	9-26-73
D. FRANKENBERGER	MGR	9-29-73

TITLE FUNCTIONAL SCHEMATIC
TERMINATOR BOARD
15" CHASSIS

TASK NO. 03095
DWG. NO. 35-433 B08
SHEET 1 OF 1



REVISIONS

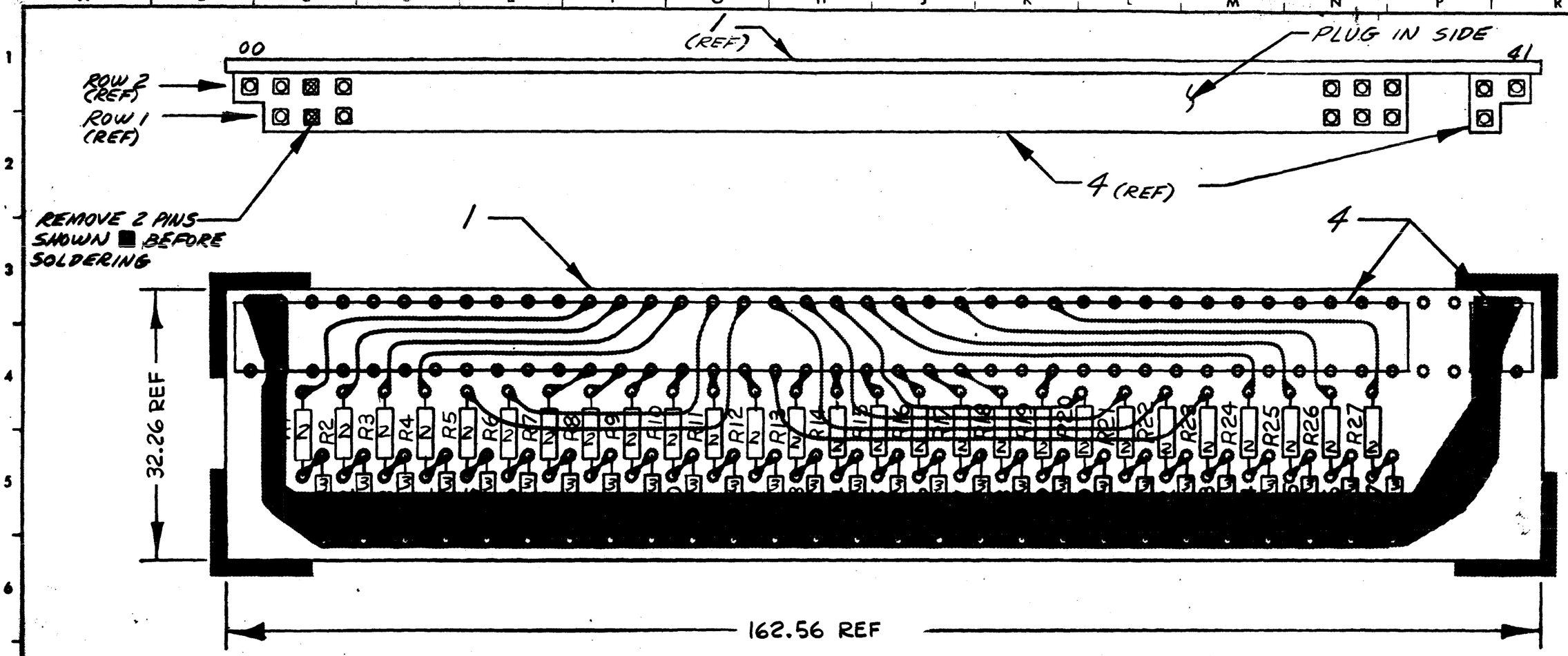
R.F.	9-21-73
[illegible]	9-20-73
[illegible]	11/20/73

NOTES

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	9-12-73
H. MATTER	CHK	9-21-73
D. FRANKENBERGER	ENG	9-25-73
N. MASI	SYS TEST	9-26-73
D. FRANKENBERGER	MGR	9-20-73

TITLE FUNCTIONAL SCHEMATIC
TERMINATOR BOARD
15" CHASSIS

TASK NO. 03095
DWG NO. 35-433 B08
SHEET 1 OF 1



MILLIMETER	INCH
32.26	1.27
162.56	6.40

APPARATUS SIDE

(COPPER SHOWN IS FAR SIDE-REF)

DO NOT MANUFACTURE W/O AUTH.

SUPERSEDED

BY PART NO. 35-433M01803

PER ECN NO. 2762

BY PC DATE 4-14-76

METRIC

RELEASED FOR PRODUCTION

MFG. ENG. [signature] DATE 11/20/73

REVISIONS

		INIT.	DATE
PRE PRODUCTION APPROVAL	DEV	[illegible]	17 Aug 72
	PROD	[illegible]	8-17-72

CHANGED: ERROR ON DWG PNS 101 & 201 WERE SHOWN REMOVED, IS NOW AND SHOULD BE 102 & 202				
DB	[illegible]	5035-01	MB	8-23-72	R01
ADDED DESIG. R1-R27, C1-C27				
KL	[illegible]	3214-43	[illegible]	9-20-73	R02
SUPERSEDED BY MOI				
[illegible]	[illegible]	2762	-	4-14-76	R03

NOTES

CHANGED TO METRIC 5-3-78, GM.

NAME	TITLE	DATE
	DRAFT	
D. BARKER	CHK	8-8-72
G. WELLY	ENGR	10-16-73
H. ROSS	Q.C.	10-18-73
D. FRANKENBERGER	MGR	10-22-73

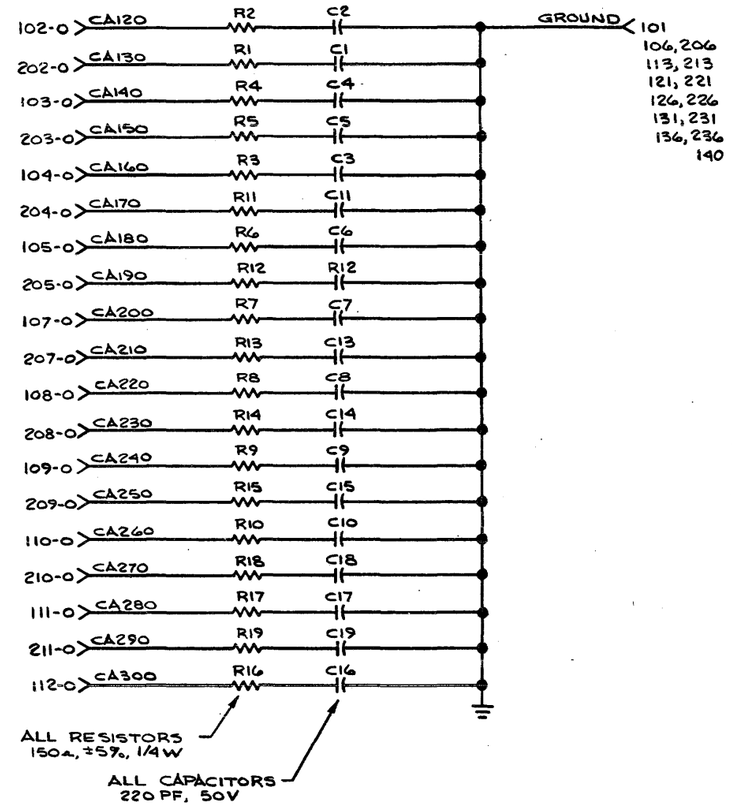
TITLE ASSY, PRINTED CIRCUIT TERMINATOR BOARD 15" CHASSIS SCALE: 3/1

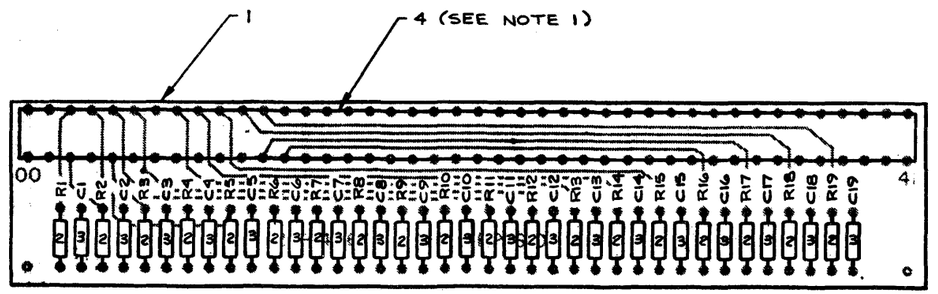
TASK NO. 03095

DWG. NO. 35-433R03B03

SHEET 1 OF 1

REVISIONS				
PRE PRODUCTION APPROVAL		INIT	DATE	ISSD.
	DEV	KPD	10/30/75	
	PROD	SS	11/7/75	
AREA L4: PIN # 240 WAS 241				
A	#	2969	-	9-28-76	R01
RELEASED FOR PRODUCTION MFG. ENG. S Sellers DATE 2/2/76				





NOTES:

1. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING.

SCALE- 2:1	NAME	TITLE	DATE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .05, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	C. JENSEN	DRAFT	30JUL75
	H. MATTER	CHK	
	R. DONNELLY	ENGR	10-28-75
	R.A. BARKER	Q.C.	9-22-76
	S. MESSINA	DIR.ENG	9-22-76

TITLE ASSEMBLY, PRINTED CIRCUIT BD. EXTENDER TERM. (CA)

TASK NO. 03045 SHEET OF 1 — 1

DWG NO. 35-596 R01 C03

Publication Number H29-394R81

METRIC

M83 SERIES MODEL 8/32, 8/32C, AND 8/32D PROCESSORS

MAINTENANCE MANUAL

Consists of:

GENERAL DESCRIPTION	
General Description	29-394R03A12
PROCESSOR	
Maintenance Specification	01-078R09A21
WRITABLE CONTROL STORE	
Installation Specification	35-555F01A20
Maintenance Specification	35-555F01R01A21
2K WRITABLE CONTROL STORE	
Installation Specification	35-663R01A20
Maintenance Specification	35-663A21
MEMORY	
Main Memory System Maintenance Specification	35-535R02A21
EXTENDED SELECTOR CHANNEL	
Installation Specification	02-328R04A20
Maintenance Specification	02-328R03A21
DISPLAY PANEL	
Hexadecimal Display Panel Specification	09-065R03A12
DRAWINGS	
Model 8/32 Backpanel Map	01-078R04D08
Model 8/32C Backpanel Map (with DFU)	01-098R03D08
Model 8/32D Backpanel Map (with DFU)	01-103R00D08
Processor CPU-A Schematic	35-536R30D08
Processor CPU-A Assembly	35-536R20E03
Processor CPU-B Schematic	35-537R17D08
Processor CPU-B Assembly	35-537R13E03
Processor CPU-C Schematic	35-555R10D08
Processor CPU-C Assembly	35-555R06E03
Processor CPU-C Schematic W/2K WCS	35-663R02D08
Processor CPU-C Assembly W/2K WCS	35-663R01E03
Processor IOU Schematic	35-539R27D08
Processor IOU Assembly	35-539R19E03
Processor ALU Schematic	35-538R16D08
Processor ALU Assembly	35-538R11E03
Memory Bus Controller (MBC) Schematic	35-535R23D08
Memory Bus Controller (MBC) Assembly	35-535R10E03
Local Memory Interface (LMI) Schematic	35-534R12D08
Local Memory Interface (LMI) Assembly	35-534R08E03
Extended Selector Channel Schematic	02-328M01R08D08
Extended Selector Channel Assembly	35-508M01R08E03
Hexadecimal Display Panel Schematic	09-065R03D08
Hexadecimal Display Panel Assembly	35-519R05D03
DMA Terminator Schematic	35-548C08
DMA Terminator Assembly	35-548B03
DMA Terminator Assembly	35-572B03
DMA Terminator Assembly	17-336R01B03
Processor Bus Terminator Schematic	35-569D08
Processor Bus Terminator Assembly	35-569R01C03
LMB Terminator Assembly	35-578R01B03
I/O Bus Terminator Schematic	35-433B08
I/O Bus Terminator Assembly	35-433R03B03
8/32 Backpanel Terminator	35-596R01C03

PERKIN-ELMER

Computer Systems Division
2 Crescent Place
Oceanport, N.J. 07757

PERKIN-ELMER

BACK PANEL MAP

CONN.	TITLE	CPB		DCB		DFU		ALU		CONN.
	BD. LOC	AA 07		AA 06		AA 05		AA 04		
	TERM. NO	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	
1	41	P5	P5	P5	P5	P5	P5	P5	P5	1
	40	GND	GND	GND	GND	GND	GND	GND	GND	
	39	DSPYL1	PPFO							
	38	ATNO20	ATNO30							
	37	ATNO00	ATNO10							
	36	GND	GND	GND	GND	GND	GND	GND	GND	
	35	B300	B310	B300	B310	B300	B310	B300	B310	
	34	B280	B290	B280	B290	B280	B290	B280	B290	
	33	B260	B270	B260	B270	B260	B270	B260	B270	
	32	B240	B250	B240	B250	B240	B250	B240	B250	
	31	GND	GND	GND	GND	GND	GND	GND	GND	
	30	B220	B230	B220	B230	B220	B230	B220	B230	
	29	B200	B210	B200	B210	B200	B210	B200	B200	
	28	B180	B190	B180	B190	B180	B190	B180	B180	
	27	B160	B170	B160	B170	B160	B170	B160	B160	
	26	GND	GND	GND	GND	GND	GND	GND	GND	
	25	S300	S310	S300	S310	S300	S310	S300	S300	
	24	S280	S290	S280	S290	S280	S290	S280	S280	
	23	S260	S270	S260	S270	S260	S270	S260	S260	
	22	S240	S250	S240	S250	S240	S250	S240	S240	
	21	GND	GND	GND	GND	GND	GND	GND	GND	
	20	S220	S230	S220	S230	S220	S230	S220	S230	
	19	S200	S210	S200	S210	S200	S210	S200	S210	
	18	S180	S190	S180	S190	S180	S190	S180	S190	
	17	S160	S170	S160	S170	S160	S170	S160	S170	
	16	GND	GND	GND	GND	GND	GND	GND	GND	
	15	A300	A310	A300	A310	A300	A310	A300	A310	
	14	A280	A290	A280	A290	A280	A290	A280	A290	
	13	A260	A270	A260	A270	A260	A270	A260	A270	
	12	A240	A250	A240	A250	A240	A250	A240	A250	
	11	GND	GND	GND	GND	GND	GND	GND	GND	
	10	A220	A230	A220	A230	A220	A230	A220	A230	
	09	A200	A210	A200	A210	A200	A210	A200	A210	
	08	A180	A190	A180	A190	A180	A190	A180	A190	
	07	A160	A170	A160	A170	A160	A170	A160	A170	
	06	GND	GND	GND	GND	GND	GND	GND	GND	
	05	MMFO	PSW230							
	04									
	03	MSEL020	RWCO	MSEL020	RWCO	MSEL020	RWCO	MSEL020	RWCO	
	02	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	
	01	GND	MSIGO	GND	MSIGO	GND	MSIGO	GND	MSIGO	
	00	P5	P5	P5	P5	P5	P5	P5	P5	
		1	2	1	2	1	2	1	2	
	41	P5	P5	P5	P5	P5	P5	P5	P5	
	40	GND	ESIGO	GND	ESIGO	GND	ESIGO	GND	ESIGO	
	39	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	
	38	FSEL000	FSEL010	FSEL000	FSEL010	FSEL000	FSEL010	FSEL000	FSEL010	
	37	STRTO	MFINO	STRTO	MFINO	STRTO	MFINO	STRTO	MFINO	
	36	GND	GND	GND	GND	GND	GND	GND	GND	
	35	B140	B150	B140	B150	B140	B150	B140	B150	
	34	B120	B130	B120	B130	B120	B130	B120	B130	
	33	B100	B110	B100	B110	B100	B110	B100	B110	
	32	B080	B090	B080	B090	B080	B090	B080	B090	
	31	GND	GND	GND	GND	GND	GND	GND	GND	
	30	B060	B070	B060	B070	B060	B070	B060	B070	
	29	B040	B050	B040	B050	B040	B050	B040	B050	
	28	B020	B030	B020	B030	B020	B030	B020	B030	
	27	B000	B010	B000	B010	B000	B010	B000	B010	
	26	GND	GND	GND	GND	GND	GND	GND	GND	
	25	S140	S150	S140	S150	S140	S150	S140	S150	
	24	S120	S130	S120	S130	S120	S130	S120	S130	
	23	S100	S110	S100	S110	S100	S110	S100	S110	
	22	S080	S090	S080	S090	S080	S090	S080	S090	
	21	GND	GND	GND	GND	GND	GND	GND	GND	
0	20	S060	S070	S060	S070	S060	S070	S060	S070	0
	19	S040	S050	S040	S050	S040	S050	S040	S050	
	18	S020	S030	S020	S030	S020	S030	S020	S030	
	17	S000	S010	S000	S010	S000	S010	S000	S010	
	16	GND	GND	GND	GND	GND	GND	GND	GND	
	15	A140	A150	A140	A150	A140	A150	A140	A150	
	14	A120	A130	A120	A130	A120	A130	A120	A130	
	13	A100	A110	A100	A110	A100	A110	A100	A110	
	12	A080	A090	A080	A090	A080	A090	A080	A090	
	11	GND	GND	GND	GND	GND	GND	GND	GND	
	10	A060	A070	A060	A070	A060	A070	A060	A070	
	09	A040	A050	A040	A050	A040	A050	A040	A050	
	08	A020	A030	A020	A030	A020	A030	A020	A030	
	07	A000	A010	A000	A010	A000	A010	A000	A010	
	06	GND	GND	GND	GND	GND	GND	GND	GND	
	05	SCLR0	CCCO	SCLR0	CCCO	SCLR0	CCCO	SCLR0	CCCO	
	04	SCCO	VCCO	SCCO	VCCO	SCCO	VCCO	SCCO	VCCO	
	03	SCLR1	GCCO	SCLR1	GCCO	SCLR1	GCCO	SCLR1	GCCO	
	02	TKILLO	LCCO		LCCO		LCCO		LCCO	
	01	GND	GND	GND	GND	GND	GND	GND	GND	
	00	P5	P5	P5	P5	P5	P5	P5	P5	
		1	2	1	2	1	2	1	2	

CONN.	TITLE	IOU	I/O	I/O	I/O	CONN.
	BD. LOC.	AA 03	AA 02	AA 01	AA 00	
	TERM. NO.	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	
1	41	P5	P5	P5 GND	P5 GND	P5 GND	1
	40	GND	GND	GND	GND	GND	GND	
	39	P15	PPFO					
	38	N15	DSPYL0					
	37	RACK0	TACK0	DMAI70	DGND	DMAI70	DGND	DMAI70	DGND	
	36	GND	GND	DMAI50	DMAI60	DMAI50	DMAI60	DMAI50	DMAI60	
	35	B300	B310	DMAI30	DMAI40	DMAI30	DMAI40	DMAI30	DMAI40	
	34	B280	B290	DGND	DMAI20	DGND	DMAI20	DGND	DMAI20	
	33	B260	B270	DMAI10	DMAI00	DMAI10	DMAI00	DMAI10	DMAI00	
	32	B240	B250	DMA090	DMA080	DMA090	DMA080	DMA090	DMA080	
	31	GND	GND	DMA070	DMA060	DMA070	DMA060	DMA070	DMA060	
	30	B220	B230	DMA050	DGND	DMA050	DGND	DMA050	DGND	
	29	B200	B210	DMA030	DMA040	DMA030	DMA040	DMA030	DMA040	
	28	B180	B190	DMA010	DMA020	DMA010	DMA020	DMA010	DMA020	
	27	B160	B170	DGND	DMA000	DGND	DMA000	DGND	DMA000	
	26	GND	GND	SCLE0	HWO	SCLR0	HWO	SCLR0	HWO	
	25	S300	S310					P4TNO	SREQO	
	24	S280	S290					XFERO	TERMO	
	23	S260	S270	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	
	22	S240	S250	PACK0	TACK0	PACK0	TACK0	PACK0	TACK0	
	21	GND	GND	CLO70	DAO	CLO70	DAO	CLO70	DAO	
	20	S220	S230	DE0	CMD0	DE0	CMD0	DE0	CMD0	
	19	S200	S210	SE0	ADES0	SE0	ADES0	SE0	ADES0	
	18	S180	S190	D140	D150	D140	D150	D140	D150	
	17	S160	S170	D120	D130	D120	D130	D120	D130	
	16	GND	GND	D100	D110	D100	D110	D100	D110	
	15	A300	A310	D080	D090	D080	D090	D080	D090	
	14	A280	A290	D060	D070	D060	D070	D060	D070	
	13	A260	A270	D040	D050	D040	D050	D040	D050	
	12	A240	A250	D020	D030	D020	D030	D020	D030	
	11	GND	GND	D000	D010	D000	D010	D000	D010	
	10	A220	A230		DMX140		DMX140		DMX140	
	09	A200	A210	DMX150	DMX120	DMX150	DMX120	DMX150	DMX120	
	08	A180	A190	DMX130	DGND	DMX130	DGND	DMX130	DGND	
	07	A160	A170	M3B20	M2B20	M3B20	M2B20	M3B20	M2B20	
	06	GND	GND	M1B20	M0B20	M1B20	M0B20	M1B20	M0B20	
	05	MMFO *	TRLMPO *	LOADO	ANSO	LOADO	ANSO	LOADO	ANSO	
	04		DMPFO *	LMREQO	DGND	LMRQO	DGND	LMRQO	DGND	
	03	MSEL020		SOTO	EOTO	SOTO	EOTO	SOTO	EOTO	
	02	MSEL000	MSEL010	XREQO	QUEO	XREQO	QUEO	XREQO	QUEO	
	01	GND	MSIGO	GND	GND	GND	GND	GND	GND	
	00	P5	P5	P5	GND	P5	GND	P5	GND	
		1	2	1	2	1	2	1	2	
	41	P5	P5	P5	GND	P5	GND	P5	GND	
	40	GND	ESIGO	GND	GND	GND	GND	GND	GND	
	39	FSEL020	FSEL030							
	38	FSEL000	FSEL010							
	37	STRTO	MFINO	RPLO	TPLO	RPLO	TPLO	RPLO	TPLO	
	36	GND	GND	DGND	BHO	DGND	BHO	DGND	BHO	
	35									
	34	GND	GND					XRACKO		
	33									
	32	MAR310								
	31	GND	GND							
	30	ACKO30								
	29	ACKO20								
	28	ACKO10	GND	PRPCO	PRPCO	PRPCO	PRPCO	PRPCO	PRPCO	
	27	ACK000	HWC							
	26	GND	GND	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO	
	25	GND	GND					P4TNO	SREQO	
	24							XFERO	TERMO	
	23	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	
	22	CLO70	DAO	PACK0	TACK0	PACK0	TACK0	PACK0	TACK0	
	21	GND	GND	CLO70	DAO	CLO70	DAO	CLO70	DAO	
0	20	DE0	CMD0	DE0	CMD0	DE0	CMD0	DE0	CMD0	0
	19	SE0	ADES0	SE0	ADES0	SE0	ADES0	SE0	ADES0	
	18	D140	D150	D140	D150	D140	D150	D140	D150	
	17	D120	D130	D120	D130	D120	D130	D120	D130	
	16	GND	GND	D100	D110	D100	D110	D100	D110	
	15	D080	D090	D080	D090	D080	D090	D080	D090	
	14	D060	D070	D060	D070	D060	D070	D060	D070	
	13	D040	D050	D040	D050	D040	D050	D040	D050	
	12	D020	D030	D020	D030	D020	D030	D020	D030	
	11	GND	GND	D000	D010	D000	D010	D000	D010	
	10	D020	D030							
	09	D000	D010							
	08									
	07									
	06	GND	GND							
	05	SCLR0	CCCO							
	04	SCCO	VCCO							
	03	SCLR1	GCCO							
	02		LCCO							
	01	GND	GND	GND	GND	GND	GND	GND	GND	
	00	P5	P5	P5	GND	P5	GND	P5	GND	
		1	2	1	2	1	2	1	2	

NOTES
1. BACKPANEL - 35-591
Ⓦ WIRE WRAP RUN

RELEASED FOR PRODUCTION ENG. DATE

PRE PRODUCTION APPROVAL INIT. DATE DEV PROD

SHEET INDEX | REV. LEV. 4 3 3 4 | SHT NO. 1 2 3 4

SEE SHEET 4 FOR REVISION INFO.

DRWN	G. MELTON	6-10-74
CHKD	G.J. HOMEFIELD	10-10-74
ENGR	T. EYFE	
DES.	S. MESSINA	

SIZE 8/32
TITLE BACKPANEL LOWER
03053
01-078RQADQB
SHEET OF 1 4

PERKIN ELMER

BACK PANEL MAP

CONN.	TITLE	LMM		LMI NOTE 2		LMM		LMM		CONN.
	BD LOC	A07		A06		A05		A04		
	TERM. NO.	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	
	41	PS	GND	PS	PS	PS	GND	PS	GND	
	40	GND	GND	GND	GND	GND	GND	GND	GND	
	39	PIS	PIS			PIS	PIS	PIS	PIS	
	38	NIS	NIS			NIS	NIS	NIS	NIS	
	37	MDI50	MDI60	MDI50	MDI60	MDI50	MDI60	MDI50	MDI60	
	36	MDI30	MDI40	MDI30	MDI40	MDI30	MDI40	MDI30	MDI40	
	35	MDI10	MDI20	MDI10	MDI20	MDI10	MDI20	MDI10	MDI20	
	34	MD090	MD100	MD090	MD100	MD090	MD100	MD090	MD100	
	33	MD070	MD080	MD070	MD080	MD070	MD080	MD070	MD080	
	32	MD050	MD060	MD050	MD060	MD050	MD060	MD050	MD060	
	31	MD030	MD040	MD030	MD040	MD030	MD040	MD030	MD040	
	30	MD010	MD020	MD010	MD020	MD010	MD020	MD010	MD020	
	29	GND	MD000	GND	MD000	GND	MD000	GND	MD000	
	28	TEMPA ⊗	VT ⊗			TEMPA ⊗	VT ⊗	TEMPA ⊗	VT ⊗	
	27	WRTO	TEMP B ⊗	OWRTO		WRTO	TEMP B ⊗	WRTO	TEMP B ⊗	
	26	GND	GND	GND	GND	GND	GND	GND	GND	
	25	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	
	24	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	
	23	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	
	22	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	
1	21	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	1
	20	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	
	19	GND	GND	GND	GND	GND	GND	GND	GND	
	18									
	17									
	16	GND	GND	GND	GND	GND	GND	GND	GND	
	15									
	14									
	13									
	12									
	11	GND	GND	GND	GND	GND	GND	GND	GND	
	10		MS000	EWRTO	MS000	EWRTO	MS000		MS000	
	09	MS010	MS020	MS010	MS020	MS10	MS020	MS010	MS020	
	08	MS030	MS040	MS030	MS040	MS30	MS040	MS030	MS040	
	07	MS050	MS060	MS050	MS060	MS50	MS060	MS050	MS060	
	06	MS070	MS080	MS070	MS080	MS70	MS080	MS070	MS080	
	05	MS090	MS100	MS090	MS100	MS90	MS100	MS090	MS100	
	04	MS110	MS120	MS110	MS120	MS10	MS120	MS110	MS120	
	03	MS130	MS140	MS130	MS140	MS30	MS140	MS130	MS140	
	02	MS150	MS160	MS150	MS160	MS50	MS160	MS150	MS160	
	01	GND	GND	GND	GND	GND	GND	GND	GND	
	00	PS	GND	PS	PS	P	GND	PS	GND	
		1	2	1	2		2	1	2	
	41	PS	GND	PS	PS	F	GND	PS	GND	
	40	GND	GND	GND	GND	GN	GND	GND	GND	
	39	LMBSYA0	LMBSYC0	LMBSYA0	LMBSYC0	LMB	YA0	LMBSYC0	LMBSYA0	LMBSYC0
	38	LMRDY0	LMDS0	LMRDY0	LMDS0	LM	DY0	LMDS0	LMRDY0	LMDS0
	37	LMBSYB0	LMRS0	LMBSYB0	LMRS0	LMB	B0	LMRS0	LMBSYB0	LMRS0
	36	GND	GND	GND	GND	GN		GND	GND	GND
	35	DUA0	MB20	DUA0	MB20	DUA	0	MB20	DUA0	MB20
	34	GND	GND	GND	GND	GN	D	GND	GND	GND
	33	MA130	MA140	MA130	MA140	MA	30	MA140	MA130	MA140
	32	MA110	MA120	MA110	MA120	MA	10	MA120	MA110	MA120
	31	MA090	MA100	MA090	MA100	MA	90	MA100	MA090	MA100
	30	MA070	MA080	MA070	MA080	MA	70	MA080	MA070	MA080
	29	MA050	MA060	MA050	MA060	MA	50	MA060	MA050	MA060
	28	GND	GND	GND	GND	GN	D	GND	GND	GND
	27	SCLR0		SCLR0		SCLR			SCLR0	
	26	MCLR0	GND	MCLR0	GND	MCLR		GND	MCLR0	GND
	25	GND	GND	GND	GND	GND		GND	GND	GND
	24	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	
	23	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	
	22	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	
	21	GND	GND	GND	GND	GND	GND	GND	GND	
0	20	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130	0
	19	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	
	18	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	
	17	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	
	16	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	
	15	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	
	14	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010	
	13	GND	GND	GND	GND	GND	GND	GND	GND	
	12	IRLMP0	DLMP0	IRLMP0	DLMP0	IRLMP0	DLMP0	IRLMP0	DLMP0	
	11	GND	GND	GND	GND	GND	GND	GND	GND	
	10	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040	
	09	MA020		MA020		MA020		MA020		
	08	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070	MAX060	MAX070	
	07	MA010		MA010		MA010		MA010		
	06	MA000		MA000	GND	MA000		MA000		
	05	PARO		PARO		PARO		PARO		
	04	INH0	ER0	INH0	ER0	INH0	ER0	INH0	ER0	
	03		SPY		SPY		SPY		SPY	
	02	PIS	NIS					PIS	NIS	
	01	GND	GND	GND	GND	GND	GND	GND	GND	
	00	PS	GND	PS	PS	PS	GND	PS	GND	
		1	2	1	2	1	2	1	2	

CONN.	TITLE	LMI (NOTE 2)		LMM		MBC		CPA		TITLE	CONN.
	BD.LOC.	A03		A02		A01		A00		BD.LOC.	
	TERM. NO.	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	TERM NO.	
	41	PS	PS	PS	GND	PS	PS	PS	PS	41	
	40	GND	GND	GND	GND	GND	QUE0	GND	MSIG0	40	
	39					DMA160	DMA170	B300	B310	39	
	38					DMA140	DMA150	B280	B290	38	
	37	MDI50	MDI60	MDI50	MDI60	DMA120	DMA130	B260	B270	37	
	36	MDI30	MDI40	MDI30	MDI40	GND	GND	GND	GND	36	
	35	MDI10	MDI20	MDI10	MDI20	DMA100	DMA110	B240	B250	35	
	34	MD090	MD100	MD090	MD100	DMA080	DMA090	B220	B230	34	
	33	MD070	MD080	MD070	MD080	DMA060	DMA070	B200	B210	33	
	32	MD050	MD060	MD050	MD060	DMA040	DMA050	B180	B190	32	
	31	MD030	MD040	MD030	MD040	DMA020	DMA030	B160	B170	31	
	30	MD010	MD020	MD010	MD020	GND	GND	GND	GND	30	
	29	GND	MD000	GND	MD000	DMA000	DMA010	S300	S310	29	
	28			TEMPA ⊗	VT ⊗	DMX140	DMX150	S280	S290	28	
	27	OWRTO		WRTO	TEMP B ⊗	DMX120	DMX130	S260	S270	27	
	26	GND	GND	GND	GND	GND	GND	GND	GND	26	
	25	LMB300	LMB310	LMB300	LMB310	LMB300	LMB310	S240	S250	25	
	24	LMB280	LMB290	LMB280	LMB290	LMB280	LMB290	S220	S230	24	
	23	LMB260	LMB270	LMB260	LMB270	LMB260	LMB270	S200	S210	23	
	22	LMB240	LMB250	LMB240	LMB250	LMB240	LMB250	S180	S190	22	
1	21	LMB220	LMB230	LMB220	LMB230	LMB220	LMB230	S160	S170	21	1
	20	LMB200	LMB210	LMB200	LMB210	LMB200	LMB210	GND	GND	20	
	19	GND	GND	GND	GND	GND	CRDY0	GND	CRDY0	19	
	18					CMC020	CREQ0	CMC020	CREQ0	18	
	17					CMC000	CMC010	CMC000	CMC010	17	
	16	GND	GND	GND	GND	GND	GND	GND	GND	16	
	15					CD300	CD310	CD300	CD310	15	
	14					CD280	CD290	CD280	CD290	14	
	13					CD260	CD270	CD260	CD270	13	
	12					CD240	CD250	CD240	CD250	12	
	11	GND	GND	GND	GND	GND	GND	GND	GND	11	
	10	EWRTO	MS000	EWRTO	MS000	CD220	CD230	CD220	CD230	10	
	09	MS010	MS020	MS010	MS020	CD200	CD210	CD200	CD210	09	
	08	MS030	MS040	MS030	MS040	CD180	CD190	CD180	CD190	08	
	07	MS050	MS060	MS050	MS060	CD160	CD170	CD160	CD170	07	
	06	MS070	MS080	MS070	MS080	GND	GND	GND	GND	06	
	05	MS090	MS100	MS090	MS100	MB820	MB820	B140	B150	05	
	04	MS110	MS120	MS110	MS120	MB820	MB820	B120	B130	04	
	03	MS130	MS140	MS130	MS140	LOAD0	PNS0	B100	B110	03	
	02	MS150	MS160	MS150	MS160	SOT0	EOT0	B080	B090	02	
	01	GND	GND	GND	GND	GND	XREQ0	GND	B070	01	
	00	PS	PS	PS	GND	PS	PS	PS	PS	00	
		1	2	1	2	1	2	1	2		
	41	PS	PS	PS	GND	PS	PS	PS	PS	41	
	40	GND	GND	GND	GND	MTPC0 ⊗	GND	B060	B050	40	
	39	LMBSYA0	LMBSYC0	LMBSYA0	LMBSYC0	LMEQ0 ⊗	BH0 ⊗	B040	B050	39	
	38	LMRDY0	LMDS0	LMRDY0	LMDS0	LMRDY0	LMDS0	B020	B030	38	
	37	LMBSYB0	LMRS0	LMBSYB0	LMRS0	PRPC0 ⊗	LMRS0	B000	B010	37	
	36	GND	GND	GND	GND	GND	GND	GND	GND	36	
	35	DUA0	MB20	DUA0	MB20	CD140	CD150	CD140	CD150	35	
	34	GND	GND	GND	GND	CD120	CD130	CD120	CD130	34	
	33	MA130	MA140	MA130	MA140	CD100	CD110	CD100	CD110	33	
	32	MA110	MA120	MA110	MA120	CD080	CD090	CD080	CD090	32	
	31	MA090	MA100	MA090	MA100	GND	GND	GND	GND	31	
	30	MA070	MA080	MA070	MA080	CD060	CD070	CD060	CD070	30	
	29	MA050	MA060	MA050	MA060	CD040	CD050	CD040	CD050	29	
	28	GND	GND	GND	GND	CD020	CD030	CD020	CD030	28	
	27	SCLR0		SCLR0		CD000	CD010	CD000	CD010	27	
	26	MCLR0	GND	MCLR0	GND	GND	GND	GND	GND	26	
	25	GND	GND	GND	GND	SCLR0	GND	SCLR0	GND	25	
	24	LMB180	LMB190	LMB180	LMB190	LMB180	LMB190	S140	S150	24	
	23	LMB160	LMB170	LMB160	LMB170	LMB160	LMB170	S120	S130	23	
	22	LMB140	LMB150	LMB140	LMB150	LMB140	LMB150	S100	S110	22	
	21	GND	GND	GND	GND	GND	GND	GND	GND	21	
0	20	LMB120	LMB130	LMB120	LMB130	LMB120	LMB130			20	0
	19	LMB100	LMB110	LMB100	LMB110	LMB100	LMB110	S080	S090	19	
	18	LMB080	LMB090	LMB080	LMB090	LMB080	LMB090	S060	S070	18	
	17	LMB060	LMB070	LMB060	LMB070	LMB060	LMB070	S040	S050	17	
	16	LMB040	LMB050	LMB040	LMB050	LMB040	LMB050	S020	S030	16	
	15	LMB020	LMB030	LMB020	LMB030	LMB020	LMB030	S000	S010	15	
	14	LMB000	LMB010	LMB000	LMB010	LMB000	LMB010			14	
	13	GND	GND	GND	GND	GND	GND	GND	GND	13	
	12	IRLMP0	DLMP0	IRLMP0	DLMP0	CA300	DLMP0	CA300	MAR310 ⊗	12	
	11	GND	GND	GND	GND	CA280	CA290	CA280	CA290	11	
	10	MA030	MA040	MA030	MA040	CA260	CA270	CA260	CA270	10	
	09	MA020		MA020		CA240	CA250	CA240	CA250	09	
	08	MAX060	MAX070	MAX060	MAX070	CA220	CA230	CA220	CA230	08	
	07	MA010		MA010		CA200	CA210	CA200	CA210	07	
	06	MA000	GND	MA000		GND	GND	GND	GND	06	
	05	PARO		PARO		CA180	CA190	CA180	CA190	05	
	04	INH0	ER0	INH0	ER0	CA160	CA170	CA160	CA170	04	
	03		SPY		SPY	CA140	CA150	CA140	CA150	03	
	02	PIS	NIS			CA120	CA130	CA120	CA130	02	
	01	GND	GND	GND	GND	GND	DMEP0 ⊗	GND	GND	01	
	00	PS	PS	PS	GND	PS	PS	PS	PS	00	
		1	2	1	2	1	2	1	2		

NOTES
1. BACKPANEL — 35-540
   ⊗ WIRE WRAP RUNS
2. SLOT ASSIGNMENTS SHOWN FOR THE BASIC 128 KB MEMORY SYSTEM.

THE LMI BOARDS ARE RE-ASSIGNED WHEN THE SYSTEM IS EXPANDED WITH CORRESPONDING CHANGES IN MA, MD, & MS STRAPPING OPTIONS.

NAME	TITLE	DATE
G. MELTON	DRAFT	6-10-74
G.J. HOMEFIELD	CHK	10-10-74
T. FYFE	ENGR	
S MESSINA	ENG MGR	

TITLE 8/32 BACK PANEL UPPER

DWG NO. 03053

REV. 01-078 R03008

SHEET OF 2-4

PERKIN-ELMER

BACK PANEL MAP

CONN.	TITLE BD. LOC. TERM. NO.	LMM 07 ROW 1	LMM 07 ROW 2	LMM 06 ROW 1	LMM 06 ROW 2	LMM 05 ROW 1	LMM 05 ROW 2	LMM 04 ROW 1	LMM 04 ROW 2	CONN.
1	41	P5	GND							1
	40	GND	GND							
	39	P15	P15							
	38	N15	N15							
	37	MD150	MD160							
	36	MD130	MD140							
	35	MD110	MD120							
	34	MD090	MD100							
	33	MD070	MD080							
	32	MD050	MD060							
	31	MD030	MD040							
	30	MD010	MD020							
	29		MD000							
	28	TEMPA	VT							
	27	WRTO	TEMPB							
	26	GND	GND							
	25	LMB300	LMB310							
	24	LMB280	LMB290							
	23	LMB260	LMB270							
	22	LMB240	LMB250							
	21	LMB220	LMB230							
	20	LMB200	LMB210							
	19	GND	GND							
	18									
	17									
	16	GND	GND							
	15									
	14									
	13									
	12									
	11	GND	GND							
	10		MS000							
	09	MS010	MS020							
	08	MS030	MS040							
	07	MS050	MS060							
	06	MS070	MS080							
	05	MS090	MS100							
	04	MS110	MS120							
	03	MS130	MS140							
	02	MS150	MS160							
	01	GND	GND							
	00	P5	GND							
		1	2	1	2	1	2	1	2	
0	41	P5	GND							0
	40	GND	GND							
	39									
	38	LMRDYO	LMD50							
	37	LMBSYO	LMB50							
	36	GND	GND							
	35	DUAO	MB20							
	34	GND	GND							
	33	MA130	MA140							
	32	MA110	MA120							
	31	MA090	MA100							
	30	MA070	MA080							
	29	MA050	MA060							
	28	GND	GND							
	27	SCLRO								
	26	MCLRO	GND							
	25	GND	GND							
	24	LMB180	LMB190							
	23	LMB160	LMB170							
	22	LMB140	LMB150							
	21	GND	GND							
	20	LMB120	LMB130							
	19	LMB100	LMB110							
	18	LMB080	LMB090							
	17	LMB060	LMB070							
	16	LMB040	LMB050							
	15	LMB020	LMB030							
	14	LMB000	LMB010							
	13	GND	GND							
	12		LMPO							
	11	GND	GND							
	10	MA030	MA040							
	09	MA020								
	08	MAX060	MAX070							
	07	MA010								
	06	MA000								
	05	PARO								
	04	INHO	ERO							
	03									
	02	P15	N15							
	01	GND	GND							
	00	P5	GND							
		1	2	1	2	1	2	1	2	

CONN.	TITLE BD. LOC. TERM. NO.	LMM 03 ROW 1	LMM 03 ROW 2	LMM 02 ROW 1	LMM 02 ROW 2	LMM 01 ROW 1	LMM 01 ROW 2	LMM 00 ROW 1	LMM 00 ROW 2	TITLE BD. LOC. TERM NO.	CONN.
1	41							P5	GND	41	1
	40							GND	GND	40	
	39							P15	P15	39	
	38							N15	N15	38	
	37							MD150	MD160	37	
	36							MD130	MD140	36	
	35							MD110	MD120	35	
	34							MD090	MD100	34	
	33							MD070	MD080	33	
	32							MD050	MD060	32	
	31							MD030	MD040	31	
	30							MD010	MD020	30	
	29								MD000	29	
	28							TEMPA	VT	28	
	27							WRTO	TEMPB	27	
	26							GND	GND	26	
	25							LMB300	LMB310	25	
	24							LMB280	LMB290	24	
	23							LMB260	LMB270	23	
	22							LMB240	LMB250	22	
	21							LMB220	LMB230	21	
	20							LMB200	LMB210	20	
	19							GND	GND	19	
	18									18	
	17									17	
	16							GND	GND	16	
	15									15	
	14									14	
	13									13	
	12									12	
	11							GND	GND	11	
	10								MS000	10	
	09							MS010	MS020	09	
	08							MS030	MS040	08	
	07							MS050	MS060	07	
	06							MS070	MS080	06	
	05							MS090	MS100	05	
	04							MS110	MS120	04	
	03							MS130	MS140	03	
	02							MS150	MS160	02	
	01							GND	GND	01	
	00							P5	GND	00	
		1	2	1	2	1	2	1	2		
0	41							P5	GND	41	0
	40							GND	GND	40	
	39									39	
	38							LMRDYO	LMD50	38	
	37							LMBSYO	LMB50	37	
	36							GND	GND	36	
	35							DUAO	MB20	35	
	34							GND	GND	34	
	33							MA130	MA140	33	
	32							MA110	MA120	32	
	31							MA090	MA100	31	
	30							MA070	MA080	30	
	29							MA050	MA060	29	
	28							GND	GND	28	
	27							SCLRO		27	
	26							MCLRO	GND	26	
	25							GND	GND	25	
	24							LMB180	LMB190	24	
	23							LMB160	LMB170	23	
	22							LMB140	LMB150	22	
	21							GND	GND	21	
	20							LMB120	LMB130	20	
	19							LMB100	LMB110	19	
	18							LMB080	LMB090	18	
	17							LMB060	LMB070	17	
	16							LMB040	LMB050	16	
	15							LMB020	LMB030	15	
	14							LMB000	LMB010	14	
	13							GND	GND	13	
	12								LMPO	12	
	11							GND	GND	11	
	10							MA030	MA040	10	
	09							MA020		09	
	08							MAX060	MAX070	08	
	07							MA010		07	
	06							MA000		06	
	05							PARO		05	
	04							INHO	ERO	04	
	03									03	
	02							P15	N15	02	
	01							GND	GND	01	
	00							P5	GND	00	
		1	2	1	2	1	2	1	2		

NOTES
1. BACKPANEL-35-542

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE 8/32 BACKPANEL MEMORY EXP.

TASK NO. 03053 DWG NO. 01-078 R03 D08 SHEET OF 3-4

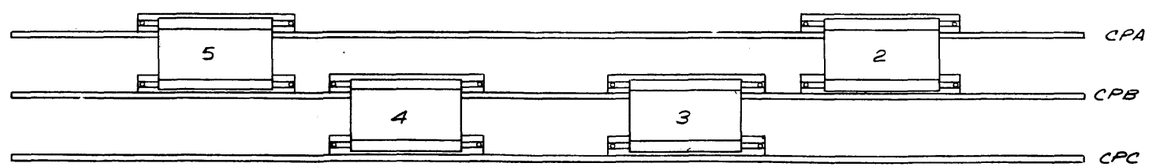
PERKIN-ELMER
2 Crescent Place, Oceanport, New Jersey 07757

CONN 5		
	2	1
16	UIR300	UIR310
15	UIR280	UIR290
14	UIR260	UIR270
13	UIR240	UIR250
12	YD300	YD310
11	YD280	YD290
10	YS300	YS310
09	YS280	YS290
08	SX300	SX310
07	SX280	SX290
06	GND	ININTO
05	GND	MAIO
04	GND	IREQO
03	GND	DREQO
02	GND	PSW210
01	GND	GND
00	GND	PASSIA

CONN 2		
	2	1
16	MC020	MC030
15	MC000	MC010
14	GND	S2BO
13	GND	PCLKO
12	GND	JUTYI
11	GND	RX3DO
10	GND	SPARE
09	GND	CS000
08	GND	STRTIA
07	GND	GND
06	GND	GND
05	BSEL031	BSEL041
04	BSEL011	BSEL021
03	GND	BSEL001
02	SSEL031	SSEL041
01	SSEL011	SSEL021
00	GND	SSEL001

CONN 3		
	2	1
24	GND	GND
23	CSAD141	GND
22	CSAD121	CSADI51
21	GND	CSADI31
20	CSAD101	CSADIII
19	CSAD081	GND
18	CSAD061	CSAD091
17	GND	CSAD071
16	CSA040	CSA050
15	GND	GND
14	GND	GND
13	GND	SPARE
12	GND	PCLKO
11	PSW251	SECLKI
10	PSW260	PSW270
09	GND	S2BO
08	ASEL031	ASEL041
07	ASEL011	ASEL021
06	GND	ASEL001
05	BSEL031	BSEL041
04	BSEL011	BSEL021
03	GND	BSEL001
02	SSEL031	SSEL041
01	SSEL011	SSEL021
00	GND	SSEL001

CONN 4		
	2	1
24	CSD301	CSD311
23	CSD281	CSD291
22	GND	CSD271
21	CSD261	CSD251
20	CSD241	GND
19	CSD221	CSD231
18	GND	CSD211
17	CSD201	CSD191
16	CSD181	GND
15	CSD161	CSD171
14	GND	CSD151
13	CSD141	CSD131
12	CSD121	GND
11	CSD101	CSDIII
10	GND	CSD091
09	CSD081	CSD071
08	CSD061	GND
07	CSD041	CSD051
06	GND	CSD031
05	CSD021	CSD011
04	CSD001	GND
03	GND	CSWPO
02	GND	INCLKO
01	GND	CLKO
00	GND	GND



REVISIONS

ADDED: "MSIGO" ON SHT. 2 TO CPA PIN 240-1.					
KR/KT	03088 43			3-24-75	R01
ADDER: SHT. 1 "PRPCO" MNEMONIC TO PIN 128-0 F228-0 SLOTS 00 THRU 02. SHT. 2 "LMBSYAO" TO PIN 139-0 SLOTS 02 THRU 07, "LMBSYCO" TO PIN 239-0 SLOTS 02 THRU 07. CHANGED: PIN 137-0 SLOT 01 WAS "LMBSYO", PIN 137-0 SLOTS 02 THRU 07 WERE LMBSYO.					
KR/KT	03088 43			3-24-75	R02
ADDED: SHEET 4.					
KR/KT	03088 52			3-24-76	R03
CONN 2 ROW 1 PIN 08 STRTIA WAS SRTI. CONN 3 ROW 2 PIN 16 CSA040 WAS CSAD041. CONN 3 ROW 1 PIN 16 CSA050 WAS CSAD051. REVISED SHTS 1 & 4.					
KR/KT	4231	R		3-4-80	R04

SCALE –	NAME	TITLE	DATE
TOLERANCE UNLESS OTHERWISE SPECIFIED	G. MELTON	DRAFT	2-14-74
		CHK	2-18-74
		ENGR	
		QA	
		MGR	

TITLE: CPA/CPB, CPB/CPC FRONT END CABLING

DWG NO. 03088
SIZE D
SCALE 01-078 R04 D08
SHEET 4-4

DRAWING 44-231, 24538

PERKIN-ELMER

BACK PANEL MAP

CONN.	TITLE	CPB AA07 ROW 1	CPB AA07 ROW 2	DCB AA06 ROW 1	DCB AA06 ROW 2	DFUB AA05 ROW 1	DFUB AA05 ROW 2	DFUA AA04 ROW 1	DFUA AA04 ROW 2	CONN.	TITLE	ALU AA03 ROW 1	ALU AA03 ROW 2	SPARE AA02 ROW 1	SPARE AA02 ROW 2	SPARE AA01 ROW 1	SPARE AA01 ROW 2	IOU AA00 ROW 1	IOU AA00 ROW 2	TITLE	CONN.
	BD.LOC.										BD.LOC.									BD.LOC.	
	TERM. NO.										TERM. NO.									TERM. NO.	
	41	P5	P5	P5	P5	P5	P5	P5	P5		41	P5	P5	P5	P5	P5	P5	P5	P5	41	
	40	GND	GND	GND	GND	GND	GND	GND	GND		40	GND	GND	GND	GND	GND	GND	GND	GND	40	
	39	DSPYL0	PPF0								39							PIS	PPE0	39	
	38	ATN020	ATN030								38							NIS	DSPYL0	38	
	37	ATN000	ATN010								37							RACK0	TACK0	37	
	36	GND	GND	GND	GND	GND	GND	GND	GND		36	GND	GND	GND	GND	GND	GND	GND	GND	36	
	35	B300	B310	B300	B310	B300	B310	B300	B310		35	B300	B310	B300	B310	B300	B310	B300	B310	35	
	34	B280	B290	B280	B290	B280	B290	B280	B290		34	B280	B290	B280	B290	B280	B290	B280	B290	34	
	33	B260	B270	B260	B270	B260	B270	B260	B270		33	B260	B270	B260	B270	B260	B270	B260	B270	33	
	32	B240	B250	B240	B250	B240	B250	B240	B250		32	B240	B250	B240	B250	B240	B250	B240	B250	32	
	31	GND	GND	GND	GND	GND	GND	GND	GND		31	GND	GND	GND	GND	GND	GND	GND	GND	31	
	30	B220	B230	B220	B230	B220	B230	B220	B230		30	B220	B230	B220	B230	B220	B230	B220	B230	30	
	29	B200	B210	B200	B210	B200	B210	B200	B210		29	B200	B210	B200	B210	B200	B210	B200	B210	29	
	28	B180	B190	B180	B190	B180	B190	B180	B190		28	B180	B190	B180	B190	B180	B190	B180	B190	28	
	27	B160	B170	B160	B170	B160	B170	B160	B170		27	B160	B170	B160	B170	B160	B170	B160	B170	27	
	26	GND	GND	GND	GND	GND	GND	GND	GND		26	GND	GND	GND	GND	GND	GND	GND	GND	26	
	25	S300	S310	S300	S310	S300	S310	S300	S310		25	S300	S310	S300	S310	S300	S310	S300	S310	25	
	24	S280	S290	S280	S290	S280	S290	S280	S290		24	S280	S290	S280	S290	S280	S290	S280	S290	24	
	23	S260	S270	S260	S270	S260	S270	S260	S270		23	S260	S270	S260	S270	S260	S270	S260	S270	23	
	22	S240	S250	S240	S250	S240	S250	S240	S250		22	S240	S250	S240	S250	S240	S250	S240	S250	22	
1	21	GND	GND	GND	GND	GND	GND	GND	GND	1	21	GND	GND	GND	GND	GND	GND	GND	GND	21	1
	20	S220	S230	S220	S230	S220	S230	S220	S230		20	S220	S230	S220	S230	S220	S230	S220	S230	20	
	19	S200	S210	S200	S210	S200	S210	S200	S210		19	S200	S210	S200	S210	S200	S210	S200	S210	19	
	18	S180	S190	S180	S190	S180	S190	S180	S190		18	S180	S190	S180	S190	S180	S190	S180	S190	18	
	17	S160	S170	S160	S170	S160	S170	S160	S170		17	S160	S170	S160	S170	S160	S170	S160	S170	17	
	16	GND	GND	GND	GND	GND	GND	GND	GND		16	GND	GND	GND	GND	GND	GND	GND	GND	16	
	15	A300	A310	A300	A310	A300	A310	A300	A310		15	A300	A310	A300	A310	A300	A310	A300	A310	15	
	14	A280	A290	A280	A290	A280	A290	A280	A290		14	A280	A290	A280	A290	A280	A290	A280	A290	14	
	13	A260	A270	A260	A270	A260	A270	A260	A270		13	A260	A270	A260	A270	A260	A270	A260	A270	13	
	12	A240	A250	A240	A250	A240	A250	A240	A250		12	A240	A250	A240	A250	A240	A250	A240	A250	12	
	11	GND	GND	GND	GND	GND	GND	GND	GND		11	GND	GND	GND	GND	GND	GND	GND	GND	11	
	10	A220	A230	A220	A230	A220	A230	A220	A230		10	A220	A230	A220	A230	A220	A230	A220	A230	10	
	09	A200	A210	A200	A210	A200	A210	A200	A210		09	A200	A210	A200	A210	A200	A210	A200	A210	09	
	08	A180	A190	A180	A190	A180	A190	A180	A190		08	A180	A190	A180	A190	A180	A190	A180	A190	08	
	07	A160	A170	A160	A170	A160	A170	A160	A170		07	A160	A170	A160	A170	A160	A170	A160	A170	07	
	06	GND	GND	GND	GND	GND	GND	GND	GND		06	GND	GND	GND	GND	GND	GND	GND	GND	06	
	05	MMF0	PSW230								05							MME0	DMPF0	05	
	04										04								FWINT0	04	
	03	MSEL020	RWC0	MSEL020	RWC0	MSEL020	RWC0	MSEL020	RWC0		03	MSEL020	RWC0	MSEL020	RWC0	MSEL020	RWC0	MSEL020	RWC0	03	
	02	MSEL000	MSGL010	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSGL010		02	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	MSEL000	MSEL010	02	
	01	GND	MSI60	GND	MSI60	GND	MSI60	GND	MSI60		01	GND	MSI60	GND	MSI60	GND	MSI60	GND	MSI60	01	
	00	P5	P5	P5	P5	P5	P5	P5	P5		00	P5	P5	P5	P5	P5	P5	P5	P5	00	
		1	2	1	2	1	2	1	2			1	2	1	2	1	2	1	2		
	41	P5	P5	P5	P5	P5	P5	P5	P5		41	P5	P5	P5	P5	P5	P5	P5	P5	41	
	40	GND	KSI60	GND	KSI60	GND	KSI60	GND	KSI60		40	GND	KSI60	GND	KSI60	GND	KSI60	GND	KSI60	40	
	39	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030		39	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	FSEL020	FSEL030	39	
	38	FSEL000	FSEL010	FSEL000	FSES010	FSEL000	FSEL010	FSEL000	FSEL010		38	FSEL000	FSEL010	FSEL000	FSEL010	FSEL000	FSEL010	FSEL000	FSEL010	38	
	37	STRT0	MFIN0	STRT0	MEIN0	STRT0	MFIN0	STRT0	MFIN0		37	STRT0	MFIN0	STRT0	MEIN0	STRT0	MEIN0	STRT0	MEIN0	37	
	36	GND	GND	GND	GND	GND	GND	GND	GND		36	GND	GND	GND	GND	GND	GND	GND	GND	36	
	35	B140	B150	B140	B150	B140	B150	B140	B150		35	B140	B150	B140	B150	B140	B150		RACK0	35	
	34	B120	B130	B120	B130	B120	B130	B120	B130		34	B120	B130	B120	B130	B120	B130	GND	GND	34	
	33	B100	B110	B100	B110	B100	B110	B100	B110		33	B100	B110	B100	B110	B100	B110		LMRR0	33	
	32	B080	B090	B080	B090	B080	B090	B080	B090		32	B080	B090	B080	B090	B080	B090	MAR310	ATN0	32	
	31	GND	GND	GND	GND	GND	GND	GND	GND		31	GND	GND	GND	GND	GND	GND	GND	GND	31	
	30	B060	B070	B060	B070	B060	B070	B060	B070		30	B060	B070	B060	B070	B060	B070	ACK030	MTPC0	30	
	29	B040	B050	B040	B050	B040	B050	B040	B050		29	B040	B050	B040	B050	B040	B050	ACK020	PRPC0	29	
	28	B020	B030	B020	B030	B020	B030	B020	B030		28	B020	B030	B020	B030	B020	B030	ACK010	GND	28	
	27	B000	B010	B000	B010	B000	B010	B000	B010		27	B000	B010	B000	B010	B000	B010	ACK000	HW0	27	
	26	GND	GND	GND	GND	GND	GND	GND	GND		26	GND	GND	GND	GND	GND	GND	GND	GND	26	
	25	S140	S150	S140	S150	S140	S150	S140	S150		25	S140	S150	S140	S150	S140	S150	GND	GND	25	
	24	S120	S130	S120	S130	S120	S130	S120	S130		24	S120	S130	S120	S130	S120	S130			24	
	23	S100	S110	S100	S110	S100	S110	S100	S110		23	S100	S110	S100	S110	S100	S110	SYN0	BH0	23	
	22	S080	S090	S080	S090	S080	S090	S080	S090		22	S080	S090	S080	S090	S080	S090	CL070	DA0	22	
0	21	GND	GND	GND	GND	GND	GND	GND	GND	0	21	GND	GND	GND	GND	GND	GND	GND	GND	21	0
	20	S060	S070	S060	S070	S060	S070	S060	S070		20	S060	S070	S060	S070	S060	S070	DE0	CMD0	20	
	19	S040	S050	S040	S050	S040	S050	S040	S050		19	S040	S050	S040	S050	S040	S050	SR0	AD280	19	
	18	S020	S030	S020	S030	S020	S030	S020	S030		18	S020	S030	S020	S030	S020	S030	D140	DI50	18	
	17	S000	S010	S000	S010	S000	S010	S000	S010		17	S000	S010	S000	S010	S000	S010	DI20	DI30	17	
	16	GND	GND	GND	GND	GND	GND	GND	GND		16	GND	GND	GND	GND	GND	GND	GND	GND	16	
	15	A140	A150	A140	A150	A140	A150	A140	A150		15	A140	A150	A140	A150	A140	A150	DI00	DI10	15	
	14	A120	A130	A120	A130	A120	A130	A120	A130		14	A120	A130	A120	A130	A120	A130	DO80	DO90	14	
	13	A100	A110	A100	A110	A100	A110	A100	A110		13	A100	A110	A100	A110	A100	A110	DO60	DO70	13	
	12	A080	A090	A080	A090	A080	A090	A080	A090		12	A080	A090	A080	A090	A080	A090	DO40	DO50	12	
	11	GND	GND	GND	GND	GND	GND	GND	GND		11	GND	GND	GND	GND	GND	GND	GND	GND	11	
	10	A060	A070	A060	A070	A060	A070	A060	A070		10	A060	A070	A060	A070	A060	A070	DO20	DO30	10	
	09	A040	A050	A040	A050	A040	A050	A040	A050		09	A040	A050	A040	A050	A040	A050	DO00	DO10	09	
	08	A020	A030	A020	A030	A020	A030	A020	A030		08	A020	A030	A020	A030	A020	A030			08	
	07	A000	A010	A000	A010	A000	A010	A000	A010		07	A000	A010	A000	A010	A000	A010			07	
	06	GND	GND	GND	GND	GND	GND	GND	GND		06	GND	GND	GND	GND	GND	GND	GND	GND	06	
	05	SCLR0	CCC0	SCLR0	CCC0	SCLR0	CCC0	SCLR0	CCC0		05	SCLR0	CCC0	SCLR0	CCC0	SCLR0	CCC0	SCLR0	CCC0	05	
	04	SCC0	VCC0	SCC0	VCC0	SCC0	VCC0	SCC0	VCC0		04	SCC0	VCC0	SCC0	VCC0	SCC0	VCC0	SCC0	VCC0	04	
	03	SCLR1	GCC0	SCLR1	GCC0	SCLR1	GCC0	SCLR1	GCC0		03	SCLR1	GCC0	SCLR1	GCC0	SCLR1	GCC0	SCLR1	GCC0	03	
	02	TKILL0	LCC0		LCC0		LCC0		LCC0		02		LCC0		LCC0		LCC0		LCC0	02	
	01	GND	GND	GND	GND	GND	GND	GND	GND		01	GND	GND	GND	GND	GND	GND	GND	GND	01	
	00	P5	P5	P5	P5	P5	P5	P5	P5		00	P5	P5	P5	P5	P5	P5	P5	P5	00	
		1	2	1	2	1	2	1	2			1	2	1	2	1	2	1	2		

NOTES

1. BACKPANEL - 35-592.

REVISIONS (CONT.)

REVISED SHTS 1 & 4. AREA R5 TERM NO. 05 & 04 DMPO WAS IRLMP0, FWINT0 WAS DMPF0. REVISED SHT 2 ALSO

KR 471 4231 R 3-6-80 R03

GP 471 3537 3-16-78 R02

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED THE REVISION LEVEL OF THE DOCUMENT

RELEASED FOR PRODUCTION

ENG. _____ DATE 2-19-76

SHEET INDEX

SHT. NO.	REV. LTR.
1	3
2	1
3	-
4	2

PRE PRODUCTION APPROVAL	INIT	DATE
REVISED SHTS 1 & 4. AREA B1: DSPYL0 WAS DSPLY1. DELETED ALL REF TO WIRE WRAP PINS.	DEV	2-19-76
	ENG	2-19-76
	MFG	2-19-76
	QA	2-19-76
	PE	2-19-76
	DES	2-19-76
	DES	2-19-76

NAME	TITLE	DATE
B. GRAY	DRAFT	2-19-76
R. CERO	CHK	2-19-76
G. WELLY	ENGR	2-19-76
R. BARKER		2-19-76
S. MESSINA	DIR ENG	2-19-76

TITLE (LOWER BACKPANEL) MODEL 8/32 C (W/DFU BACKPANEL)

TASK NO. 03150

DRG NO. 01-098803008

SHEET OF 1 - 4

PERKIN ELMER

BACK PANEL MAP

CONN.	TITLE	LMM	LMI NOTE 2	LMM	LMM
	BD. LOC.	A07	A06	A05	A04
	TERM.	ROW	ROW	ROW	ROW
	NO.	1 2	1 2	1 2	1 2
1	41	PS GND	PS PS	PS GND	PS GND
	40	GND GND	GND GND	GND GND	GND GND
	39	P15 P15		P15 P15	P15 P15
	38	N15 N15		N15 N15	N15 N15
	37	MD150 MD160	MD150 MD160	MD150 MD160	MD150 MD160
	36	MD130 MD140	MD130 MD140	MD130 MD140	MD130 MD140
	35	MD110 MD120	MD110 MD120	MD110 MD120	MD110 MD120
	34	MD090 MD100	MD090 MD100	MD090 MD100	MD090 MD100
	33	MD070 MD080	MD070 MD080	MD070 MD080	MD070 MD080
	32	MD050 MD060	MD050 MD060	MD050 MD060	MD050 MD060
	31	MD030 MD040	MD030 MD040	MD030 MD040	MD030 MD040
	30	MD010 MD020	MD010 MD020	MD010 MD020	MD010 MD020
	29	GND MD000	GND MD000	GND MD000	GND MD000
	28	TEMPA ⊛ VT ⊛	TEMPA ⊛ VT ⊛	TEMPA ⊛ VT ⊛	TEMPA ⊛ VT ⊛
	27	WRTO TEMP B ⊛	0WRTO	WRTO TEMP B ⊛	WRTO TEMP B ⊛
	26	GND GND	GND GND	GND GND	GND GND
	25	LMB300 LMB310	LMB300 LMB310	LMB300 LMB310	LMB300 LMB310
	24	LMB280 LMB290	LMB280 LMB290	LMB280 LMB290	LMB280 LMB290
	23	LMB260 LMB270	LMB260 LMB270	LMB260 LMB270	LMB260 LMB270
	22	LMB240 LMB250	LMB240 LMB250	LMB240 LMB250	LMB240 LMB250
	21	LMB220 LMB230	LMB220 LMB230	LMB220 LMB230	LMB220 LMB230
	20	LMB200 LMB210	LMB200 LMB210	LMB200 LMB210	LMB200 LMB210
	19	GND GND	GND GND	GND	GND GND
	18				
	17				
	16	GND GND	GND GND	GND	GND GND
	15				
	14				
	13				
	12				
	11	GND GND	GND GND	GND	GND GND
	10	EWRT0 MS000	EWRT0 MS000	EWRT0 MS000	MS000
	09	MS010 MS020	MS010 MS020	MS010 MS020	MS010 MS020
	08	MS030 MS040	MS030 MS040	MS030 MS040	MS030 MS040
	07	MS050 MS060	MS050 MS060	MS050 MS060	MS050 MS060
	06	MS070 MS080	MS070 MS080	MS070 MS080	MS070 MS080
	05	MS090 MS100	MS090 MS100	MS090 MS100	MS090 MS100
	04	MS110 MS120	MS110 MS120	MS110 MS120	MS110 MS120
	03	MS130 MS140	MS130 MS140	MS130 MS140	MS130 MS140
	02	MS150 MS160	MS150 MS160	MS150 MS160	MS150 MS160
	01	GND GND	GND GND	GND GND	GND GND
	00	PS GND	PS PS	PS GND	PS GND
		1 2	1 2	1 2	1 2
0	41	PS GND	PS PS	PS GND	PS GND
	40	GND GND	GND	GND	GND
	39	LMB5YA0 LMB5YC0	LMB5YA0 LMB5YC0	LMB5YA0 LMB5YC0	LMB5YA0 LMB5YC0
	38	LMRDY0 LMDS0	LMRDY0 LMDS0	LMRDY0 LMDS0	LMRDY0 LMDS0
	37	LMB5YB0 LMRS0	LMB5YB0 LMRS0	LMB5YB0 LMRS0	LMB5YB0 LMRS0
	36	GND GND	GND GND	GND GND	GND GND
	35	DUA0 MB20	DUA0 MB20	DUA0 MB20	DUA0 MB20
	34	GND GND	GND GND	GND	GND GND
	33	MA130 MA140	MA130 MA140	MA130 MA140	MA130 MA140
	32	MA110 MA120	MA110 MA120	MA110 MA120	MA110 MA120
	31	MA090 MA100	MA090 MA100	MA090 MA100	MA090 MA100
	30	MA070 MA080	MA070 MA080	MA070 MA080	MA070 MA080
	29	MA050 MA060	MA050 MA060	MA050 MA060	MA050 MA060
	28	GND GND	GND GND	GND	GND GND
	27	SCLR0	SCLR0	SCLR0	SCLR0
	26	MCLR0 GND	MCLR0 GND	MCLR0 GND	MCLR0 GND
	25	GND GND	GND GND	GND GND	GND GND
	24	LMB180 LMB190	LMB180 LMB190	LMB180 LMB190	LMB180 LMB190
	23	LMB160 LMB170	LMB160 LMB170	LMB160 LMB170	LMB160 LMB170
	22	LMB140 LMB150	LMB140 LMB150	LMB140 LMB150	LMB140 LMB150
	21	GND GND	GND GND	GND GND	GND GND
0	20	LMB120 LMB130	LMB120 LMB130	LMB120 LMB130	LMB120 LMB130
	19	LMB100 LMB110	LMB100 LMB110	LMB100 LMB110	LMB100 LMB110
	18	LMB080 LMB090	LMB080 LMB090	LMB080 LMB090	LMB080 LMB090
	17	LMB060 LMB070	LMB060 LMB070	LMB060 LMB070	LMB060 LMB070
	16	LMB040 LMB050	LMB040 LMB050	LMB040 LMB050	LMB040 LMB050
	15	LMB020 LMB030	LMB020 LMB030	LMB020 LMB030	LMB020 LMB030
	14	LMB000 LMB010	LMB000 LMB010	LMB000 LMB010	LMB000 LMB010
	13	GND GND	GND GND	GND GND	GND GND
	12	IRLMP0 DLMP0	IRLMP0 DLMP0	IRLMP0 DLMP0	IRLMP0 DLMP0
	11	GND GND	GND GND	GND GND	GND GND
	10	MA030 MA040	MA030 MA040	MA030 MA040	MA030 MA040
	09	MA020	MA020	MA020	MA020
	08	MAX060 MAX070	MAX060 MAX070	MAX060 MAX070	MAX060 MAX070
	07	MA010	MA010	MA010	MA010
	06	MA000	MA000 GND	MA000	MA000
	05	PAR0	PAR0	PAR0	PAR0
	04	INH0 ER0	INH0 ER0	INH0 ER0	INH0 ER0
	03	SPY	SPY	SPY	SPY
	02	PI5 NI5			PI5 NI5
	01	GND GND	GND GND	GND GND	GND GND
	00	PS GND	PS PS	PS GND	PS GND
		1 2	1 2	1 2	1 2

CONN.	TITLE	LMI (NOTE 2)	LMM	MBC	CPA	TITLE	CONN.
	BD. LOC.	A03	A02	A01	A00	BD. LOC.	
	TERM.	ROW	ROW	ROW	ROW	TERM	
	NO.	1 2	1 2	1 2	1 2	NO.	
1	41	PS PS	PS GND	PS PS	PS PS	41	
	40	GND GND	GND GND	GND QUE0	GND MSIG0	40	
	39			DMA160 DMA170	B300 B310	39	
	38			DMA140 DMA150	B280 B290	38	
	37	MD150 MD160	MD150 MD160	DMA120 DMA130	B260 B270	37	
	36	MD130 MD140	MD130 MD140	GND GND	GND GND	36	
	35	MD110 MD120	MD110 MD120	DMA100 DMA110	B240 B250	35	
	34	MD090 MD100	MD090 MD100	DMA090 DMA090	B220 B230	34	
	33	MD070 MD080	MD070 MD080	DMA060 DMA070	B200 B210	33	
	32	MD050 MD060	MD050 MD060	DMA040 DMA050	B180 B190	32	
	31	MD030 MD040	MD030 MD040	DMA020 DMA030	B160 B170	31	
	30	MD010 MD020	MD010 MD020	GND GND	GND GND	30	
	29	GND MD000	GND MD000	DMA000 DMA010	S300 S310	29	
	28		TEMPA ⊛ VT ⊛	DMX140 DMX150	S280 S290	28	
	27	0WRT0	WRT0 TEMP B ⊛	DMX120 DMX130	S260 S270	27	
	26	GND GND	GND GND	GND GND	GND GND	26	
	25	LMB300 LMB310	LMB300 LMB310	LMB300 LMB310	S240 S250	25	
	24	LMB280 LMB290	LMB280 LMB290	LMB280 LMB290	S220 S230	24	
	23	LMB260 LMB270	LMB260 LMB270	LMB260 LMB270	S200 S210	23	
	22	LMB240 LMB250	LMB240 LMB250	LMB240 LMB250	S180 S190	22	
	21	LMB220 LMB230	LMB220 LMB230	LMB220 LMB230	S160 S170	21	
1	20	LMB200 LMB210	LMB200 LMB210	LMB200 LMB210	GND GND	20	1
	19	GND GND	GND GND	GND CRDY0	GND CRDY0	19	
	18			CMC020 CREQ0	CMC020 CREQ0	18	
	17			CMC000 CMC010	CMC000 CMC010	17	
	16	GND GND	GND GND	GND GND	GND GND	16	
	15			CD300 CD310	CD300 CD310	15	
	14			CD280 CD290	CD280 CD290	14	
	13			CD260 CD270	CD260 CD270	13	
	12			CD240 CD250	CD240 CD250	12	
	11	GND GND	GND GND	GND GND	GND GND	11	
	10	EWRT0 MS000	EWRT0 MS000	CD220 CD230	CD220 CD230	10	
	09	MS010 MS020	MS010 MS020	CD200 CD210	CD200 CD210	09	
	08	MS030 MS040	MS030 MS040	CD180 CD190	CD180 CD190	08	
	07	MS050 MS060	MS050 MS060	CD160 CD170	CD160 CD170	07	
	06	MS070 MS080	MS070 MS080	GND GND	GND GND	06	
	05	MS090 MS100	MS090 MS100	M3820 M2820	B140 B150	05	
	04	MS110 MS120	MS110 MS120	M1820 M0820	B120 B130	04	
	03	MS130 MS140	MS130 MS140	LOAD0 RN50	B100 B110	03	
	02	MS150 MS160	MS150 MS160	SOT0 EOT0	B080 B090	02	
	01	GND GND	GND GND	GND XPEQ0	GND B070	01	
	00	PS PS	PS GND	PS PS	PS PS	00	
		1 2	1 2	1 2	1 2		
0	41	PS PS	PS GND	PS PS	PS PS	41	0
	40	GND GND	GND GND	GND MTPC0 ⊛	GND B060	40	
	39	LMB5YA0 LMB5YC0	LMB5YA0 LMB5YC0	LMEQ0 ⊛ BH0 ⊛	B040 B050	39	
	38	LMRDY0 LMDS0	LMRDY0 LMDS0	LMRDY0 LMDS0	B020 B030	38	
	37	LMB5YB0 LMRS0	LMB5YB0 LMRS0	PRPC0 ⊛ LMRS0	B000 B010	37	
	36	GND GND	GND GND	GND GND	GND GND	36	
	35	DUA0 MB20	DUA0 MB20	CD140 CD150	CD140 CD150	35	
	34	GND GND	GND GND	CD120 CD130	CD120 CD130	34	
	33	MA130 MA140	MA130 MA140	CD100 CD110	CD100 CD110	33	
	32	MA110 MA120	MA110 MA120	CD080 CD090	CD080 CD090	32	
	31	MA090 MA100	MA090 MA100	GND GND	GND GND	31	
	30	MA070 MA080	MA070 MA080	CD060 CD070	CD060 CD070	30	
	29	MA050 MA060	MA050 MA060	CD040 CD050	CD040 CD050	29	
	28	GND GND	GND GND	CD020 CD030	CD020 CD030	28	
	27	SCLR0	SCLR0	CD000 CD010	CD000 CD010	27	
	26	MCLR0 GND	MCLR0 GND	GND GND	GND GND	26	
	25	GND GND	GND GND	SCLR0 GND	SCLR0 GND	25	
	24	LMB180 LMB190	LMB180 LMB190	LMB180 LMB190	S140 S150	24	
	23	LMB160 LMB170	LMB160 LMB170	LMB160 LMB170	S120 S130	23	
0	22	LMB140 LMB150	LMB140 LMB150	LMB120 LMB130	S100 S110	22	0
	21	GND GND	GND GND	GND GND	GND GND	21	
	20	LMB120 LMB130	LMB120 LMB130	LMB120 LMB130	FWINT0	20	
	19	LMB100 LMB110	LMB100 LMB110	LMB100 LMB110	S080 S090	19	
	18	LMB080 LMB090	LMB080 LMB090	LMB080 LMB090	S060 S070	18	
	17	LMB060 LMB070	LMB060 LMB070	LMB060 LMB070	S040 S050	17	
	16	LMB040 LMB050	LMB040 LMB050	LMB040 LMB050	S020 S030	16	
	15	LMB020 LMB030	LMB020 LMB030	LMB020 LMB030	S000 S010	15	
	14	LMB000 LMB010	LMB000 LMB010	LMB000 LMB010		14	
	13	GND GND	GND GND	GND GND	GND GND	13	
	12	IRLMP0 DLMP0	IRLMP0 DLMP0	CA300 DLMP0	CA300 MAR310 ⊛	12	
	11	GND GND	GND GND	CA280 CA290	CA280 CA290	11	
	10	MA030 MA040	MA030 MA040	CA260 CA270	CA260 CA270	10	
	09	MA020	MA020	CA240 CA250	CA240 CA250	09	
	08	MAX060 MAX070	MAX060 MAX070	CA220 CA230	CA220 CA230	08	
	07	MA010	MA010	CA200 CA210	CA200 CA210	07	
	06	MA000 GND	MA000	GND GND	GND GND	06	
	05	PAR0	PAR0	CA180 CA190	CA180 CA190	05	
	04	INH0 ER0	INH0 ER0	CA160 CA170	CA160 CA170	04	
	03	SPY	SPY	CA140 CA150	CA140 CA150	03	
	02	PI5 NI5		CA120 CA130	CA120 CA130	02	
	01	GND GND	GND GND	GND DMEP0 ⊛	GND GND	01	
	00	PS PS	PS GND	PS PS	PS PS	00	
		1 2	1 2	1 2	1 2		

NOTES
1. BACKPANEL — 35-540
⊛ WIRE WRAP RUNS
2. SLOT ASSIGNMENTS SHOWN FOR THE BASIC 128 KB MEMORY SYSTEM

THE LMI BOARDS ARE RE-ASSIGNED WHEN THE SYSTEM IS EXPANDED WITH CORRESPONDING CHANGES IN MA, MD, & MS STRAPPING OPTIONS

REVISIONS

AREA N7-TERM NO 20 FWINT0 WAS ADDED			
GP	3537	3-16-78	R01

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE (UPPER BACKPANEL) MODEL 8/32 C (W/DFU BACKPANEL)

TASK NO. 03150 SHEET OF 2 - 4

DWG NO. 01-098R01D08

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

DMA WRITE DATA BUFFERS

DMA CONTROL BITS FROM DMA 15:17

DMA 16 AND 17 TRANSCEIVERS

DMA

ADDRESS

COUNTER

REGISTER

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION:
8/32 MBC 35-535R25

USED IN MANUAL 29-394

NOTE: THIS REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

CONTINUED BELOW

REVISIONS

PRE PRODUCTION APPROVAL	INIT DATE
	DEV 2-27 Nov 8,74
	PROD [illegible] 11-5-74

REVISED PER ECO'S ON INDICATED SHEETS

3/4	RPT	03088-27	1-27-75	R01

ADDED 03E TO M6 LMREQRI WAS NC 00S12 WENT TO 00S15 ADDED 00S11 & 14 WENT TO PSRB, 00S10 WAS NC

3/4	RPT	03088-28	2-7-75	R02

CHANGED: SHT 12 WAS R02 REVISION.

3/4	RPT	03088-46	2-10-75	R03

CHANGED: SHT 1 WAS R03 SHT 5 WAS R00, SHT 7 WAS R01, SHTS, 10, 11, 13 & 14 WERE R02

SHT 1	RPT	03088-66	4-16-75	R04

REV LEV OF SHT 11 WAS R03 " " " " " R03

SHT 1	RPT	03088-74	5-1-75	R05

RELEASED FOR PRODUCTION ENG. [illegible] 75

35-535 P.C. BOARD REF IN AREA 59 WAS R05
REV LEV OF SHT 1 WAS R05
" " " " 9 WAS R02
" " " " 12 WAS R03
" " " " 10 WAS R03

SHT 1	KCA	2526	5-30-75	R06

AREA 59, 35-535 WAS R09. CHG. SHT 6, REV LEVEL WAS R01. CHG. SHT 13, REV LEVEL WAS R03.

3/4	RPM	2575	7-18-75	R07

REVISED SHT 9.

3/4	KC	2570	8-26-75	R08

AREA 59, 35-535 WAS R10. CHG. SHT. 10.

3/4	KC	2601	9-9-75	R09

REVISED SHTS 9 & 10, SUPPLEMENTARY INFO TABLE 8/32 MBC WAS R11

2/3	RM	2662	10-30-75	R10

REVISED SHT 11, SUPPLEMENTARY INFO TABLE 8/32 MBC WAS R13

WS	RM	2663	10-30-75	R11

REVISED SHTS 9 THRU 13. SUPPLEMENTARY INFO TABLE 8/32 MBC WAS R14

3/4		2727	3-1-76	R12

REVISED SHTS 11, 12 & 13. TABLE 8/32 MBC WAS R15

JH	KWZ	2758	3-12-76	R13

REVISED SHT 13, TABLE 8/32 MBC WAS R16

WS		2808	4-8-76	R14

REVISED SHTS 11 & 13 8/32 MBC WAS R18

VC	VRB	2840	5-10-76	R15

REVISED SHTS 1, 9, 10, 11, 12, 13, 35-535 REV LEV WAS R18.

WS	RM	3107	3-7-77	R16

REVISED SHT'S 12, 13, & 14. 8/32 MBC WAS REV LEV R21

PM	RM	3176	4-21-77	R17

REVISIONS (CONT'D)

REVISED SHTS 1, 11 & 13. 35-535 WAS R22.

GS	RM	3172	5-10-77	R18

REVISED SHT 13.

GS	RM	3186	7-8-77	R19

REVISED SHTS 1, 11/12/13 & 14. 35-535 WAS R23.

GS	RM	3476	12-23-77	R20

REVISED SHT. 8, 35-535 WAS R24.

GP	RM	3420	2-17-78	R21

REVISED SHT 10. ADDED MANUAL REF THIS SHT. AREA 59.

GS	VRL	3531	5-23-78	R22

REVISED SHTS 1, 10, & 14.

VTW	LI	9007-06	10-22-80	R23

SHEET INDEX	REV LEVEL	23	1		1	1	2		3	6	10	11	9	13	7
	SHEET NO.	1	2	3	4	5	6	7	8	9	VC	11	12	13	14

NOTES

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	10-14-74
G.W. HOMEFIELD	CHK	
T. FYFE	ENGR	
S. MESSINA	MGR	
R.A. BARKER	QC	

TITLE: FUNCTIONAL SCHEMATIC 8/32 MBC

TASK NO. 03088 DWG NO. 35-535 R23D08 SHEET OF 1-14

BRUNING 44-231 16042

BRUNING 44 731 16042

CTEB1 12L4

P5RA A7, 2A1, 5G2, 3D7

DMA000 01 (129-1) DMA001 03 (1A1, 1E6) DMA010 04 (229-1) DMR011 06 (1B1, 1D6) DMA020 12 (131-1) DMR021 10 (1B1, 1E6) DMA030 15 (231-1) DMR031 13 (1B1, 1E6) 10E9 DMENBO

03W 19-118 QUAD BUS XCEIVER — ENB, B0 B1 B2 B3, A0 A1 A2 A3, SEL, I0 I1 I2 I3

DMT001 DMT011 DMT021 DMT031

03T 19-132 QUAD 2:1 MUX — SEL, 1Y 2Y 3Y 4Y, 1A 2A 3A 4A, 1B 2B 3B 4B, ENB

LMF160 LMF000 LMF170 LMF010 LMF180 LMF020 LMF190 LMF030

03H 19-131 QUAD-D FLIP FLOP — CLR, 1D 2D 3D 4D, CLK, 1Q 2Q 3Q 4Q

LMB000 3C4 LMB010 3C4 LMB020 3C4 LMB030 3C5

DMA040 01 (132-1) DMR041 03 (1C1, 1E6) DMA050 04 (232-1) DMR051 06 (1C1, 1E6) DMA060 12 (133-1) DMR061 10 (1C1, 1F6) DMA070 15 (233-1) DMR071 13 (1D1, 1G6)

02W 19-118 QUAD BUS XCEIVER

DMT041 DMT051 DMT061 DMT071

02T 19-132 QUAD 2:1 MUX

LMF200 LMF040 LMF210 LMF050 LMF220 LMF060 LMF230 LMF070

02U 19-131 QUAD-D FLIP FLOP

LMB040 3F4 LMB050 3F4 LMB060 3F4 LMB070 3F5

DMA080 01 (134-1) DMR081 03 (1E1, 1G6) DMA090 04 (234-1) DMR091 06 (1E1, 1G6) DMA100 12 (135-1) DMR101 10 (1E1, 1H6) DMA110 15 (235-1) DMR111 13 (1E1, 1H6)

01W 19-118 QUAD BUS XCEIVER

DMT081 DMT091 DMT101 DMT111

01T 19-132 QUAD 2:1 MUX

LMF240 LMF080 LMF250 LMF090 LMF260 LMF100 LMF270 LMF110

01U 19-131 QUAD-D FLIP FLOP

LMB080 3K4 LMB090 3K4 LMB100 3K4 LMB110 3K5

DMA120 01 (137-1) DMR121 03 (1F1, 1H6) DMA130 04 (237-1) DMR131 06 (1F1, 1H6) DMA140 12 (138-1) DMR141 10 (1G1, 1A6) DMA150 15 (238-1) DMR151 13 (1G1, 1K6)

00W 19-118 QUAD BUS XCEIVER

DMT121 DMT131 DMT141 DMT151

00T 19-132 QUAD 2:1 MUX

LMF280 LMF120 LMF290 LMF130 LMF300 LMF140 LMF310 LMF150

CTEA0 12J3

00J 19-131 QUAD-D FLIP FLOP

LMB120 3C8 LMB130 3C9 LMB140 3C9 LMB150 3C9

CTBA0 10E6

DMCA0 01 (10C7) CAF160 02 (6F8) CAF170 04 (6J8) CAF180 06 (6J8) CAF190 10 (6L8) CAF200 12 (6L8) CAF210 14 (6A4) 15

03K 19-134 HEX BUFF/INV

03M 19-132 QUAD 2:1 MUX

CD160 4H3 CD000 4D1 CD170 4H4 CD010 4D2 CD180 4H4 CD020 4D2 CD190 4H4 CD030 4D2

03J 19-131 QUAD-D FLIP FLOP

LMB160 3F8 LMB170 3F8 LMB180 3F8 LMB190 3F6

01 CAF220 02 (6C4) CAF230 04 (6D4) CAF240 06 (6F4) CAF250 10 (6F4) CAF260 12 (6J4) CAF270 14 (6J4) 15

02M HEX BUFF/INV 19-134

02S 19-132 QUAD 2:1 MUX

CD200 4H8 CD040 4D3 CD210 4H8 CD050 4D4 CD220 4H8 CD060 4D4 CD230 4H9 CD070 4H4

02K 19-131 QUAD-D FLIP FLOP

LMB200 3K5 LMB210 3K6 LMB220 3K6 LMB230 3K6

01 CAF280 02 (6L4) CAF290 04 (6M4) CAF300 06 (6R4) CMCB000 10 (11H6) 12 14 15

03M HEX BUFF/INV 19-134

01S 19-132 QUAD 2:1 MUX

CD240 4N3 CD080 4D6 CD250 4N4 CD090 4D6 CD260 4N4 CD100 4D6 CD270 4N4 CD110 4D6

02K 19-131 QUAD-D FLIP FLOP

LMB240 3K8 LMB250 3K9 LMB260 3K9 LMB271 11H7

085 1K P5

DMT121 DMT131 DMT141 DMT151 DMT161 DMT171 1N8

11H7 CMCB011

11J7 IRQ

11G7 CMC021

DMAFWQ 11L1

00M 19-132 QUAD 2:1 MUX

CD280 4N8 CD120 4D8 CD290 4N8 CD130 4D8 CD300 4N8 CD140 4D8 CD310 4N9 CD150 4D9

00K 19-131 QUAD-D FLIP FLOP

LMB280 3N8 LMB290 3N9 LMB300 3N9 LMB310 3N9

CTBB0 10F6

LDLMF1 11G9

REVISIONS

CHANGED: 01M10 WAS CMC000 MNEMONIC. 6/4 TP 4-17-75 R01

Computer Systems Division Oceanport, N.J. 07757

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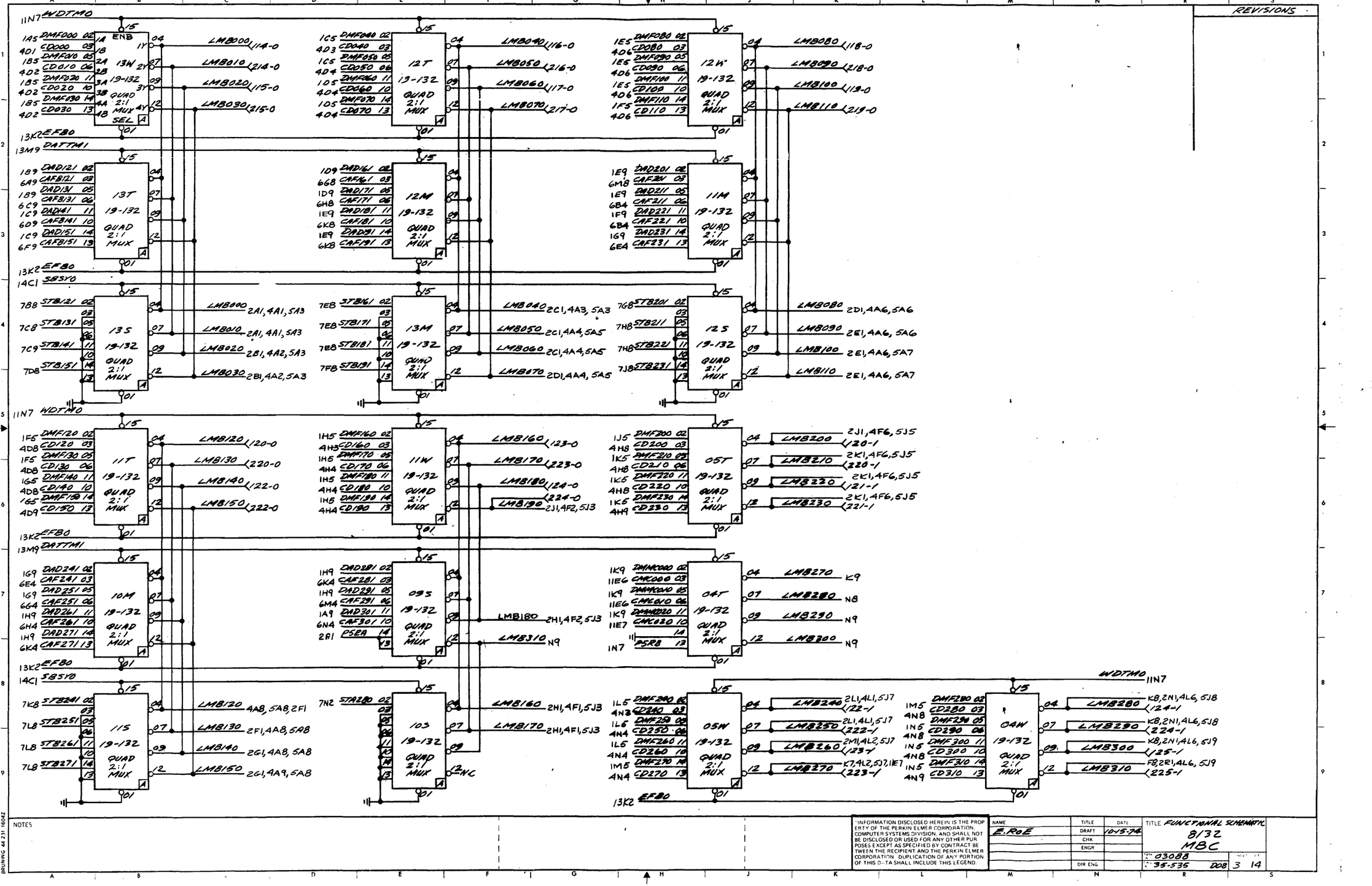
TITLE: FUNCT SCHEMATIC 8/32 MBC

03088 35535-R01 D08 SHEET 2 OF 14

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	10-15-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32
MBC

03088
35-535 D08

3 14

BRUNING 44 231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
EARTHE S/WT. 19-132's INVERTION BUBBLES ON PINS 4,7,9,12 WERE NOT SPEC'D.			
	2570	8-26-75	R01

11H6 RDDATO

3C4 LMB000 02 1A
1A5 DMF001 03 1B
3C4 LMB010 05 2A
1B5 DMF011 06 2B
3C4 LMB020 11 3A
1B5 DMF021 10 3B
3C5 LMB030 14 4A
1B5 DMF031 13 4B
SEL 01
MB00

ENB 15
10W 19-132 QUAD 2:1 MUX
A
1Y 04 CD000 → 127-0 (2H5,3A1)
2Y 07 CD010 → 227-0 (2H5,3A1)
3Y 09 CD020 → 128-0 (2H5,3A1)
4Y 12 CD030 → 228-0 (2J5,3A2)

RDDATO

3F4 LMB040 02 1A
1C5 DMF041 03 1B
3F4 LMB050 05 2A
1C5 DMF051 06 2B
3F4 LMB060 11 3A
1C5 DMF061 10 3B
3F5 LMB070 14 4A
1D5 DMF071 13 4B
01
MB00

15
10T 19-132 QUAD 2:1 MUX
A
04 CD040 → 129-0 (2K5,3D1)
07 CD050 → 229-0 (2K5,3D1)
09 CD060 → 130-0 (2K5,3D1)
12 CD070 → 230-0 (2K5,3D2)

RDDATO

3K4 LMB080 02 1A
1D5 DMF081 03 1B
3K4 LMB090 05 2A
1E5 DMF091 06 2B
3K4 LMB100 11 3A
1E5 DMF101 10 3B
3K5 LMB110 14 4A
1E5 DMF111 13 4B
01
MB00

15
09W 19-132 QUAD 2:1 MUX
A
04 CD080 → 132-0 (2L5,3H1)
07 CD090 → 232-0 (2L5,3H1)
09 CD100 → 133-0 (2M5,3H1)
12 CD110 → 233-0 (2M5,3H2)

RDDATO

3C8 LMB120 02 1A
1F5 DMF121 03 1B
3C9 LMB130 05 2A
1F5 DMF131 06 2B
3C9 LMB140 11 3A
1G5 DMF141 10 3B
3C9 LMB150 14 4A
1G5 DMF151 13 4B
01
9G8 MB00

15
09T 19-132 QUAD 2:1 MUX
A
04 CD120 → 134-0 (2N5,3A5)
07 CD130 → 234-0 (2N5,3A6)
09 CD140 → 135-0 (2N5,3A6)
12 CD150 → 235-0 (2R5,3A6)

3F8 LMB160 02 1A
1G5 DMF161 03 1B
3F8 LMB170 05 2A
1H5 DMF171 06 2B
3F8 LMB180 11 3A
1H5 DMF181 10 3B
3F6 LMB190 14 4A
1H5 DMF191 13 4B
01
9G8 M00

15
07W 19-132 QUAD 2:1 MUX
A
04 CD160 → 107-1
07 CD170 → 207-1
09 CD180 → 108-1
12 CD190 → 208-1

STCDO

5E3 ST161 02 1A
5E3 ST171 03 1B
5E3 ST181 05 2A
5E3 ST191 06 2B
11 3A
10 3B
14 4A
13 4B
01

16
07T 19-132 QUAD 2:1 MUX
A
04 CD160 → 2H5,3D5
07 CD170 → 2H5,3D6
09 CD180 → 2H5,3D6
12 CD190 → 2J5,3D6

3K5 LMB200 02 1A
1J5 DMF201 03 1B
3K6 LMB210 05 2A
1J5 DMF211 06 2B
3K6 LMB220 11 3A
1K5 DMF221 10 3B
3K6 LMB230 14 4A
1K5 DMF231 13 4B
01
M00

15
07S 19-132 QUAD 2:1 MUX
A
04 CD 200 → 109-1
07 CD210 → 209-1
09 CD220 → 110-1
12 CD230 → 210-1

11C6 STCDO

5E3 ST201 02 1A
5E3 ST211 03 1B
5D3 ST221 05 2A
6D3 ST231 06 2B
11 3A
10 3B
14 4A
13 4B
01

15
07M 19-132 QUAD 2:1 MUX
A
04 CD200 → 2J5,3H5
07 CD210 → 2K6,3H6
09 CD220 → 2K5,3H6
12 CD230 → 2K6,3H6

3K8 LMB240 02 1A
1L5 DMF241 03 1B
3K9 LMB250 05 2A
1L5 DMF251 06 2B
3K9 LMB260 11 3A
1L5 DMF261 10 3B
3K9 LMB270 14 4A
1M5 DMF271 13 4B
01
M00

15
06W 19-132 QUAD 2:1 MUX
A
04 CD240 → 112-1
07 CD250 → 212-1
09 CD260 → 113-1
12 CD270 → 213-1

STCDO

5E3 ST241 02 1A
5E3 ST251 03 1B
5F3 ST261 05 2A
5F3 ST271 06 2B
11 3A
10 3B
14 4A
13 4B
01

15
06T 19-132 QUAD 2:1 MUX
A
04 CD240 → 2L5,3H8
07 CD250 → 2L5,3H9
09 CD260 → 2M5,3H9
12 CD270 → 2M5,3H9

3N8 LMB280 02 1A
1M5 DMF281 03 1B
3N9 LMB290 05 2A
1N5 DMF291 06 2B
3N9 LMB300 11 3A
1N5 DMF301 10 3B
3N9 LMB310 14 4A
1N5 DMF311 13 4B
01
M00

15
06S 19-132 QUAD 2:1 MUX
A
04 CD280 → 114-1
07 CD290 → 214-1
09 CD300 → 115-1
12 CD310 → 215-1

11C6 STCDO

5F3 ST281 02 1A
5F3 ST291 03 1B
5F3 ST301 05 2A
5N9 ST311 06 2B
11 3A
10 3B
14 4A
13 4B
01

15
06M 19-132 QUAD 2:1 MUX
A
04 CD280 → 2N5,3L8
07 CD290 → 2N5,3L9
09 CD300 → 2N5,3L9
12 CD310 → 2R5,3L9

NOTES

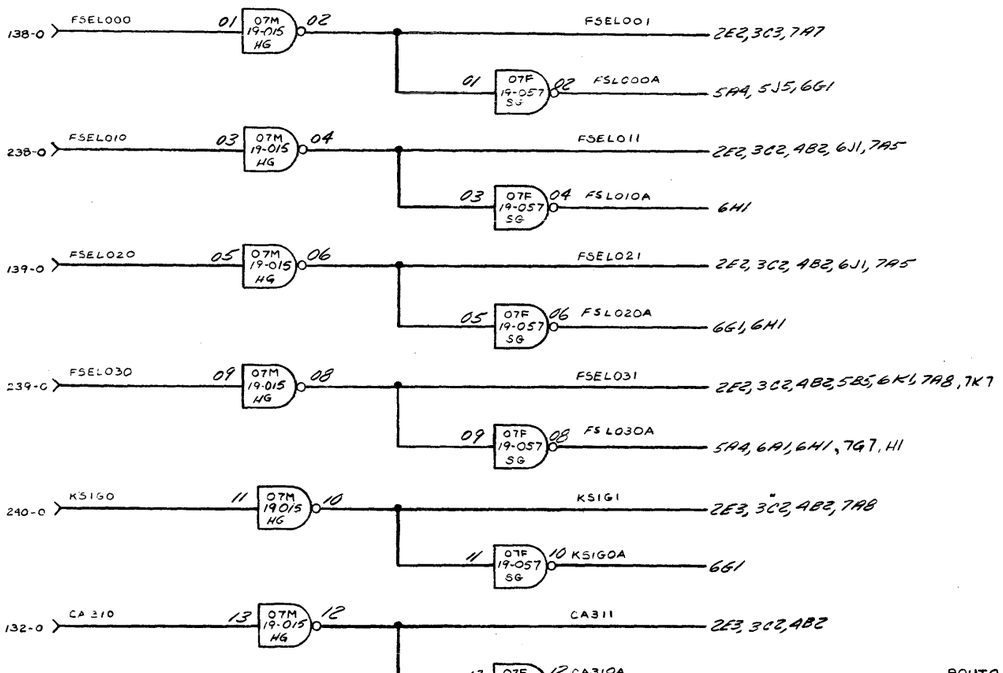
NAME	TITLE	DATE
TERRY PINGITORE	DRAFT	10-15-74
	CHK	
	ENGR	
	DIR ENG	

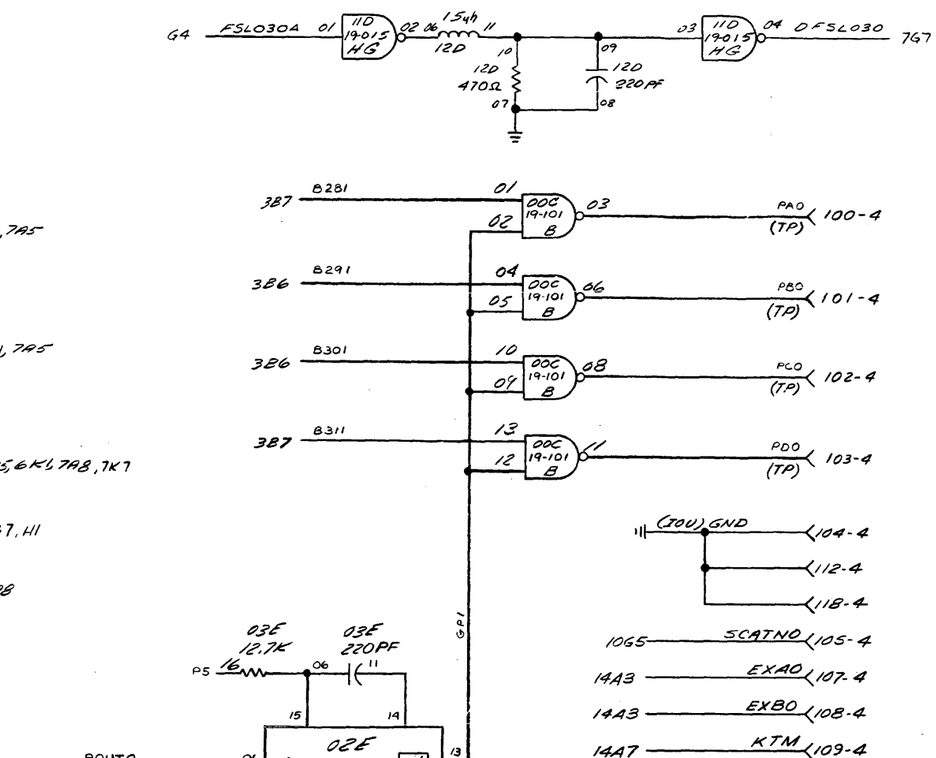
TITLE FUNCT. SCHEMATIC M 8/32 MBC

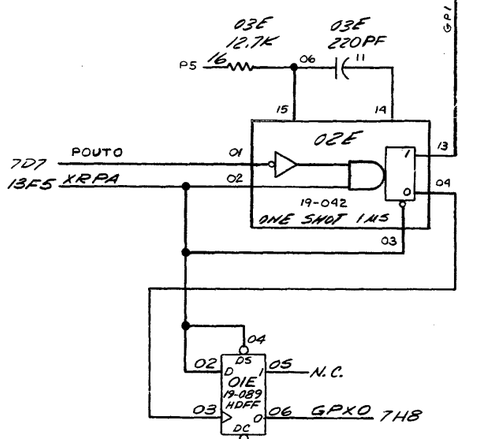
DWG NO 03088
SIZE A
SCALE NONE
35-535 R01 R08
SHEET 4 OF 14

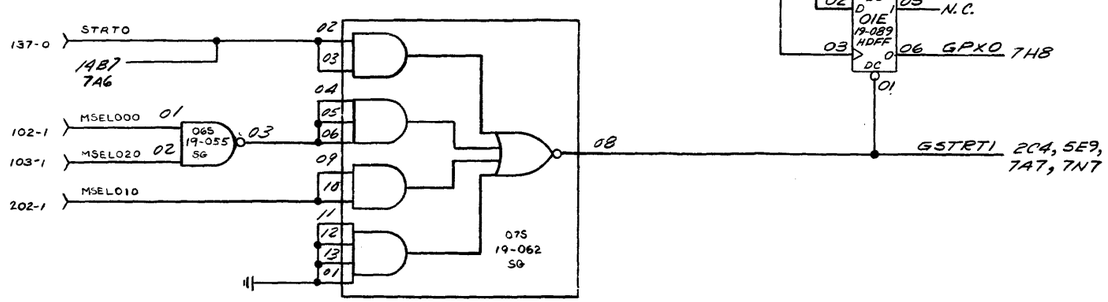
BRUNING 44-231 160-12

PERKIN-ELMER









REVISIONS

PRE PRODUCTION APPROVAL	DEV PROD	INIT	DATE
			11/1/74
			4/4/75

GATE 05H OUTPUT 8, CAP 220PF, RES 470, INDUCTOR MOVED TO SHT 7 DELETED GATE 01K OUTPUT 8,

GM	GJS	03088-18		12/4/74	R01

CHANGED PER MARKED PRINTS.

GM	GJS	03088-19		4/4/75	R02

ADDED 7N7 TO G5 FSEL030A, 7K7 WAS ADDED TO FSEL031, G4

GM	GJS	03088-23		4-8-75	R03

CHANGED: SHEETS 2 & 3.

GM	GJS	03088-32		4-14-75	R04

CHANGED: SHEET 5 WAS REV. 3. REV. OF BOARD WAS R05.

GM	GJS	03088-36		4-28-75	R05

CHANGED: SHT 3, 5, WAS R03.

GM	GJS	03088-38		4-21-75	R06

SHT 7 WAS R03

GM	GJS	03088-57		4-8-75	R07

ADDED 11D AT LOC J1 & M1 AND RESISTOR AT K1, CAP AT L1. CHANGED SHEETS 2 & 14 WERE R02 13 & 4 WERE R00, 3 & 7 WERE R04 & 15 WAS R03 13 WAS R01

GM	GJS	03088-65		4-15-75	R08

CHANGED, SHT 16 WAS R01, SHT 19 WAS R03 SHT 12 WAS R01

GM	GJS	03088-68		4-18-75	R09

07M WAS 19-057 REV LEV OF SHT 7 WAS R05

GM	GJS	03088-70		4-29-75	R10

REV LEV OF SHT 15 WAS 2 " " " " 14 WAS 4

GM	GJS	03088-75		5-2-75	R11

CHANGED: REV OF SHEET 14 WAS 5.

GM	GJS	03088-79	MB	5-9-75	R12

RELEASED FOR PRODUCTION — DATE 5/12/75

AREA N9 ADDED WAS 35-589 PER CHG SHT 3 REV 16.

GM	RC	2572	—	7-10-75	R13

REVISED SHT 2&6.

GM	RC	2570	—	8-25-75	R14

REVISED SHTS 1, 5 & 16. AREA J1 & M1, 11D WAS 19-062. AREA K1, 12D 06 - 11 15μh WAS 9.7μh, AREA L1, 12D 08-09 220 PF WAS 1000 PF. AREA R9, 35-539 R16 WAS R15.

GM	RC	2605	—	9-9-75	R15

REVISED SHTS 4, 6 & 9. REV LEV OF 35-539 WAS R16

WS	JB	2800	-	5-18-76	R16

REVISED SHTS 1 & 14. 35-539 WAS R17.

JC	JF	2752	-	7-14-76	R17

REVISED SHTS 1, 5 & 12. 35-539 REV LEV WAS R18

WS	JJ	3129	-	3-2-77	R18

REVISED SHTS 1, 2, 3, 5, 6, 7 & 9. 35-539 REV LEV WAS R19

WS	JJ	2980	-	3-22-77	R19

REVISED SHTS 1 & 6. 35-539 REV LEV WAS R20

WS		3195	-	5-16-77	R20

COUNT LOWER LEFT

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

8/32-10U	35-539E27

USED IN MANUAL 29-399

SHEET INDEX	REV	28	6	6	3	8	5	11		4	1			3	2	3	6	4
	SHT NO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

REVISIONS CONT.

REVISED SHT 14 35-539 REV LEVEL WAS R20

GP	VT	3531		3-16-78	R22
REVISED SHTS 5, 35-539 WAS R22.					
GP	VT	3787	M	10-11-78	R23
GP	VT	3267	M	10-12-11	R21
REVISED SHTS 2 & 7 35-539 WAS R23					
REVISED SHT 7. 35-539 WAS R21. MANUAL NO. ADDED	GP	VT	3799	M	10-11-78	R24

REVISIONS MADE TO SHT. 15	MQ	VT	3872	M	1-22-79	R25
REVISIONS TO SHTS. 9 & 16.	MQ	VT	3858	M	1-23-79	R26
REVISED SHTS 1, 7, 14, 15, & 16.	KR	VT	4231	R	3-10-80	R27
REVISED SHTS 1, 5, & 7	VT	VT	4543	MS	2-19-81	R28

NAME	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC
T. TREN	DRAFT	9-6-74	M8/32-10U
G. J. HOMEFIELD	CHK	10-15-74	
G. SYROVY	ENGR	11-1-74	
S. C. MESSINA	MGR		TASK NO. 03088
Z. A. BAKER			DWG NO. 35-539R28S008

SHEET OF 1 / 16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS				
ADDED SHEET COORDINATE IN AREA H5				
GM	GJJ	03088-18	16-12-74	R01
ADDED GATE AREA A5 19-055 IN 065.				
GM	GJJ	03088-32	1-14-75	R02
ROM # WAS 17089 F78				
GM	GJJ	03088-65	4-15-75	R03
AREA 8A, 8BN, 19-1323 INVERSION BUBBLES ON PINS 9, 7, 9, 8, 12 WERE NOT SHOWN				
GM	RC	2570	8-25-75	R04
03M-11 WAS NC AREA A7				
GM	7	2752	12-14-76	R05
AREA F6: DR31 WAS CROSS-REF TO GM9				
WS	JV	2980	3-3-77	R06

SELSHO A4

SELSHO 01 05M 19-057 SG 02

SELSHA

SELHO F1

SELHOB

FSEL001 IF2 01
FSEL011 IF2 02
FSEL021 IF3 03
FSEL031 IF4 04
KSIG1 IF4 07
CA311 IF5 06
HW1 5K3 05

OBL 19-142 F45 256X 4-BIT ROM

ME1 13
ME2 14

OUTPUTS 12 11 10 09

06J 19-126 5G → 08 ENSHA0
07J 19-126 5G → 08 ENSHB0
07J 19-126 5G → 06 ENSHC0

GSTRT1 IN8
DBEN1 6G5
TERM1 5N7

08J 19-057 5G → DBENO

07H 19-115 HA → STC1 3J3,7H9
07H 19-115 HA → STD1 3J3

065 19-055 5G

03J 1K MCR081 3H6
03J 1K MCR091 3H6

03M 19-132 QUAD 2:1 MUX
02M 19-132 QUAD 2:1 MUX
04M 19-132 QUAD 2:1 MUX
03K 19-132 QUAD 2:1 MUX
02K 19-132 QUAD 2:1 MUX
04K 19-132 QUAD 2:1 MUX

S200 119-1
S210 219-1
S220 120-1
S230 220-1
S160 117-1
S170 217-1
S180 118-1
S190 218-1

NOTES

BRUNING 44-231 16042

NAME	TITLE	DATE
C CUTLER	DRAFT	8-7-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32-10U

TASK NO. 03085
DWG NO. 35-539 RC6 008
SHEET OF 2-16

PERKIN ELMER

REVISIONS				
ADDED: NEW SHEET LOCATIONS IN AREA M2				
GM	G.JS	03088-18	4-12-74	R01
ADDED: I9-134 TO AREA D1				
GM	G.JS	03088-29	1-9-74	R02
ADDED: 19-057 GATE 08U, LOC E1				
GM	K.JS	03088-32	4-14-75	R03
ADDED: GATE 19-055 @ SHT LOC B1, BOARD LOC 14H. ROM # WAS 19-088F79				
GM	G.JS	03088-38	4-27-75	R04
AREA D1: DELETED GATES AT 12S. DELETED 1K RESISTOR AT 10S01/16. FOR PREV. REV INFO SEE VOIDED MI-FILM COPY 35-539 008, SHT 3, R05.				
GM	G.JS	03088-65	5-15-75	R05
WS	JV	2980	3-3-77	R06

14L9 FLSYN1 13 — 14H 19-055 SG — 11 GFLSYNO — 6K8
7K3 GSR1 12

5K3 HW1 05
1F5 CA311 06
1F4 KS1161 07
1F4A FSEL031 04
1F3 FSEL021 03
1F2 FSEL011 02
1F1 FSEL001 01
15
13 ME1
14 ME2

07K 19-142 FAG 4817 ROM

Y1 12 — 08J 19-057 SG — 10 SELSLIB H6
Y2 11 — 03 05H 19-057 SG — 04 SELSLIA AG6
Y3 10
Y4 09

2H5 STC1
2H4 STD1

06J 19-126 SG — 06 ENSLAO K9, 7E9
05J 19-126 SG — 08 ENSLBO L7, 7E9
05J 19-126 SG — 06 ENSLCO N7, G7, 7E9

A200 109-1 — 055 19-057 SG — 01
A210 209-1 — 03
A220 110-1 — 05
A230 210-1 — 09

B200 129-1 — 11
B280 134-1 — 13
B210 229-1 — 01
B290 234-1 — 03
B220 130-1 — 05
B300 135-1 — 09
B230 230-1 — 11
B310 235-1 — 13
A280 114-1 — 01
A290 219-1 — 03
A300 115-1 — 05
A310 215-1 — 09

A160 107-1 — 11
A170 207-1 — 13
A180 108-1 — 01
A190 208-1 — 03

B160 127-1 — 05
B240 132-1 — 09
B170 227-1 — 11
B250 232-1 — 13
B180 128-1 — 01
B260 133-1 — 03
B190 228-1 — 05
B270 233-1 — 09
A240 112-1 — 11
A250 212-1 — 13
A260 113-1 — 05
A270 213-1 — 09

A231 4K5
A221 4K4

B201 2C6, 4G3
B211 2D6, 4G3
B291 1J3, 2D6, 4B5, 7H2
B221 2D6, 4G3
B301 1J3, 2D6, 7H2, 8C1
B231 2D6, 4G3
B311 1J4, 2D6, 4B5, 7H1, 8C1 1J2 2C6, 4B5
B281

A281 2E6, 4B5
A291 2E6, 4B5
A301 2E6, 4A5
A311 2E6, 4A5

2K6, 4J2, 7D8 B161
2K6, 4J2 B171
2K6, 4K5 B251
2L6, 4J2 B181
2L6, 4A5 B261
2L6, 4J5 B191
7H2, 2K6, 4G5 B271
2K6, 4G5 B241

A241 2M6, 4C5
A251 2M6, 4C5
A261 2M6, 4C5
A271 2M6, 4C5

MCR121 7J5
MCR131 7G4
MCR141 7G4
MCR151 7G2
MCR081 2B5 A161
MCR091 2B5 A171
CAT N1 10M6 A181
MCR111 7H5 A191
DR121 6G9
DR131 6L9
DR141 6M9
DR151 6N9
DE081 6G9 A241
DE091 6G9 A251
DE101 6G9 A261
DE111 6G9 A271

SELSLIA F2
SELSLIB F1
ENSLCO M3
ENSLBO M2
ENSLAO M1

03T 19-132 QUAD 2:1 MUX
02T 19-132 QUAD 2:1 MUX
04T 19-132 QUAD 2:1 MUX
03S 19-132 QUAD 2:1 MUX
02S 19-132 QUAD 2:1 MUX
04S 19-132 QUAD 2:1 MUX

S280 124-1
S290 224-1
S300 125-1
S310 225-1
S240 122-1
S250 222-1
S260 123-1
S270 223-1

NOTES

NAME	TITLE	DATE
C.CUTLER	DRAFT	8-12-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32-10U

TASK NO. 03088
DWG NO. 35-539 R06 008
SHEET OF 3-16

BRUNING 44-231 16042

PERKIN ELMER

REVISIONS					
ROM # WAS 19-089 F00					
GM	VJS	03088-65	SS	4-16-75	R01
AREA R9: 19AM(21-025 F02) & RELATED CIRCUITRY WAS NOT SPEC'D.					
WS	VRA	2844	-	5-1276	R02
AREA C3: 08M-13874 WERE CONNECTED TO GROUND					
GP	WJ	3799	M	10-11-78	R03

514 KB1 — 05 A — Y1 12 GDHBHO
5K6 KA1 — 06 B
5K3 HW1 — 07 C
1F5 CA311 — 09 D — 08M 19-192 FA7 4 BIT ROM
1F4 KSIG1 — 03 E
1F4 FSEL031 — 02 F — Y2 11 GDLBHO
1F3 FSEL021 — 01 G
1F2 FSEL011 — 15 H — Y3 10 GDLBLO
7L8 MFINI — 13 ME1 — Y4 09 GDAO
14 ME2

3K6 B161, 3K6 B171, 3K6 B181, 3K7 B191 → 13S 19-134 HEX BUFF/INV (A) → D000 109-0, D010 209-0, D020 110-0, D030 210-0

3B6 B201, 3B6 B211, 3B6 B221, 3B6 B231 → 13T 19-134 HEX BUFF/INV (A) → D040 112-0, D050 212-0, D060 113-0, D070 213-0

3A6 A221, 3A6 A231 → 13T 19-13A (B)

A311 3G6, A301 3G6, A291 3G6, A281 3G6 → 11T 19-134 HEX BUF/INV (A)

A271 3R6, A261 3R6, A251 3R6, A241 3R6 → 11S 19-134 HEX BUFF/INV (A) → D110 215-0, D100 115-0, 13K 01 330 R5, 13K 02 330 P5

B311 3B7, B301 3B6 → 11T 19-134 (B)

B291 3B6, B281 3B7 → 11M 19-134 (B)

B271 3K7, B261 3R6, B251 3R6, B241 3K7 → 11M 19-134 HEX BUFF/INV (A) → D150 218-0, D140 118-0, D130 217-0, D120 117-0

B231, B221, B211, B201 → 11S 19-134 (B) → GNA, S7 D150 BN4, 11N4, 11N5; GNA, S7 D140 BN3, BN5, 11N5

B191, B181, B171, B161 → 11K 19-134 (B) → GNA BR5 BN4, S7, 11N4; GNA BR4 BN4, 11N4, S7

S7 GEA BR4 BN2, 11N2; S7, GEA BR3 BN2, 11N2; GEA BR2 BN2, 11N2, P8; GEA BR1 BN1, 11N2, P8 → 11K 19-134 HEX BUFF/INV (A) → D090 214-0, D080 114-0

P5
16
13M 330Ω
07 D070 6J4, 982
09 D060 6J4, 982
10 D050 6J4
11 D040 6H4
12 D030 6C4
13 D020 6C4
14 D010 6B4
15 D000 6B4
01 D150 G9
02 D140 H9
03 D130 H9
04 D120 J9
05 D110 J9
06 D100 J9
08 NC
21-025F03

K9 D090, K9 D080, NC
07 09 10 11 12 13 14 15 01 02 03 04 05 06 08
16
19M 470Ω
21-025F02

NOTES

NAME	TITLE	DATE
C. CUTLER	DRAFT	8-9-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
M8/32-IOU
TASK NO. 03088
DWG NO. 35-539 R03 008
SHEET OF 4 - 16

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
PRE PRODUCTION APPROVAL	DEV PROD	INIT	DATE Nov 5 1974
CHANGED: SHEETS 3, 4, & 5 WERE R00, REV.			
	03088-28		1-24-75 R01
ADDED: SHEETS 6-9; REF TO SHT 8 ON '4000' THRU 'A310' LEADS.			
	03088-39		1-27-75 R02
CHANGED: SHEETS 4 & 5 WERE R01 REV.			
	03088-41		1-27-75 R03
CHANGED: SHEETS 4 & 5 WERE R02 REV			
	03088-56		4-10-75 R04
RELEASED FOR PRODUCTION ENG. DATE 5/1/75			
REV LEV OF SHT 5 WAS R03 REV LEV OF DCS LOC 59 WAS R00, REV LEV OF CPC WAS R06			
	2506	–	5-27-75 R05
ENTIRE SHT, 19-077's INVERSION BUBBLES PIN 6, WAS NOT SPEC'D. REVISED SHTS 12, 6 & 7.			
	2570	–	8-25-75 R06
REVISED SHT. 8			
	2688	–	12-12-75 R07
REVISED SHTS 1 & 8 ADDED MANUAL REF. THIS SHT. AREA R7.			
	3587		5-23-78 R08
REVISED SHTS 1 & 5. AREA 59 35-555 WAS R08. 35-555 F01 WAS R04.			
	4279	MS	2-28-80 R09
REVISED SHTS 1, 2, 4, 5, 59. AREA A1 PSW261A W/LOCATOR 5N5 WAS PSW260A W/LOCATOR 5N6. AREA A2 PSW271A W/LOCATOR 5N7 WAS PSW270A W/LOCATOR 5N8.			
	4231	R	3-10-80 RID

4L7 AAD030
4L5 AAD040
4L1 AAD051
5N5 PSW261A
5N7 PSW271A
4L8 AAD020
4F6 AAD000
4F5 AAD010
4L3 ASTKNO
5H5 WCLK0A

3D1 SB001 — 00W 19-077 256-BIT MEM — 8H1 107-0 A000
3D1 SB011 — 00T 19-077 256-BIT MEM — 8H1 207-0 A010
3D2 SB021 — 00S 19-077 256-BIT MEM — 8H1 108-0 A020
3D2 SB031 — 00M 19-077 256-BIT MEM — 8H2 208-0 A030
3D3 SB041 — 00K 19-077 256-BIT MEM — 8H2 109-0 A040
3D4 SB051 — 00J 19-077 256-BIT MEM — 8H3 209-0 A050
3D4 SB061 — 01W 19-077 256-BIT MEM — 8H3 110-0 A060
3D4 SB071 — 01T 19-077 256-BIT MEM — 8H3 210-0 A070

3D5 SB081 — 01S 19-077 256-BIT MEM — 8H4 112-0 A080
3D6 SB091 — 01M 19-077 256-BIT MEM — 8H4 212-0 A090
3D6 SB101 — 01K 19-077 256-BIT MEM — 8H4 113-0 A100
3D6 SB111 — 01J 19-077 256-BIT MEM — 8H5 213-0 A110
3D7 SB121 — 03S 19-077 256-BIT MEM — 8H5 114-0 A120
3D8 SB131 — 03M 19-077 256-BIT MEM — 8H6 214-0 A130
3D8 SB141 — 04S 19-077 256-BIT MEM — 8H6 115-0 A140
3D8 SB151 — 04M 19-077 256-BIT MEM — 8H6 215-0 A150

3J1 SB161 — 08W 19-077 256-BIT MEM — 8K1 107-1 A160
3J1 SB171 — 08T 19-077 256-BIT MEM — 8K1 207-1 A170
3J2 SB181 — 08S 19-077 256-BIT MEM — 8K2 108-1 A180
3J2 SB191 — 08M 19-077 256-BIT MEM — 8K2 208-1 A190
3J3 SB201 — 08K 19-077 256-BIT MEM — 8K2 109-1 A200
3J4 SB211 — 09W 19-077 256-BIT MEM — 8K3 209-1 A210
3J4 SB221 — 09T 19-077 256-BIT MEM — 8K3 110-1 A220
3J4 SB231 — 09S 19-077 256-BIT MEM — 8K3 210-1 A230

3J5 SB241 — 09M 19-077 256-BIT MEM — 8K4 112-1 A240
3J6 SB251 — 09K 19-077 256-BIT MEM — 8K4 212-1 A250
3J6 SB261 — 10W 19-077 256-BIT MEM — 8K5 113-1 A260
3J6 SB271 — 10T 19-077 256-BIT MEM — 8K5 213-1 A270
3J7 SB281 — 10S 19-077 256-BIT MEM — 8K5 114-1 A280
3J8 SB291 — 10M 19-077 256-BIT MEM — 8K6 214-1 A290
3J8 SB301 — 10K 19-077 256-BIT MEM — 8K6 115-1 A300
3J8 SB311 — 11W 19-077 256-BIT MEM — 8K7 215-1 A310

USED IN MANUAL 29-394

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

8/32 CPC	35-555 R09
8/32 CPC/4 DCS	35-555 F01 R07

SHEET INDEX	REV	10	2	1	4	6	1	1	2	1
	SHT NO.	1	2	3	4	5	6	7	8	9

NOTES

NAME	TITLE	DATE
G. MELTON	DRAFT	10-15-74
G.J. HOMEFIELD	CHK	1-23-75
E. DEANGELO	ENGR	
R. BARKER	G.A.	
R.E. JONES	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC 8/32 CPC

TASK NO. 03088 — DWG NO. 35-555 R10 DCS — SHEET OF 1-9

BRUNING 44-231 16042

Computer Systems Division
Oceanport, N.J. 07757 S

REVISIONS

ENTIRE SHT. 19-077'S, INVERSION BUBBLE ON PIN 6, WAS NOT SPEC'D.				
V	LC	2570	—	8-25-75 R01
AREA A1 PSW261B WAS PSW260B. AREA A2 PSW271B WAS PSW270B AREA M9 LOCATOR 235-1 WAS 236-1.				
KR		4231	R	3-7-80 R02

4L8 BAD030
4L6 BAD040
4L2 BAD051
5N6 PSW261B
5N8 PSW271B
4F9 BAD020
4F8 BAD000
4F4 BAD010
4L4 BSTKN0
5H5 WCLK0

3D1 SB001 — 04K 19-077 256-BIT MEM — DATA IN / DATA OUT / ME1 / ME2 / ME3 / WE — 127-0 B000
3D1 SB011 — 05W 19-077 256 BIT MEM — 227-0 B010
3D2 SB021 — 05T 19-077 256 BIT MEM — 128-0 B020
3D2 SB031 — 05S 19-077 256 BIT MEM — 228-0 B030
3D3 SB041 — 05M 19-077 256 BIT MEM — 129-0 B040
3D4 SB051 — 05K 19-077 256 BIT MEM — 229-0 B050
3D4 SB061 — 06W 19-077 256 BIT MEM — 130-0 B060
3D4 SB071 — 06T 19-077 256 BIT MEM — 230-0 B070

3D5 SB081 — 06S 19-077 256 BIT MEM — 132-0 B080
3D6 SB091 — 06M 19-077 256 BIT MEM — 232-0 B090
3D6 SB101 — 06K 19-077 256 BIT MEM — 133-0 B100
3D6 SB111 — 07W 19-077 256 BIT MEM — 233-0 B110
3D7 SB121 — 07T 19-077 256 BIT MEM — 134-0 B120
3D8 SB131 — 07S 19-077 256 BIT MEM — 234-0 B130
3D8 SB141 — 07M 19-077 256 BIT MEM — 135-0 B140
3D8 SB151 — 07K 19-077 256BIT MEM — 235-0 B150

3J1 SB161 — 13S 19-077 256 BIT MEM — 127-1 B160
3J1 SB171 — 14W 19-077 256 BIT MEM — 227-1 B170
3J2 SB181 — 14T 19-077 256 BIT MEM — 128-1 B180
3J2 SB191 — 14S 19-077 256 BIT MEM — 228-1 B190
3J3 SB201 — 14M 19-077 256 BIT MEM — 129-1 B200
3J4 SB211 — 14K 19-077 256 BIT MEM — 229-1 B210
3J4 SB221 — 15W 19-077 256 BIT MEM — 130-1 B220
3J4 SB231 — 15T 19-077 256 BIT MEM — 230-1 B230

3J5 SB241 — 15S 19-077 256 BIT MEM — 132-1 B240
3J6 SB251 — 15M 19-077 256 BIT MEM — 232-1 B250
3J6 SB261 — 15K 19-077 256 BIT MEM — 133-1 B260
3J6 SB271 — 16W 19-077 256 BIT MEM — 233-1 B270
3J7 SB281 — 16T 19-077 256 BIT MEM — 134-1 B280
3J8 SB291 — 16S 19-077 256 BIT MEM — 234-1 B290
3J8 SB301 — 16M 19-077 256 BIT MEM — 135-1 B300
3J8 SB311 — 16K 19-077 256 BIT MEM — 235-1 B310

NOTES:

FUNCTIONAL SCHEMATIC
5/32 CPC
35-555702D08 2 9

PERKIN ELMER
Computer Systems Division
Oceanport, N J 07757

REVISIONS

CHANGED: MNEMONIC SCLK1 WAS BCLK1.				
G/H	JAN	03088-28	JS	1-23-78 R01

117-0 S000 04 1D 1Q 02 NC
1Q̄ 03 SB001 1C1, 2C1
217-0 S010 05 2D 03W 19-131 2Q 07 NC
2Q̄ 06 SB011 1E1, 2E1
118-0 S020 12 3D QUAD D FF 3Q 10 NC
3Q̄ 11 SB021 1F1, 2F1
218-0 S030 13 4D 4Q 15 NC
4Q̄ 14 SB031 1G1, 2G1
SW3 SCLK1 09 CLK
P5-16 10J 1K 01 CLR A

119-0 S040 04 03T 19-131 QUAD D FF 02 NC
03 SB041 1J1, 2J1
219-0 S050 05 07 NC
06 SB051 1K1, 2K1
120-0 S060 12 10 NC
11 SB061 1L1, 2L1
220-0 S070 13 15 NC
14 SB071 1N1, 2N1
09
01 A

122-0 S080 04 04W 19-131 QUAD D FF 02 NC
03 SB081 1C3, 2C3
222-0 S090 05 07 NC
06 SB091 1E3, 2E3
123-0 S100 12 10 NC
11 SB101 1F3, 2F3
223-0 S110 13 15 NC
14 SB111 1G3, 2G3
09
01 A

124-0 S120 04 04T 19-131 QUAD D FF 02 NC
03 SB121 1J3, 2J3
224-0 S130 05 07 NC
06 SB131 1K3, 2K3
125-0 S140 12 10 NC
11 SB141 1L3, 2L3
225-0 S150 13 15 NC
14 SB151 1N3, 2N3
09
01 A

117-1 S160 04 12W 19-131 QUAD D FF 02 NC
03 SB161 1C5, 2C5
217-1 S170 05 07 NC
06 SB171 1E5, 2E5
118-1 S180 12 10 NC
11 SB181 1F5, 2F5
218-1 S190 13 15 NC
14 SB191 1G5, 2G5
09
01 A

119-1 S200 04 12T 19-131 QUAD D FF 02 NC
03 SB201 1J5, 2J5
219-1 S210 05 07 NC
06 SB211 1K5, 2K5
120-1 S220 12 10 NC
11 SB221 1L5, 2L5
220-1 S230 13 15 NC
14 SB231 1N5, 2N5
09
01 A

122-1 S240 04 13W 19-131 QUAD D FF 02 NC
03 SB241 1C7, 2C7
222-1 S250 05 07 NC
06 SB251 1E7, 2E7
123-1 S260 12 10 NC
11 SB261 1F7, 2F7
223-1 S270 13 15 NC
14 SB271 1G7, 2G7
09
01 A

124-1 S280 04 13T 19-131 QUAD D FF 02 NC
03 SB281 1J7, 2J7
224-1 S290 05 07 NC
06 SB291 1K7, 2K7
125-1 S300 12 10 NC
11 SB301 1L7, 2L7
225-1 S310 13 15 NC
14 SB311 1N7, 2N7
09
01 A

P5 16 11M 1K

202-1 MSEL010
103-1 MSEL020
102-1 MSEL000 09 10U 19-057 SG 08

11K 19-116
06 I0
05 I1
04 I2
03 I3
01 STB1
02 SELB
14 SELA
15 STB2
10 O0
11 O1
12 O2
13 O3
INPUTS
OUTPUTS
1Y 07
2Y 09

02 D 05 Q 04 11M 19-063 T DC 03
M37X1 4A1
S37X1 4A2
M7X1 5G7
10 D 09 Q 12 11M 19-063 T DC 11
S7X1 5G6

111-3 SRCLK1
5G2 SCLR0A

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
8/32 CPC
TASK NO. 03088
DWG NO. 36-535 R01D08
SHEET OF 3-9

BRUNING 44-231 16042

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

CHANGED: MNEMONIC 'SODD091' WAS 'SSEL041'; ADDED: GATE @ SHT LOC B4-19-055 @ 03H; 19-126 @ 01H SHT LOC F4; DELETED: 2-33-035 SWITCHES @ 16A & 16B	G/11	03088-28	1-23-75	R01
ADDED: RES ON 'PSW251' LEAD, @ 11H, PINS 01 & 16.	G/11	03088-41	1-23-75	R02
WSELO WENT TO SL4 WSELIA, WSELOA & WSELI WENT TO SL3		03088 -56	4-10-75	R03
AREA L1 LOCATOR 1A1 WAS 2A1. AREA L2 LOCATOR 2A1 WAS 1A1. AREA E4 01H-09 & 01H-10 WERE REVERSED.	KR	4231	3-7-80	R04

NOTES

	NAME	DATE
DRAFT		
CHK		
ENGR		
DIR ENG		

TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC

TASK NO. 03088 DWG NO. 35-555 R04 D08 SHEET 4 OF 9

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
CHANGED: 18K10 WAS CONN TO 'M7X1 NET; 18K8 WAS CONN TO BK10 NET, DELETED: 19-057 GATE ON 'PCLK0' NET, ADDED: GATE @ LOC 12K 19-055; GATE @ LOC 10J 19-057; GATE @ LOC 08H 19-056.	G/N	MK	03088-28	1-23-75	R01
ADDED: 1K PULL-UP @ LOC 11H ON PSW260.	G/N	MK	03088-41	1-23-75	R02
DELETED IC 09H, 19057 ADDED 12J, 19-064	GM	GD	03088-56	4-10-75	R03
ADDED 08J IN LOC E8, 07H06 WENT TO 10N13 10J09 WENT TO 09N15, 07H05 WENT TO 07H09 & 07N13 07H04 WENT TO SCLR0A, 06H WAS SHOWN THUS					
AREA B8 10N15 WAS CONNECTED 10J01. 10H05 WAS CONNECTED TO 10J03 10H03 & 10H12 WERE N.C.	GM	MG	2506	–	5-27-75 R04
AREA N5 PSW261A WAS PSW260A. AREA N6 PSW 261B WAS PSW260B. AREA N7 PSW 271A WAS PSW270A. AREA N8 PSW 271B WAS PSW270B. AREA G7 PSW261 WAS PSW260. AREA G9 PSW 271 WAS PSW270.	KR	27	4231	R	3-10-80	R06

NOTES

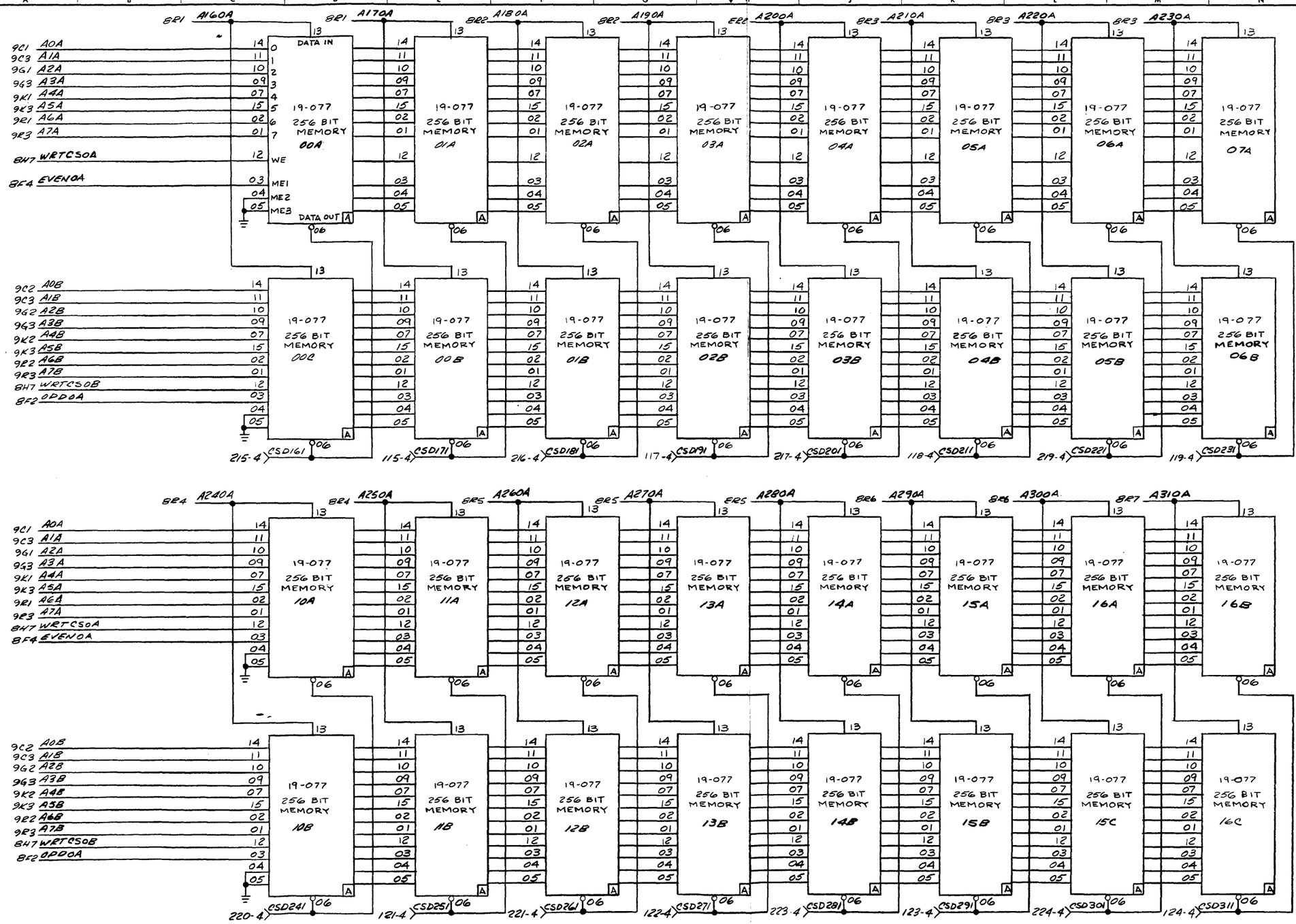
P. EDWARDS

FUNCTIONAL SCHEMATIC
8/32 CPC
03088
35-555-5706008
SHEET 5 OF 9

BRUNING 44 231 16042

Computer Systems Division
Oceanport, N J 07757

REVISIONS



SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

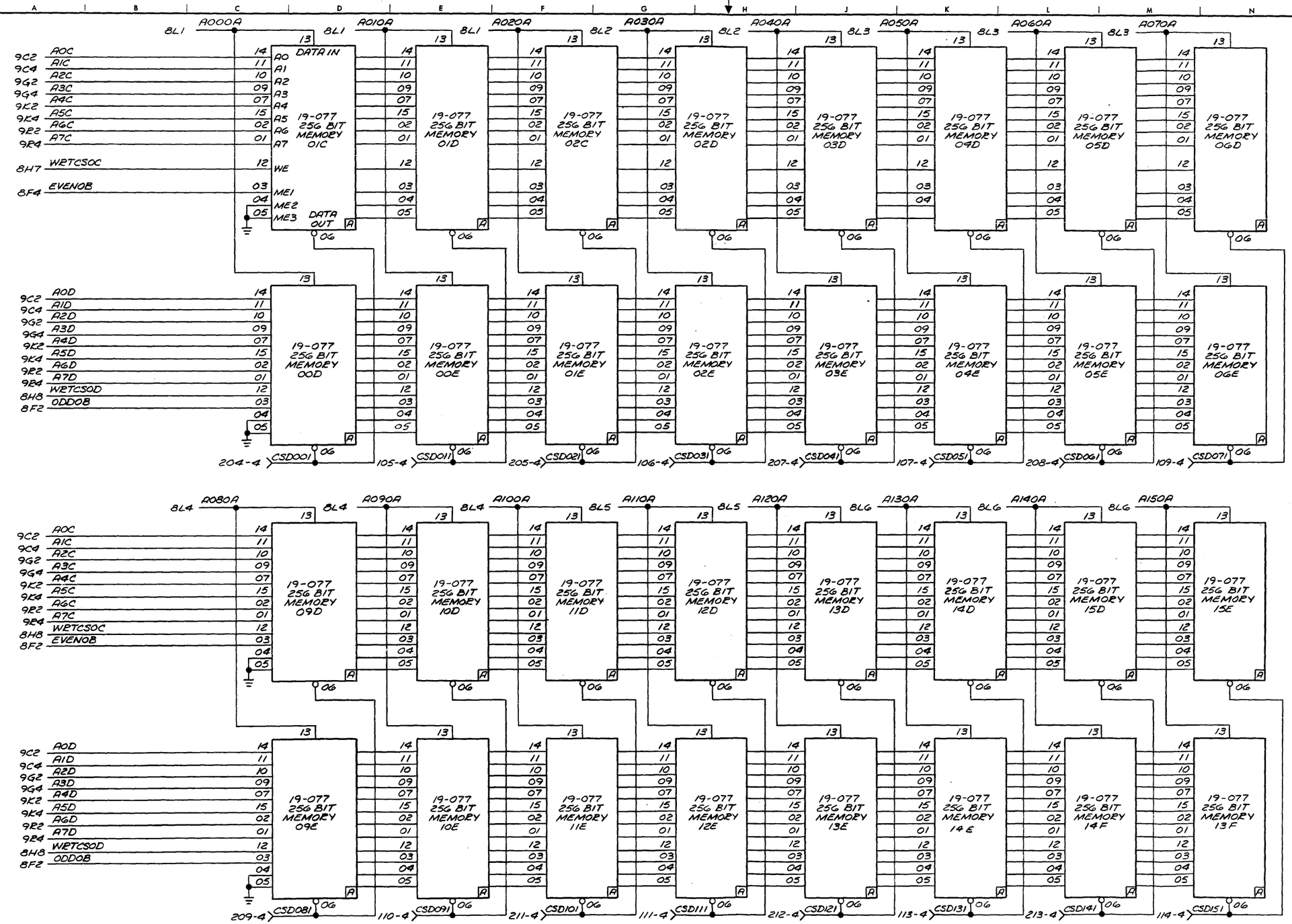
TITLE
FUNCTIONAL SCHEMATIC
M8/32 CPC
(DCS OPTION)

TASK NO. 03088
DWG NO. 35-555 D08
SHEET OF 6–9

BRUNING 44-231 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N J 07757

REVISIONS				
ENTIRE SHT 19-077'S INVERSION BUBBLE ON PIN 6 WAS NOT SPEC'D				
RC	2570	—	8-25-75	RDV



SCALE—

TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE
FUNCTIONAL SCHEMATIC
M8132 CPC
(DCS OPTION)

TASK NO. 03088
DWG NO. 35-555 B01 D08
SHEET OF 7 — 9

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
FOR PREVIOUS INFO. SEE VOIDED COPY 35-555 R00 D08
WS WA 2688 | - | 12-12-75 | R01
AREA C1-C4: STRAPPING OPTION BRACKET WAS NOT SPEC'D. AREA A9: NOTE 1 WAS NOT SPEC'D
GS WA 3587 | 5-23-78 | R02

SEE NOTE 1 FOR STRAPPING OPTION.

216-3 CSA040 → 09A 19-057 SG (05 → 06) → pin 25 → 21
116-3 CSA050 → 09A 19-057 SG (09 → 08) → pin 27 → 23
218-3 CSA060 → 09A 19-057 SG (11 → 10) → pin 29 → 46
117-3 CSA070 → 09A 19-057 SG (13 → 12) → pin 31 → 43
11A

21, 22, 23, 24 → 09B 19-060 SG (01, 02, 04, 05) → 06 → ODD0A → 6A4, 6A9
46, 45, 44, 43 → 08D 19-060 SG (01, 02, 04, 05) → 06 → ODD0B → 7A4, 7A9
21, 22, 23, 24 → 09B 19-060 SG (13, 12, 10, 09) → 08 → EVEN0A → 6A2, 6A6
46, 45, 44, 43 → 08D 19-060 SG (13, 12, 10, 09) → 08 → EVEN0B → 7A2, 7A6

5E3 PCLK0 → 12C 19-057 SG (13 → 12)

103-4 CSWP0 → 07B 19-057 SG (05 → 06) → 09C 19-130 5B (05, 01, 02, 04 → 06)

DELAY LINE 100 nS 30-018: 01, 08, 09, 10, 16; 02 → 15 NC; 03 → 10C → 04 → 13 NC; 07 → 40 → 100Ω → 29 → 11C

02, 01, 13 → 11C 19-059 5A → 12

01 → 07B 19-057 SG → 42 → WRTC50A → 6A2, 6A6
03 → 07B 19-057 SG → 04 → WRTC50B → 6A4, 6A8
01 → 08C 19-057 SG → 02 → WRTC50C → 7A2, 7A6
03 → 08C 19-057 SG → 04 → WRTC50D → 7A4, 7A8

1C3	A000	12S 19-057 SG	03C 19-057 SG	A000A	7C1	1C7	A160	02W 19-057 SG	04C 19-057 SG	A160A	6C1
1D3	A010	12S 19-057 SG	03C 19-057 SG	A010A	7D1	107	A170	02W 19-057 SG	04C 19-057 SG	A170A	6D1
1F3	A020	12S 19-057 SG	03C 19-057 SG	A020A	7F1	1F7	A180	02W 19-057 SG	04C 19-057 SG	A180A	6F1
8G3	A030	12S 19-057 SG	03C 19-057 SG	A030A	7G1	1G7	A190	02W 19-057 SG	04C 19-057 SG	A190A	6G1
1H3	A040	12S 19-057 SG	03C 19-057 SG	A040A	7H1	1H7	A200	02W 19-057 SG	07C 19-057 SG	A200A	6H1
1K3	A050	12S 19-057 SG	03C 19-057 SG	A050A	7J1	1K7	A210	02W 19-057 SG	07C 19-057 SG	A210A	6J1
1L3	A060	11T 19-057 SG	04C 19-057 SG	A060A	7L1	1L7	A220	02T 19-057 SG	07C 19-057 SG	A220A	6L1
1M3	A070	11T 19-057 SG	04C 19-057 SG	A070A	7M1	1M7	A230	02T 19-057 SG	07C 19-057 SG	A230A	6M1
1C5	A080	11T 19-057 SG	12C 19-057 SG	A080A	7C5	1C9	A240	02T 19-057 SG	13C 19-057 SG	A240A	6C5
1D5	A090	11T 19-057 SG	12C 19-057 SG	A090A	7D5	1D9	A250	02T 19-057 SG	13C 19-057 SG	A250A	6D5
1F5	A100	11T 19-057 SG	12C 19-057 SG	A100A	7F5	1F9	A260	02T 19-057 SG	13C 19-057 SG	A260A	6F5
1G5	A110	11T 19-057 SG	12C 19-057 SG	A110A	7G5	1G9	A270	02T 19-057 SG	14C 19-057 SG	A270A	6G5
1H5	A120	11S 19-057 SG	12C 19-057 SG	A120A	7H5	1H9	A280	02S 19-057 SG	14C 19-057 SG	A280A	6H5
1K5	A130	11S 19-057 SG	13C 19-057 SG	A130A	7J5	1K9	A290	02S 19-057 SG	14C 19-057 SG	A290A	6J5
1L5	A140	11S 19-057 SG	13C 19-057 SG	A140A	7L5	1L9	A300	02S 19-057 SG	14C 19-057 SG	A300A	6L5
1M5	A150	11S 19-057 SG	13C 19-057 SG	A150A	7M5	1M9	A310	02S 19-057 SG	14C 19-057 SG	A310A	6M5

NOTES:
1. STRAPPING ADDRESS X'800-9FF'
   21-25, 22-28, 23-30, 24-31,
   46-25, 45-28, 44-30, 43-32

SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE: FUNCTIONAL SCHEMATIC M8/32 CPC (DCS OPTION)
TASK NO. 03088
DWG NO. 35-555 R02 D08
SHEET 8 OF 9

BRUNING 44-231 24938

REVISIONS			
PRE PRODUCTION / PRODUCTION APPROVAL	DEV ENG	INIT	DATE
CHANGED: [illegible] PIN 3J WAS @ DTC, SELECTED: C-21-033 FROM PIN 4CM1A01 C1-C4 TO 4CM1A01 C1-C4 TO 4CM1A BOARD; 12-033 ENTS ALL BUT BDMS A,B,D,F 4K20 W 120,140,150,160 BET. USM # 117.			
ADDED: ALL CAPT ECC FOR FOI VERSION.			
CHANGED: ITEM 16 TO PAS IN PINS G1A14, G2A15.			
ADDED: ITEM 45 TO [illegible]			
RELEASED FOR PRODUCTION MFG ENG. DATE			
ITEM 23.106 11C WAS ITEM 23.106 18 EXCEPT 16 DELETED ITEM 36			
ITEM 114, ITEM 40, 41, 42 WAS NOT SPECIFIED			

00R

+C1 +C2 +C3 +C4

A B C D E F H J K M S T W

EQUIPPED FOR FOI VERSION

EQUIPPED FOR FOI VERSION

EQUIPPED FOR FOI VERSION

EQUIPPED FOR FOI VERSION

16R

+C5 +C6 +C7 +C8

49 TYP (CONTACTS CLOSEST TO THE EDGE OF BOARD SHOULD BE BENT INWARD PRIOR TO SOLDERING.)

1

3

VIEW B-B
TYP 6 PLACES

48 TYP(16) PLACES

50 TYPICAL 2 PLACES

11 TYPICAL 4 PLACES

4 TYP

5 TYP

2

2

39 TYP 8 PLACES

40 TYP ALL UNSPECIFIED

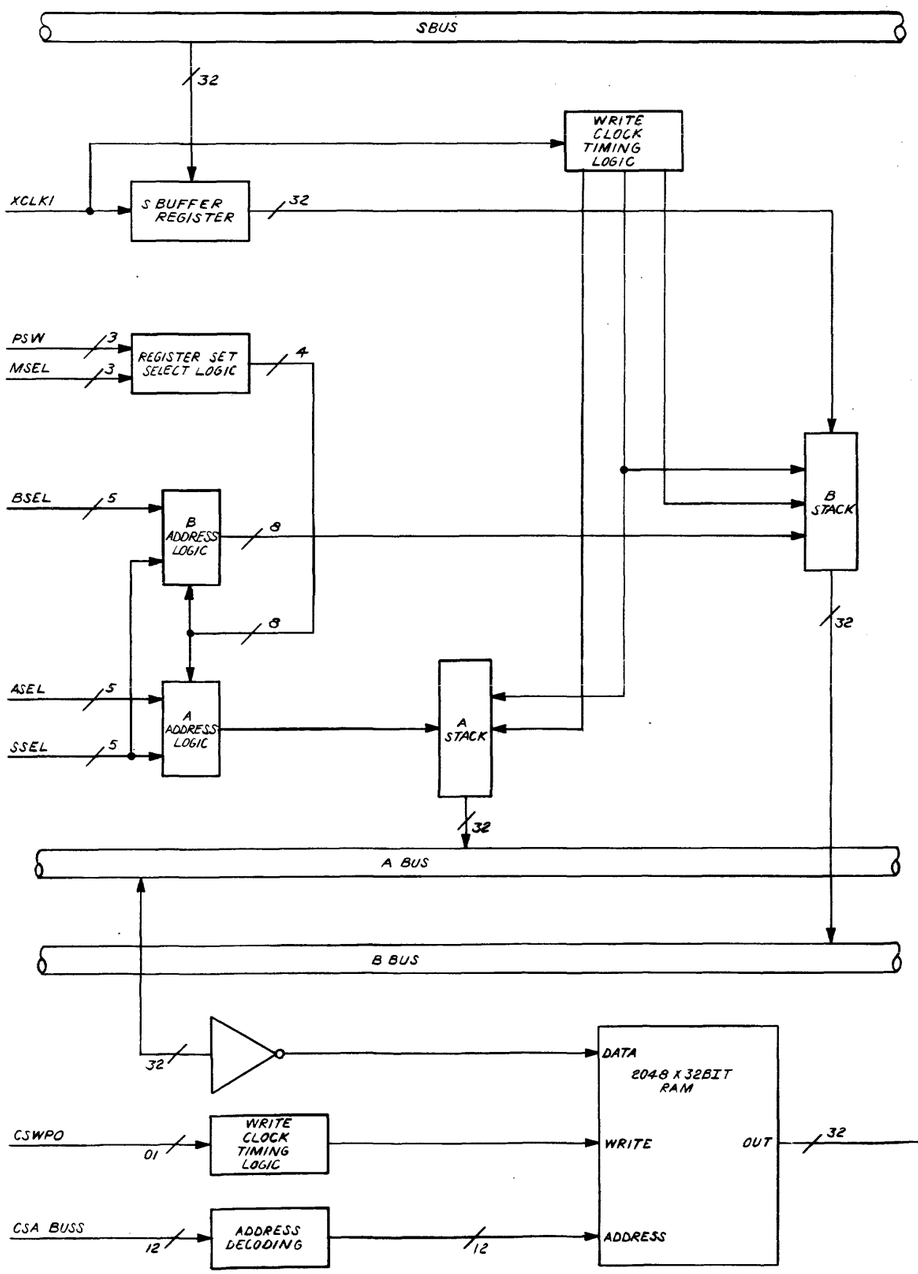
PARTIAL VIEW A-A
TYP 3 PLACES

COMPONENT	REF DESIGNATION

LIMPERT			TITLE	ASSEMBLY PRINTED CIRCUIT MOD 0/35 CPC
NOMEFIELD				
HAMER				
STAPLES				
MESSINA				

03082
335-555 206E03
SHEET 1 OF 1

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757



CONN	TERM. NO.	CABLE CONNECTOR MAP ROW 2	ROW 1	BACK PANEL MAP ROW 1	ROW 2	TERM. NO.	CONN
5	16			P5	P5	41	
	15			GRD		40	
	14					39	
	13					38	
	12					37	
	11			GRD	GRD	36	
	10			B300	B310	35	
	09			B280	B290	34	
	08			B260	B270	33	
	07			B240	B250	32	
	06					31	
	05			B220	B230	30	
	04			B200	B210	29	
	03			B180	B190	28	
	02			B160	B170	27	
	01			GRD	GRD	26	
	00			S300	S310	25	
				S280	S290	24	
				S260	S270	23	
4	24	CSD301	CSD311	S240	S250	22	1
	23	CSD281	CSD291			21	
	22	GRD	CSD271	S220	S230	20	
	21	CSD261	CSD251	S200	S210	19	
	20	CSD241	GRD	S180	S190	18	
	19	CSD221	CSD231	S160	S170	17	
	18	GRD	CSD211	GRD	GRD	16	
	17	CSD201	CSD191	A300	A310	15	
	16	CSD181	GRD	A280	A290	14	
	15	CSD161	CSD171	A260	A270	13	
	14	GRD	CSD151	A240	A250	12	
	13	CSD141	CSD131	GRD	GRD	11	
	12	CSD121	GRD	A220	A230	10	
	11	CSD101	CSD111	A200	A210	09	
	10	GRD	CSD091	A180	A190	08	
	09	CSD081	CSD071	A160	A170	07	
	08	CSD061	GRD	GRD	GRD	06	
	07	CSD041	CSD051			05	
	06	GRD	CSD031			04	
	05	CSD021	CSD011	MSEL020	RWC0	03	
	04	CSD001	GRD	MSEL000	MSEL010	02	
	03	GRD	CSWP0	GRD		01	
	02	GRD		P5	P5	00	
	01	GRD	GRD				
	00	GRD	GRD	P5	P5	41	
				GRD		40	
						39	
						38	
				STRT0		37	
3	24	GRD	GRD	GRD	GRD	36	0
	23	CSA140	GRD	B140	B150	35	
	22	CSA120	CSA150	B120	B130	34	
	21	GRD	CSA130	B100	B110	33	
	20	CSA100	CSA110	B080	B090	32	
	19	CSA080	GRD	GRD	GRD	31	
	18	CSA060	CSA090	B060	B070	30	
	17	GRD	CSA070	B040	B050	29	
	16	CSA040	CSA050	B020	B030	28	
	15	GRD	GRD	B000	B010	27	
	14	GRD	GRD	GRD	GRD	26	
	13	GRD	GRD	S140	S150	25	
	12	GRD	PCLK0	S120	S130	24	
	11	PSW251	SRCLK1	S100	S110	23	
	10	PSW261	PSW271	S080	S090	22	
	09	GRD	S2B0	GRD	GRD	21	
	08	ASEL031	ASEL041	S060	S070	20	
	07	ASEL011	ASEL021	S040	S050	19	
	06	GRD	ASEL001	S020	S030	18	
	05	BSEL031	BSEL041	S000	S010	17	
	04	BSEL011	BSEL021			16	
	03	GRD	BSEL001	A140	A150	15	
	02	SSEL031	SSEL041	A120	A130	14	
	01	SSEL011	SSEL021	A100	A110	13	
	00	GRD	SSEL001	A080	A090	12	
						11	
2				A060	A070	10	
				A040	A050	09	
				A020	A030	08	
				A000	A010	07	
				GRD	GRD	06	
				SCLR0		05	
						04	
						03	
						02	
				GRD		01	
				P5	P5	00	

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV EH	8/11/77
	PROD	

SHTS. 1-10 HAVE BEEN REVISED. WCS WAS DCS ON ALL SHTS. P5 FOR ROW 1 & 2 WERE ANTI SHORN PSW 261 WAS PSW 260 PSW 271 WAS PSW 270

BS	EH	ECR 3442	11-1-77	R01

RELEASED FOR PRODUCTION
PROJ. ENG. EH DATE 2/22/78

REVISED SHTS 1 & 6. AREA S9 35-663 WAS R01

KR		4279	MS	2-28-80 R02

35-663	R04
BOARD	REV LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

REVISION	2	1	1	1	2	1	1	1	1
SHEET	1	2	3	4	5	6	7	8	9	10

SCALE —

NAME	TITLE	DATE
C. MICHAELS	DRAFT	7/20/77
W. LIMPERT	CHK	7/29/77
B. HAGERMAN	ENGR	2/24/78
R.A. BARKER	Q.C.	2/24/78
N. LEMONDE	MGR.	2/24/78

TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC W/2K WCS

ASY NO 03898 SHEET OF 1 — 10

DWG NO 35-663 R02 D08

BRUNING 44-231 24538

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

RESISTOR PACK 111 IN AREA RB WAS NOT SHOWN. IN AREA A1 PSW126A WAS PSW 260A IN AREA A2 PSW 271A WAS PSW 270A			
BS	W.R.	CCP 3962	11-1-77	R01

4D1 SB001 — 5L7 AAD030, 5L5 AAD040, 5L1 AAD051, 6N6 PSW261A, 6N8 PSW271A, 5L8 AAD020, 5F6 AAD000, 5F5 AAD010, 5L3 ASTKNO, 6H5 WCLK0A; DATA IN; ME1, ME2, ME3; WE; DATA OUT; 00W 19-077 256-BIT MEM

4D1 SB011 — 00T 19-077 256-BIT MEM

4D2 SB021 — 005 19-077 256-BIT MEM

4D2 SB031 — 00M 19-077 256-BIT MEM

4D3 SB041 — 00K 19-077 256-BIT MEM

4D4 SB051 — 00J 19-077 256-BIT MEM

4D4 SB061 — 01W 19-077 256-BIT MEM

4D4 SB071 — 01T 19-077 256-BIT MEM

9H1 A000 (107-0) 06; 9H1 A010 (207-0) 06; 9H1 A020 (108-0) 06; 9H2 A030 (208-0) 06; 9H2 A040 (109-0) 06; 9H3 A050 (209-0) 06; 9H3 A060 (110-0) 06; 9H3 A070 (210-0) 06

4D5 SB081 — 015 19-077 256-BIT MEM

4D6 SB091 — 01M 19-077 256-BIT MEM

4D6 SB101 — 01K 19-077 256-BIT MEM

4D6 SB111 — 01J 19-077 256-BIT MEM

4D7 SB121 — 035 19-077 256-BIT MEM

4D8 SB131 — 03M 19-077 256-BIT MEM

4D8 SB141 — 045 19-077 256-BIT MEM

4D8 SB151 — 04M 19-077 256-BIT MEM

9H4 A080 (112-0) 06; 9H4 A090 (212-0) 06; 9H4 A100 (113-0) 06; 9H5 A110 (213-0) 06; 9H5 A120 (114-0) 06; 9H6 A130 (214-0) 06; 9H6 A140 (115-0) 06; 9H6 A150 (215-0) 06

4J1 SB161 — 08W 19-077 256-BIT MEM

4J1 SB171 — 08T 19-077 256-BIT MEM

4J2 SB181 — 085 19-077 256-BIT MEM

4J2 SB191 — 08M 19-077 256-BIT MEM

4J3 SB201 — 08K 19-077 256-BIT MEM

4J4 SB211 — 09W 19-077 256-BIT MEM

4J4 SB221 — 09T 19-077 256-BIT MEM

4J4 SB231 — 095 19-077 256-BIT MEM

9K1 A160 (107-1) 06; 9K1 A170 (207-1) 06; 9K2 A180 (108-1) 06; 9K2 A190 (208-1) 06; 9K2 A200 (109-1) 06; 9K3 A210 (209-1) 06; 9K3 A220 (110-1) 06; 9K3 A230 (210-1) 06

4J5 SB241 — 09M 19-077 256-BIT MEM

4J6 SB251 — 09K 19-077 256-BIT MEM

4J6 SB261 — 10W 19-077 256-BIT MEM

4J6 SB271 — 10T 19-077 256-BIT MEM

4J7 SB281 — 105 19-077 256-BIT MEM

4J8 SB291 — 10M 19-077 256-BIT MEM

4J8 SB301 — 10K 19-077 256-BIT MEM

4J8 SB311 — 11W 19-077 256-BIT MEM

11J 21-025 F03 RESISTOR MODULES — 08 N.C., 13 N.C., 14 NC, 15 NC, 16 PS; 180Ω 1/8W

9K4 A240 (112-1) 06; 9K4 A250 (212-1) 06; 9K5 A260 (113-1) 06; 9K5 A270 (213-1) 06; 9K5 A280 (114-1) 06; 9K6 A290 (214-1) 06; 9K6 A300 (115-1) 06; 9K7 A310 (215-1) 06

NOTES

	NAME	TITLE	DATE
DRAFT	P.CARD	DRAFT	7-8-77
CHK		CHK	
ENGR		ENGR	
DIR ENG		DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC W/2K WCS

TASK NO. 7-298 | SHEET OF 2-10

DWG NO. 35-663R01 D09

BRUNING 44 231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

RESISTOR PACK 16J IN AREA BB WAS NOT SHOWN. IN AREA AJ PSW26JB WAS PSW 26JB. IN AREA BE PSW27JB WAS PSW 27JB.			
BS	WM	ECR 3442	11-1-77	B01

4D1 SB001 — DATA IN; 04K 19-077 256-BIT MEM; ME1 ME2 ME3; WE; DATA OUT
5L8 BAD030
5L6 BAD040
5L2 BAD051
6N5 PSW26JB
6N7 PSW27JB
5F9 BAD020
5F8 BAD000
5F4 BAD010
5L4 BSTKNO
6H5 WCLKO

4D1 SB011 — 05W 19-077 256 BIT MEM — 127-0 B000
4D2 SB021 — 05T 19-077 256 BIT MEM — 227-0 B010
4D2 SB031 — 05S 19-077 256 BIT MEM — 128-0 B020
4D3 SB041 — 05M 19-077 256 BIT MEM — 228-0 B030
4D4 SB051 — 05K 19-077 256 BIT MEM — 129-0 B040
4D4 SB061 — 06W 19-077 256 BIT MEM — 229-0 B050
4D4 SB071 — 06T 19-077 256 BIT MEM — 130-0 B060
4D5 SB081 — 06S 19-077 256 BIT MEM — 230-0 B070
4D6 SB091 — 06M 19-077 256 BIT MEM — 132-0 B080
4D6 SB101 — 06K 19-077 256 BIT MEM — 232-0 B090
4D6 SB111 — 07W 19-077 256 BIT MEM — 133-0 B100
4D7 SB121 — 07T 19-077 256 BIT MEM — 233-0 B110
4D8 SB131 — 07S 19-077 256 BIT MEM — 134-0 B120
4D8 SB141 — 07M 19-077 256 BIT MEM — 234-0 B130
4D8 SB151 — 07K 19-077 256 BIT MEM — 135-0 B140
4J1 SB161 — 13S 19-077 256 BIT MEM — 235-0 B150
4J1 SB171 — 14W 19-077 256 BIT MEM — 127-1 B160
4J2 SB181 — 14T 19-077 256 BIT MEM — 227-1 B170
4J2 SB191 — 14S 19-077 256 BIT MEM — 128-1 B180
4J3 SB201 — 14M 19-077 256 BIT MEM — 228-1 B190
4J4 SB211 — 14K 19-077 256 BIT MEM — 129-1 B200
4J4 SB221 — 15W 19-077 256 BIT MEM — 229-1 B210
4J4 SB231 — 15T 19-077 256 BIT MEM — 130-1 B220
4J5 SB241 — 15S 19-077 256 BIT MEM — 230-1 B230
4J6 SB251 — 15M 19-077 256 BIT MEM — 132-1 B240
4J6 SB261 — 15K 19-077 256 BIT MEM — 232-1 B250
4J6 SB271 — 16W 19-077 256 BIT MEM — 133-1 B260
4J7 SB281 — 16T 19-077 256 BIT MEM — 233-1 B270
4J8 SB291 — 16S 19-077 256 BIT MEM — 134-1 B280
4J8 SB301 — 16M 19-077 256 BIT MEM — 234-1 B290
4J8 SB311 — 16K 19-077 256 BIT MEM — 135-1 B300
16J 21-025 F03 RESISTOR MODULE — 235-1 B310

09 07 06 05 04 12 02 01 03 11 10 — 08 NC; 13 NC; 14 NC; 15 NC; 16 P5
100Ω 1/4W ×9 to +08

P. CARD		7/8/77	FUNCTIONAL SCHEMATIC 8/32 CPC W12K WCS
			03898
			35-663R01 D08

SHEET OF 3-10

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA M7 PIN 11 FOR IC 11K WAS NOT SHOWN				
LTR	BY	REF DWG	DATE	ECO
A			11-1-77	E01

03W 19-131 QUAD D FF

117-0 S000	04	1D	1Q
			1Q̄
217-0 S010	05	2D	2Q
			2Q̄
118-0 S020	12	3D	3Q
			3Q̄
218-0 S030	13	4D	4Q
			4Q̄
6U3 SCLK1	09	CLK	
P5 16 2 10J 1K	01	CLR	

02	NC
03	SB001 2C1, 3C1
07	NC
06	SB011 2E1, 3E1
10	NC
11	SB021 2F1, 3F1
15	NC
14	SB031 2G1, 3G1

03T 19-131 QUAD D FF

119-0 S040	04	1D	1Q
219-0 S050	05	2D	2Q
120-0 S060	12	3D	3Q
220-0 S070	13	4D	4Q
	09	CLK	
	01	CLR	

02	NC
03	SB041 2J1, 3J1
07	NC
06	SB051 2K1, 3K1
10	NC
11	SB061 2L1, 3L1
15	NC
14	SB071 2N1, 3N1

04W 19-131 QUAD D FF

122-0 S080	04	1D	1Q
222-0 S090	05	2D	2Q
123-0 S100	12	3D	3Q
223-0 S110	13	4D	4Q
	09	CLK	
	01	CLR	

02	NC
03	SB081 2C3, 3C3
07	NC
06	SB091 2E3, 3E3
10	NC
11	SB101 2F3, 3F3
15	NC
14	SB111 2G3, 3G3

04T 19-131 QUAD D FF

124-0 S120	04	1D	1Q
224-0 S130	05	2D	2Q
125-0 S140	12	3D	3Q
225-0 S150	13	4D	4Q
	09	CLK	
	01	CLR	

02	NC
03	SB121 2J3, 3J3
07	NC
06	SB131 2K3, 3K3
10	NC
11	SB141 2L3, 3L3
15	NC
14	SB151 2N3, 3N3

12W 19-131 QUAD D FF

117-1 S160	04	1D	1Q
217-1 S170	05	2D	2Q
118-1 S180	12	3D	3Q
218-1 S190	13	4D	4Q
	09	CLK	
	01	CLR	

02	NC
03	SB161 2C5, 3C5
07	NC
06	SB171 2E5, 3E5
10	NC
11	SB181 2F5, 3F5
15	NC
14	SB191 2G5, 3G5

12T 19-131 QUAD D FF

119-1 S200	04	1D	1Q
219-1 S210	05	2D	2Q
120-1 S220	12	3D	3Q
220-1 S230	13	4D	4Q
	09	CLK	
	01	CLR	

02	NC
03	SB201 2J5, 3J5
07	NC
06	SB211 2K5, 3K5
10	NC
11	SB221 2L5, 3L5
15	NC
14	SB231 2N5, 3N5

13W 19-131 QUAD D FF

122-1 S240	04	1D	1Q
222-1 S250	05	2D	2Q
123-1 S260	12	3D	3Q
223-1 S270	13	4D	4Q
	09	CLK	
	01	CLR	

02	NC
03	SB241 2C7, 3C7
07	NC
06	SB251 2E7, 3E7
10	NC
11	SB261 2F7, 3F7
15	NC
14	SB271 2G7, 3G7

13T 19-131 QUAD D FF

124-1 S280	04	1D	1Q
224-1 S290	05	2D	2Q
125-1 S300	12	3D	3Q
225-1 S310	13	4D	4Q
	09	CLK	
	01	CLR	

02	NC
03	SB281 2J7, 3J7
07	NC
06	SB291 2K7, 3K7
10	NC
11	SB301 2L7, 3L7
15	NC
14	SB311 2N7, 3N7

P5 16 11M 1K 1

11K 19-116

202-1 MSELO10	06	0	1Y 07
103-1 MSELO20	05	1	
	04	2	
	03	3	
	01	STB1	
	02	SELB	
	14	SELA	
	15	STB2	
102-1 MSELO00 09 10J 19-057 SG 08	10	0	2Y 09
	11	1	
	12	2	
	13	3	

INPUTS / OUTPUTS

11M 19-063 (DS, DC)

02	M37X1 5A1
05	S37X1 5A2
09	M7X1 6G7
12	S7X1 6G6

111-3 SRCLK1
6G2 SCLR0A

NOTES

BRUNING 44-231 16042

NAME	TITLE	DATE
P. CARD	DRAFT	7/8/77
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC 8/32 CPC W/12K WCS

TASK NO. 03898 | DWG NO. 35-663R01 D08 | SHEET OF 4-10

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
DESIGNATION FOR AADOS1 WAS 3A1. DESIGNATION FOR BADOS1 WAS 2A1				
BS	BW	ECP 3462	11-1-77	BD1

455 M37X1
106-3 ASELOO1
103-3 BSELOO1
456 S37X1
100-3 SSELOO1
201-3 SSELO11
207-3 ASELO11
109-3 S2B0
6H3 WSELI
204-3 BSELO11
6H4 WSELO
6H3 WSELIA
6H3 WSELOA
104-3 BSELO21
101-3 SSELO21
211-3 PSW251
P5 16 07C 01 1K
11H 1K 01
03J 19-126 SG
03H 19-055 SG
04J 19-057 SG
05J 19-059 SA
01H 19-126 SG
02K 19-126 SG
02M 19-126 SG
02J 19-062 SG
05H 19-062 SG
BADO10 3A2
AADO10 2A2
AADOOO 2A2
BADOOO 3A2
BADO20 3A2
AADO20 2A2

6G8 AKLO
6H4 WSELO
6H3 WSELIA
6G9 BKLO
6H3 WSELOA
6H3 WSELI
6B3 SSELXO
02H 19-126 SG
03K 19-126 SG
AADOS1 2A1
BADOS1 3A1
SKLO 6G8
ASTKNO 2A2
BSTKNO 3A2
6D3 DWCO
108-3 ASELO41
6L1 SODDO41
105-3 BSELO41
208-3 ASELO31
202-3 SSELO31
205-3 BSELO31
107-3 ASELO21
04H 19-062 SG
00H 19-126 SG
01H 19-126 SG
02K 19-126 SG
AADO40 2A1
BADO40 3A1
AADO30 2A1
BADO30 3A1
AADO20 2A2

P CARD 7/8/77

FUNCTIONAL SCHEMATIC
8/32 CPC
W/2K WCS
C3898
35 443R01 DOB 5-10

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

IN AREA 6G PSW26.1 WAS PSW26.0			
IN AREA 5G PSW27.1 WAS PSW27.0			
IN AREA 10H5 PSW26.1B WAS PSW26.0B			
IN AREA 11H6 PSW26.1B WAS PSW26.0B			
IN AREA 11H3 PSW27.1A WAS PSW27.0A			
IN AREA 11H8 PSW27.1B WAS PSW27.0B			
JPS	A	9462	11-1-77	R01
AREA B8 10H15 WAS CONNECTED TO 10J01. 10H05 WAS CONNECTED TO 10J03. 10H03 & 10H12 WERE N.C.				
KR	A	9279	MS	2-28-80	R02

08J 01 1K 16 P5

H5 WCLKO

105-0 SCLRO

SCLROA 4M8

102-3 SSELO41

30DD041 5G5

SOLK1 4A2

WSELIA 5A5, 5G1

WSELOA 5A5, 5G1

H4 WSELO

5G5 SSELKO

WSELO 83, 5A5, 5G1

137-0 STRTO

DWCO 5G5

112-3 PCLKO

9A5 U3

WSELI 05 WSELI D4, 5A4, 5G2

F3 PCLKO

H3 WSELI

WCLKO D1, 3A3

WCLKOA 2A3

P5 16 07H 01 1K

19-118 ENB

N.C. 02 I0 Z0 03
N.C. 05 I1 Z1 06 N.C.
N.C. 11 I2 Z2 10 N.C.
N.C. 14 I3 Z3 13 N.C.
06H XCEIVER
B0 B1 B2 B3
01 14 12 15
N.C. N.C. N.C.

203-1 RWCO

P5W26.1A 2C1

P5W26.1B 3C1

P5W27.1A 2C1

P5W27.1B 3C1

457 S7X1

457 M7X1

210-3 PSW26.1

P5 11H 15 1K 02

5G1 AKLO

5K3 SKLO

5G2 BKLO

110-3 PSW27.1

10H 30-018 DELAY LINE 100 ns

11H 100 Ω

P. CARD

7/8/77 FUNCTIONAL SCHEMATIC
W/ZN WCS
3828
35-662-FR-2 DOS 6-10

BRUNING A4 231-1042

REVISIONS

NO	PRODUCTION APPROVAL	DESCRIPTION	DATE
		RELEASED	7-22-77
		RELEASED BETWEEN SEQ-001 SEQ-49 AND SEQ-001 / 111-18 WERE ADDED. REVISED PARTS 16 / 111 WERE ADDED. REVISED BETWEEN 16-49 / 16-49 WAS LABELED AT	11-8-77

SEE NOTE 1

SEE NOTE 2

.530 MAX
.062 REF.
.125 MAX.

PARTIAL VIEW A-A
TYP 3 PLACES

NOTES:
1. HEADER STIFFENER (ITEM 3) TO BE SOLDERED TO GND BUS AT 2 ENDS AND CENTER (ASPP SIDE).
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

4 TYP 2 PLACES

3 TYP 4 PLACES

33 TYP 8 PLACES

34 TYP ALL UNSPECIFIED

COMPONENT	REF DESIGNATION

NAME	TITLE	DATE
V. HELVATY	DRAFT	7-28-77
W. LAMBERT	CHK	8-3-77
J. VAN DE HEUVEL	ENGR	
C. R. BARKER	QA	
A. ARMOUR	MGR	

TITLE ASSEMBLY
MULTI-WIRE 8/32 CPC W/ER DCS

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