PERKIN-ELMER

MODEL 3230 PROCESSOR

Installation and Maintenance Manual

47-004 R21

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PREFACE

This manual provides the technician with information necessary to install, operate, and maintain the Model 3230 Digital System.

Chapter 1 is an installation guide that covers unpacking, staging hardware and cabling, initial power-up checkout, and on-line testing information. Chapter 2 provides unpacking procedures and general configurations for the Perkin-Elmer 3230. Chapter 3 contains descriptions and figures of mechanical components, cooling facilities, and electrical plugs and receptacles required for the Perkin-Elmer 3230. Chapter 4 contains general information for the 34-038 Power Subsystem. Chapter 5 provides installation and operation procedures for the System Control Panel. The remaining chapters include Processor and Memory Board Installation, Block Diagram Analyses, and a Microword Description. Also described are the functions of the CPU-A, CPU-B, CPU-C, CPU-D, LBC, and STM boards. Adjusting and Troubleshooting procedures, Test Aid Data, High Speed Data Handling, Hardware Documentation, Microcode and Bootloader listings are included.

Revision 21 includes revisions 20 and 21 and contains the following changes:

- revised filter maintenance procedure
- revised microprogram listing

CHAPTER 1
PROCESSOR INSTALLATION GUIDE

1.1 STAGING NEW HARDWARE

1. Unpack equipment and inspect for damage.

2. The Basic 3230 Processor is housed in one rack which contains a processor chassis, an I/O expansion chassis, a blower cooling system, an AC power distribution system, and a DC power system. (Battery Backup).

3. Refer to the 34-038 Power Subsystem Installation and Maintenance Manual, Publication Number 47-010, for AC power connection and requirements.

4. Install the processor rack in the space allocated and connect the power cable with the AC distribution panel circuit breaker off.

5. Adjust the permanent leveling legs to the racks to prevent rack rollers from moving the rack. The cabling between the processor and I/O peripherals are interfaced between the cable convenience panel and the applicable I/O device.

1.2 MODEL 550 VDU STAGING AND CABLING

1. Carefully check the VDU for mechanical shipping damage.

2. Install the VDU in the space provided.

3. Install the signal cable, 17-272F01, from the VDU to the cable convenience panel.

4. With the power switch in the OFF position, install the power cord into the customer's power receptacle.

1.3 INITIAL POWER-UP

1. Prior to initial power-up of the processor, ensure that all printed circuit boards are securely seated and all cables are securely fastened.

2. Turn on the AC distribution panel circuit breaker and power up the processor. Check the voltages for proper settings on all chassis.

1.4 FINAL ON-LINE TESTING

To test the system's on-line capabilities, run the following multimedia diagnostics that apply to the configuration:

06-230R01 Perkin-Elmer 3200 Basic Confidence Test
06-228R02 Perkin-Elmer 3200 Processor Test Part 1
06-229R02 Perkin-Elmer 3200 Processor Test Part 2
06-236R02 Perkin-Elmer 3200 Memory Test
06-238R00 Perkin-Elmer 3200 Commercial Instruction Test
06-235R02 Perkin-Elmer 3200 MAT/CACHE Test
06-243R01 Model 550 VDU Test
06-127R09 PALS Off-Line Test
06-159R07 Perkin-Elmer 3200 System Exerciser
06-133R09 Common Universal Clock Test Program
06-246R01 Error Logger Test
06-161R06 Perkin-Elmer 3200 SELCH Test

NOTE

Test programs must be at revision level indicated or higher.

Refer to the appropriate maintenance manuals if problems are encountered.

1.5 TEST EQUIPMENT

C.E tool kit
Extender board
Oscilloscope
Extender board ribbon cables (shielded)
Model 3220 Test Aid
Perkin-Elmer 3200 backpanel extender

SYSTEM INSTALLATION
CHECKLIST

Customer_____ Date Started_____

	INITIAL
Staging Hardware and Cabling	_____
Initial Power-up Checkout	_____
Final Testing W/MMD	_____
Customer OS Running	_____

NOTES:

Date Completed_____

Installation C.E._____

Figure 1-1 System Installation Checklist

CHAPTER 2
INTRODUCTION

2.1 GENERAL INFORMATION

The Model 3230 Processor features a highly modular structure that permits configuration to the user's exact processing requirements. The system can be configured for convenient expansion as the user's requirements grow. Circuit descriptions are provided in the appropriate maintenance or instruction manuals.

2.2 UNPACKING

The system is shipped with all mounting hardware, cables, plugs, etc., necessary for complete installation.

Read the following procedures before starting an installation:

1. Carefully remove each component from its carton or crate. Observe any special unpacking instructions included with the component.

2. Inspect all components for physical damage. Consult your local Perkin-Elmer office in the event of damage.

3. If any components are shipped from the factory already mounted, ensure that all terminals and connectors are secured properly.

2.3 GENERAL CONFIGURATION AND EXPANSIONS

This section provides a general configuration for the Model 3230 System. Cables, memory expansion, power supplies, and mechanical components are discussed in detail in later chapters.

The basic Model 3230 system consists of:

1 Model 3230 Processor with 512 kb of MOS Memory
1 Loader Storage Unit
1 Consolette
1 2-line Communications Multiplexor
1 Model 550 VDU
1 Universal Clock
1 Perkin-Elmer 3200 SELCH
1 150 A Power Supply
1 Battery Backup
1 I/O Chassis

CHAPTER 3
MECHANICAL CONFIGURATION

3.1 MECHANICAL COMPONENTS

Figures 3-1 through 3-4 illustrate the mechanical components of a typical Perkin-Elmer digital system. Dimensions and mounting information are provided for the system cabinet, chassis support rails, side skins, and doors. Figure 3-2 illustrates the basic cabinet.

The front and rear doors are released by depressing the two spring latches at the top. The same door is used for all configurations with appropriate cutouts for magnetic tape configurations. (Refer to Figure 3-4.)

The same side skin is used for all configurations and is removed when bolting two cabinets together. It is released by the two 1/4 turn nylon fasteners. The side skins are lined with a foam sound absorbing material. (Refer to Figure 3-1.) For further details of the Model 3230 system cabinet, refer to 01-142F01 included in this manual.

3.2 COOLING

Refer to Figure 3-5 during this description. The cabinet is cooled by a packaged blower located at the bottom of the cabinet using the air available at the bottom of the rack, which is either room ambient or air supplied through a raised floor system. The air is distributed by an internal plenum located along the right side of the cabinet opening (if viewed from the front). The air input to the blower enters directly into the bottom section of the plenum. The plenum contains five removable covers located vertically in the appropriate spaces, as illustrated by Figure 3-5.

The blower must be plugged into the AC panel at the rear of the cabinet. The main circuit breaker on the AC distribution panel must be in the ON position to power up the system. The blower air switch is located on the top of the plenum system and is wired as shown in Figure 3-5. The blower is shut off by the main circuit breaker on the AC distribution panel. The blower supplied (36-036F02) requires 230 V AC, 50/60 Hz.

A removable and washable filter is located in the base of the blower package and is accessible from the front of the cabinet when the cover door is removed.

CAUTION

IT IS RECOMMENDED THAT THE SYSTEM BE TURNED OFF BEFORE THE FILTER IS REMOVED FOR MAINTENANCE. DIRT CAN BE BLOWN INTO THE SYSTEM AND DEPOSITED ON THE CIRCUIT BOARDS OR CLOG AIR DISTRIBUTION SCREENS LOCATED INSIDE THE PLENUMS.

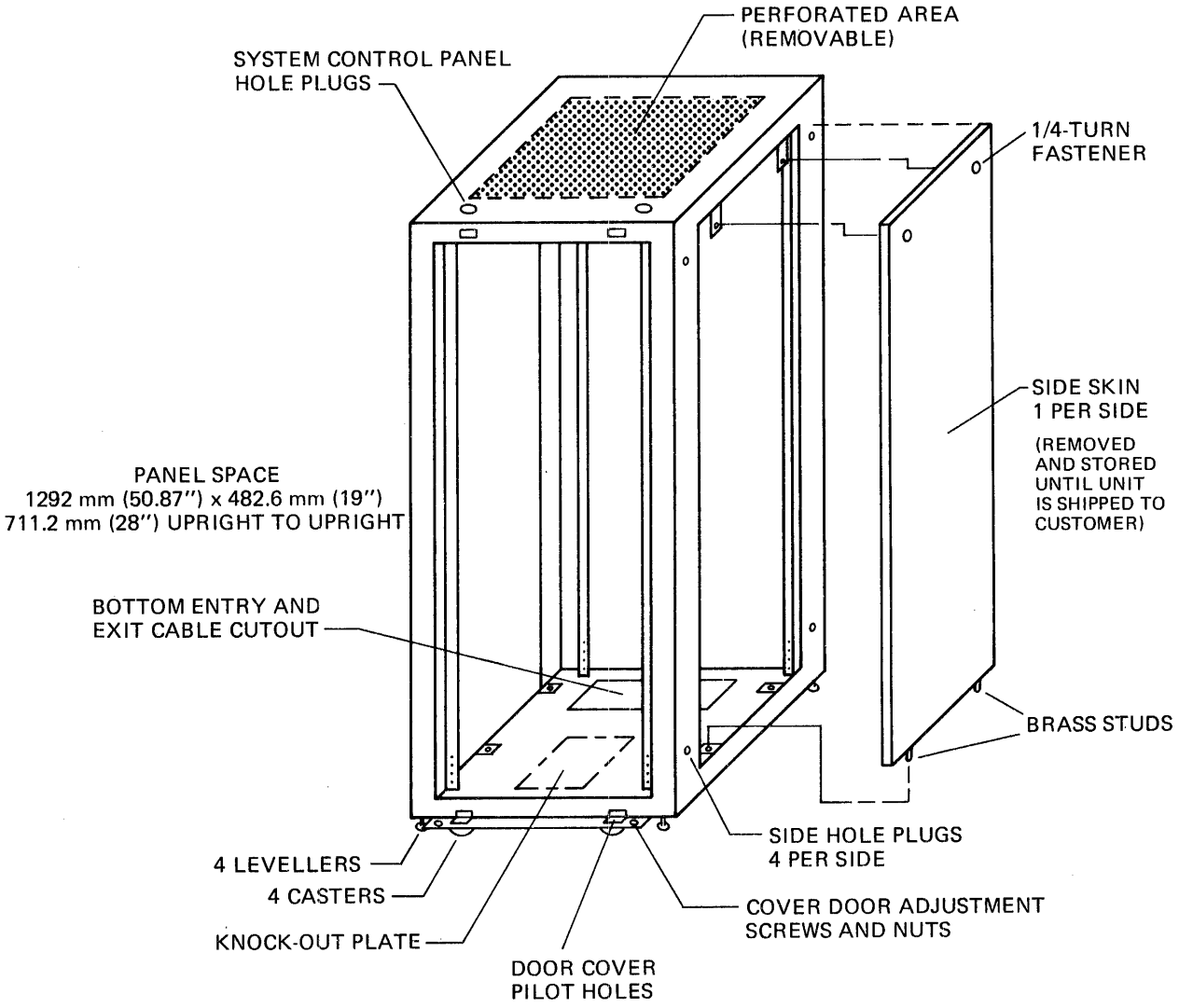
Two types of plenum covers are provided: solid and perforated. Solid covers are snapped in place at locations where there are no card files. Perforated covers are used in locations having an operating card file. In the Model 3230, perforated covers are factory installed. No changes are required.

3.3 177.8 mm (7-INCH) BOARDS IN A 381 mm (15-INCH) CHASSIS

One or two 177.8 mm (7-inch) boards (half-boards) may be inserted into a 381 mm (15-inch) chassis via the 16-398 Half-Board Adapter Kit (refer to Figure 3-6). The Half-Board Adapter Kit may hold two active 177.8 mm (7-inch) boards or one active and one blank 177.9 mm (7-inch) board, depending on requirements. No wiring takes place between the boards and the adapters. The adapters are designated such that the connectors on the boards plug directly into the chassis.

BASIC RACK STRUCTURE
56" FOR MODEL 3230

11-218

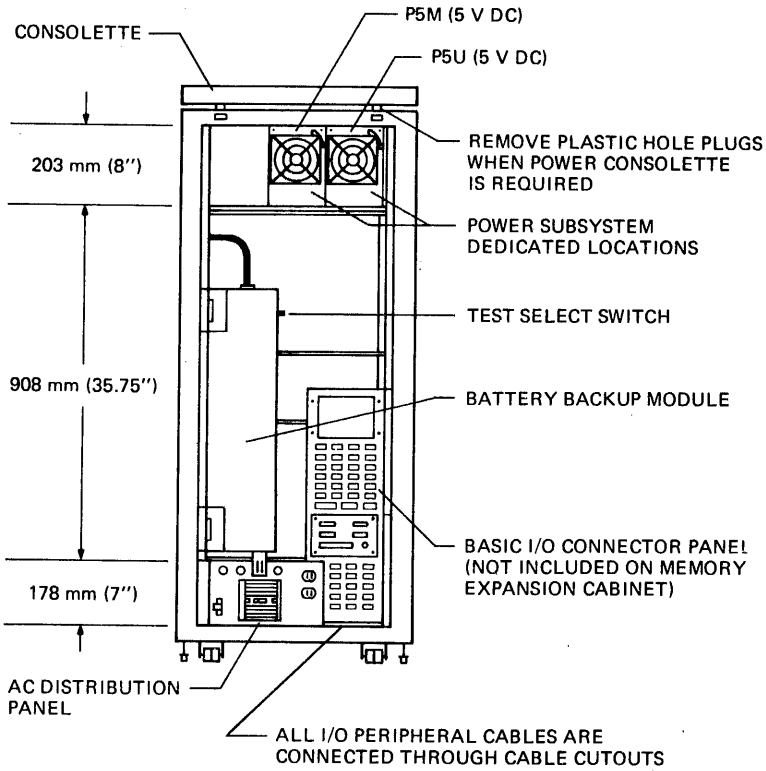


NOTE

MATL: CRS.104 THK (STRUCTURE)
SIDE SKINS CRS .047 THK.
PAINT: P.E. #464 TEXTURED

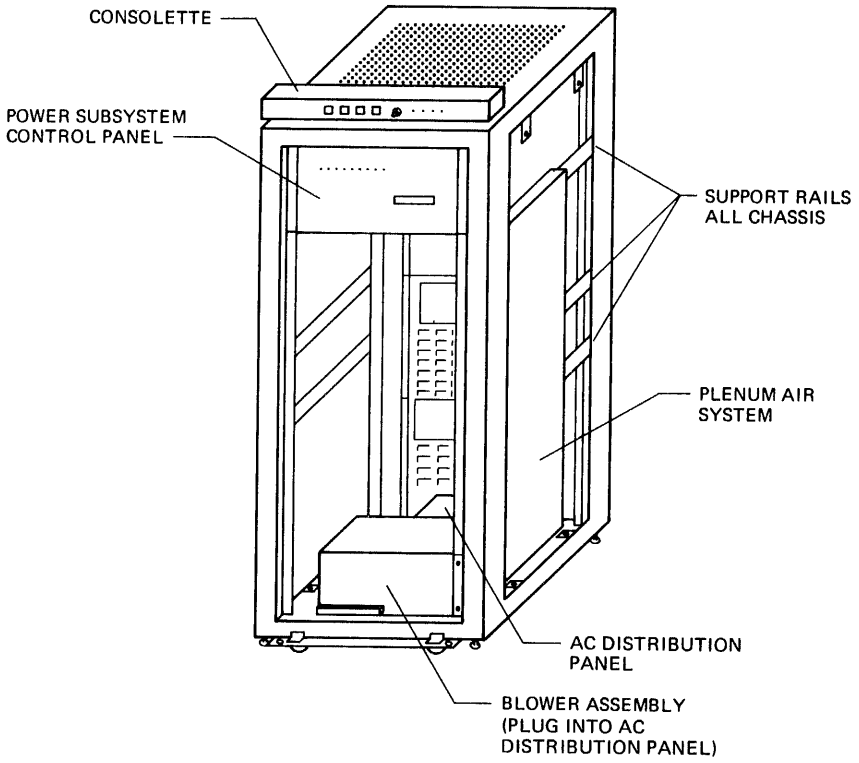
Figure 3-1 Basic Rack Structure

1855



(REAR VIEW)

1856



(FRONT VIEW)

Figure 3-2 Basic System Cabinet

1857

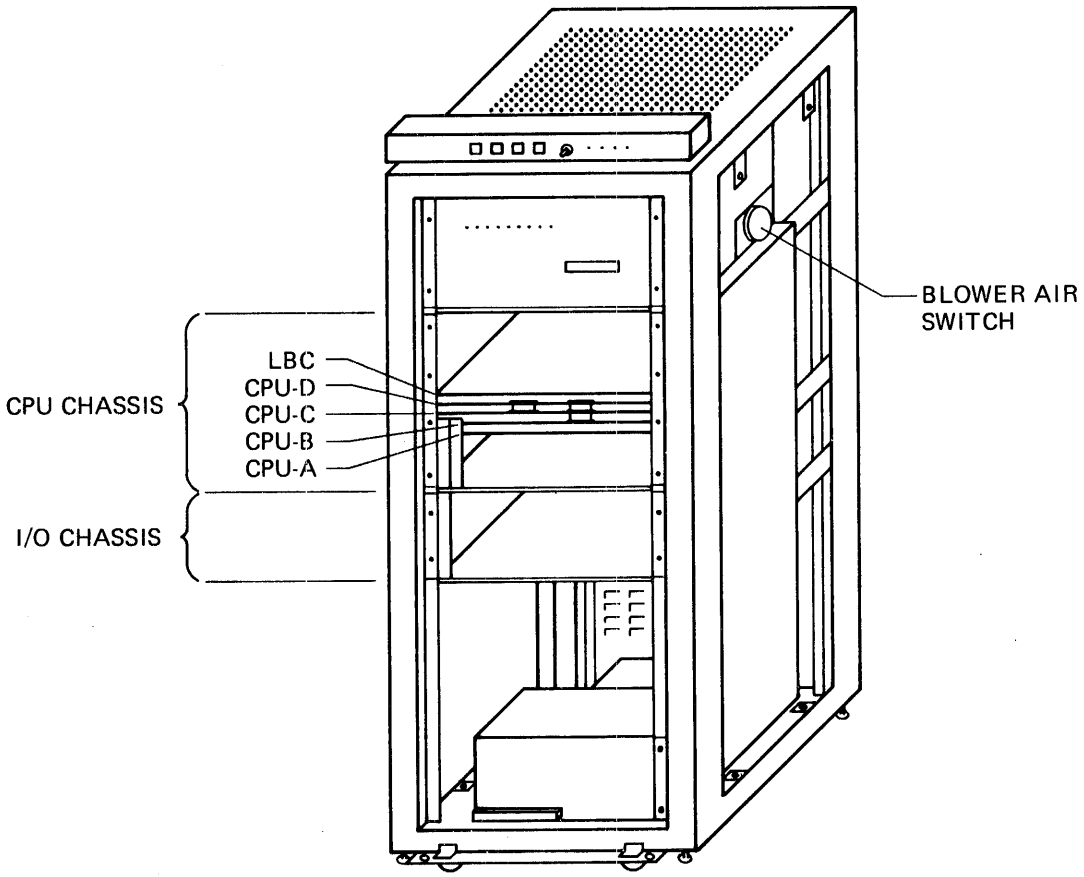
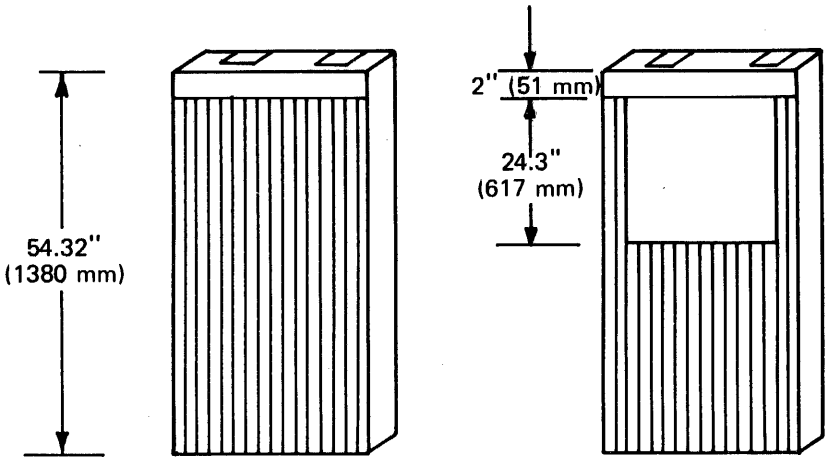


Figure 3-3 Chassis Layout (Front)

0108-1

PARTS TO BE ATTACHED PRIOR TO SHIPMENT



FULL DOOR
– 13.045 F01 –

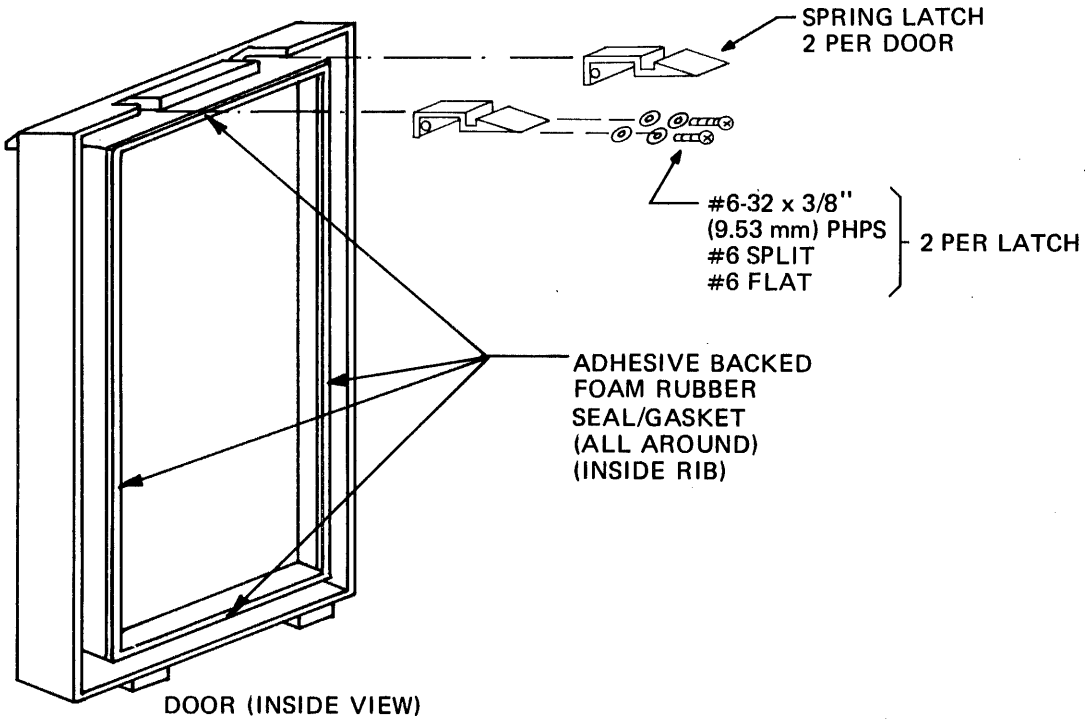
NOTE:

USE FOR ALL FRONT & REAR DOOR COVERS WHEN PERIPHERAL CUT-OUTS ARE NOT REQ'D (SEE REAR VIEW) DETAIL FOR LATCH & GASKET REQ'MNTS TYPICAL - ALL DOORS

MAG-TAPE DOOR
– 13.045 F02 –

NOTE:

USE FOR ALL
45 IPS
75 IPS
MAG TAPE
UNITS



DOOR (INSIDE VIEW)

Figure 3-4 Doors and Latches

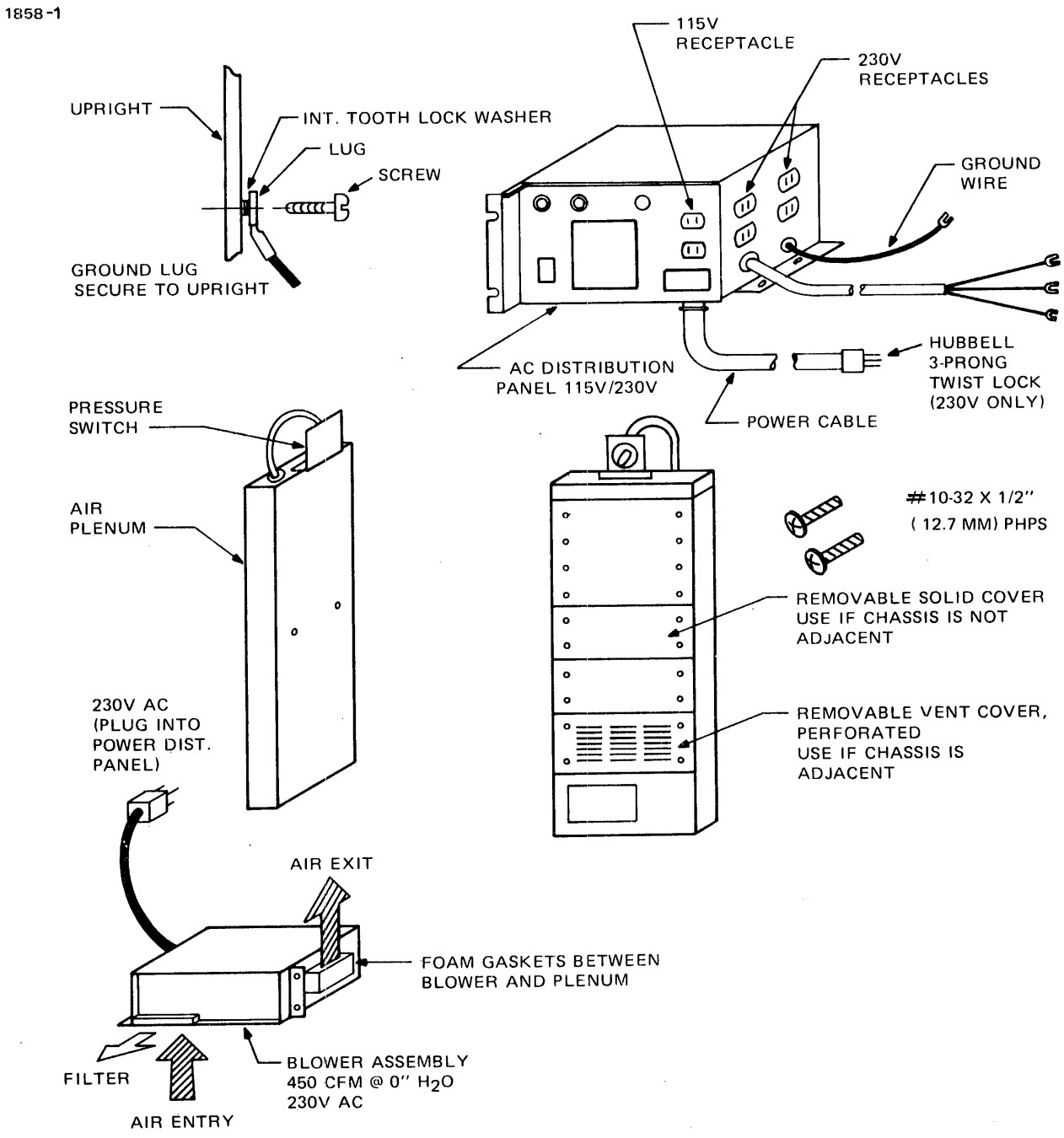


Figure 3-5 Blower/Plenum/Power Distribution

0110

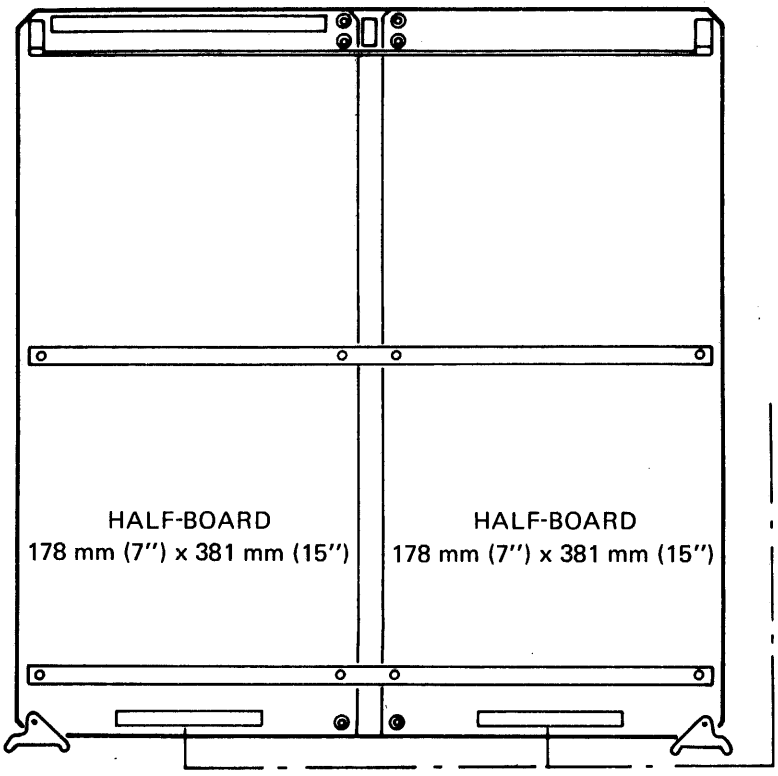


Figure 3-6 16-398 Half-Board Adapter

CHAPTER 4
POWER SUBSYSTEM

4.1 INTRODUCTION

For complete detailed installation and maintenance information, refer to the 34-038 Power Subsystem Installation and Maintenance Manual, Publication Number 47-010.

The Perkin-Elmer 34-038 Power Subsystem is a modularly designed power conversion system suitable for use in the Perkin-Elmer 3230 System. It supplies 5 volt logic power (P5) and 5 volt memory power (P5U). The unique modular construction of the power subsystem provides a built-in expansion capability and allows immediate field replacement of modules. The power subsystem is designed for Underwriter Laboratory (UL), Canadian Standards Association (CSA), and Verband Deutscher Electrotechniker (VDE) approval.

The basic units of the power subsystem are built into the system cabinets. Optional modules are available, which allow each cabinet to be configured for its own specific requirements. A master CPU cabinet may need to add only one P5 power module; an I/O cabinet may require two P5 power modules; an MOS memory cabinet may require one or two P5 power modules, a P5U power module, and a battery backup module to protect against memory data loss in the event of AC power outage.

The maximum power subsystem for each system cabinet consists of the following modular and nonmodular units: one AC distribution panel; one front-end module, which provides AC line rectification and filtering; up to two P5 power modules (+5 V at 150 A each) designed for parallel operation capability; one Power Subsystem Controller (PSC); one battery backup module for the memory power module; and one P5U memory supply. The module which supplies P5U is identical to, and interchangeable with the modules which supply P5. The basic subsystem provides only one P5 power module; the second P5 (slave) module, the memory power module, and the battery backup module are optional, depending on configuration.

CHAPTER 5
SYSTEM CONTROL PANEL

5.1 SYSTEM CONTROL PANEL

This section describes the installation and operation of the System Control Panel.

5.1.1 Introduction

The System Control Panel mounts at the top front of the basic processor cabinet and is fastened in place via two 25.4 mm (1") aluminum lock nuts. (Refer tc Figure 5-1.)

As shown in Figure 5-1, the System Control Panel is hooked up to the backpanel via two ribbon cables which are labeled. P3 and P2 are keyed such that they can be installed only one way on the processor backpanel J3 and in the power subsystem controller (PSC) J1.

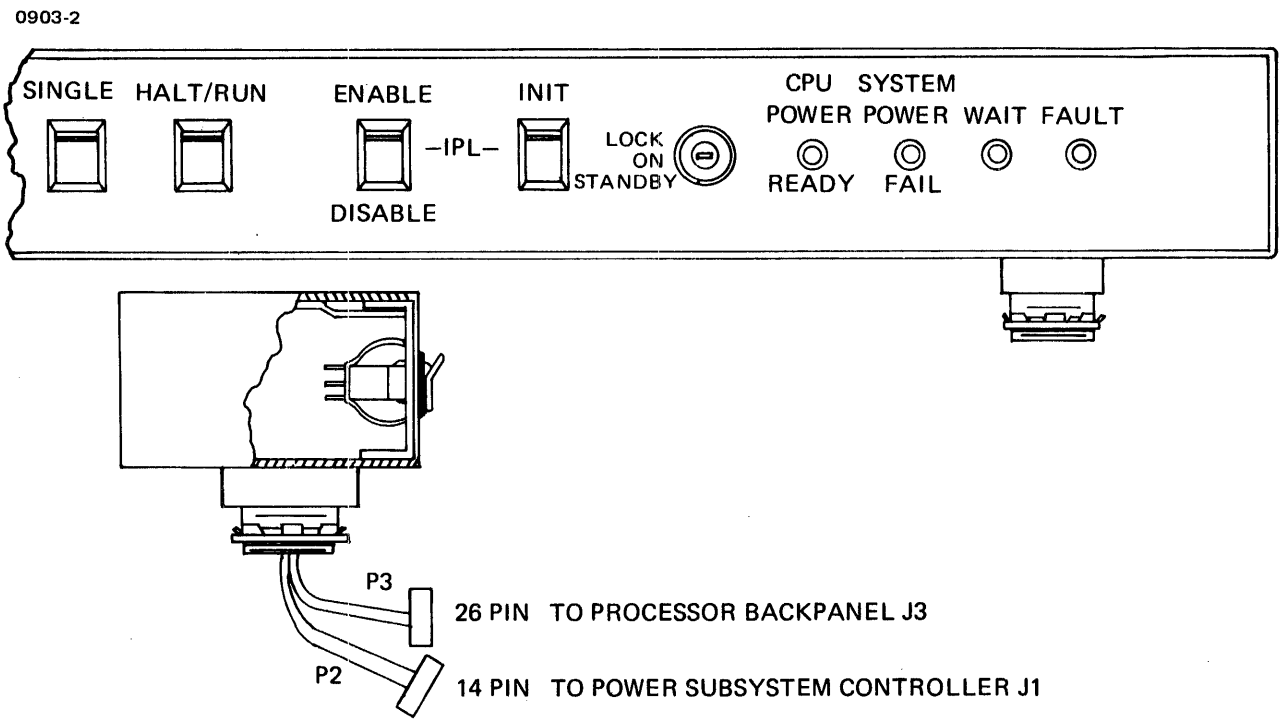


Figure 5-1 System Control Panel (Front View)

5.1.2 Key-Operated Security Lock

This is a 3-position (STANDBY/ON/LOCK) key-operated locking switch which controls the primary power to the system. The key lock performs the following functions:

STANDBY - Processor 5 volts off, 5 volts STANDBY (P5U) on

ON - The primary power is on.

LOCK - The primary power is on and the INITIALIZE HALT/EXE and SINGLE switches on the System Control Panel are disabled.

5.1.3 INITIALIZE (INIT) Switch (Momentary Switch)

The initialize switch causes the system to be initialized. After the initialize operation, all device controllers on the system multiplexor bus are cleared and certain functions in the processor are reset. This switch is disabled when the key is in the LOCK position.

5.1.4 IPL ENABLE/DISABLE Switch

When the IPL ENABLE/DISABLE switch is in the ENABLE position and AC power is restored, if the security lock switch is placed in the ON position from the STANDBY position, or if the INIT switch is depressed, the system is reloaded from the LSU.

5.1.5 HALT/RUN Switch

When depressed, this single action switch causes a running system to halt and enter the processor console service state, or it forces a halted system in the processor console service state to enter the run mode.

If the system is in the FAULT mode and is looping in the memory test section of self test, depressing the HALT/RUN switch causes the system to enter the processor console service state and displays the faulting address on the system console. This allows other means to be used for diagnosing the probelem.

5.1.6 SINGLE Switch

This switch, when placed in the ON position, puts the processor in the single instruction cycle mode and takes a running program to the processor console service mode. When in the single instruction cycle mode, the processor is returned to the processor console service mode after execution of each user instruction. The Location Counter displays the address of the next instruction to be executed. The status portion of the PSW reflects the execution of the previous instruction.

5.1.7 Indicators

POWER	This indicates that system power is on.
WAIT	The running program can place the processor into the wait state by setting the wait bit of the current Program Status Word (PSW). The WAIT indicator is turned on to inform the operator that the system is in the wait state. The WAIT indicator also turns on when the processor is in the console service mode.
SYSTEM POWER FAIL	This lamp indicates a failure in an expansion cabinet power system.
FAULT	The FAULT indicator turns on during system initialization and remains on until successful completion of the microcode power-up test. The indicator remains on if the processor self-test fails.

CHAPTER 6
PROCESSOR AND MEMORY INSTALLATION

6.1 INTRODUCTION

This chapter describes the installation of the 3230 processor and memory. All processor and memory boards occupy slots in the basic 3230 system chassis, as shown in Figure 6-1.

The basic processor and memory consists of:

1 CPU-A board, 35-767 in slot 4
1 CPU-B board, 35-768 in slot 5
1 CPU-C board, 35-769 in slot 6
1 CPU-D board, 35-770 in slot 7
1 CPU-LBC board, 35-771 in slot 8
1 STM (512 kb), 35-764 in slot 9/16
1 cable 17-234F08 (50 pin)
1 cable 17-234F09 (50 pin, 3 header)

1859

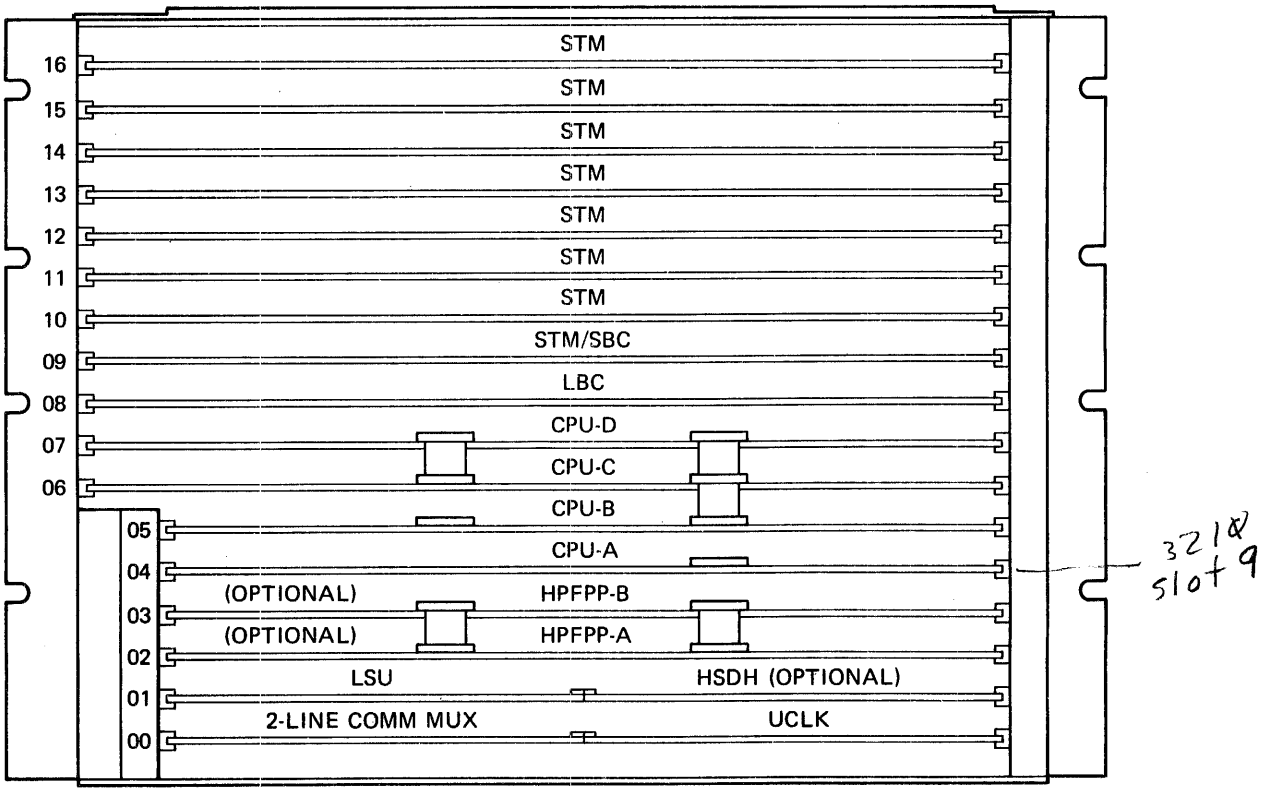


Figure 6-1 Front View of a 3230 Chassis

6.2 CPU-A (35-767)

The CPU-A board must always be installed in slot 4. Before installing this board, ensure that the Privileged Illegal ROM and option strapping are correct. The Privileged Illegal ROM (19-188F25) is in location 10J. If the board is equipped with Writable Control Store option (35-767F04), the Privileged Illegal ROM is a 19-188F27.

At location 05M, the COMM option and the HPFPP option must be disabled by strapping A to G and C to G, respectively; the DROMs are enabled by strapping TP2 to TP8 at location 05E.

Ensure that the Test Aid DIP switches in the connector 5 location of the CPU-A board are in the OFF (open) position.

The CPU-A board may now be installed.

6.3 CPU-B (35-768)

The CPU-B board must always be installed in slot 5. There is no strapping on the CPU-B board.

6.4 CPU-C (35-769)

The CPU-C board must always be installed in slot 6 of the CPU chassis. This board contains the strapping required for allocating segments of memory to shared memory. At the time of manufacture, the board is strapped such that all memory is local. Memory may be allocated as shared memory in 1-megabyte increments. Refer to the functional schematic for the CPU-C board, 35-769D08, Sheet 13, for strapping information.

6.5 CPU-D (35-770)

The CPU-D board must be installed in slot 7 of the CPU chassis. No strapping options are contained on this board. Certain straps located on this board are used for factory maintenance purposes. Refer to Chapter 15, Adjustments, for this information.

On the CPU-D board, if the following straps have not been installed, the DMA system hangs up.

LOCATION	STRAP
00A	10 to 72
02A	09 to 73
CONN 6	112-6(TPD) 113-6(TPC)

6.6 CPU-LBC (35-771 or 35-806)

The CPU-LBC board is always installed in slot 8. Before installing the LBC, check CONN 5 for the following:

215-5 (TP10) connected to 216-5 (TP9) if LBC drives 4 megabytes of memory or less (35-771 LBC) or if LBC drives 8 megabytes or less (35-806 LBC)

221-5 (TP4) connected to 222-5 (TP3)

217-5 (TP8) connected to 218-5 (TP7)

TPA connected to TPB

No connection between 224-5 (TP1) and 223-5 (TP2)

No connection between 214-5 (TP11) and 213-5 (TP12)

6.7 STM

The STMs must be installed in descending slots beginning with slot 16. Slot 16 has the lowest memory address and slot 09 has the highest. The denser STMs must always occupy the lower memory addresses (higher slot number).

The 35-764 F02 (512 kb), F03 (1.0 Mb), and F04 (2.0 Mb) STMs may be mixed in memory configurations up to 8 Mb using the 35-806 LBC only. For configurations over 8 Mb, only the F03 and F04 modules may be used.

When a Shared Bank Controller is installed in slot 09 for shared memory, local memory is restricted to 14 megabytes.

6.8 PROCESSOR CABLING

Install the following cables:

CABLE	FROM	TO	TO
17-234F08 (50 pin)	CPU-D CONN 5	CPU-C CONN 5	NA
17-234F09 (50 pin)	CPU-D CONN 4	CPU-C CONN 4	CPU-B CONN 3

6.9 RACKO/TACKO PRIORITY CHAIN

The 3230 I/O System implements a unique RACKO/TACKO priority daisy chain as compared to previous systems - Models 7/32, 8/32, and 3220. The 3230 RACKO/TACKO priority chain starts on the first I/O slot, "zero" side, of the CPU chassis and traverses down the "zero" side to the last I/O slot of the last I/O expansion chassis. Then it is returned (RETACKO) to the first I/O slot, "one" side of the CPU chassis and traverses down the "one" side to the last I/O slot of the last I/O expansion chassis where it is terminated. Figures 6-2 and 6-3 represent the old and new I/O priority chain schemes, respectively.

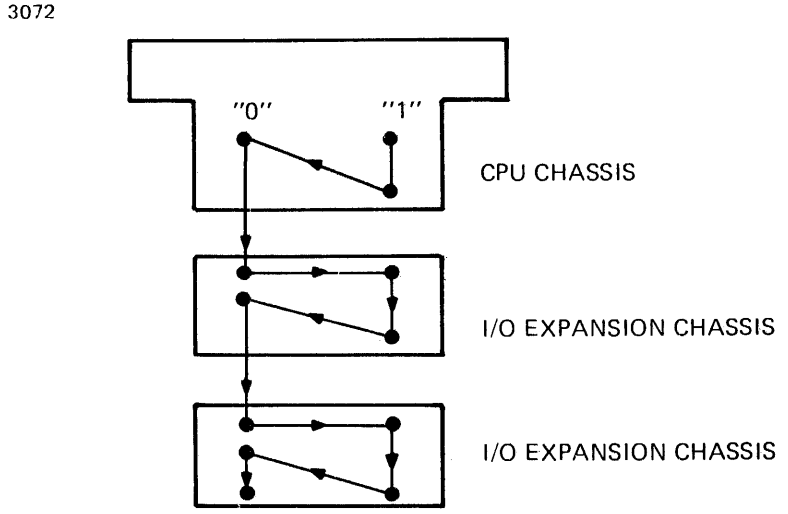


Figure 6-2 Old System (3220) I/O Priority Chain

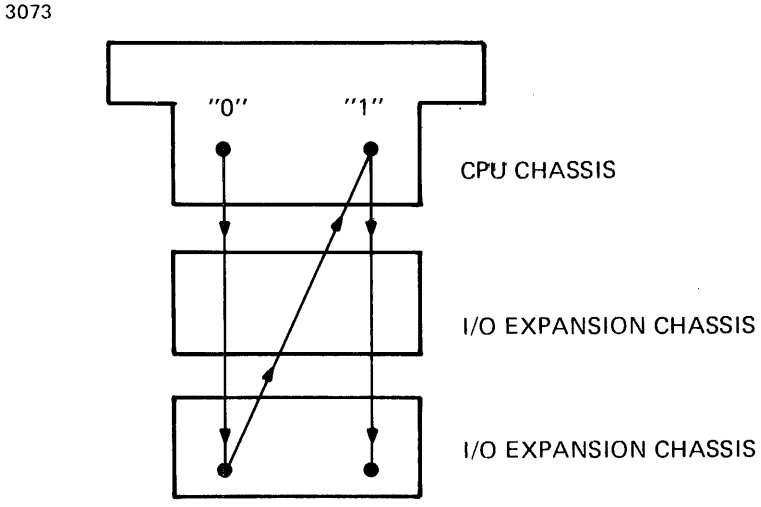


Figure 6-3 New System (3230) I/O Priority Chain

6.9.1 RETACKO Strapping Procedure

The RACKO/TACKO return path (RETACKO) strapping procedure follows. All references should be made to Figure 6-4.

1. Insure that twisted pair wire is used:

   yellow = signal RETACKO
   black = ground connection

   Pin Identification Format:

   X_1XX = YYZZ
   X_1 = row number (1 or 2)
   XX = pin number
   YY = slot number
   ZZ = connector

2. CPU Chassis:

   A. connect: 114-0006 to 122-0101 (yellow)
      connect: 119-0006 to 140-0101 (black) GND

3. I/O Expansion Chassis:

   A. connect: 114-0006 to 114-0002 (yellow)
      connect: 119-0006 to 119-0002 (black) GND

   B. Remove the following jumper from all the I/O chassis except the last one:

      disconnect 114-0006 to 214-0006 (orange)

   C. Insure that the last I/O expansion chassis has the following jumper installed:

      connect: 114-0006 to 214-0006 (orange)

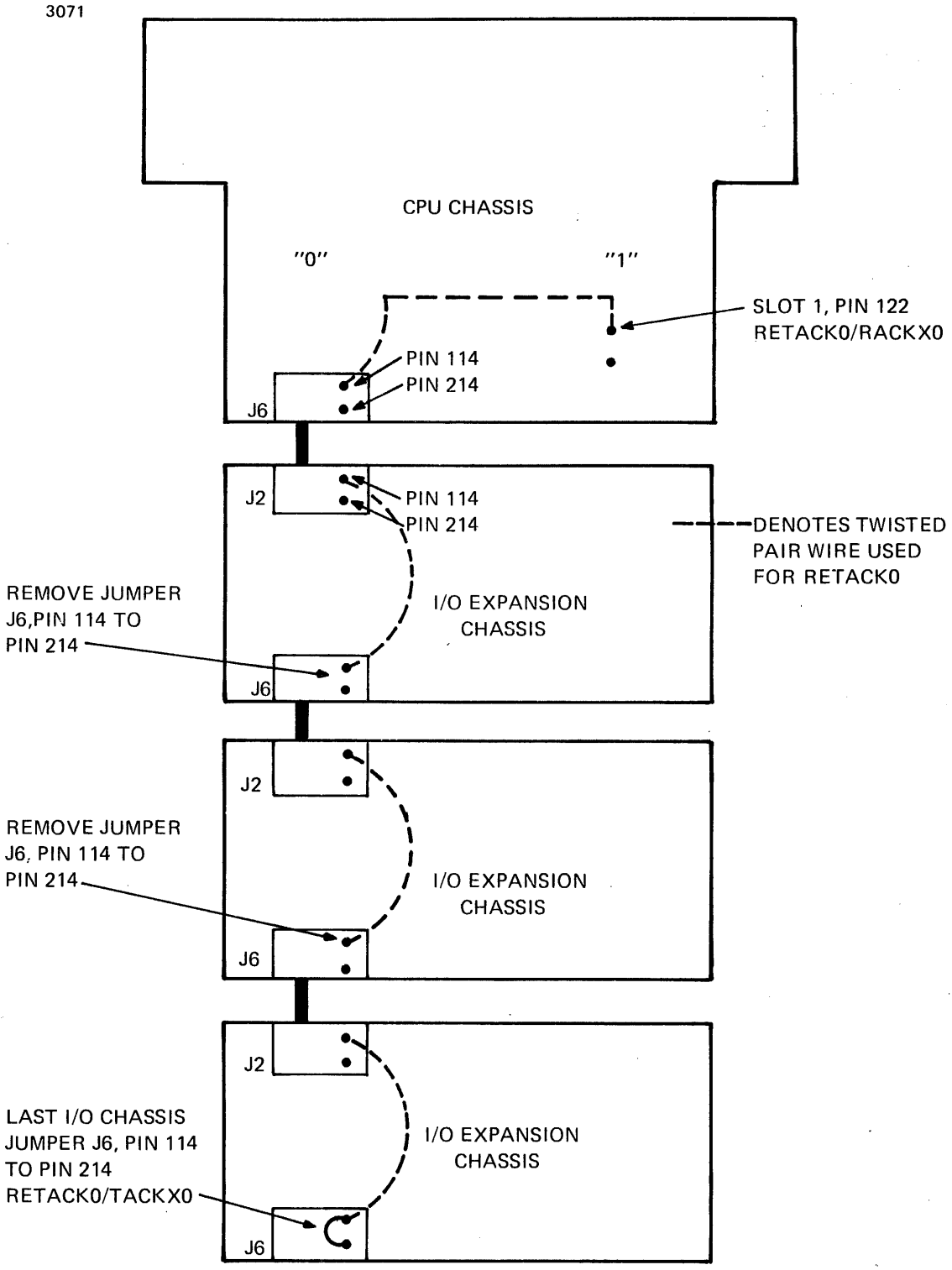


Figure 6-4 RETACK0 Return Path Strapping
(System Cabinet, Rear View)

6.10 MULTILEVEL EXTERNAL INTERRUPTS

1. The Model 3230 is capable of acknowledging four levels of external interrupts. An attention (ATN) line and a priority chain (RACK0/TACK0) are associated with each interrupt level.

2. The four attention lines (ATN000:030) located on the CPU-A (CPU chassis - slot 4) are wired to the OR-tied attention lines of the device controllers (or external CPU).

3. The four acknowledge lines (ACK000:030) are the source of the priority chain. They are located on the CPU-D board.

4. ATN/ACK levels must not be crossed. That is, ATN000 must be OR-tied to ATN line of those devices in the ACK000 priority chain. Similarly, ATN010 must be in the ACK010 priority chain, etc.

5. If interrupt levels are different between two I/O chassis that are connected with the 35-813 FXX terminators and 17-464 FXX or 17-503 FXX cables, insure that straps E2 to E3 (RACK0/TACK0) and E7 to E8 (ATN0) are removed on the 35-813 terminators.

CHAPTER 7
BLOCK DIAGRAM ANALYSIS

7.1 INTRODUCTION

This chapter provides an overview of the 3230 Processor. Refer to Functional Schematic 01-142D08, Sheet 1, for a block diagram. Each board in the CPU is discussed individually in order to understand how the logic is partitioned within the CPU. This understanding is necessary in order to isolate faults to the board level.

7.2 SYSTEM ORGANIZATION

The CPU is organized between three 32-bit buses: the A, B, and S buses. The A bus presents data to the Arithmetic Logic Unit (ALU). The B bus presents data to the ALU, HPFPP, WCS, and Link Register. The S bus transfers the ALU output data to the appropriate destination. The source and destination of the A, B, and S buses and the functions performed by the ALU are controlled by microinstructions contained in the control store.

7.3 CPU-A BOARD

The CPU-A board contains the heart of the microprocessor which is used to emulate the instruction set. This board houses all elements of control store for the machine, the control store addressing, both fixed and writable control store, interrupt handling, and power fail/initialize control.

7.3.1 Fixed Control Store (FCS)

Fixed Control Store (FCS) consists of 2 k words, 32 bits each, of Read-Only-Memory (ROM) which is a high-speed, solid-state, nonvolatile memory. Each word in FCS is 32 bits long and represents one microinstruction. Each microinstruction read out of FCS is placed in the 32-bit ROM Data Register (RDR). RDR is the instruction register for the microprocessor and drives the RD bus. Most microinstructions are executed in one machine cycle of 200 nanoseconds. RD bits are decoded to direct the processor through its operations. The meaning of the microinstruction word is explained in Chapter 8.

7.3.2 Writable Control Store (WCS)

The optional Writable Control Store (WCS) is a high-speed, static-random access memory consisting of 2 k words of 32 bits each. The WCS can hold user-defined microinstructions. At the microinstruction level, the WCS is loaded/unloaded to or from the B bus as addressed by the contents of the Link Register (LR).

Writable Control Store is supported by user-level instructions. Refer to the 3230 User's Manual, Publication Number 29-721.

7.3.3 ROM Data Register (RDR)

The ROM Data Register (RDR) is a 32-bit register which is loaded at the beginning of every machine cycle with microinstructions fetched from control store. The RDR drives the RD bus. This register can also be described as a pipeline register, since it allows for overlapping of ROM access and instruction execution.

7.3.4 Control Store Address Register (CSAR)

Locations in control store are addressed by the 12-bit Control Store Address Register (CSAR). Microinstructions are normally located at sequential addresses in the control store. The CSAR is an up-counter which increments by one as each new microinstruction is read into the RDR. The CSAR, therefore, holds the address of the next sequential microinstruction to be executed. When it becomes necessary to jump out of sequence, the CSAR can be loaded with a new address from the RDR register, the Decoder Read-Only-Memories, the Link Register, or the priority interrupt encoder; or it can be cleared by the hardware to zero for an instruction read or system initialization.

7.3.5 Link Register (LR)

A branch and link capability is provided in this machine by means of the 12-bit Link Register (LR). The LR is also used as a pointer for reading from or writing to the optional WCS.

When the microprogram specifies Link, the LR is unconditionally loaded with the address of the current microinstruction being executed and is automatically incremented by one prior to the next system clock. When the microprogram executes a Branch/Return, the CSAR is loaded from the LR.

The LR may also be loaded from the B bus in order to nest microsubroutines or when LR is used as a pointer to WCS. (After a read/write WCS, the LR is automatically incremented.)

7.3.6 Decoder Read-Only-Memory (DROM) and Privileged Illegal ROM (PILROM)

The DROMs are constructed using three 512x4-bit ROMs which are addressed by the 8-bit op-code field of the Instruction Register. They contain the D1 and D2 vector addresses which are entry points for instruction emulation routines. The microprogram interrogates the D1 address at instruction read time and the D2 vector during instruction emulation. The 12 bits of the resulting readout are jammed into the CSAR, resulting in an automatic transfer to an address which is related to the user's operation code.

The Privileged/Illegal ROM (PILROM) is also addressed by the 8-bit op-code field and is interrogated at D1 time to supply privileged instruction, illegal instruction, and WCS enable information to the CSAR control logic.

7.3.7 Priority Interrupt Encoder

The priority interrupt encoder provides high-speed interrupt handling to the microprogram. It monitors 14 interrupt lines, sets their priorities, and when interrogated by the microprogram, provides a vectored branch into the interrupt service table in the microcode.

7.3.8 Initialize Logic

System initialization is controlled on the CPU-A board by the initialize logic. This logic interfaces to the power system and, together, they monitor and control the DC power required in the system. Early Power Fail (EPF) and Primary Power Fail (PPF) interrupts are also generated by this logic.

7.3.9 Console Support Logic

The console support logic monitors the EXECUTE/HALT switch and the single switch from the System Control Panel and creates console attention interrupts to the microprogram.

7.3.10 Test Aid

The CPU-A has a built-in test aid. Sixteen switches in two DIP packages at the front of the CPU-A board provide CSAR match/SYNC, microcode single step, WCS destination match, and external match capabilities for troubleshooting.

7.4 CPU-B BOARD

The CPU-B board is the processor's arithmetic board. It contains a 32-bit ALU which is fed by the 32-bit A multiplexor and a 32-bit B multiplexor, a 32-bit shift register, the PSW, a flag register, and the A and B register stacks.

7.4.1 Arithmetic Logic Unit (ALU)

The Arithmetic Logic Unit (ALU) is 32 bits wide with full look-ahead carry logic. It is fed by the 32-bit A and B multiplexors and its output generates the S bus.

7.4.2 A Multiplexor

The 32-bit A multiplexor feeds the ALU from either the A bus or the shift register.

7.4.3 B Multiplexor (B Bus Shifter)

The 32-bit B multiplexor feeds the A input to the ALU and is used as the input to the register stacks for divide operations. It also performs all of the ALU shift operations defined in the shifter microcode field.

7.4.4 32-Bit Shift Register

This register can be loaded from the S bus, shifted left or shifted right (one place per processor clock), and can be presented to the B bus or to the ALU via the A multiplexor.

7.4.5 Flag Register (FLR)

The Flag Register (FLR) is a 4-bit register containing the following flags: Carry (C), Overflow (V), Greater than Zero (G), and Less than Zero (L). These flags are modified at the conclusion of arithmetic and logical microoperations to reflect the result of the operation. The FLR is loaded from bits 28:31 of the S bus when either the FLR or the Program Status Word (PSW) is the specified destination register.

7.4.6 Program Status Word (PSW)

The Program Status Word (PSW) is a 24-bit register used to indicate the system status relative to the user program being emulated. Bits 8:27 of the PSW are used as interrupt masks to define the operational status or mode of the user-level processor. Some of the PSW bits have hardware significance, while others are of significance only to the microprogram. Bits 28:31 of the PSW make up the Condition Code (CC) field which reflects the result of the previous user instruction.

The status portion of the PSW is 32 bits long. Only 24 bits, however, are implemented in the hardware of this machine. Bits 0:7 are not used and are forced to zero.

The CC may be updated only from the FLR. When PSW is the specified destination register, bits 8:27 of the S bus are loaded into bits 8:27 of the PSW, and S bus bits 28:31 are captured in the FLR. The CC field remains unchanged until the microprogram causes it to be updated from the FLR when the jam bit is set in the microword. The PSW is unloaded onto the A bus.

7.4.7 A and B Register Stacks

The 32-bit A and B register stacks hold the 4 microregisters, 8 general register sets of 16 registers each, and an alternate register set of 16 registers. These stacks are loaded simultaneously from the S bus (from the B multiplexor in the case of a divide) and always hold identical data. The A and B register stacks can be unloaded by the A and/or B source field of the microword to their respective latch registers.

7.4.8 Register Stack Control

The register stack control provides address and timing for the register stacks.

7.5 CPU-C BOARD

The CPU-C board provides an interface between the central processing unit and memory system. All registers associated with memory addressing and memory data are located on this board. This unit also contains the Memory Address Translator (MAT). The MAT provides dynamic address relocation and memory protection.

7.5.1 Location Counter (LOC)

The Location Counter (LOC) is a 24-bit addendum to the PSW which holds the address of the next user instruction to be executed in main memory. The LOC is implemented as an up-counter which increments by two for each halfword of data required to execute an instruction.

7.5.2 Processor Memory Address Logic

The Memory Address Register (MAR) is a 24-bit register which contains the address of main memory to be accessed. The LOC is selected as the address to memory during instruction reads through the Program Address (PA) multiplexor; in all other cases, the PA selects the MAR.

Each time a memory reference is made, including instruction reads, the output of the PA multiplexor is loaded into an auxiliary address register (ZMAR). If a fault is detected in the system, the data in the ZMAR remains unchanged until directed by the microprogram. The first time, after a fault, that MAR is the selected B source, the data contained in the ZMAR is unloaded.

On a processor operation to memory, the 13 most significant bits of the program address are subject to relocation and placed on the LMA bus, while the 11 least significant bits are placed on the bus unchanged.

7.5.3 Memory Address Translator (MAT)

Dynamic memory relocation is provided when enabled by bit 21 of the PSW. This is accomplished by adding the relocation field of the selected segmentation register to bits 16:20 of the program address which has bits 8:15 forced to zero. This relocated address is then used to access memory.

The segmentation registers also contain the necessary information to provide memory access protection for the selected segment.

7.5.4 Memory Data Register (MDR)

Processor data from/to main memory is contained in the Memory Data Register (MDR). This register is 32 bits wide and is loaded from the S bus before initiating a memory write operation. The data contained in the MDR is gated onto the local memory bus (MDS bus) for writes to local memory.

The data, when it becomes available on a memory read, is loaded into the MDR from the MDS bus or EDMA bus. The microprogram can then access the data by specifying the MDR as the B bus source.

7.6 CPU-D BOARD

The CPU-D board is the machine's control board. The system clocks for the processor, as well as I/O, EDMA, and memory control logic, are all contained on this unit. Refer to Chapter 12 for a detailed analysis of the CPU-D and for all information concerning clocks and control logic.

7.6.1 Instruction Register (IR)

The Instruction Register (IR) is a 16-bit register divided into three fields: operation code (OP), user destination (YD), and user source (YS). The IR is loaded during an instruction fetch, when the data is available from memory.

7.6.2 Input/Output (I/O)

The 16-bit parallel Input/Output (I/O) bus is used to send and receive information to and from device controllers. These operations are achieved by gating S bus data onto the D bus and activating an I/O control line, or by activating a control line and gating D bus data onto the internal B bus.

7.6.3 Extended Direct Memory Access (EDMA) Registers

Data paths for Extended Direct Memory Access (EDMA) operations to memory are contained within the CPU-D board. The local memory address on an EDMA operation is loaded into the EDMA Memory Address Register (EMAR) and sent to the LMA bus. Data on write operations from an EDMA device, e.g., a BSELCH, is loaded into the EDMA Memory Data Register (EMDR) and presented to the local memory bus through the MDS multiplexor. For memory read cycles, data goes from memory to the EMDR and then onto the EDMA bus.

7.7 LOCAL BANK CONTROLLER (LBC)

This board provides an interface between the processor and the storage module (main memory) in the system (refer to Chapters 13 and 18). The major functions of this module are the generation of the necessary timing for the storage modules, error code generation and checking, cache memory, error logging, and memory refresh control.

Address and data information between the processor and main memory is latched in registers contained on the LBC. Refer to Chapter 13 for detailed descriptions of the timing and control logic on this board.

7.7.1 Input Data Register (IDR)

At the start of a memory write operation, the data on the MDS bus (MDS000:310) from the processor is latched in the Input Data Register (IDR). This data is then presented to the error correction logic in order to generate the seven parity bits used for error correction. The data, along with the parity bits, is then gated to the local memory bus (LMB000:380).

7.7.2 Output Data Register (ODR)

For memory read operations, good data (data which has been checked and corrected if necessary) is latched in the Output Data Register (ODR). The ODR is constructed using tri-state devices. These outputs are used to form the bidirectional MDS bus.

7.7.3 Good Data Register (GDR)

The Good Data Register (GDR) is used to latch checked/corrected data to be returned to the processor on memory read cycles, or which is to be written into memory. Data is written to memory from the GDR any time a memory read is initiated and an error is detected and corrected, or on a partial word write operation (byte or halfword write) whether or not an error has been detected.

7.7.4 Uncorrected Data Register (UDR)

Data read from memory is stored into the Uncorrected Data Register (UDR). This data is used as an input to the error correction/detection logic along with the parity bits contained in the Uncorrected Parity Register (UPR).

If the data is found to be valid, this good data is loaded into the GDR, unmodified. If a single-bit error is detected, the error correction logic generates correct data and loads it into the GDR where it is then transferred to the applicable destination.

7.7.5 Cache

Cache memory, implemented on the LBC board, is 1 kb of direct mapped write-through cache. Four high speed, 256x9-bit random access memories are used to construct the cache. This memory is divided into 64 independent 16-byte buffers.

On memory read operations, data is accessed directly from the cache if it is valid. If the data in the cache is not valid, a quadword (16 bytes) read operation is initiated to memory. The fullword of data required by the processor is output on the MDS bus and the entire quadword is stored in the cache; that segment is then marked valid.

On memory writes, the data is stored into the cache if the addressed segment is valid. At the same time, the data is stored into main memory. If the segment is not valid, then cache is not affected, but the write operation takes place in a normal fashion.

7.7.6 Error Logger

Each time an error is detected on a read from memory, information concerning the type of error (single-bit or multiple-bit) and the chip location for single-bit errors are stored in a 2 kilobit (4 Mb) or 4 kilobit (8 Mb) random access memory. The data in this memory can be accessed by the processor by issuing a read error logger command.

CHAPTER 8
MICROWORD DESCRIPTION

8.1 INTRODUCTION

The microword consists of groups of data bits that are fetched from control store as a 32-bit microinstruction word. Groups of ROM Data (RD) bits of the microinstruction control various hardware functions of the microprocessor. The specific function of the data bit groups may be altered by the format of the microinstruction, the operation modifiers, or the specific source or destination register. The following is a breakdown of these data bit groups which are called instruction word fields. Refer to Table 8-1 and Figure 8-1 during this description.

8.2 MEMORY CONTROL FIELD (MC) - RD BITS 0, 1, 2, AND 3

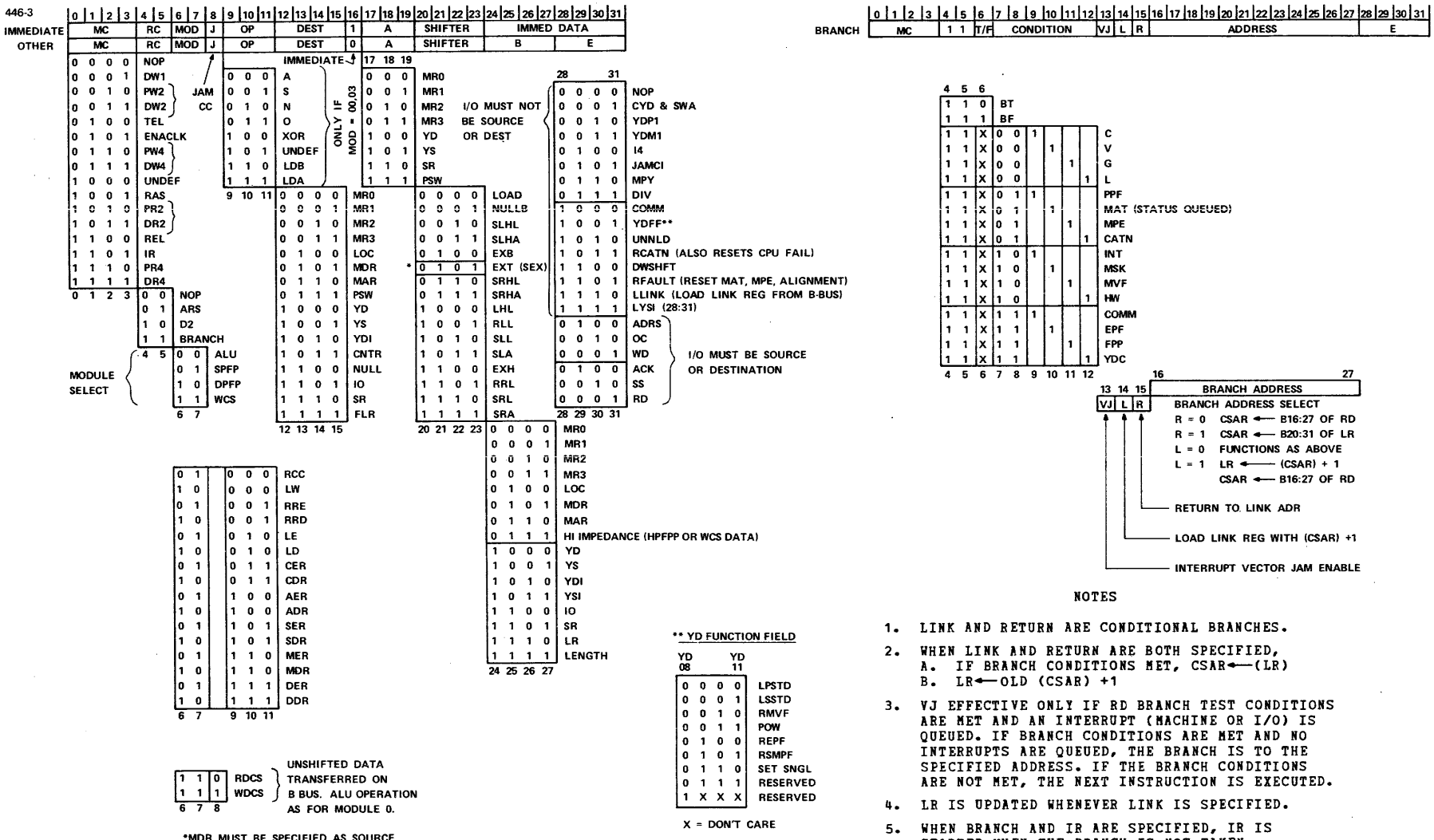
The Memory Control Field (MC) is primarily used either to read from, or to write into, memory. The memory address selected depends upon the contents of the Location Counter (LOC) (during IR only) or the Memory Address Register (MAR) and the bias added by the MAT. The type of memory operation (read or write) and the amount of data fetched is controlled by the MC. Privileged memory operations disable the relocation and protection of the MAT. Fullword memory operations must be aligned on fullword memory address boundaries. Halfword memory operations must be on halfword or fullword boundaries. Violation of these alignments causes alignment faults. All memory read operations access memory as a fullword. The MC causes the processor hardware to steer and load only the required portion of the data.

NOTE

All MC options which cause data to be written to main memory (with the exception of TEL) also cause the ECC bits, corresponding to the fullword receiving the data, to be updated.

TABLE 8-1 INSTRUCTION WORD FIELDS

FIELD	MEANING
A	Selects register to be used as first operand. Data is available on the A bus.
ADDRESS	Specifies branch address data to be loaded into the CSAR.
B	Selects register to be used as second operand. Data is available on the B bus.
COND	Specifies conditions tested for conditional branch.
D	Selects destination register to receive the result. Data is available on the S bus.
DATA	Specifies immediate data as second operand on B bus.
E	Specifies the extended options to be performed.
I	Enables loading of immediate data to the B bus. The data used is controlled by the D field.
J	Causes condition code to be updated, or controls data direction (read or write) when module 3 (WCS) is selected.
L	Causes the link register to be loaded with the address of the current microinstruction plus one.
R	Specifies that a branch to the address contained in the link register is performed if the specified branch conditions are met.
MC	Memory control field specifies type of memory operation.
MOD	Selects active CPU module(s) fixed-point ALU, floating-point processor, or Writable Control Store (WCS).
OP	Specifies the fixed-point or floating-point operation.
RC	Control store addressing and alternate register set control field.
SHIFTER	Specifies B bus shifter function.
T/F	Specifies whether COND must be true or false to branch.
VJ	Enables interrupt vector jam when branch is taken.
YDFF	Specifies extended operations addressed by the YD field of the instruction register and enabled by the E field.



NOTES

1. LINK AND RETURN ARE CONDITIONAL BRANCHES.
2. WHEN LINK AND RETURN ARE BOTH SPECIFIED,
   A. IF BRANCH CONDITIONS MET, CSAR←(LR)
   B. LR←OLD (CSAR) +1
3. VJ EFFECTIVE ONLY IF RD BRANCH TEST CONDITIONS ARE MET AND AN INTERRUPT (MACHINE OR I/O) IS QUEUED. IF BRANCH CONDITIONS ARE MET AND NO INTERRUPTS ARE QUEUED, THE BRANCH IS TO THE SPECIFIED ADDRESS. IF THE BRANCH CONDITIONS ARE NOT MET, THE NEXT INSTRUCTION IS EXECUTED.
4. LR IS UPDATED WHENEVER LINK IS SPECIFIED.
5. WHEN BRANCH AND IR ARE SPECIFIED, IR IS STARTED WHEN THE BRANCH IS NOT TAKEN.

Figure 8-1 Microword Format

NOTE

The E field, in formats other than register-to-register immediate data, identifies additional operations to be performed or options to the primary operation.

The MC field, in all formats, controls main memory accesses.

MC Value

0000 - NOP — No memory operation is attempted.

0001 - DW1 — Nonprivileged byte data write. Byte of data contained in the Memory Data Register (MDR) is written to the byte memory address specified by the MAR. Bits 16:31 of the MDR are gated to the memory bus. The data to be written must be in the appropriate byte position of the least significant halfword of MDR.

0010 - PW2 — Privileged halfword data write. Halfword of data contained in MDR bits 16:31 is written to the halfword specified by the MAR.

0011 - DW2 — The same operation as PW2, except that the MAR address may be relocated and/or protected by the MAT.

0100 - TEL — Test error logger operation causes a byte write operation to the address specified by MAR. Bits 24:31 of MDR are written into memory. The byte write is privileged and the error correction logic is disabled; thus, if the byte written is different from the previous contents, the Error Correction Code (ECC) in memory is incorrect. No error is logged in the error logger.

0101 - ENACLK — No memory operation is implied. Destination clocks for all machine registers (except YDI, flags, and CSAR) are disabled whenever a fullword or halfword boundary error, ECC error, or MAT violation occurs. To allow loading machine registers following such a condition, the ENACLK option must be specified.

0110 - PW4 — Privileged fullword memory write. The data contained in MDR 0:31 is written to the address specified by MAR.

0111 - DW4 — Nonprivileged fullword memory write. The relocation and protection of the MAT is enabled.

1000 - UNDEF The MC and the hardware are undefined.

1001 - RAS The halfword addressed by MAR is read into MDR, bits 16:31. Bit 16 of the data is set, and the halfword is written back to memory. The MAT is not disabled. The data in MDR, bits 16:31, reflects the previous state of the data in memory. Bits 0:15 of the MDR are undefined.

1010 - PR2 Privileged halfword read from memory. The MAT is disabled. A halfword of data selected by the address in MAR is loaded into MDR 16:31. Bits 0:15 of the MDR are undefined. The address is in the MAR.

1011 - DR2 Nonprivileged halfword read from memory. The MAT is enabled. Data is loaded into MDR in the same manner as PR2. The address is in the MAR.

1100 - REL Read error logger is treated as a PR2. The error logger, at the address corresponding to the contents of MAR, is interrogated. Error logger data replaces the contents of MDR bits 16:31. Bits 0:15 of the MDR are undefined.

1101 - IR Instruction read from memory. This operation causes a fullword read from memory. The data from the read is loaded into the instruction register and the MDR. The address is specified by the location counter. If CNTR contains a nonzero value, the IR is deferred until the CNTR equals zero.

1110 - PR4 Privileged fullword memory read operations. MDR bits 0:31 are loaded with the data read from the fullword address contained in the MAR. The MAT is disabled during the memory cycle.

1111 - DR4 Nonprivileged fullword memory read operation. Similar to PR4, except that the MAT is enabled.

8.3 ROM CONTROL FIELD (RC) - RD BITS 4 AND 5

00 - NOP — Normal operation microinstructions are fetched in sequential order. The CSAR is incremented by one, unless IR is specified in the MC field.

01 - ARS — Sequential order of microinstruction fetch is unaffected. The alternate register set is selected for use with a general register. The user-level machine has no access to this set of registers.

10 - D2 — Jam the address which is contained in Decoder ROM 2 (DROM2) into the CSAR. The address specified by DROM2 is controlled by the contents of the instruction register.

11 - BRANCH — Allows the CSAR to be jammed by RD bits 16:27 if conditions are met.

8.4 MODULE SELECT FIELD (MOD) - RD BITS 6 AND 7

00 - ALU — The microinstruction operation uses the fixed-point ALU and the fixed-point operation codes (RD bits 9, 10, and 11).

01 - SPFP — The microinstruction operation uses the High Performance Floating-Point Processor (HPFPP) for single-precision operations. Single-precision registers are used. The fixed-point ALU is conditioned to load the B bus to the S bus. The type of single-precision operation is defined by RD bits 9, 10, and 11.

10 - DPFP — The microinstruction operation uses the HPFPP for double-precision operations. Double-precision registers alone are affected by the operation. The fixed-point ALU is conditioned to load the B bus to the S bus. The type of double-precision operation is defined by bits 9, 10, and 11.

11 - WCS — The Writable Control Store (WCS) module is selected as a source or destination for data on the B bus. The fixed-point ALU is allowed to operate using the WCS data as B bus source data. RD bit 8 defines whether data is to be written or read from WCS.

8.5 JAM CONTROL - RD BIT 8

RD bit 8 is used to jam the flag register into the condition code portion of the PSW.

8.6 OPERATION INSTRUCTION WORD FIELD - RD BITS 9, 10, AND 11

Refer to Table 8-2 for fixed-point operations. These operations are also valid when the WCS module is selected. Tables 8-3 and 8-4 list the single-precision and double-precision floating-point operations, respectively.

TABLE 8-2 FIXED-POINT ALU OPERATIONS

RD BITS			MNEMONIC	MEANING
9	10	11		
0	0	0	A	Add the A bus and B bus shifter output data.
0	0	1	S	Subtract the A bus and B bus shifter output data.
0	1	0	N	AND the A bus and B bus shifter output data.
0	1	1	OR	OR the A bus and B bus shifter output data.
1	0	0	XOR	Exclusive-OR the A bus and B bus shifter output data.
1	0	1	UNDEF	Undefined operation
1	1	0	LDB	Load B bus shifter output data to S bus.
1	1	1	LDA	Load A bus data to the S bus.

TABLE 8-3 SINGLE-PRECISION FLOATING-POINT OPERATIONS

RD BITS			MNEMONIC	MEANING
9	10	11		
0	0	0	RCC	Read condition code - place contents of HPFPP flag register on B bus.
0	0	1	RRE	Read register single-precision and place contents on B bus.
0	1	0	LE	Load single-precision data from B bus to HPFPP.
0	1	1	CER	Compare single-precision data register-to-register.
1	0	0	AER	Add single-precision data register-to-register.
1	0	1	SER	Subtract single-precision data register-to-register.
1	1	0	MER	Multiply single-precision data register-to-register.
1	1	1	DER	Divide single-precision data register-to-register.

TABLE 8-4 DOUBLE-PRECISION FLOATING-POINT OPERATIONS

RD BITS			MNEMONIC	MEANING
9	10	11		
0	0	0	LW	Load word - load most significant 32-bit portion of 64-bit double-precision floating-point number.
0	0	1	RRD	Read register double-precision and place contents on B bus.
0	1	0	LD	Load least significant 32-bit portion of 64-bit double-precision floating-point number.
0	1	1	CDR	Compare double-precision register-to-register.
1	0	0	ADR	Add double-precision register-to-register.
1	0	1	SDR	Subtract double-precision register-to-register.
1	1	0	MDR	Multiply double-precision register-to-register.
1	1	1	DDR	Divide double-precision register-to-register.

8.7 DESTINATION INSTRUCTION WORD FIELD - RD BITS 12, 13, 14, AND 15

Result data on the S bus is loaded into the specified destination. (Refer to Table 8-5.)

TABLE 8-5 DESTINATION REGISTERS

RD BITS				MNEMONIC	MEANING
12	13	14	15		
0	0	0	0	MR0	Microregister 0
0	0	0	1	MR1	Microregister 1
0	0	1	0	MR2	Microregister 2
0	0	1	1	MR3	Microregister 3
0	1	0	0	LOC	Location counter
0	1	0	1	MDR	Memory data register
0	1	1	0	MAR	Memory address register
0	1	1	1	PSW	Program status word
1	0	0	0	YD or ARSYD	General register specified by YD field of IR
1	0	0	1	YS or ARSYS	General register specified by YS field of IR
1	0	1	0	YDI	YD field of IR
1	0	1	1	CNTR	Counter
1	1	0	0	NULL	No destination. Used when the HPFPP or WCS is the implied destination.
1	1	0	1	IO	Used for output I/O instructions
1	1	1	0	SR	Shift register
1	1	1	1	FLR	Flag register

8.8 IMMEDIATE DATA CONTROL BIT - RD BIT 16

Microinstructions other than Branch may use the immediate data control bit. When this bit is active, RD bits 24:31 provide the least significant eight bits into the B bus shifter. The remainder of the B source is null.

When the PSW is the destination, bits 28:31 of the S bus are captured in the Flag Register (FLR). The PSW condition code field is updated from the FLR only when the JAM option is specified in the microinstruction word.

When the destination is YD or YS, the general or scratchpad register whose number is in the YD or YS field of IR receives the S bus data. The current set is selected by bits 24:27 of the PSW. When module 1 or 2 is selected (by RD bits 6 and 7), the floating-point register specified by the YD field of IR receives the resultant floating-point data.

By specifying YDI as the destination, the YD field of IR is loaded from S bus bits 28:31. Microflags resulting from the operation are still valid in this case. YDI is also the destination for CYD&SWA, YDP1, and YDM1 E field options.

8.9 A SOURCE INSTRUCTION WORD FIELD - RD BITS 17, 18, AND 19

Refer to Table 8-6 for first operand registers. Data from the A source appears on the A bus input to the fixed-point ALU only.

TABLE 8-6 FIRST OPERAND REGISTERS (A BUS DATA)

RD BITS			MNEMONIC	MEANING
17	18	19		
0	0	0	MR0	Microregister 0
0	0	1	MR1	Microregister 1
0	1	0	MR2	Microregister 2
0	1	1	MR3	Microregister 3
1	0	0	YD or ARSYD	Register specified by YD field of IR
1	0	1	YS or ARSYS	Register specified by YS field of IR
1	1	0	SR	Shift register
1	1	1	PSW	Program status word

When module 0 or 3 is selected, use of YD or YS as a source causes the general or scratchpad register whose number is in the YD or YS field of IR to be presented to the A ALU input.

When module 1 or 2 is selected, the specified floating-point register is presented as the HPFPP first operand input.

8.10 SHIFTER INSTRUCTION WORD FIELD - RD BITS 20, 21, 22, AND 23

Refer to Table 8-7 for shifter options. The shifter alters B bus data according to the selected option. The modified data is supplied to the fixed-point ALU as second operand data.

TABLE 8-7 SHIFTER OPTIONS

RD BITS				MNEMONIC	ACTION
20	21	22	23		
0	0	0	0	-	No action - pass data unmodified.
0	0	0	1	NULLB	Force data to zero.
0	0	1	0	SLHL	Shift left halfword logical (bits 16:31) by one.
0	0	1	1	SLHA	Shift left halfword arithmetic (bits 16:31) by one.
0	1	0	0	EXB	Exchange bytes (least significant 16 bits).
0	1	0	1	EXT	Extend sign - MDR must be source.
0	1	1	0	SRHL	Shift right halfword logical (bits 16:31) by one.
0	1	1	1	SRHA	Shift right halfword arithmetic (bits 16:31) by one.
1	0	0	0	LHL	Load halfword logical.
1	0	0	1	RLL	Rotate left logical by one.
1	0	1	0	SLL	Shift left logical by one.
1	0	1	1	SLA	Shift left arithmetic by one.
1	1	0	0	EXH	Exchange halfwords.
1	1	0	1	RRL	Rotate right logical by one.
1	1	1	0	SRL	Shift right logical by one.
1	1	1	1	SRA	Shift right arithmetic by one.

8.11 B SOURCE INSTRUCTION WORD FIELD - RD BITS 24, 25, 26, AND 27

Refer to Table 8-8 for second operand register options. Second operand register data is propagated onto the B bus. The data is then passed through the shifter to the ALU.

8.12 E INSTRUCTION WORD FIELD - RD BITS 28, 29, 30, AND 31

Refer to Table 8-9 for the extended field options. The extended field provides the ability to extend the function of any microinstruction without requiring the use of a second microinstruction.

TABLE 8-8 SECCND OPERAND REGISTERS

RD BITS				MNEMONIC	MEANING
24	25	26	27		
0	0	0	0	MR0	Microregister 0
0	0	0	1	MR1	Microregister 1
0	0	1	0	MR2	Microregister 2
0	0	1	1	MR3	Microregister 3
0	1	0	0	LOC	Location counter
0	1	0	1	MDR	Memory data register
0	1	1	0	MAR	Memory address register
0	1	1	1	CBUS	Data bus from modules 1, 2, and 3
1	0	0	0	YD or ARSYD	Register specified by YD field of IR
1	0	0	1	YS or ARSYS	Register specified by YS field of IR
1	0	1	0	YDI	YD field of IR
1	0	1	1	YSI	YS field of IR
1	1	0	0	IO	Used for input I/O instructions
1	1	0	1	SR	Shift register
1	1	1	0	LR	Link register
1	1	1	1	LENGTH	Length in halfwords of last instruction fetched

TABLE 8-9 EXTENDED FIELD OPTIONS

NOTE

I/O is neither a source nor a destination.

RD BITS				MNEMONIC	MEANING
28	29	30	31		
0	0	0	0	-	No action
0	0	0	1	CYD&SWA	Clear YD field of IR and set wait indicator.
0	0	1	0	YDP1	Increment YD field of IR by one.
0	0	1	1	YDM1	Decrement YD field of IR by one.
0	1	0	0	I4	Increment the MAR by 4.
0	1	0	1	JAMCI	Jam carry in ALU (arithmetic mode only)
0	1	1	0	MPY	Multiply
0	1	1	1	DIV	Divide
1	0	0	0	COMM	Data on S bus is gated onto the I/O bus and accepted by the communication assist unit.
1	0	0	1	YDFF	YD function field
1	0	1	0	UNNLD	Unnormalized floating-point load - defeats HPFPP normalizing logic.
1	0	1	1	RCATN	Reset console attention and CPU fail indicator.
1	1	0	0	DWSHFT	Doubleword shift
1	1	0	1	RFAULT	Reset MAT, MPE, and ALIGN errors.
1	1	1	0	LLINK	Load link register from B bus bits 20:31.
1	1	1	1	LYSI	Load YS field of IR from S bus bits 28:31.
0	1	0	0	ADRS	I/O must be destination. ADRS selects device on the I/O bus.

TABLE 8-9 EXTENDED FIELD OPTIONS (Continued)

RD BITS				MNEMONIC	MEANING
28	29	30	31		
0	0	1	0	OC	I/O must be destination. Data on the I/O bus is command for selected device.
0	0	0	1	WD	I/O must be destination. Data on the I/O bus is character information for selected device.
0	1	0	0	ACK	I/O must be source. Interrupting device address is received.
0	0	1	0	SS	I/O must be source. The status data of a selected device is received.
0	0	0	1	RD	I/O must be source. Data is received from the selected device.

If the ARS bit is set in the RC field, all sources or destinations specifying YD or YS for module 0 or 3 operations access the alternate register set. This bit is set by the microcode assembler whenever ARSYD or ARSYS is specified in the microinstruction.

Specifying MDR as a source immediately following a memory read operation causes the processor to stop until memory data becomes available. After a fullword memory read, all 32 bits of MDR are loaded.

NOTES

EXT may be specified only if the B source is MDR.

If MDR is either the B source or the destination, EXB performs as follows:

- If MAR contains an even number, EXB occurs; otherwise, no EXB occurs.
- If MDR is specified as the destination register and MAR contains an even number, only MDR 17:23 is modified. If MAR contains an odd number, only MDR 24:31 is modified.

NOTES

Unless otherwise stated, extended field options shown in Table 8-9 may not be used when I/O is specified as either a source or a destination.

The POW command causes the system clear sense line to go inactive, thereby causing the signal SCLR0 to become active from the PSC. The entire system is consequently initialized.

The JAMCI option forces a carry-in of one to the least significant bit of the ALU. If the microinstruction is an add, the result on the S bus is one greater than the expected sum. If the microinstruction is a subtract, the result on the S bus is one less than the expected difference. If the microinstruction is neither add nor subtract, JAMCI has no effect.

The DWSHFT option causes SR to participate as the least significant 32 bits of the doubleword being shifted according to the B bus shifter option. The most significant 32 bits are supplied by the specified second operand register. The doubleword shifted result replaces the contents of the specified destination register (most significant 32 bits) and the shift register (least significant 32 bits).

- When YSI is specified as the B source and LYSI is specified as the E field modifier, the YS field of the instruction register increments by one, regardless of any other microword directive.

- Any fullword memory operation specified in the MC field (i.e., PR4, DR4, PW4, DW4), when specified with YDP1 or YDM1 as E field modifiers, causes an automatic I4 (causing the MAR to increment by X'4').

8.13 YD FUNCTION FIELD (YDFF)

The YD Function Field (YDFF) is an extension of E field operations. The YDFF functions are selected by the value in the YD field of the instruction register and are enabled by code X'9' - YDFF in the E field. Refer to Table 8-10 for YDFF operations.

TABLE 8-10 YD FUNCTION FIELD OPERATIONS

YDI				MNEMONIC	FUNCTION
08	09	10	11		
0	0	0	0	LPSTD	Load Process Segment Table Descriptor
0	0	0	1	LSSTD	Load Shared Segment Table Descriptor
0	0	1	0	RMVF	Reset Memory Voltage Failure Interrupt
0	0	1	1	POW	Power Down, Initialize
0	1	0	0	REPF	Reset Early Power Fail Interrupt
0	1	0	1	RSMPF	Reset Shared Memory Early Power Fail Interrupt
0	1	1	0	SETSNGL	Set the Single-Step User Instruction Interrupt
0	1	1	1	RESERVED	
1	0	0	0	RESERVED	
1	0	0	1	RESERVED	
1	0	1	0	RESERVED	
1	0	1	1	RESERVED	
1	1	0	0	RESERVED	
1	1	0	1	RESERVED	
1	1	1	0	RESERVED	
1	1	1	1	RESERVED	

8.14 DATA FORMATS

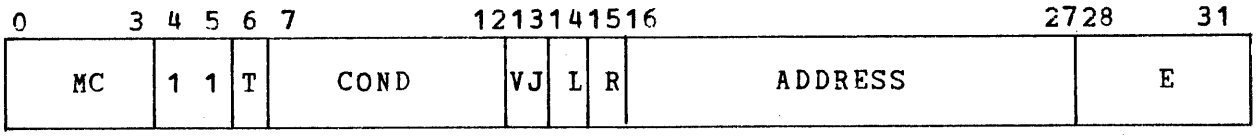
All internal data paths, except those to input/output control, are 32 bits wide. The basic machine operand is consequently a 32-bit fullword. Positive fixed-point data is expressed in true binary form with a sign bit of zero. Negative fixed-point data is expressed in two's complement notation with a sign bit of one. Floating-point data is expressed as a signed magnitude fraction with a biased exponent. The quantity expressed is the product of the fraction and 16 raised to the power of the exponent. Each single-precision floating-point number requires a 32-bit fullword; 8 bits are used for the fraction sign and exponent, and 24 bits are used for the fraction. Each double-precision floating-point number requires a 64-bit doubleword; 8 bits are used for the fraction sign and exponent, and 56 bits are used for the fraction.

Binary information is represented in hexadecimal notation (base 16) for simplicity.

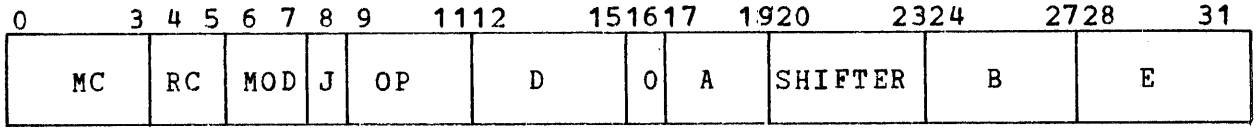
8.15 INSTRUCTION FORMATS

Microinstructions can be in any one of three formats designated Branch, Register-to-Register, and Register-to-Register Immediate. The instruction formats are shown in Figure 8-2.

BRANCH



REGISTER-TO-REGISTER



REGISTER-TO-REGISTER IMMEDIATE

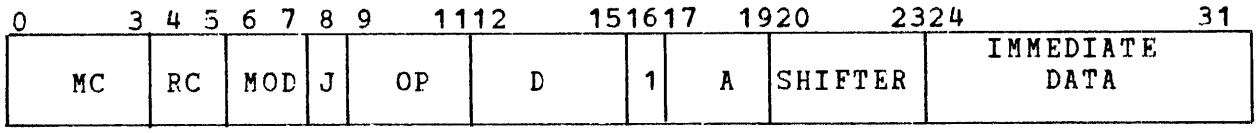


Figure 8-2 Instruction Word Formats

When the branch format is not specified by bits 4 and 5 of the microinstruction word being set, bits 6 and 7 select the processor module that performs the microinstruction. Module 0 is the internal fixed-point ALU. Module numbers 1 and 2 are directed to the optional High Performance Floating-Point Processor. Module number 1 identifies a single-precision operation, and module number 2 identifies a double-precision operation. Module 3 is the optional WCS. When module 3 is selected, module 0 also participates in the operation; thus, data contained in WCS can participate directly in a logical or arithmetic operation. The unshifted B operand for such an operation can be stored in a WCS location.

8.15.1 Branch

The specified condition(s) are matched against the corresponding machine state. If a match exists, the condition is true; if there are no matches, the condition is false.

The T bit in the branch formats specifies whether the true or false state of the conditions specified by the COND field is to be used. For example, if the condition is true and the T bit is one, or if the condition is false and the T bit is zero, a branch is executed by loading CSAR with the effective branch address.

If the L bit is set in the branch formats, the contents of CSAR are copied to the Link Register (LR), and the LR is incremented by one. If the branch conditions are met, the branch address is copied to CSAR. This is a Branch-and-Link operation.

If the R bit is set, the L bit reset, and branch conditions are met, the contents of LR are gated to CSAR, effecting a return from a prior Branch-and-Link operation.

If the L and R bits are both set and the branch conditions are met, a branch to the address specified by the contents of LR occurs, and LR is loaded with the address of the instruction following the branch instruction. This is a Branch-and-Link-Register operation, which may be useful for table-driven WCS routines.

The VJ bit enables direct-vectored hardware interrupts when set in the branch format. If the branch conditions are not met, no branch is taken, and VJ has no effect. If the branch conditions are met and VJ is set, one of eight distinct hardware interrupt vectors can become the branch address if a machine or I/O interrupt is queued. If no interrupt is queued, VJ has no effect, nor has it any effect on the loading of LR when the L bit is set. Refer to Table 8-11 for a description of the possible interrupt vectors. Interrupts have a priority reflected in the order of the vector addresses; the interrupt with the lowest vector address takes precedence over any other queued interrupt. The floating-point fault interrupt vector can be branched to only when a floating-point fault has occurred and the microword specifies an Instruction Read (IR) and a floating-point Read Condition Code (RCC).

TABLE 8-11 HARDWARE INTERRUPT VECTORS

VECTOR ADDRESS	INTERRUPT CAUSE
07	MAC or MPE error during instruction fetch, or illegal instruction detected
08	Alignment fault - halfword or fullword
09	MAT or MPE (noncorrectable memory error)
0A	Console attention, SNGL (single instruction cycle) or PPF
0B	EPF (Early Power Fail) or SEPF (Shared Memory Early Power Fail)
0C	I/O interrupt, ATN0
0D	I/O interrupt, ATN1
0E	I/O interrupt, ATN2
0F	I/O interrupt, ATN3
18	Floating-Point Processor Arithmetic Fault

8.15.2 Register-to-Register

These instructions combine a first operand register and a second operand register. The result is copied to one or two destination registers.

The OP field specifies the fixed-point or floating-point operation to be performed. The MOD field, in formats other than branch, acts as an extension to the OP field by causing the fixed-point ALU, optional HPFPP, or fixed-point ALU and optional WCS to be selected.

The J field (JAM) causes the PSW condition code field to be updated from the FLR. This bit has a special meaning when module 3 is specified.

The D field selects the S bus destination register; the A field selects the A input to the ALU; and the B field selects the B bus source.

The RC field (ARS) causes the scratchpad registers to be selected when YD or YS is the source or destination for modules 0 or 3.

The SHIFTER field selects the function to be performed by the B bus shifter.

8.15.3 Register-to-Register Immediate

These instructions are similar to the register-to-register format except that the second operand is taken from the least significant 8 bits of the microinstruction, known as the immediate DATA field. These 8 bits become the least significant 8 bits on the B bus. The remaining 24 bits are forced reset.

CHAPTER 9
CPU-A BOARD

9.1 INTRODUCTION

The main function of the CPU-A board is the control of the micromachine. Both Fixed Control Store (FCS) and the optional Writable Control Store (WCS), when equipped, are present on this board. In addition, the branch logic, interrupt support, and initialize control are contained on this board. Functional Schematic 35-767D08 should be referenced during this chapter.

9.2 CONTROL STORE

9.2.1 Control Store Address Register (CSAR)

The CSAR provides all of control store with the address of the next microinstruction to be fetched. The CSAR, a 12-bit up counter, is normally in the increment mode, addressing sequential microinstructions. When the microprogram specifies a D2, branch, calculate address (D1), or instruction read, the CSAR is loaded from its strobed 4-to-1 multiplexors (Sheet 2). The signals VSELA0, VSELB0, GDIR1A, and LDCSAR0 control the loading of the CSAR and steering for its multiplexors. Refer to Table 9-1 for the CSAR control line functions. The CSAR can be loaded from one of the four multiplexed inputs (two of which have steering of their own), or the outputs of the multiplexors can be disabled in order to load zeros on an instruction read. Refer to Figure 9-1 for a simplified block diagram of CSAR load sources. Figure 9-2 shows a flowchart which depicts the conditional loading of the CSAR. The CSAR can also be cleared to zero by System Clear (SCLR0D) for initialization or by FESCAP0, the resulting signal of a manual WCS escape operation.

The CSAR is loaded or incremented by the rising edge of RCLK1. When LDCSAR0 (3E4) is active, the CSAR is loaded on the rising edge of RCLK1; in all other cases it is incremented on this edge. Refer to Figure 9-3 for CSAR timing information.

TABLE 9-1 CSAR CONTROL LINE FUNCTIONS

CONTROL LINE				
LDCSAR0	GDIR1A	VSELB0	VSELA0	CSAR OPERATION
0	0	0	0	LOAD FROM LINK REGISTER
0	0	0	1	LOAD FROM RD 16-27
0	0	1	0	LOAD INTERRUPT VECTOR
0	0	1	1	LOAD DECODER ROM VECTOR
0	1	X	X	LOAD ZERO (INSTRUCTION READ)
1	X	X	X	INCREMENT CSAR

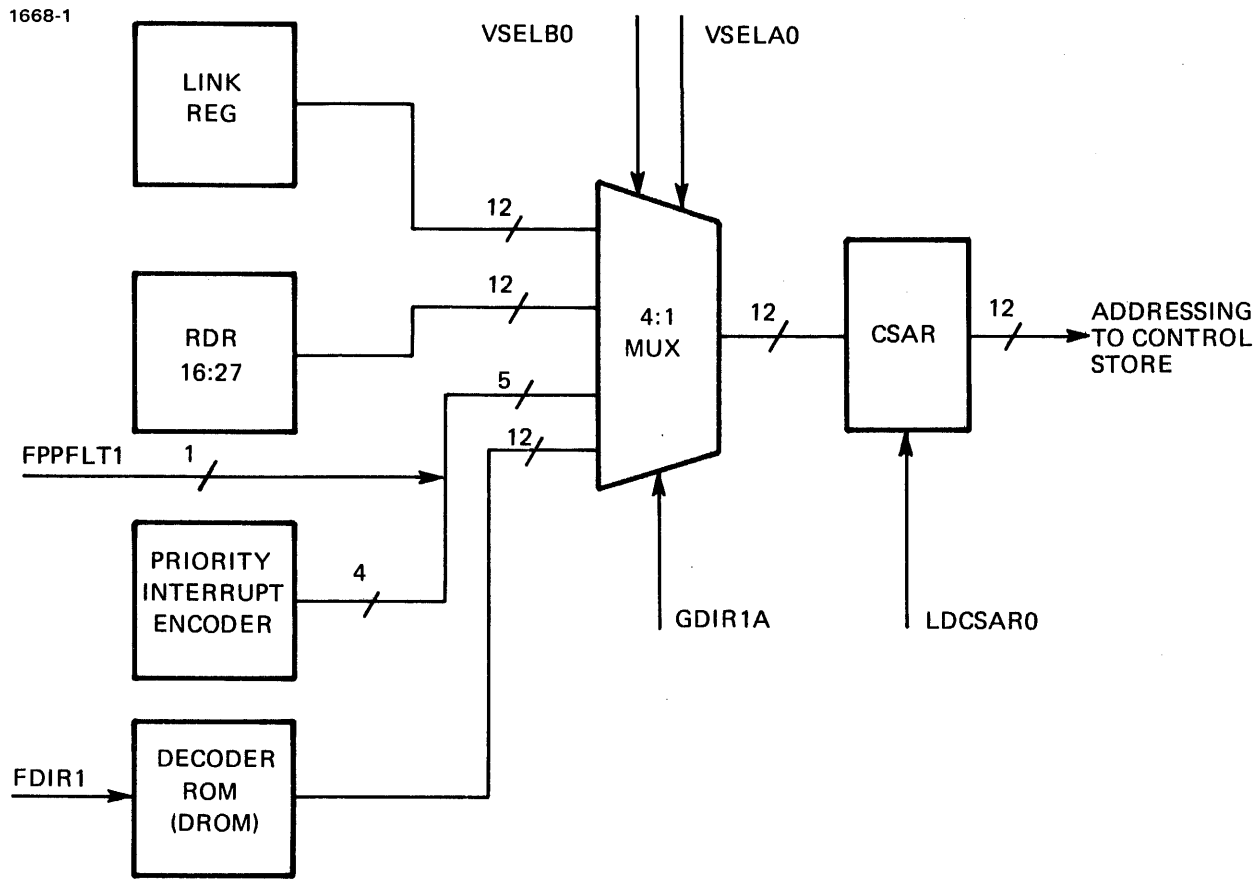


Figure 9-1 Simplified Block Diagram of CSAR Sources

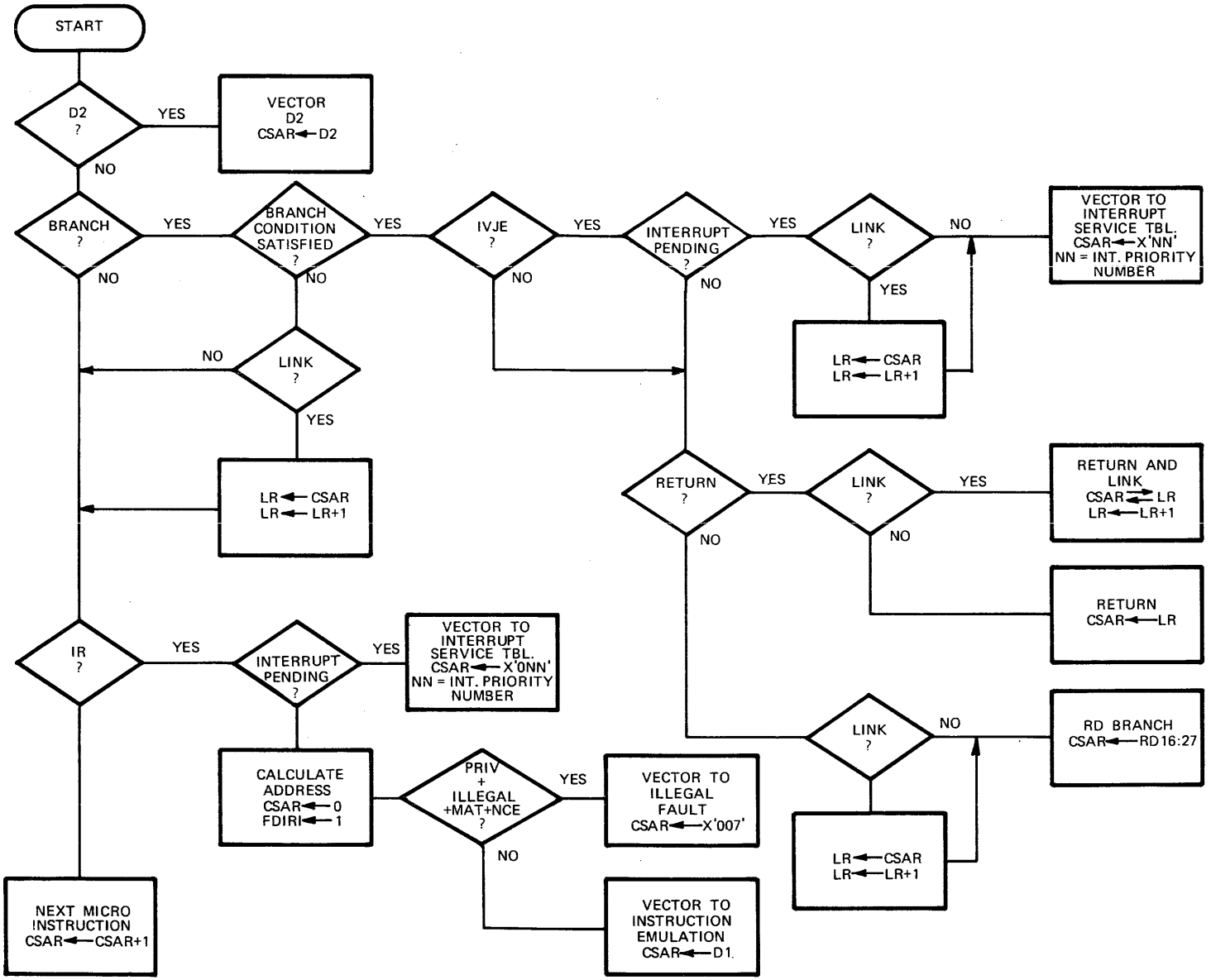


Figure 9-2 Flowchart of CSAR Loading and Microinstruction Sequencing

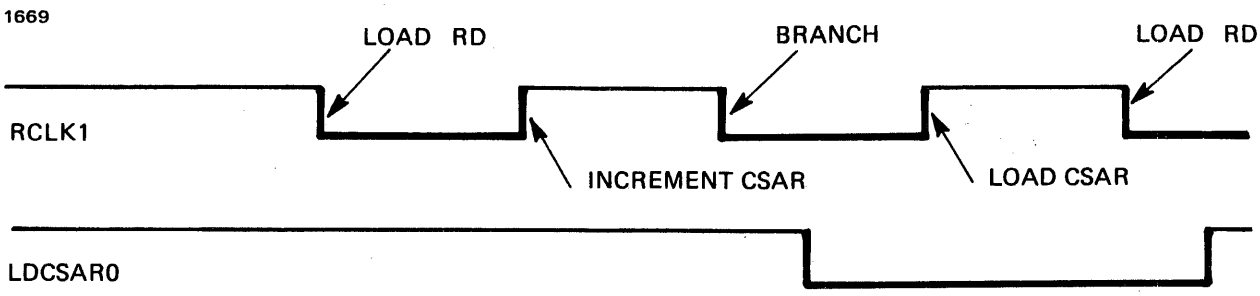


Figure 9-3 CSAR Timing

9.2.2 Link Register (LR)

The 12-bit Link Register (LR) (Sheet 3) provides the microprogram with a branch and link capability. In addition, it provides a means of branching to a calculated microprogram address and provides addressing for reading from or writing to the optional Writable Control Store (WCS). In a branch and link microinstruction, the LR is unconditionally loaded with the contents of the CSAR. The LR, a 12-bit up counter, is then allowed to increment by one, pointing to the microlocation immediately following the branch and link microinstruction. Timing for a branch and link microinstruction is illustrated in Figure 9-4. When a link is specified in the microprogram, gate 09E11 (3F5) goes high (a function of RD decoding), enabling gate 09D08 (3H7) to generate Link Register Clock (LRCLK0). LRCLK0 goes active twice during a link instruction. The first active condition performs a load from the CSAR, and the second active state increments the loaded quantity by one. LRCLK0 is generated by the following term:

LRCLK0=09E111•[(RCLK0A•SCLK0A)+(RCLK1•SCLK1)].

The low active load input to the LR, 09E080 (3H5), goes active during a register-to-register microinstruction specifying load link from the B bus via 09E09 (3H5) or a branch instruction specifying link 09E10 (3H5). Refer to Figure 9-5 for load timing. LDLR1 10D06 (3H4) active selects the CPU-B bus on the LR's input multiplexors and also generates LRCLK0 via 09D10 at RCLK1 time. The LR can be unloaded to the B bus via the multiplexors on Sheet 12. Refer to Section 9.2.4 for the LR's operation with WCS.

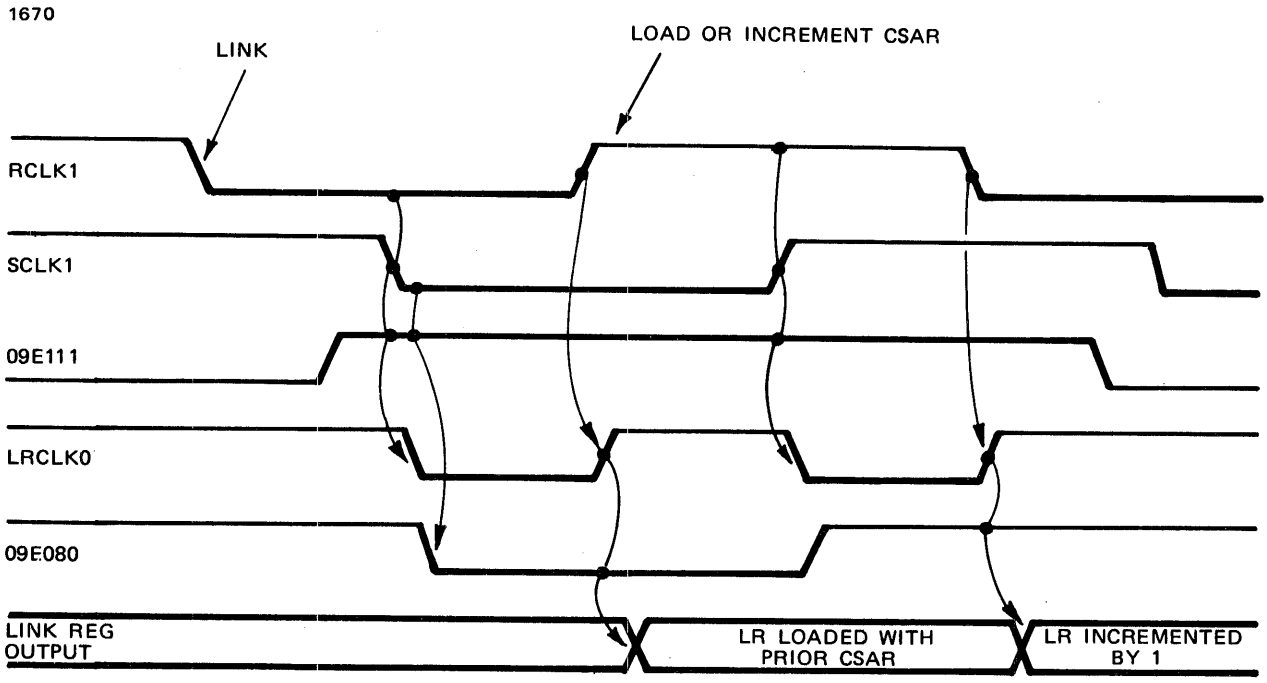


Figure 9-4 Link Register Timing for Branch and Link

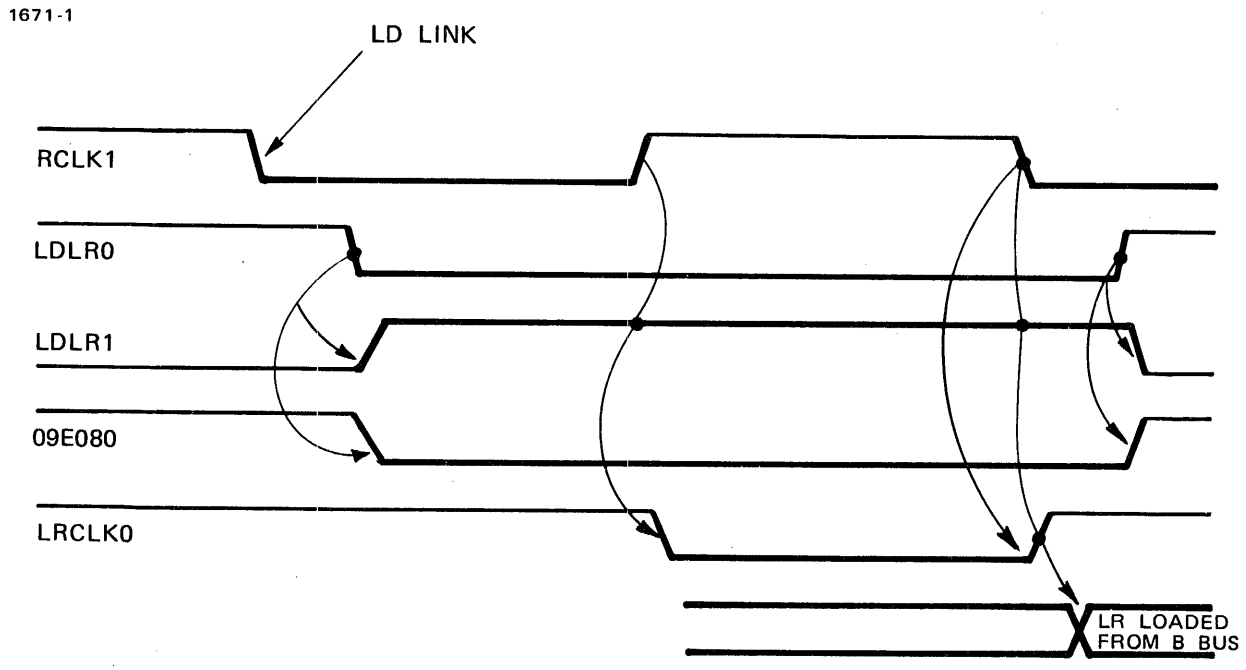


Figure 9-5 Link Register Load Timing

9.2.3 Fixed Control Store (FCS)

The Fixed Control Store (FCS) holds the processor emulator in high-speed ROM. FCS is organized as 2,048 words of 32 bits. Each 32-bit word represents one microinstruction. FCS is comprised of eight 1k x 8-bit ROMs and is divided into two pages, Page 0 and Page 1, both of which are addressed by the CSAR. These pages are selected by the two most significant bits of CSAR (CSAR201 and CSAR211) utilizing the ROM's low and high active Chip Enable (CE) inputs for chip select address decoding (Sheet 4 of schematics). Refer to Table 9-2 for control store addressing.

FCS is addressed by the CSAR which is settled no later than 13 ns after the rising edge of RCLK1. The FCS ROM should be settled a maximum of 70 ns after CSAR addresses are settled. FCS is input to the ROM Data Register (RDR), which is clocked by the falling edge of RCLK1 and requires an 8 ns set-up.

Figure 9-6 shows FCS timing. FCS is disabled during a WCS read or write operation by the signal WCSSEL0 (10K5). Refer to Section 9.2.4 for further information.

TABLE 9-2 CONTROL STORE ADDRESSING

CSAR 201	CSAR 211	CONTROL STORE ADDRESSES (HEX)	CONTROL STORE ENABLED
0	0	000 TO 3FF	PAGE 0 FCS
0	1	400 TO 7FF	PAGE 1 FCS
1	0	800 TO BFF	PAGE 0 WCS
1	1	C00 TO FFF	PAGE 1 WCS

1672

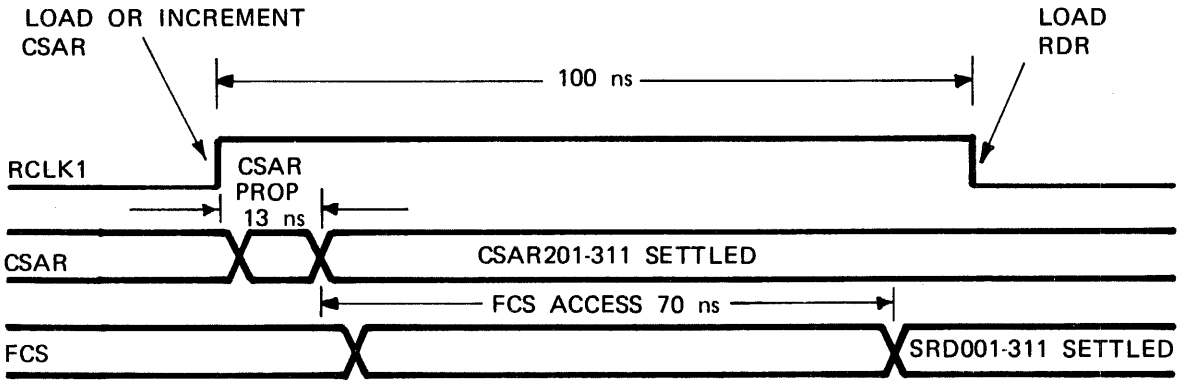


Figure 9-6 FCS Timing

9.2.4 Writable Control Store (WCS)

The WCS option, when equipped, provides the means for entering and executing user defined microinstructions. The WCS option is configured as 2,048 words by 32 bits held in volatile high-speed Random Access Memory (RAM), and operates as an extension of control store. The WCS option is composed of 64 1k x 1-bit RAMs (Sheets 5, 6, 7, and 8). Addresses to the WCS are multiplexed. In the execution mode, addressing is provided by the CSAR (WCSSEL0A=1) and microinstructions may be fetched from WCS when selected (refer to Table 9-2 for control store addressing). In the read or write WCS modes, WCSSEL0A (10K5) active, addressing is provided by the LR. Data is transferred to or from the B bus. The LR must be preloaded with the starting WCS address before a WCS transfer begins; it is automatically incremented upon completion of that transfer by the "WCS INC." term of IC 09D (3G7). A read or write WCS begins with WCS1 (10E4) going active. Refer to Figure 9-7 for WCS timing. WCS1 active and IC 10B06 high causes the WCS select flip-flop (IC 10B09,10) to set.

WCSSEL0 disables the FCS (Sheet 4) and WCSSEL1 (IC 10B09); enables the chip select steering to be a function of the LR; enables the WCS read clock (CKWCSR0) for read operations (RD080 inactive); and steers the WCS address multiplexors (Sheets 5 and 7) to select the LR inputs. A read or write WCS operation requires two CPU clocks. This is accomplished by activating option stop (OPSTOP0-10F3). OPSTOP0 generates an RSTOP0 on the CPU-D board, which prevents the generation of RCLK1. The input to the WCS skip clock flip-flop, IC 10B02, goes high at the beginning of a WCS read/write operation. The next rising edge of BCLK0 causes the output of the skip clock flip-flop, IC 10B06, to go low, forcing OPSTOP0 inactive and the input to the WCS select flip-flop low. The next rising edge of SCLK0A resets the WCS select flip-flop, completing the operation. All of the preceding timing description is common for a WCS read or write operation. The following paragraphs describe particulars for a Read or Write WCS.

Write WCS

The output of gate 09C03 (WCS1 ANDed with 10B06) is, in turn, ANDed with RD081, causing Write WCS (WWCS1) to go active. This signal and its complement, WWCS0, enable the data input buffers (Sheets 5, 6, 7, and 8) to the WCS RAM. The WCS Write Enables (WCSWE00 and WCSWE10) are generated by the following terms:

WCSWE00 = WCSCE01•WWCS1•SCLK1A•BCLK1A
WCSWE10 = WCSCE11•WWCS1•SCLK1A•BCLK1A

NOTE

WCSCE01 is the output of gate 07B03 (10L2). WCSCE11 is the output of gate 07B06 (10L3).

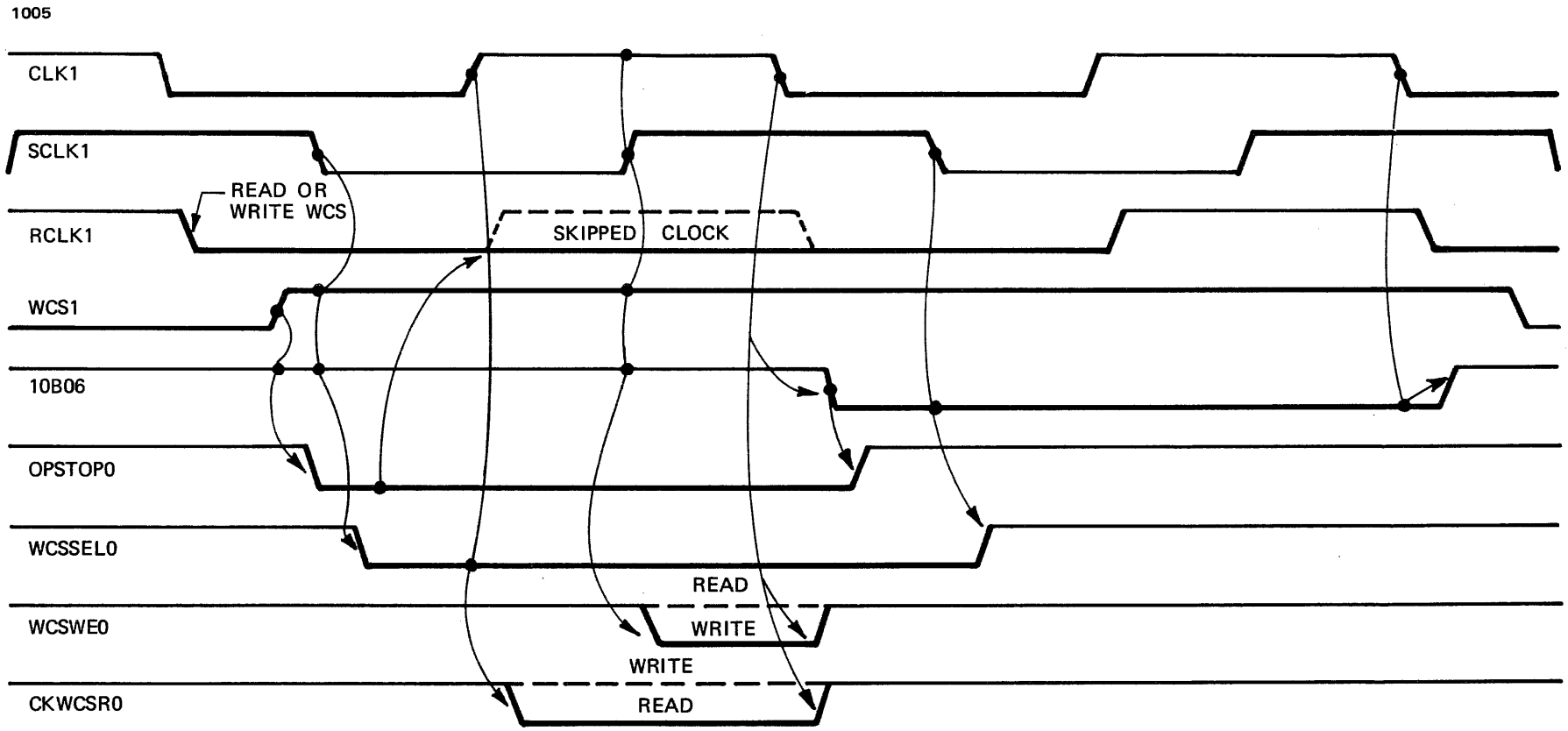


Figure 9-7 WCS Timing

Read WCS

The output of IC 10C06 (10B1) (WCS1 NANDed with RD080) is used to enable the four octal latches (ICs 11H, 11J, 14H, and 14J at schematic location 10A) to drive the B bus. These latches are clocked by the rising edge of the WCS read clock (CKWCSR0). CKWCSR0 is generated by the following term:

CKWCSR0=WCSSEL1•BCLK1A•$\overline{RD080}$.

If the microprogram is hung on a routine in WCS, due either to a programming error or a faulty WCS memory device, control can be returned to the System Control Terminal by placing the console in the single mode and depressing the HALT/EXE switch. This causes the CSAR to be cleared, FESCAP0 (3E8) active and forces the microprogram to enter the console service routine.

9.2.5 ROM Data Register (RDR)

The ROM data register latches the output of control store on a microinstruction fetch and presents its outputs to the processor as the ROM Data (RD) bus. (Refer to Sheet 9 of the schematics.) The four most significant bits of the RDR (RD001-RD031) are composed of J-K flip-flops and are clocked by the falling edge of RCLK1A. The remaining 28 bits (RD041:RD311) are composed of quad-D flip-flops and are clocked by the rising edge of RCLK0. (Refer to Figure 9-6, FCS Timing.)

On an initialize, the RDR is cleared by the ROM Data Clear signal (RDCLR0). RDCLR0 is the output of a cross-coupled latch (2K7) which is set by SCLR0D (Systems Clear) and remains set, holding the RDR cleared, until the CSAR increments to X'004'. RDCLR0 is reset when CSAR290 goes active.

9.2.6 Decoder ROM (DROM) and Privileged Illegal ROM (PILROM)

The DROM and PILROM provide the hardware with the calculate address (D1, D2), privileged and illegal instruction vector addressing for the Processor Emulator (05-090). Listings for the DROM and PILROM (and the format ROM on the CPU-D board) appear in the microprogram listing (05-090A13). Refer to Table 9-3 for an explanation of this data.

The DROM is organized as 512 words of 12 bits each and consists of three 512k x 4-bit high-speed ROMs (Sheet 10). The DROM is addressed by the 8-bit op-code field of the instruction register (IR000-IR070), located on the CPU-D board, and provides the D1 or D2 vector address to the CSAR multiplexor. FDIR1 (3K8) (decoded instruction read flip-flop) goes active on the first clock of an instruction fetch and is used as the most significant address of the DROM. When FDIR1 is active, D1 is selected; when inactive, the DROM outputs the D2 vector address. The 256 word by 4-bit PILROM has two functional variations, 19-188F25 (PILROM without WCS option) and 19-188F27 (PILROM with WCS option). (Refer to Table 9-3 for further information.)

TABLE 9-3 LISTING INFORMATICN FOR DROM, PILROMs AND FORMAT ROM

Refer to the listing of the Processor Emulator (05-090A13).

ADDRESS	DATA	DESCRIPTION
08NN	0000 XYYY	PIL, D1 VECTOR
09NN	0000 ZWWW	Format, D2 VECTOR

where: NN = IR001 - IR071, the 8-bit op-code field of the instruction register.

X = PRIV1, COMILL1, FLTILL1, and WCS, respectively, the output of the PILROM (see Note) in nexadecimal.

YYY = DD201 - DD311, the output of the decoder ROM's D1 vector in hexadecimal.

WWW = DD201 - DD311, the output of the decoder ROM's D2 vector in hexadecimal.

Z = RX1, RI20, RXRX1, and RR1, respectively, the output of the CPU-D format ROM in hexadecimal.

NOTE

The listing (05-090A13) represents the 19-188F27 PILROM, for a WCS equipped CPU-A board. A non-WCS CPU-A board is equipped with the 19-188F25 PILROM which has the following differences underlined:

08E5	0000	<u>4</u>3B5	<u>ILEG</u>
08E8	0000	<u>4</u>3B7	<u>ILEG</u>
08E9	0000	<u>4</u>3B3	<u>ILEG</u>

The PILROM is addressed by the op-code field of the instruction register and its outputs are tested at D1 time (FDIR1 active) to determine whether the instruction is privileged, illegal, or a WCS operation. Refer to Sheets 3 and 10 of the schematics. Having passed all prior interrupt tests, the CSAR, at D1 time, is conditioned to load the D1 vector address, (i.e., LDCSAR0-active; VSELA0, VSELB0, and LDIR1A-inactive) unless one of the conditions listed in Table 9-4 causes an illegal fault. In the latter case, VSELA0 goes active and the CSAR is loaded from the priority interrupt encoder input. The priority interrupt encoder is jammed to X'007' by FDIR1 (Sheet 13), the illegal fault microprogram location.

The WCS Execute (WCSEX1) output of the PILROM goes active when an Enter Control Store (EDCS) or a Branch to Control Store (BDCS) user instruction is being executed. WCSEX1 is the input to the WCS Execute flip-flop which clocks FWCSEX1 active on the next rising edge of RCLK1. FWCSEX1 enables the CSAR to fetch microinstructions from the optional WCS.

TABLE 9-4 ILLEGAL FAULT CONDITIONS

Base Algorithm for VSELA0 at D1 time

$\underline{VSELA0} = FDIR1 \bullet [COMILL1 + FDIR1 \bullet PRIV1 \bullet PSW231 + FLTILL \bullet (\overline{FPP1} + FPP1 \bullet PSW131) + MATMPE0]$

EXPLANATION OF FAULT CONDITIONS

FAULT CONDITION	REASON
FDIR1•COMILL1	Illegal Instruction
FDIR1•PRIV1•PSW231	Privileged Instruction
FDIR1•FLTILL1•$\overline{FPP1}$	Illegal Floating-Point Instruction (HPFPP not equipped)
FDIR1•FLTILL1•FPP1•PSW131	Privileged Floating-Point Instruction
FDIR1•MATMPE0	Machine Malfunction

9.3 BRANCH LOGIC

The branch logic provides 16 testable conditions for microprogram decisions. These conditions are input to four 4-to-1 multiplexors with RD071 and RD081 controlling their select lines, breaking the conditions down into four groups of four conditions each (see Sheet 11). Furthermore, the outputs of the multiplexors are NORed, which allows more than one condition to be tested at a time by enabling or disabling individual multiplexors. Refer to Table 9-5, which shows the grouping of conditions and the controlling RD bits. A branch microinstruction begins with RD041 and RD051 active, causing BRANCH0 and its complement BRANCH1 to become active (see Sheet 3). The four multiplexor outputs are NORed with BRANCH0 to cause True Branch (TBRCH0) active when the selected condition(s) are true. RD061 determines whether a true branch (RD061 inactive) or a false branch (RD061 active) condition is specified. Load CSAR (LDCSAR0) is used to load the CSAR with the branch address. LDCSAR0 goes active on a branch by the following algorithms:

LDCSAR0=TRBRCH1+FBRCH1
True branch TRBRCH1=$\overline{\text{TBRCH0}}$•$\overline{\text{RD060}}$•BRANCH1
False branch FBRCH1=$\overline{\text{TBRCH0}}$•RD061

Vector selects A and B (VSELA0 and VSELB0), used to steer the CSAR input multiplexor, are affected by the following algorithms during a branch:

VSELB0=BRANCH1•GBRCH1•$\overline{\text{RD131•INT1}}$
$\overline{\text{GBRCH1}}$=$\overline{\text{TRBRCH1+FBRCH1}}$
$\overline{\text{VSELA0}}$=RD131•INT1•RD150•(RD060•TBRCH1•BRANCH1+TBRCH0•RD061)

A conditional return is specified during a branch when RD150 is active, which causes VSELA0 to be low. An Interrupt Vector Jam Enable (IVJE) may also be specified with a branch and is represented above as $\overline{\text{RD131•INT1}}$, IVJE inactive. IVJE is explained in Section 9.4.

TABLE 9-5 BRANCH CONDITION GROUPS

1886

	RD 061	RD 071 RD 081	RD 091 RD 101 RD 111 RD 121	CONDITION	DESCRIPTION
	0			BT	Branch True
	1			BF	Branch False
Group 1		0 0	1	C	Carry Flag
		↓	1	V	Overflow Flag
		↓	1	G	Greater Than Flag
		↓	1	L	Less Than Flag
Group 2		0 1	1	PPF	Primary Power Fail Interrupt
		↓	1	MAT	Memory Address Translator Interrupt
		↓	1	MPE	Noncorrectable Memory Error Interrupt
		↓	1	CATN	Console Attention Interrupt
Group 3		1 0	1	INT	Priority Encoder Interrupt Pending
		↓	1	MASK	User Branch
		↓	1	MVF	Memory Voltage Failure
		↓	1	HW	I/O Halfword Signal
Group 4		1 1	1	COMM	Communications Option Strap
		↓	1	EPF	Early Power Fail Interrupt
		↓	1	FPP	Floating-Point Processor Strap
		↓	1	YDC	Carry-out from YD Register

9.4 INTERRUPT SUPPORT

9.4.1 Priority Interrupt Encoder (PIE)

The Priority Interrupt Encoder (PIE) provides the microprograms with the means of handling interrupts in the order of their priority. Inputs provide 11 possible conditions. The PIE generates the vector address for the highest priority interrupt pending (if enabled) and jams the interrupt line (INT1) active (13H8). Refer to Table 9-6 for a listing of interrupt priorities and their resulting vector addresses. At calculate address time (D1 time), FDIR1 goes active and disables the priority encoder, jamming its output to X'007' which is used for the illegal fault vector.

External interrupts (ATN00-ATN30) are masked by certain PSW bits. Refer to Table 9-7 for external interrupt masking. A 256 x 4-bit ROM decodes the PSW mask bits and outputs external interrupt enable lines (13D6). A listing for the external interrupt mask ROM appears in Table 9-8.

TABLE 9-6 INTERRUPT PRIORITIES

INTERRUPTS (IN ORDER OF PRIORITY)	ACTIVE SIGNAL	MASK	ENTRY TO INTERRUPT SERVICE TABLE	ENTRY TO ILLEGAL FAULT SERVICE
Alignment Fault	ALGN0	None	008	Disabled
Noncorrectable Memory Error	FNCE0	PSW21	009	007
Memory Address Translator Fault	MAT0			
Primary Power Fail	FPPF1	None	00A	Disabled
Console Attention	CATN0			
Single Step	SNGL0			
Early Power Fail	FEPF1	PSW18	00B	
External Interrupt Level 0	ATN00	See Table 9-7	00C	
External Interrupt Level 1	ATN10		00D	
External Interrupt Level 2	ATN20		00E	
External Interrupt Level 3	ATN30		00F	
Illegal Instruction	COMILL1	None	Disabled	007
Privileged Instruction	PRIV1	PSW23		
Floating-Point Instruction	FLTILL1	PSW13		
Floating-Point Processor Arithmetic Fault	FPPFLT0	See Note	018	Disabled

NOTE

FPPFLT0 is enabled by an Instruction Read (IR) and Read Condition Code (RCC) from the HPFPP.

TABLE 9-7 EXTERNAL INTERRUPT MASKING

PSW BITS		
17	20	
0	0	All Levels Disabled
0	1	Higher Levels Enabled
1	0	All Levels Enabled
1	1	Current and Higher Levels Enabled

where the current level is a function of the currently active register set.

PSW BITS					EXTERNAL INTERRUPT ENABLED			
17	20	25	26	27	LEVEL 0	LEVEL 1	LEVEL 2	LEVEL 3
0	0	X	X	X	NO	NO	NO	NO
0	1	0	0	0	NO	NO	NO	NO
0	1	0	0	1	YES	NO	NO	NO
0	1	0	1	0	YES	YES	NO	NO
0	1	0	1	1	YES	YES	YES	NO
0	1	1	0	0	YES	YES	YES	YES
0	1	1	0	1	YES	YES	YES	YES
0	1	1	1	0	YES	YES	YES	YES
0	1	1	1	1	YES	YES	YES	YES
1	0	X	X	X	YES	YES	YES	YES
1	1	0	0	0	YES	NO	NO	NO
1	1	0	0	1	YES	YES	NO	NO
1	1	0	1	0	YES	YES	YES	NO
1	1	0	1	1	YES	YES	YES	YES
1	1	1	0	0	YES	YES	YES	YES
1	1	1	0	1	YES	YES	YES	YES
1	1	1	1	0	YES	YES	YES	YES
1	1	1	1	1	YES	YES	YES	YES

X = Don't Care

TABLE 9-8 LISTING FOR ROM IC 19-142F44 EXTERNAL INTERRUPT MASK ROM

ADDRESS	DATA	ADDRESS	DATA	ADDRESS	DATA
00	0	10	F	20	Not Used, Should be Zero
01	0	11	F	•	
02	0	12	F	•	
03	0	13	F	FF	
04	0	14	F		
05	0	15	F		
06	0	16	F		
07	0	17	F		
08	0	18	8		
09	8	19	C		
0A	C	1A	E		
0B	E	1B	F		
0C	F	1C	F		
0D	F	1D	F		
0E	F	1E	F		
0F	F	1F	F		

All data in hexadecimal

9.4.2 Interrupt Vector Jam Enable (IVJE)

The IVJE logic provides the microprogram with a conditional vectored branch capability for interrupt handling. The microprogram can enable the IVJE logic with a branch IVJE microinstruction. A branch microinstruction enables IVJE by setting RD151. In this case, a 2-way branch is possible. If the branch condition is satisfied (GBRCH1 active), and INT1 (interrupt) is active, the CSAR loads from the priority interrupt encoder and a branch is taken to the Interrupt Service Table, X'008-00F', (refer to Figure 9-2). If the branch condition is satisfied and INT1 is not active, the CSAR loads the RD branch address (Sheet 2). If the branch condition is not satisfied, the CSAR does not load (LDCSAR0-inactive, 3E5), INT1 is ignored, and the CSAR increments to the next sequential microprogram address. An instruction read microinstruction enables IVJE automatically. INT1 active jams GDIR1 and GDIR1A inactive, aborting the Instruction Read; the CSAR loads from the priority interrupt encoder causing a branch to the Interrupt Service Table. If INT1 is inactive, GDIR1 and GDIR1A go active, beginning an Instruction Read.

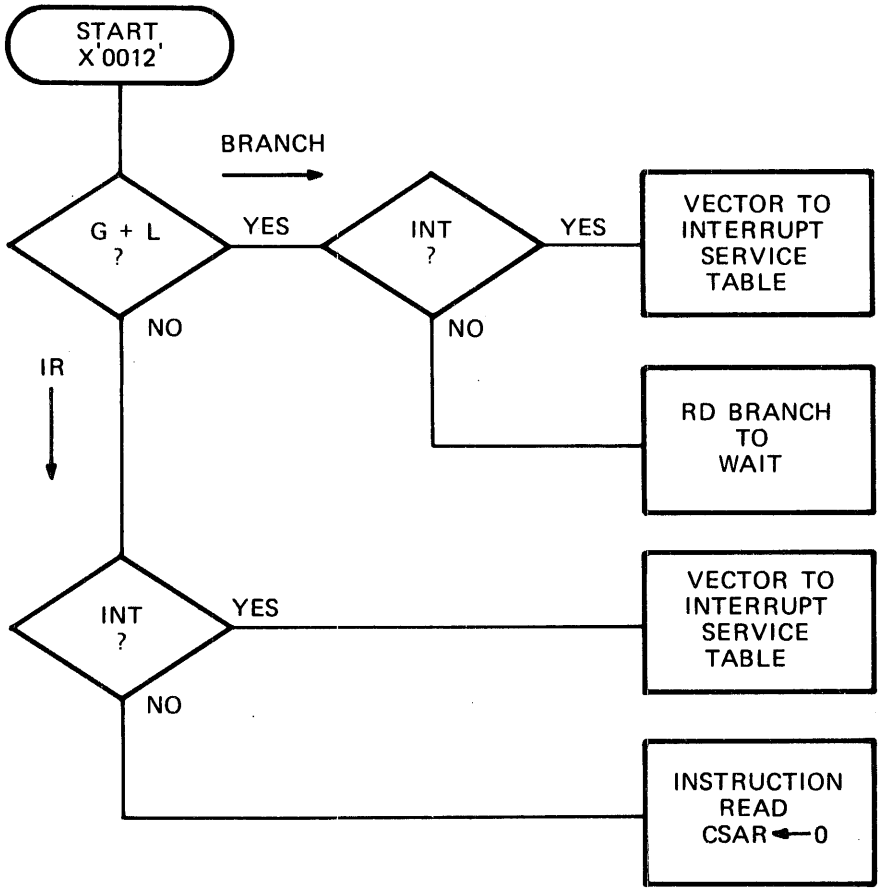
Branch IVJE and IR may be specified in the same microinstruction. Refer to Figure 9-8 for an example of this condition.

```
                    130  * ************************************************              32251300
                    131  *                                                             32251310
                    132  *         INTERRUPTIBLE WAIT LOOP                             32251320
                    133  *                                                             32251330
                    134  * ************************************************              32251340

0011  002C F480     136  TWAIT    NI     NULL,PSW,'80',EXB   TEST PSW B16:            32251360
0012  0C1C 0121     137  WAIT     BT     G+L,WAIT,CYC&SWA+IVJE+IR WAIT IF SET; ELSE EXIT.  32251370

0013  006C 0050     139  EXIT     L      NULL,MDR,IR         GLOBAL EXIT.            32251390
                    140  *                                  IF MEMORY READING AT TERMINATION,  32251400
                    141  *                                  FAULTS LEFT QUEUED UNTIL IR.  32251410
                    142  * ************************************************************  32251420
```

1674-1



CONTROL LINE

INT1	GBRCH1	TRBRCH1	LDCSAR0	VSELA0	VSELB0	GDIR1(A)
A	A	A	A	A	N	N
N	A	A	A	N	A	N
A	N	N	A	A	N	N
N	N	N	A	X	X	A

A = ACTIVE
N = NOT ACTIVE
X = DON'T CARE

NOTE: THIS EXAMPLE IS EXTRACTED FROM THE PROCESS EMULATOR - 05-090.

Figure 9-8 Example of a Branch with IVJE and IR

9.5 INITIALIZE CONTROL

The initialize control logic provides the processor with an orderly shut-down and restart capability. System initialization is performed as a result of one of the following conditions:

1. Placing the System Control Panel STANDBY-ON-LOCK switch in the STANDBY position,

2. Operating the System Control Panel INITIALIZE switch,

3. Power Fail Detect (PFDT0) activated by an external source, such as the watchdog timer or the Loader Storage Unit (LSU),

4. PFDT0 activated by the Power Subsystem Controller (PSC) as a result of AC or DC voltage fault,

5. Operating the MAINTENANCE RESET switch on the power system front panel, or

6. Command Power Down (POW0) executed by the microprogram.

The system initialization logic interfaces with the PSC through the following signals (refer to the CPU-A schematics, 35-767D08, Sheet 14):

1. NVM0 (Non-Valid Memory)
2. NVRS0 (Non-Valid Memory Reset)
3. PRDY1 (Power Ready)
4. SCLRS1 (System Clear Sense)
5. SCLR0 (System Clear)

The NVM0 signal is received by the processor on the Local Bank Controller (LBC) where it is buffered and gated with the nonconfigured memory signal and sent to the CPU-A as Gated Memory Voltage Failure (GMVF0-11B6). NVM0 is active, from the PSC, as a result of memory voltage (P5U) having gone out of regulation. This signal is a testable branch condition and is used by the microprogram during the power-up on initialize sequence, to determine a cold-start or warm-start condition.

The NVRS0 signal is a > 1.4 ms pulse to the PSC which causes the NVM0 signal to be reset.

The PRDY1 signal indicates the condition of all AC and DC voltages to the system. On powering up, PRDY1 is active > 100 ms after all DC voltages are in regulation and is inactive 3 ms minimum before DC voltages are out of regulation. (Refer to Figure 9-9.)

SCLRS1 is a command signal to the PSC which, when active, causes SCLR0 active.

9.5.1 Initialization

Refer to Figures 9-9 and 9-10 during this discussion.

Initialization is started by PFDT0 (14B5) active for one of the foregoing reasons. The cross-coupled latch at schematic location 14D5 latches and debounces PFDT0 and its output (IC 16S08) triggers the 1 ms power fail timer, IC 12S05. The leading edge of this pulse sets the Early Power Fail Flip-Flop (FEPF1) which, with PSW181 active, provides the processor with an Early Power Detect interrupt. (Refer to Section 9.4.1, Priority Interrupt Encoder.) The trailing edge of the 1 ms power fail timer pulse sets the Primary Power Fail Flip-Flop (FPPF1), which provides a nonmaskable interrupt to the microprogram.

Under normal operating conditions, the microprogram is interrupted by the Primary Power Fail (PPF) interrupt, performs its shut-down routine, and issues the command Power-Down (POW0). Command POW0 is then latched by the cross-coupled latch at schematic location 14C8 and input to the analog pulse stretcher comprised of three comparators in IC location 15S. The pulse stretcher passes the low input, forcing the transistor 14M (14L9) off, SCLRS1 active, and the PSC responds with SCLR0 active approximately 3 ms later. SCLR0 resets the cross-coupled latch at 14C8, causing the input to the analog pulse stretcher high. The pulse stretcher then delays that input 500 ms before deactivating SCLRS1.

If processor clocks are stopped (e.g., by the Test Aid), system initialization must be forced by placing the System Control Panel STANDBY-ON-LOCK switch in the STANDBY position, shutting off processor power (P5). This causes PRDY1 inactive from the PSC and causes SCLRS1 active by removing the base drive voltage from transistor 14M (14L9).

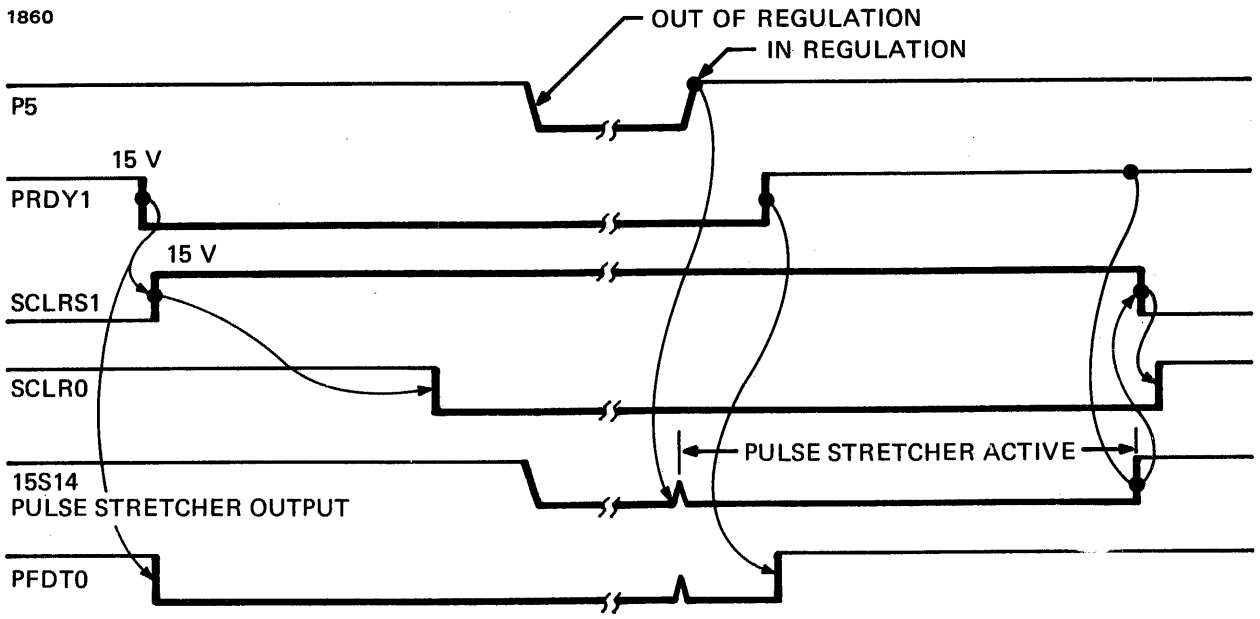


Figure 9-9 Power-Down, Power-Up Timing

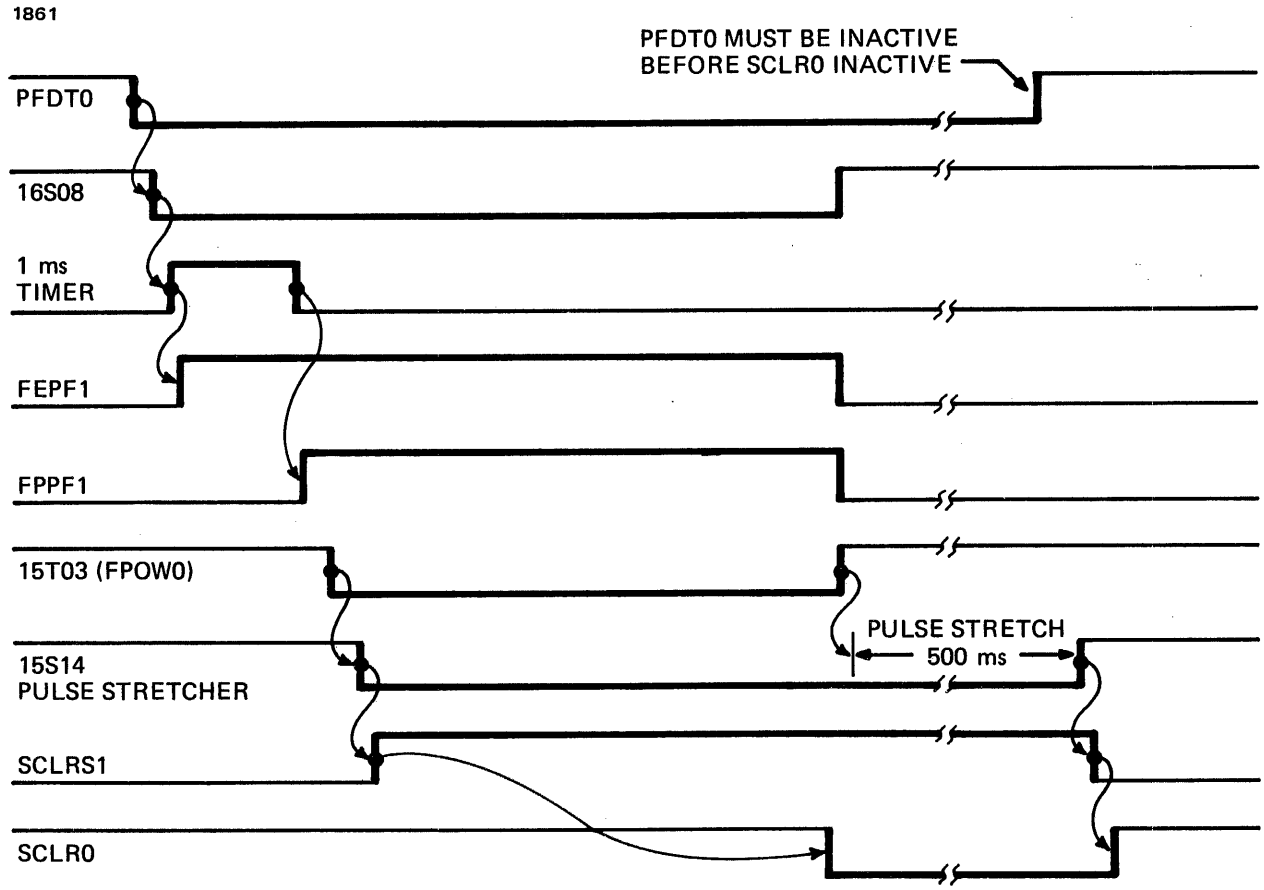


Figure 9-10 Initialize Timing

9.6 TEST AID

A Test Aid is provided on the CPU-A board which gives the customer engineer or technician the means for halting the microprogram or a SYNC pulse for troubleshooting. (Refer to Sheet 15 of the schematics.)

The Test Aid provides four switch selectable methods of halting the processor. The 16 DIP switches in the connector 5 location of the CPU-A board enable the four match conditions, as well as providing an input for the microaddress match/SYNC. A chart is provided at schematic location 15H1 which shows the switch functions. The external trap (EXTRAP0) condition is enabled by placing switch 1 in the ON position. Its input must be settled 20 ns before the falling edge of CLK1.

The second DIP switch causes the processor to halt whenever CSAR201 is active. This is provided to trap the microprogram whenever a WCS address is loaded in the CSAR. The single switch (switch 3) places the microprocessor in the single-step mode. In this mode, one microinstruction is executed each time the ADVANCE switch located on the CPU-D board is depressed.

The fourth switch enables the CSAR address match condition. Switches 5-8 and 1-8 on the right-hand DIP provide the address match information.

Any of the previously mentioned conditions, when enabled, cause TRAP0 to go active, signaling the CPU-D to halt clocks.

The SYNC (SYN0) output goes active when the match switches and the CSAR outputs are the same and BCLK0 is inactive, providing a low active pulse at the beginning of the selected microinstruction. This pulse may be used as SYNC input to an oscilloscope or logic analyzer.

9.7 MNEMONICS

The following is a list of mnemonics found on the CPU-A board. The meaning and the 35-767D08 schematic source of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AENH0	"A" enable high - used by CPU-B to control the most significant 16 bits of the A bus	13E4
AENL0	"A" enable low - used by CPU-B to control the least significant 16 bits of the A bus	13E5

MNEMONIC	MEANING	SCHEMATIC LOCATION
ALGNO	Alignment error signal from CPU-D that indicates an alignment fault has been detected	13E9
APSW281:311	Auxiliary PSW bits 28:31 - used by the branch logic to determine user mask match	11G8
ATN000:030	I/O attention lines - these are the four levels of I/O interrupts from the multiplexor bus.	13A7
B001:311	B bus bits 00:31 - B bus source data from the CPU-A	Sheets 5,6,7, and 8
BCLKO	Buffered clock	12D2
BRANCHO	Branch decoded from RD bits	3E4
BSTKSO	RD decoded output for the B stack latch on the CPU-B	13N4
CATN1	Console attention interrupt from the System Control Panel	11F4
CCATNO	RD decoded clear console attention	12J3
CKWCSRO	Clock writable control store register clock that latches the output of writable control store	10M5
CL070	Control line 7 - early indication of pending power failure provided for I/O devices	14F6
CLK1A	System clock net for CPU-A from the CPU-D board	12A2
CLKCCO	Clock condition code - used by the CPU-A to load the auxiliary condition code	11D9
CLKPSWO	Clock PSW - clock decoded by RD to load the PSW	13E3
COMILL1	Communication illegal - defines communication instructions option as being illegal	10K9

MNEMONIC	MEANING	SCHEMATIC LOCATION
COMM1	Strap option to allow the communication instruction package	11J2
CSAR200:310	Control store address register bits 20:31 - used to select words in control store	Sheet 2
DCLK0	Destination clock - clock used to load registers	12E4
DD201:311	Decoder read-only-memory data - data used to vector to instruction emulation routine	Sheet 10
DEXB0	RD decoded exchange byte for the CPU-C board	13N1
DEXT0	RD decoded sign extension - signal to CPU-C to perform sign extension on the MDR source	13E1
DFTEN0	RD decoded double-precision floating-point enable - optional High Performance Floating-Point Processor is conditioned for a double-precision operation.	13N9
DIR0	RD decoded instruction read - used to initiate instruction fetch and calculate address	3B5
DISA0	Disable A source data - generated on the CPU-D board during calculate address to inhibit data from the general register selected by the YS or X2 fields	13B5
DISB0	Disable B source data - generated on the CPU-D board during calculate address to inhibit data from the B source MDR	13J3
DISCS0	Disable control store	4B4
DISDRM1	Disable decoder read-only-memories	4B4
DIV0	RD decoded fixed-point divide operation	12J3
DSTOP0	Destination stop - inhibits the generation of destination clocks	12B4

MNEMONIC	MEANING	SCHEMATIC LOCATION
DWSHFT0	RD decoded doubleword shift - provides 64-bit shift capability	12L8
ENB0	Enable CPU-A board B bus sources	12L8
ENBS0	Enable B source data on the CPU-B board - gates bits 0:15 of the shift register or zeros onto the B bus	12L8
ENCSAR1	Enable control store address register - allows the CSAR to count up by one on each RCLK	Sheet 15
EXTRAP0	External trap - test feature provided to allow an external function tc cause the microprocessor to halt when the external event occurs	15C9
FCATN1	Flip-flops set side output of console attention	11H5
FDIR0	Flip-flop reset side output of gated decoded instruction read - set first clock after DIR if branch is not valid	3E8
FEPF1	Flip-flop set output of early power fail detections	14H1
FESCAP0	Flip-flop reset output of writable control store escape - provides the ability to escape from a hung WCS microprogram	3E8
FLR281:311	Output of the flag register used to be directly tested by the microcode or to be loaded into the auxiliary PSW	Sheet 11
FLTILL1	Floating-point instructions are illegal - Privileged/Illegal read-only-memory output that can force vector to illegal instruction	10K9

MNEMONIC	MEANING	SCHEMATIC LOCATION
FNCE0	Flip-flop reset output from CPU-D board which indicates that a double-bit error has occurred in local memory	11B2
FPPFLT0	Floating-point processor fault - indicates an arithmetic fault interrupt from the high performance floating-point processor	13A9
FPPF0	Output of the primary power failure flip-flop - the signal causes a testable branch condition to become valid, causing the microprogram to shut down.	11B2
FPP1	Strap option on the CPU-A that, depending on how it is strapped, indicates the presence, or lack of presence, of the high-speed floating-point processor	14H4
FSCATN0	Output of latch used to synchronize the console attention interrupt to the system clocks	11G3
FSMPE0	Output of latch used to delay the receipt of the double-bit error indication from the CPU-D	Sheet 3
FSPPF0	Output of latch used to delay the branch testability of the primary power failure flip-flop	11G2
FWCSEX1	Flip-flop output that indicates that a writable control store instruction is in process. This allows the upper page of control store to be WCS.	10M8
GBRCH1	Gated branch - this signal indicates that a branch occurs, regardless of whether it is a true or false branch.	11R3
GDIR0	Gated decoded instruction read - signal provided for the CPU-D board to indicate the start of an instruction fetch. Consists of RD decoded IR and branch not valid.	3E7

MNEMONIC	MEANING	SCHEMATIC LOCATION
GFLR291	Gated flag register bit 29 - flag register bit 29 (overflow) is ORed with the false SYNC timeout of the I/O system.	13N2
GRD091:111	Gated RD bits that control the type of operation to be performed by the fixed-point ALU. When floating-point operations are specified in the microinstruction, the ALU is forced into a load B operation. When the calculate address logic disables the B source, the ALU is forced into a load A operation.	13N2
GSNGL0	Gated single - the single cycle flip-flop output is gated by decoded instruction read.	11F5
HW0	Halfword I/O signal - when this signal is low, the currently selected I/O device provides for halfword data paths.	11B6
INT1	Interrupt pending - this signal is used by the CSAR control logic to force pending interrupt service.	13H8
IR000-IR070	Instruction register bits 0:7 - this is the user-level operation code portion of the Instruction Register. The DROM uses the op-code for vector address data.	Sheet 10
JAMCI0	Jam carry-in to the ALU on CPU-B board	12K2
LDCSAR0	Load the control store address register - the outputs of the CSAR multiplexors are loaded into the CSAR on the leading edge of RCLK.	3E5
LDIO0	RD decoded load I/O - used to disable E field decoding during I/O operations	13E2

MNEMONIC	MEANING	SCHEMATIC LOCATION
LDLR0	RD decoding of load link register - data in the B bus is loaded into the CSAR on the trailing edge of DCLK.	12J4
LFLR0	RD decoding of load flag register - signal generated by the CPU-B enables the flag register to load from the S bus.	13E3
LR201-LR311	Link register bits 20:31	Sheets 7, 10
LRCLK0	Link register clock - used to load and increment the link register	3J7
LSR0	RD decoded load shift register - the shift register on the CPU-B is the destination and is loaded with the data on the S bus.	13D2
MAT0	Signal supplied by the CPU-C board that indicates a MAT interrupt	11G3
MATMPE0	Logical OR of MAT interrupt and noncorrectable error interrupt - used to force interrupt vector	13E9
MAT201-MAT311	Test aid match data switches used to select CSAR address match	Sheet 15
MEXT0	Match external switch - allows the stopping of the micro-program because of an external event	15C8
MPY0	RD decoding of the E field specifying a multiply operation	12J3
MSK1	Branch mask valid - the ANDing of the PSW condition code and the YD field of IR has been satisfied. User instruction branch takes place.	11L7
MSNGL0	Test aid switch that allows the microprogram to be advanced one step at a time. Actual stepping is done on the CPU-D board.	15C8

MNEMONIC	MEANING	SCHEMATIC LOCATION
MVF0	Memory voltage failure - this signal is supplied by the LBC. During power up, it indicates that the Memory Voltage (P5U) went out of regulation (memory data is unreliable) or during normal operation MVF indicates, if NCE0 is also active, that nonpresent memory has been accessed.	11B6
MWCS0	Test aid switch that stops the microprocessor when CSAR20 becomes active. This occurs when fetching microinstruction from WCS.	15C8
NVRS0	Nonvalid memory reset - active low resets the nonvalid memory signal from the PSC.	14N4
OPSTOP0	Option stop signal caused by reading from or writing into WCS - this is supplied to the CPU-D and causes the microprogram to stop.	10G3
PFDT0	Power failure detected - caused by the power supply, INITIALIZE switch, or KEY switch. This signal causes the eventual shut-down of the processor.	14B5
POW0	RD decoding of the E and YDFF, indicating a command to power-down the processor	14D7
PRDY1	Power ready - high active ($\approx$15 V) all voltages ready and in regulation	14M7
PRIV1	Privileged instruction op-code is contained in the instruction register. This is an output of the PILROM.	10K9
PSW131:271	Program status word bits 13:27	Sheets 3, 13

MNEMONIC	MEANING	SCHEMATIC LOCATION
RCATN0	Reset console attention - part of the HALT/RUN switch on the System Control Panel. Controls console attention interrupt.	11B5
RCLK0	System clock that is allowed only when RSTOP is inactive - used to advance CSAR, load RD register, etc.	12D3
RD001:311	RD register data output bits 0:31 - this data represents the micro-instruction word.	Sheet 9
RDCLR0	RD register clear	9A2
REPF0	Reset early power fail interrupt	14E6
RSMINT0	Reset shared memory early power fail interrupt	14E5
RSTOP0	ROM stop - used to inhibit system clocks when necessary to prevent the incrementing or loading of the CSAR and RDR	12B2
SCATN0	Set console attention - part of the HALT/RUN switch on the System Control Panel. This controls the console attention interrupts.	11B5
SCLK1	Skewed system clock - this clock is delayed by 50 ns from the regular clock.	12B5
SCLR0	Systems clear - resets the processor and all devices	14B9
SCLRS1	System clear sense - high active ($\approx$15 V) causes system clear active from the PSC	14M8
SETSNGL0	Set single step - active low causes the single-step user instruction flop to be set.	14F7
SFTEN0	Single-precision floating-point operation enabled	13J3

MNEMONIC	MEANING	SCHEMATIC LOCATION
SH0	Shift - generated by the CPU-B board - disables the A bus multiplexor during multiply operations when a shift only is required	13B5
SMINT0	Shared memory early power fail interrupt	14F5
SNGL0 SNGL1A	Signals from the single switch on the System Control Panel - these signals cause the micro-program to cycle each user instruction and halt until HALT/RUN is depressed.	11B4 3B9
SR00:10	Shift register control signals - these signals are generated for the CPU-B to control shift register operations (load, shift right, shift left).	Sheet 13
SRD001:311	Source RD bits 00:31 - these are control store output signals that set or reset RD bits.	Sheet 5
SV0	Set overflow - generated by the I/O control logic on the CPU-D when a false SYNC timeout occurs.	13G2
SWA0	Set wait - decoded from the E field portion of the micro-instruction	12J2
SYN0	SYNC - test point which is activated each time a system clock occurs during the selected CSAR address match	15K5
TBRCH0	True branch - indicates the specified branch condition has been met	11R2
TRAP0	Trap - test aid signal indicating that the selected match function has been found. The CPU-D causes an RSTOP to occur when Trap is active.	15K6

MNEMONIC	MEANING	SCHEMATIC LOCATION
ULLR0	Unload link register - RD decoding of the link register as a source	12K6
ULSR0	Unload shift register - RD decoding of the shift register as a source; supplied to the CPU-B	12J6
UNNLD0	Unnormalized load - E field decoding of unnormalized load. The normalizing logic of the HPFPP is disabled.	12J3
UPSW0	Unload program status word	13D4
VECT01:31	Vector jam data lines - these lines are loaded into the least significant four address lines of the CSAR for interrupt service.	Sheets 2, 3
VSELA0 VSELB0	Data select lines on the 4:1 multiplexors that determine the source of data to be loaded into the CSAR	3L2 2B1
WAIT1	This signal is generated by the CYD&SWA E field option. When active, the WAIT indicator on the System Control Panel is illuminated.	14N2
WCS1	RD decoding of the module control field of the micro-instruction - when active, the WCS is the selected module.	10F3
WCSA00:90	Writable control store address selection lines - select a specific word in WCS	Sheets 5, 7
WCSCE00	Writable control store chip select control	5B7
WCSEX1	Decoder ROM output that indicates that a writable control store instruction is being executed	10L8
WCSSEL0	Writable control store selected	4B5

MNEMONIC	MEANING	SCHEMATIC LOCATION
WCSWE00	Writable control store write enable - used to write into WCS, Page 0	5B7
WCSWE10	WCS write enable used to write into WCS, Page 1	5B8
YD081:111	YD field of the instruction register - the YD field selects one of 16 general registers, normally used for a user instruction destination.	Sheet 11
YDC1	YD field carry - this signal indicates that the YD field is equal to X'F'.	11K5
YDFEN0	YD function enable - low active enables the YD function field decoder.	12J3

CHAPTER 10
CPU-B BOARD

10.1 INTRODUCTION

The CPU-B board contains the main Arithmetic Logic Unit (ALU), the register stack, the Program Status Word (PSW) register, the Flag Register (FLR), and a 32-bit Shift Register (SR). Logic is also located on this board to perform fixed-point multiply, divide, and shift operations.

All of the above functions are described in this chapter. The functional schematics for the CPU-B board, 35-768D08, should be used as a reference for this chapter.

10.2 INTERNAL PROCESSOR BUSES

Within the Central Processing Unit, data is transferred between the various registers of the processor over three distinct 32-bit buses. These are identified as the A bus, the B bus, and the S bus.

Data from the source registers, specified by the microprogram, is gated onto the A and B buses and presented to the B and A inputs of the ALU, respectively. The ALU, in turn, performs the operation specified by the microprogram. The result of that operation is formed at the outputs of the ALU and is called the S bus. Data on the S bus is loaded into the indicated destination register. The A and B buses are high impedance buses formed by devices with 3-state outputs. The only source on the S bus is the output of the ALU and is, therefore, driven by totem pole devices.

10.3 ARITHMETIC LOGIC UNIT (ALU)

The ALU section comprises a 32-bit parallel arithmetic/logic network using a fast look-ahead carry. The arithmetic or logical result, performed by the ALU network, is formed on the 32-bit S bus. Refer to the table on Sheet 14 of the functional schematics for information concerning the logical level of the select and mode inputs to the ALU integrated circuits for the functions used. Each ALU function used is described in the following paragraphs. All gate references are to the arbitrary labels on Figure 10-1.

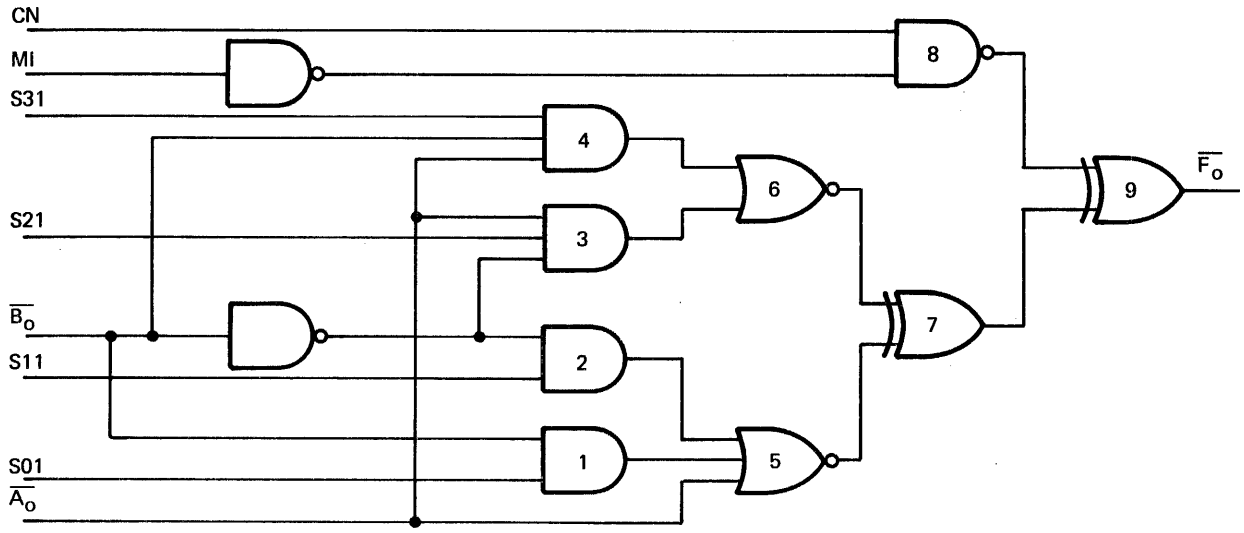


Figure 10-1 Least Significant ALU Stage

10.3.1 AND

The AND function, produced by the AND microinstruction, conditions the ALU to logically AND each bit from the output of the B bus shifter with the output of the A bus multiplexor. In this mode, the output equation for gate 5 is (Bo.Ao) and the output equation for gate 6 is (Ao). The simplified expression for the output from gate 7 is (Ao.Bo). Since gate 8 is disabled by the M1 input to the ALU, its output is high, causing the output from gate 9 to be defined by the same equation as the output from gate 7, the AND function.

10.3.2 OR

The OR microinstruction causes each bit from the output of the B bus shifter to be logically ORed with the corresponding bit from the gated output of the A bus multiplexor. Gate 5 produces a low because of the complementary Bo inputs. The outputs equation for gates 6 and 7 is (Ao+Bo) which corresponds to the $\overline{Fo}$ output from gate 9.

10.3.3 Exclusive-OR

The Exclusive-OR microinstruction produces a logical low at the S bus if the corresponding bits from the output of the B bus shifter with the output of the A bus multiplexor are at different logic levels. The expressions for the outputs from gates 5 and 6 are (Ao.Bo) and (AoBo), respectively. The function of the output from gate 7 is, therefore, $Ao\overline{Bo}+\overline{Ao}Bo$, the Exclusive-OR function. Since the output from gate 8 is again high, $\overline{Fo}$ is the same as the output from gate 7.

10.3.4 Add

The ALU is conditioned to the Add mode, an Add microinstruction. Note that with the exception of the M1 control line, Add is the same as Exclusive-OR. The M1 control line enables the Carry network internal to the ALU device so that the output from gate 8 is CN. The function, Fo, now becomes CN ($A_o\overline{B_o}+\overline{A_o}B_o$)+$\overline{CN}$ ($A_oB_o+A_oB_o$). Figure 10-1 shows only the least significant stage of the 19-067 4-bit ALU. The next three stages are identical except for the internally propagated carry.

10.3.5 Subtract

The Subtract function produced by the 4-bit ALU device is A-B-1. For this reason, the carry-in to the least significant stage is inverted by the Exclusive-OR gate (14C1) on a Subtract microinstruction. The output equation for gate 5 is ($A_o.B_o$) and the equation for gate 6 is ($A_o+\overline{B_o}$). Gate 7 produces a high output when the equation ($A_o.B_o+A_oB_o$) is satisfied. The output function, $\overline{F_o}$=CN ($\overline{A_oB_o}$)+$\overline{CN}$ ($A_oB_o+A_o\overline{B_o}$), yields A-B.

10.3.6 Load B

For the Load B operation, the ALU is conditioned to the F=A mode since the B bus shifter is tied to the A input to the ALU. In this mode, gates 1, 2, 3, and 4 are enabled by S01, S11, S21, and S31, respectively, and gate 8 is disabled by M1. Since both gates 1 and 2 are enabled, at least one of their outputs is high, producing a low at the output from gate 5. The state of gate 6 is the inverse of $\overline{A_o}$. If $\overline{A_o}$ is low, the output of gate 7 is high and the output of gate 8 is low ($\overline{F_o}$). For $\overline{A_o}$ high, the inverse is true at each stage, causing $\overline{F_o}$ to also be high. Therefore, in this mode, the state of $\overline{F_o}$ is the same as the state of $\overline{A_o}$, independent of the $\overline{B_o}$ input. The state of the gated B bus is passed, unmodified, to the S bus.

10.3.7 Load A

During a Load A, the ALU is conditioned to the F=B mode since the A bus is tied to the B inputs to the ALU. In this mode, gates 1 and 3 are disabled, gates 2 and 4 are enabled, and gate 8 is disabled by M1. If the $\overline{B_o}$ input is low, the output of gate 5 is low and the output of gate 6 is high, causing two highs at the inputs to gate 9 and a low at $\overline{F_o}$. When $\overline{B_o}$ is high, the inputs to gate 7 are equal (both low if $\overline{A_o}$ is high or both high if $\overline{A_o}$ is low), causing $\overline{F_o}$ to follow $\overline{B_o}$.

10.4 REGISTERS

10.4.1 Register Stack

The 8 sets of 16 user general registers, 4 microregisters used by the microprogram, and the 16 auxiliary registers used for interruptible instructions are all located in the register stack (Sheets 8, 9, 10, and 11).

The register stack is actually comprised of two separate stacks with common inputs and independent outputs forming a dual output port stack. Any of the registers may be accessed on the A stack, independent of the register specified on the B stack. Since the inputs to the A stack and B stack are common, the corresponding registers in each half contain identical information.

Data inputs to the register stack (DIN000-DIN310) are generated from 2:1 multiplexors (Sheets 8 and 9). In the normal mode, these multiplexors are conditioned to select the S bus data. The only exception to this is during a divide operation. (Refer to Section 10.6.) The outputs of the register stack are stored by transparent octal latches. During the read mode, READOA and READOB inactive (6H5), these latches are in the transparent mode. The outputs follow the inputs. When READO goes active, the data present at the inputs becomes latched. (Refer to Figure 10-2.)

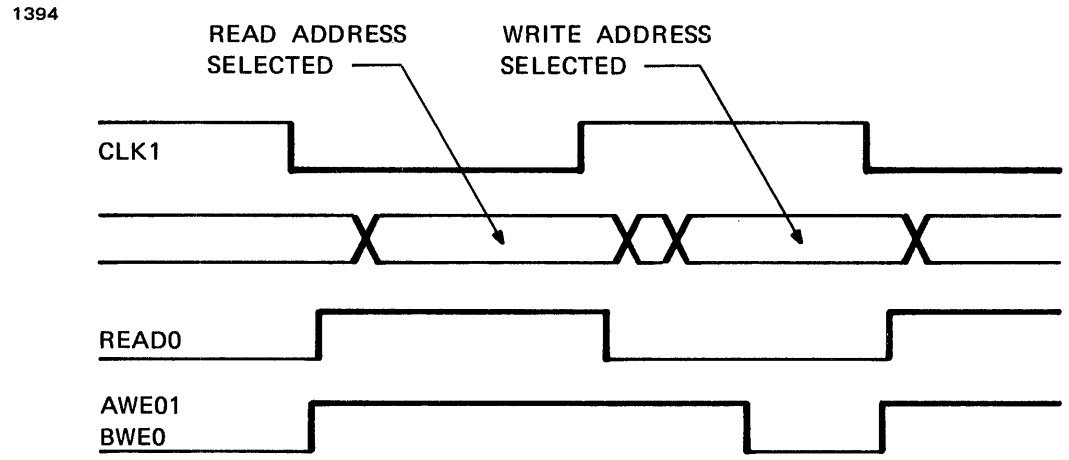


Figure 10-2 Register Stack Timing

The address and chip select inputs to the register stack are generated on Sheets 6 and 7 of the functional schematics. The functions are decoded separately during the read and write portions of the cycle using AND/NOR gates, so that different registers within the stack may be accessed and modified for a single microinstruction. Refer to the table on the upper right-hand quarter of Sheet 7 for information on the logic levels of the various address lines for the specific register being used.

10.4.2 Shift Register

The Shift Register (SR), located on Sheet 12, is a 32-bit register which may be used as a general purpose register by the microprogram, or may operate in either a shift right mode or a shift left mode for multiply and divide operations (refer to Sections 10.5 and 10.6). The SR is also used in conjunction with the B bus shifter for 64-bit shift operations. Refer to the table on Sheet 12, location S8, for information on the logical states of the select inputs for the various modes of operation for the shift register.

The decoding for the mode select inputs to the SR is located on the functional schematics for the CPU-A board, 35-767D08, Sheet 13.

10.4.3 Program Status Word (PSW) Register

The Program Status Word (PSW) register contains the status portion of the user's PSW. The status portion of the PSW is 32 bits long. Only 24 bits, however, are implemented in the hardware of this machine. PSW bits 00:07 are forced to appear reset when the PSW is unloaded.

The PSW, located on Sheet 13 of the functional schematics, is constructed using 19-231 integrated circuits. This device is a 4-bit edge-triggered latch with both totem pole (Q) and tri-state (Y) outputs. The Y outputs are used to form the A bus while the Q outputs are used for decoding functions.

Bits 08:27 are loaded on the trailing edge of CLK1 from the S bus when PSW is the selected destination register (CLKPSW0 active). The condition code portion of the PSW, bits 28:31, is copied from the flag register on the leading edge of the next SCLK1 after jam condition code is specified by the microprogram (CLKCC0 active). The tri-state outputs of the PSW are enabled when PSW is the selected A bus source, 03T03 low (13E9).

10.4.4 Flag Register (FLR)

The Flag Register (FLR) (Sheet 15) is a 4-bit register which contains additional information about the last logical or arithmetic microinstruction. The FLR contains the Carry flag (C), the Overflow flag (V), the Greater Than flag (G), and the Less Than flag (L).

The FLR is loaded from the S bus whenever either the FLR or the PSW register is specified as a destination. The contents of the FLR are copied into the CC when Jam CC is specified. The outputs from the FLR are also used by the branch circuit for conditional branches.

On any microinstruction other than a branch, and if the FLR and PSW are not the specified destination registers, the FLR is modified as follows:

1. Carry Flag - The C flag sets on an add operation if the carry-out of the ALU look-ahead carry circuits (CARRY1) (2B9) is active, or on a subtract operation if CARRY1 is inactive. The C flag is modified on shift operations according to the state of the B bus bit indicated in Table 10-1. The C flag sets if the corresponding B bus bit is set and resets if the B bus bit is inactive. For all other cases, the C flag is reset.

TABLE 10-1 SHIFT TABLE

OPERATION	B BUS BIT
Shift left halfword logical (16 bits)	B161
Shift left halfword arithmetic (16 bits)	B171
Shift left logical (32 bits)	B001
Shift left arithmetic (32 bits)	B011
Shift right halfword logical (16 bits)	B311
Shift right halfword arithmetic (16 bits)	B311
Shift right logical (32 bits)	B311
Shift right arithmetic (32 bits)	B311

2. Overflow Flag - The V flag is set on an Add if:

   - the B bus number sign is positive, and if the B bus sign is the same as the A bus sign and the resulting sign (S bus) is negative.
   - the B bus number is negative, and if the B bus sign is the same as the A bus sign and the result is positive.

   This flag is also set on a Subtract operation if the B bus sign is positive and the signs of the B bus and A bus differ and the result sign is negative, or if the sign of the B bus is negative and the B and A bus signs differ and the result is positive. For all other combinations of A, B, and S bus signs on Add and Subtract, the V flag becomes reset.

3. Greater Than and Less Than - The G flag is set if the result of the operation is not zero and the sign bit is not set. (For fullword operations (32-bit), the sign bit is S001; for halfword operations (16-bit), the sign bit is S161.) The L flag is set if the sign bit is active. Either flag is reset if its corresponding conditions are not met.

10.5 MULTIPLY OPERATIONS

Since a signed multiply algorithm is used, no special set-up is required for the operands. (Refer to Figure 10-3.) During a multiply, the ALU is conditioned to the Add mode and the B bus shifter and SR are conditioned to the shift right mode.

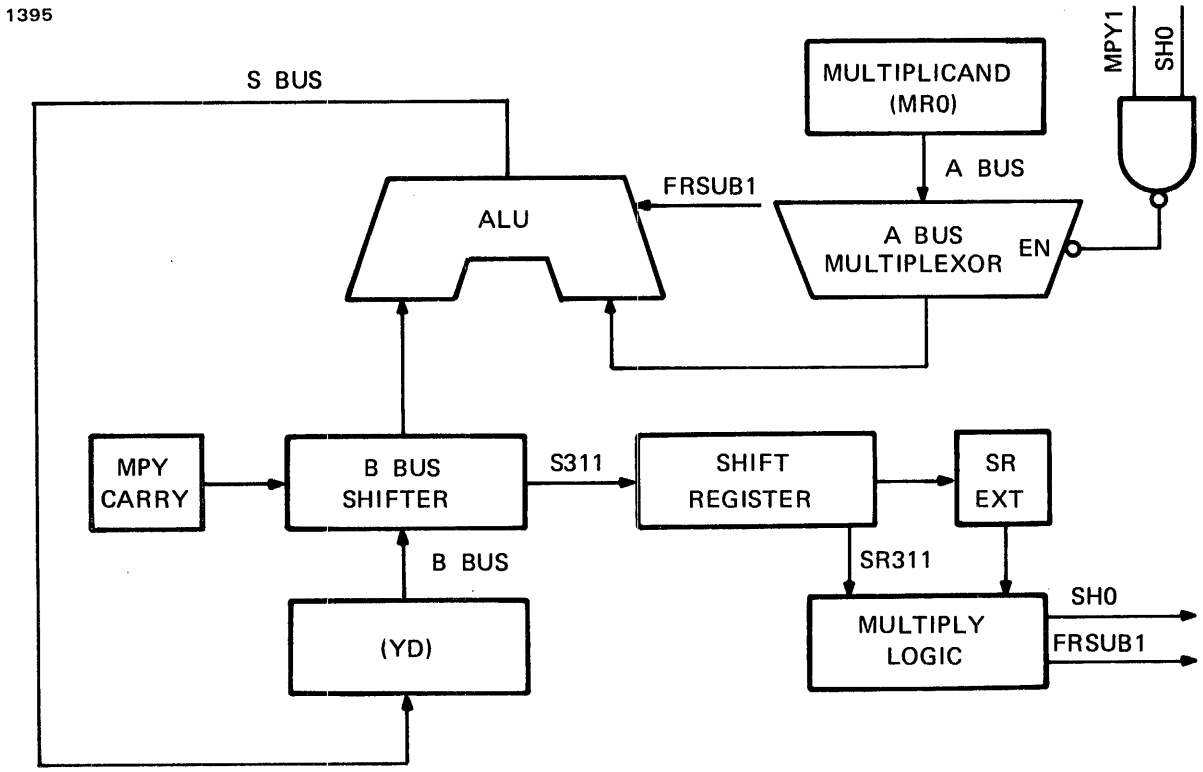


Figure 10-3 Simplified Block Diagram for Multiply

Refer to Table 10-2 to determine the function to be performed for each setting of SR131 and the SR extension (SR EXT) bits. If a shift operation is required (SH1 active) (14G9), the A bus multiplexor is disabled, forcing the B bus data to be shifted by the B bus shifter and added to zero. When a subtract is called for, the ALU select bits are changed from an add, as indicated by the microprogram, to a subtract (FRSUB1 active) (14H8), yielding B minus A. The Add mode is selected by default.

TABLE 10-2 MULTIPLY TABLE

SR311	SR EXT	OPERATION
0	0	SHIFT
0	1	ADD
1	0	SUBTRACT
1	1	SHIFT

10.5.1 Halfword Multiply

Initial Setup

MR0 bits 0:15=multiplicand
MR0 bits 16:31=zero
SR bits 16:31=multiplier
Counter=16

Operation

1. Shift YD right one place, bringing in multiply carry (MPCY1).

2. Test SR311, SR EXT

   If 0,0 or 1,1 - Load YD with shifted data (A bus multiplexor disabled). MPCY=last value of MPCY1.

   If 0,1 - Load YD with multiplicand added to shifted data. MPCY1=sign of multiplicand.

   If 1,0 - Load YD with multiplicand subtracted from shifted data (FRSUB active). MPCY=sign of multiplicand.

3. Shift SR right one place.

4. Repeat 1, 2, and 3, 15 times.

5. Shift YD right one place to YD.

Result

Result is contained in YD.

10.5.2 Fullword Multiply

Initial Setup

MR0=multiplicand
SR=multiplier
Counter=32

Operation

Same as halfword multiply, Section 10.5.1.

Result

Most significant 32-bit result in YD; least significant 32-bit result in SR.

10.6 DIVIDE OPERATIONS

During a divide microinstruction, the ALU is conditioned to the Add mode; the B bus shifter and shift register are conditioned to the shift left mode. Prior to executing a divide, the microprogram ensures that the divisor is in two's complement negative form and the dividend is positive. Refer to Figure 10-4 for a simplified block diagram of divide operations.

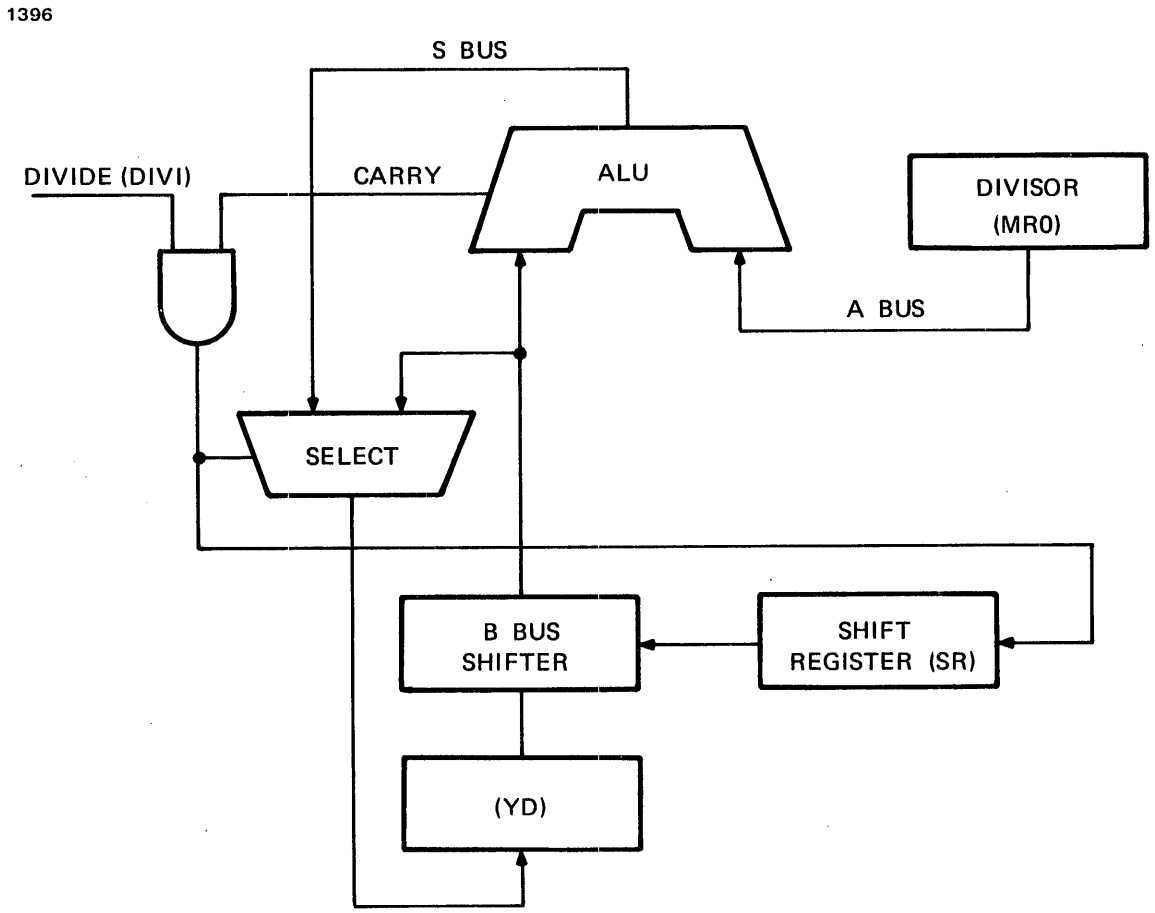


Figure 10-4 Simplified Block Diagram for Divide

10.6.1 Halfword Divide

Initial Setup

MR0 bits 0:15=divisor
MR0 bits 16:31=zero
YD=positive dividend (32 bits)
Counter=16

Operation

1. Shift YD left one place and add to divisor.

2. Test for carry-out from ALU.

   If Carry=1, load YD from S bus and shift SR left, bringing in Carry.

   If Carry=0, load YD from shifted B bus (shift only) and shift SR left, bringing in zero.

3. Repeat 1 and 3, 16 times.

Result

YD bits 16:31 contain remainder.
SR bits 16:31 contain quotient.

10.6.2 Fullword Divide

Initial Setup

MR0=divisor
YD=most significant 32 bits of dividend
SR=least significant 32 bits of dividend
Counter=32

Operation

1. Shift YD left one place and add to divisor.

2. Test for carry-out from ALU.

   If Carry=1, load YD from S bus and shift SR left, bringing in Carry.

   If Carry=0, load YD from shifted B bus (shift only) and shift SR left, bringing in zero.

3. Repeat 1 and 2, 32 times.

Result

YD=remainder
SR=quotient

10.7 B BUS SHIFTER

The B bus shifter (Sheets 2 through 5) performs all the shift functions indicated by the shift control field of the microformat word, except sign Extension (EXT). For EXT, the B bus shifter is conditioned to the load mode and the sign extension is actually performed on the CPU-C board.

The shift control ROM data bits, RD201-RD231, are decoded by three Read-Only-Memories (ROMs, Sheet 14) in order to condition the integrated circuits forming the shifter to the correct mode for each operation. The table provided in the schematics indicates the information contained in the ROMs.

Generally, the B bus shifter is constructed by using two tri-state 2:1 multiplexors that are wire OR-tied for four bits. One multiplexor provides the Load and Exchange Halfword functions, while the other provides for shifting left or right one position. For bits 16:31, a tri-state buffer is also provided to implement exchange byte. Additional open collector AND/NOR gates are used at bit positions 0, 16, and 31 to control bits shifted into the B bus shifter at the boundary positions.

10.8 MNEMONICS

The following is a list of mnemonics found on the CPU-B board. The meanings and 35-768D08 schematic source of each signal are also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
A001-A311	A bus. A source data bus.	10H
ADD1	Add operation decoded.	14G2
AENH0	Enable for the most significant 8 bits of the A bus multiplexor.	2H1
AENL0	Enable for the least significant 24 bits of the A bus multiplexor.	3N1
AMUXS0	The select input to the A bus multiplexor.	13E9
AMX000	The most significant bit of the A bus multiplexor. The second operand sign bit.	2D6
ASTKS0	Output enable for the A stack latch.	13C8
AWE0	Write enable to the A half of the register stack.	6K5

MNEMONIC	MEANING	SCHEMATIC LOCATION
AYDEN1	Enables the A stack address decoding logic to look at the YD field of the Instruction Register (IR).	6C4
AYSDEN1	Enables the A stack address decoding logic to select the general registers or alternate register set.	6A4
AYSEN1	Enables the A stack address decoding logic to look at the YS field of the IR.	6C4
B001-B311	B bus - B source data bus.	Sheets 8,9
BMC001-BMC111	B bus shifter control bits used for selecting the operation to be performed by the B bus shifter.	Sheet 14
BMX000-BMX310	Outputs of the B bus shifter used as the first operand to the ALU.	Sheets 2,3, 4,5
BRD200	Buffered RCM data bit 20.	14M9
BRD210	Buffered ROM data bit 21.	14M8
BSTKS0	Output enable for the B stack latch.	8F4
BWE0	Write enable to B stack.	8D1
BYDEN1	Enables the B stack address decoding logic to look at the YD field of the IR.	7C4
BYSDEN1	Enables the B stack address decoding logic to select the general registers or alternate register set.	7A4
BYSEN1	Enables the B stack address decoding logic to look at the YS field of the IR.	7C4
CARRY1	Carry out from the ALU.	2B9
CISR1	Carry in to bit zero of the shift register.	5N9
CLFLR0	Clear the flag register. Clears the flag register for I/O operations if FLR is not the destination.	15N2

MNEMONIC	MEANING	SCHEMATIC LOCATION
CLK1B	Basic system clock.	6J1
CLKCC0	Clock condition code. Copies FLR to condition code register.	13E3
CLKPSW0	Clock program status word. Loads status portion of the PSW.	13E8
CN08111	Carry out from bits 8:11 of ALU.	2C7
CN12151	Carry out from bits 12:15 of ALU.	2A8
CN24271	Carry out from bits 24:27 of ALU.	4C7
CYIN1	Carry in to least significant ALU.	14D1
DCLK0	Destination clock low active.	6H3
DCLK1	Destination clock high active.	6H3
DIN000-DIN310	Data input to register stack.	Sheets 8,9
DIV1	Divide operation decoded.	8G8
DSTOP0	Destination stop. Disables destination clock when required.	6J1
ENBS0	Enable B source. Gates bits 0:15 of SR or all zeros onto the B bus.	12A9
EXB0	Exchange byte. Condition B bus shifter to perform an exchange byte operation.	4C1
FLR281	Carry flag	15N8
FLR291	Overflow flag	15N6
FLR301	Greater Than flag	15N4
FLR311	Less Than flag	15N2
FRSUB1	Force subtract. Changes the mode of the ALU from an add operation to a subtract operation during a multiply.	14J9

MNEMONIC	MEANING	SCHEMATIC LOCATION
GO811	Generate out from bits 8:11 of ALU.	2B5
GO12151	Generate out from bits 12:15 of ALU.	2B5
G16311	Generate out from bits 16:31 of ALU.	2C8
G24271	Generate out from bits 24:27 of ALU.	4B5
G28311	Generate out from bits 28:31 of ALU.	4B5
GFLR291	Gated overflow flag. Set overflow when false SYNC is detected on an I/O operation.	13E3
GPSWXX1	Gated PSW bits 25, 26, and 27. These bits are forced high when the alternate register set is selected by the microprogram.	13L4
GRD091	Gated ROM data bit 9. RD091 forced high for HPFPP operations.	14B1
GRD101	Gated ROM data bit 10. RD101 forced high for HPFPP operations.	14B4
GRD111	Gated ROM data bit 11. RD111 forced low for HPFPP operations.	14B2
HZERO1	Halfword zero. An all-zeros condition detected on bits 16:31 of the S bus.	15D4
JAMCIO	Jam carry in to ALU decoded.	14B1
LOAD1	The ALU conditioned to the load mode. F=A or F=B.	14G1
LFLRO	Load flag register. The flag register is the selected destination register.	15E9
M1	Mode select to the ALU. Conditions the ALU to the logical mode when high.	14G1
MPCY1	Multiply carry. Carry in to bit 0 of B bus shifter during a multiply.	14G7
MPYO	Multiply operation decoded.	14C9

MNEMONIC	MEANING	SCHEMATIC LOCATION
P08111	Propagate out from bits 8:11 of ALU.	2C5
P12151	Propagate out from bits 12:15 of ALU.	2B5
P16311	Propagate out from bits 16:31 of ALU.	4B8
P24271	Propagate out from bits 24:27 of ALU.	4B5
P28311	Propagate out from bits 28:31 of ALU.	4B5
PSW081:271	The Q outputs of the Program Status Word register.	Sheet 13
RAA00:70	Address bus to the A half of the register stack.	Sheet 6
RBA00:70	Address bus to the B half of the register stack.	Sheet 7
RDXX0	ROM data bits low active.	Sheets 6, 7,13
RDXX1	ROM data bits high active.	Sheets 6, 7,13
S000-S310	S bus. Low active outputs of the ALU.	Sheets 2,3, 4,5
S001-S311	S bus. Buffered outputs of the ALU.	Sheets 2,3, 4,5
SCLK1	Skewed clock. A clock skewed by 50 ns past CLK1.	6J1
SCLR0B	System clear. Initialize signal to the B board.	12A1
SH0	Shift. Disables the A bus multiplexor during multiply operations when a shift only is required.	14J9
SHCRY1	Shifted carry. The input to the C flag during shift operations.	15E1
SR00-SR10	The select inputs to the shift register.	12A9
SR001-SR311	Outputs of the shift register.	Sheet 12

MNEMONIC	MEANING	SCHEMATIC LOCATION
SSEL0	Select line to the input multiplexors of the register stack.	8J9
SUB1	Decoded subtract operation.	14G2
ULSR0	Unload shift register. Selects the SR as the B bus source.	12A1
XRP1	External pullup resistor.	6E1
YD081-YD111	The user destination field of the instruction register.	Sheet 6
YS01-YS031	The user source field of the instruction register.	Sheet 6
ZER01	All zeros detected on the most significant 16 bits of the S bus.	2N7
ZERR0	All zeros detected on the full 32-bit S bus.	15E4

CHAPTER 11
CPU-C BOARD

11.1 INTRODUCTION

The Perkin-Elmer 3230 CPU-C Board, Part Number 35-769, contains the processor's Location Counter (LOC), Memory Address Register (MAR), and the Memory Data Register (MDR). In addition, the CPU-C contains the MDR adder (or summer) which is used during calculate address for RX2 and RX3 user instructions. The C board also has the Memory Address Translator (MAT) logic which provides memory address relocation and protection.

The functional schematics for the CPU-C board, 35-769D08, should be used as a reference for this chapter.

11.2 PROCESSOR MEMORY ADDRESS LOGIC

11.2.1 Memory Address Register (MAR) and Fault Memory Address (ZMAR)

Refer to Sheets 2, 6, 7, 14, 15, and 16 of Functional Schematic 35-769D08 during this discussion.

The MAR is a 24-bit register/counter. The contents of MAR are used for addressing a specific location in memory. If the Program Status Word (PSW) bit 21 is set, the contents of MAR are used by the MAT to generate a new (relocated) address.

MAR is loaded from the S bus when the microinstruction specifies Load MAR (LMAR0) or a Decoded Instruction Read (DIR0), provided MAR Stop (MARSTP0) is inactive. If the microinstruction calls for Increment MAR (IMAR0), the register increments by four. The load or increment occurs on the trailing edge of CLK1C unless Memory Stop (MSTOP0) is active.

The output of MAR (MAR081:311) connects to the program address multiplexors and the ZMAR multiplexors. MAR081:151 are also output to the multiplexors that source SPA081:151 for the MDR adder.

When DIR0 is not active, MAR081:311 drive program address lines PA08:31 which feed the program address latch, FPA081:311. These lines also input to the ZMAR multiplexors. The FPA register latches the current processor memory access when the Data Unavailable flip-flop (FDUA0) goes active. The ZMAR multiplexors normally output MAR081:311 on their corresponding ZMAR lines. However, if during a memory access a memory fault occurs (i.e., alignment, MAT fault or uncorrectable error), Enable Interrupt MAR (EIMAR1 and EIMAR0) go active to output the contents of the FPA register to ZMAR lines, and to inhibit the FPA register from latching a new program address. A microinstruction, specifying MAR as a source after a memory fault, Unload MAR (UMAR), retrieves the faulting address from ZMAR via the B bus multiplexors. (Note that the faulting address is the program address unmodified, even if MAT is enabled.) All subsequent MAR reads return the contents of MAR.

MAR081:MAR151 through SPA081:151 and FPA161:311 input to the MDR adder during Calculate Address (CAMA0).

11.2.2 Location Counter (LOC)

Refer to Sheets 2, 6, 7, 14, 16, 22, and 23 of 35-769D08.

The LOC is a 24-bit register/counter and its contents always point to the address of the next user instruction to be executed. On an instruction fetch, LOC is used during calculate address. LOC is loaded from the S bus when it is specified as the destination by the microinstruction and Destination Stop (DSTOP0) is not active. In addition, LOC is incremented by 2 when Increment LOC is active during calculate address. The load or increment is performed on the trailing edge of CLK1C.

The LOC outputs, LOC081:301, input to the program address multiplexors and B bus multiplexors. LOC081:151 drive the multiplexors that source SPA081:151 for the MDR adder. Note that LOC311 is not implemented and is forced reset.

11.2.3 Program Address Multiplexors (PA MUX)

Refer to Sheets 6, 7, and 16 of 35-769D08

The PA MUX selects either the LOC or MAR outputs. LOC outputs are selected during instruction fetch and calculate address; the MAR outputs are selected at all other times. PA081:311 input to the program address latch. PA081:151 connect to the Process Segment Table Entry (PSTE) comparator and the MAT relocation summer. PA081:201 are used by the program address relocation summer and PA211:311 input to LMA drivers. The segment limit detection involves PA161:201. PA301 is transmitted to the CPU-D board and defines the halfword memory boundaries. PA080:150 are used to select one of 256 Segment Table Entries from the MAT register stack.

11.2.4 Memory Data Register Summer (MDRΣ)

Refer to Sheet 20 of 35-769D08 during this description.

The MDR summer (MDRΣ) is a 24-bit full adder using bits 8:31 of the Memory Data Register (MDR) and the 24-bit PA multiplexor outputs as the numbers to be added. The MDR is used exclusively during calculate address to determine the address displacement of the second operand for RX2 and RX3 instructions. The RX2 and RX3 format instructions require three values to arrive at the program address of the second operand data to complete the instruction. The RX2 format requires that a 15-bit displacement (negative or positive) in the second halfword of the instruction be added to an index value contained in a general register specified by the YS field of the Instruction Register (IR). The result of this addition is then added to the value of the incremented LOC (location of next instruction). This final number is the program address of the second operand. The RX3 format requires that the least significant 24 bits of MDR (represented by the least significant 24 bits of the 48-bit RX3 instruction) be added to an index value contained in the general register specified by the YS field of the IR. The result is then added to a second index value contained in the general register specified by MDR bits 4:7. This final number is the program address of the second operand.

The MDRΣ provides the ability to add three numbers together in a single microinstruction. During an RX2 address calculation, the incremented LOC and the least significant 15 bits of MDR are added and provided as SUM8:31. The MDR data is sign extended at the inputs of the MDRΣ by 2:1 multiplexors and logic on MDR161. The MDR during RX2 contains the same data in both halfwords of the MDR. MDR bit 01 represents the sign of MDR displacement data. The state of MDR bit 01 is forced on the adder inputs from bits 16:12. This provides either a negative or positive displacement. The PA multiplexor has the incremented LOC on its outputs. The MDR, when specified as a B bus source during calculate address of the RX2 format, yields the added MDR and LOC. If the RX3 format second operand address is being calculated, the MAR contains the first level index indicated by the YS field of the IR. The first level index and the MDR displacement are added and supplied as the MDR data on the B bus.

11.2.5 Memory Address Bus Drivers

Refer to Sheets 10 and 12 of 35-769D08 during this description.

The memory address bus drivers provide a 24-bit physical address in memory on the LMA080:310 lines. These lines are active if the processor or MAT access the memory. A set of tri-state line drivers is provided for each. On a processor access of memory, ENRPA0 (Enable Regular Path) outputs the program address relocation summer and PA211:311 to the LMA bus. On a MAT access, ENMAA0 (Enable MAT Access) outputs the MAT relocation summer and four gated MAT bits, GMA251:281 to LMA, and LMA290:310 are forced inactive.

11.3 PROCESSOR MEMORY DATA LOGIC

11.3.1 Processor Memory Data Register

Refer to Sheets 17, 18, and 19 of 35-769D08 during this description.

The MDR is a 32-bit register used by the microprocessor to receive or send data to memory.

Data loaded into the MDR from the MDR data multiplexors may come from two different sources: the S bus when the microinstruction specifies the MDR as a destination, or the Memory Data Sense (MDS) bus during instruction read or memory read operations. The MDR is split into two halfwords: MDH and MDL. Each may be loaded independently. On a fullword read, a fullword of data is loaded into the MDR. On a halfword read, only MDL (MDR16I:311) is loaded. For an instruction read on a fullword address boundary, MDS160:310 are loaded into both MDH and MDL. On an instruction read that resides on a halfword boundary, MDR is not loaded. If a second halfword has to be fetched for the instruction, it is loaded into both halves of MDR.

11.3.2 Memory Data Multiplexors

Refer to Sheets 17, 18, and 19 of 35-769D08 during this description.

The memory data multiplexors select the data to be loaded into the MDR and the bus from which it is loaded: the MDS bus or the processor S bus. When selecting the buffered MDS bus, the memory data multiplexor can load either the most significant or least significant halfword of MDS into MDRH or MDRL. The MAT status register also may be loaded into the MDRL. This occurs when a microinstruction specifies a memory read operation and Reset Fault (RFAULT) is specified by the microprogram with a MAT interrupt queued. The memory operation must be performed within resident local memory. When these conditions are satisfied, the multiplexors output the MAT status bits EMAT291:311 to the MDR forcing zeros on all other bits.

11.3.3 Local Memory Data Bus Drivers

Refer to Sheet 21 of 35-769D08 during this description.

The local Memory Data Bus (MDB) drivers supply the data to be written into memory by the processor. The MDB drivers are connected to the MDS bus, which is a bidirectional data bus used for reading from and writing to memory. The MDB drivers are enabled only during a memory write operation provided that the MAT does not require an access (FMATCY1). Halfword memory write operations from the processor always position the halfword to be written in the MDR (bits 16:31). This data may be written to a halfword or fullword boundary. MDR161:311 drive MDS160:310 on any processor to memory write operation (LWRTO, LHWRTO). To write a halfword to a fullword boundary, LHWRTO is active to output MDR161:311 to MDS000:150.

11.4 MEMORY ADDRESS TRANSLATOR (MAT)

11.4.1 MAT Function

When the MAT is disabled, the program address lines (PA081:310) directly address the memory via the local memory bus (LMA080:310). With MAT enabled, the memory location specified by LMA080:310 is the sum of the least significant 16 bits of the program address (PA161:311) and a bias value contained in an entry of the Process Segment Table (PST) in memory.

The PST for a task can consist of a maximum of 256 contiguous double fullwords or entries. Only the first 32 bits of an entry are of significance to the hardware. The starting address of the PST is specified by the Process Segment Table Descriptor (PSTD). The CPU-C board has a PSTD register which is loaded from the MDR on command from a microinstruction - Load PSTD (LPSTD). The PSTD register is implemented in hardware as shown in Figure 11-1.

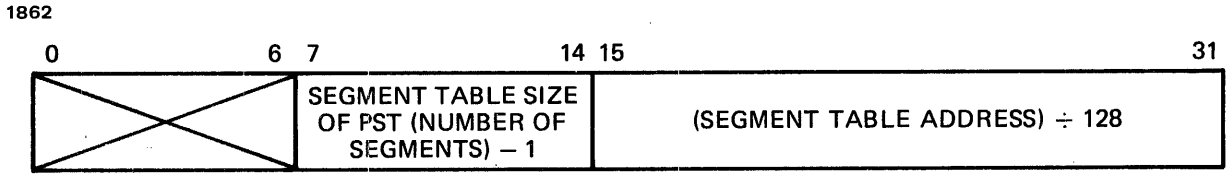


Figure 11-1 Process Segment Table Descriptor (PSTD)

When the MAT is enabled, the program address is considered to consist of two fields - the segment field and the offset field, as shown in Figure 11-2. With PSTD bits 15:31, PA08:15 are used as an index into the PST to select an entry. The accessed entry indicates if it is private or shared. If private, the Segment Table Entry (STE) contains the starting address of a segment in memory to which the offset field of the PA serves as an index. If PA08:15 is greater than the segment size specified by the PSTD, a MAT fault is generated.

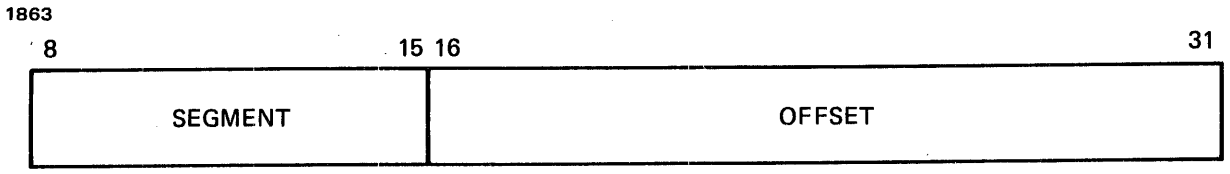


Figure 11-2 Program Address (MAT Enabled)

If the entry is shared, the Shared Segment Table (SST) must be accessed to obtain the STE. The SST can consist of 8,192 double fullwords or entries. The starting address in memory of the SST is contained in the Shared Segment Table Descriptor (SSTD). The CPU-C board has an SSTD register which is loaded from the MDR on command by a microinstruction - Load SSTD (LSSTD). The SSTD is implemented in hardware as shown in Figure 11-3. Before the SST is accessed, the shared segment size in the STD is compared with the PST STE. If SSTD bits 2:14 are less than the STE size, a MAT fault results; if not, the SST is accessed. SSTD bits 15:31 point to the first location in the SST and the STE serves as an index. The STE obtained from the SST points to the segment in memory and PA16:31 index into the segment. Only the first 32 bits of a Segment Table Entry relate to the hardware. An STE, whether private or shared, has the format shown in Figure 11-4. The fields are defined as follows:

Bit(s)

0 R - Reference Bit. This bit is set in the STE when the segment is accessed.

1 P - Presence Bit. This bit is set when the segment described is present in memory; it is reset when the segment is not present. A reference to a segment that is not present (P=0) results in a MAT fault and the CPU ignores bits 2:31 of the STE.

2 D - Dirty Bit. This bit is set by hardware when a Write is to be executed in the segment.

3:5 A - Access Mode Bits. The A field specifies the allowed modes of access to the segment. Bit 3, when set, allows read accesses; bit 4, when set, allows write access; and bit 5, when set, allows instruction read accesses. An attempt to access a segment in a mode that is not enabled results in a MAT fault.

6, 7 L - Access Level Bits. The L field is used in conjunction with PSW 10 and 11. If the contents of PSW 10 and 11 are greater than or equal to the L field, then access of the segment is allowed. If the contents of PSW 10 and 11 are less than the L field, a MAT fault occurs.

8 S - Shared Bit. If the Shared bit is zero, MAT performs the protection and the relocation functions as defined for a private segment. If S=1, the selected segment is shared. In this case, the SRF field of the PST STE is used in conjunction with the address contained in the STE as a byte offset into the Shared Segment Table. The S bit in the Shared Segment Table must be zero for all entries. The contents of the A fields of the PST STE and the SST STE are ANDed to determine the allowed access mode. All other protections and relocations are performed using the data from the SST STE.

10:14 SLF - Segment Limit Field. The SLF specifies the size of the segment. If the SLF is less than PA161:201, a MAT fault results.

15:31 SRF- Segment Relocation Field. The interpretation of this field depends upon the state of the S bit. If S=0 in the PST, the SRF is the bias value of the segment divided by 128, to which the offset field of the program address is added to obtain the physical address in memory. If S=1 in the PST, the PST SRF is the byte offset or index into the SST where the STE for the segment is located. If the PSTE SRF is greater than the segment size specified by the STD, a MAT fault results. Note that for a shared segment the least significant three bits of the PST SRF must be zero because the SST is aligned on a double fullword boundary. For all other cases, the least significant four bits must be zero as the SRF is the address of a segment aligned to a 2^{11} byte boundary divided by 2^{7}. As a result, bits 29:31 are not implemented in the hardware.

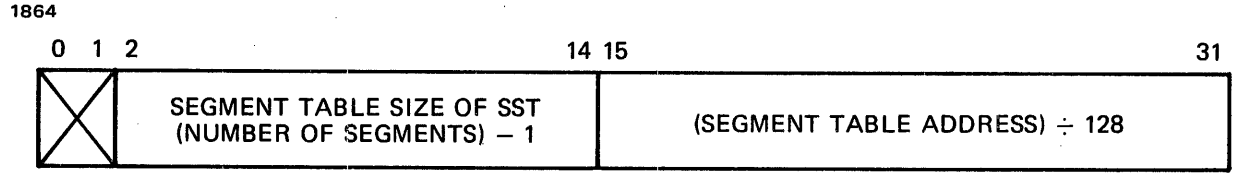


Figure 11-3 Shared Segment Table Descriptor (SSTD)

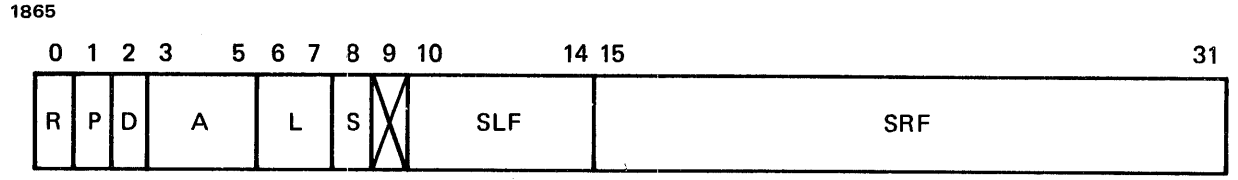


Figure 11-4 Hardware Segment Table Entry

In order to eliminate repeated memory accesses to gain a segment entry, the CPU-C board stores the STE in a register stack when it is first obtained. The stack has a capacity for 256 entries. The only other memory access to an entry that resides in the stack would be to set the Dirty bit on a memory write operation if the access mode permits a write.

Two stacks are provided for the Presence bit. The Presence stacks must be set to zero whenever the CPU is powered up or initialized. When the PSTD register is loaded, a Presence stack is initialized to zero. When both stacks are in the process of initializing, the CPU is halted.

11.4.2 Process Segment Table Descriptor (PSTD) and Segment Size Comparator (Sheet 3 of 35-769D08)

The PSTD is loaded from MDR071:311 by Load PSTD (LPSTD0). The first eight bits - the segment size - are compared to PA081:151. An error (EPSTD1) is generated if the program address exceeds the segment size.

Segment Table Descriptor bits STD161:311 are disabled when GETSSTE1 is active. These bits are tied to those of the SSTD and input to the MAT Relocation Summer.

11.4.3 Shared Segment Table Descriptor (SSTD) and Shared Segment Size Comparator (Sheet 4 of 35-769D08)

The SSTD is loaded from MDR021:311 by DCLK1 when a Load SSTD (LSSTD0) is specified. The first 13 bits (the shared segment size) are compared with the Buffered Relocation bits BRF091:211. An error (ESSTD0) is generated if BRF091:211 is greater than the shared segment size when a shared STE is to be accessed.

STD151:311 are enabled on an STE memory access (GETSSTE0). These connect with those of the PSTD and input to the MAT Relocation Summer.

11.4.4 MAT Relocation Summer and LMA Drivers (Sheet 10 of 35-769D08)

The MAT Relocation Summer generates the memory address for the MAT when an STE must be obtained. The Segment Table Descriptor bits STD151:311 are input to the summer. On a nonshared access, PA081:111 are added to the STD bits. PA121:151 generate Gated Memory Address bits GMA251:281 and are input to the LMA drivers. When a Shared Segment Entry is to be obtained (GETSSTE0 active), Buffered Relocation bits BRF091:171 are selected for the addition and BRF181:211 assert GMA251:281.

The adder outputs and GMA251:281 connect to the LMA drivers when enabled by Enable MAT Access (ENMAA0A). LMA290:310 are forced inactive.

MAT Program Address bits MPA081:111 are used in decoding the memory that is to be accessed.

11.4.5 Stack Load Buffer (Sheet 8 of 35-769D08)

The buffer is loaded from the buffered Memory Data Bus (MDS lines) with an STE when MAT Cycle (FMATCY0) goes inactive. The buffer has both active and tristate outputs. The latter are enabled by Disable Stack (DISSTK0) when the STE is to be written in the Segment Table Register Stacks.

The following outputs connect to the stack:

PRES1 - Presence bit
DIRT0 - Dirty bit
L01:11 - Access level bits
SLF01:41 - Segment Limit Field
SRF081:201 - Segment Relocation Field

The active buffer outputs FSHARED1 and the Buffered Access Mode bits BA01:21 connect to a tristate 2:1 multiplexor and a quad register which stores the bits if the buffer indicates that the PSTE is shared. The stored access bits are ANDed with BA01:21 of the shared STE. ASHARED1 selects the quad-register outputs, and the multiplexor drives SHARED1, A01, A11, and A21 of the stack.

The remaining active buffer outputs are Buffered Relocation bits (BRF091:211) which specify the Shared Segment Table Entry.

11.4.6 Segment Table Register Stacks (Sheet 8 of 35-769D08)

The MAT stacks consist of three 256x9 and two 256x1 Random Access Memories. The two Presence stacks - A stack and B stack - are accessed by AP081:151 and BP081:151, respectively. The remaining stacks are directly addressed by Program Address bits PA080:150. The 256x9 stacks are always selected and the Presence stacks are enabled by A/B Chip Select (ACS0 and BCS0). The outputs of the stacks go tristate when Disable Stack (DISSTK1) and A/B Write Enable (AWE0 or BWE0) go active. The Presence bit is written to the selected stack by an active write enable. The 256x9 stacks are written into by Write Stack 0 (WSTK0).

11.4.7 MAT Control (Sheet 9 of 35-769D08)

The MAT control determines if the MAT requires a memory access. When a MAT memory cycle is necessary, the MAT control takes care of loading the stack buffer, writing into the stacks, and generating a MAT cycle to memory if the retrieved PSTE is a shared entry.

On initialize or power up (BSCLR0A), the MAT is disabled (MATEN1 low) until the PSTD register (LPSTDCK0) is loaded. The MAT is enabled when PSW 21 is set; a privileged memory operation (RD031) is not to be executed and Decoded Enable Clock is inactive. If a segment is not present in the stack or if present and a processor write to memory is to be performed, ENRAP0 is gated inactive and ENMA00 active. Figure 11-5 shows the timing waveforms for a MAT cycle to memory.

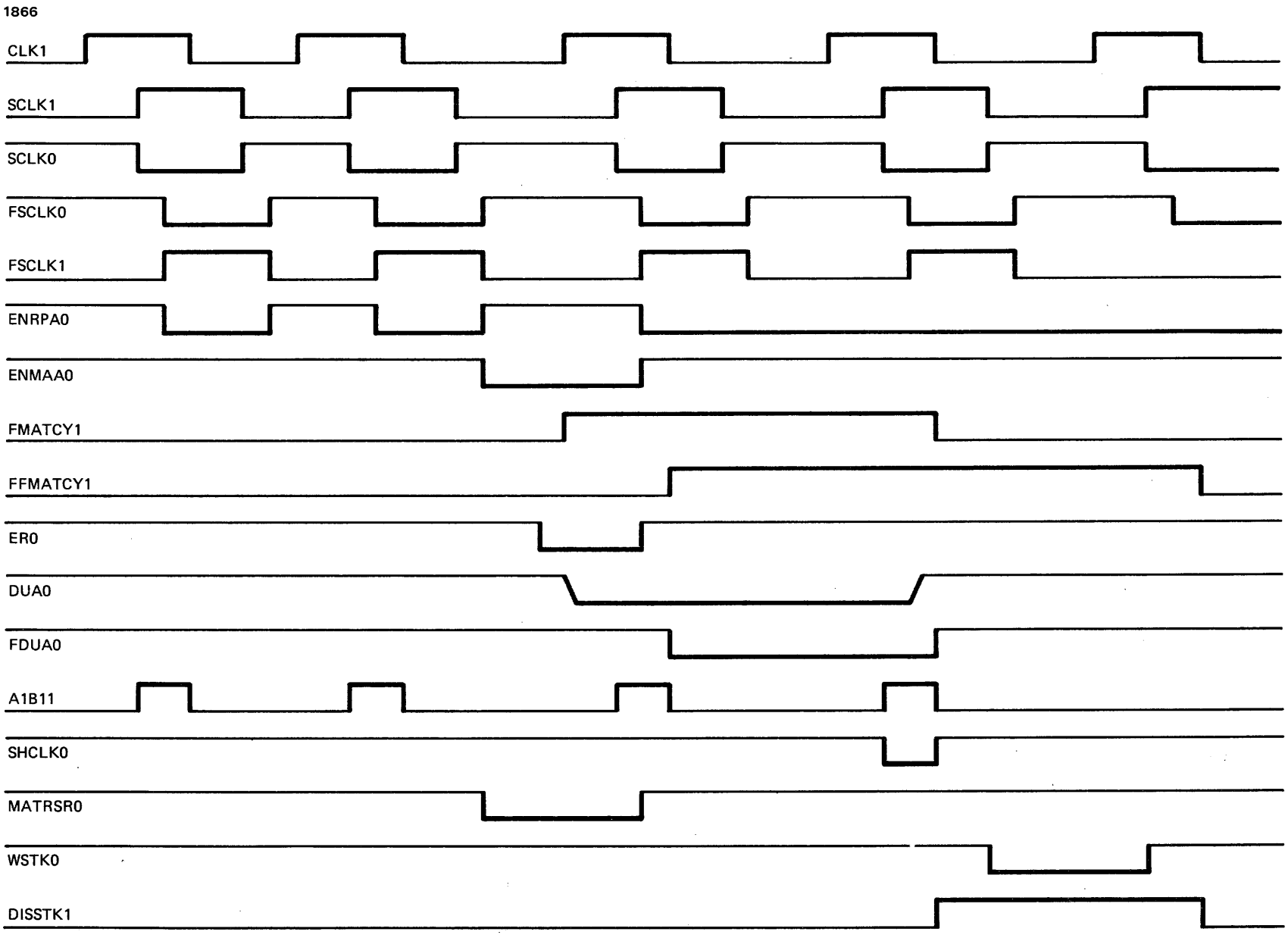


Figure 11-5 MAT Cycles to Memory Timing

ENRAP0 disables the LMA drives of the PA Relocation Summer and ENAMA0C enables those of the MAT Relocation Summer. ENMA00 goes to the CPU-D board 35-770 to initiate a memory cycle, and the MAT Read and Set Reference bit (MATRSR0) goes to the memory. The MAT Read and Set Dirty bit (MATRSD0) is sent to memory if the segment is to be written into and a write is permitted.

When FMATCY is set, it disables the MDS drivers to memory and allows FFMATCY to toggle set on the trailing edge of the CLK1 which directly sets FMATCY. Data Unavailable (DUA0) from memory is toggled into FDUA if it is active on CLK0. An inactive DUA0 allows FMATCY and FDUA to toggle reset on the trailing edge of CLK1. FMATCY0 going high toggles the MDS lines into the stack buffer. After FDUA0 goes high, the stacks are disabled (DISSTK1), SHCLK0 is generated and, if the segment is not shared, the stack is written into (WSTK0) from the buffer register. CLK0 then toggles FMATCY reset.

If FSHARED1 is active, GETSSTE0 is generated to indicate that another MAT cycle is required.

11.4.8 Program Address Relocation Summer and LMA Drivers (Sheet 12 of 35-769D08)

When the MAT is disabled, PA081:201 are gated through the adder to the LMA drivers. PA211:311 connect directly to the drivers. With the MAT enabled (MATEN0), PA081:151 are zeroed to the adder. The Segment Relocation Fields - SRF081:201 and PA161:201 are summed. ENRPA0 enables the LMA drivers. Relocated Program Address bits (RPA081:111) are used in decoding the memory that is to be accessed.

11.4.9 MAT Fault Decode (Sheet 11 of 35-769D08)

On memory references when the MAT is enabled, the protect function comes into play. MAT interrupts (MATFALT0 and MAT) are set when a MAT violation occurs. The checks that are made are listed in the table on Sheet 11 - MAT Fault Codes. The fault code is generated by the 8:3-line priority encoder and the code is latched in EMAT291:311. It remains latched until Clear States (CLSTA0) goes active; this also clears the MAT. MATFLT0 can also set on a Memory Fault (MFAULT0) and is directly cleared by RFAULT0.

11.4.10 Presence Bit Initialization (Sheet 5 of 35-769D08)

Each of the Presence stacks has its own initialization control. The logic consists of a pair of 8-bit counters that are cleared by BSCLR0. This line also sets FAINCR and FBINCR and their associated J-K registers. With these registers set, Write Enable (AWE0 and BWE0) and Chip Select (ACS0 and BCS0) to the stacks go active. FAINCR1A and FBINCR1A select the output of the counters as the address (APA081:151 and BPA081:151) for their stacks. ACP1 and BCP1 increment the counters on the trailing edge of CLK1 until a carry is generated. At this time, A11 is allowed to toggle the first set of J-K registers reset and A/BWE0 and A/BCS0 are disabled and directly clear their respective FA/BINCR.

If neither stack is selected, the A stack is chosen when LPSTD1 goes active and generates APE1 to permit the first J-K to be toggled set and the A counter to be loaded from MDR080:150 by ACP1. The A stack remains selected while a new task is loaded in the PSTD. LPSTD1 now activates BPE0, allows the first J-K of the B stack logic to be toggled set, and enables the J input of FAINCR. BPE0 permits the B ccunter to be loaded from MDR080:150 by BCP1 and A1B11 toggles FAINCR set; the A stack then initializes. When both stacks are being initialized, MATSTOP0 is generated to halt the processor.

11.4.11 Local/Shared Memory Detection (Sheet 13 of 35-769D08)

The chosen strapping option is a function of shared memory. The strapping shown is for nc shared memory. RPA081:111 are generated by the Program Address Relocation Summer and MPA081:111 by the MAT Relocation Summer. If Processor to Shared Buffer Controller (PSBC0) is active, it indicates a shared memory access by the processor. If MAT to Shared Buffer Controller (MSBC0) is active, it indicates a shared memory access by the MAT.

11.5 B BUS MULTIPLEXOR

Refer to Sheets 22 and 23 of 35-769D08 during this description.

The CPU-C B bus multiplexor supplies the data contents of the register specified by the microinstruction B source field. The B bus multiplexor is capable of driving the B bus from the following four sources: memory data register (processor MDR), memory address register, location counter, and the memory data register adder output. The memory data register adder output is used only during the calculate address sequence of instruction reads. The MDR data contents may be sign extended from bit 16 of the MDR. The state of MDR 16 is propagated through to MDR bit 00. This is used for halfwcrd reads from memory where MDR bits 0:15 are undefined. LOC is a 24-bit source. Bits 0:7 and bit 31 are forced reset by the B bus multiplexor when LOC is specified as the source. The MAR is a 24-bit source. Bits 0:7 are forced reset by the B bus multiplexor when the MAR is the specified source. When the MAR is the source under special conditions, the fault memory address register (ZMAR) contents are used instead of the MAR.

11.6 MNEMONICS

The following is a list of the mnemonics found on the CPU-C board. A brief description and the schematic source of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
A01:21	Access mode bits	8B9
A1B11	Pulse generated from the AND of CLK1 and SCLK1	3H6
ACP1	A presence stack clock	5M3
ACTR080:150	A presence stack counter output	Sheet 5
ALGN0	When low, a memory alignment fault has occurred. This fault may be caused by a fullword access to a halfword address or a halfword access to a byte address.	15F8
APA081:111 APA121:151	Program address bits for the A presence stack	Sheets 6 and 7
APE1	A presence stack counter load enable	5H2
ASHARED0	Shared bit of auxiliary register	8A5
ASHRD1	Second buffered shared bit	8C9
AXRP1	1 k ohm resistor connected to P5 - used to give noise immunity to unused inputs.	4R6
B001:311	Second operand data (B bus) from the CPU-C board - RD bits 24, 25, 26, and 27 determine the specific source register. The source registers may be: Location Counter (LCC), Memory Data Register (MDR), Memory Address Register (MAR), or Fault Memory Address Register (ZMAR) and the adder output of the MDR (SUM). The MDR may be sign extended from bit 16:00.	Sheets 22 and 26
BA01:21	Access mode bits of stack buffer	8C3
BCLR0	B net of system clear	3L7

MNEMONIC	MEANING	SCHEMATIC LOCATION
BCP1	B presence stack clock	5M9
BCS0	B presence stack chip select	5M6
BCTR080:150	B presence stack counter output	Sheet 5
BPA:081:111 BPA:121:131	Program address bits for the B presence stack	Sheets 6, 7
BPE0	B presence stack counter load enable	5N8
BRF091:211	Segment relocation field bits - active outputs of stack buffer register	Sheet 8
BWE0	B presence stack write enable	5M5
CAGDIR0	Calculate address gated decoded instruction read	14F2
CAMA0	Calculate memcry address signal from CPU-D during calculate address that controls the output of the PA multiplexor - during RX2, LOC is added to the MDR. During RX3, when CAMA0 is low, the MAR (first) level of index is added to the MDR.	14B2
CLK1	Buffered output of CLK1C, system clock - this clock is to synchronize the CPU-C logic to the rest of the processor.	5N3
CLK1C	The CPU-C net of system clock generated on the CPU-D	3G4
CLRA0	Clear auxiliary register	11N2
CLSTA0	Clear MAT status (fault) register	11N4
CWR0	Change write to a read memory operation - this signal is generated after any memory fault (MAT, MPE, or ALGN) and prevents any further access until error recovery starts.	11N5
DCLK1	Destination clock - DCLK1 allows a selected destination on the CPU-C to be loaded; similar to CLK1, except no clock is generated during DSTOP.	3H7

MNEMONIC	MEANING	SCHEMATIC LOCATION
DENCLK0	Decoded enable clock	15D8
DEXB0	Decoded exchange byte - RD decoding of exchange byte supplied by the CPU-A	19K6
DEXT0	Decoded sign extension - RD decoding of MDR sign extend; if not inhibited by the calculate address sequence, the state of MDR16 is propagated through to MDR00.	22F8
DIR	Decoded instruction read - RD decoding of instruction read used to control PA multiplexors (when low selects the LOC contents) and loading of the MDR during calculate address	4H6
DIRT0	Dirty bit - tri-state output of stack buffer register	8B3
DISA1	Disable A byte - enables loading of MDR bits 8:15. This signal is also used to inhibit loading the most significant byte of the least significant MDR half-word.	19R6
DISB1	Disable B byte - enables loading of MDR bits 0:7. This signal is also used to inhibit loading the most significant byte of the MDR most significant halfword.	19R6
DISEXT0	Disable MDR sign extension - signal from CPU-D during calculate address to inhibit RD implied MDR sign extend	22G8
DISSTK1	Disable stack	9R5
DRD1	Decoded data read - RD decoded memory data read (memory data read, not instruction read). This signal is used to help define when tc clear a fault.	15B8
DSTOP0	Destination stop - this is used to control whether to allow a clock to occur and thereby load a selected destination.	3H4
DUA0	Data unavailable - line from memory	9J3
EAL	Error of access level	9G8

MNEMONIC	MEANING	SCHEMATIC LOCATION
EEDCLK0	Even EDMA memory data register clock - signal from the CPU-D that, on the positive transitiCn, loads the data from either the local memory or from the EDMA.	11M1
EIMAR0	Enable interrupt MAR - this signal, when low, indicates that a memory fault has occurred and that the fault address may be read. The output enable of the normal MAR is disabled and the ZMAR is enabled. Reading the fault address resets the EIMAR flip-flop allowing the MAR to be read.	15E4
EMAT291:311	MAT code fault bits	11M6,11M8, 11M9
ENMAA0	Enable MAT LMA drivers - also indicates MAT access to memory	9G5
ENPAR0	Enable MAT relocated LMA drivers - when inactive on a PMEM, it indicates a MAT access of memory	9G4
EP241	Execute protect bit 24 - this bit, when active, indicates that the current memory segment selected causes a MAC interrupt if used for program execution.	4N5
EPSTD1	Error - process segment size	3B9
ESLF1	Error of segment limit field	9L7
ESSTD0	Error - shared segment size	4C9
EXB0	Exchange byte - when low, an exchange byte occurs on the least significant halfword on the B bus (bits 16:31).	19R7
FAINCR1	A presence stack increment flip-flop	5N2
FBINCR1	B presence stack increment flip-flop	5N7
FDIRT0	Dirty bit of stack buffer register	8A3
FDUA0	Data unavailable from memory flip-flop	9L2
FFMATCY	Auxiliary MAT memory cycle flip-flop	9M3
FMATCY	MAT memory cycle flip-flop	9K3

MNEMONIC	MEANING	SCHEMATIC LOCATION
FNCE0	Flop output of noncorrectable error - signal is generated on the CPU-D. It is an indication that a double-bit error has occurred.	6B8
FPA081:151	Program address register bits - stores 8 bits of PA on a memory fault	Sheet 15
FPACLK1	Clock for FPA register	15J5
FPRES1	Presence bit of stack buffer register	8A3
FSCLK	Skewed SCLK flip-flop	9A4
GDIR0	Gated decoded instruction read - controls steering of PA multiplexor during calculate address	3N9
GETSSTE0	Get shared segment table entry	9N6
GEXT1	Gated MDR sign extension - when active, causes the state of MDR16 to be propagated to MDR00	22F7
HALT0	Halt processor - DMA request queued or memory is busy	9G2
ILOC0	Increment location counter - generated on CPU-D during calculate address	2N6
IMAR	Increment MAR	2L1
JAMDIRT0	Jam dirty bit into stack buffer register	19E6
JAMSHRD1	Jam shared bit into stack buffer register	19E6
L01:11	Access level bits	8D3, 8E3
LHWRT0	Local halfword memory write - used to gate least significant halfword to local memory for halfword memory write	21A8
LLOC0	Lcad location counter - RD decoding specifying the location counter as a destination	23C8

MNEMONIC	MEANING	SCHEMATIC LOCATION
LMA080:310	Memory address data line - this is the physical address presented to memory.	Sheet 25
LMAR0	Load memory address register - RD decoding of MAR as a destination register	23C7
LMDR0	Load memory data register - RD decoding of MDR as a destination register	23C7
LOC081:301	Location counter output lines	Sheet 2
LPSTD0	Load process segment table descriptor	3L1
LPSTDCK0	Load process segment table descriptor clock	3M1
LSSTD0	Load shared segment table descriptor	4L5
LWRT0	Local memory write enable - gates the selected inputs of the 2:1 multiplexor onto the MDS bus	21A1
MAR081:311	Memory address register data output lines	Sheet 2
MARSTP0	MAR stop - generated on CPU-D during calculate address of RX squared (RXRX) format. This signal allows the MAR to be loaded with DSTOP active.	2A1
MAT0	MAT interrupt	11N4
MATEN1	MAT enable	9D2
MATRSD0	MAT read and set dirty bit	19E8
MATRSR0	MAT read and set reference bit	9J5
MATSTOP0	MAT stop	5K3
MCLK1	System clock gated by memory stop (MSTOP)	5L1
MDHLK0	Memory data register high clock - data on the inputs of MDR bits 00:15 are latched on the positive transition of clock.	17R1
MDHSA1	Memory data register multiplexor steering signal - select data input to MDR bits 00:15	17M1

MNEMONIC	MEANING	SCHEMATIC LOCATION
MDLCK0	Memory data register low clock - data on the inputs of memory data register bits 16:31 are latched on the positive transition of clock.	18R1
MDLSA1	Memory data register low multiplexor select line - selects the type of data input to the memory data register bits 16:31	15B1
MDR000:311	Memory data register data output lines	Sheets 17, 18, 19
MDRΣ0	Memory data register sum output select	23B2
MDS000:310	Memory data system bidirectional data lines - data either to be written to or read from local memory	Sheet 16
MDSB0	Memory data register multiplexor select generated by CPU-D - selects type of data to be loaded into the MDR	18D1
MEMSA0 MEMSB0	B bus multiplexor enable for CPU-C source registers	22G2 22G3
MFAULT0	Memory fault - indicates that a memory fault has been queued because of a non-correctable error, MAT interrupt, or alignment fault	15A6
MPA081:111	MAT program address bits	Sheet 13
MSBC0	MAT to shared buffer controller	13F4
MSELB1	B bus multiplexor select line	23B2
MSTOP0	Memory stop - used to inhibit system clocks while the memory system is busy or data is unavailable	3G4
PA081:311	Program address multiplexor outputs - the outputs reflect the contents of the location counter during calculate address or the contents of the MAR at any other time.	Sheets 6, 7 and 14
PMEM1	Processor memory operation request	9G2

MNEMONIC	MEANING	SCHEMATIC LOCATION
PRES1	Presence bit - tri-state output of stack buffer register	8B3
PSBC0	Processor to shared buffer controller	13F2
PSEL1	Processor selected - generated by the CPU-D when memory address and data are relevant to a processor as opposed to an EDMA memory cycle	9A3
PSW10 PSW11	Program status word bits indicating access level of the processor	9A8, 9A7
PSW211	Program status word bit 21 - this is the relocation/protection bit of the PSW that enables the MAC.	9A2
RD00:03	Memory control field of microinstruction	Sheet 4
RD150	ROM data register bit of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	23A5
RD240	ROM data register bit of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	22B2
RD001:041	ROM data register bits of the microinstruction word - the RD bits control all processor level functions.	3A6,3A1, 3A7,16B2
RD261	ROM data bit 26	23B2
RD051	ROM data register bits of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	16B2
RD121:141	ROM data register bits of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	23A6, 23A7
RD161	ROM data register bits of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	22B2

MNEMONIC	MEANING	SCHEMATIC LOCATION
RD251:271	ROM data register bits of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	22B1, 23B1
RD271A	ROM data register bits of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	23B1
READ1	Read but not read and set	11D7
RFAULT0	Reset fault - used to clear memory fault conditions	11N3
RPA081:111	Relocated program address bits	Sheet 13
S001:311	S bus data output from the CPU-B	Sheet 13
SCLR0C	Systems clear CPU-C net	3L4
SHCLK0	Shared clock	9N3
SCLK1	Skewed CLK1 clock	3H5
SHARED	Shared bit of stack	8B9
SLF01:41	Segment limit field bits	8E3, 8G3
SPA081:151	Program address bits	Sheet 16
SRF091:201	Segment relocation field bits - tri-state outputs of stack buffer register	Sheet 8
STD151:311	Address field of segment descriptors	Sheets 3,4, 10
SUM081:311	Outputs of adder used during calculate address to resolve effective address of RX2 and RX3 formats. The contents of MDR and LOC (RX2) or the MDR and MAR (RX3) are added together. The resulting data is available on the B bus as the MDR data.	Sheet 20
ULOC0	Unload location counter - RD decoding of location counter as the B bus source register	22F1

MNEMONIC	MEANING	SCHEMATIC LOCATION
UMAR	Unload memory address register - RD decoding of the MAR as the B bus source register	22H2
UMDR0	Unload memory data register - RD decoding of MDR as the source register	22G2
WSTK0	Write into segment table register stacks	9N3
XRPA	Pull-up terminations for unused inputs to provide noise immunity	3K1
XRPB	Pull-up terminations for unused inputs to provide noise immunity	3E1
XRPC	Pull-up terminations for unused inputs to provide noise immunity	5M8
XRPD	Pull-up terminations for unused inputs to provide noise immunity	6D8
XRPF	Pull-up terminations for unused inputs to provide noise immunity	7A1
XRPG	Pull-up terminations for unused inputs to provide noise immunity	14L9
ZMAR081:311	Output of a 2:1 MUX-ZMAR is the contents of the FPA register on an MFAULT0; otherwise, it is the contents of MAR.	Sheet 15

CHAPTER 12
CPU-D BOARD

12.1 INTRODUCTION

The Model 3230 CPU-D Board, Part Number 35-770, contains the processor clock control, processor-to-memory logic, and memory control. It also has the EDMA protocol control, EDMA transceivers, EDMA-to-memory contention and mode logic, EDMA address and data registers, and the memory bus logic. In addition, the board includes the user's instruction and auxiliary instruction registers, instruction ROM format, calculate address logic, source, destination, and E field decoders, the repeat counter, input-output control, S bus buffers, and B bus multiplexors.

12.2 PROCESSOR AND MEMORY TIMING SIGNALS

Processor timing signals are derived from a 2-stage Johnson counter (Sheet 9) whose sequence is modified by the skip logic when memory is accessed. The two J-K flip-flops of the counter and the two D flip-flops of the skip logic are initialized by A System Clear (ACLR0) cn power up/down. OSC0, a 20 MHz square-wave, is the buffered output of a crystal oscillator and the toggle input for these flip-flops. Clock (CLK) and Skew Clock (SCLK) are each a buffered cutput of the Johnson counter. A1B1 is a decoded state of the counter.

When memory is not being accessed, the J input of FA is a function of the state of the FB flip-flop, and CLK and SCLK are square-waves of a 200 ns period (refer to Figure 12-1). A1B1 is active for 50 ns.

When memory is accessed, the processor timing is modified by the skip logic to accommodate the memory cycle. Figure 12-2 shows the waveforms of a processor-to-memory operation when no cache exists.

A memory cycle is started when the processor activates an Early Read Line (LER0 or SER0, Sheet 4). In response, the memory enables and then disables the Data Unavailable line (DUA0). DUA0 must be brought low before the trailing edge of CLK1, and when DUA0 is brought high by the memory, it must do so again before the trailing edge of CLK1. In addition, on the first falling edge of CLK1 after ER0, memory enables the Memory Busy line (LMBSY0 or SMBSY0) if memory has not completed its cycle at that time. The basic memory cycle without cache is 500 ns.

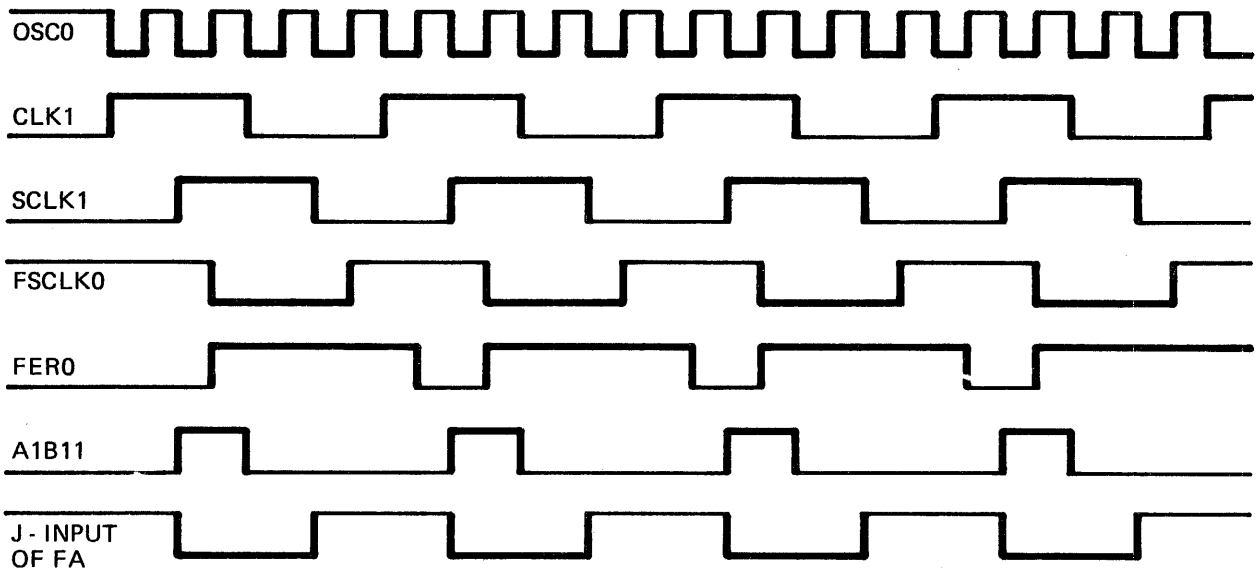


Figure 12-1 Processor Timing - No Memory Access

All memory, whether local or shared, has the same address and data bus. Local ERO (LERO) and Shared ERO (SERO) determine which memory is to be accessed.

A processor-to-memory operation (PMEM1) is decoded on Sheet 4 after the falling edge of CLK1. If no EDMA memory access is pending and the memory is not busy (HALTO high), the J-input of FA is now also controlled by FERO. An inactive FERO and HALTO and a decoded PMEM1 inhibits the Johnson counter from changing state for an interval of 50 ns - the period of the crystal oscillator. FER1 enables the LERO line (assume shared memory does not exist) nominally 25 ns before the rising edge of CLK1. The memory now enables DUAO and, if no cache exists, DUAO remains low until after the trailing edge of CLK1. On this edge, FDUA and FDUSKP are toggled set (Sheet 4) and the memory asserts the LMBSYO line which brings HALTO down. With FDUSKP set, FERO again controls the J-input of FA and causes the Johnson counter to remain in the reset state for an additional 50 ns. Before the trailing edge of CLK1, the memory removes DUAO, and FDUA and FDUSKP toggle reset on this edge. If DUAO is not removed, FDUA remains set but FDUSKP toggles reset and further skips are prevented for this memory cycle.

Normally, LMBSYO is removed on the CLK1 falling edge following the removal of DUAO. Memory can maintain LMBYSO active if it is not ready to accept another memory access in the following clock cycle or whenever it must perform a refresh operation. For refresh, no skips are performed.

Figure 12-3 shows the waveforms for a memory read access on a cache hit. Here, only one skip is performed, DUA0 is deactivated before the first CLK1 trailing edge after LER0, LMBSY0 is not asserted for this memory operation, and FDUA and FDUSKP never toggle set. Note also, in both Figures 12-2 and 12-3, that MDHCLK0 and MDLCK0 (Sheet 7) toggle the data into the processor's memory data register on a memory read operation.

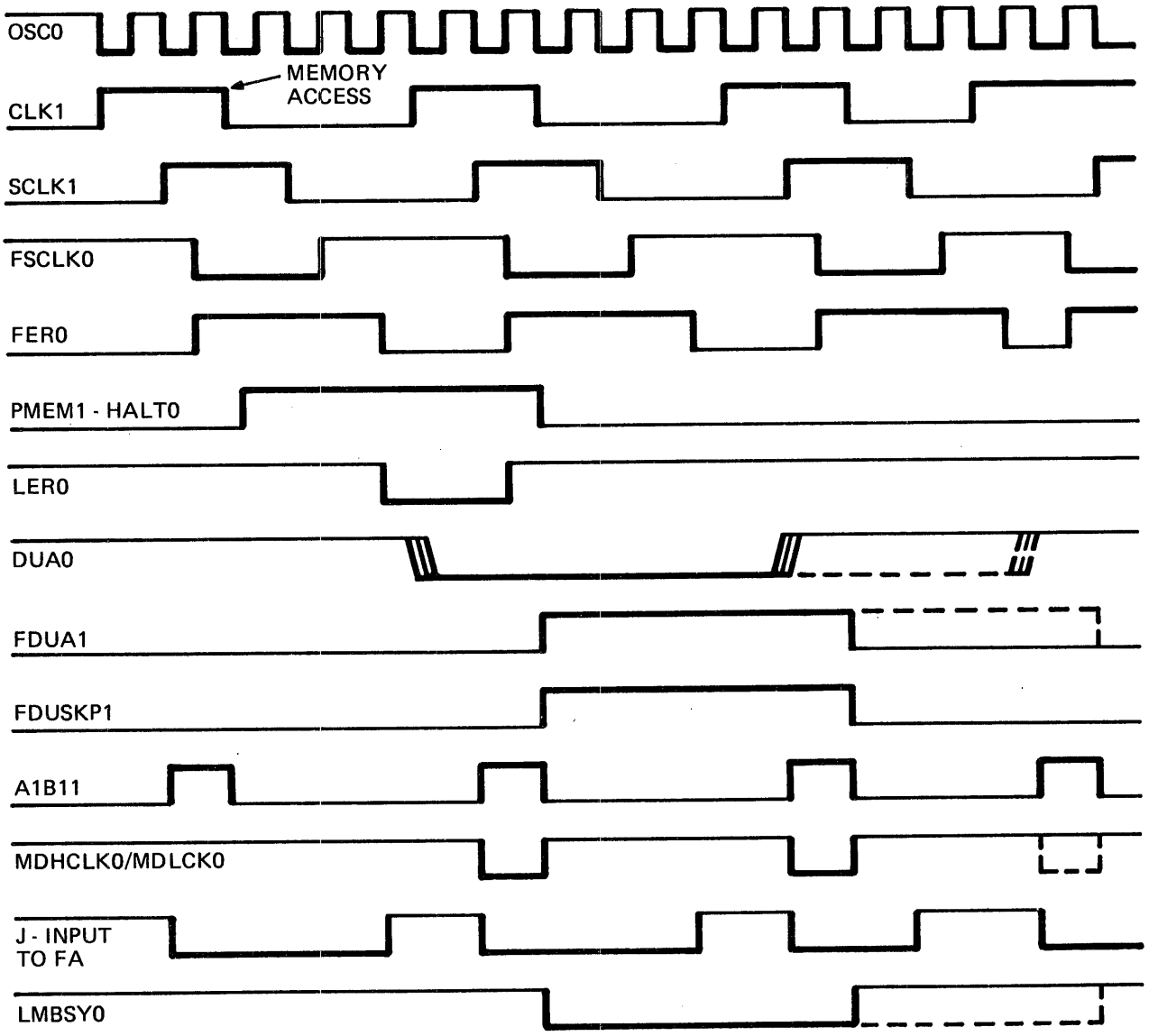


Figure 12-2 Processor Timing - Processor-To-Memory Access - No Cache

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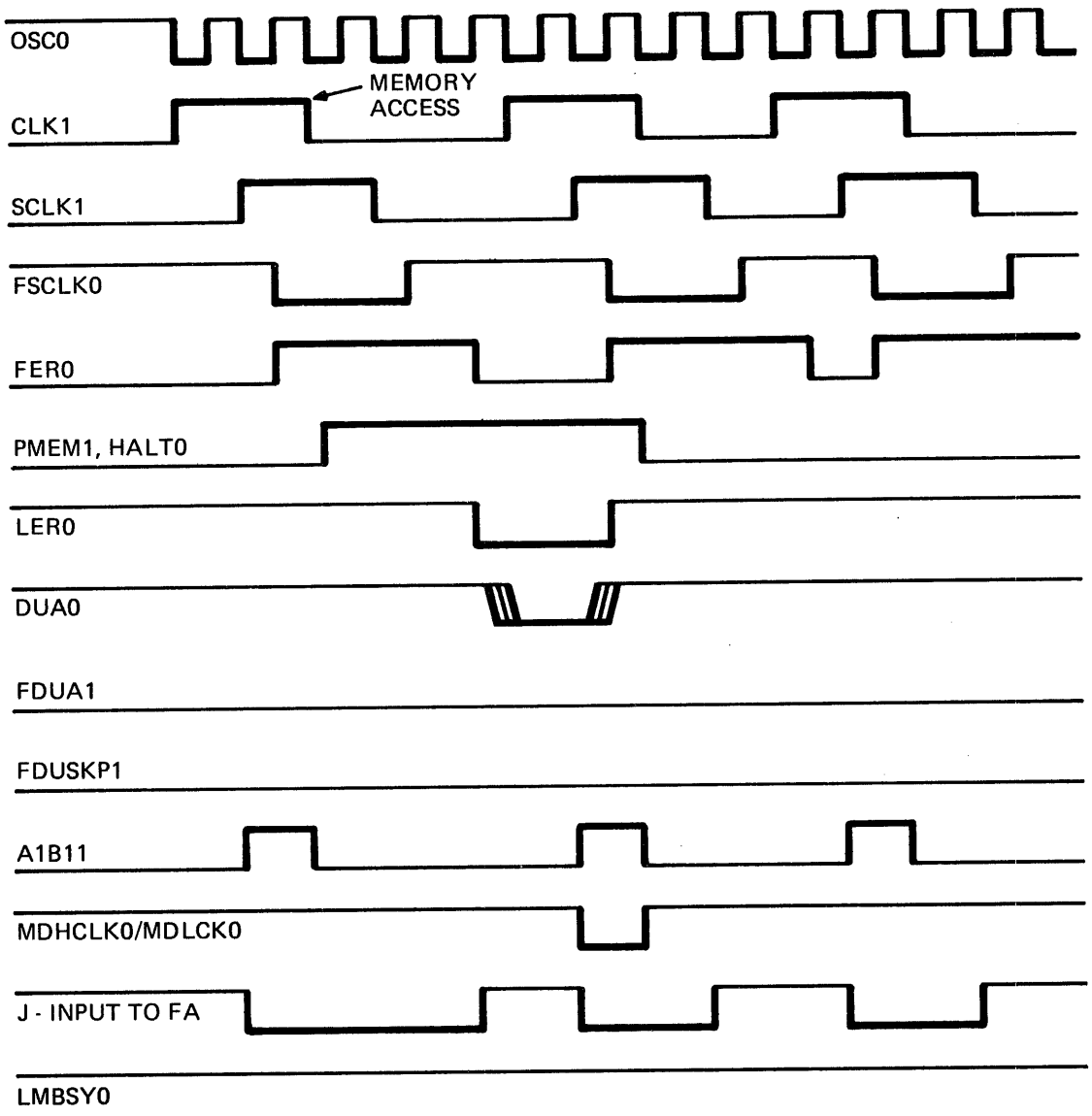


Figure 12-3 Processor - Processor-To-Memory Access - Cache Hit

12.3 PROCESSOR MEMORY OPERATION DECODE

Processor-to-memory operations are decoded from the memory control field of the microinstruction, RD00:03. Table 12-1 lists the operations specified by these bits.

TABLE 12-1 RD BIT OPERATIONS

RD BIT				OPERATION
00	01	02	03	
0	0	0	0	No Action
0	0	0	1	DW1 - Data Write Byte
0	0	1	0	PW2 - Privileged Write Halfword
0	0	1	1	DW2 - Data Write Halfword
0	1	0	0	TEL - Data Write Byte, No ECC
0	1	0	1	ENACLK - Enable Destination Clocks
0	1	1	0	PW4 - Privileged Write Fullword
0	1	1	1	DW4 - Data Write Fullword
1	0	0	0	Undefined
1	0	0	1	RAS - Read and Set
1	0	1	0	PR2 - Privileged Read Halfword
1	0	1	1	DR2 - Data Read Halfword
1	1	0	0	REL - Read Error Logger
1	1	0	1	IR - Instruction Read
1	1	1	0	PR4 - Privileged Read Fullword
1	1	1	1	DR4 - Data Read Fullword

Microinstructions are clocked on the trailing edge of CLK.

Decoded Memory (DMEM) is generated from RD00:03 on Sheet 4. Processor-to-Memory (PMEM) is asserted by DMEM0, a gated decoded instruction read (GGDR0), second part of instruction read (2IR0), gated second instruction read (GSIR0) or calculate memory address read halfword (CMR20).

Memory operations are more finely resolved on Sheet 6 where the result of the decoding is latched in a pair of quad-D registers. On power up/down, the registers are initialized reset by D System Clear (DCLR0). Latching is done on the leading edge of CLK1E and the clocking is inhibited if Processor Data Unavailable (PDUA0) is active. PDUA0 is always enabled/disabled on the trailing edge of CLK.

The quad registers store the following information about the memory access: Both Instruction Read (FBIR), Odd Instruction Read (FOIR), Even Instruction Read (FEIR), Read (FRD), Even Data (EVDAT), and fullword data. Instruction read accesses are contained in Set Calculate Address Part 1 (SCAP11), which is a function of GDIR0 and inhibited by ROM Stop (RSTOP0A). A Read operation is an active RD001 or CWR0 - change write to a read. A write is the complement of the read, provided the Instruction Register flip-flop (FINR0) is reset. Fullword data is signaled when RD011 and RD021 are both active and halfword data is signaled when either of these bits is inactive. CMR20 and DMEM0 serve as a gate enabling function.

On instruction reads and halfword data operations, program address bit 30 (PAR30) indicates whether or not the instruction to be fetched or the halfword data operation is on a fullword address boundary. If the instruction lies on a fullword boundary, FBIR is toggled set and a fullword is accessed. The first 16 bits of the readout are loaded in the instruction register and the second 16 bits are loaded in both halves of the Memory Data Register (MDR). If the instruction resides on an odd boundary (PAR 301 active), FOIR is toggled set, the halfword is accessed, and the second Instruction Read flip-flop (FSIR) is set on the trailing edge of MCLK0. The accessed 16 bits are stored in the instruction register and, if the instruction is not of a short-format (RR0 inactive), GSIR0 is generated and FEIR is toggled set on the next available CLK1E. The even halfword is accessed and loaded into both halves of the MDR. If the instruction fetched from the odd halfword is a short (16-bit) format (RR0), FEIR and GSIR0 are not enabled and memory is not accessed.

On a halfword data operation that is to be executed on a fullword address boundary, EVDAT gets set. For a halfword read, memory bus data bits 00:15 are loaded into 16:31 of the MDR, and for a halfword write, bits 16:31 of the MDR are asserted on memory data lines 00:15.

Outputs of the quad-D registers and their logical combinations generate Fullword (FW) and Read Fullword (RDFW). Gated Read (GRD) is generated from FRD when PDUA1 is active or HALT0 is high.

12.4 LOCAL/SHARED MEMORY

Local and shared memory are accessed over the same memory address and data buses. An access is initiated by activating an ER0 line. Each memory has a dedicated ER0 line - Local ER0 (LER0) and Shared ER0 (SER0), Sheet 4. In addition, each memory has a dedicated busy line - Local Memory Busy (LMBSY0) and Shared Memory Busy (SMBSY0) controlled by the respective memory. The Data Unavailable (DUA0) line is common to both.

LER0 and SER0 (Sheet 4) can be activated by the processor, the Memory Address Translator (MAT), or by an EDMA device.

12.5 PROCESSOR-TO-MEMORY

Figures 12-2 and 12-3 show the waveforms for a processor-to-memory operation with and without cache. All processor accesses are to local memory unless Processor to Shared Bank Controller (PSBC0), Sheet 4, is active. On a processor-to-memory operation (PMMEM1), if an EDMA bus operation is not pending (HALT0 high), the Enable MAT Access (ENMAA0), PSBC0, and LMBSY0A lines are inactive, and LER0 is pulsed low by FER1 if the Change Write to Read line (CWR0) is high. If PSBC0 is active, SER0 is gated low by FER1. In either case, if CWR0 is low, no ER0 can be sent.

If the processor must perform a MAT access of memory, ENMAA0 active inhibits the CPU path to the ER0 lines and enables the MAT path. Here again, PSBC0 determines whether LER0 or SER0 is to be gated.

Before an ER0 line is pulsed, the processor has output the memory address and, in the case of a write into memory operation, the memory data. On a write to memory, DAWT1 has been decoded and the write line (WRT0) enabled. In addition, Load Write (LWRT0), Sheet 7, outputs the memory data bits of the MDR to their respective MDS lines. For an even data halfword write (EDAT1), Load Halfword Write (LHWRT0) steers MDR bits 16:31 to MDS00:15.

For a processor read from memory, MDSB0, MDHSA1, and MDLSA1 (Sheet 7) steer the readout into the appropriate half or halves of the MDR. Memory Data Register Low Clock and High Clock, (MDLCK0 and MDHCLK0) toggle the MDR halves as a function of A1B11. MDR is loaded on the rising edge of MDLCK0 and MDHCLK0. MDHCLK0 pulses low for an RDFW, FBIR, or FEIR, and MDLCK0 during an FEIR or GRD. Note that the MDR clocks are present until FDUA is reset. When FDUA resets, the memory operation decode register changes state and disables the MDR toggles.

Periodically, the memory requires time to perform a refresh which is under the control of the memory logic. The memory cycle-steals a refresh cycle by asserting its memory busy line. As long as a busy line is active, no access to memory is attempted.

A local memory access to a cache-equipped memory is initiated as for a memory without cache; that is, ERO is generated as previously described, and memory asserts DUAO in response. On a cache hit, memory removes DUAO before the trailing edge of CLK1 when ERO is enabled. Refer to Figure 12-3 for timing waveforms. As a result, neither the FDUA nor FDUSKP flip-flops toggle set and the skip logic functions only once during this access. Cache readout is valid on the trailing edge of CLK1. Data is clocked into the MDR and/or IR as described above. Note that whether or not the access results in a cache hit, A1B11 always clocks the MDR on the first CLK1 for as long as PDUAO is held active.

12.6 PROTOCOL LOGIC TO ACQUIRE THE EDMA BUS

Bus occupancy on the EDMA is controlled by the EDMA Protocol Logic. Figure 12-4 shows the signals and nominal timing generated by the logic in response to a request for bus occupancy. The Extended Request (XREQO) line, common to all devices on the EDMA, is activated by a device that wants to use the bus. An active XREQO results in a QUEO which queues and synchronizes the requesting EDMA device to the protocol timing. Transmit Priority Chain (TPCO) is then sent. TPCO is connected to each device in a daisy chain fashion. A device that has not been queued sends TPCO to the next device on the bus. A queued device does not transmit TPCO. The EDMA device that has captured TPCO now must activate the Local Memory Request line (LMREQO) if it desires access to local memory; otherwise, the access will be interpreted as that for shared memory. The device that has captured TPCO is granted the EDMA only when the Start of Transmission (SOT) signal is received from the protocol logic. When the device is finished with the bus, it signals the protocol logic by sending an End of Transmission (EOT) signal, not shown in Figure 12-4.

The protocol logic is found on Sheet 6. It is separated into two parts:

1. Three flip-flops (twc D and one J-K) toggled by an LC oscillator, and

2. A quad-D register connected as a ring counter that is toggled by a separate L-C oscillator.

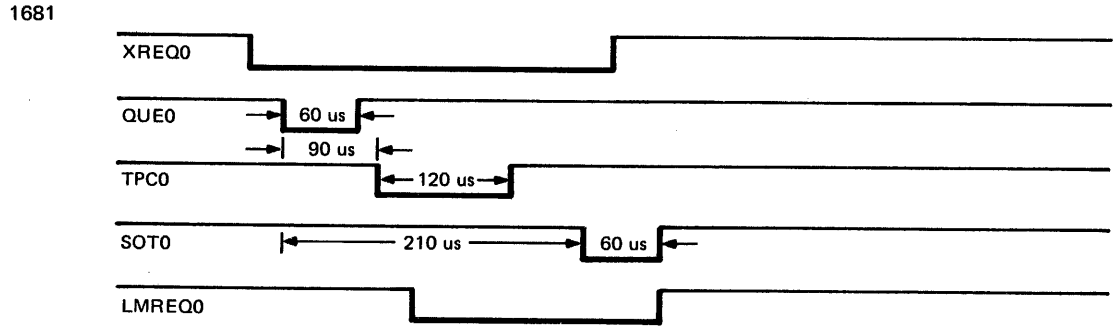


Figure 12-4 EDMA Protocol

Each oscillator is adjusted for a nominal 60 ns period. Figure 12-5 contains the waveforms for the protocol logic.

On power up/down, the C net of System Clear (CCLR0) inhibits the upper oscillator and forces the two D flip-flops clear. System Clear (SCLR1) (Sheet 8) forces FPC reset through Reset C (RESC0). This initialized state inhibits the lower oscillator and holds the quad-D register cleared. In the idle state, the clock inputs to all registers are low.

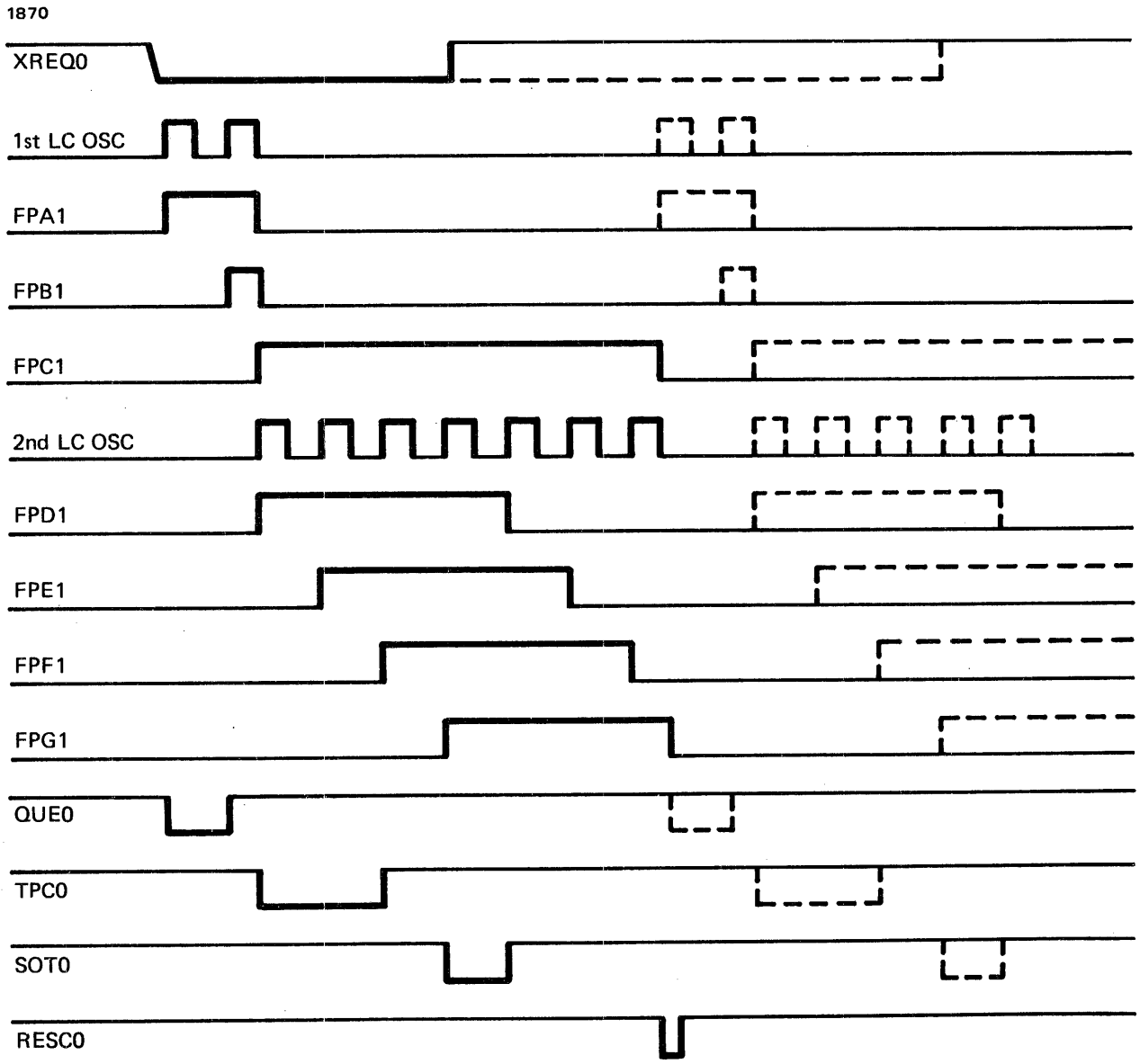


Figure 12-5 EDMA Protocol Logic Waveforms

On XREQ0, the forced clear is removed from the D flip-flops, and the upper oscillator is enabled. On the first rising edge of the buffered output of the oscillator, QUE0 is enabled and terminated on the next rising edge and the enabling of the lower oscillator starts. The next falling edge sets FPC which gates TPC0. FPC0 disables the upper oscillator, forcing the D flip-flops reset and removes the low from the clear inputs of the quad-D register. This register also changes state on the rising edge of the buffered oscillator output. TPC0 is disabled when FPF is set. SOT0 is gated when FPG is set and terminated by the cleared state of FPH.

The protocol logic returns to the idle state when RESC0 goes active. RESC0 (Sheet 8) is pulsed low by the protocol oscillator (PROSC1) during the interval when FPG is set and FPD reset. A reset FPC disables the lower oscillator, holds the quad-Ds cleared, and allows another protocol sequence to start if XREQ0 is active.

The width of TPC0 is increased if an EOT has not been received in response to the previous SOT0 to clear FEOT (Sheet 8). Hold Start (HOST1) inhibits the transmission of SOT0 (Sheet 8) if a burst mode to local memory is being executed; or if an EDMA device is waiting for an answer from memory [(FLADR+FLADRA)•FERD+DMASEL•FERD+ENACSC].

Test points are available for maintenance and factory use.

P5 pull-up resistor = TPH, TPC, TPE, and TPF
GRD = TPD

NOTE

TPC and TPD are normally strapped.

12.7 EDMA BUS TRANSMISSIONS

When the selected device has received an SOT0, it must output an address and a memory control field followed by a Load (LOAD0) pulse. If the access is a read from memory, LOAD0 is accompanied by an End of Transmission (EOT). If the access is a write, EOT is not sent with the address LOAD0; rather, after the address, the device outputs a halfword of data followed by a LOAD0. On a halfword write, an EOT is sent with this LOAD0. However, on a fullword write, an EOT is not transmitted until the device outputs the second halfword, and then outputs a LOAD0 with EOT. (Refer to Figure 12-6).

When a memory outputs a halfword readout, it also sends two bits to identify the responding memory, a parity error bit, and a memory malfunction bit. This is followed by an Answer (ANS0) pulse. On a fullword read, another halfword is sent, also followed by an ANS0.

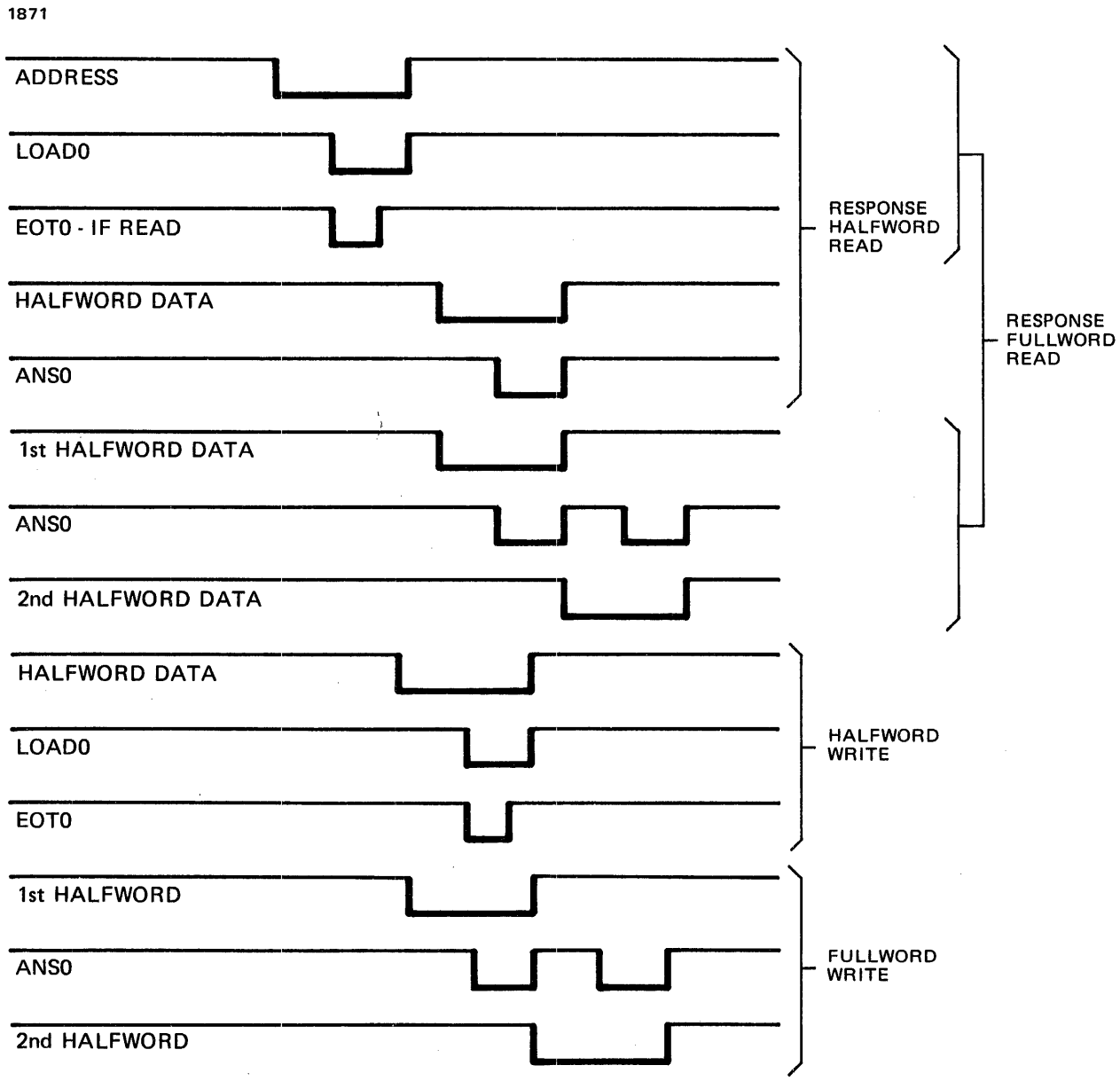


Figure 12-6 EDMA to Memory

12.8 EDMA TO MEMORY

An EDMA request to memory is indicated by XREQ0 (Sheet 2) which is activated by the EDMA device (refer to Figure 12-7) and directly sets FMREQ. The state of FMREQ is synchronized by the edges of A1B11 (Sheet 2) and the double-ranked quad-D registers to the processor timing. On synchronization, HALT is generated to prevent the processor from accessing local memory on the next available memory cycle. When the device is granted the EDMA bus via SOT0, FSOT is set and generates LDMAL0 (Load EDMA MAR) (Sheet 7) and enables the ILDMA0 (Increment or Load MAR) gate. FSOT also enables the D input of FLADR (Load EDMA Address Register) (Sheet 2).

The EDMA transceivers, memory address register (EDMAR), the data register (EDMA MDR), LMA bus drives, and the data bus logic are found on Sheets 15-18.

FLADR sets on the leading edge of LOAD0. ILDMA0 goes high to load the memory address; HOST1 goes active; and the memory control field (DMA15:17) is loaded into the D registers (Sheet 5). In addition, the state of FLADR is synchronized to the processor timing. If the stored DMA15:17 bits indicate a read from memory (FERD1), the trailing edge of SCLK1 enables DMASEL if memory is not busy. The decision to select DMA to local memory (DMALM1) or DMA to shared memory is determined by the FLMRQ0 state which was set by SOT0. A low FLMRQ0 is an EDMA to local memory and a high to shared memory. However, if a read of memory is not indicated (FERD0), EEDCLK0 (Even EDMA Data Clock) is low (FLADRA0 inactive), and/or if a halfword write is to be performed (FEFW0 and DL301D), OEDCLK0 (Odd EDMA Data Clock) is low (Sheet 7). The leading edge of the LOAD0 for the first halfword of data sets FLDARA (Load EDMA Data A) and the data loaded into the EDMA MDR and FLDARA0 keeps HOST1 active. The state of FLDARA is also synchronized to the processor clocks for a write halfword. On synchronization, DMASEL would be asserted on the trailing edge of SCLK1 if the memory is available.

If the EDMA request is neither a read nor write halfword, a fullword write is indicated (FEFW1). With EDMA Fullword Write (EFWRT1) active, OEDCLK0 is low. On the leading edge of the second data halfword LOAD0, FLDARB toggles set and OEDCLK0 clocks the data into the lower half of the EDMA MDR. The state of FLDARB is synchronized to the processor timing. On synchronization, DMASEL1 is asserted on the falling edge of SCLK1 if the memory is available.

When DMASEL1 goes active, the skip logic comes into play to modify the processor timing as described in Section 12.2. DMASEL1 and DMBZY1 (the latter on Sheet 2) perform the first skip; FDUSKP1 and FER0 perform the second skip.

For a write operation, DMASEL1 and FERD0 enable WRT0 to memory (Sheet 4) and DMAWRT0 (Sheet 7) to output the EDMA MDR to the memory data bus (Sheet 7). An EDMA halfword operation to memory is signaled by DMAHW0 (Sheet 5).

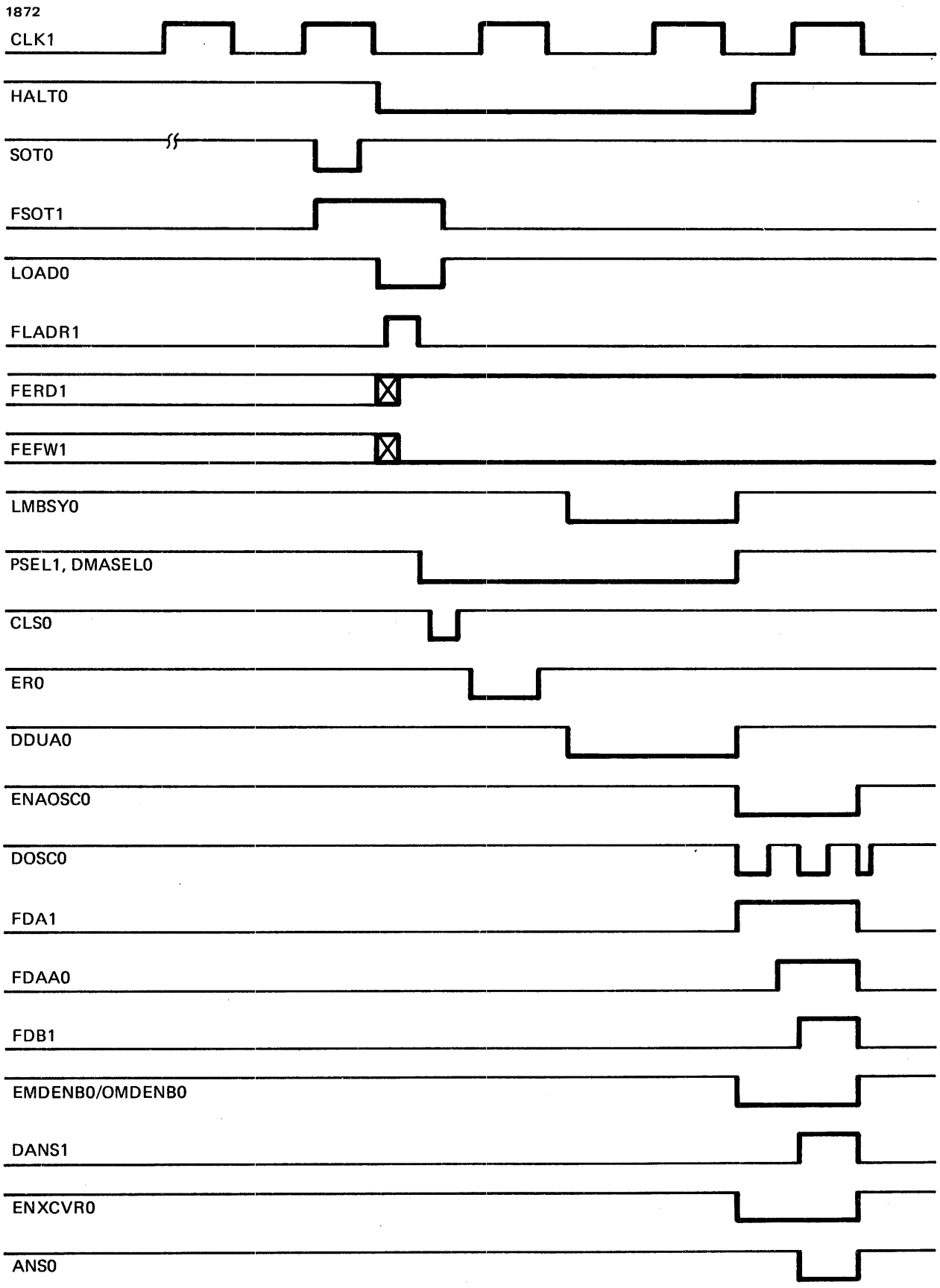


Figure 12-7 EDMA to Memory - Halfword Read

For a read operation, FERD1 and FERD0A (Sheets 17 and 18) steer the MDS. This data register is loaded on the trailing edge of CLK1D during DDUA1 (DMA Data Unavailable) via EEDCLK0 and OEDCLK0 (Sheet 7) lines to the EDMA MDR input.

CLS0 is asserted immediately after DMASEL1 goes high by DMBZY1, FB0, and FSCLK1 (Sheet 2). CLS0 directly clears FMREQ, FSOT, and the LMRQ0 latch. This signal also gates CLAD0 (Clear Address and Data flip-flops) (Sheet 7) to clear FLADR, FLDARA and FLDARB if a Burst Read (BRTRD0) is not being processed.

On an EDMA read, the memory to EDMA control logic (Sheet 5) (Figures 12-7 and 12-8) will transmit the readout to the EDMA device. The output of the 5-input NOR gate is normally low. It goes high for an EDMA read (FERD1) but not a burst mode (BRST1) during an active DDUA0. At this time (CLK1), the J-K flip-flop sets to generate ENOSC0 (enable oscillator). The set state also removes the low clear on the 3-stage Johnson counter. ENAOSC0 starts DOSC0 (DMA Oscillator) (Sheet 3) and enables the transceiver via ENLAND0 for ANS0. The state of the Johnson counter and the steering logic on Sheet 8 generate EMDENDB0 (Even Data Enable), OMDENB0 (Odd Data Enable), and DANS1 (DMA Answer). DANS1 drives the ANS0 line of the transceiver. The transceivers that transmit the answer to the EDMA are enabled by ENXCVR0.

1688-1

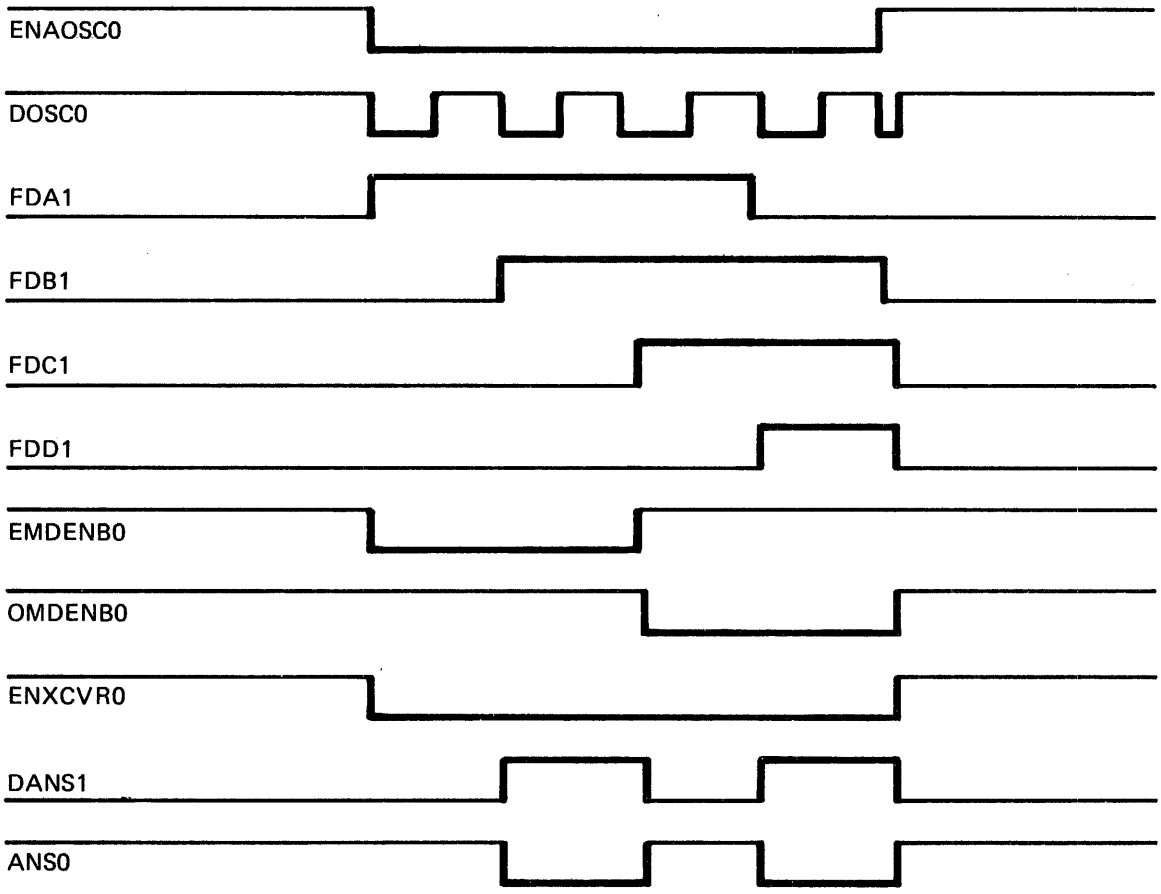


Figure 12-8 LM to EDMA Answer - Fullword Read

For a fullword read, EMDENB0 is activated when FDA sets and DANS1 is activated by FDB1. These signals terminate when FDC sets; this enables OMDENB0. DANS1 is again enabled when FDA resets. Both OMDENB0 and DANS1 are disabled when FDB clears.

For a halfword read from an even memory address boundary, EMDENB0 outputs the data to the EDMA device. On a halfword read from an odd boundary, OMDENB0 enables the data to the EDMA bus.

The oscillator is stopped by logic that examines the memory mode of operation and the state of the counter. For a halfword or fullword read, ENOSC0 is driven high when the last ANS0 pulse is disabled. The J-K flip-flop that disables ENOSC0 clears the J-K that began the sequence. The reset state of this J-K initializes the counter and the last J-K is forced to the clear state.

A burst mode operation on the EDMA bus requires handshaking between the processor and the requesting device. This handshaking is performed over the LOAD0 and ANS0 lines. The requesting device always sends LOAD0 and the processor sends ANS0.

In a burst read mode and in response to ANS0, the device transmits LOAD0 to the processor to indicate that the device is ready to receive another fullword. If the device requires no additional data, it then transmits EOT to signal the end of the burst read mode.

In a burst write mode, the processor transmits an ANS0 to indicate that it can handle another fullword of data to store in memory. In response, the device transmits a fullword of data. With the last fullword to be written in memory, the device also sends EOT to signal the end of the burst write mode.

The first fullword write of a burst write operation begins as a normal EDMA fullword write to local memory. However, when ST1 pulses high because of CLS0 and BRWRT1 (the decode of the EDMA memory operation field) direct sets the J-K flip-flop to enable the oscillator (ENAOSC0), DOSC0 toggles the Johnson counter and FDA1 gates DANS1 (Sheet 8) to output ANS0 through the enabled transceiver. The device responds with two halfwords of data and two LOAD0s. With BRWRT0 and FEFW1 active, the LOAD0s set FLDARA and FLDARB in turn and another EDMA to local memory request is synchronized to the processor timing. ENAOSC0 is disabled after ANS0 and the local memory to EDMA control logic is initialized reset. During the first fullword store of the burst write, DDUA1 and CLK1F toggle FBRWRT set. When the device transmits the last fullword of the burst write, it also sends EOT which, with BRWRT1, changes the memory control field from a burst write mode to a fullword write. The last fullword is then stored as a normal fullword write.

If a Burst Read (BRTRD) mode is decoded, CLADA0 is inhibited from being pulsed by ST1 (Sheet 7). As a result, FLDAR remains set, still synchronized to the processor timing. During the first fullword read of the burst read, DDUA1 and CLK1F toggle FBRTRD set. At the same time, ENAOSC0 is enabled to output the first fullword of data to the device. When FDA sets, CLADA0 is enabled to clear (FLADR) and disabled when FDAA sets. The fullword of data is transmitted to the device as for a normal EDMA fullword read. In response to ANS0, the device sends a LOAD0 to signal for another fullword read. If LOAD0 is not returned before the next memory cycle becomes available, due to the fact that FLADR resetting is delayed, FLADR1 is still stored in the quad-D register (Sheet 2). DMASEL remains active and the next fullword is read from memory. During this access, FDRDY gets set to indicate that valid data resides in the EDMA MDR. Whenever FLADR is toggled set by the handshaking LOAD0, ENAOSC0 is enabled by FBRTRD1oFLADR1oFDRDY1. On the last fullword transmission of a burst read, the device sends EOT which gets synchronized as FQEOT (Sheet 2) and changes the EDMA memory control field to a fullword read.

The EDMA memory address register is incremented (ILDMA0) during burst modes on the trailing edge of DDUA1 after FSOT is cleared (Sheet 7).

12.9 CLOCK STOPS

Clock stops are used to inhibit microprocessor clocks for an event requiring more than one clock period. There are three types of clock stops that suspend different levels of processor functions. Destination clock stops (DSTOP) inhibit the loading of data into a destination register. ROM clock stops (RSTOP) inhibit the loading of a new microword into the ROM data register and prevent the CSAR address from changing. Memory clock stops (MSTOP) stop all microprocessor functions. DSTOP and RSTOP are forced active by MSTOP. Refer to Sheet 9 of Functional Schematic 35-770D08 during the following breakdown of the signals causing DSTOP and RSTOP.

MFAULT0 — Memory fault causes DSTOP to inhibit the loading of destinations after a memory fault. This condition remains in effect until the memory fault is serviced.

BRANCH0 — Branch causes DSTOP to prevent the loading of random data into random registers.

OPTSTP0 — Option stop causes both DSTOP and RSTOP during operations with the Writable Control Store (WCS) or the High Performance Floating-Point Processor (HPFPP). Option stop remains active until the WCS or HPFPP operation is complete.

AFINR0	This signal causes DSTOP during the second half of the RX squared calculate address. This signal prevents the source string address contained in the shift register from being destroyed.
CMR20	This signal causes DSTOP and RSTOP during the calculate address of the RX3 or RI2 formats.
IOSTOP0	I/O operation in process stop. Both DSTOP and RSTOP are made active until the I/O Sync is received.
2IR0	This signal is generated during the beginning of the second part of the RX squared format address calculation and causes DSTOP to save the shift register contents.
AMSTOP0/BMSTOP0	Memory contention signal that causes DSTOP and RSTOP during the period of contention.
RX2STP0	Stop generated during calculate address of an RX2 format instruction. This stop causes RSTOP and allows the location counter to be incremented to point to the next instruction.
RX3STP0	RX3 format calculate address stop that causes RSTOP to remain active.
CNTE00	Counter not equal to zero. When the repeat counter is loaded, RSTOP remains active until the count is reduced to zero.
GMATSTOP0	This signal activates both DSTOP and RSTOP when the MAT needs to access memory.
COMSTP0	Communication stop asserts DSTOP and RSTOP for loading into the communication hardware assist board.
NOCNT0	Causes a DSTOP for one clock period if repeat counter is loaded with a zero value.

Memory Stop (MSTOP) occurs if a memory access is attempted by the processor (PMEM1) or the MAT (GENMAA1), and the desired memory is busy (LMBSY1/SMBSY1). MSTOP is also activated if the MDR is specified as a source (UMDR1) and a memory operation is in progress (PDUA1). In addition, the clock single-step control test feature causes FTIT1 as long as TRAP0 remains active to control MSTOP. Depressing the advance pushbutton disables FTIT1 for one clock period. MSTOP also activates if the processor (PMEM1) is trying to activate a memory cycle but an EDMA port has won contention for the memory (HALT1).

12.10 INSTRUCTION REGISTER AND AUXILIARY INSTRUCTION REGISTER

The Instruction Register (IR) is a 16-bit register that is loaded with the user-level instruction to be emulated. The IR is broken into three major segments. An 8-bit operation code (OP CODE) defines the format (RR, RI, or RX) and an address location within the DROM on CPU-A. (Refer to Sheet 11 of 35-770D08.) The DROM address extracts the microprogram address of the emulation sequence. Two 4-bit fields are called the user general register destination (YD) and the user general register source or index (YS). These 4-bit fields select one of 16 general registers on the CPU-B board. (Refer to Sheet 3 of 35-770D08.)

The Auxiliary Instruction Register (AIR) is a 12-bit register used during the RX squared format instructions. (Refer to Sheet 12 of 35-770D08.) The first eight bits are the operation modifier code. The remaining four bits are used by the microprogram as a data constant. The AIR may be examined by unloading the YSI field of the IR after the calculate address of an RX squared format. After reading the contents of the AIR, it is cleared.

12.11 FORMAT DECODING

Format decoding controls the operation of the calculate address. There are four basic formats of user-level instructions, register-to-register (RR), immediate data-to-register (RI), memory data to register (RX), and string manipulation (RX squared). The format type is decoded from the OP CODE portion of the IR. The 8-bit OP CODE field is used to select a 4-bit word within the format ROM. The state of the four data outlines determines the format currently being executed. The RI1 format is implied by the default (all four outputs inactive) of the format ROM outputs. The format ROM output that indicates an RX format is further decoded into three RX formats: RX1, RX2, and RX3. The state of MDR bits 00, 01, and the RX format ROM output selects one of the three RX formats.

12.12 CALCULATE ADDRESS

The calculate address is initiated by a microprogram specified Instruction Read (IR). The calculate address logic resolves the format requirements of the current user instruction being executed. At the conclusion of the calculate address, the following conditions exist, depending on the selected instruction format:

RR — The Shift Register and the MAR equal the contents of the general register specified by the YS field.

RI1 — The Shift Register and the MAR contain the 32-bit data resulting from the addition of the contents of the general register specified by the YS field and the sign extended least significant 16 MDR bits.

RI2 — The Shift Register (SR) and the MAR contain the 32-bit data resulting from the addition of the contents of the general register specified by the YS field and the full 32 bits of the MDR.

RX1 — The Memory Address Register (MAR) and the SR contain the program address of the second operand data contained in memory. This address is the result of adding the sign extended least significant 16 bits of the MDR and the data contained in the general register specified by the YS field.

RX2 — The MAR and the SR contain the program address of the second operand data contained in memory. The program address is the result of adding the contents of the general register specified by the YS field, the sign extended least significant 16 bits of the MDR, and the incremented contents of the location counter. Bits 0:19 of the SR are undefined.

RX3 — The MAR and the SR contain the program address of the second operand data contained in memory. The program address is the result of adding the contents of the general registers specified by the YS field and MDR bits 4:7 and the least significant 20 bits of MDR. Bits 0:19 of the SR are undefined.

RX Squared — The SR contains the program address of the source data string. This address is generated during the first half of the RX squared format in the same manner as defined by the RX1, RX2, or RX3 formats. The MAR contains the program address of the destination data string. This address is generated during the second half of the RX squared. The address contained in the MAR is the result of addition in the same method as RX1, RX2, or RX3.

The microword contained in the RD register during the calculate address is an Add operation. The SR is the destination. The general register specified by the YS field is the A bus source, and the MDR is the B bus source. Instruction Read and MDR sign extend are also specified. The MAR is forced to be a destination during calculate address.

Figures 12-9 through 12-16 are examples of the logic sequences during calculate address. All the figures show examples when there is no memory contention and the data access is ideal (cache hit). The microprogram and the calculate address are suspended as required (MSTOP0). Refer to Sheets 10 and 11 of 35-770D08 during this description.

Figures 12-9 and 12-12 depict the sequence required for RR, RX1, or RI1 formats. Figure 12-13 differs in that the fullword instruction (RX1, RI1) starts on a halfword boundary and must therefore initiate two memory cycles to fetch the required 32 bits. GGDIR1 becomes active when the microword specifies an IR and if no repeat counter operation is in progress or no interrupts were queued during the previous instruction execution. The next CLK1 causes a memory read to the address specified by the Location Counter (LOC). The LOC is incremented (ILOC) at the trailing edge of CLK1. The ALIR1 flip-flop is direct set during CLK1. This allows the IR to be loaded when the memory data is available (DUA0). The FINR1 and CAP1 flip-flops are set at the trailing edge of CLK1. The format of the instruction is determined by the contents of the IR (if it is an RX format) and MDR bits 0 and 1. The instruction format determines if DISA0 or DISB0 is active. Disable the A Source (DISA0) is active on RX or RI formats if the YS field of the IR is zero. When the YS field is zero, no index value is to be added. When DISA0 is active, the A bus source data is forced to be inactive. This results in the MDR being added to zero. RR format instructions disable DISA0. The YS field equal to zero is a valid A bus source for RR instructions. Disable the B Source (DISB0) is made active by the RR instruction format. The MDR is specified by the microword to be the B source data. The MDR is invalid for RR instructions. DISB0 forces the B bus data to be inactive. The contents of the general register by YS are added to zero. The LOC is incremented (ILOC) on the first clock after CAP1 is set by FCP1 if the format is not RR. FCP1 ensures that ILOC occurs for only one clock period.

In Figure 12-12, in addition to the previous description, GSIR0 becomes active on the same CLK1 that FINR1 sets. GSIR0 indicates that a second read is initiated. The data contained in the MDR is not valid until the second read, when memory data is available. The calculate address is suspended until the MDR is valid. The GDIR0 signal is inhibited by the RR format decoding.

The final CLK1 of the calculate address loads the SR and MAR with the result of the microinstruction Add operation. The CSAR is loaded on the leading edge of CLK1 with an X'007' if a memory fault occurred during the calculate address or if the instruction in the op-code is not an exercised option; e.g., HPFPP or WCS. If no memory fault exists and if the instruction is legal, the D1 address vector, as selected by the op-code data, is loaded into the CSAR.

Figures 12-10 and 12-13 are examples of calculate address for the RX2 format. The RX2 format starts the same as RX1 and is decoded during FCP1 and causes RX2STP0. RX2STP0 keeps CAP1 from resetting on the next MCLK1A. This allows LOC to be incremented before it is added into the address calculation. The MDRE0 signal becomes active during CAP1 when the RX2 format is decoded. The MDRE0 causes the MDR data on the CPU-C to be added to the incremented LOC which is available on the output of the PA multiplexor. The MDR source data on the B bus reflects the results of the addition. The SR and MAR are loaded with the results of adding the contents of YS and the MDR adder output. Figure 12-13 shows the effect of GSIR0 on the RX2 format.

Figures 12-11 and 12-14 are examples of calculate address for 48-bit instructions, RX3 and RI2. RX3 and RI2 format instructions use the full 32-bit MDR to complete the calculate address. The calculate address for RX3 and RI2 formats is in two parts, defined by CAP1 and CAP2. During CAP1, the LOC is incremented, the format is decoded, and the contents of the general register specified by the YS field are loaded into SR and MAR. The B bus source data is disabled (DISB0) as it was during RR formats. RX3STP0 suspends the microprogram during the CAP1 cycle. CMR20 and CAP21 beccme active on the same MCLK1 that CAP1 resets. CMR20 causes a halfword memory read to fetch the remaining 16 bits for the least significant 16 bits of the MDR. CMR20 also causes the LOC to be incremented to reflect the 48-bit instruction length. The RI2 format causes the 32-bit MDR, when it is valid (DUA0), to be added to the contents of YS and is loaded into SR and MAR. The RX3 format causes MDRE0 to become active, enabling the MDR adder on the CPU-C. CAMA0 goes low when CMR20 is inactive and CAP2 is active. This selects the contents of the MAR on the outputs of the PA multiplexor of the CPU-C. During CAP2, with the RX3 format, X20 goes low, enabling MDR bits 4:7 to select the second level index general register. The final clock of the calculate address loads the added result of the contents of the general register specified by MDR bits 4:7 and the MDR adder output. The MDR adder output consists of the contents of the MDR and the contents of the general register specified by YS, which was loaded into the MAR during CAP1. The most significant 12 bits of the MDR adder output are undefined. Figure 12-14 shows the effect of GSIR0 on 48-bit formats. GSIR0 is caused by starting the instruction on a halfword boundary.

The RX squared instruction format requires two calculate address sequences. Each calculate address operation is essentially an RX format calculate address. The back-to-back calculate address sequences may each be RX1, RX2, or RX3 format. The result of the first calculate address is contained in the SR. The second result is loaded into the MAR. Figures 12-15 and 12-16 are examples of the RX squared format calculate address. Figure 12-15 shows the sequence for an RX1 followed by an RX1. Figure 12-16 shows an RX1 followed by an RX3. In either figure, there are few differences between the previously discussed RX format calculate address and the individual RX formats calculated in the RX squared. The MCLK1 that causes CAP1 to reset in the first calculate address loads the SR and MAR with the RX1 address data. 2IR0 becomes active because of the RX squared format. BLIR1 sets on the leading edge of MCLK1 and the memory read for the second RX format is started. ALIRCK0 enables the Auxiliary Instruction Register (AIR) and the YS field of the IR (Sheet 12 of 35-770D08) to be loaded when the memory data becomes available. DSTOP0 is held active by 2IR0 and AFINR1. This prevents the address data contained in the SR from being overwritten. MARSTP1 enables the MAR to be loaded when DSTOP is active.

The Length Counter (Sheet 11) is incremented each time the LOC is incremented. This provides an instruction length count at the conclusion of calculate address. The length counter is cleared at the beginning of each instruction read.

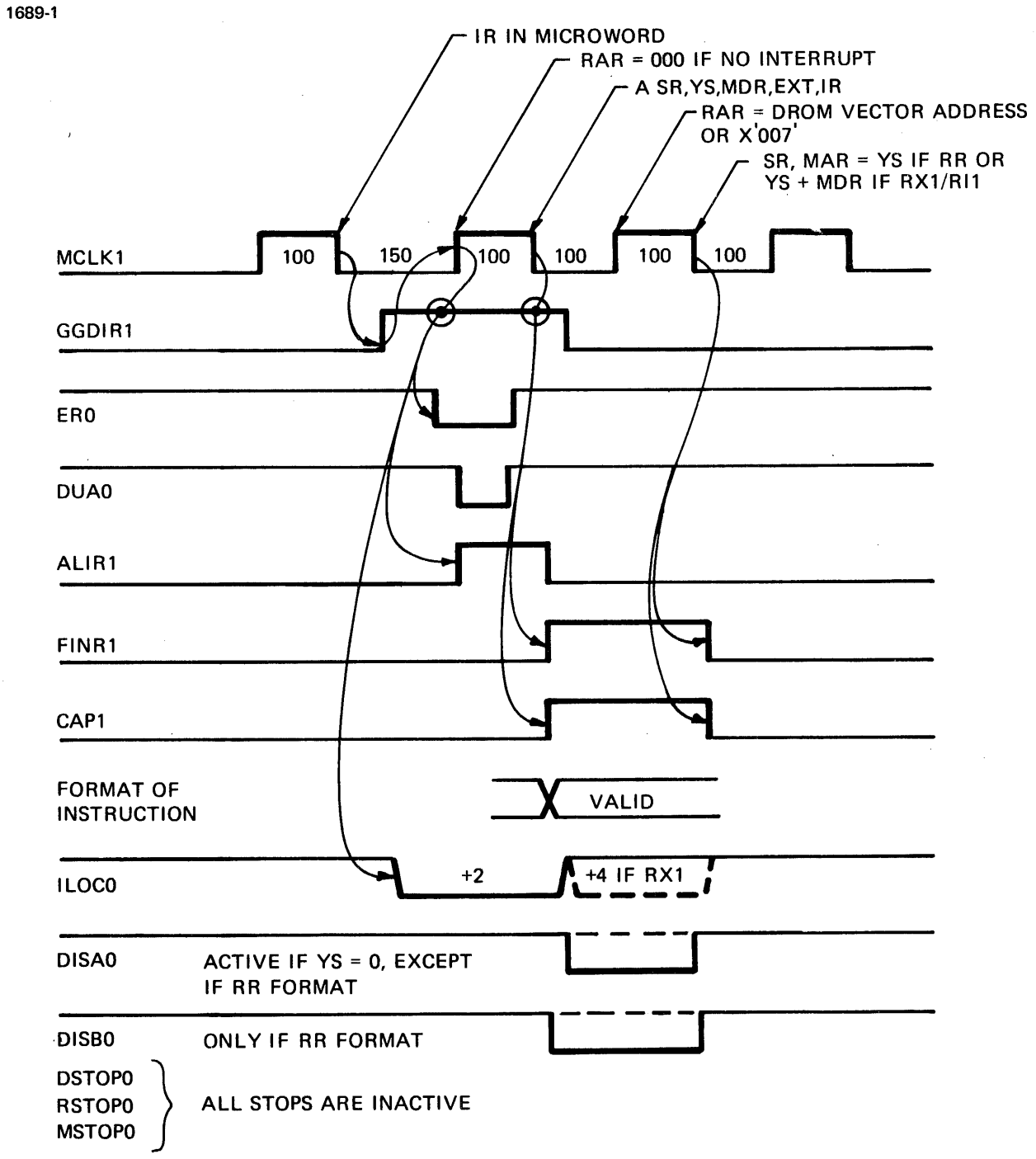


Figure 12-9 RR, RX1, or RI1 Format (Cache Hit on Fullword Boundary)

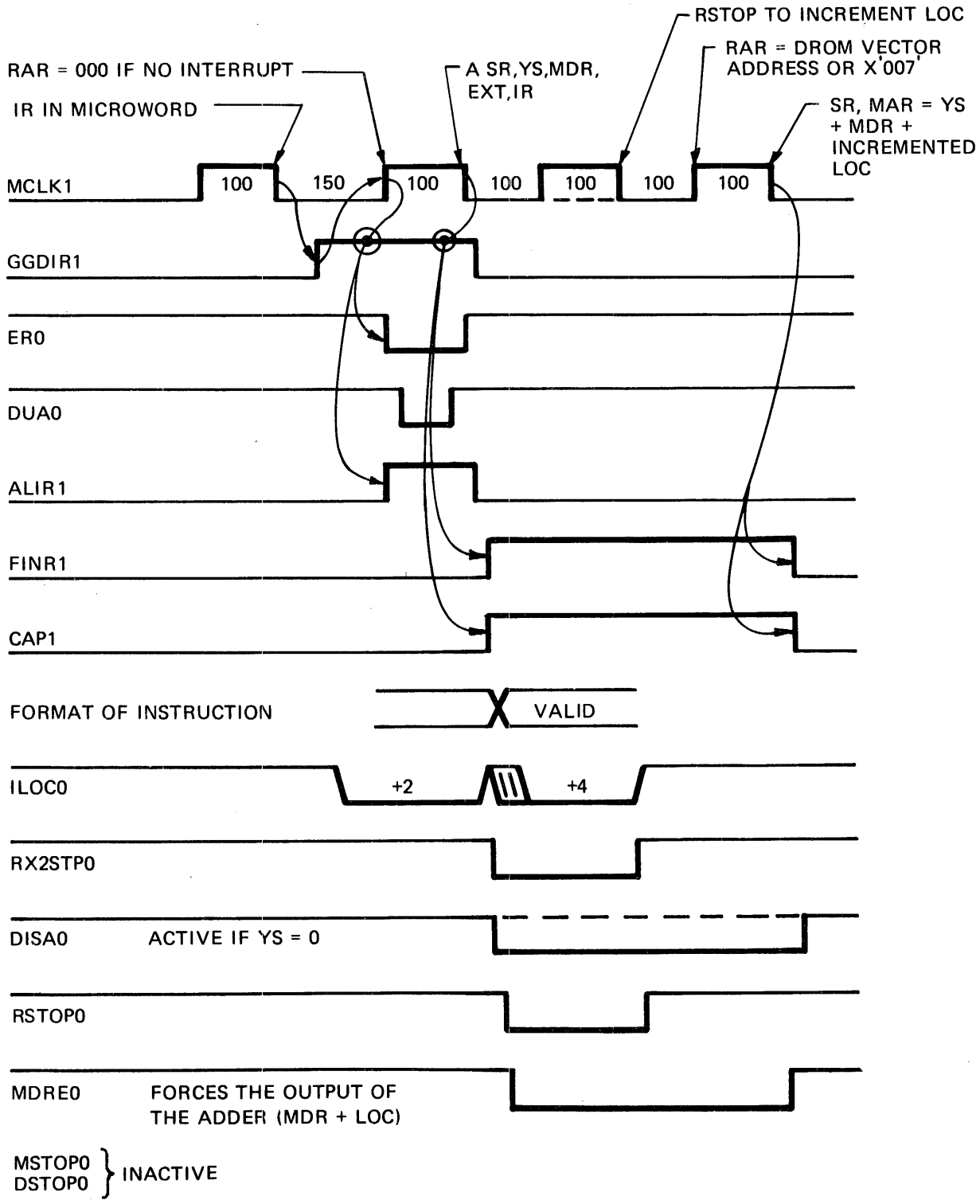


Figure 12-10 RX2 Format (Cache Hit on Fullword Boundary)

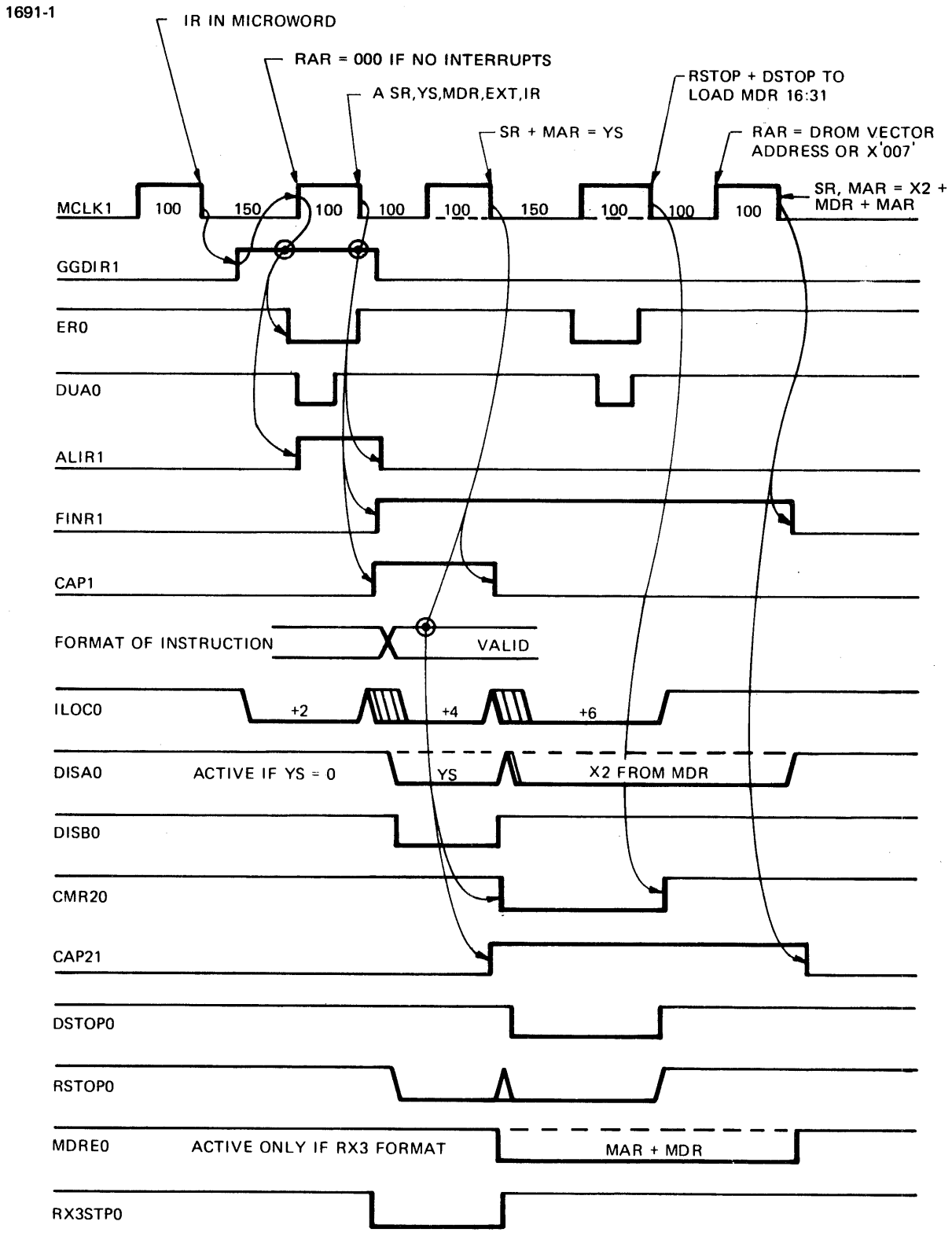


Figure 12-11 RX3 or RI2 Format (Cache Hit on Fullword Boundary)

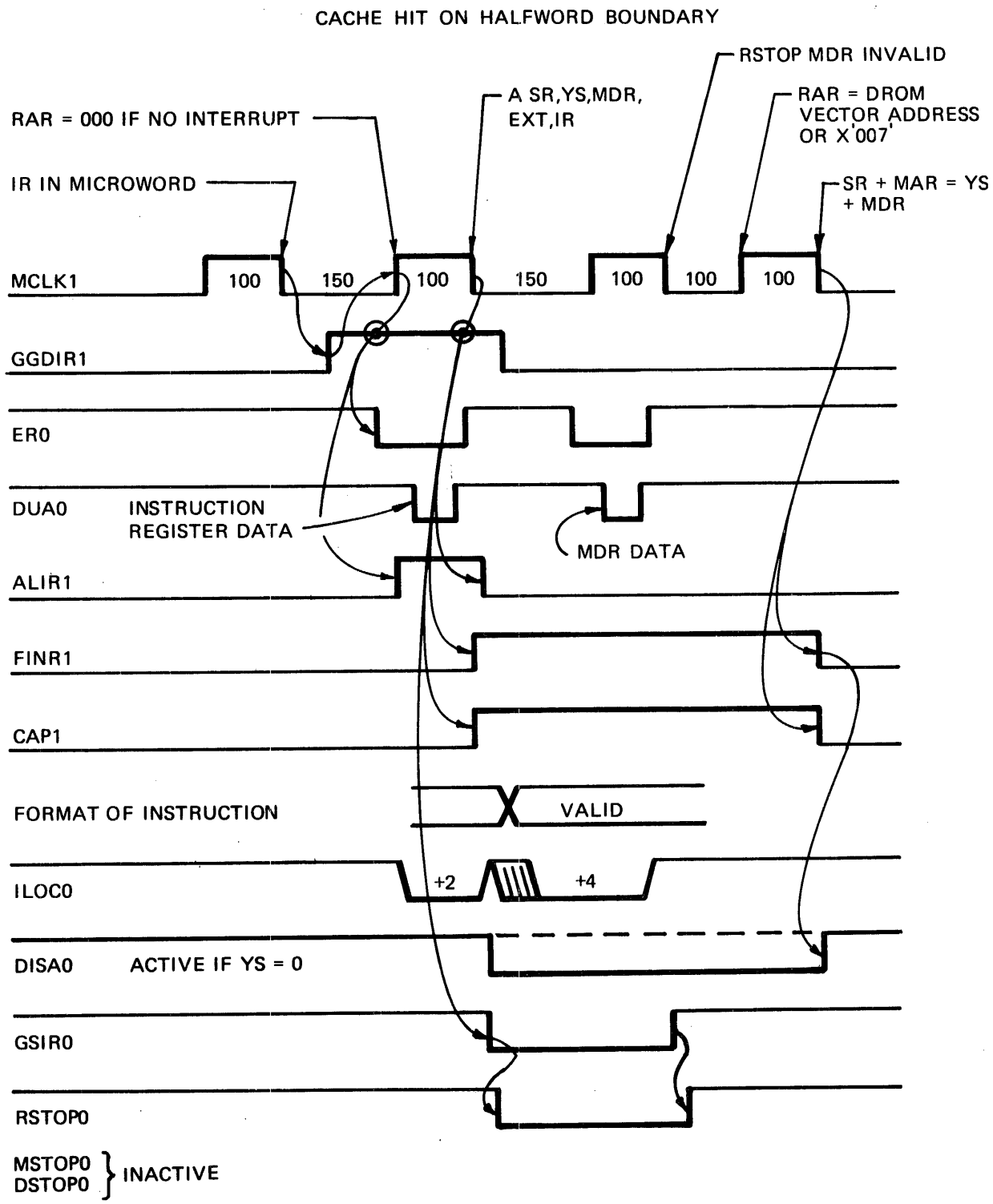


Figure 12-12 RI1 or RX1 Format

RX2 FORMAT
CACHE HIT ON HALFWORD BOUNDARY

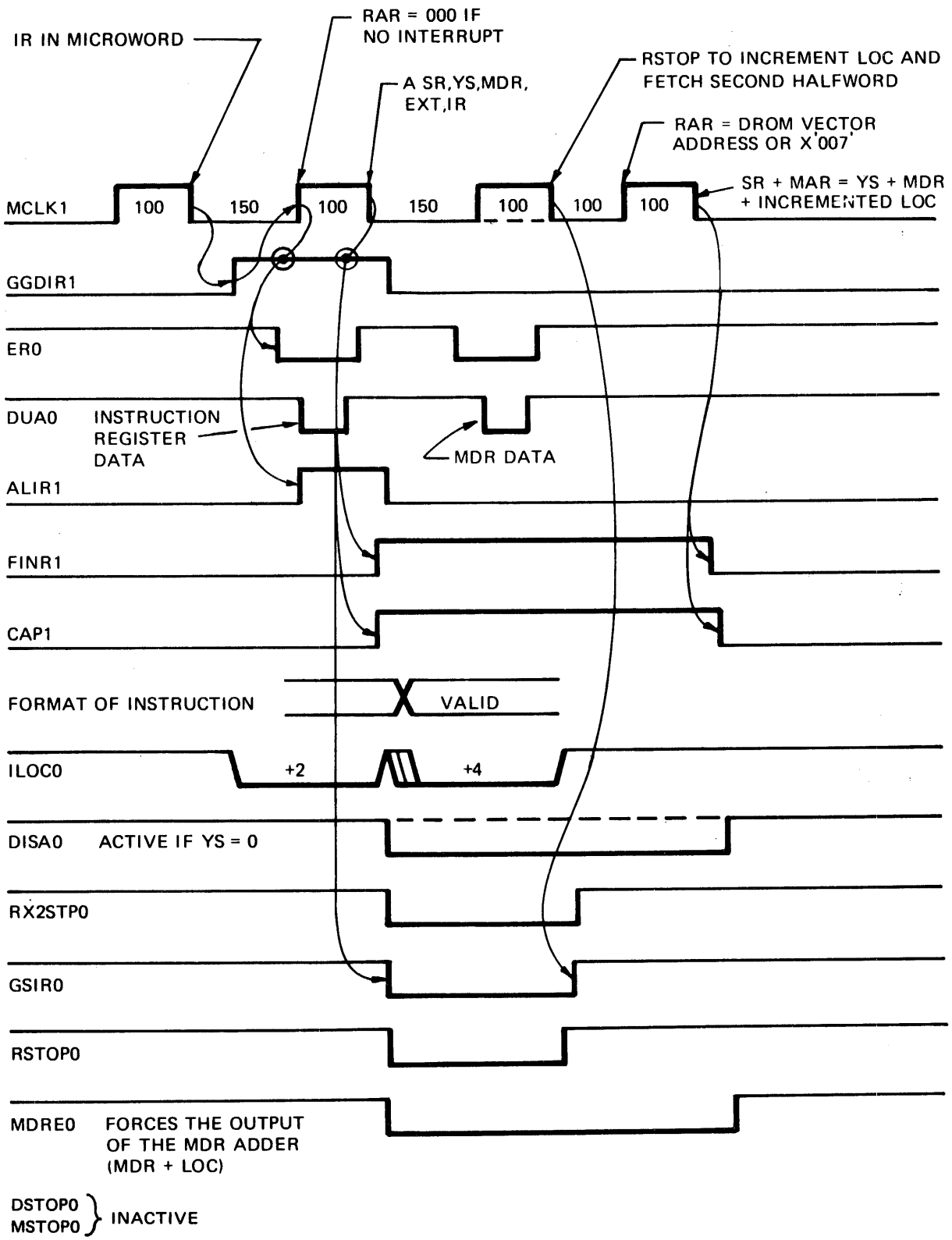


Figure 12-13 RX2 Format (Cache Hit on Halfword Boundary)

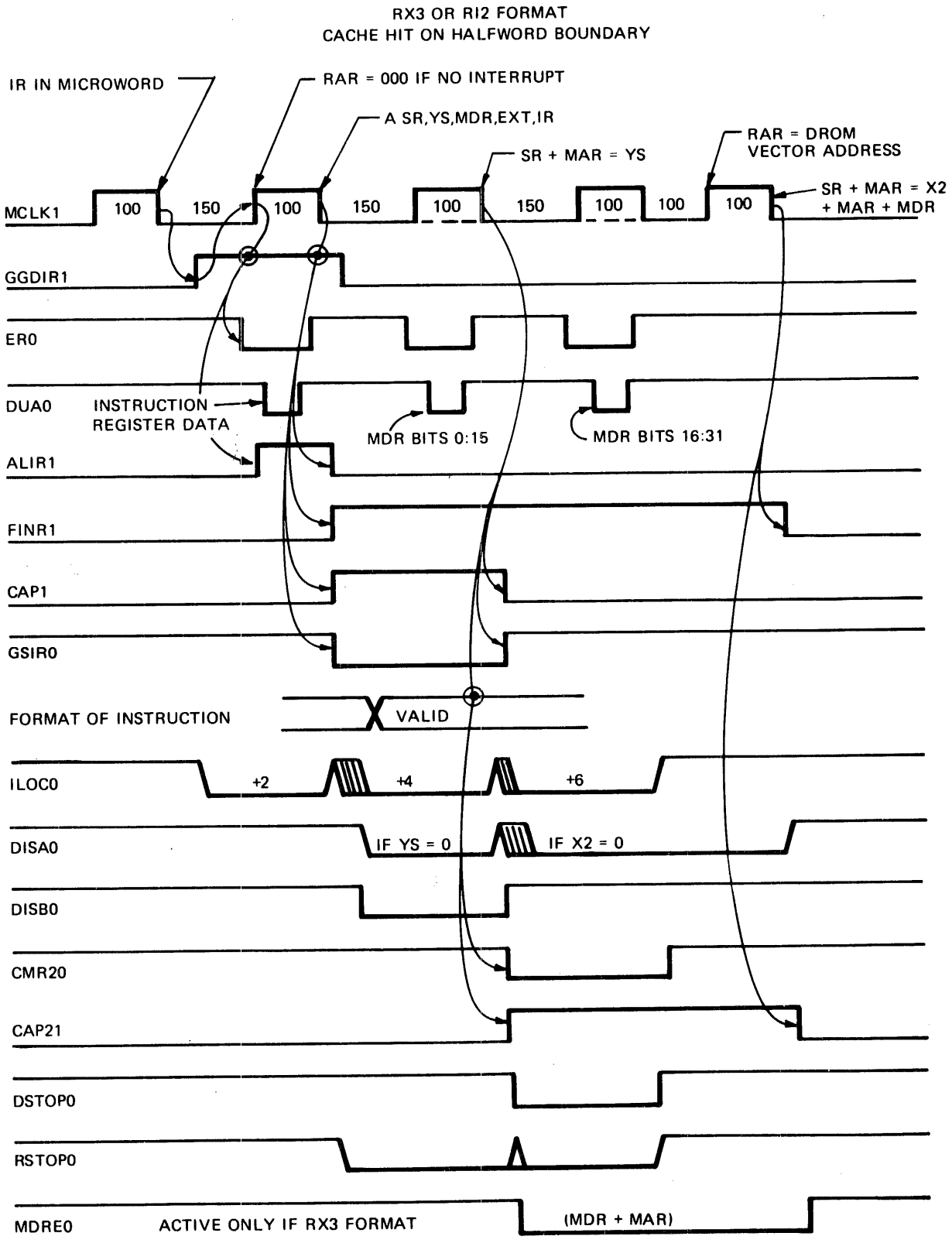


Figure 12-14 RX3 or RI2 Format (Cache Hit on Halfword Boundary)

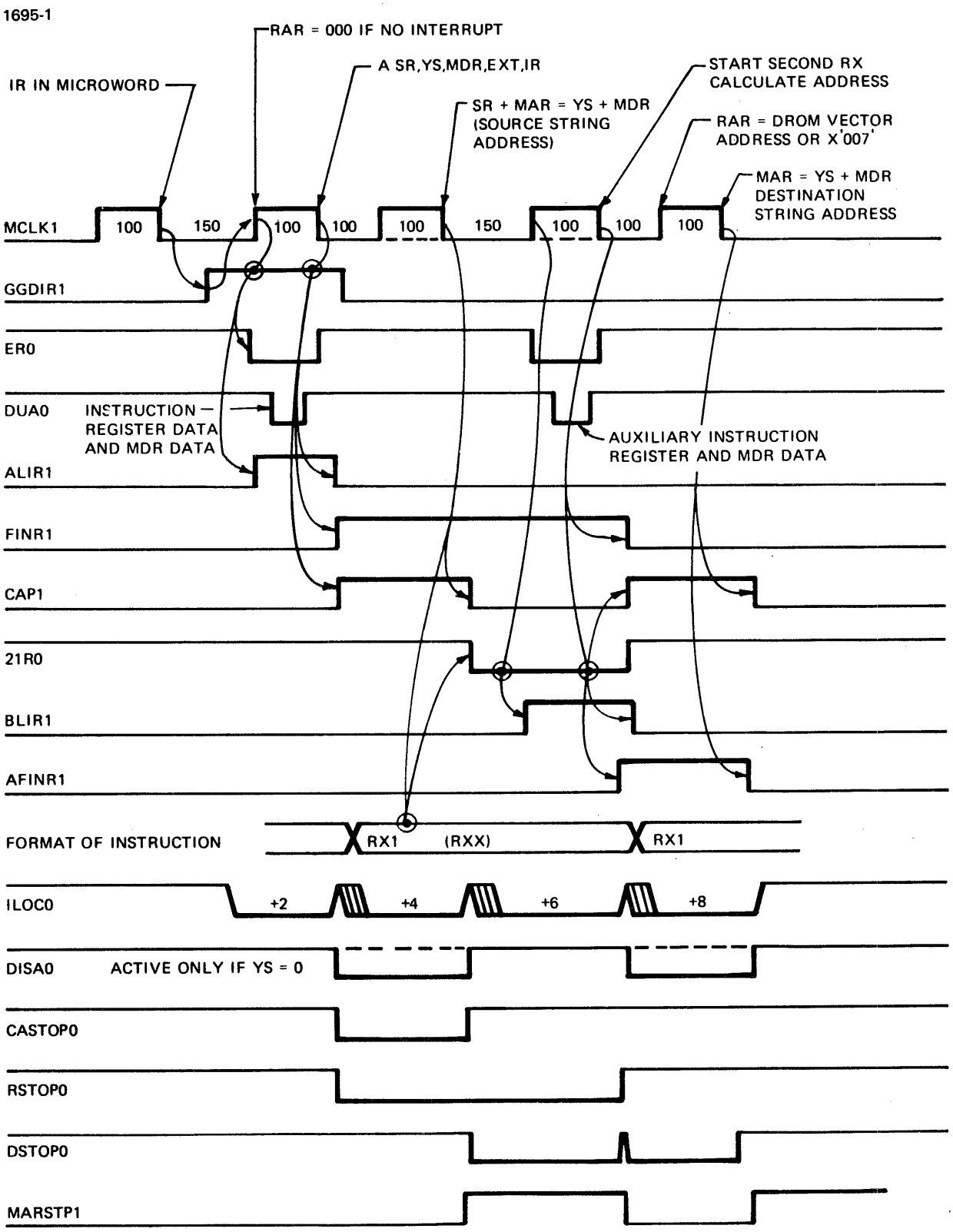


Figure 12-15 RX Squared (RXX) Format (RX1 Followed by RX1) A11 Memory Data in Cache

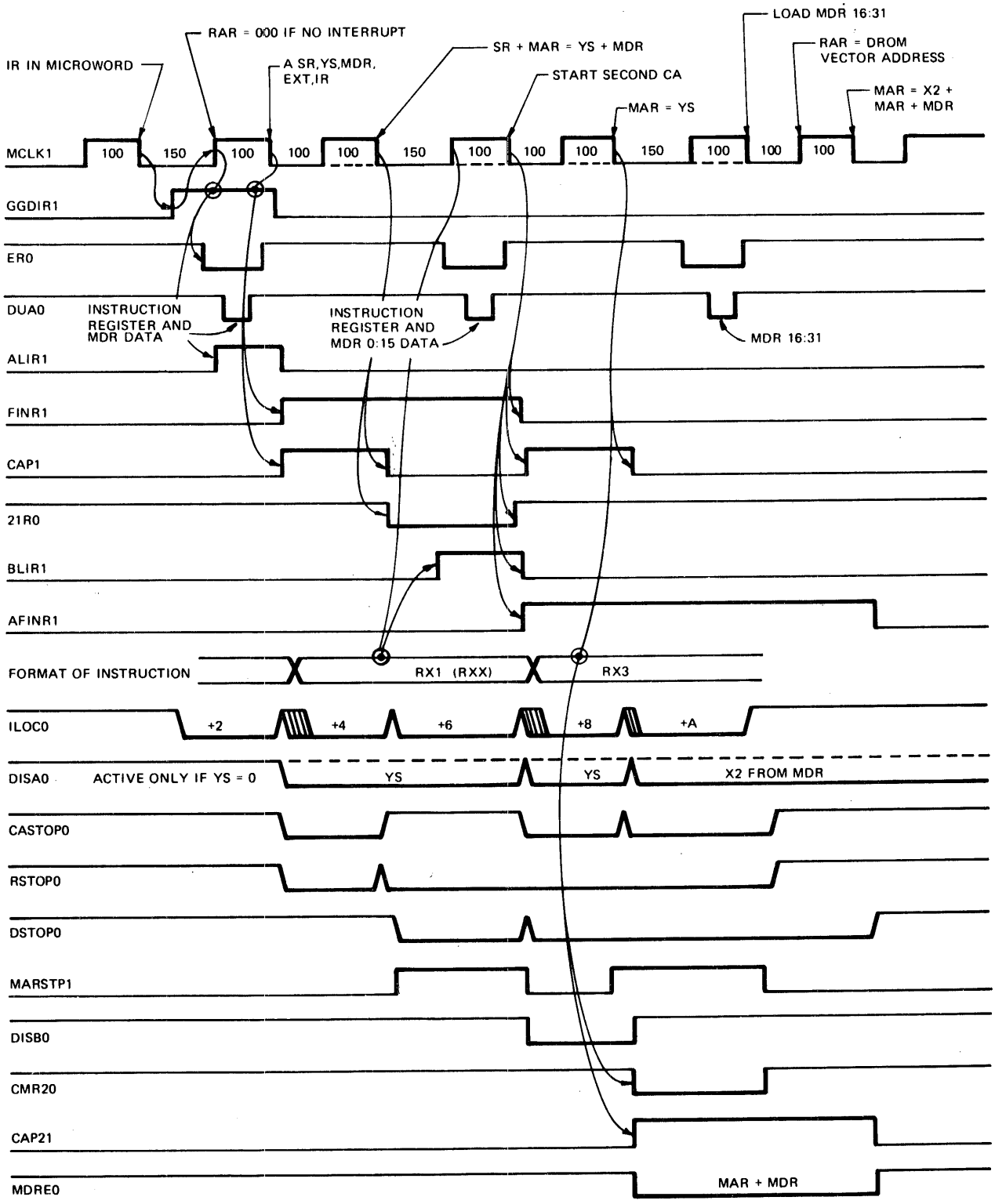


Figure 12-16 RX Squared (RXX) Format (RX1 Followed by RX3) All Memory Data in Cache

12.13 REPEAT COUNTER

The repeat counter (Sheet 11) is a 6-bit down counter which provides the ability to repeat a microinstruction up to 64 times. This is accomplished by loading the counter with the complement of the data on the S bus. Once the counter is loaded, RSTOP0 is forced active by CNTE00 until the counter is empty. The counter's count is decremented by one for each CLK1F if MSTOP and OPSTOP0 are not active.

12.14 B BUS MULTIPLEXORS

The B bus multiplexors on the CPU-D (Sheet 14) provide the B source information when I/O, LENGTH, YSI, or YDI is specified by the microinstruction. The contents of the AIR and either LENGTH, YSI, or YDI are provided once after an RX squared format calculate address has occurred. After the AIR has been read, it is cleared and then provides the inactive data bits 16:27 for LENGTH, YSI, and YDI. The most significant 16 bits of the 32-bit CPU-D B bus source are supplied by the CPU-B board as inactive data bits.

12.15 I/O SYSTEM

The I/O system provides the ability for the microprocessor to communicate with devices external to the processor. These devices and their controllers are connected to the I/O multiplexor bus. Refer to Sheet 13 of 35-770D08 during this description. The I/O multiplexor bus consists of a 16-bit bidirectional data bus and nine control lines.

Figure 12-17 shows an example of an I/O output operation. This sequence applies to the device addressing (ADRS), transmission of data to the device (DA), and transmission of command data (CMD). When a microinstruction specifies I/O as a destination, IOSTOP0 becomes active. IOSTOP0 causes RSTOP0 (Sheet 9) which suspends the microprogram. This is necessary to hold the data on the I/O bus until the operation is complete. The trailing edge of the first MCLK1 causes FDAT0 to become active. FDAT0 enables the I/O data bus transceivers and the data on the S bus is placed on the I/O multiplexor bus. The next MCLK1 causes FCOUT to become active. FCOUT causes the I/O output control line, selected by RD bits 29, 30, and 31, to become active. When the I/O control line becomes active, the device, if selected, responds with SYN0. The first leading edge of MCLK1 after the receipt of SYN0 causes the BSYN0 (13K2) flip-flop to set. On the trailing edge of the MCLK1 causing BSYN0 to set, FSYN0 sets. When FSYN0 becomes active, IOSTOP0 becomes inactive, allowing the microprogram to continue. The trailing edge of the MCLK1 following the setting of FSYN0 causes FCOUT0 and FDAT0 to reset, completing the operation.

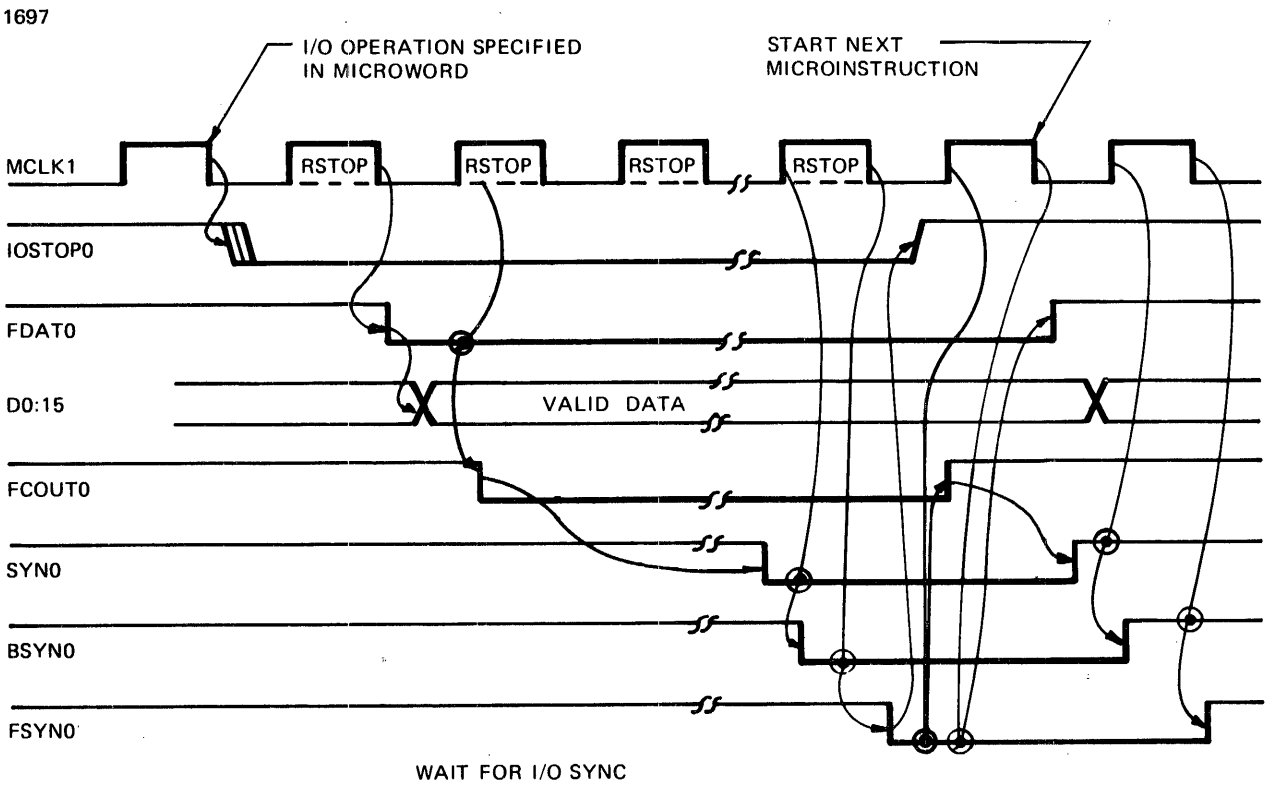


Figure 12-17 I/O Output Operation (ADRS, DA, CMD)

Figure 12-18 is an example of an I/O input operation. The sequence shown applies to request for device status (SR), request for data from the selected device (DR), and acknowledge interrupt (TACK). When a microinstruction specifies I/O as a source, IOSTOP0 becomes active suspending the microprogram until the data is received from the selected device. FCIN0 sets on the leading edge of MCLK1 after IOSTOP0 becomes active. FCIN0 enables the received data through the data transceivers. The selected device responds by causing SYN0 to be active. When SYN0 is active, the data from the device is valid on the I/O data bus. The leading edge of the MCLK1 following the receipt of SYN0 causes the BSYN0 flip-flop (13K2) to set. On the trailing edge of the MCLK1 after BSYN0 sets, FSYN0 sets. When FSYN0 becomes active, ISTOP0 becomes inactive, allowing the microprogram to continue. The clock following the setting of FSYN0 becomes the destination clock for the input I/O operation.

The acknowledge interrupt control has four outputs. These are used for the four possible I/O interrupt priority levels. The TACK lines are controlled by PSW27 and PSW26. When COMM is the device to be acknowledged, TACK00 is forced regardless of the state of PSW27 and PSW26.

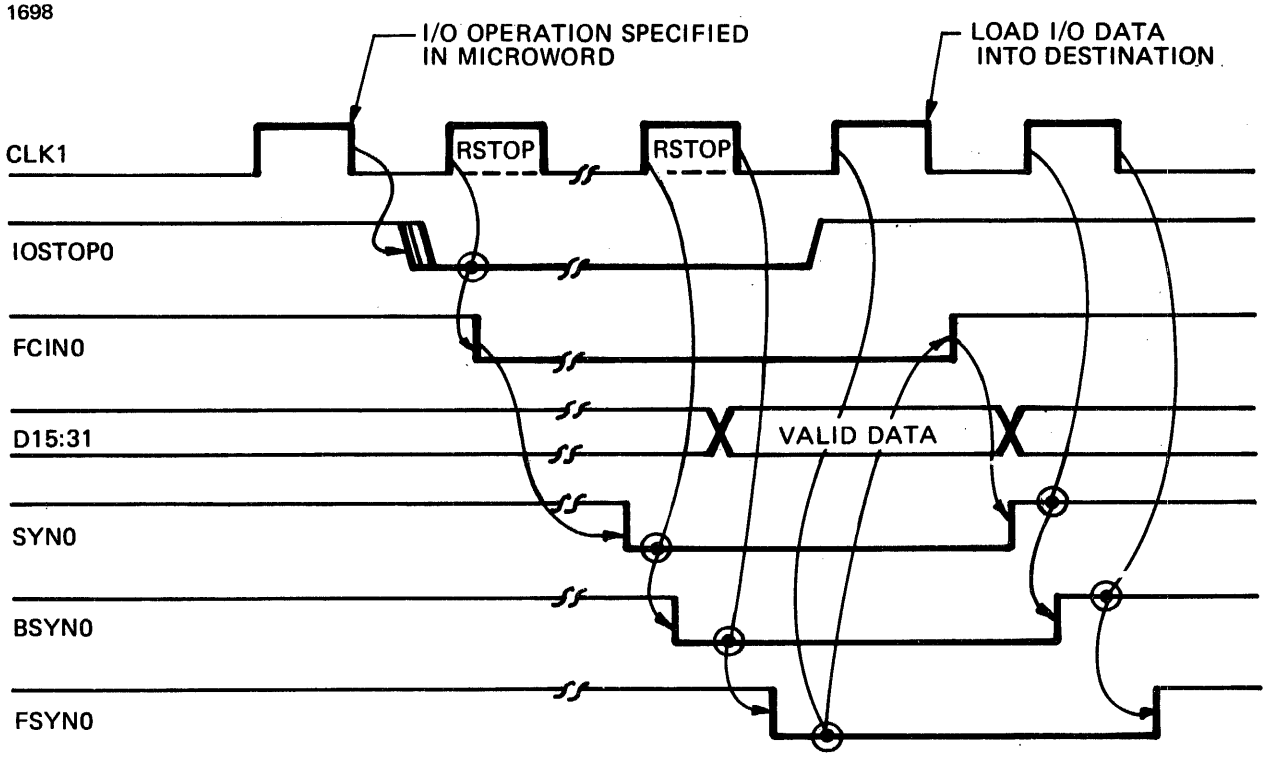


Figure 12-18 I/O Input Operation (SR, DR, TACK)

12.16 MNEMONICS

The following is a list of the mnemonics found on the CPU-D board. The 35-770D08 schematic location and a brief description of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
ACLR0	A clear signal on power up or down	2H1
ADRS0	Address control line for I/O bus - selects specific I/O controller	13D6
ADV0	A device signal which defeats the RSTOP caused by TRAP0 from CPU-A Test Aid	9D1
AFINR	Auxiliary instruction read flip-flop - used during second RX format of RXRX instruction	10D2
AIR00:11	Auxiliary instruction register - bits 00:11 contain second RX format op-code and YD fields	Sheet 12

MNEMONIC	MEANING	SCHEMATIC LOCATION
AIRQ0	Auxiliary instruction register queue - allows AIR tc load second RX information	10L4
ALIR0	A load instruction register flip-flop signal - defines the loading of IR as opposed to the AIR	10M5
ALIRCK0	Auxiliary IR clock	10R5
AMDR001 AMDR011	Auxiliary MDR bits use no instruction decoding for calculate address	3M7 3M8
AMDRCK0	Auxiliary MDR clock for loading the YS field	7J5
AMSTOP0	A memory stop - inhibits MCLK, RCLK, DCLK	9F4
ANS0	Answer - EDMA bus control sequel generated when either local or shared memory is read from	8K7
ASEL1	Select line for CPU-D board B bus source data	14H9
A1B10	A timing pulse generated from CPU clock generator logic	9L4
A1B11	A timing pulse generated from CPU clock generator logic	9L4
A1B11A	A timing pulse generated from CPU clock generator logic	9L4
B161:311	B bus signals	Sheet 14
BCLR0	B clear signal on power up or down	2H2
BCNT0	Board control signal - use to load data into the communication option board.	13C6
BLIR	B load instruction register flip-flop - defines the load time for the AIR as opposed to the IR	10M5
BMSTOP0	B memory stop signal inhibits MCLK, RCLK, DCLK	9F5
BRANCH0	Branch - decoded from microcode	9G1

MNEMONIC	MEANING	SCHEMATIC LOCATION
BRST0	Burst mode deccded from EDMA bus - defines EDMA mode of data transfer where more than one halfword is transferred	5N8
BRTD1	Burst read mode decoded from EDMA bus	5J6
BWRT1	Burst write mode decoded from EDMA bus	5J7
CACLK1	Calculate address clock - allows either the exit from calculate address or the second RX fetch in RXRX format	10M7
CAIR	Clear auxiliary instruction register flip-flop - clears the AIR so that 4-bit sources do not continue to display the AIR	12K4
CAMA0	Calculate memory address - used by the CPU-C to cause the MDR adder to use the MAR rather than LOC	10G4
CAP1	Calculate address part 1 - used by all formats of instructions. Calculate address is completed on all 32-bit or less length instructions.	10G2
CAP2	Calculate address part 2 - used by 48-bit format instructions	10G4
CAR261	A carry line fcr the EDMA MAR	15J6
CASTOP0	Calculate address stop - while active, the processor is suspended in calculate address.	10M6
CCLR0	C clear signal on power up or down	2H2
CLADA0	Clear address and data registers for EDMA to memory	7H1
CLFLR0	Clear flag register	13H7
CLK1	Nonstoppable processor clock	9N5
CLK1A:1F	Nonstoppable processor clock	Sheet 9
CLRDY0	Clear ready flip-flop	7E1
CLS0	Clear local memory request and start flip-flops	7D2

MNEMONIC	MEANING	SCHEMATIC LOCATION
CLSTA0	Clear MAT status register	7F8
CLST0	Clear FSOT	2M8
CMD0	Command control line for I/O bus - define when data on the I/O bus is for command information	13E6
CMR20	Calculate address memory read halfword - during calculate address of 48-bit formats, a third halfword must be fetched.	10G5
CNTE0	Count equal to zero - use to inhibit a specified instruction read until the microcode counter on the CPU-A has been completed	11R7
COMM0	Communication module - decode of E field. Data on the S bus is gated into the I/O bus and loaded into the communication hardware assist board.	12E4
COMSTP0	Communication stop - causes an RSTOP and inhibits the microprogram	13D2
CWR0	Change write memory to read memory	4G6
CYD0	Clear YD field of the instruction register - decoded from the E field of the microinstruction	12E3
D000:150	I/O data bus	Sheet 13
DA0	Data available control line for I/O bus - validates data on the I/O bus being sent to the devices	13E6
DANS1	Answer to EDMA bus	8H5
DAWT1	Data write into memory	6D3
DCLK0	Destination clock	9N8
DCLR0	D clear signal on power up or down	2H1
DDUA0	EDMA data unavailable	4N2
DISA0	Disable A source data - used during calculate address to inhibit A source data when YS is equal to zero	10G8

MNEMONIC	MEANING	SCHEMATIC LOCATION
DISB0	Disable B source data - used during calculate address to inhibit MDR data when it is incomplete or when an RR format is executing	10D5
DISEXT0	Disable sign extension - disable the MDR sign extension during calculate address	11H2
DL081:171 DL181:291 DL301	EDMA MAR output - after buffering, these drive the LMA bus.	Sheet 15 Sheet 16, 15B9
DMA000:030	EDMA bus lines	Sheet 15
DMA040:150	EDMA bus lines	Sheet 16
DMA160:170	EDMA bus lines	5A9
DMABZ1	DMA busy	2M7
DMAHW0	EDMA halfword mode	5H8
DMALM1	DMA to local memory	2K7
DMARS0	EDMA read and set - memory reads addressed location B EDMA and then restores the AW with the MSD bit set.	5H9
DMASEL	EDMA select flip-flop	2N6
DMASM1	DMA to shared memory	2K7
DMAWRT0	EDMA write	7R8
DMEM0	Decoded microinstruction memory operation	4F7
DMX080:150	EDMA bus lines	Sheet 15
DOIT0	Allows the MAR to be loaded during the calculate address of RXRX format instructions	10M7
DOSC0	EDMA oscillator for memory to EDMA control logic	5F1
DR0	Data request control line for I/O bus - validates data on the I/O bus to be loaded into the processor	13D6
DRFAULT0	Decoded reset fault	12E5

MNEMONIC	MEANING	SCHEMATIC LOCATION
DSTOP0	Destination stop - inhibits the system clock from loading a destination. DCLK is stopped.	9L1
DUA0	Data unavailable control line from local memory - while this signal is active, the data on the memory bus is invalid.	4B2
ED001:151	Tristate output of EDMA MDR and input to EDMA transceivers	Sheets 17, 18
EDAT1	Even data halfword memory operation	6D4
EEDCLK0	EDMA even data register clock signal	7N5
EFLDEN0	E field enable	14F9
EFWRT1	EDMA fullword data write	2N4
EMDENB0	Enable even half of EDMA data register	8G1
EMDR001:151 EMDR161	EDMA MDR outputs used for driving the MDS bus	Sheet 17, Sheet 18
ENAOSC0	Enable oscillator for memory to EDMA data transmission	5H3
ENCE1	Noncorrectable error from memory on an EDMA memory access	10D7
ENEX00	Enable external oscillator - for maintenance purposes	9J7
ENMAA0	Enable MAT access	4G6
ENXCVR0	Enable transceivers for a processor-to-EDMA transceiver	8H2
EOT0	End of transmission control line in EDMA bus protocol	8H8
ERD1	EDMA read	5G7
EVDAT	Even memory data operation for CPU flip-flop	6G4
EXOSC0	External oscillator connection - for maintenance only	9F9

MNEMONIC	MEANING	SCHEMATIC LOCATION
FADV1	Advance flip-flop output in clock single-step control	9E2
FAULTO	Lights the FAULT lamp on the system control panel	12G5
FB	The B flip-flop of CPU clock generator	9J5
FBIR	Instruction read flip-flop indicating an instruction fetch on a fullword memory address boundary	6G1
FBRTRD	Burst read flip-flop	5M6
FBRWRT	Burst write flip-flop	5M8
FCIN	Input control flip-flop for I/O operation	13A5
FCOMM	Communication module flip-flop for I/O operation	13C3
FCOUT	Output control flip-flop for I/O operation	13H5
FDA	Flip-flop used for generating memory to EDMA bus signals	Sheet 5
FDAA	Flip-flop used for generating memory to EDMA bus signals operation	Sheet 5
FDAAO	Auxiliary FA used in the memory to EDMA control	5L2
FDAT	Data control flip-flop for I/O operations - data on the S bus is transmitted into the I/O bus.	13K4
FDB	Flip-flop used for generating memory to EDMA bus signals	Sheet 5
FDC	Flip-flop used for generating memory to EDMA bus signals	Sheet 5
FDEOT	Detected end of transmission flip-flop used in burst read from local memory	2C9
FDRDY	Data ready flip-flop used for look-ahead in burst read from local memory	5L4
FDUA	Data (from local memory) unavailable flip-flop	4E2

MNEMONIC	MEANING	SCHEMATIC LOCATION
FDUSKP	Data unavailable skip flip-flop - causes an added 50 ns on the up time of CLK1	4E3
FEFW	EDMA fullword flip-flop	5G8
FEIR	Even address instruction read flip-flop - used when instruction read is started on a halfword boundary; suppressed on RR formats	6G2
FENCE	The flip-flop that stores state of ENCE1 on an EDMA access of memory	7N2
FEOT	End of transmission flip-flop	8K8
FER	Early read flip-flop	9J5
FERD	EDMA read flip-flop	5G6
FINR	Instruction read flip-flop	10G1
FLADR	Load EDMA address flip-flop	2J4
FLADRA	Load first halfword of EDMA data flip-flop	2M5
FLADRB	Load second halfword of EDMA data flip-flop	2N4
FLMRQ	Local memory request flip-flop	2G8
FMREQ	Memory request flip-flop	2D4
FNCE0	Noncorrectable error flip-flop indicates a detected multiple error during a processor memory read	10G6
FOIR	Odd address instruction read flip-flop - used when an instruction read occurs on a halfword boundary. Second halfword is fetched when FEIR is set.	6G2
FPA FPB FPC FPD FPE FPF FPG	EDMA protocol generating flip-flops	Sheet 6

MNEMONIC	MEANING	SCHEMATIC LOCATION
FPPF0	Primary power fail - this signal is generated on the CPU-A board and is used to generate an I/O device status bit during sense status.	13G6
FQEOT	EOT queued for burst read to memory	2G7
FRD	Memory read operation flip-flop	6G2
FSCLK1	Skew clock flip-flop	9F6
FSOT	Start of transmission flip-flop for EDMA to local memory	2F4
FSYN	SYNC flip-flop for I/O operations	13L5
FTIT1	When active, causes an MSTOP in order to provide the ability to single step through the microprogram	9G3
FW1	Fullword memory operation flip-flop	6H1
GBRANCH0	Gated branch	9G1
GDAT0	Gate data from S bus to I/O bus	13K7
GDIR0	Gated decoded instruction read - this signal is generated on the CPU-A. When active, it indicates the attempt to initiate an instruction read cycle.	10A1
GENMAA1	Gated enable MAT access	4J6
GEOT	Gated EOT signal	8M8
GGDIR1	GDIR0 is inhibited if the repeat microinstruction counter is not zero.	10D1
GMATSTOP0	Gated MAT stop	4J4
GRD0	Gated memory read	6L3
GSIR0	Gated second instruction read - queueing of the requirement for a second memory read when the instruction fetch is on a halfword boundary	6N2
HALT0	Halt honoring processor memory request	2K5
HOST1	Hold EDMA protocol oscillator stopped	8N2

MNEMONIC	MEANING	SCHEMATIC LOCATION
I40	Increment MAR by 4 - an E field decode	12E3
ILDMA0	Increment or load EDMA MAR	7N4
ILOC0	Increment LOC - this signal occurs during the calculate address sequence.	10C7
IMAR	Increment MAR by 4.	12J8
INHFS0	Inhibit false SYNC test point - disables the generation of the I/O false SYNC escape	13N1
IO161:311	IO data bits received from multiplexor bus	Sheet 13
IOOP1	I/O operation has been specified by the microinstruction.	13K5
IOSTOP0	IO stop to inhibit RCLK - prevents the microinstruction from changing during I/O operations	13L6
IRD001:151	Instruction register input data lines that represent the OP CODE, YD, and YS fields	Sheets 3, 12
IRXX0	Used in the calculate address logic to inhibit the end of the calculate address sequence on the first format completion of an RXRX format instruction	10N2
LDCTR0	Load repeat counter	12N8
LDIO0	Load I/O	12N9
LDMAL0	Load EDMA MAR	7M3
LEN271:301	Length register bits	11N2
LER0	Local memory early read	4N8
LFLR0	Load flag register	12L7
LHWRT0	Enables multiplexor to output MDR16:31 to MDS00:15 for a write even halfword	7N9
LINC1	Length increment for length register	10M9

MNEMONIC	MEANING	SCHEMATIC LOCATION
LIR1	Load instruction register	10R5
LIRCK1	IR clock to load op-code	10A3
LMA080:310	Memory address bus lines	Sheet 15
LMBSY0	Local memory busy	4J2
LMDR1	Load memory data register	12N9
LMREQ0	Local memory request	2A4
LOAD0	EDMA bus load signal for address or data	8K7
LPSTD0	Load process segment table descriptor	12E1
LSSTD0	Load shared segment table descriptor	12E1
LWRT0	Load write - enables the multiplexors to drive MDS000:310 to local memory	7N8
LYDI0	Load YD immediate - RD decoding of the destination field that implies that the YD portion of the IR is loaded	12M9
LYSI0	Load YD immediate - RD decoding of the E field that causes the YS field of the IR to be loaded from the least significant 4 bits of the S bus. The register specified in the destination field of the microinstruction is also loaded.	12E5
MARSTP1	Memory address register stop	9L1
MATSTCP0	MAT stop	4G4
MCLK0	Memory clock	9M8
MDHCLK0	MDR clock for MDR00:15	7J4
MDHSA1	Memory data register high (even) select line for inputting to the MDR	7E3
MDLCK0	MDR clock for MDR16:31	7J6
MDLSA1	Memory data register low (odd) select line for inputting to the MDR	7E3
MDRE0	Memory data register adder enable - generated for the CPU-C board during calculate address	11J7
MDS000:150 MDS160:310	Memory data bus	Sheet 17 Sheet 18

MNEMONIC	MEANING	SCHEMATIC LOCATION
MDSB0	Memory data register select line for inputting to the MDR	7E2
MFAULT0	Memory fault indicates that a MAT, NCE, or alignment fault interrupt is pending. DSTOP is forced active until the interrupt is serviced.	9G1
MOPCLK1	MSTOP or OPSTOP clock	11K8
MREAD1	Memory read	6D2
MSBC0	MAT to shared bank controller	4G7
MSTOP0	Memory stop	9H4
NCE0	Noncorrectable error from memory	10A6
NOCNT0	No repeat counter operation	11R4
OEDCLK0	Odd EDMA MDR clock	7N7
OMDENB0	Odd EDMA MDR enable to EDMA bus	8F2
OPTSTP0	Option stop - this signal is generated by either the WCS or HPFPP options to inhibit the microprogram during their operations.	9H3
OSC0	Oscillator - buffered output of the 20 MHz crystal or the external oscillator divider flop	9L8
PA301	Program address bit 30	4B6
PDUA1	Processor data unavailable	4N1
PMEM1	Processor attempt to initiate a memory cycle	4D8
PROSC1	Protocol oscillator	6M9
PSBC0	Processor to shared bank controller	4G7
PSEL1A	Processor selected for memory operation	2N5
PSW181	Program status bits 18, 26, 27	10A7

MNEMONIC	MEANING	SCHEMATIC LOCATION
PSW261	Program status bits 18, 26, 27	13B5
PSW271	Program status bits 18, 26, 27	13B5
QUE0	Queue control line of EDMA protocol	6N5
RCLK0	ROM clock - this clock is inhibited by RSTOP and, when stopped, the microprogram stops.	9N8
RD001	ROM data register data bits forming the microinstruction	6A2
RD011	ROM data register data bits forming the microinstruction	4B5
RD021	ROM data register data bits forming the microinstruction	4B6
RD031	ROM data register data bits forming the microinstruction	12A7
RD041	ROM data register data bits forming the microinstruction	9G1
RD051	ROM data register data bits forming the microinstruction	9G1
RD121	ROM data register data bits forming the microinstruction	12J9
RD131	ROM data register data bits forming the microinstruction	12J7
RD141	ROM data register data bits forming the microinstruction	12J7
RD150	ROM data register data bits forming the microinstruction	12J7
RD161	ROM data register data bits forming the microinstruction	14D8
RD240	ROM data register data bits forming the microinstruction	14D8
RD251	ROM data register data bits forming the microinstruction	12E7, 12E8

MNEMONIC	MEANING	SCHEMATIC LOCATION
RD261	ROM data register data bits forming the microinstruction	14D7
RD271	ROM data register data bits forming the microinstruction	14D7
RD281:311	ROM data register data bits forming the microinstruction	12A6, 12A7
RDAX081:151 RDAT001:151 RDAT161:171	Received data lines from EDMA transceivers	Sheet 15 Sheets 15, 16 5A9
RDFW0	Read fullword	6M2
RESC0	Reset C flip-flop of EDMA protocol logic	8F6
RFAULT0	Reset memory fault interrupts	12H6
RI20	Format ROM output that indicates that the current op-code in the IR is a 48-bit immediate instruction	11F3
RI2RX31	Format decoded signal that indicates that a 48-bit format instruction is being processed (RI2 or RX3)	11H5
RMSR1	Read MAT status register	7C6
RR1	Register-to-register user instruction	11H1
RSTOP0	ROM stop	9L3
RX21	RX2 user instruction format	11H5
RX2STP0	RX2 user instruction stop - this stop allows the LCC to be incremented for the calculate address.	10N1
RX31	RX3 user instruction format	11H4
RXXSTOP0	RX squared format instruction stop	11H3
S161:311	S bus bits 16:31	Sheet 14
SAFINR1	Set A instruction read flip-flop	10A2
SB291	Set bit 29 - this signal, when active, causes bit 29 of the sensed I/O status to be set.	13F7

MNEMONIC	MEANING	SCHEMATIC LOCATION
SCAP11	Set calculate address part 1 - causes the CAP1 flip-flop to be set	10D3
SCLK1	Skew clock - delayed system clock. This clock starts 50 ns after CLK1. While CLK1 is stretched during its up time, SCLK1 is stretched during its down time.	9N6
SCLR0	System clear	2D2
SDFF1	Set data flip-flop	13K2
SER0	Shared memory early read	4N9
SMBSY1	Shared memory busy	2G8
SOT0	Start of transmission control line of EDMA protocol	6R7
SR0	Status control line for I/O	13C6
SRXX1	Set RX squared format instruction - causes the calculate address logic to be queued for RX squared format	11H1
STB1	Strobe	14J9
SV0	Set overflow caused by the I/O system when a false SYNC timeout occurs	13N6
SYN0	SYNC control line of I/O - response from selected device to any I/O control line activation	13M1
TACK000	Transmit acknowledge level 0	13A9
TACK010	Transmit acknowledge level 1	13A9
TACK020	Transmit acknowledge level 2	13B9
TACK030	Transmit acknowledge level 3	13B9
TPC0	Transmit priority chain line of EDMA protocol	6N6
TRAP0	Signal generated by the CPU-A on board test aid - this signal causes MSTOP which stops the microprogram.	9A3

MNEMONIC	MEANING	SCHEMATIC LOCATION
ULIOO	Unload I/O decoded from the destination field of RD	14G6
ULYSJO	Unload YSI	14H8
UMDR1	Unload processor MDR decoded from the destination field of the micro-instruction	14H7
WRT	Write in memcry line	4M3
X20	This signal is generated during the calculate address of an RX3 format and defines the seccnd level index MDR data rather than the YS field of the IR.	10H3
XREQO	Request line of EDMA protocol	6B6
YDO81	User destination register select bits 8, 9, 10, and 11	3M2
YD091	User destination register select bits 8, 9, 10, and 11	3M2
YD101	User destination register select bits 8, 9, 10, and 11	3M2
YD111	User destination register select bits 8, 9, 10, and 11	3M2
YDCLKO	Clock to increment, decrement, or load the YD field of the instruction register	3D4
YDM10	Decrement the YD field of the IR by one - this is decoded from the E field of the microinstruction.	12E3
YDP10	Increment the YD field of the IR by one - this is decoded from the E field of the microinstruction.	11E8
YSO1	User source select bits 0, 1, 2 and 3	3M3
YS11	User source select bits 0, 1, 2 and 3	3M4
YS21	User source select bits 0, 1, 2 and 3	3M4
YS31	User source select bits 0, 1, 2 and 3	3M4

CHAPTER 13
4 MB LOCAL BANK CONTROLLER (LBC) (35-771)

13.1 INTRODUCTION

13.1.1 General

The 3230 memory system using the 35-771 local bank controller (LBC) may consist of any combination of 35-764 F02 (1/2 Mb), F03 (1 Mb), or F04 (2 Mb) storage modules with a local memory capacity of 4 Mb. The following board is available in the 3230 system:

35-771F01 with cache

13.1.2 Power Requirements

Table 13-1 provides the power requirements for the LBC board.

TABLE 13-1 POWER REQUIREMENTS

VOLTAGE SYMBOL	MODULE TYPE	NOMINAL VOLTAGE	MAXIMUM CURRENT DRAIN (AMPS)		
			OPERATING (SELECTED)	OPERATING (UNSELECTED)	BATTERY MODE
P5	35-771F01	+5.0 V	16.7A	16A	16A*
P5U	35-771F01	+5.0 V	1.8A	1.8A	1.8A

*P5 supply may be depowered in the battery mode.

13.1.3 Strapping and Test Point Information

The following test points are located on the front edge of the 35-771 LBC Board:

1. ECC Disable (TP1 and TP2, Sheet 5)

   Strapping TP1 to TP2 disables the Error Check and Correction (ECC) circuit, thereby preventing correction or detection of data errors. The error logger cannot be updated with the ECC disabled.

   For normal ECC and error logger operation, TP1 and TP2 should be left unstrapped.

2. Cache Miss (TP3 and TP4, Sheet 12) (F01 only)

   Leaving the strap from TP3 to TP4 open forces a cache miss condition causing all processor reads to be made from the STM in the quadword mode. This mode of operation is useful in diagnosing cache-related problems.

   For normal cache operation, TP3 and TP4 should be left strapped.

3. P5U Monitor (TP6, Sheet 13)

   The P5U supply voltage (+5.0 V + 1%) may be monitored at TP6 using TP1, TP3, or TP7 for the ground reference.

4. MB1 Monitor (TP5, Sheet 13)

   The MB1 flip-flop may be monitored at this point using TP1, TP3, TP7, TP10, or TP12 for the ground reference.

5. Cache Bypass (TP7 and TP8, Sheet 16)

   Strapping TP7 to TP8 enables operation of the cache on the F01 board. The F01 board may be used in the cache bypass mode (TP7 and TP8 unstrapped) for test purposes or in cases where the cache is malfunctioning.

6. Memory Strap (TP9 and TP10, Sheet 3)

   TP9 and TP10 should always be strapped for the 3230 system. TP9 and TP10 should be strapped for $\leq$4 Mb. Strap should be deleted for >4 Mb up to 16 Mb.

7. UCE Lamp Reset (TP11 and TP12, Sheet 7)

   The UCE lamp may be reset by momentarily shorting TP11 and TP12. This feature must be used only by trained personnel.

13.1.4 LBC LED Indicator Information

The following LED indicators are located on the front edge of the 35-771 LBC board:

1. P5U Indicator

   The P5U indicator lights whenever the P5U supply is active. The P5U supply remains active at all times unless the REMOTE POWER switch (X5) or the MAINTENANCE RESET switch is placed to the OFF position. Before removing the LBC board or STMs, verify that the P5U LED is extinguished and that the KEY switch on the System Control Panel (SCP) is in the OFF position.

2. Cache Parity Indicator

   The cache parity indicator lights whenever the cache buffer has output data with bad parity. The indicator remains lit until the SCP INITIALIZE switch is depressed or the KEY switch has been placed in the OFF position.

3. Uncorrectable Error (UCE) and Module Identification Indicators

   The Uncorrectable Error (UCE) indicator lights whenever a Storage Module (STM) outputs a data word containing a detectable multiple bit error. When the UCE indicator is lit, the module ID indicators contain the 256 kb block (module) address where the last Read error occurred.

   The UCE indicator remains lit until the SCP INITIALIZE switch is depressed, until the KEY switch is placed in the OFF position, until an REL instruction is executed, until a Read is executed to nonpresent memory, or until TP11 and TP12 are shorted. When the UCE indicator is off and the module ID indicators are on, they indicate that a memory access was made to the module specified by the lamps, but that the system is not equipped with that module.

13.2 FUNCTIONAL ANALYSIS

13.2.1 Refresh

Refer to Figures 13-1 and 13-2 for refresh timing information. The Storage Modules (STMs) utilize 16k or 64k x 1 MOS dynamic Random Access Memories (RAMs) which require periodic refresh cycles at each of the 128 row address locations every two milliseconds. This is accomplished by executing a single refresh cycle every 16 microseconds (cycle steal mode) or a 128 refresh cycle burst every two milliseconds (burst mode). During any refresh cycle, every memory chip within the system is selected and refreshed at the same row location.

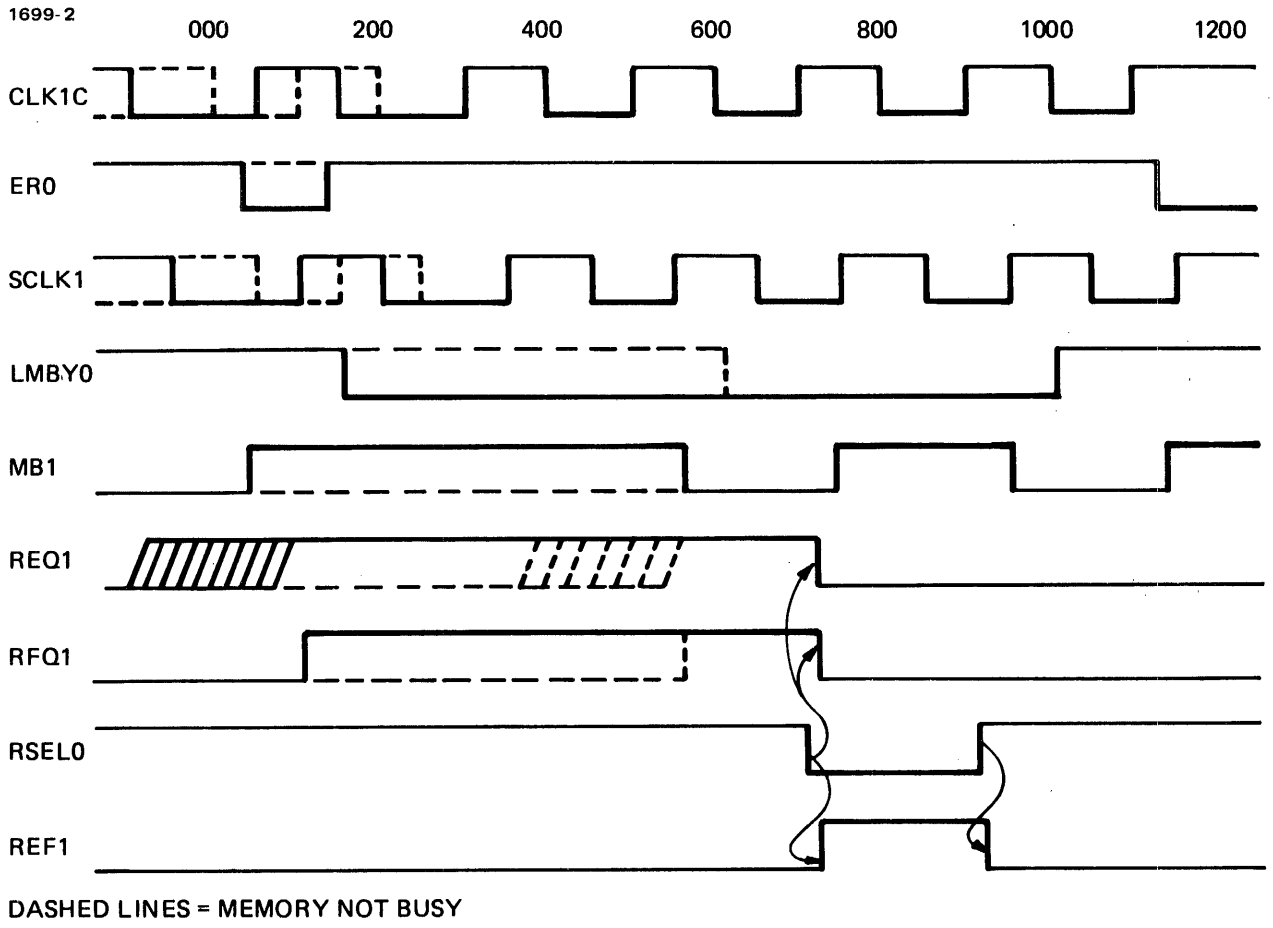


Figure 13-1 Refresh Cycle Steal Timing

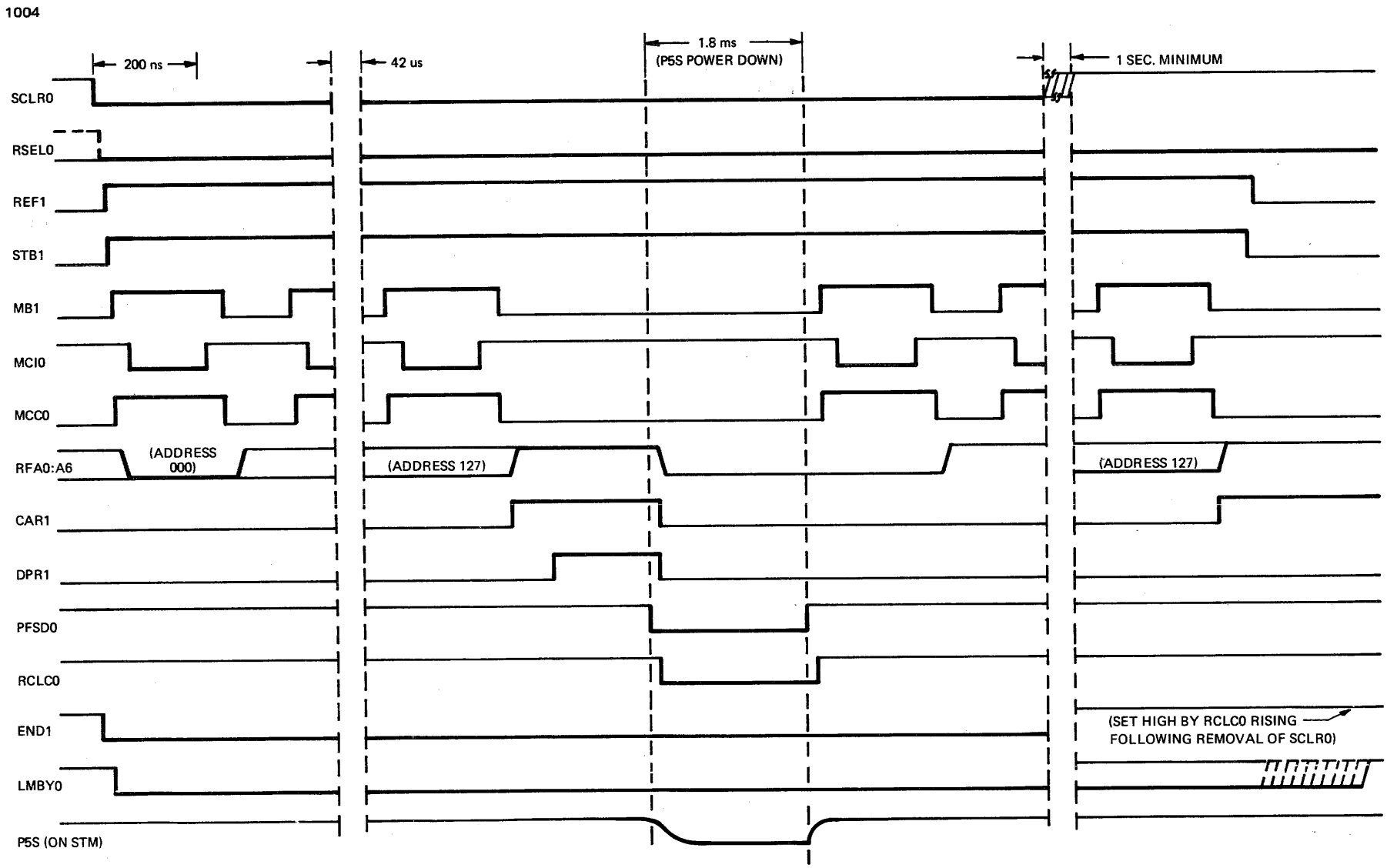


Figure 13-2 Burst Refresh Timing (128 Cycles)

13.2.1.1 Burst Mode

The burst mode is entered whenever the consolette INITIALIZE switch is depressed or the KEY switch is placed to the OFF position, causing the System Clear (SCLR0) line to go active. SCLR0 (13B3) causes REF1 (13K3) to go active, enabling the refresh address driver 11C (3N2) and setting the MB1 flip-flop. MB0 sets the TA001 flip-flop (16B6), starting the TA timer, which causes MCI0 (16S5) to go active and initiate the refresh cycle to the STM(s). With MREF0 (9G5) active, all STMs in the system are enabled to perform the refresh cycle (refer to the chapter on the STM for a detailed description).

The LBC refresh scheme is designed to accommodate 64k x 1 memory chips. Some 64k chips require 128 rows (2 ms refresh), and some 64k chips require 256 rows (4 ms refresh). To insure data integrity, the LBC does burst refresh as follows: When SCLR0 goes active, the LBC does a 256 cycle burst refresh, insuring that all rows are refreshed. Then every 2 ms, a 128 cycle burst refresh is performed. This accommodates both types of 64k RAMs and saves power over doing a 256 cycle burst refresh every 2 ms. When SCLR0 goes inactive, the LBC does a 256 cycle burst refresh before returning to cycle steal mode.

When TA201 (13G8) goes high, the refresh counter (13K5 and 13M5) is advanced and the MB1 flip-flop (13K7) is cleared. This causes MCC0 (9G2) to go active, ending the first refresh cycle. When TA181 (13G8) goes low, the MB1 flip-flop (13K7) is directly set, starting the next refresh cycle. This mode of operation continues for 128 cycles allowing the DPR1 flip-flop (13J2) to be clocked set and PFSD (13N2) to be activated. PFSD0 (9R4) going active causes the STM(s) P5S switch to turn off, placing it into a low power standby mode and activating RCLC0 (9N5). RCLC1 (13E4) causes the refresh counter (13J5 and 13M5) and the DPR1 flip-flop (13J2) to be cleared, allowing the 1.8 ms one-shot (13M2) to time out and deactivate PFSD1. PFSD0 (9R4) going inactive causes the STM(s) P5S switch to turn on, deactivating RCLC0 (9N5), thereby setting the MB1 flip-flop (13K7) and initiating another 128 cycle burst.

This mode of operation continues until SCLR0 and SCLR0A (13A3) are brought high by returning the System Control Panel KEY switch to the ON position and timing out the initialize function. This causes the END1 flip-flop (13F5) to be clocked set after completing a 256-cycle burst, allowing the STB1 flip-flop (13H1) to be clocked reset at the end of that burst. STB1 going low causes REF1 (13K3) and REF0 (13N3) to go inactive, allowing LMBY0 (15N8) to be returned high, indicating to the processor that the memory is ready to accept a command. Figure 13-2 shows the timing for a 128 cycle burst refresh cycle. Memory refreshing is continued by performing a single refresh cycle steal every 16 microseconds.

13.2.1.2 Cycle Steal Refresh

A refresh cycle steal is initiated whenever the free-running 16 microsecond oscillator (13B2) clocks the REQ1 flip-flop (13D2) set, thereby allowing the RFQ1 flip-flop (15K7) to queue up this request. Flip-flop 07A (13E2) and the RSEL0 flip-flop (13F2) are used to further synchronize the start and end of the refresh cycle to prevent overlapping of memory operations. Operation in the refresh cycle steal mode is identical to the burst refresh cycle, with the exception that only one cycle is executed and the DPR1 flip-flop (13J2) is never activated.

13.2.2 LBC Operating Modes

The LBC operates in a number of different modes (refer to Table 13-2) as determined by the states of ROM data lines RD011:031 (3E7), WRT0 (3A6), DMAHW0 (3A6), PSEL1 (3A6) and LMA030 at the time ER0 (13G7) goes active. These signals are loaded into transparent latches whose outputs drive the mode selector logic consisting of one of eight decoders 20F (14C3) and 20J (14C5) and miscellaneous gate functions (left half of Sheet 14). For any given operation, certain mode decoder outputs go active (refer to Table 13-2), setting up the control logic for the specific data manipulation required.

There are seven basic functional modes used by the LBC to service all operations. They are:

1. Store Fullword (Figure 13-3)

2. Store Partial Word (Figure 13-4) including:

   - store byte
   - store halfword
   - read and set
   - test error logger

3. CPU Read Fullword (with cache hit) (Figure 13-5)

4. CPU Read Fullword (with cache miss) (Figure 13-6)

5. Read Fullword with cache not equipped (bypassed) or DMA read (Figure 13-7)

6. Read Error Logger Status (LMA190 low) (Figure 13-8)

7. Read Error Logger (LMA190 high)

NOTE

All read halfword operations are decoded as read fullword operations by the LBC. Data steering for halfword operations is performed on the CPU-C board.

TABLE 13-2 LBC OPERATING MODES

1873-2

MATRSD0	MATRSR0	DRST0	PSELIA	WRT0	RD 011	RD 021	RD 031	PROCESSOR OPERATIONS	MODE DECODER OUTPUTS ACTIVE (See Sheet 14 35-728D08)
1	1	1	1	0	0	0	0	No Memory Operation	
1	1	1	1	0	0	0	1	Store Byte	SBY1, SPW1, SPW0
1	1	1	1	0	0	1	0	Store Halfword (Privileged)*	SHW1, SPW1, SPW0
1	1	1	1	0	0	1	1	Store Halfword (Data)*	SHW1, SPW1, SPW0
1	1	1	1	0	1	0	0	Test Error Logger (Store Byte)	TEL0, TEL1, SBY1
1	1	1	1	0	1	0	1	No Memory Operation	
1	1	1	1	0	1	1	0	Store Fullword (Privileged)*	SFW1, SFW0
1	1	1	1	0	1	1	1	Store Fullword (Data)*	SFW1, SFW0
1	1	1	1	1	0	0	0	No Memory Operation	
1	1	1	1	1	0	0	1	Read and Set Halfword	RST0, RST1, SFW1, ROAST1
1	1	1	1	1	0	1	0	Read Halfword (Privileged)* (Fullword Operation)	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	0	1	1	Read Halfword (Data)* (Fullword Operation)	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	0	0	Read Error Logger	EL0, REL1 (active with LMA190 high), ELST1 (active with LMA190 low)
1	1	1	1	1	1	0	1	Read Fullword (Instruction Read)*	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	1	0	Read Fullword (Privileged)*	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	1	1	Read Fullword (Data)*	PRFW0, PRFW1, RFW1, ROAST1
			PSELIA	WRT0	DMAHW0			DMA Operations	
1	1	1	0	0	0			Store Halfword	SHW1, SPW1, SPW0
1	1	1	0	0	1			Store Fullword	SFW1, SFW0
1	1	1	0	1	0			Read Halfword (Fullword Operation)	DRFW0, DRFW1, RFW1, ROAST1
1	1	1	0	1	1			Read Fullword (Fullword Operation)	DRFW0, DRFW1, RFW1, ROAST1
1	1	0						DMA Read and Set	DRST0
1	0	1						MAT Read and Set Reference Bit	MATRSR0
0	1	1						MAT Read and Set Dirty Bit	MATRSD0

*LBC does not differentiate between privileged and data instruction.

1701-2

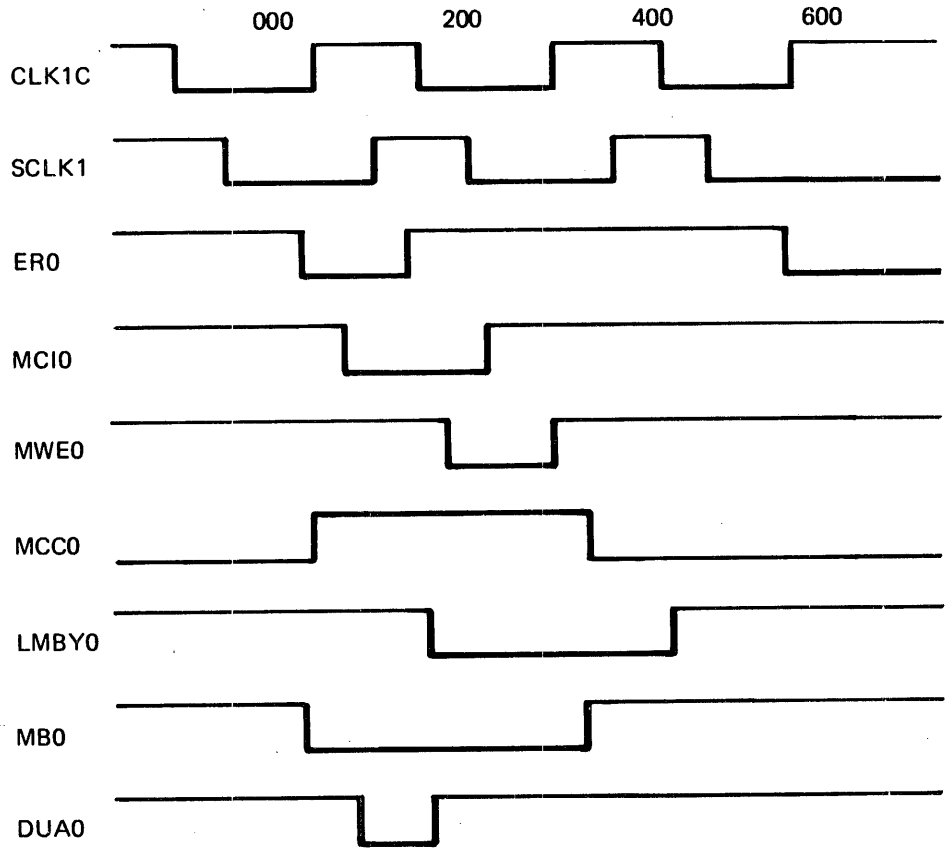


Figure 13-3 Store Fullword

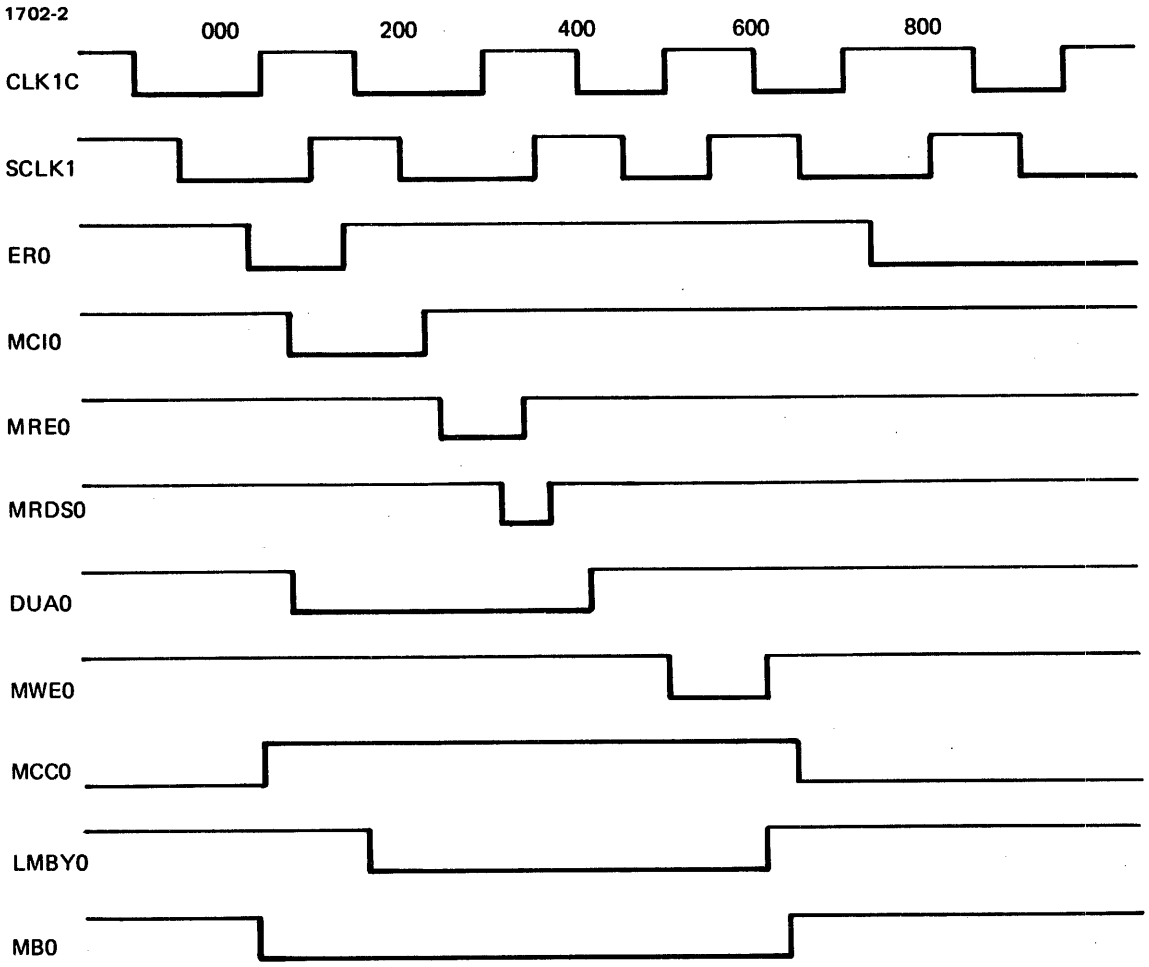


Figure 13-4 Store Partial Word

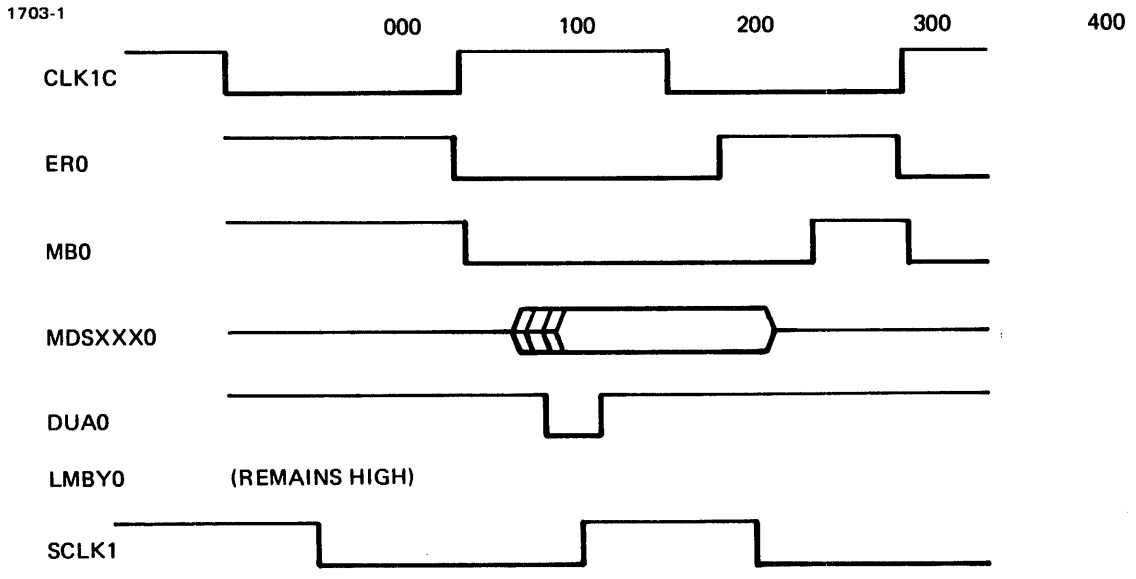


Figure 13-5 CPU Read (With Cache Hit)

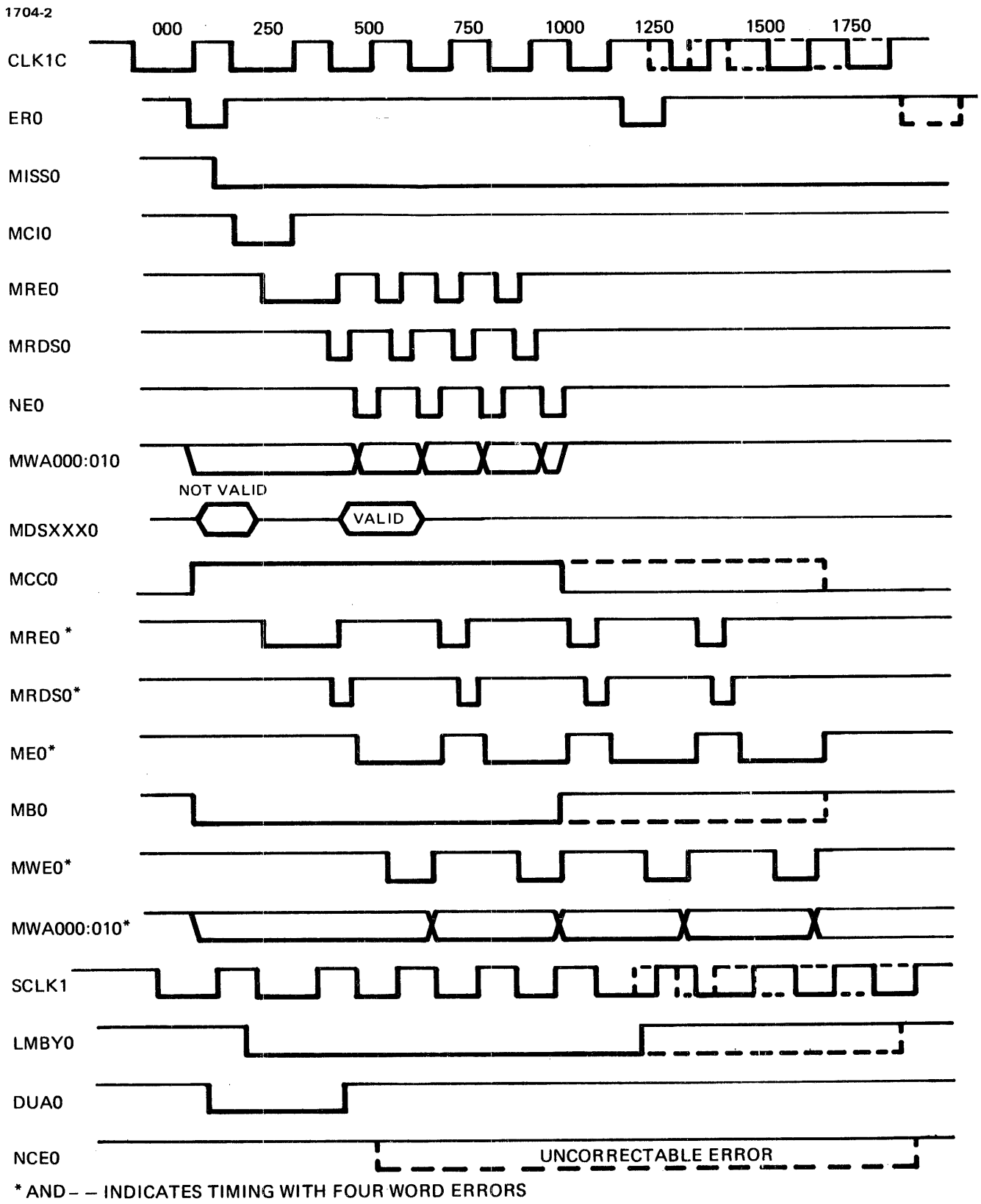


Figure 13-6 CPU Read (With Cache Miss)

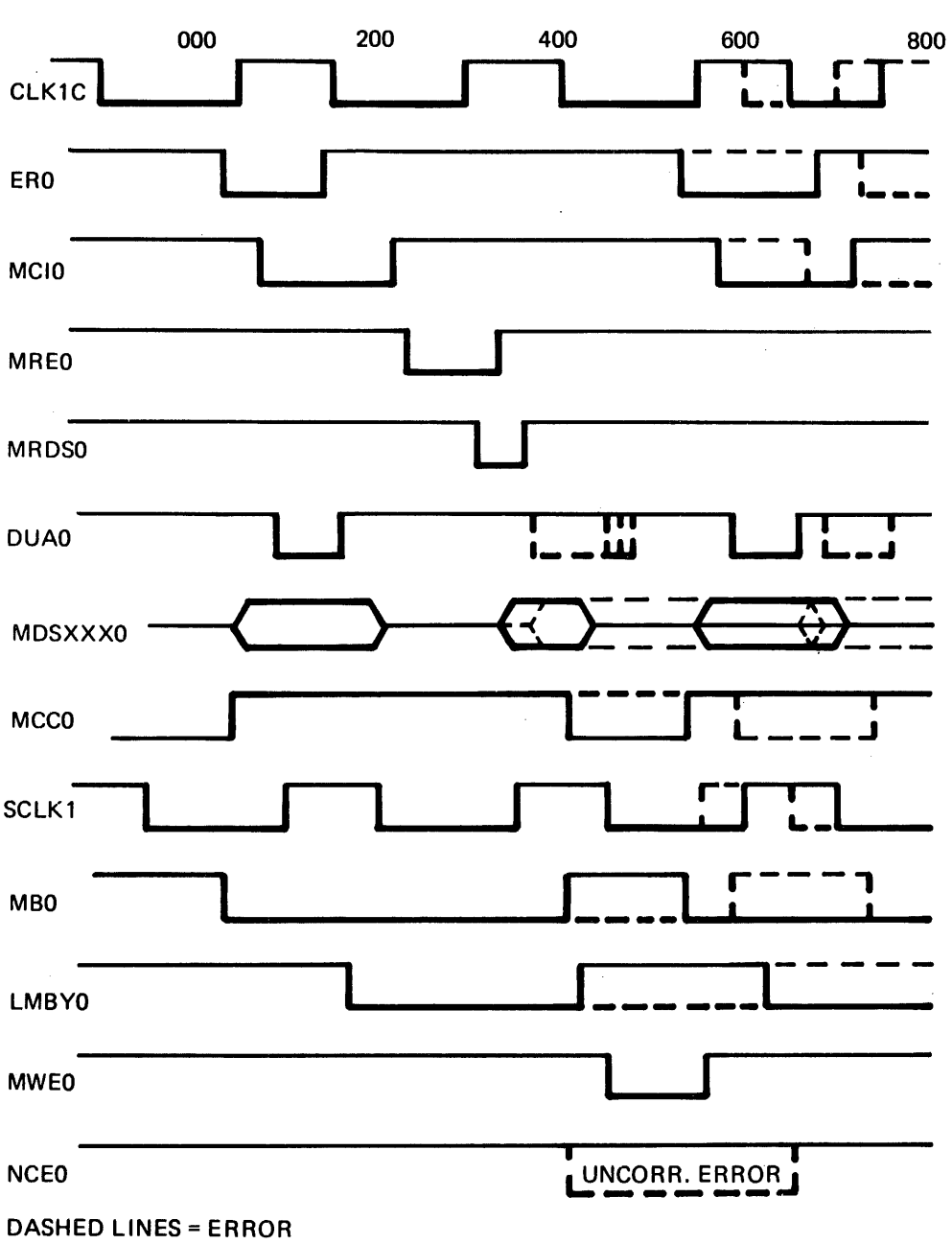
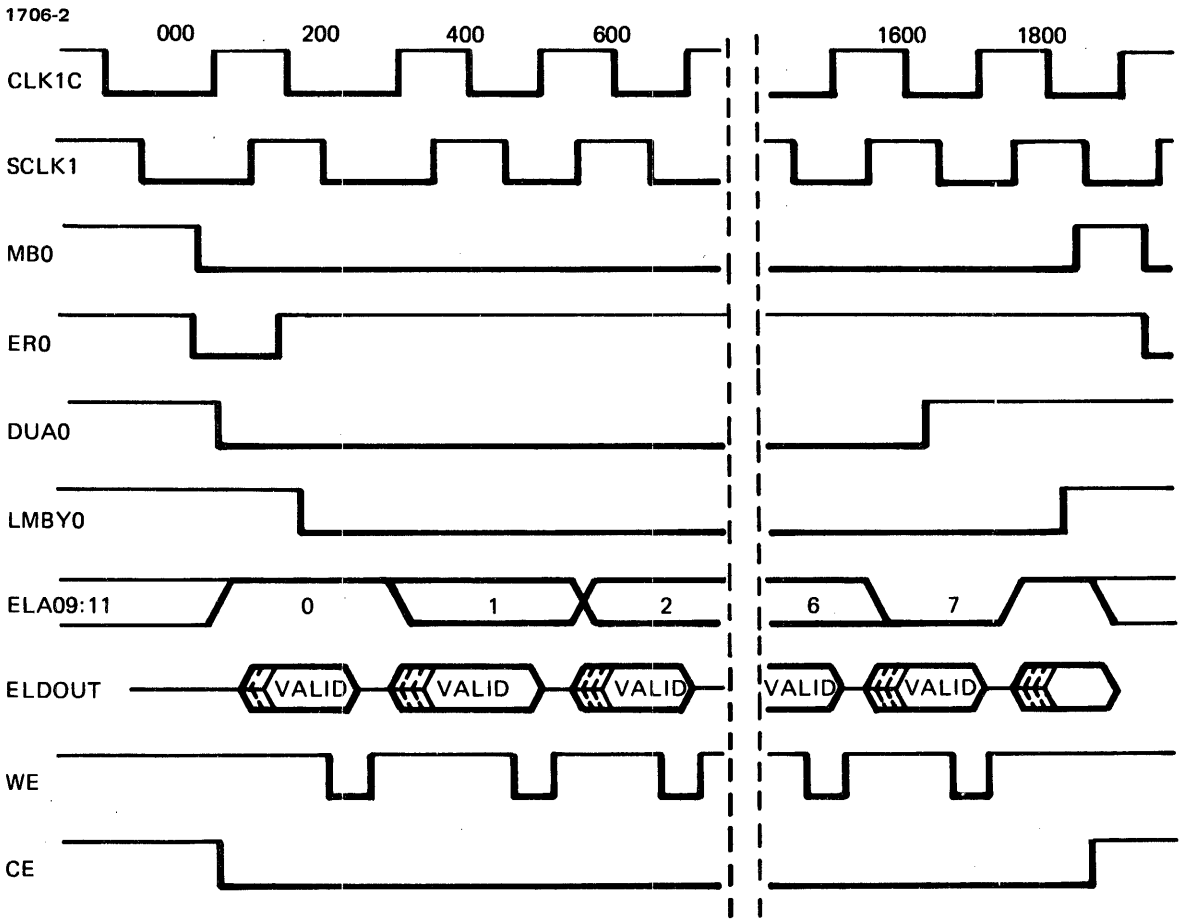
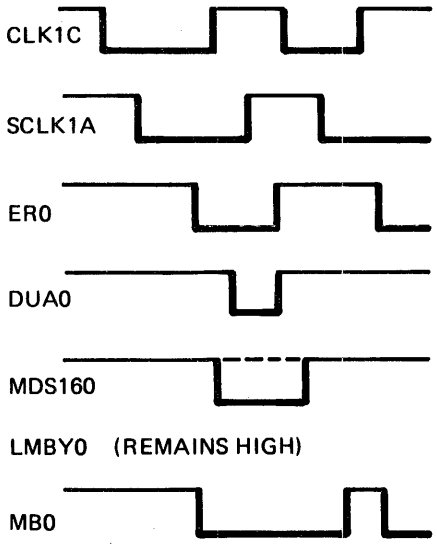


Figure 13-7 Cache Bypass



A. Read Error Logger



B. Read Error Logger Status

Figure 13-8 Read Error Logger Status

Timing diagrams for the A and B timers are provided in Figures 13-9 and 13-10. Table 13-3 provides data and address bus alignment information. The subsequent sections describe each of the seven basic functional modes.

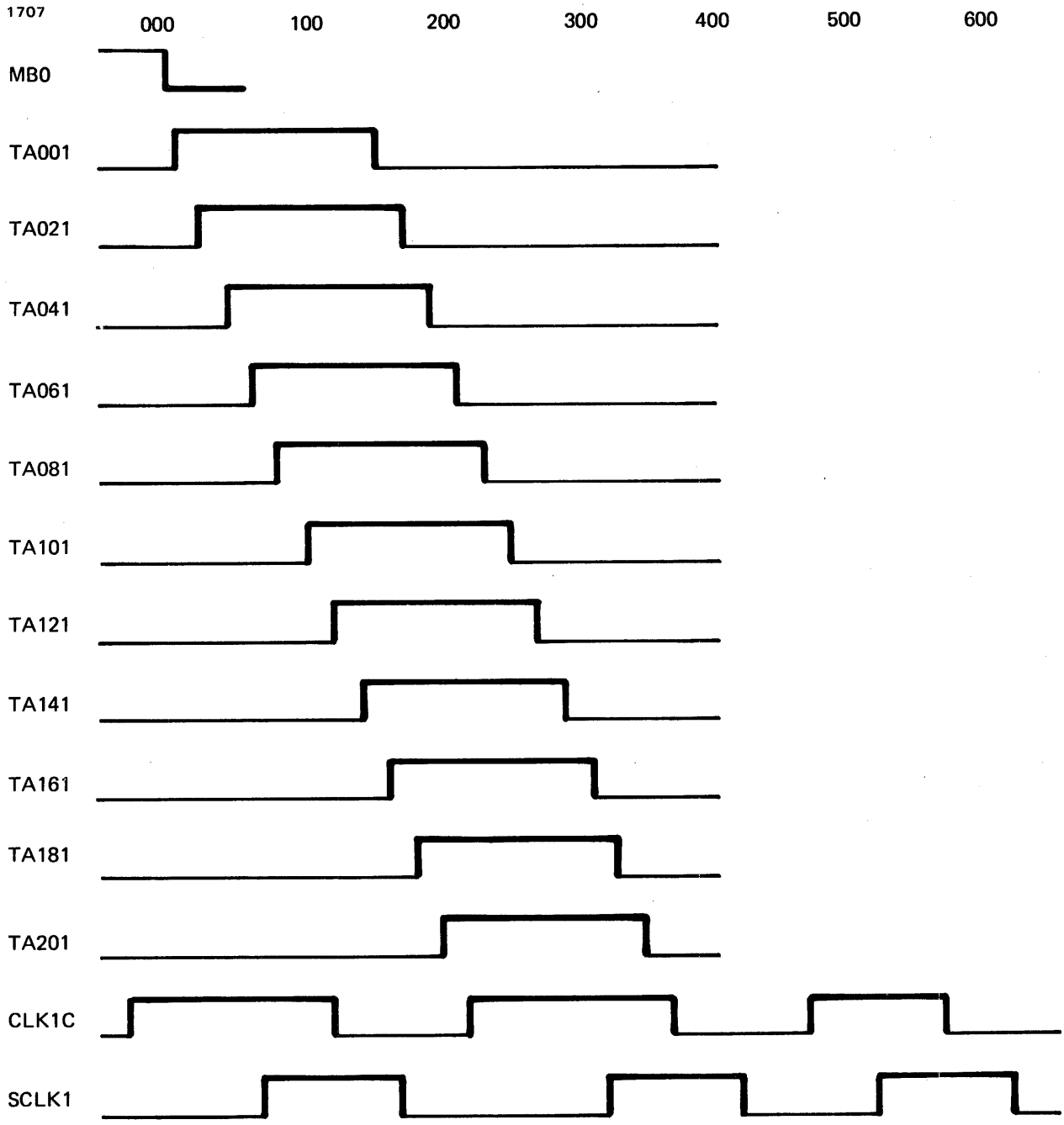


Figure 13-9 A Timer

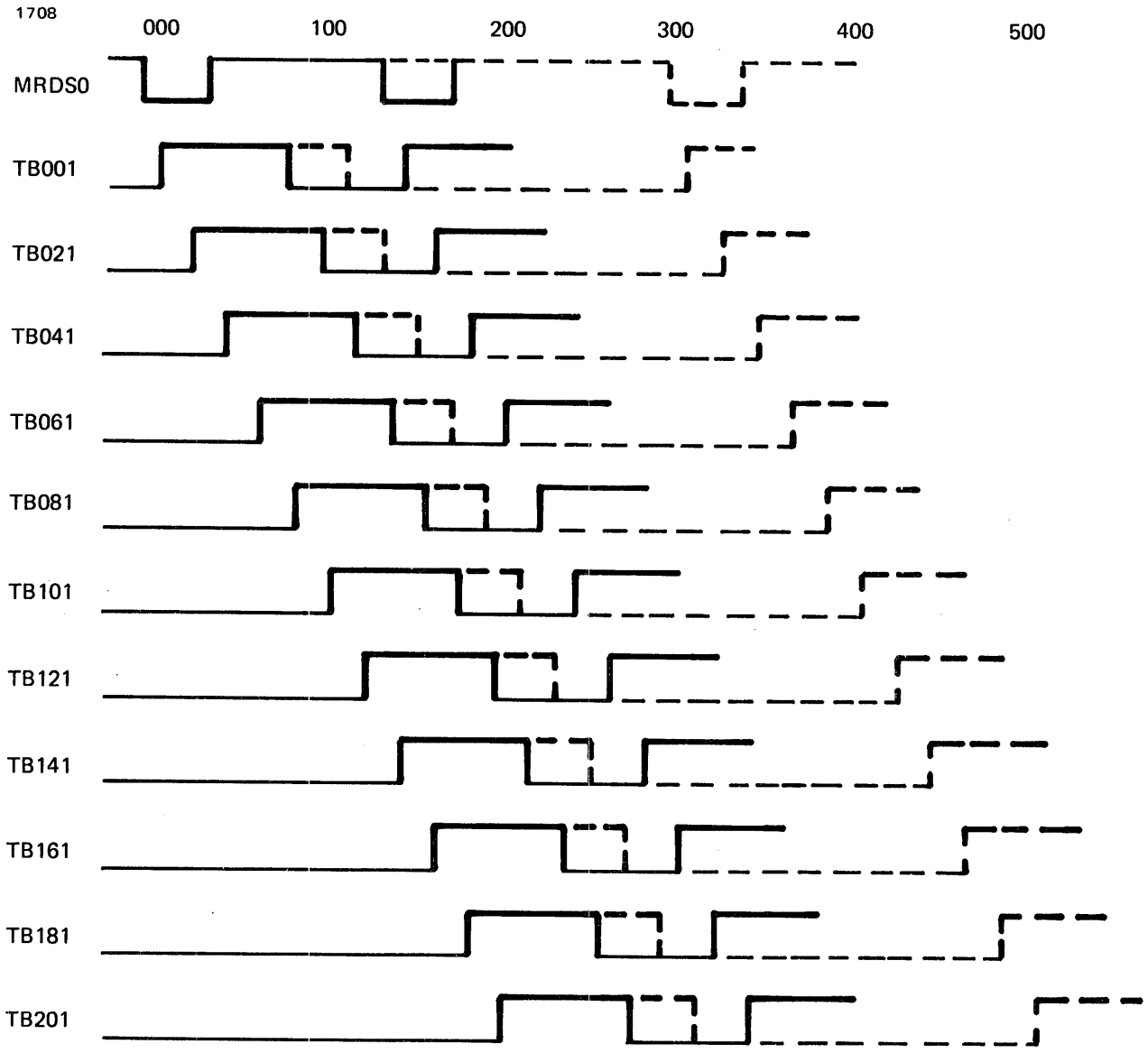


Figure 13-10 B Timer

TABLE 13-3 3230 MEMORY SYSTEM DATA AND ADDRESS BUS ALIGNMENT FOR SYSTEMS UP TO 4 MB OF MEMORY

1874-1

LMA	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	DATA
LMB							00 REF0	01 1	02 2	03 3	04 4	05 5	06 6	07	08	09	10	11	12	13	14	15			16 → 31 32 → 38
							← REFRESH ADDRESS →																		
35-764F02 (STM)			MEA0	1	2	BLK															MWA 000	MWA 010			
ERROR LOG ADDRESS & STATUS BIT			0	1	2	3	4	5	6	7	8														
			MOD. NO./BLK				WORD COLUMN LMA 28	LMA 29	S0	S1	S2	ST. BIT													
A BUS	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
MDS							0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			16 → 31
ERROR LOG DATA																									16 → 31
ERROR LOG STATUS BIT																									ST. BIT
ELA ADDRESS BUS			A 10	A 11	A 12	A 13	ELA 04	ELA 05	ELA 06	ELA 07	ELA 08	ELA 09	ELA 10	ELA 11	ELA CE										
EL WRITE ADDRESS			A 10	A 11	A 12	A 13	WA 0	WA 1	S 0	S 1	S 2	S 3	S 4	S 5	S 6										
EL READ ADDRESS			A 10	A 11	A 12	A 13	A 14	A 15	A 16	A 17	A 18	A 19	AD 2	AD 1	AD 0										

13.2.2.1 Store Fullword

A store fullword cycle is initiated at the processor by setting up the write data lines MDS000:310 (2A4), address lines LMA080:310 (3A1-3A9), write control line WRT0 (3A6), and mode control lines DMAHW0 (3A6), PSEL1, and RD011:031 (3A7). After these lines are set up, the processor generates an ER0 (13G7), clocking the MB1 flip-flop set, thereby starting the memory cycle. MB1 going active causes write data to be latched in the input data register (2G8), addresses to be latched in the address register (3A), and the control lines in their respective registers (3A6). MB0 having set the TA timer flip-flop (16B6) causes MCI0 (16S5) to go active, latching up the address presented on LMB001:151 (3G5,3L2) into the STM selected by lines MEA020 and MEA030 (9G). After satisfying the STM address hold time, the EA0 flip-flop (16R4) is set, thereby tri-stating the LMB001:151 address drivers (3G5,3L2). TA101 (2R4 and 15B2) going active enables the input data register (2G8) and the data bus drivers (Sheets 8 and 9), placing the word to be written onto lines D000:310 and LMB000:310. Lines D000:310 are input to the parity generators (4C5,4F5), whose outputs P000:060 propagate through the write parity register (7F7) onto lines GP000:060. This causes the parity data to be placed onto lines LMB321:381 by the parity data drivers (9E8). TAA121 (15A4) causes WE0 to go low, activating MWE0 (9G3), allowing the data present on lines LMB001:381 to be written into the selected STM. Following the removal of WE1 (14J3), NCLR1 (14R4) goes active, clearing the MB1 flip-flop (13K7) which enables MCC0 (9G2). With MCC0 activated, the write cycle is completed and CLK0D (15M9) causes LMBY0 to go high, signaling to the prccessor that the memory is no longer busy.

13.2.2.2 Store Partial Word

A store partial word cycle is initiated in the same way as described in the store fullword description. The cycles differ in that the word to be modified must be read from the STM before performing the write. This is necessary to allow new parity data to be generated from the modified word. The following description continues from the point just prior to enabling the input data register, as described in the store fullword operation.

WDEN0 (2R4) going active enables the input data register (2G8), placing the byte (store byte operation or test error log operation) or halfword (store halfword operation) of write data onto data lines D000:310. WDEN0 (14K9) also activates LDBY01:31, causing D000:310 to be loaded into the Good Data Registers (GDR) (Sheet 6).

NOTE

WDEN0 does not go active during a read and set operation.

TA161 (15G1) going active sets the RE1 flip-flop (15J3) which, in turn, activates the Uncorrected Data Register (UDR) (Sheets 8 and 9) and MRE0 (9G1). The STM responds in 240 nanoseconds by activating MRDS0 (9G6), signaling that lines LMB001:381 have been loaded with the read data. RDS0 causes the RE1 flip-flop (15J3) to be reset, removing MRE0 (9G1), latching the UDR (Sheets 8 and 9) and starting the TB timer (16B2). Data lines D000:310 and UP000:060 propagate through the parity checkers (Sheets 4 and 5), generating the Error Check and Correction (ECC) syndrome code on lines P000:060. If no data bit errors are generated, the syndrome code lines are all low deactivating MER0 (5N2). If a single data bit is in error, MER0 goes low along with one output from the DC error decoder (5J8) and one output from the DA or DB error decoder. One of the correction lines EB000:310 (Sheet 6) or EPB000:060 (7C4) goes high, causing the data bit in error to be input to the GDR (Sheet 6) or Good Parity Register (GPR) (7F4) to be corrected (inverted). If any two data bits are in error, MER0 goes low, correction lines EB000:310 and EPB000:060 remain low (no correction), and the uncorrectable error decoder (7M5) goes low allowing the UCE0 flip-flop (7N4) to be activated. UCE0 at AOI gate 20K (15B2) prevents activating ED1 and ED0 when the modified word is written back into the STM, causing all logical ones to be stored in the STM. This is necessary because the new parity data generated could otherwise make the data appear error free on subsequent reads from this location. TB021 (14G9) going active causes LDGP1 (read and set or test error logger operation only) and select LDBY01:31 lines (14M7) to go active, thereby loading the part of the word not to be modified into the GDRs (Sheet 6). TB080 (14G9) going low deactivates LDBY01:31 and UDD0 (15L4) and activates GDD1 (15N4), placing the modified word onto lines D000:310 (Sheet 6). New parity data is generated from this word and appears on lines P000:060 (Sheets 4 and 5) which are loaded into the write parity register (7F7) and output on lines GP000:060.

NOTE

A test error logger operation does not store away new parity data, but it uses the old parity by enabling the GPR (7F4) onto lines GP000:060.

A read and set operation differs from the above description in that the entire word from the STM is loaded into the GDR and, in turn, output to the processor from the output data register (see read fullword operation for description). Additionally, the most significant bit of the halfword D000 or D160 (15G6), as addressed by LMA140, is set on write data line D000A or D160A (15K6) if MATRS0, DMARS0, or RST0 are activated. D020A is set on write data line D020A if MATRSD0 is activated.

TBB141 (15A2) activates ED1 and ED0, placing the modified word data and parity data onto lines LMB001:381 (Sheets 8 and 9). TB161 (15A4) causes WE0 and MWE0 (9G3) to go active, placing the STM in the write mode. WE1 (14J3) going inactive causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7), enabling MCC0 (9G2). LMBY0 (15N8), having gone high at the previous edge of CLK0D, signals to the processor that the cycle is complete and the memory is no longer busy.

A DMA read and set and MAT read and set operation is similar to a regular read and set operation, except that only bit 0 is set.

A MAT read and set dirty bit is also similar to a regular read and set operation except that bit 2 is set.

13.2.2.3 Read Fullword (Cache Bypassed)

The LBC operates in the cache bypassed mode for any DMA read operation, or for a CPU read operation with the cache bypass strap (16L7) removed (bypass enabled). When the LBC is not equipped with the cache buffer option, it must operate in the bypassed mode. Additionally, those equipped with the cache buffer may be operated in this mode for test or troubleshooting purposes.

A read fullword operation begins with the processor setting up the address bus and control lines to their appropriate states followed by the initiation of the cycle with ER0 (13G7) being activated. ER0 sets the MB1 flip-flop (13K7), causing the address register (3B3,3B7) and control registers (3A6) to be latched and the TA timer flip-flop (16B6) to be set. Lines MX021:031, LMB001:151 (3G3), and MEA000:030 (Sheet 9) are presented with the address which is latched into the selected STM by MCI0 (16S5). After satisfying the STM address hold time, EA0 (16S4) going active tri-states the address drivers (3E3,3E7,9L8).

TA161 (15G1) going active sets the RE1 flip-flop (15J3) which, in turn, activates the UDR (Sheets 8 and 9) and MRE0 (9G1). The STM responds in 240 nanoseconds by activating MRDS0 (9G6) signaling that lines LMB001:381 have been loaded with the read data. RDS0 causes the RE1 flip-flop (15J3) to be reset, removing MRE0 (9G1), latching the UDR (Sheets 8 and 9) and starting the TB timer (16B2). Data lines D000:310 and UP000:060 propagate through the parity checkers (Sheets 4 and 5), generating the Error Check and Correction (ECC) syndrome code on lines P000:060. If no data bit errors are generated, the syndrome code lines are all low deactivating MER0 (5N2). If a single data bit is in error, MER0 goes low along with one output from the DC error decoder (5J8) and one output from the DA or DB error decoders. One of the correction lines EB000:310 (Sheet 6) or EPB000:060 (7C4) goes high, causing the data bit input to the GDR (Sheet 6) or GPR (7F4) to be corrected (inverted). If any two data bits are in error, MER0 goes low, correction lines EB000:310 and EPB000:060 remain low (no correction), and the uncorrectable error decoder (7M5) goes low, allowing the UCE0 flip-flop (7N4) to be activated.

TB080 causes lines LDBY01:31 and LDGP1 (14M6) to load and enable the GDRs (Sheet 6) and the GPR (7F3), placing the data (corrected) onto lines D000:310 and GP000:060. ODD1 (16N3) going active places this data onto the MDS000:310 lines (2A5) for the processor. If an error has been detected, TBB101 (15A1) activates ED1 and ED0 enabling the write data drivers (Sheets 8 and 9) onto LMB001:381; TBB121 (15A3) activates WE0, enabling MWE0 (9G4); and WE0 (14J3) going inactive causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7). If no errors were detected, NE1 (14J2) going active causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7). CLK0D (15M9) going active with DUA0 inactive raises the LMBY0 line, signaling to the processor that the memory is no longer busy.

13.2.3 Cache Option Description

The LBC is equipped with a 256-word cache buffer. The following is a brief description of the cache circuit.

The cache consists of a 256x36 cache buffer (11H1-11H8) which contains byte parity logic (11L1-11L8) and a parity error indicator circuit (11R7). A 64x14 index buffer (12F6) and a 14-bit address comparator (12M3, 12M7) is used to directly map 4-word sets (quadword blocks) stored in the cache buffer. A 64x1 (1/4 of 256x1 RAM IC 26R) validator buffer (12N1) is used to qualify the contents of the index buffer.

The cache buffer is loaded with four consecutive words of data any time a CPU read operation is executed at an address which is not contained in the index buffer (MIS1 high) (12S6), or which is not qualified by the validator (NVAL1 high) (12R3). The cache buffer is also updated with the single word of a store fullword or partial word operation if the index buffer contains the address (MIS1 low) and it is qualified by the validator (NVAL1 low). In this way, the contents of a valid block (4-word set) always matches what is stored in the STM.

The memory system contains up to 4 Mb (1 M words) of storage and the cache buffer contains 256 words (64 x 4-word sets) of storage. The cache buffer is always loaded with a 4-word set as addressed by the index field (refer to Figure 13-11).

1875

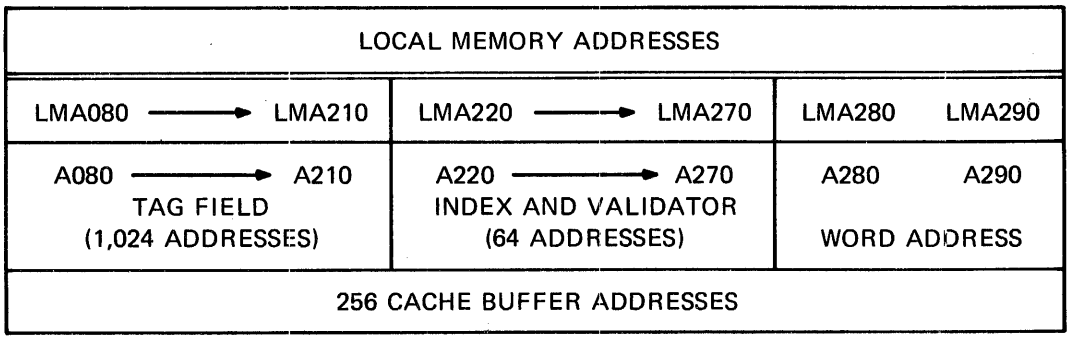


Figure 13-11 Physical Address Fields

This word set may be stored in the STM at any one of the 1,024 locations as addressed by the tag field. When the cache buffer is loaded with a 4-word set, the 14 bits of the tag field are loaded into the index buffer, and the validator bit is set at the location as addressed by the index field. A subsequent CPU read from one of the four word locations generates a match condition at the index address comparator (12M3, 12M7, causing MIS1 (Index Mismatch) to go inactive. Validator output NVAL1 (not valid) goes inactive and is ORed with MIS1, allowing the HIT1 flip-flop to be set. This is called a cache Hit and indicates that the word being addressed is contained in the cache buffer. CPU reads from word locations that are not stored in the cache buffer cause MIS1 (12S6) or NVAL1 to go active, preventing the HIT1 flip-flop from being set. This is called a cache Miss.

13.2.4 CPU Read Fullword (Cache Enabled)

13.2.4.1 Cache Miss

Upon initially powering up the system, a CPU read from any memory location must produce a Miss (refer to cache description) condition because the cache buffer is volatile, and depowering the system causes its contents to be lost. When the consolette power switch has been placed to the ON position or the INITIALIZE switch has been depressed, the main memory remains in the burst refresh mode for a period of time determined by the initialize timer. During this period of time, the validation buffer (12N2) is input with refresh addresses A150:200 from its address multiplexor (12K2), the data input VAL1 is set low (invalid), and the write enable is activated by TA061 (12N3) at IC 22C pin 05. This causes all 64 locations of the invalidator to be written to the invalid state synchronously with the performance of the burst refresh operation.

When the processor initiates the first CPU read, the validator causes NVAL1 (12S6) to go active, preventing the HIT1 flip-flop from being set and activating QWM0, QWM1, and QWE0 (16S7). QWE0 (9K7) causes LMB160 to go low, signaling to the STM that a quadword operation is to be initiated. QWM1 (16K6) allows TA101 to activate MCI0, starting a quadword read cycle. TA160 (15F4) going active sets the RE1 flip-flop (15J3) which, in turn, activates the UDR (Sheets 8 and 9) and MRE0 (9G1). The STM responds in 240 nanoseconds by activating MRDS0 (9G6), signaling that lines LMB001:381 have been loaded with the read data. RDS0 causes the RE1 flip-flop (15J3) to be reset, removing MRE0 (9G1), latching the UDR (Sheets 8 and 9), and starting the TB timer (16B2). Data lines D000:310 and UP000:060 propagate through the parity checkers (Sheets 4 and 5), generating the Error Check and Correction (ECC) syndrome code on lines P000:060. If no data bit errors are generated, the syndrome code lines are all low deactivating MER0 (5N2). If a single data bit is in error, MER0 goes low along with one output from the DC error decoder (5J8) and one output from the DA or DB error decoders. One of the correction lines EB000:310 (Sheet 6) or EPB000:060 (7C4) goes high, causing the data bit in error to be input to the GDR (Sheet 6) or GPR (7F4) to be corrected (inverted). If any two data bits are in error, MER0 goes low, correction lines EB000:310 and EPB000:060 remain low (nc correction), and the uncorrectable error decoder (7M5) goes low, allowing the UCE0 flip-flop (7N4) to be activated. UCE0 (12A1) going active causes VAL1 (12N1) to go low, invalidating the word to be stored in the cache buffer.

LDGP1 and LDBY01:31 (14M5-14M9) are activated, loading the corrected word and parity bits into the GDR (Sheet 6) and GPR (7F3). RURE1 (15K4) causes UDD0 to go active and GDD1 to go inactive, disabling the UDR (Sheets 8 and 9) and enabling the GDR and GPR. The corrected word data is output to lines MDS000:310 by the GDR (Sheet 2), returning the word requested by the processor. This word is also written into the cache buffer via lines D000:310 (11J7), along with four parity bits generated by the cache parity circuits (11L2-11L8). If a memory error has been detected, ME1 (15B3) is active, allowing TB121 to activate WE0 (15F3) and MWE0 (9G4), causing the corrected data (D000:310 and GP000:060) appearing on lines LMB001:381 (Sheets 8 and 9) to be written back into the STM. WE1 (15E3) going inactive sets the EWE1 flip-flop (15F3), causing the RE1 flip-flop (15J3) to be set and the ME1 and NE1 flip-flop (15L2) to be reset. TBB040 (3H7) or NE1 (no error detected) causes the word counter (WA011 and WA001) to be advanced, placing the next word address on lines MWA001 and 011 (9G5) prior to MRE0 (9G1) being reactivated. The STM responds with the second word of data reactivating MRDS0 within 40 nanoseconds after MRE0 has gone active. The word, along with the parity bits, is processed by the ECC circuit and stored into the cache buffer at the next word address; but it is not output onto lines MDS000:310. The processor, having received the first word of data, no longer expects an output from the memory, but is waiting for the memory to go not busy.

This cyclic mode of operation continues until the fourth word has been read from the STM and has been processed. WC0 (15G2) goes active when the word address counter (3N6) has been advanced to the fourth word count, preventing the RE1 flip-flop (15J3) from generating any further MRE0 (9G1) pulses. After processing the fourth word, WCC1 (14J2) goes inactive, causing NCLR1 (13G9) to reset the MB1 flip-flop (13K7). The cache buffer (11H5) now contains the 4-word set that resides in the STM at the tag field address (A080:210), which is stored in the index buffer (12E5) at the location addressed by the index field (A220:270). If none of the four words contained uncorrectable errors, the validation buffer location, as addressed by the index field, is set (valid); otherwise, it is reset (not valid).

13.2.4.2 Cache Hit

A cache hit occurs on a CPU read operation if MIS1 (16L7), NVAL1 (16L8) and PER1 (16L8) do not go active, thereby preventing QWM1, QWM0, and QWE0 from going active. This causes the word of data to be output from the cache buffer (11H5) onto lines D000:310 which are loaded into the ODR (Sheet 2) and output onto lines MDS000:310.

A cache hit occurring on a store fullword or store partial word operation causes the new word stored in the STM to be loaded into the cache buffer. A cache hit occurring on a test error logger operation or read and set operation, and an uncorrectable error being detected on a store partial word operation cause the valid bit to be reset (not valid). Cache operation criteria is provided in Table 13-4.

13.2.5 Read Error Logger (Including ECC Description)

The error logger consists of an 8k x 1 (two 4k x 1 RAMs) buffer (10L8), an address multiplexor (10F1), a 16-bit shift register (10K1 and 10K5), a shift address generator (10D6), a syndrome code register (10C8), an Error Status flip-flop (10N2), and control circuitry (Sheet 10).

13.2.5.1 ECC Circuit Description

The Error Check and Correction (ECC) circuitry (Sheets 4 through 7) consists of parity/syndrome generators P000:060 (Sheets 4 and 5); error detector MER0 (5M3); first-level error decoders DA0:7, DB0:7, and DC0:7 (5J7); correction bit decoders EB000:160 (Sheet 6) and EPB000:060; uncorrectable error detector (UCE0) with LED display indicator (7M5 and 7R7); and Exclusive-OR bit correction gates (Sheets 6 and 7). The ECC code implemented provides detection and correction of all single-bit errors and detection of all double-bit error combinations.

TABLE 13-4 CACHE OPERATICN CRITERIA

LOAD CACHE BUFFER
1. Store Fullword operation with a hit (singleword load) 2. Store Partial Word operation with a hit (singleword load) 3. CPU Read with a miss or cache parity error (quadword load)
RESET VALID BIT (INVALIDATE)
1. Test Error Logger operation with a hit. 2. Read and Set operaticn with a hit. 3. Store Partial Word operation with uncorrectable error and a hit. 4. Quadword load to cache buffer with uncorrectable error(s). 5. Initialization or power-up of system (invalidates all 64 locations)
SET VALID BIT
1. Quadword load to cache buffer with no uncorrectable errors detected.
LOAD INDEX BUFFER
1. Quadword load

The Error Correction Code (ECC) logic is used to generate the proper parity bits (P00:P06) when writing into the STM (LMB32:LMB37) or to check the 39-bit data word read from the STM.

When writing into memory, the data to be written is available on D00:D31. The seven parity bits (UP00:UP06) are forced low. The resulting parity bit (P00:P06) outputs, along with the 32-bit data word, are written to the STM. (Refer to Table 13-5.)

Reading from the STM fetches a 39-bit data word, which is provided on the inputs of the ECC logic (D00:D31 and P00:06). The syndrome output should be all zero if there is no error. (Refer to Table 13-5.) The syndrome output bits (P00:P06) are decoded to correct any single-bit error. Refer to Table 13-6 for decoding the syndrome bits after a read operation.

TABLE 13-5 ERROR CORRECTION CODE (ECC) LOGIC TABLE

1003

PARITY TO BE WRITTEN ON WRITE

DATA TO BE WRITTEN ON WRITE

FORCED LOW ON WRITE

P00:06

D000:310 (LOW ACTIVE BUS)

UP00:06

P00:06							D000:310 (LOW ACTIVE BUS)																										UP00:06							PARITY TYPE
0	1	2	3	4	5	6	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	0	1	2	3	4	5	6	
X							X	X	X		X	X	X		X					X			X					X			X					X	X		X							ODD
	X						X			X	X	X		X		X			X		X					X		X			X				X	X			X						EVEN
		X						X		X	X		X	X			X			X					X			X				X				X	X							ODD
			X						X			X	X	X				X			X	X			X		X	X	X				X					X						EVEN
				X			X	X	X	X					X	X	X	X					X	X	X	X									X				X						ODD
					X										X	X	X	X	X	X	X	X									X	X	X	X	X	X	X					X			EVEN
						X																	X	X	X	X	X	X	X	X	X	X	X	X	X								X		EVEN

X = BITS USED TO GENERATE SYNDROME

ON READ SYNDROME OUTPUTS SHOULD BE ZERO IF NO ERROR

DATA READ FROM THE STM

EXAMPLE: DATA TO BE WRITTEN = X'00000000' PARITY GENERATED = 1001000
DATA READ AFTER WRITE = X'80000000' PARITY READ = 1001000 SYNDROME RESULT = 1100100 DATA BIT 0 ERROR (SEE TABLE 13-4)

TABLE 13-6 ECC SYNDROME CODE

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION	
0	0	0	0	0	0	0	NE	0	
0	0	0	0	0	0	1	PB6	1	
0	0	0	0	0	1	0	PB5	2	
0	0	0	0	0	1	1	ME	3	
0	0	0	0	1	0	0	PB4	4	
0	0	0	0	1	0	1	ME	5	
0	0	0	0	1	1	0	ME	6	
0	0	0	0	1	1	1	DB28	7	0
0	0	0	1	0	0	0	PB3	8	
0	0	0	1	0	0	1	ME	9	
0	0	0	1	0	1	0	ME	10	
0	0	0	1	0	1	1	DB27	11	
0	0	0	1	1	0	0	ME	12	
0	0	0	1	1	0	1	DB19	13	
0	0	0	1	1	1	0	DB11	14	
0	0	0	1	1	1	1	ME	15	
0	0	1	0	0	0	0	PB2	16	
0	0	1	0	0	0	1	ME	17	
0	0	1	0	0	1	0	ME	18	
0	0	1	0	0	1	1	DB26	19	
0	0	1	0	1	0	0	ME	20	
0	0	1	0	1	0	1	DB18	21	
0	0	1	0	1	1	0	DB10	22	1
0	0	1	0	1	1	1	ME	23	
0	0	1	1	0	0	0	ME	24	
0	0	1	1	0	0	1	DB23	25	
0	0	1	1	0	1	0	DB15	26	
0	0	1	1	0	1	1	ME	27	
0	0	1	1	1	0	0	DB31	28	
0	0	1	1	1	0	1	ME	29	
0	0	1	1	1	1	0	ME	30	
0	0	1	1	1	1	1	ME	31	
0	1	0	0	0	0	0	PB1	32	
0	1	0	0	0	0	1	ME	33	
0	1	0	0	0	1	0	ME	34	
0	1	0	0	0	1	1	DB25	35	
0	1	0	0	1	0	0	ME	36	
0	1	0	0	1	0	1	DB17	37	
0	1	0	0	1	1	0	DB9	38	
0	1	0	0	1	1	1	ME	39	2
0	1	0	1	0	0	0	ME	40	
0	1	0	1	0	0	1	DB22	41	
0	1	0	1	0	1	0	DB14	42	
0	1	0	1	0	1	1	ME	43	
0	1	0	1	1	0	0	ME	44	
0	1	0	1	1	0	1	ME	45	
0	1	0	1	1	1	0	ME	46	
0	1	0	1	1	1	1	ME	47	

TABLE 13-6 ECC SYNDROME CODE (Continued)

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION
0	1	1	0	0	0	0	ME	48
0	1	1	0	0	0	1	DB20	49
0	1	1	0	0	1	0	DB12	50
0	1	1	0	0	1	1	ME	51
0	1	1	0	1	0	0	DB3	52
0	1	1	0	1	0	1	ME	53
0	1	1	0	1	1	0	ME	54
0	1	1	0	1	1	1	ME	55
0	1	1	1	0	0	0	DB7	56
0	1	1	1	0	0	1	ME	57
0	1	1	1	0	1	0	ME	58
0	1	1	1	0	1	1	ME	59
0	1	1	1	1	0	0	ME	60
0	1	1	1	1	0	1	ME	61
0	1	1	1	1	1	0	ME	62
0	1	1	1	1	1	1	ME	63
1	0	0	0	0	0	0	PB0	64
1	0	0	0	0	0	1	ME	65
1	0	0	0	0	1	0	ME	66
1	0	0	0	0	1	1	DB24	67
1	0	0	0	1	0	0	ME	68
1	0	0	0	1	0	1	DB16	69
1	0	0	0	1	1	0	DB8	70
1	0	0	0	1	1	1	ME	71
1	0	0	1	0	0	0	ME	72
1	0	0	1	0	0	1	DB21	73
1	0	0	1	0	1	0	DB13	74
1	0	0	1	0	1	1	ME	75
1	0	0	1	1	0	0	DB2	76
1	0	0	1	1	0	1	ME	77
1	0	0	1	1	1	0	ME	78
1	0	0	1	1	1	1	ME	79
1	0	1	0	0	0	0	ME	80
1	0	1	0	0	0	1	ME	81
1	0	1	0	0	1	0	DB30	82
1	0	1	0	0	1	1	ME	83
1	0	1	0	1	0	0	DB1	84
1	0	1	0	1	0	1	ME	85
1	0	1	0	1	1	0	ME	86
1	0	1	0	1	1	1	ME	87
1	0	1	1	0	0	0	DB6	88
1	0	1	1	0	0	1	ME	89
1	0	1	1	0	1	0	ME	90
1	0	1	1	0	1	1	ME	91
1	0	1	1	1	0	0	ME	92
1	0	1	1	1	0	1	ME	93
1	0	1	1	1	1	0	ME	94
1	0	1	1	1	1	1	ME	95

TABLE 13-6 ECC SYNDROME CODE (Continued)

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION	
1	1	0	0	0	0	0	ME	96	
1	1	0	0	0	0	1	ME	97	
1	1	0	0	0	1	0	DB29	98	
1	1	0	0	0	1	1	ME	99	
1	1	0	0	1	0	0	DB0	100	
1	1	0	0	1	0	1	ME	101	
1	1	0	0	1	1	0	ME	102	
1	1	0	0	1	1	1	ME	103	6
1	1	0	1	0	0	0	DB5	104	
1	1	0	1	0	0	1	ME	105	
1	1	0	1	0	1	0	ME	106	
1	1	0	1	0	1	1	ME	107	
1	1	0	1	1	0	0	ME	108	
1	1	0	1	1	0	1	ME	109	
1	1	0	1	1	1	0	ME	110	
1	1	0	1	1	1	1	ME	111	
1	1	1	0	0	0	0	DB4	112	
1	1	1	0	0	0	1	ME	113	
1	1	1	0	0	1	0	ME	114	
1	1	1	0	0	1	1	ME	115	
1	1	1	0	1	0	0	ME	116	
1	1	1	0	1	0	1	ME	117	
1	1	1	0	1	1	0	ME	118	
1	1	1	0	1	1	1	ME	119	7
1	1	1	1	0	0	0	ME	120	
1	1	1	1	0	0	1	ME	121	
1	1	1	1	0	1	0	ME	122	
1	1	1	1	0	1	1	ME	123	
1	1	1	1	1	0	0	ME	124	
1	1	1	1	1	0	1	ME	125	
1	1	1	1	1	1	0	ME	126	
1	1	1	1	1	1	1	ME	127	

NOTE

PB = Parity Bit
DB = Data Bit
ME = Multiple Bit Error

During a faulty read operation, data from the STM is input to the parity check generators causing one or more parity/syndrome lines P000:060 to go high and activating MER0 (5N2). These lines are also input to the first level decoders (5J5-5J8), whose outputs are further decoded by the correction bit generators (Sheet 6 and 7C3). If a single-bit error is detected, one correction line EB000:160 or EPB000:060 goes high (active), correcting the bit in error. If the error detected was not a single bit error, lines EB000:160 and EPB000:060 remain low (no correction) causing UCE0 (7N3) to go active and latching the address (1 of 4) of the faulty STM in the uncorrected error display (7R7).

13.2.5.2 Error Logger Description

Parity/syndrome lines P000:060 are latched in the syndrome register (10C8) whose outputs S000:S050 are steered onto error log address lines ELA04:11, along with the word address lines WA000 and 010 via the address multiplexors (10E1 and 10G1). Line S060 is used as the error log RAM Chip Enable (CE) decode, placing all even codes (refer to Table 13-6) into 4k x 1 RAM 17K (10K8) and odd codes into 4k x 1 RAM 14k (10N8). STM module select address lines ELMA0:3 (10J7 and 10M7) are input directly to the 4k x 1 RAMs as most significant addresses. ME1 (10F5) and ME0 (10R7), having gone active, cause a low to be written into the address location of the selected RAM. In this way, all the information necessary to locate the failing bit (syndrome code lines S000:060) of a specific word column (WA000 and 010) on the faulty STM (ELMA0:3) is contained by the error log RAM address. The single bit (LD01 or LD02) stored at a specific address validates the address information (zero stored) or invalidates it (one stored).

There are two operations provided for obtaining error logger information; read error logger status and read error logger. Both operations are initiated by sending the read error log code on lines RD011:31 and setting address bit LMA030 for a read error logger status or resetting address bit LMA030 for a read error logger operation.

A read error logger status operation responds with line MDS160 being set if the error logger contains error information, or reset if no errors have been stored. The status flip-flop (10N2) is reset upon performing a read error logger status operation. A read error logger operation takes the address presented on lines LMA080:180 and steers it to the error log RAMs (10K8, 10N8) via the address multiplexor, along with lines AD01:21 from the shift counter (10E5). The contents of eight address locations are read from each 4k x 1 RAM (operated in parallel) and loaded into their respective shift registers. Each address location is written back to a one (no error state) before reading out from the next address location. The timing used to perform this operation is derived from system clocks CLK1D and SCLK1A (10B4).

After loading the shift registers, their contents are enabled onto lines D160:310, which output onto lines MDS 160:310 by the output data register (Sheet 2). AD31 (14J2) going active causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7), readying it to accept the next ER0. RCAR0 (10M3), having gone active, allows the ELDUA1 flip-flop to be reset, removing DUA0 (15M8) and causing LMBY0 (15N8) to be deactivated on the next transition of CLK0D.

13.3 MNEMONICS

The following is a list of the mnemonics used on the LBC board. The meaning and 35-771D08 schematic source of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
A080:A310	Internal address bus lines	Sheet 3
AD01:AD31	Shift counter bits	10E6
BMCI0	Buffered memory cycle initiate	9R6
BMVF0	Buffered memory voltage failure	3S8
BSCLR0	Buffered system clear	9R4
BYP0/1	Cache bypass	16K6,16L8
CAEN0/1	Cache enable flip-flop	16S6
CAR1	Refresh counter carry	13H5
CAWE0	Cache write enable	11E2
CB011:CB031	Control bits	3G8
CH1T1	Cache Hit	12S5
CLK0D	Buffered processor clock	10D4
CLK1C	Processor clock	9N8
CLK1D	Buffered processor clock	9S8
CLR0	Cycle steal clear	13D2
CLR0B	Clear DU circuit	15E7
CLTB1	TB timer feedback	16A1
CPER1	Buffered cache parity detect	16R8
CVF1	Clear voltage fail detector	14E8
D000:D310	Internal data bus lines	Sheets 2,6,8, 9,10,11
D000A	Test and set bit	15K5
D160A	Test and set bit	15K6
DA0:DA7	First-level error decode bits	5K6,5K7
DB0:DB7	First-level error decode bits	5K5,5K6
DC0:DC7	First-level error decode bits	5K8,5K9
DERR0	Disable error correction line	5G6
DHW0	Buffered DMA halfword line	3D6
DMAHW0	DMA halfword line	3A6
DPR1	Depower line	13K2
DRFW0/1	DMA read fullword	14E7
DRST0	DMA read and set	14D1
DSFW0	DMA store fullword	14D4
DSHW0	DMA store halfword	14D3
DUA0/1	Data unavailable	15N7

MNEMONIC	MEANING	SCHEMATIC LOCATION
EA0/1	Enable address flip-flop	16S4
EB000:EB310	Data bit correction lines	Sheet 6
ED0/1	Enable data lines	15G1
ELMA00:30	Module address to error logger	3G2,3G3
EL0	Error logger select line	14H5
ELA04:ELA11	Error logger address lines	Sheet 10
ELDUA0/1	Error logger data unavailable	10N4
ELST1	Error logger status select line	14H5
END1	Standby end flip-flop	13F5
EPB000:EPB310	Parity bit correction lines	Sheet 7
ER0	Memory cycle start	13G7
EWE1	End write enable flip-flop	15F3
FNPM0/1	Nonpresent memory flip-flop	14S5
GDD1	Good data disable flip-flop	15N4
GP000:GP060	Good parity lines	7H2,7H4
HIT0/1	Cache hit flip-flop	12S6
LD01	Error logger RAM output	10L8
LD02	Error logger RAM output	10R8
LDBY01:LDBY31	Load byte	Sheet 14
LDGP1	Load good parity line	14M5
LDOD1	Load output data register	16K9
LMA080:310	Local memory address lines	Sheet 3
LMB001:381	Local memory bus lines	Sheets 3,8,9
LMBY0/1	Local memory busy flip-flop	15N8
MATRSD0	MAT read and set dirty bit	14D1
MATRSR0	MAT read and set reference bit	14D1
MB0/1	Memory busy flip-flop	13K8
MB0A	Buffered memory busy lines	13N7
MB1A	Buffered memory busy lines	13N7
MB1B	Buffered memory busy lines	13N8
MB1C	Buffered memory busy lines	13N8
MCC0	Memory cycle complete line	9G2
MCI0	Memory cycle initiate line	16R5
MDS000:MDS310	Processor data bus lines	Sheet 2
ME0/1	Memory error flip-flop	15L2
MEA000:MEA030	Memory expansion address lines	9G1,4
MER0	Memory error detect line	15N1,5N2
MER1	Memory error detect line	15F8,5N6
MIS1	Cache index compare line	12S6
MRDS0	Memory read data strobe	9G6
MRE0	Memory read enable control line	9G1
MREF0	Memory refresh line	9G5
MVF0	Memory voltage fail	9N8
MWA001	Memory word address line	9G3
MWA011	Memory word address line	9G5
MWE0	Memory write enable control line	9G3

MNEMONIC	MEANING	SCHEMATIC LOCATION
NCE0	Noncorrectable error line	9S8
NCLR1	Normal clear line	14R4
NE0/1	No error flip-flop	15N2
NPM0	Nonpresent memory line	14R4
NVAL1	Valid RAM data output	12N3
ODD1	Output data disable	16N3
P000:P060	Parity/syndrome bits	Sheets 4,5
PER1	Cache parity error line	11R5
PFSD0/1	P5 shutdown lines	9R4
PRFW0/1	Processor read fullword line	14H5
PSBY0	Processor store byte line	14D2
PSEL1	Processor select line	3A6
PSEL1A	Buffered processor select line	3D6
PSFW0	Processor stcre fullword line	14D4
PSHW0	Processor store halfwcrd line	14D3
PUI0	Power-up initialize line	13F4
QWE0	Quadword enable line	16S7
QWM0/1	Quadword mode lines	16S8
RCAR0	Ripple carry line	10L3
RCLC0/1	STM refresh clear lines	9N5
RCLR0	Internal refresh clear line	13F5,13H4
RCT0/1	Refresh clear time select lines	13G9,13L4
RD011	ROM data line	3E7
RD021	ROM data line	3E7
RD031	ROM data line	3E7
RDS0/1	Buffered memory read data strobe lines	9R5
RE0/1	Read enable flip-flop	15K3
REF0/1	Refresh mode control lines	13N3
REF0A	Buffered refresh mode control line	13J3
REL1	Read error logger line	14H5
REQ1	Cycle steal request flip-flop	13D2
RFA0:RFA7	Refresh address bus	13N5
RFQ1	Refresh queue flip-flop	15L6
RFW1	Read fullword control line	14G6
RCAST1	Read and/or set control line	14H6
RSEL0	Refresh cycle steal select line	13G4
RST0/1	Read and set control lines	14H2
RURE1	Data bus control line	14M7
S000:S060	Syndrome bit lines	10D8,10D9
SBY1	Store byte control line	14H2
SCLK0A	Buffered processor shift clock	10D4
SCLK1	Processor shift clock	9N8
SCLK1A	Buffered processor shift clock	9S7

MNEMONIC	MEANING	SCHEMATIC LOCATION
SCLR0	Systems clear relay contact	13A3
SCLR0A	Systems clear line	13A3
SCLR0B	Buffered systems clear line	13G4
SCLR0C	Buffered systems clear line	13A4
SCLR1B	Buffered systems clear line	13A3
SFW0/1	Store fullword lines	14H4
SHIFT1	Shift register advance line	10L2
SHW1	Store halfwcrd line	14H4
SPW0/1	Store partial word line	14H2
STB0/1	Standby mode flip-flop	13H2
TA001:TA201	TA timer outputs	Sheet 16
TB001:TB161	TB timer outputs	Sheet 16
TEL0/1	Test error logger control lines	14H2
UCE0/1	Uncorrectable error flip-flop	7R4
UDD0/1	Uncorrectable data disable flip-flop	15L3
UFP1	P5U pullup	13F1
UP000:UP060	Uncorrected parity bit lines	9J8
VAL0/1	Valid bit data input	12H1
VF1	Voltage fail flip-flop	13N4
WA000/1	Word address counter bits	3S5
WA010/1	Word address counter bits	3S5
WC0	Word counter carry	3S8
WCC0/1	Word counter carry	3S7
WDEN0	Write data enable line	14M9
WE0/1	Write enable lines	15E3
WRT0	Write contrcl line	13J1
WRT0A	Buffered write control line	3M1
WRT1	Buffered write control line	14A3
XRP1	P5 pullup	15N3
XRP2	P5 pullup	14K3
XRP3	P5 pullup	3S7
XRP4	P5 pullup	10N4

CHAPTER 14
3230 STORAGE MODULE

14.1 INTRODUCTION

The Storage Module (STM) is a random access memory using either 16k or 64k dynamic MOS RAM chips as the storage element. Depending on the STM's functional variation, the total memory per STM is either 512 kb (F02), 1.024 Mb (F03) or 2.048 Mb (F04). The STM has on-board 4-way interleaving capability. The 39-bit data field is broken into 32 data bits and 7 parity bits. An organizational list of the STM functional variations is shown in Table 14-1. A block diagram of the STM is provided on Sheet 1 of functional schematic 35-764D08. A description of each block is given in the following sections.

TABLE 14-1 FUNCTIONAL VARIATIONS

PART NO.	VARIATION	MEMORY CAPACITY	ORGANIZATION	STORAGE ELEMENT
35-764	F02	512 kb	128 k x 39	16 k x 1
	F03	1.024 Mb	256 k x 39	64 k x 1
	F04	2.048 Mb	512 k x 39	64 k x 1

14.1.1 Module Select

Module select contains a set of 4 binary coded switches that permit the selection of modules from 1 of 16 STMs to a total capacity of 8 Mb (8 Mb mode). In addition to the switches, there is a strap option for three more expansion lines. This option provides the means to access additional memory up to 16 Mb (16 Mb mode). A component block layout is shown in Figure 14-1. Figure 14-2 is an example of the module selection switches.

Table 14-2 is a decode table for memory expansion up to 4 Mb using the 35-771 LBC. Table 14-3 is a decode table for memory expansion up to 8 Mb using the 35-806 LBC. Table 14-4 is an expansion decode table for memory exceeding 8.192 Mb and up to 16.384 Mb. The 35-771 LBC can be used for expansions up to 4 Mb only. For memory expansions between 8.192 Mb and 16.384 Mb, only the F03 (1 Mb) and F04 (2 Mb) modules may be used.

1876

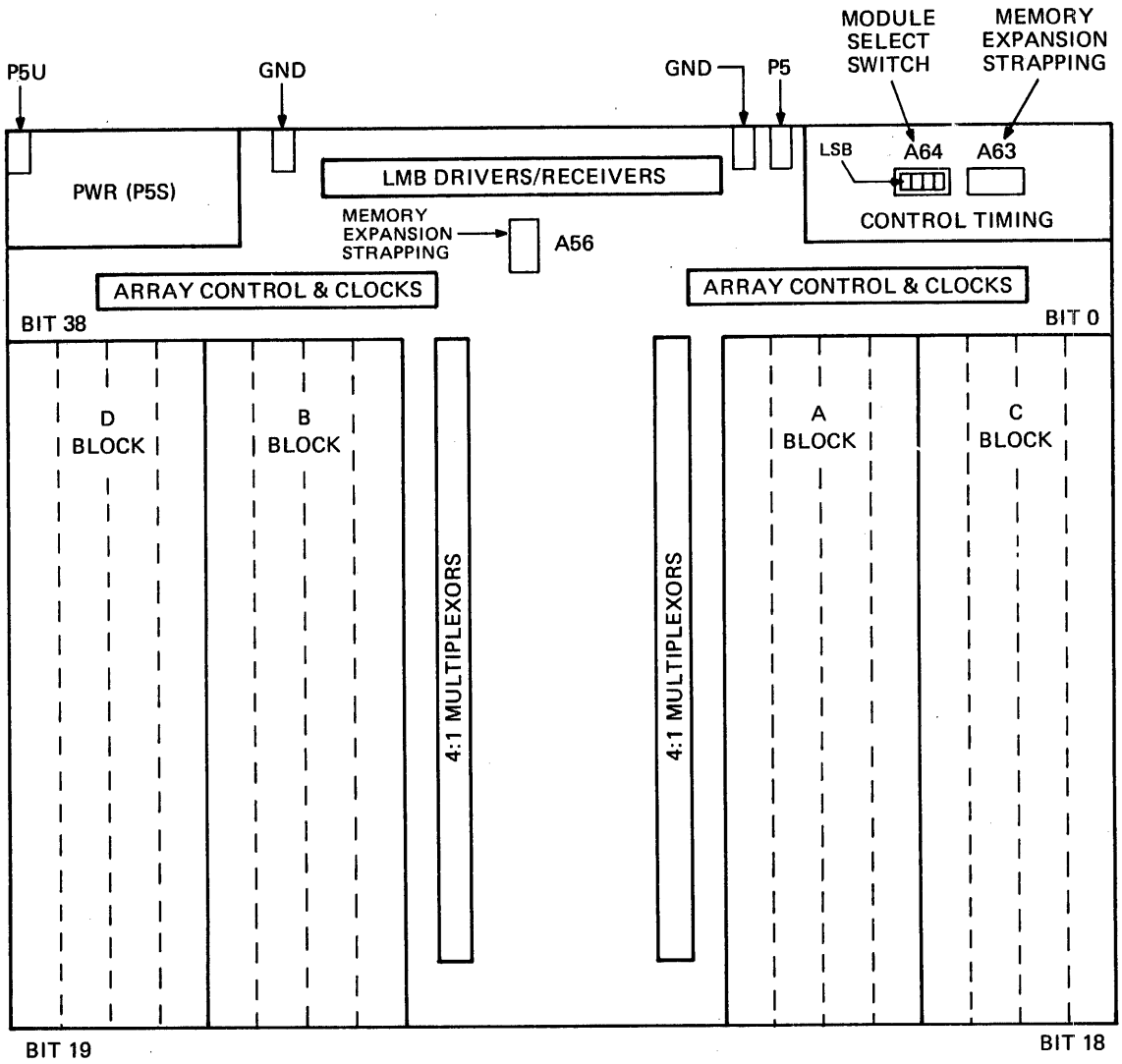
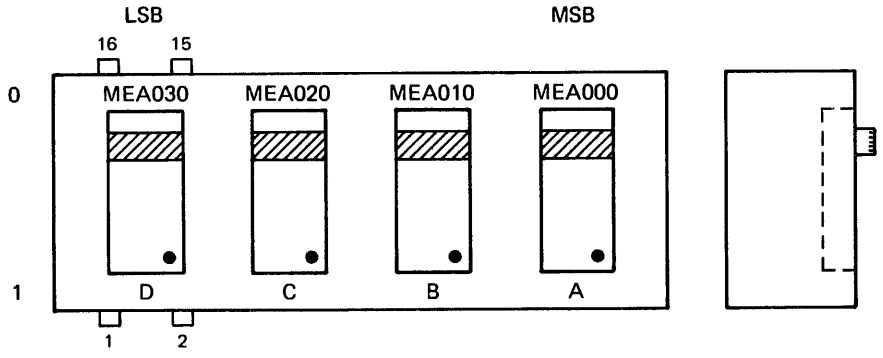


Figure 14-1 2.0 Mb STM Component Block Layout

1710-1



NOTE

SWITCH POSITION IS CLOSED ON THE SIDE ON WHICH THE DOT APPEARS.

Figure 14-2 Module Selection Switches

TABLE 14-2 MEMORY EXPANSION DECODE TABLE USING THE 4 MB 35-771 LBC (UP TO 4.096 MB - 4 MB MODE)

VARIATION	MEA030 Switch D	MEA020 Switch C	MEA010 Switch B	MEA000 Switch A	STM DECODED	STORAGE CAPACITY
F02	X	0	0	0	0	512 kb
	X	1	0	0	1	1,024 kb
	X	0	1	0	2	1,536 kb
	X	1	1	0	3	2,048 kb
	X	0	0	1	4	2,560 kb
	X	1	0	1	5	3,072 kb
	X	0	1	1	6	3,584 kb
	X	1	1	1	7	4,096 kb
F03	X	X	0	0	0	1,024 kb
	X	X	1	0	1	2,048 kb
	X	X	0	1	2	3,072 kb
	X	X	1	1	3	4,096 kb
F04	X	X	X	0	0	2,048 kb
	X	X	X	1	1	4,096 kb

NOTE

For STM strapping information, see Figure 14-4.

TABLE 14-3 MEMORY EXPANSION DECODE TABLE USING THE 8 MB 35-806 LBC (UP TO 8.192 MB - 8 MB MODE)

VARIATION	MEA030 Switch D	MEA020 Switch C	MEA010 Switch B	MEA000 Switch A	STM DECODED	STORAGE CAPACITY
F02	0	0	0	0	0	512 kb
	1	0	0	0	1	1,024 kb
	0	1	0	0	2	1,536 kb
	1	1	0	0	3	2,048 kb
	0	0	1	0	4	2,560 kb
	1	0	1	0	5	3,072 kb
	0	1	1	0	6	3,584 kb
	1	1	1	0	7	4,096 kb
	0	0	0	1	8	4,608 kb
	1	0	0	1	9	5,120 kb
	0	1	0	1	10	5,632 kb
	1	1	0	1	11	6,144 kb
	0	0	1	1	12	6,656 kb
	1	0	1	1	13	7,168 kb
	0	1	1	1	14	7,680 kb
	1	1	1	1	15	8,192 kb
F03	X	0	0	0	0	1,024 kb
	X	1	0	0	1	2,048 kb
	X	0	1	0	2	3,072 kb
	X	1	1	0	3	4,096 kb
	X	0	0	1	4	5,120 kb
	X	1	0	1	5	6,144 kb
	X	0	1	1	6	7,168 kb
	X	1	1	1	7	8,192 kb
F04	X	X	0	0	0	2,048 kb
	X	X	1	0	1	4,096 kb
	X	X	0	1	2	6,144 kb
	X	X	1	1	3	8,192 kb

NOTE

For STM strapping information, see Figure 14-4.

TABLE 14-4 MEMORY EXPANSION DECODE TABLE USING THE 8 MB 35-806 LBC (FOR MEMORY CAPACITY EXCEEDING 8.192 MB AND UP TO 16.384 MB) (16 MB MODE)

VARIATION	MEA030	MEA020	MEA010	MEA000	STM DECODED	STORAGE CAPACITY
F03 *	0	0	0	0	0	1,024 kb
	1	0	0	0	1	2,048 kb
	0	1	0	0	2	3,072 kb
	1	1	0	0	3	4,096 kb
	0	0	1	0	4	5,120 kb
	1	0	1	0	5	6,144 kb
	0	1	1	0	6	7,168 kb
	1	1	1	0	7	8,192 kb
	0	0	0	1	8	9,216 kb
	1	0	0	1	9	10,240 kb
	0	1	0	1	10	11,264 kb
	1	1	0	1	11	12,288 kb
	0	0	1	1	12	13,312 kb
	1	0	1	1	13	14,336 kb
	0	1	1	1	14	15,360 kb
	1	1	1	1	15	16,384 kb
F04 *	X	0	0	0	0	2,048 kb
	X	1	0	0	1	4,096 kb
	X	0	1	0	2	6,144 kb
	X	1	1	0	3	8,192 kb
	X	0	0	1	4	10,240 kb
	X	1	0	1	5	12,288 kb
	X	0	1	1	6	14,336 kb
	X	1	1	1	7	16,384 kb

NOTE

For STM strapping information, see Figure 14-4.

14.1.2 Memory Cycle Start/End

The memory cycle is initiated by the negative-going edge of Memory Cycle Initiate (MCI0) and is disabled by Memory Cycle Complete (MCC0), terminating all memory operations. This block also initiates timing for the row and column address strobes.

14.1.3 LMB Description

14.1.3.1 LMB 001:381

LMB lines 001:381 carry the address, read/write data, to and from memory. During the address time, LMB lines 001:131 carry the row and column address to the RAMs. During the read/write time, LMB lines 001:381 carry the RAM data. Table 14-5 lists the function of each bus line.

TABLE 14-5 BUS LINE FUNCTIONS

1885

LMB	R/W MODE ADDRESS	NAME	REFRESH MODE ADDRESS	R/W DATA
001	Row Add	A0	Ref Address	Data Bit 0
011	Row Add	A1	Ref Address	1
021	Row Add	A2	Ref Address	2
031	Row Add	A3	Ref Address	3
041	Row Add	A4	Ref Address	4
051	Row Add	A5	Ref Address	5
061	Row Add	A6	Ref Address	6
071	Column Add	A7		7
081	Column Add	A8		8
091	Column Add	A9		9
101	Column Add	A10		10
111	Column Add	A11		11
121	Column Add	A12		12
131	Column Add	A13		13
141	Chip Row Access (MS)	A14		14
151	Chip Row Access (LS)	A15		15
161	Quad Word Enable	QWE0		16
171	Data			17
181	↓			18
191				19
201				20
211				21
221				22
231				23
241				24
251				25
261				26
271				27
281				28
291				29
301				30
311	↓			31
321	Check Bits			Check Bit 00
331	↓			01
341				02
351				03
361				04
371				05
381	↓			06

14.1.3.2 LMB 001:061

During the address time of the bus function, LMB lines 0:6 latch the address of one of the 128-cell rows within each RAM chip in the array.

14.1.3.3 LMB 071:131

During address time of the bus function, LMB lines 071:131 latch the address of one of the 128-cell columns within each RAM chip in the array.

14.1.3.4 LMB 141:161

During the address time of the bus function, LMB lines 141:151 enable access to one of the 4-word rows in either the A or B array. LMB line 161, when low (inactive), enables access to all four rows (quadword) in either array.

14.1.4 I/O Transceiver

The I/O transceiver carries data to and from the array on 39 bidirectional lines. The transceiver is controlled by the mode control circuitry via the Data Out Enable (DOE0) and Data In Enable (DIE0) signals.

14.1.5 Mode Control

The mode control receives Memory Write Enable (MWE0) or Memory Read Enable (MRE0) signals from the LBC and generates Read, Data Out Enable (DOE), or Write, Data In Enable (DIE) signals to the I/O transceiver.

14.1.6 Memory Read Data Strobe

The Memory Read Data Strobe (MRDS0) signal indicates availability of the read data on the LMB lines.

14.1.7 Word Access Decoder

Lines MWA001:011 enable access to one of the 4-word rows in either the A or B array. These lines must agree with LMB lines 141:151.

14.1.8 Strobe Clock Drivers

The address drivers access the storage cell within the selected RAM chip. The Row Address Strobe (RAS) and Column Address Strobe (CAS) clock drivers facilitate the R/W operation of the selected word in either the A or B array.

14.1.9 RAM Chip Array

The RAM chip array is configured in a horseshoe arrangement as shown in Figure 14-3, with one inner 39-bit quadword labeled A array which is divided into two blocks: block A, which consists of bits 0:18, and block B, which has bits 19:38. A complementary outer 39-bit quadword labeled B array is also divided into two blocks: block C, consisting of bits 0:18, and block D, consisting of bits 19:38.

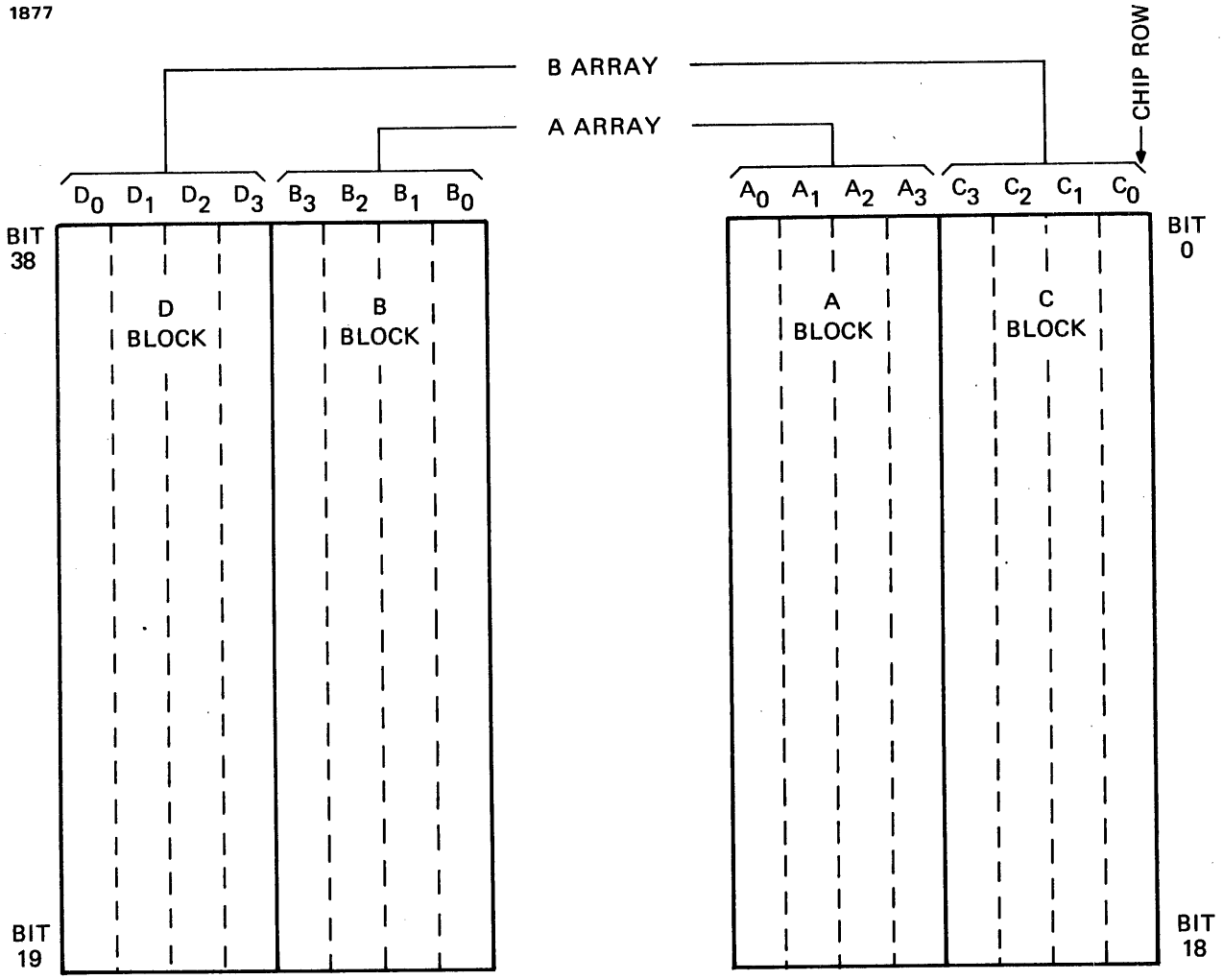


Figure 14-3 RAM Chip Array

14.2 STORAGE MODULE OPERATION

The module select switches and memory expansion straps enable selection of one of the possible 16 STMs. When a module is selected, a high level is generated on (MS1), Sheet 2 (H5). Figure 14-4 depicts module selection and contains tables listing memory expansion strapping.

14.2.1 Timing

14.2.1.1 Start of Memory Cycle

A memory cycle starts upon arrival of the negative-going edge of (MCI0) as shown in Figure 14-5. Noting that the module has been selected (MS1 is high), MCI0 clocks the memory busy flip-flop (A49) and generates (MB0), which latches the LMB lines 0:16 on the F02 version, as well as MEA020 and MEA030 on the F03 and F04 versions (3A4). Also generated by the memory busy flip-flop is MB1, which passes through a delay line (A62) and generates the row (RAS) and column (CAS) strobe timing, RAST1 and CAST1.

14.2.1.2 End of Memory Cycle

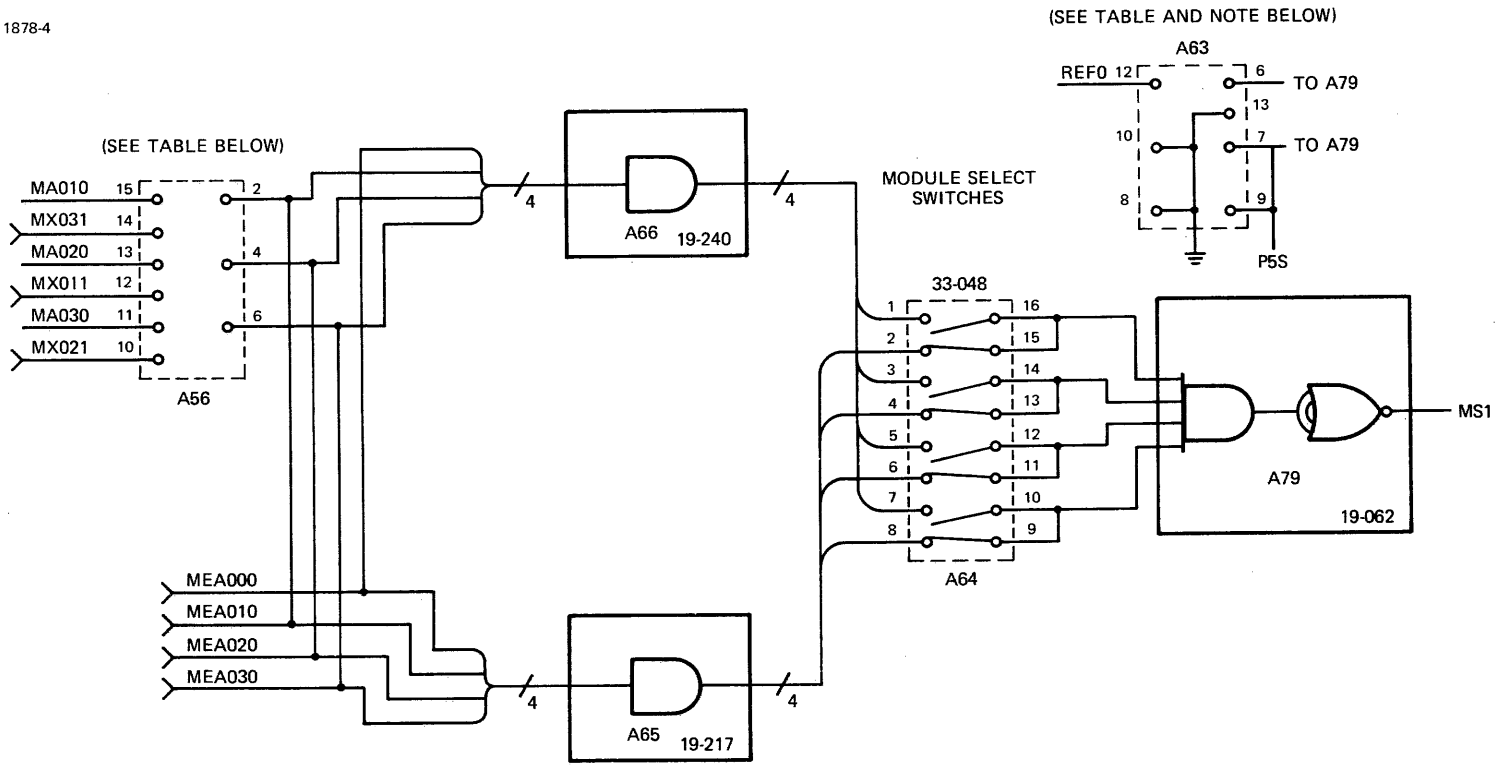
Every memory cycle ends on the low-going edge of the Memory Cycle Complete (MCC0). MCC0 resets the memory busy flip-flop which disables RAST1 and CAST1, thus completing the memory cycle.

14.2.1.3 Address Latches and Drivers

Upon arrival of MCI0, MB0 goes low and enables the address latches and expansion address (depending on the functional variation of the board) to latch in the row and column addresses (refer to Figure 14-6). LMB lines 141:151 (3A7), which select one of the 4-chip (word) rows (0-3) if a single fullword is desired, are also strobed. During the address time, LMB line 161 determines if a quadword is desired. If low, all four rows (words) in the array are enabled, and lines LMB 141:151 are ignored. When the row and column address are propagated through the driving circuitry, the single memory cell in the row or rows is selected.

14.2.1.4 RAS Drivers

The leading edge of MCI0 clocks the Memory Busy flip-flop (A49). MB1 is then passed through a delay line and also propagated through complementary AND gates (A50, A51), which generate RAS timing for both A and B arrays (RASTA1, RASTB1). (Refer to Figure 14-5.) The RAS timing strobes are then propagated through the word row decoding circuitry with the selected word row or rows depending upon the state of A141, A151, and QWE0 at location 3A9. The output of the RAS drivers enables the selected rows of RAMs. All RAS drivers are selected simultaneously during a refresh cycle.



MODULE SELECT

A56 LOCATION

4 MB MODE (35-771 LBC)				
F02	.512 MB	6-11		
F03	1.0 MB	14-11	10-13	
F04	2.0 MB	14-11	10-13	2-15

8 MB MODE (35-806 LBC)				
F02	.512 MB	12-11		
F03	1.0 MB	14-11	10-13	
F04	2.0 MB	14-11	10-13	4-15

16 MB MODE (35-806 LBC)				
F03	1.0 MB	14-11	10-13	
F04	2.0 MB	14-11	10-13	6-15

NOTE: STRAPPING OPTIONS ARE NECESSARY FOR F02, F03, AND F04 VARIATIONS.

A63 LOCATION

4 MB MODE (35-771 LBC)					
F02	.512 MB	12-6	8-9	11-14	
F03	1.0 MB	12-6	10-7	8-9	
F04	2.0 MB	8-9	10-7	6-13	11-5

8MB MODE (35-806 LBC)					
F02	.512 MB	12-6		11-14	
F03	1.0 MB	12-6		8-9	
F04	2.0 MB	8-9	10-7	12-6	11-5

16 MB MODE (35-806 LBC)				
F03	1.0 MB	12-6		
F04	2.0 MB	12-6	8-9	11-5

Figure 14-4 Module Select Circuit

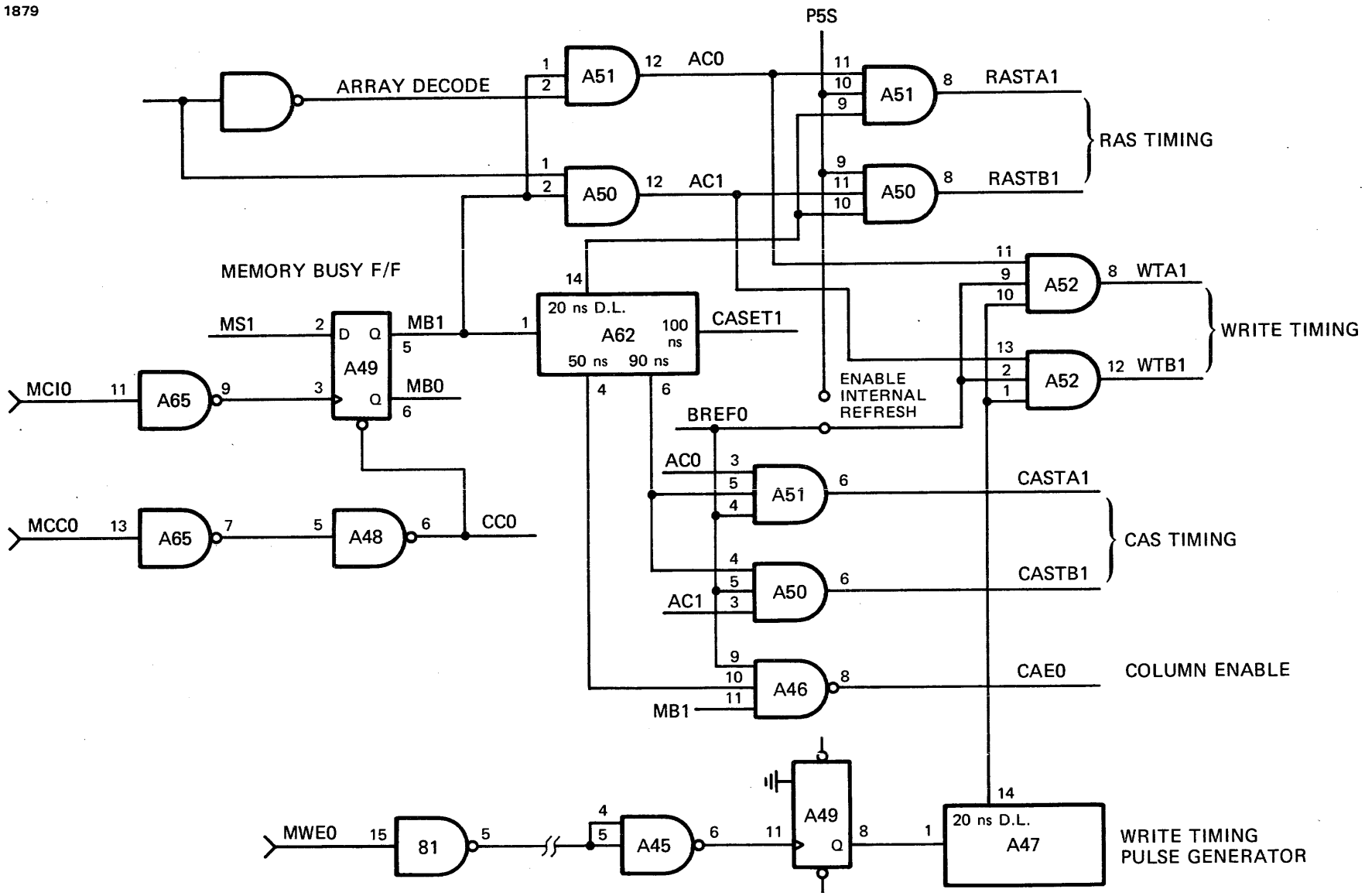


Figure 14-5 Timing Control

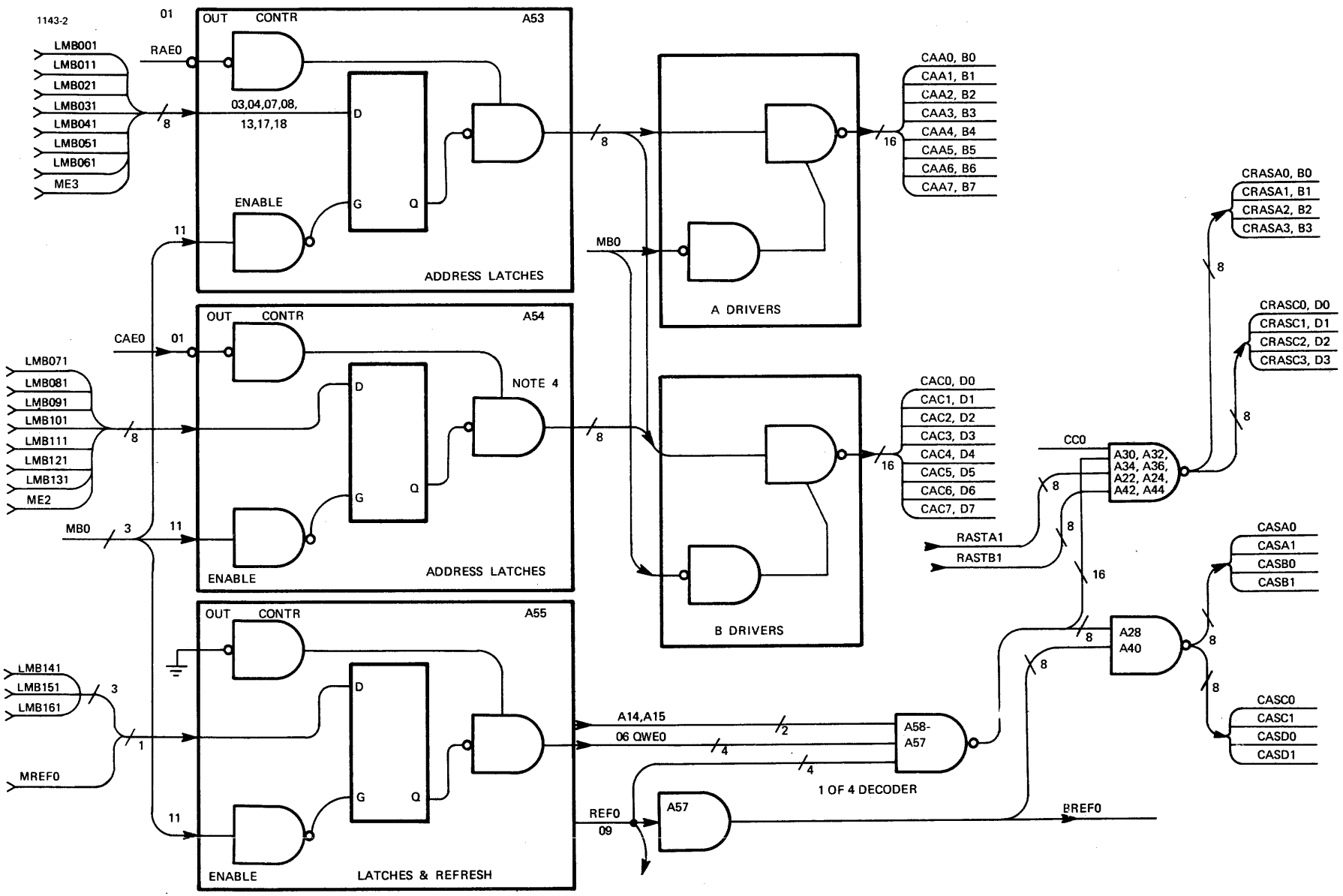


Figure 14-6 Address Latches and Decoder

14.2.1.5 Memory Word Access Decode

Refer to Table 14-6 during this discussion. The Memory Word Access (MWA001:011) lines are similar in function to LMB lines 141:151, which are discussed in the section on address latches and drivers. The lines in the decoder provide access to one of the 4-word rows in the A or B array. The MWA lines generate (WA0) and (WA1). These lines are used to steer the RAST1 and WT1 decoding to one of the 4-word rows during the Read-Modify-Write operation. (Refer to Figure 14-7.)

TABLE 14-6 BLOCK AND ROW DECODE TABLE

	LMB				BLOCK	ROW
	141	151	MEA030	MEA010	DECODED	DECODED
F02	0	0	0	X	C/D	0
	0	1	0	X		1
	1	0	0	X		2
	1	1	0	X		3
	0	0	1	X	A/B	0
	0	1	1	X		1
	1	0	1	X		2
	1	1	1	X		3
F03	0	0	X	X	A/B	0
	0	1	X	X		1
	1	0	X	X		2
	1	1	X	X		3
F04	0	0	X	0	C/D	0
	0	1	X	0		1
	1	0	X	0		2
	1	1	X	0		3
	0	0	X	1	A/B	0
	0	1	X	1		1
	1	0	X	1		2
	1	1	X	1		3

Note: Zero indicates low level (<.8 V at connector).

14.2.1.6 Write Clock Drivers

The MWA lines are used to steer the write timing pulse WTA1 and WTB1 for selection of the appropriate word row to be written into. The word row is selected by the decoding of these strobes and by word select lines WA0 and WA1 and their inverse, which generate a low (active) pulse on the selected CWE line. (Refer to Figure 14-8.)

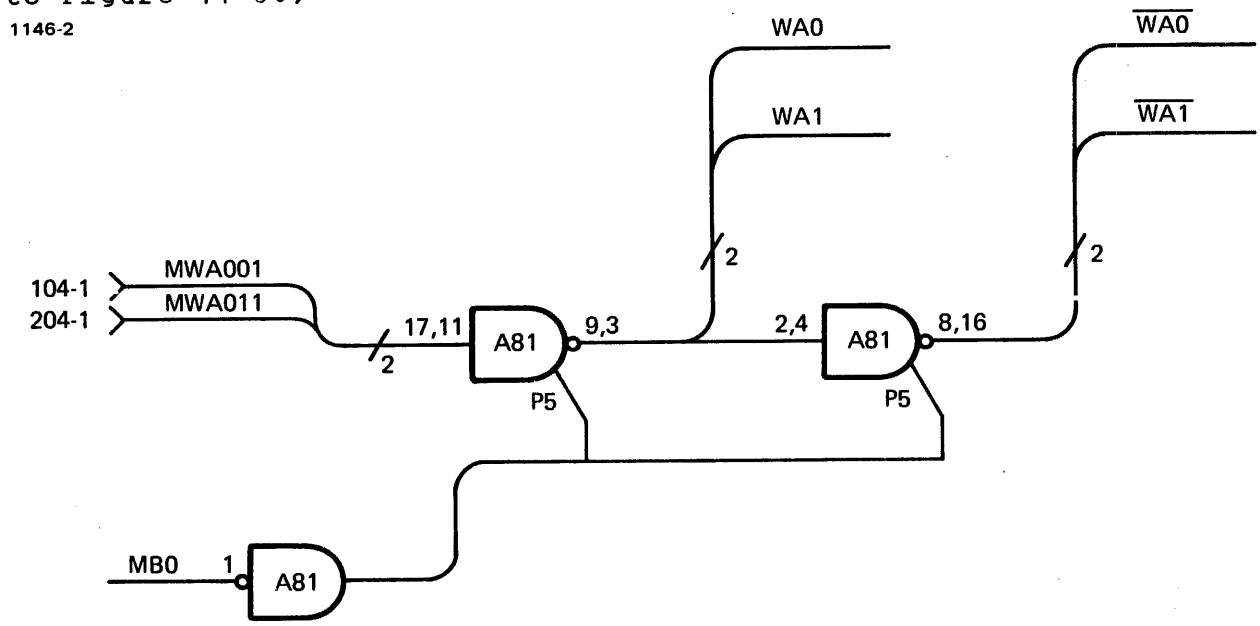


Figure 14-7 Word Access Decode

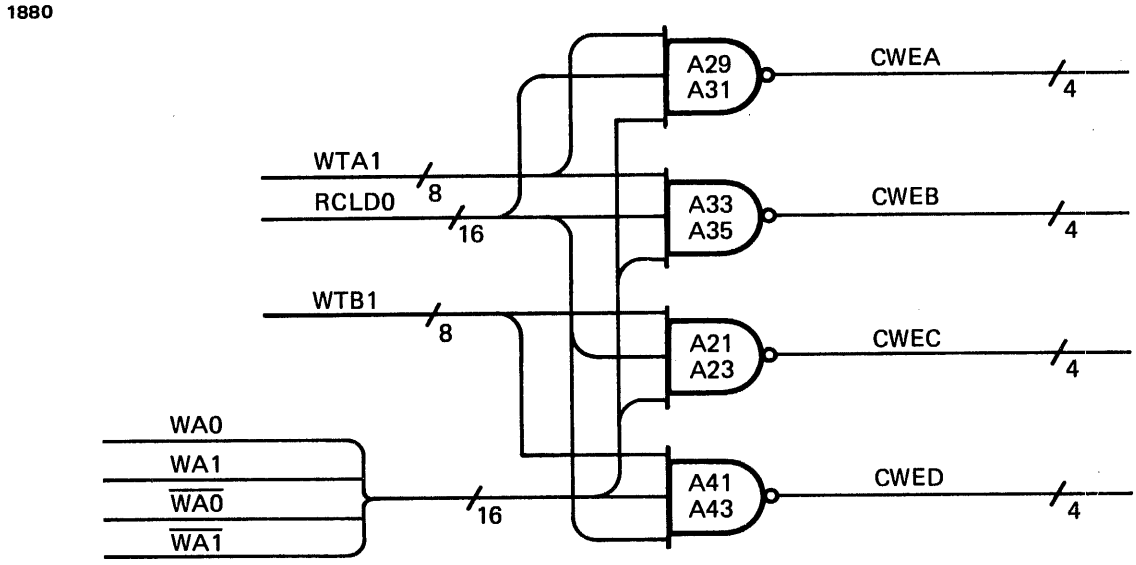


Figure 14-8 Write Clock Drivers

14.2.1.7 Write Mode

A write to memory occurs upon arrival of Memory Write Enable (MWE0) going low (active). The output generates a high (inactive) level on the output of A66, Pin 7 (RE0). This signal disables the 4:1 multiplexors and thus enables the write data to be placed onto the internal bidirectional data bus. The Data Input Enable (DIE0) going low (active) activates I/O receivers which place the write data into the RAM chip's D input, as shown in Figure 14-9. Simultaneously, the Write Timing flip-flop (A49) is clocked and, along with single-shot pulse generator (A47), produces Write Timing Pulse WTA1 or WTB1. (Refer to Figure 14-6.) The presence of Chip Write Enable (CWE) (4B1) at both A and B arrays stores the data into the RAM location determined by LMB lines 001:131 during the address time. Figure 14-10 shows the timing during a write operation.

14.2.1.8 Read Mode

A read from memory occurs when the selected STM receives Memory Read Enable (MRE0). This low-active signal generates the signal Data Cut Enable (DOE0). Since MWE0 is high (inactive) during this time, as shown in Figure 14-11, RE0 is low (active). This enables the 4:1 multiplexors to receive data from the RAMs. In addition, DOE0 is propagated through a delay (typically 12 ns) to an input of NAND gate A81 and is coupled with a delayed (typically 100 ns) CASET1 to generate a Memory Read Data Strobe (MRDS0) signal. (Refer to Figure 14-12.) The MWA lines then select one of four channels of the multiplexor which places the read data onto the internal bidirectional bus. The first MRDS0 (first word in the quadword mode) is delayed by CASET1 and delay line A77 (typically 100 ns), to insure proper setup and access time of the RAM data. The second, third, and fourth MRDS0s (in quadmode operation) are delayed by the RC circuit and propagation delay of the gates between A81, pin 8 (DOE0) and A81, pin 14 (MRDS0) (typically 20 ns).

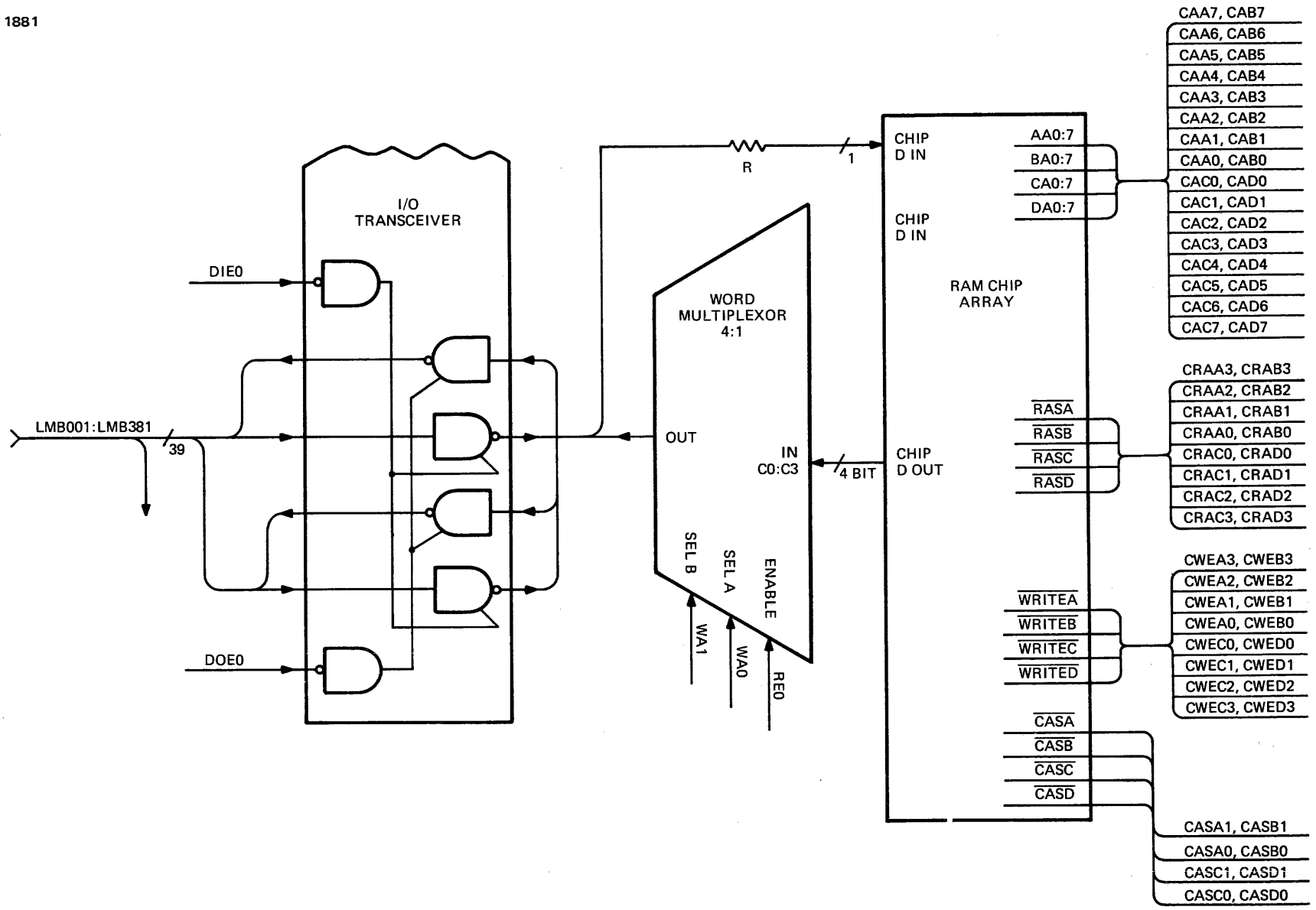


Figure 14-9 Data Input/Output

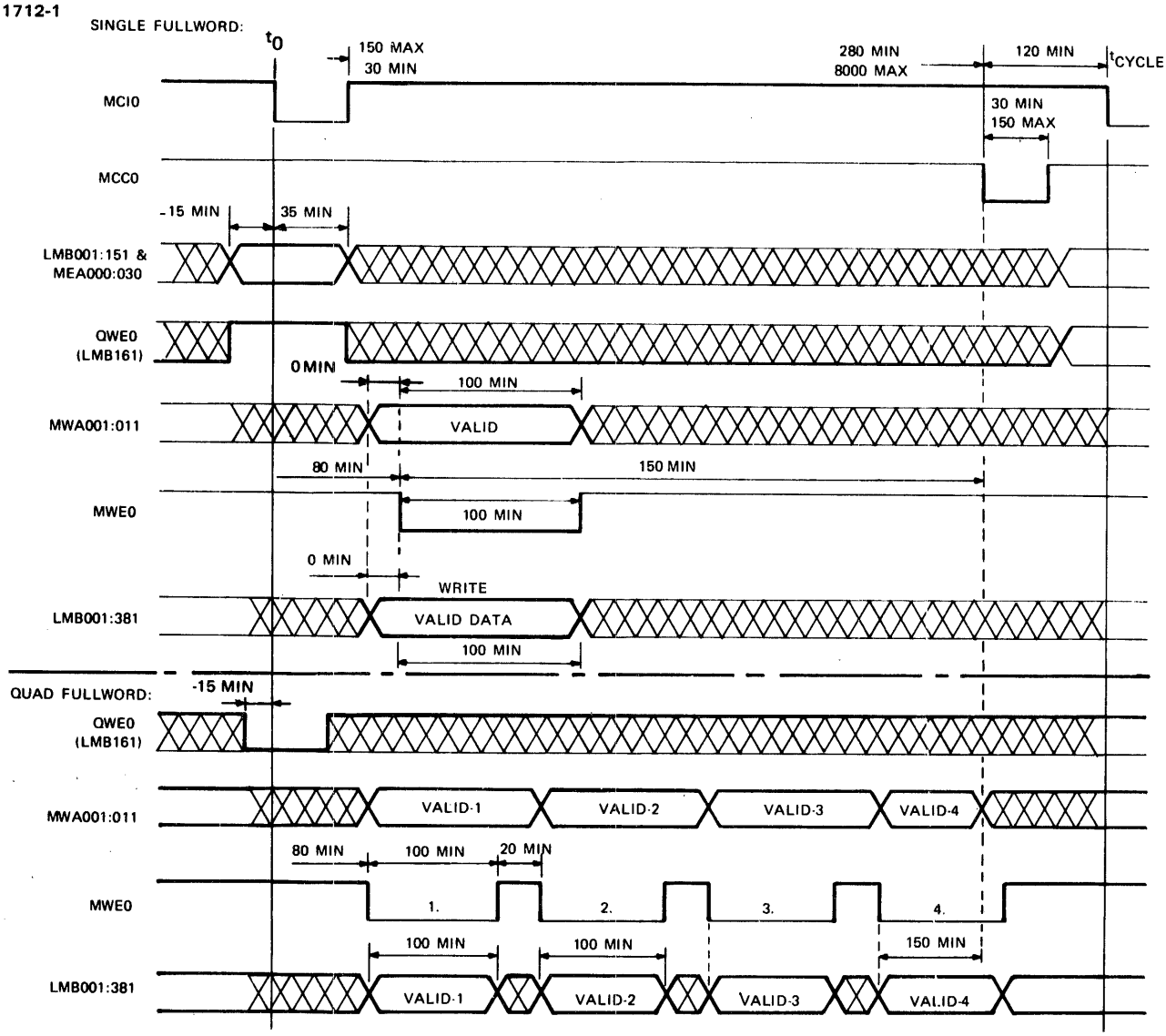


Figure 14-10 STM Write Mode Timing Diagram

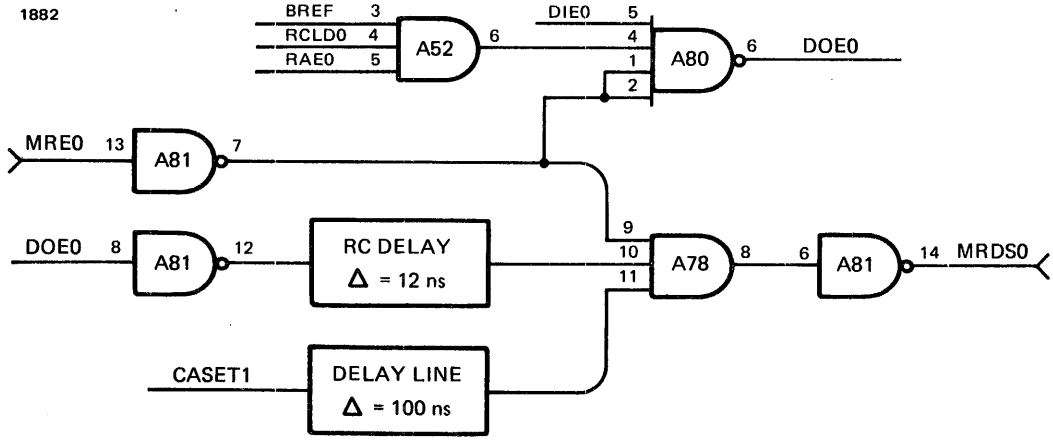


Figure 14-11 Read Control

1713-1

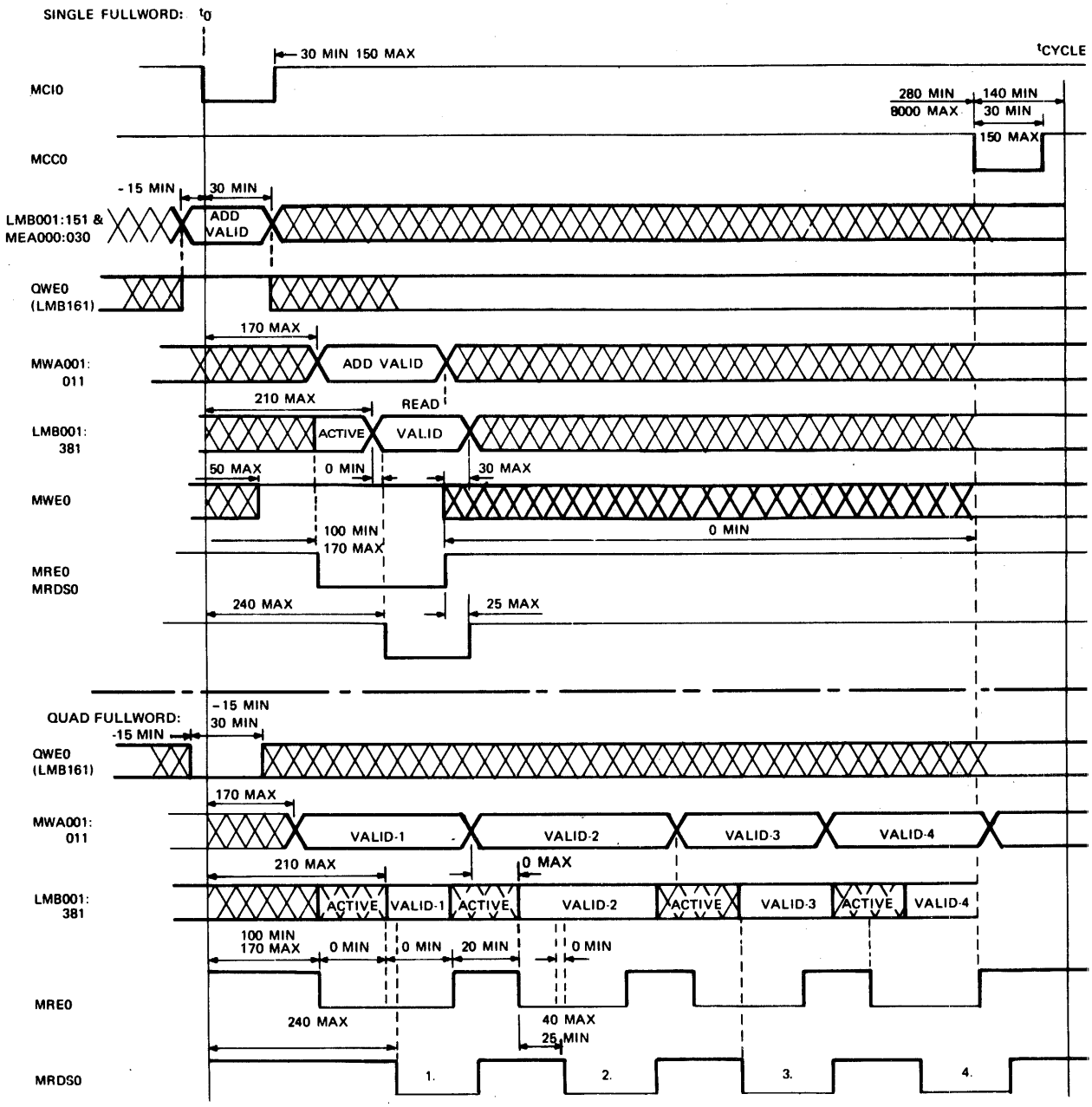


Figure 14-12 STM Read Mode Timing Diagram

14.2.1.9 Refresh

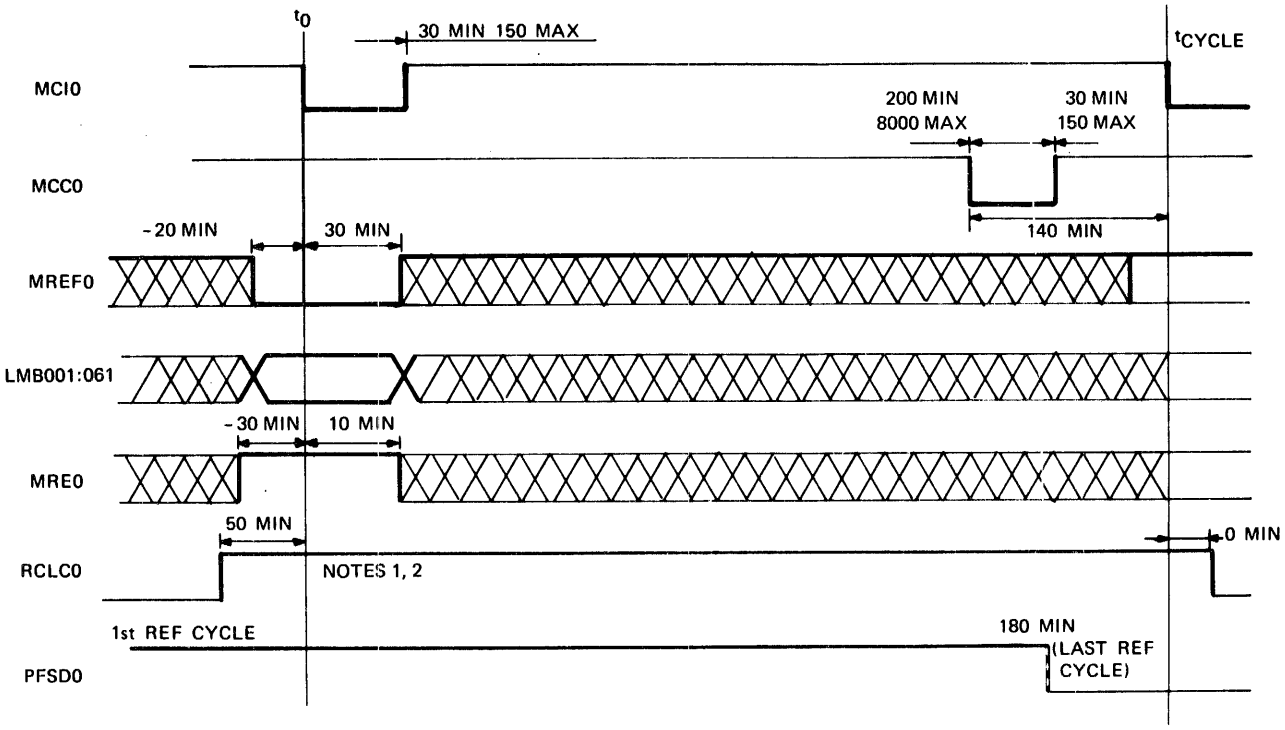
The dynamic nature of the RAM chips requires periodic refreshment of stored data every 2.0 ms. (Refer to Figure 14-13.) Refresh is accomplished when the STM receives the MREF0 signal. This signal sets the STM into the refresh mode, prevents write operations, and enables all RAS drivers to produce RAS clock to all RAMs.

Refresh (row) address lines are latched by arrival of MCI0 and clocked by RAS into the RAMs. The STM operates in two refresh modes: cycle steal mode, and burst (battery backup) mode.

Cycle steal - 128 refresh cycles are generated every 2 ms in between read or write operations.

Burst (battery backup) - 128 refresh cycles are generated in one burst every 2 ms. In between the bursts, the P5S is shut down, thus reducing the current drain on P5U which is battery backed up.

1715-1



NOTES

1. APPLICABLE IN THE BURST REFRESH MODE ONLY

2. THE RISE AND FALL TIME OF RCLC0 IS LESS THAN 100 ns (.8 V TO 2.4 V).

Figure 14-13 STM Refresh Mode Timing Diagram

14.2.2 Power Supply

14.2.2.1 Introduction

The 3230 STM uses two +5.0 V supplies: P5 and P5U. P5 powers the nonrefresh circuitry. P5U (which is a separate uninterrupted +5.0 V supply) is used to supply the RAM chips and refresh-related circuitry. P5U must be maintained to ensure valid memory. Another source derived from P5U is P5S (switched). The P5S is generated via an on-board PNP transistor switch controlled by PFSD0. P5S powers refresh control circuitry which is pulsed every 2 ms during battery backup operation.

14.2.2.2 P5S Power-Down

A P5S power-down sequence starts upon arrival of PFSD0 going low (active). This sets comparator A61, pin 10 high which is compared to pin 11 (which maintains a 2.4 V level during normal operation). Since A61, pin 10 is higher than pin 11, pin 13 of A61 goes low, turning off the PNP transistor switch and thereby causing P5S to discharge eventually to ground. As P5S discharges below 4.8 V, A61, pin 14 goes low activating MCLC0, CC0, and RCLD0 to prevent an accidental write operation into RAMs. Low RCLC0 indicates to the controller (LBC) that the STM is in the low-power mode.

14.2.2.3 P5S Power-Up

P5S power-up is accomplished following the release of PFSD0=1 (inactive). PFSD0 going high turns on the PNP transistor switch which raises P5S to P5U level. Once P5S reaches approximately 4.8 V, A61, pin 14 goes high releasing RCLC0, CC0, and RCLD0. This signifies to the controller that the STM is ready to accept refresh cycles.

14.3 MNEMONICS

The following is a list of the mnemonics on the STM board. The meaning and the 35-764D08 schematic location of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
BREF0	Buffered refresh	2E1
BSCLR0	Buffered systems clear	16B5
CA"A":CA"D"	Chip address lines (A-D)	3G1-9
CAE0	Column address enable	2M4
CAS"A":CAS"D"	Column address strobe	3M5-9
CASTA1:CASTB1	Column address strobe timing	2M4
CRAA0:CRAD0	Row address strobe	3K1-9
CWEA:D	Chip write enable	4D1-9

MNEMONIC	MEANING	SCHEMATIC LOCATION
DIE0	Data in enable	2M7
DOE0	Data out enable	2M8
LMB001:061	Local memory bus (row address and data lines)	3A2
LMB071:131	Local memory bus (column address and data lines)	3A5
LMB141:151	Local memory bus (word row selection and data lines)	3A7
LMB161	Local memory bus (single/quad select and data line)	3A7
LMB171:381	Local memory bus (data lines)	6E7
MB0	Memory busy	2D3
MCC0	Memory cycle complete	2A3
MCI0	Memory cycle initialize	2A3
MEA00:30	Memory expansion address	2B7
MRDS0	Memory read data strobe	2M8
MRE0	Memory read enable	2E7
MREF0	Memory refresh	3A7
MS1	Module select	2H5
MWA001:011	Memory word access	2B9
MWE0	Memory write enable	2E7
MX031:011	Memory super expansion address	2A5
P5	+5 V supply	16A8
P5S	+5 V switched supply (internal)	16M7
P5U	+5 V uninterruptible supply	16L6
PFSD0	P5S shutdown	16B6
RAE0	Row address enable	2F4
RAST1	Row address strobe timing	2M2
RCLC0:D0	Refresh clear	16J5
RE0	Read enable	2J6
REF0	Refresh	3C7
WA0, WA1	Word access select lines	2C9
WT1	Write timing	2N3

CHAPTER 15
ADJUSTMENTS

15.1 INTRODUCTION

This section provides the adjustments for the EDMA Protocol Logic, EDMA control oscillator, and the High Performance Floating-Point Processor (HPFPP). The CPU clocks are derived from a crystal oscillator and require no adjustments.

15.2 EDMA PROTOCOL LOGIC OSCILLATOR ADJUSTMENT

These oscillators are set at the factory and usually do not require further adjustments. If adjustments are necessary, however, the following procedure should be followed (refer to Sheet 6 of Functional Schematic 35-770D08):

1. Turn processor power off.
2. Connect 04H09 to ground.
3. Connect 04B11 to ground.
4. Connect 04B04 to ground.
5. Turn processor power on.
6. With scope probe on QUE0 (04R08), adjust capacitor 02A (80-02) for a 60 to 65 nanoseconds pulse width of QUE0.
7. Attach another scope probe on SOT0 (04R11). Adjust capacitor 04A (02-80) for 270 to 280 nanoseconds from falling edge of QUE0 to falling edge of SOT0.

15.3 LOCAL MEMORY TO EDMA CONTROL OSCILLATOR ADJUSTMENT

Perform the following steps (refer to Sheet 5 of Functional Schematic 35-770D08):

1. Turn power off.
2. Connect 01A01 to ground.
3. Connect 01A04 to ground.
4. Turn power on.
5. Adjust capacitor 00A (80-02) for FDA1 to be a square wave period of 480 microseconds.

NOTE

If the waveform appears unstable, readjust the capacitor to a different position.

15.4 CLOCK ADJUSTMENTS FOR THE HPFPP

Refer to the High Performance Floating-Point Processor Installation and Maintenance Manual, Publication Number 29-705, while performing the following steps:

1. Turn CPU power off and remove the HPFPP.
2. Install an M80 Extender Board (28-015) in slot 6 of the processor chassis.
3. Install the HPFPP in the M80 Extender Board with the HPFPP-A Board on top.
4. Connect a scope probe to TP1 (100-2 on HPFPP-A) ACLK1A and adjust the scope time base for 20 nanoseconds/division. (Refer to Functional Schematic 35-715D08, Sheet 4, Location M7.)
5. Select nominal clocks by setting the dip switches in location 16A on the HPFPP-A to the following positions:

SWITCH #	POSITION	SWITCH #	POSITION
1	OFF	5	OFF
2	ON	6	OFF
3	OFF	7	ON
4	OFF	8	OFF

6. Turn CPU power on and momentarily ground pin 5 of the IC at 16B (HPFPP-A).

NOTE

Grounding 16B05 forces the HPFPP oscillator into a free-running condition which can be halted only by an initialize or power down.

7. Set the HPFPP clocks to nominal by adjusting the trimmer capacitor at location 14B on the HPFPP-A Board. Nominal clocks are:

   ACLK1A (TP-1) = 100 nanoseconds (rise edge to rise edge at 1.5 V levels)

8. Turn CPU power off and remove HPFPP from the extender board.

9. Remove extender board from the processor chassis.

10. Install the HPFPP-B Board in slot 6 and the HPFPP-A board in slot 5 of the processor chassis. Install the two 50-conductor cables between connectors 3 and 4 of the HPFPP-A and -B Boards.

CHAPTER 16
02-663 TEST AID

16.1 INTRODUCTION

The 02-663 Test Aid is a compact, durable, and simple-to-use test fixture. It provides the necessary control to display the B, S, and ROM DATA (RD) buses of the processor, as well as the Control Store Address (CSA), four processor flags, Instruction Register (IR), and I/O attention lines (INT).

This chapter covers the operation, installation, and maintenance of the Test Display.

16.2 GENERAL DESCRIPTION

The 02-663 Test Aid consists of two printed circuit board assemblies, one of which is attached to the processor boards by two front cables. The other board is connected to the backpanel on one of the processor board positions and cabled to the first board by a single flat ribbon cable. Figure 16-1 shows the connections to the processor.

Figures 16-2 and 16-3 show the switch, displays, and cable connections of the test display.

The numbered parts illustrated in Figures 16-2 and 16-3 have the following functions:

1. Cable to CPU-B board connector 4, slot 05
2. Cable to CPU-A board connector 3, slot 04
3. Cable to Test Aid multiplexor
4. Control store address display
5. Display for selected bus
6. Bus selection switch
7. Flag register display
8. Cable from Test Aid multiplexor to display box
9. Connector to mate at location 0, slot 04
10. Connector to mate at location 1, slot 04

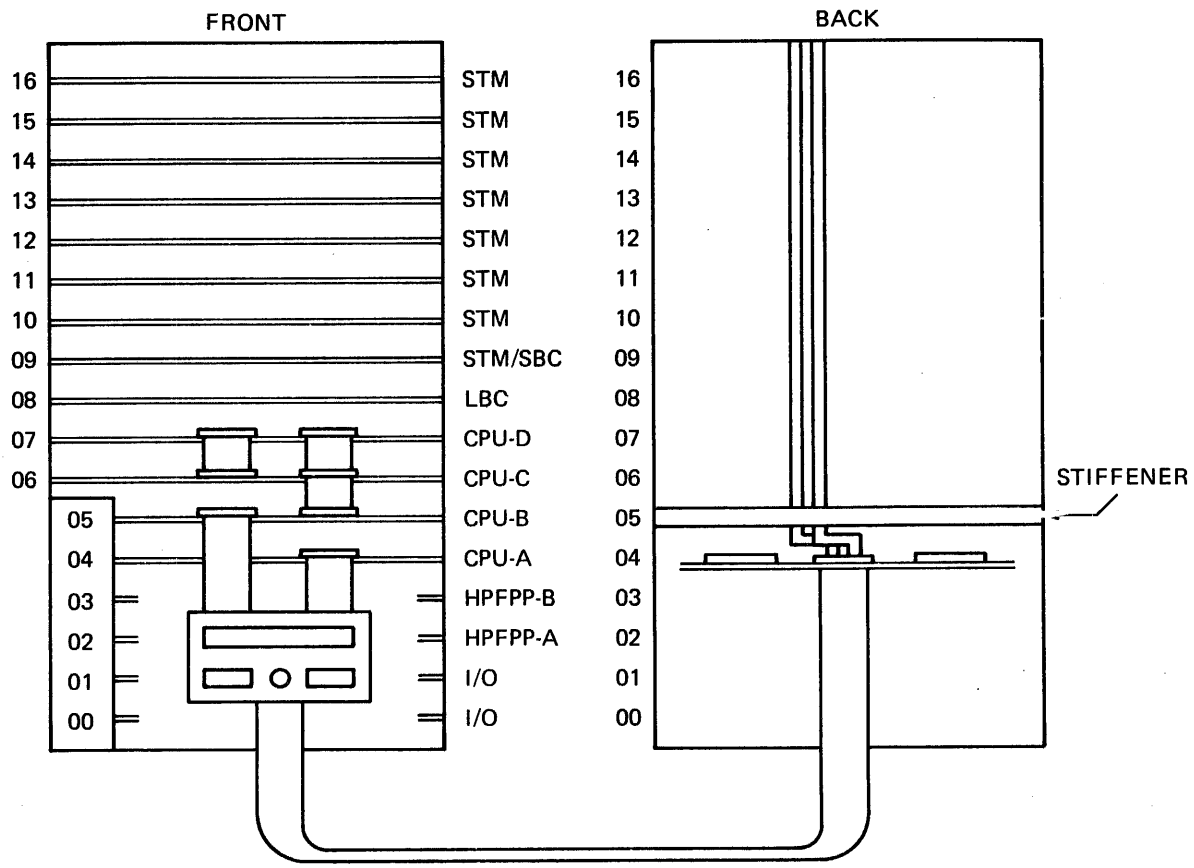


Figure 16-1 Test Aid Connections to Processor

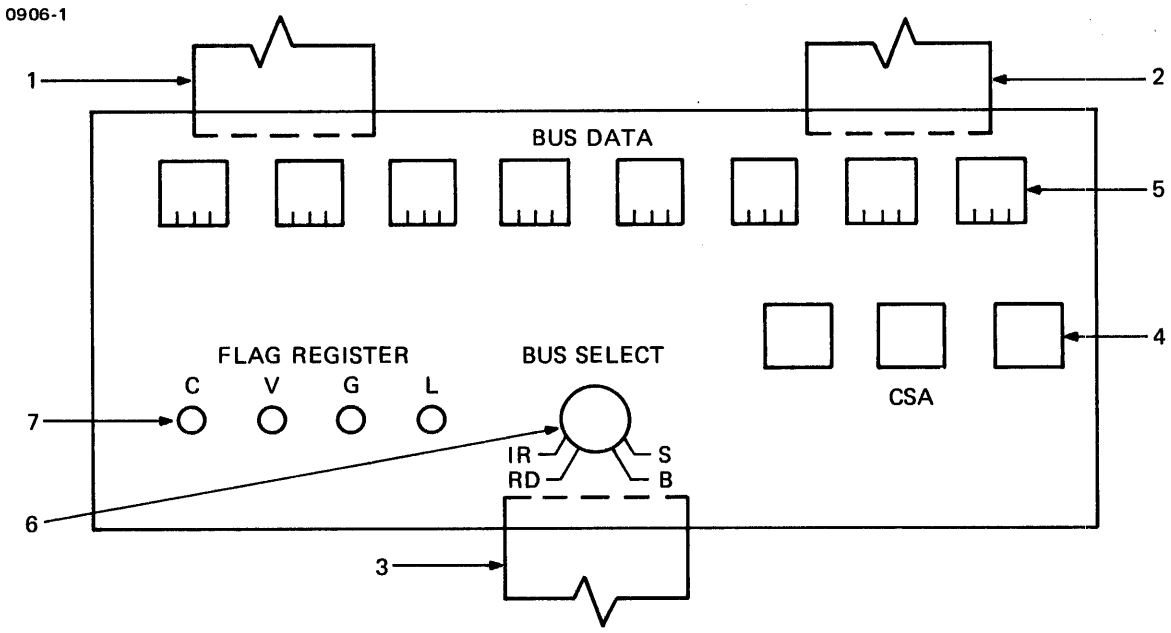


Figure 16-2 Display Box

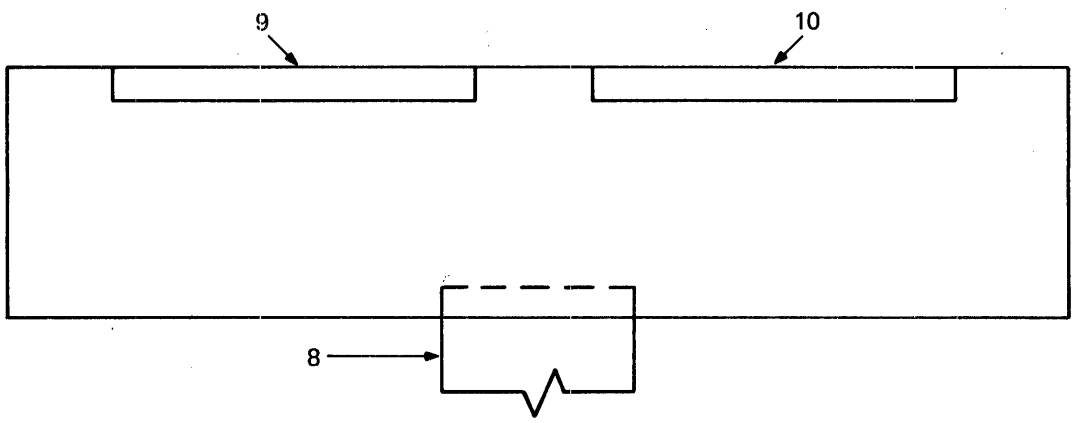


Figure 16-3 Test Aid Multiplexor Board

16.3 INSTALLATION AND OPERATION PROCEDURE

Install and operate the 02-663 Test Aid as follows:

1. Place the console power switch in the STANDBY position.
2. Install cable 1 (refer to Figure 16-2) on connector 4 of the CPU-B board, slot 05. (Refer to Figure 16-1.)
3. Install cable 2 (refer to Figure 16-2) on connector 3 of the CPU-A board, slot 04. (Refer to Figure 16-1.)
4. Put the Test Aid multiplexor on the backpanel CPU-A position, slot 04.
5. Connect the cable from the display box to the Test Aid multiplexor. The cable should lie flat with no twists.
6. Select the bus to be displayed, IR, B, S, or RD by switch 6 (refer to Figure 16-2).
7. Operate the system in the usual manner. The displays track the state of the buses.

16.4 POWER SUPPLY

Power is supplied to the Test Aid multiplexor directly from the backpanel. Power is supplied to the display board from the Test Aid multiplexor through the cable.

16.5 EXTENDER BOARD OPERATION

Cable 2 (refer to Figure 16-2) is provided with enough length for extender board operation.

16.6 TEST AID OPERATION

16.6.1 Test Aid Multiplexor

The Test Aid multiplexor buffers the flag register bits and sends them to the display board; it also corrects the logic levels of some signals and multiplexes the instruction register with I/O attention lines, B bus, and RCM Data Bus (RD Bus) data to the display board. The bus selection switch on the display board generates the two multiplexor control lines, IR0 and RD0, which steer the multiplexors as follows:

IR0	RD0	FUNCTION TO DISPLAY
Low	Low	Nct used
Low	High	IR bus with attention lines
High	Low	RD bus
High	High	B bus

NCTE

The RD bus does not display RD bits 6, 7, or 8. Bit 7 is SFTEN1 (Single-Precision Floating-Point Enable); bit 6 is DFTEN1 (Double Precision Floating-Point Enable); and bit 8 is tied to ground.

16.6.2 Display Board

The display board selects either the input from the backpanel board or the S bus data by a signal from the selector switch. It then displays the selected bus on the hexadecimal display. The control store address is also inverted and displayed on hexadecimal displays. The flag register bits are displayed on individual LEDs.

16.7 TEST AID DISPLAY

The 02-663 Test Aid uses the Model 8/32 test display printed circuit assembly. The following is a mnemonic cross reference between the 8/32 test display schematics provided (35-612D08) and the Test Aid multiplexor board.

TEST AID CONN PIN NO.	8/32	02-663
203-5	SAB1ENO	IRO
103-5	SAB2ENO	RDO
121-5	CCO	FLR280
221-5	VCCO	FLR290
120-5	GCCO	FLR200
220-5	LCCO	FLR310
216-3	CSAD040	CSAR200
116-3	CSAD050	CSAR210
218-3	CSAD060	CSAR220
117-3	CSAD070	CSAR230
219-3	CSAD080	CSAR240
118-3	CSAD090	CSAR250
220-3	CSAD100	CSAR260
120-3	CSAD110	CSAR270
222-3	CSAD120	CSAR280
121-3	CSAD130	CSAR290
223-3	CSAD140	CSAR300
122-3	CSAD150	CSAR310
119-5	SAB0	MXD001
219-5	SAB1	MXD011
118-5	SAB2	MXD021
218-5	SAB3	MXD031
117-5	SAB4	MXD041
217-5	SAB5	MXD051
116-5	SAB6	MXD061
216-5	SAB7	MXD071
115-5	SAB8	MXD081
215-5	SAB9	MXD091
114-5	SAB10	MXD101
214-5	SAB11	MXD111
113-5	SAB12	MXD121
213-5	SAB13	MXD131
112-5	SAB14	MXD141
212-5	SAB15	MXD151
111-5	SAB16	MXD161
211-5	SAB17	MXD171
110-5	SAB18	MXD181
210-5	SAB19	MXD191
109-5	SAB20	MXD201
209-5	SAB21	MXD211
108-5	SAB22	MXD221
208-5	SAB23	MXD231
107-5	SAB24	MXD241
207-5	SAB25	MXD251
106-5	SAB26	MXD261
206-5	SAB27	MXD271
105-5	SAB28	MXD281
205-5	SAB29	MXD291
104-5	SAB30	MXD301
204-5	SAB31	MXD311
204-4	CSD001	S001
105-4	CSD011	S011

TEST AID CONN PIN NO.	8/32	02-663
205-4	CSD021	S021
106-4	CSD031	S031
207-4	CSD041	S041
107-4	CSD051	S051
208-4	CSD061	S061
109-4	CSD071	S071
209-4	CSD081	S081
110-4	CSD091	S091
211-4	CSD101	S101
111-4	CSD111	S111
212-4	CSD121	S121
113-4	CSD131	S131
213-4	CSD141	S141
114-4	CSD151	S151
215-4	CSD161	S161
115-4	CSD171	S171
216-4	CSD181	S181
117-4	CSD191	S191
217-4	CSD201	S201
118-4	CSD211	S211
219-4	CSD221	S221
119-4	CSD231	S231
220-4	CSD241	S241
121-4	CSD251	S251
221-4	CSD261	S261
122-4	CSD271	S271
223-4	CSD281	S281
123-4	CSD291	S291
224-4	CSD301	S301
124-4	CSD311	S311

CHAPTER 17
HIGH SPEED DATA HANDLING OPTION

17.1 INTRODUCTION

The High Speed Data Handling Option upgrades the autodriver channel of the processor and adds two instructions to the user instruction repertoire. The autodriver channel calculation time for CRC-BISYNC is greatly reduced and error checking capability is increased to include the CRC-SDLC format. The two added instructions are: Process Byte (PB) and Process Byte Register (PBR). These provide the capability to perform error checking of characters or generation of check characters one data byte at a time. An error check can be calculated in any one of the three formats: LRC, CRC-BISYNC (also called CRC-16), or CRC-SDLC.

17.2 BLOCK DIAGRAM ANALYSIS

The D bus receivers shown in Figure 17-1 buffer direct the I/O bus data to the appropriate logic. The address logic determines if the High Speed Data Handling Option has been selected by the processor. The steering counter logic determines what type of data is being sent to the board and enables the appropriate register for loading. Three types of data can be sent to the board: format data, residual check character data, or the current data character tc be included in the residual check character. The format select register is set up by the format data from the processor. One of three formats can be selected: LRC, CRC-BISYNC, or CRC-SDLC. The current data character register contains the current data character for inclusion into the residual character. Table 17-1 contains the base numbers used to calculate the residual check character and is used to calculate CRC-BISYNC and CRC-SDLC. The table in use is selected by the format select logic. The check character buffer contains the residual check character and is updated with a new residual check character each time the current data character register is loaded. The D bus drivers gate data to the D bus when the processor attempts to read the check character buffer. The box active logic is part of the control logic that allows the board to accumulate an error check character. In the case of the 3221 processor operation, it captures the acknowledge interrupt signal when the check character buffer is read.

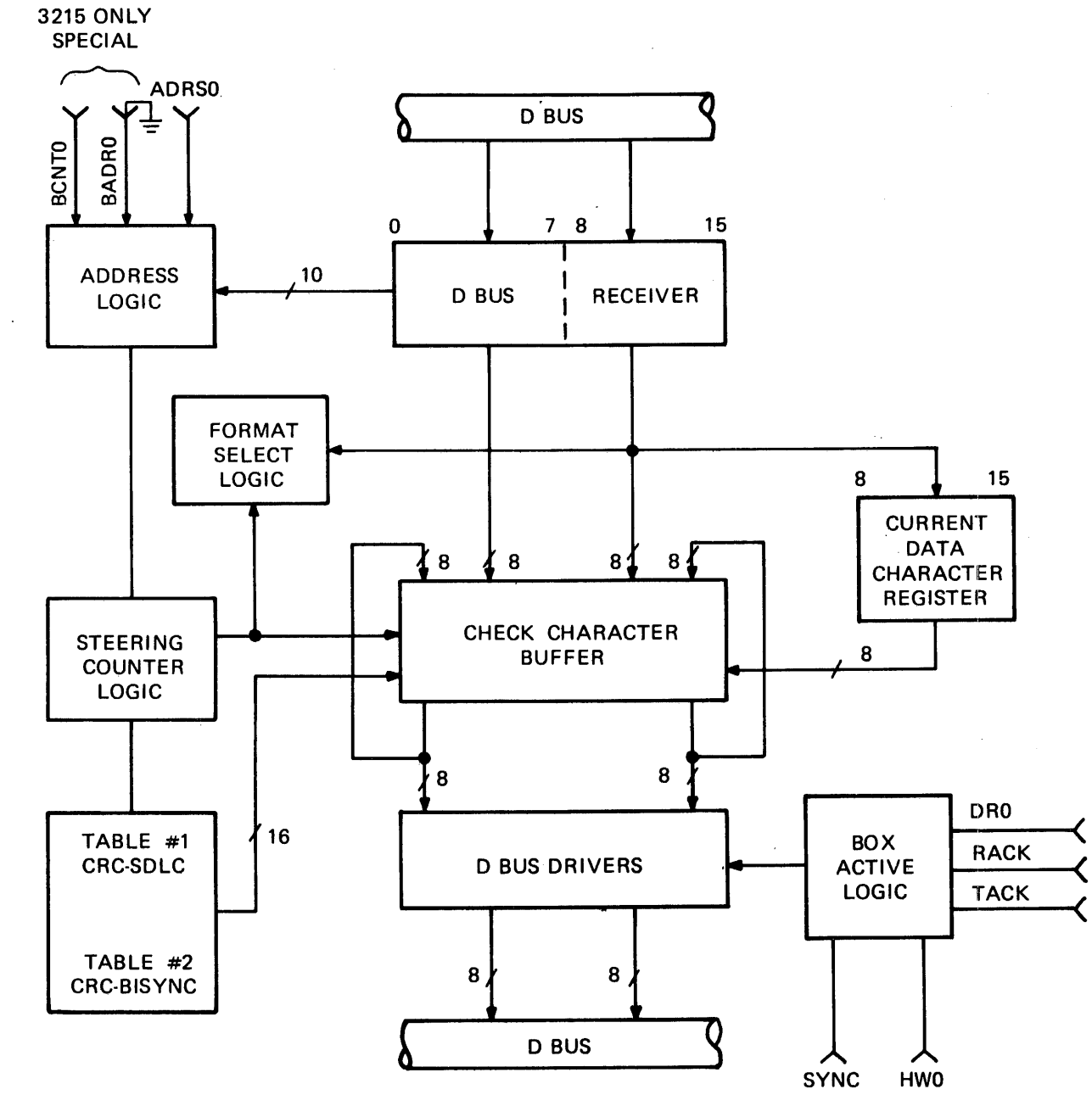


Figure 17-1 High Speed Data Handling Option Block Diagram

TABLE 17-1 DATA BASE TABLES

(a) Data for the CRC-BISYNC

00	0000	C0C1	C181	0140	C301	03C0	0280	C241
08	C601	06C0	0780	C741	0500	C5C1	C481	0440
10	CC01	0CC0	0D80	CD41	0F00	CFC1	CE81	0E40
18	0A00	CAC1	CB81	0B40	C901	09C0	0880	C841
20	D801	18C0	1980	D941	1B00	DBC1	DA81	1A40
28	1E00	DEC1	DF81	1F40	DD01	1DC0	1C80	DC41
30	1400	D4C1	D581	1540	D701	17C0	1680	D641
38	D201	12C0	1380	D341	1100	D1C1	D081	1040
40	F001	30C0	3180	F141	3300	F3C1	F281	3240
48	3600	F6C1	F781	3740	F501	35C0	3480	F441
50	3C00	FCC1	FD81	3D40	FF01	3FC0	3E80	FE41
58	FA01	3AC0	3B80	FB41	3900	F9C1	F881	3840
60	2800	E8C1	E981	2940	EB01	2BC0	2A80	EA41
68	EE01	2EC0	2F80	EF41	2D00	EDC1	EC81	2C40
70	E401	24C0	2580	E541	2700	E7C1	E681	2640
78	2200	E2C1	E381	2340	E101	21C0	2080	E041
80	A001	60C0	6180	A141	6300	A3C1	A281	6240
88	6600	A6C1	A781	6740	A501	65C0	6480	A441
90	6C00	ACC1	AD81	6D40	AF01	6FC0	6E80	AE41
98	AA01	6AC0	6B80	AB41	6900	A9C1	A881	6840
A0	7800	B8C1	B981	7940	BB01	7BC0	7A80	BA41
A8	BE01	7EC0	7F80	BF41	7D00	BDC1	BC81	7C40
B0	B401	74C0	7580	B541	7700	B7C1	B681	7640
B8	7200	B2C1	B381	7340	B101	71C0	7080	B041
C0	5000	90C1	9181	5140	9301	53C0	5280	9241
C8	9601	56C0	5780	9741	5500	95C1	9481	5440
D0	9C01	5CC0	5D80	9D41	5F00	9FC1	9E81	5E40
D8	5A00	9AC1	9B81	5B40	9901	59C0	5880	9841
E0	8801	48C0	4980	8941	4B00	8BC1	8A81	4A40
E8	4E00	8EC1	8F81	4F40	8D01	4DC0	4C80	8C41
F0	4400	84C1	8581	4540	8701	47C0	4680	8641
F8	8201	42C0	4380	8341	4100	81C1	8081	4040

TABLE 17-1 DATA BASE TABLES (Continued)

(b) Data for the CRC-SDLC

00	0000	1189	2312	329B	4624	57AD	6536	74BF
08	8C48	9DC1	AF5A	BED3	CA6C	DBE5	E97E	F8F7
10	1081	0108	3393	221A	56A5	472C	75B7	643E
18	9CC9	8D40	BFDB	AE52	DAED	CB64	F9FF	E876
20	2102	308B	0210	1399	6726	76AF	4434	55BD
28	AD4A	BCC3	8E58	9FD1	EB6E	FAE7	C87C	D9F5
30	3183	200A	1291	0318	77A7	662E	54B5	453C
38	BDCB	AC42	9ED9	8F50	FBEF	EA66	D8FD	C974
40	4204	538D	6116	709F	0420	15A9	2732	36BB
48	CE4C	DFC5	ED5E	FCD7	8868	99E1	AB7A	BAF3
50	5285	430C	7197	601E	14A1	0528	37B3	263A
58	DECD	CF44	FDDF	EC56	98E9	8960	BBFB	AA72
60	6306	728F	4014	519D	2522	34AB	0630	17B9
68	EF4E	FEC7	CC5C	DDD5	A96A	B8E3	8A78	9BF1
70	7387	620E	5095	411C	35A3	242A	16B1	0738
78	FFCF	EE46	DCDD	CD54	B9EB	A862	9AF9	8B70
80	8408	9581	A71A	B693	C22C	D3A5	E13E	F0B7
88	0840	19C9	2B52	3ADB	4E64	5FED	6D76	7CFF
90	9489	8500	B79B	A612	D2AD	C324	F1BF	E036
98	18C1	0948	3BD3	2A5A	5EE5	4F6C	7DF7	6C7E
A0	A50A	B483	8618	9791	E32E	F2A7	C03C	D1B5
A8	2942	38CB	0A50	1BD9	6F66	7EEF	4C74	5DFD
B0	B58B	A402	9699	8710	F3AF	E226	D0BD	C134
B8	39C3	284A	1AD1	0B58	7FE7	6E6E	5CF5	4D7C
C0	C60C	D785	E51E	F497	8028	91A1	A33A	B2B3
C8	4A44	5BCD	6956	78DF	0C60	1DE9	2F72	3EFB
D0	D68D	C704	F59F	E416	90A9	8120	B3BB	A232
D8	5AC5	4B4C	79D7	685E	1CE1	0D68	3FF3	2E7A
E0	E70E	F687	C41C	D595	A12A	B0A3	8238	93B1
E8	6B46	7ACF	4854	59DD	2D62	3CEB	0E70	1FF9
F0	F78F	E606	D49D	C514	B1AB	A022	92B9	8330
F8	7BC7	6A4E	58D5	495C	3DE3	2C6A	1EF1	0F78

17.3 FUNCTIONAL DESCRIPTION

Sheet 2 of the High Speed Data Handling Schematic (02-428D08) contains the logic comprising the most significant portion (bits 0:7) of the Residual Check Character Register (RCCR). Sheet 3 of the schematic contains the least significant portion (bits 8:15) of the RCCR. The most significant bits can be loaded with three different data forms: data from the D bus, data from Table 17-1, or data from the RCCR itself. The least significant bits can also be loaded with three data formats. The major difference is that the former is loaded with its own contents, while the latter is loaded with the Exclusive-ORed data of the RCCR's most significant 8 bits and the least significant 8 bits of the Table Data (TDAT 8:15). The steering counter shown on Sheet 5 determines the format of data loaded into the RCCR.

Sheet 4 of the schematics contains the format register, Current Character Register (CCR), and the CRC tables. The CCR is an 8-bit register containing the data character currently being calculated into the RCCR. The CCR is loaded from the D bus if the steering counter (Sheet 5) causes it to be a destination. The output of the CCR is Exclusive-ORed with the least significant bits of the RCCR. The resultant data is used as the new residual check character in the LRC mode of error check or the resultant data is applied as an address on CRC tables. There are two distinct data groups that provide data base information for the calculation of character error checks in either a CRC-SDLC or CRC-BISYNC format. Selection of a specific character within the tables is accomplished by the address data from the Exclusive-ORed gates. This address information selects one 16-bit character out of a possible 256 in a given table. Table selection is accomplished by the Format Register (FMTR) which is loaded from the D bus if the steering counter (Sheet 5) selects the FMTR to be a destination. Data loaded into the FMTR specifies one of three types of error checking: LRC, CRC-BISYNC, or CRC-SDLC.

Sheet 5 of the schematics contains both timing and control logic for the High Speed Data Handling Board. This logic may be divided into three categories:

- addressing logic
- acknowledge logic
- clock steering logic

Depending upon strap options, the addressing logic determines if the board is selected by the processor. If TP6 is high, the processor has selected the board and an operation is in progress.

The High Speed Data Handling Option Board has a preferred device address of X'006' when strapped for operation on the processor. The acknowledge logic captures the RACK0 signal once the board is selected by the 3215 processor. The RACK0 signal, when captured, results in gating the contents of the RCCR to the D bus. The acknowledge logic is disabled when the board is set up for a 3240 processor and all RACK0s are propagated as TACK0s. Assuming the board is selected, every transition of CMD0 and DA0 (3240 processor only) or BCNT0 (3215 processor only) causes an internal clock to be generated in the clock steering logic. This clock toggles a 2-bit counter that steers a delayed clock to the appropriate destination register. There are three valid states:

- 01 causes the FMTR to be loaded.
- 10 causes the RCCR to be loaded from the D bus.
- 11 causes the CCR to be loaded and the RCCR to be updated.

The counter remains in state 11 until either an ADRS1 (3240 processor) or an ACK0 (3215 processor) is received. At this time the counter is cleared and the board returned to the initialized state until it is again accessed by the processor.

17.4 CHARACTER ERROR CHECKING CALCULATIONS

The following examples describe the interaction between the processor and the High Speed Data Handling Option Board.

LRC Example:

1. The FMTR is loaded with X'02', placing the High Speed Data Handling Option Board in the LRC mode of error checking.

2. The RCCR is loaded with an initial residual of X'0000'. The initial residual can be any number.

3. The CCR is loaded with X'01' and is Exclusive-ORed with the least significant 8 bits of the RCCR.

4. The resultant data (step 3) is loaded into the least significant 8 bits of the RCCR leaving the most significant bits unchanged. The RCCR contains the value of X'001'.

5. The CCR is loaded next with an X'03' and Exclusive-ORed with the current contents of the RCCR. The resultant data is loaded into the RCCR. The content of the RCCR is X'002'.

CRC-BISYNC Example:

1. The FMTR is loaded with X'00', placing the High Speed Data Handling Option Board in the CRC-BISYNC mode of error checking.

2. The RCCR is loaded with an initial residual value of X'0000', but can be any number.

3. The CCR is loaded with X'01' and Exclusive-ORed with the least significant 8 bits of the RCCR.

4. The resulting data (step 3) is applied to the address inputs of the CRC-BISYNC portion of the ROM table. The CRC-BISYNC table output is X'C0C1'.

5. The most significant 8 bits of the ROM table output are loaded into the most significant 8 bits of the RCCR, and the least significant 8 bits of the ROM table output is Exclusive-ORed with the initial most significant 8 bits of the RCCR.

6. The resulting data (step 5) is loaded into the least significant 8 bits of the RCCR. The RCCR contains the value X'C0C1'.

7. The CCR is next loaded with an X'02' and is Exclusive-ORed with the least significant 8 bits of the RCCR. The output of the CRC-BISYNC table is X'5140'.

8. The least significant 8 bits of the CRC-BISYNC table are Exclusive-ORed with the most significant 8 bits of the RCCR. The RCCR still contains the X'C0C1' residual. The most significant 8 bits of the CRC-BISYNC table are loaded into the most significant 8 bits of the RCCR, and the least significant 8 bits of the RCCR are loaded with the Exclusive-ORed result.

CRC-SDLC Example:

Calculations for the CRC-SDLC are identical to the CRC-BISYNC with the exception that the data base table used is for CRC-SDLC.

Table 17-1 is a listing of the data base tables used to calculate CRC-BISYNC and CRC-SDLC. The Exclusive-ORed result of the contents of the CCR and the least significant 8 bits of the RCCR become the 8-bit address of a word in the appropriate table. The words contained in the table are partial results.

17.5 MNEMONICS LIST

The following is a list of the mnemonics within the High Speed Data Handling Option Board. These mnemonics represent the function of a given signal in an abbreviated form, and are taken from the 02-428D08 schematics.

MNEMONIC	MEANING	SCHEMATIC LOCATION
ACCM0	Accumulates a check character; indicates that the steering counter is in the 11 state	Sheets 2, 3, and 5
ADRS0	Used by the processor I/O system when selecting a device on the bus (3240 processor only)	Sheet 5
BADR0	High speed data handling address line (3221 processor only); must be grounded at backpanel	Sheet 5
BCNT0	High speed data handling control line (3221 processor only)	Sheet 5
C001:150	Newly calculated residual character input data	Sheets 2 and 3

MNEMONIC	MEANING	SCHEMATIC LOCATION
CCRNTO	Clears the steering counter and initializes the board	Sheets 4 and 5
D000:150	D bus data sent and received by the processor	Sheets 2, 3, and 4
DCRO	Unused processors	Sheet 5
ELRES1	Early load residual character - used when loading the RCCR from the D bus	Sheets 2 and 5
LDATA1	Loads data character from the D bus into the Current Character Register (CCR)	Sheets 4 and 5
LFMT1	Loads Format Register (FMTR) from the D bus	Sheets 4 and 5
LLRES1	Late load residual character - used when updating the RCCR from the internal calculations (C001:151)	Sheets 2 and 5
LRCD081:151	LRC data - this is the Exclusive-ORed contents of the CCR and the least significant 8 bits of the RCCR.	Sheets 3 and 4
LRCEN1	LRC enable - decoded state of the FMTR indicating the selected LRC format of error check	Sheets 3 and 4
RACKO	Received acknowledge - when operation is in progress, indicates processor is unloading RCCR	Sheet 5
RCD001:151	Residual character data - contents of the Residual Check Character Register	Sheets 2, 3, and 4
TDAT001:151	Table data output - may be from either the CRC-BISYNC or CRC-SDCC portion of the table	Sheets 2, 3, and 4
ULCRC1	Unloads the Residual Check Character Register into the D bus	Sheets 3 and 5

CHAPTER 18
8 MB LOCAL BANK CONTROLLER (LBC)(35-806)

18.1 INTRODUCTION

18.1.1 General

The 3230 memory system consists of 1 Local Bank Controller (LBC) and up to 8 Storage Modules (STMs). The LBC (35-806F01) can be strapped for either 8 Mb main memory capacity which uses 512 kb, 1 Mb, or 2 Mb STMs, or 16 Mb main memory capacity, which uses 1 Mb or 2 Mb STMs.

18.1.2 Power Requirements

Table 18-1 shows the power requirements for the LBC board.

TABLE 18-1 POWER REQUIREMENTS

VOLTAGE SYMBOL	MODULE TYPE	NOMINAL VOLTAGE	MAXIMUM CURRENT DRAIN (AMPS)		
			OPERATING (SELECTED)	OPERATING (UNSELECTED)	STANDBY MODE
P5	35-806F01	+5.0 V	16.7A	16A	16A*
P5U	35-806F01	+5.0 V	1.8A	1.8A	1.8A

*P5 supply may be depowered in the standby mode.

18.1.3 Strapping and Test Point Information

The following test points are located on the front edge of the 35-806 LBC Board:

1. ECC Disable (TP1 and TP2, Sheet 5)

   Strapping TP1 to TP2 disables the Error Check and Correction (ECC) circuit, thereby preventing correction or detection of data errors. The error logger if equipped cannot be updated with the ECC disabled.

   For normal ECC and error logger operation, TP1 and TP2 should be left unstrapped.

2. Cache Miss (TP3 and TP4, Sheet 12) (F01 only)

   Leaving the strap frcm TP3 to TP4 open forces a cache miss condition causing all processor reads to be made from the STM in the quadword mode. This mode of operation is useful in diagnosing cache-related problems.

   For normal cache operation, TP3 and TP4 should be left strapped.

3. P5U Monitor (TP6, Sheet 13)

   The P5U supply voltage (+5.0 V + 1%) may be monitored at TP6 using TP1, TP3, or TP7 for the ground reference.

4. MBIC Monitor (TP5, Sheet 13)

   The MBI flip-flop may be monitored at this point using TP1, TP3, TP7, TP10, or TP12 for the ground reference.

5. Cache Bypass (TP7 and TP8, Sheet 16)

   Strapping TP7 to TP8 enables operation of the cache on the F01 board. The F02 board must have these pins unstrapped, as it is not equipped with the cache. The F01 board may be used in the cache bypass mode (TP7 and TP8 unstrapped) for test purposes or in cases where the cache is malfunctioning.

6. 8 Mb Strap (TP9 and TP10, Sheet 3)

   Strapping TP9 to TP10 puts the LBC in 8 Mb mode. Leaving TP9 to TP10 open puts the LBC in 16 Mb mode.

7. UCE Lamp Reset (TP11 and TP12, Sheet 7)

   The UCE lamp may be reset by momentarily shorting TP11 and TP12. This feature must be used only by trained personnel.

8. Cycle Steal Refresh Inhibit 0/1 (TP13 and TP14, Sheet 13)

   Cycle steal refresh may be inhibited by connecting either TP13 or TP14 to TP12 (GND). This feature must be used only by trained personnel.

9. Refresh Counter Load (TP15, Sheet 13)

   The refresh counter may be preset to all 1s by connecting TP15 to TP12 (GND). This feature must be used only by trained personnel.

10. Timer A Set (TP16, Sheet 16)

    The A timer may be fcrced on by connecting TP16 to TP12 (GND). The timer will remain in the active high state as long as TP16 is grounded. This feature must be used only by trained perscnnel.

11. P5 Shutdown and P5 Shutdown A (TPA and TPB, Sheet 13)

    TPA and TPB must remain strapped. Only trained personnel should remcve this strap.

12. Tag Address Lines 8-21 (TPP, TPQ, TPN, TPM, TPL, TPK, TPJ, TPI, TPH, TPG, TPF, TPE, TPD, and TPC, Sheet 12) (F01 only)

    These 14 lines are the output of the Cache Tag RAMs. These test points must never be connected together or shorted to ground.

18.1.4 LBC LED Indicator Information

The following LED indicators are located on the front edge of the 35-806 LBC board:

1. P5U Indicator

   The P5U indicator lights whenever the P5U supply is active. The P5U supply remains active at all times unless the REMOTE POWER switch (X5) or the MAINTENANCE RESET switch is placed to the OFF position. Before removing the LBC board or STMs, verify that the P5U LED is extinguished and that the KEY switch on the System Control Panel (SCP) is in the OFF position.

2. Cache Parity Indicator (35-806 F01 board only)

   The cache parity indicator lights whenever the cache buffer has output data with bad parity. The indicator remains lit until the SCP INITIALIZE switch is depressed or the KEY switch has been placed in the OFF position.

3. Uncorrectable Error (UCE) and Module Identification Indicators

   The Uncorrectable Error (UCE) indicator lights whenever a Storage Module (STM) outputs a data word containing a detectable multiple bit error. When the UCE indicator is lit, the module ID indicators contain the 512 kb module address where the last Read error occurred (8 Mb Mode), or the 1 Mb module address where the last Read Error occurred (16 Mb Mode).

The UCE indicator remains lit until the SCP INITIALIZE switch is depressed, until the KEY switch is placed in the OFF position, until an REL (Data) instruction is executed, until a Read is executed to nonpresent memory, or until TP11 and TP12 are shorted. When the UCE indicator is off and the module ID indicators are on, they indicate that a memory access was made to the module specified by the lamps, but that the system is not equipped with that module.

18.2 FUNCTIONAL ANALYSIS

18.2.1 Refresh

Refer to Figures 18-1 and 18-2 for refresh timing information. The Storage Modules (STMs) utilize 16k x 1/64k x 1 MOS dynamic RAMs which require periodic refresh cycles at each of the 128/256 row address locations every two to four milliseconds. This is accomplished by executing a single refresh cycle every 16 microseconds (cycle steal mode) or a 128/256 refresh cycle burst every two to four milliseconds (standby mode). During any refresh cycle, every memory chip within the system is selected and refreshed at the same row location.

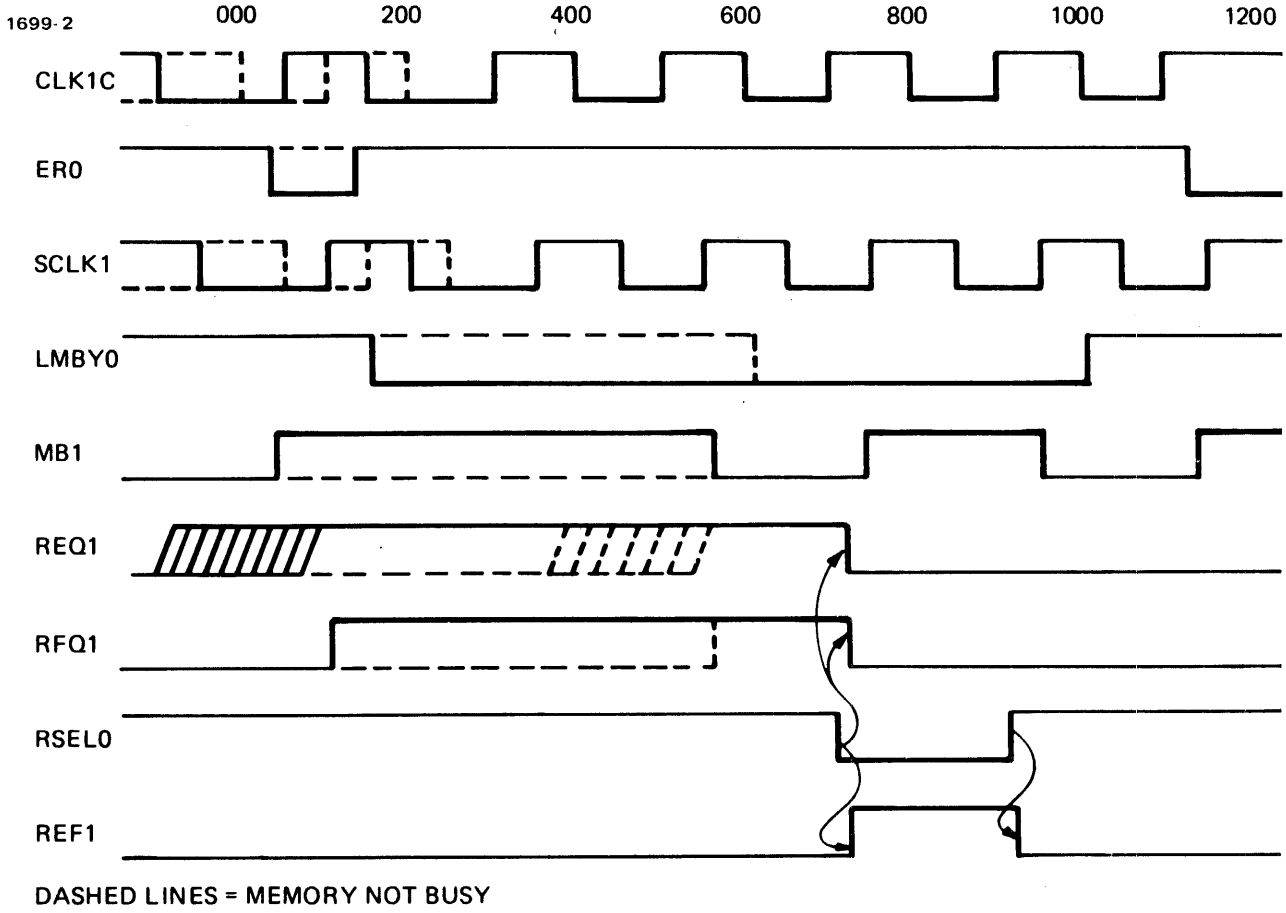


Figure 18-1 Refresh Cycle Steal Timing

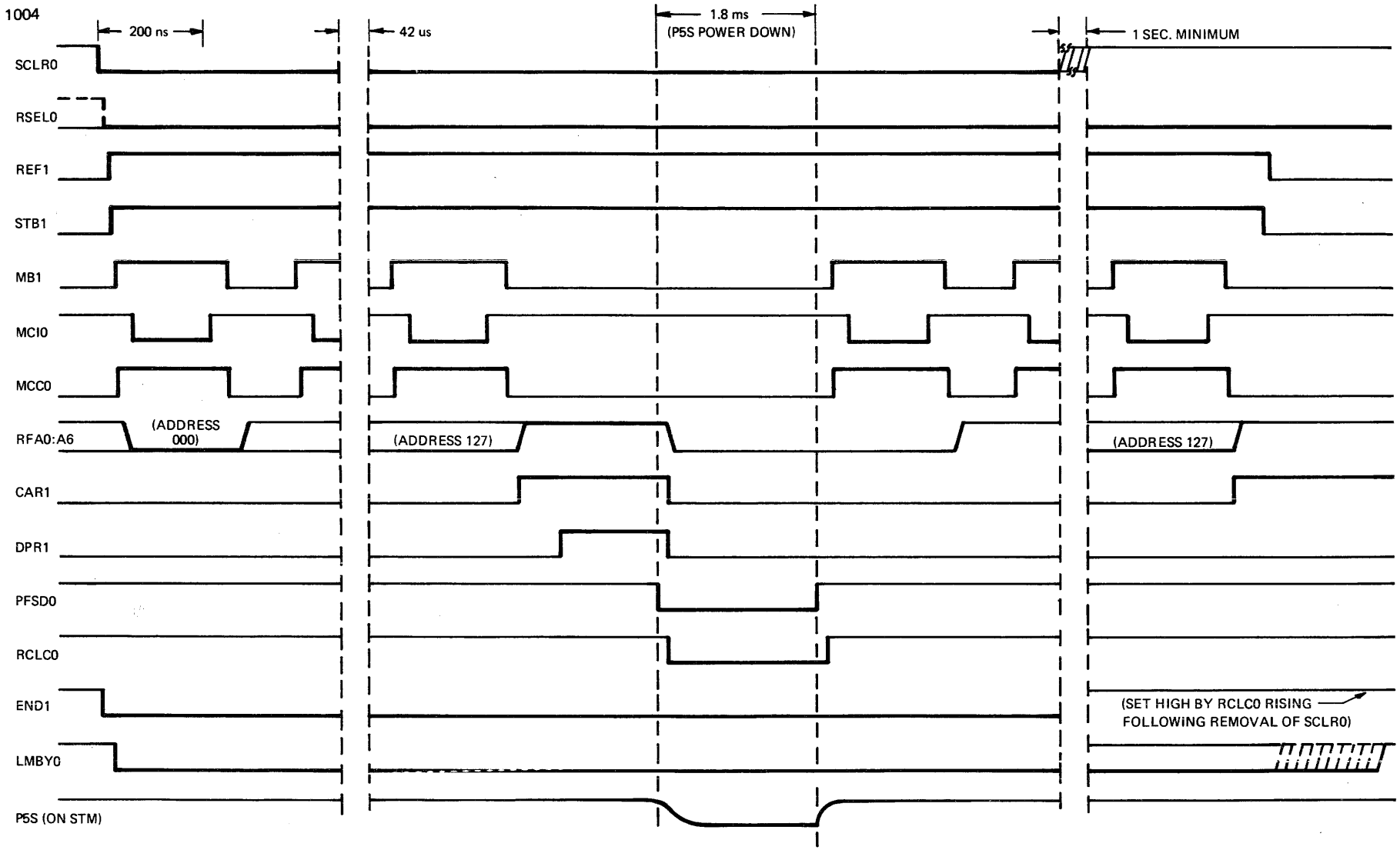


Figure 18-2 Burst Refresh Timing

18.2.1.1 Burst Standby Mode

The standby mode is entered whenever the consolette INITIALIZE switch is depressed or the KEY switch is placed to the OFF position, causing the System Clear (SCLR0) line to go active. SCLR0 (13C3) causes REF1 (13K3) to go active, enabling the refresh address driver 11C (3M2) and setting the MB1 flip-flop. MB0 sets the TA001 flip-flop (16B6), starting the TA timer, which causes MCI0 (16S5) to go active and initiate the refresh cycle to the STM(s). With MREF0 (9G5) active, all STMs in the system are enabled to perform the refresh cycle (refer to the chapter on the STM for a detailed description).

The LBC refresh scheme is designed to accommodate 64k x 1 memory chips. Some 64k chips require 128 rows (2 ms refresh), and some 64k chips require 256 rows (4 ms refresh). To insure data integrity, the LBC does burst refresh as follows: When SCLR0 goes active, the LBC does a 256 cycle burst refresh, insuring that all rows are refreshed. Then every 2 ms, a 128 cycle burst refresh is performed. This accommodates both types of 64k RAMs and saves power over doing a 256 cycle burst refresh every 2 ms. When SCLR0 goes inactive, the IBC does a 256 cycle burst refresh before returning to cycle steal mode.

When TA201 (13G8) goes high, the refresh counter (13J5 and 13M5) is advanced and the MB1 flip-flop (13K7) is cleared. This causes MCC0 (9G2) to go active, ending the first refresh cycle. When TA181 (13G8) goes low, the MB1 flip-flop (13K7) is directly set, starting the next refresh cycle. This mode of operation continues for 128 cycles allowing the DPR1 flip-flop (13J2) to be clocked set and PFSD (13N2) to be activated. PFSD0 (9R4) going active causes the STM(s) P5S switch to turn off, placing it into a low power standby mode and activating RCLC0 (9N5). RCLC1 (13E4) causes the refresh counter (13J5 and 13M5) and the DPR1 flip-flop (13J2) to be cleared, allowing the 1.8 ms one-shot (13M2) to time out and deactivate PFSD1. PFSD0 (9R4) going inactive causes the STM(s) P5S switch to turn on, deactivating RCLC0 (9N5), thereby setting the MB1 flip-flop (13K7) and initiating a 128 cycle burst.

This mode of operation continues until SCLR0 is brought high by returning the System Control Panel KEY switch to the ON position and timing out the initialize function. This causes the END1 flip-flop (13F5) to be clocked set after completing a 256-cycle burst, allowing the STB1 flip-flop (13H1) to be clocked reset at the end of that burst. STB1 going low causes REF1 (13K3) and REF0 (13L3) to go inactive, allowing LMBY0 (15N8) to be returned high, indicating to the processor that the memory is ready to accept a command. Memory refreshing is continued by performing a single refresh cycle steal every 16 microseconds.

18.2.1.2 Cycle Steal Refresh

A refresh cycle steal is initiated whenever the free-running 16 microsecond oscillator (13B2) clocks the REQ1 flip-flop (13D2) set, thereby allowing the RFQ1 flip-flop (15K7) to queue up this request. Flip-flop 07A (13E2) and the RSEL0 flip-flop (13F2) are used to further synchronize the start and end of the refresh cycle to prevent overlapping of memory operations. Operation in the refresh cycle steal mode is identical to the burst refresh cycle, with the exception that only one cycle is executed and the DPR1 flip-flop (13J2) is never activated.

18.2.2 LBC Operating Modes

The LBC operates in a number of different modes (refer to Table 18-2) as determined by the states of ROM data lines RD011:031 (3E7), WRT0 (3A6), DMAHW0 (3A6), PSEL1 (3A6) and LMA190 (3A5) at the time ER0 (13G7) goes active. These signals are loaded into transparent latches whose outputs drive the mode selector logic consisting of one of eight decoders 20F (14C3) and 20J (14C5) and miscellaneous gate functions (left half of Sheet 14). For any given operation, certain mode decoder outputs go active (refer to Table 18-2), setting up the control logic for the specific data manipulation required.

TABLE 18-2 LBC OPERATING MODES

1873-2

MATRSD0	MATRSR0	DRST0	PSELIA	WRT0	RD 011	RD 021	RD 031	PROCESSOR OPERATIONS	MODE DECODER OUTPUTS ACTIVE (See Sheet 14 35-728D08)
1	1	1	1	0	0	0	0	No Memory Operation	
1	1	1	1	0	0	0	1	Store Byte	SBY1, SPW1, SPW0
1	1	1	1	0	0	1	0	Store Halfword (Privileged)*	SHW1, SPW1, SPW0
1	1	1	1	0	0	1	1	Store Halfword (Data)*	SHW1, SPW1, SPW0
1	1	1	1	0	1	0	0	Test Error Logger (Store Byte)	TEL0, TEL1, SBY1
1	1	1	1	0	1	0	1	No Memory Operation	
1	1	1	1	0	1	1	0	Store Fullword (Privileged)*	SFW1, SFW0
1	1	1	1	0	1	1	1	Store Fullword (Data)*	SFW1, SFW0
1	1	1	1	1	0	0	0	No Memory Operation	
1	1	1	1	1	0	0	1	Read and Set Halfword	RST0, RST1, SPW1, ROAST1
1	1	1	1	1	0	1	0	Read Halfword (Privileged)* (Fullword Operation)	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	0	1	1	Read Halfword (Data)* (Fullword Operation)	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	0	0	Read Error Logger	EL0, REL1 (active with LMA190 high), ELST1 (active with LMA190 low)
1	1	1	1	1	1	0	1	Read Fullword (Instruction Read)*	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	1	0	Read Fullword (Privileged)*	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	1	1	Read Fullword (Data)*	PRFW0, PRFW1, RFW1, ROAST1
			PSELIA	WRT0	DMAHW0			DMA Operations	
1	1	1	0	0	0			Store Halfword	SHW1, SPW1, SPW0
1	1	1	0	0	1			Store Fullword	SFW1, SFW0
1	1	1	0	1	0			Read Halfword (Fullword Operation)	DRFW0, DRFW1, RFW1, ROAST1
1	1	1	0	1	1			Read Fullword (Fullword Operation)	DRFW0, DRFW1, RFW1, ROAST1
1	1	0						DMA Read and Set	DRST0
1	0	1						MAT Read and Set Reference Bit	MATRSR0
0	1	1						MAT Read and Set Dirty Bit	MATRSD0

*LBC does not differentiate between privileged and data instruction.

There are seven basic functional modes used by the LBC to service all operations. They are:

1. Store Fullword (Refer to Figure 18-3)

2. Store Partial Word (Refer to Figure 18-4) including:

   - store byte
   - store halfword
   - read and set
   - test error logger

3. CPU Read Fullword (with cache hit)
   (Refer to Figure 18-5)

4. CPU Read Fullword (with cache miss)
   (Refer to Figure 18-6)

5. Read Fullword with cache not equipped (bypassed) or DMA read (Refer to Figure 18-7)

6. Read Error Logger Status (LMA190 low)
   (Refer to Figure 18-8)

7. Read Error Logger (LMA190 high)
   (Refer to Figure 18-9)

NOTE

All read halfword operations are decoded as read fullword operations by the LBC. Data steering for halfword operations is performed on the CPU-C board.

1701-2

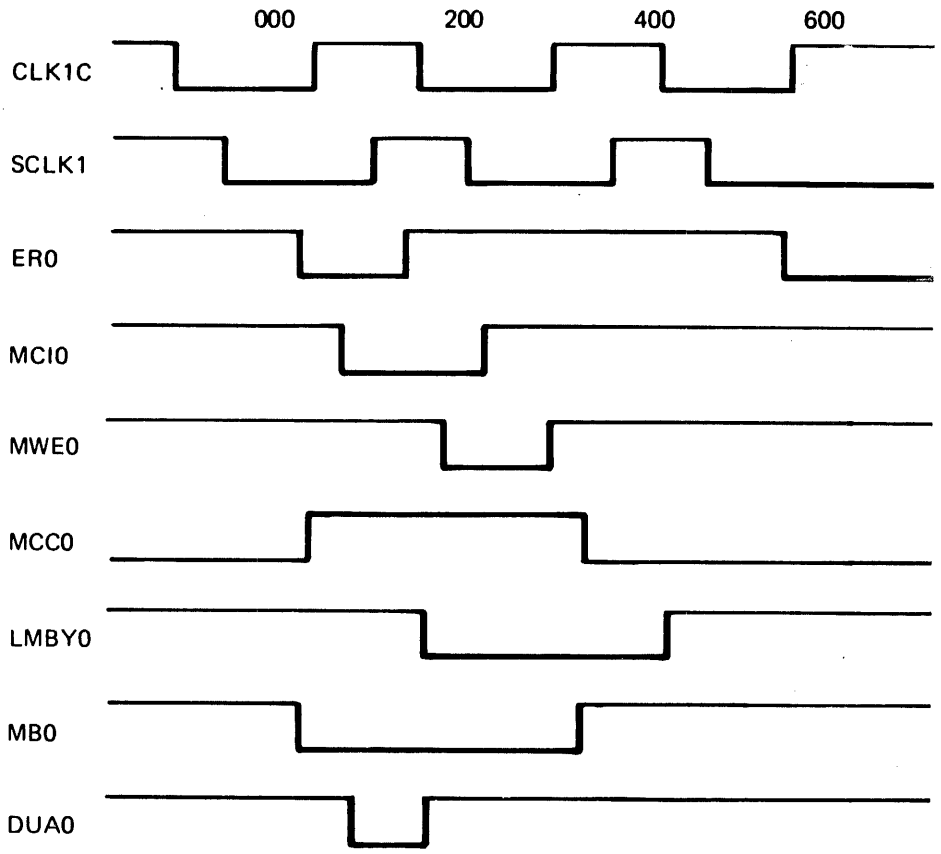


Figure 18-3 Store Fullword

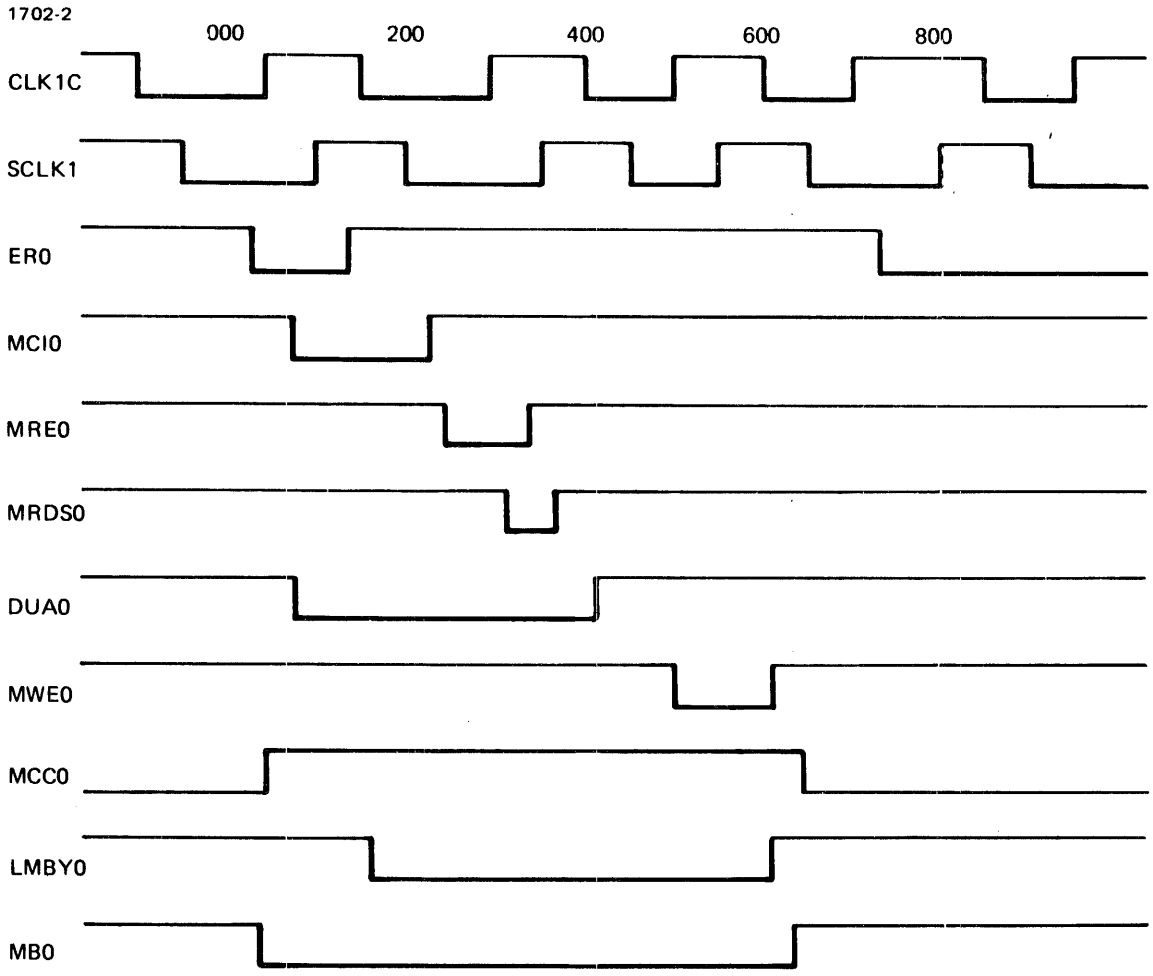


Figure 18-4 Store Partial Word

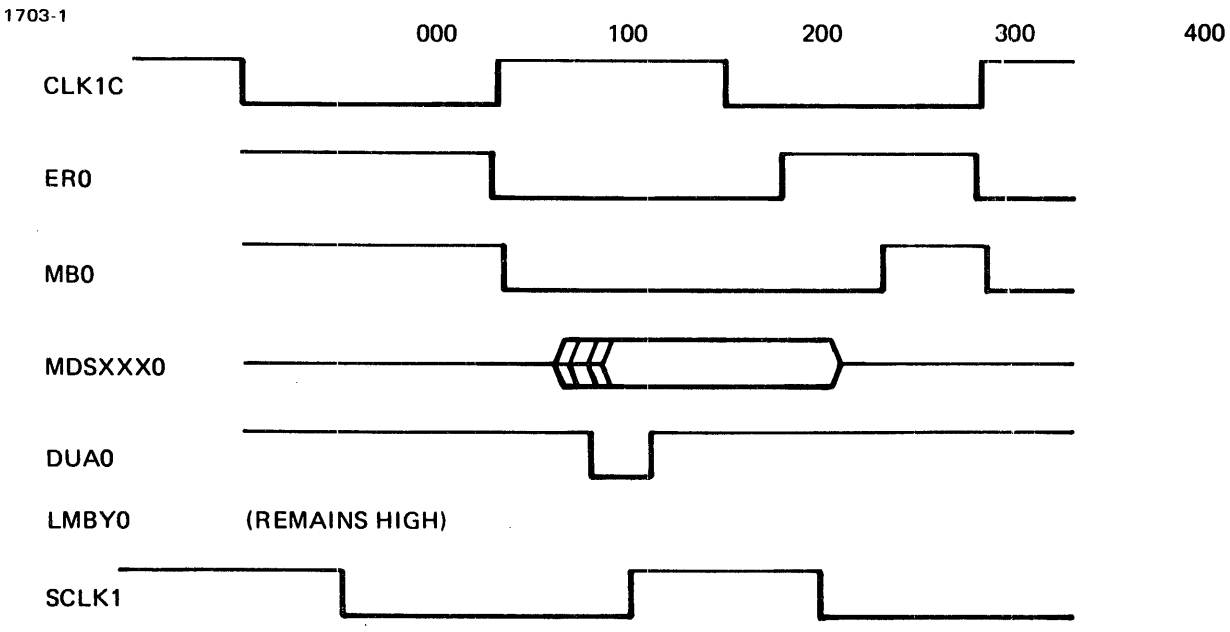


Figure 18-5 CPU Read (With Cache Hit)

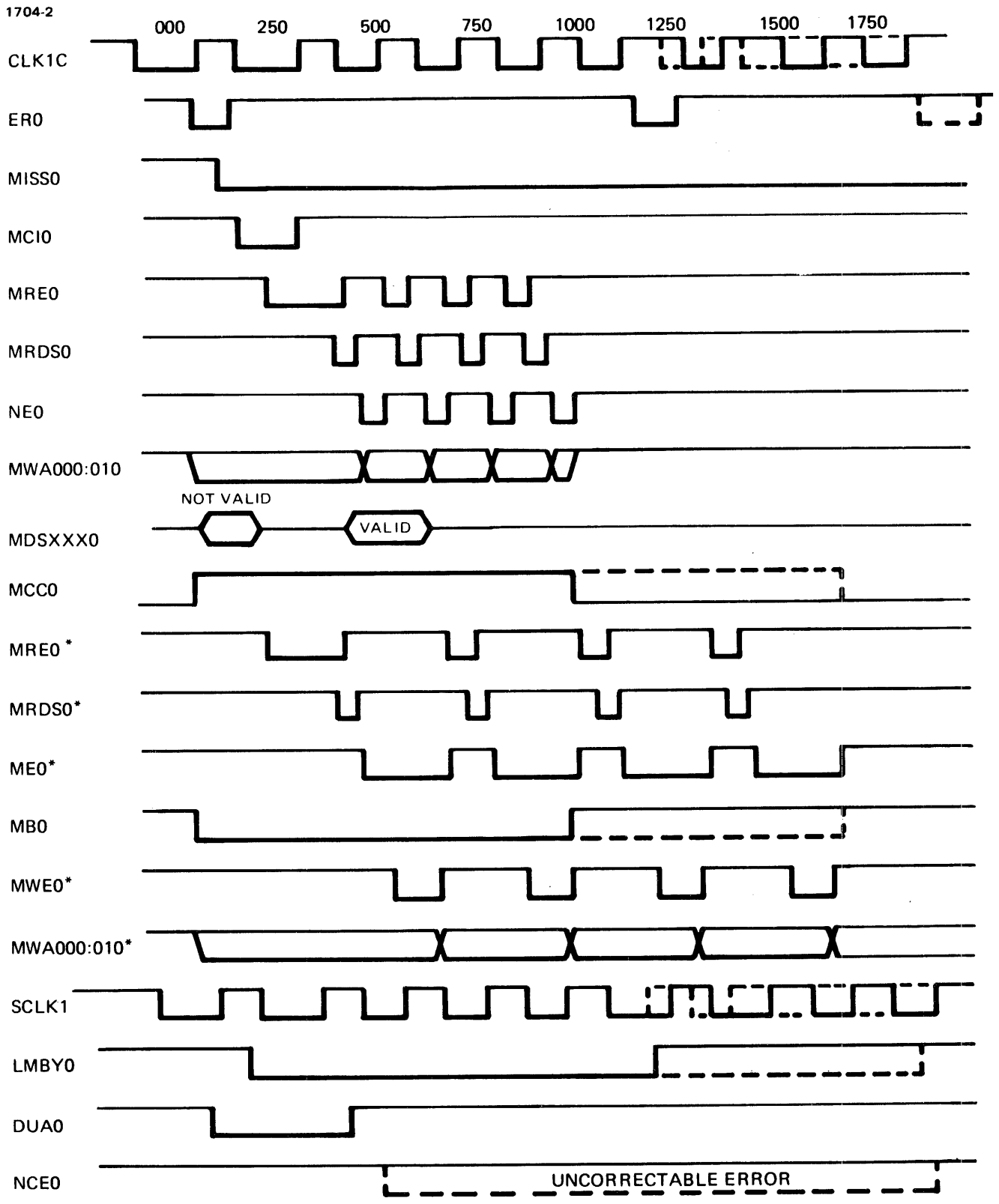


Figure 18-6 CPU Read (With Cache Miss)

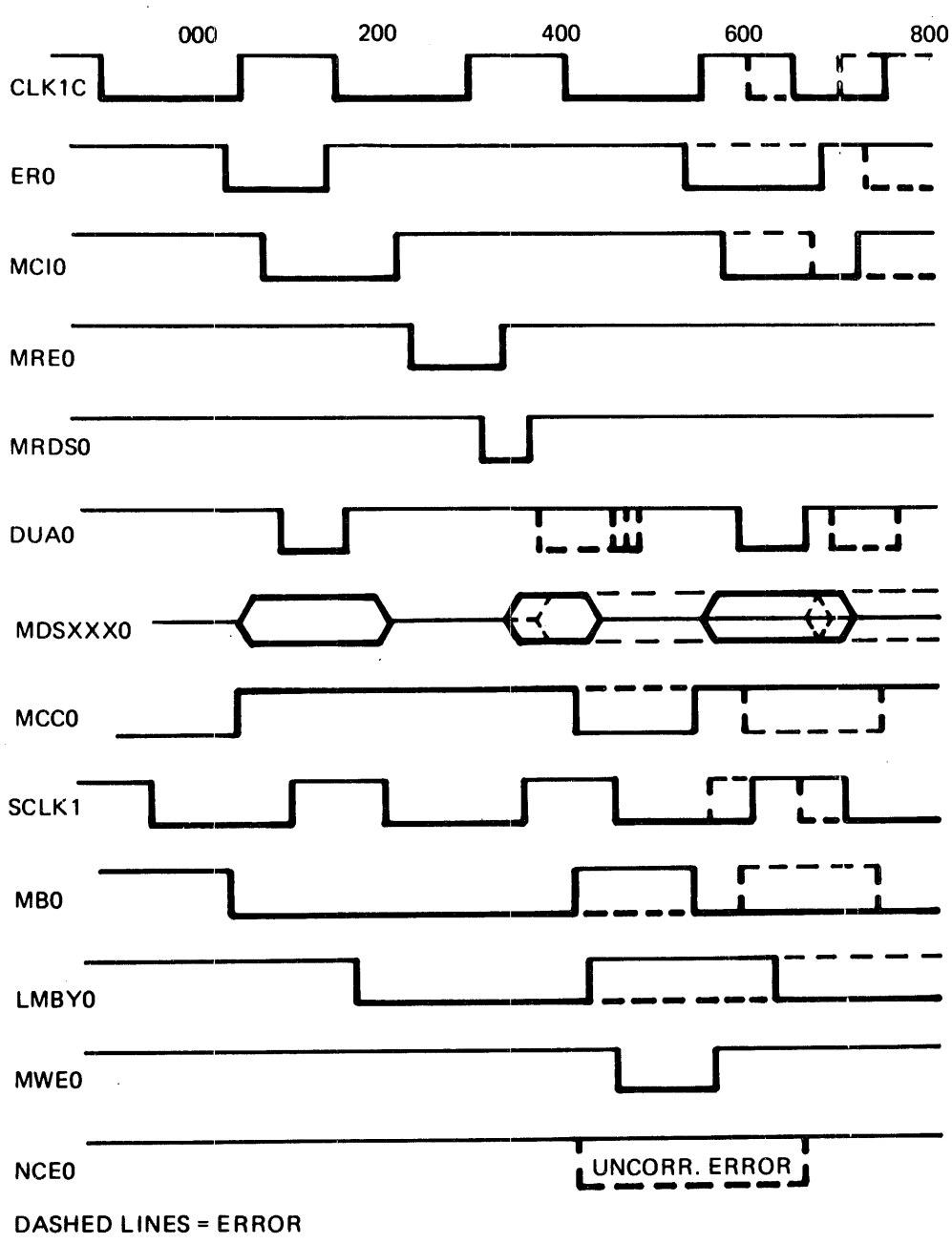


Figure 18-7 Cache Bypass

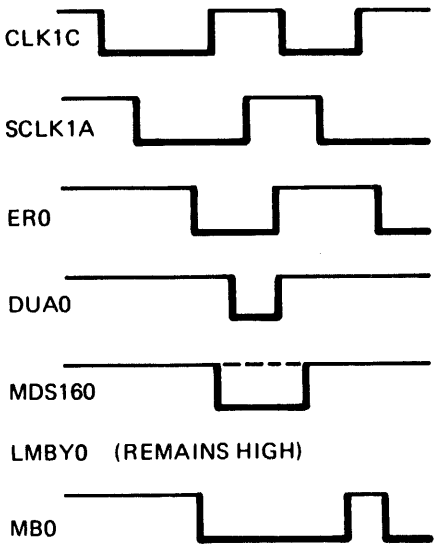


Figure 18-8 Read Error Logger Status

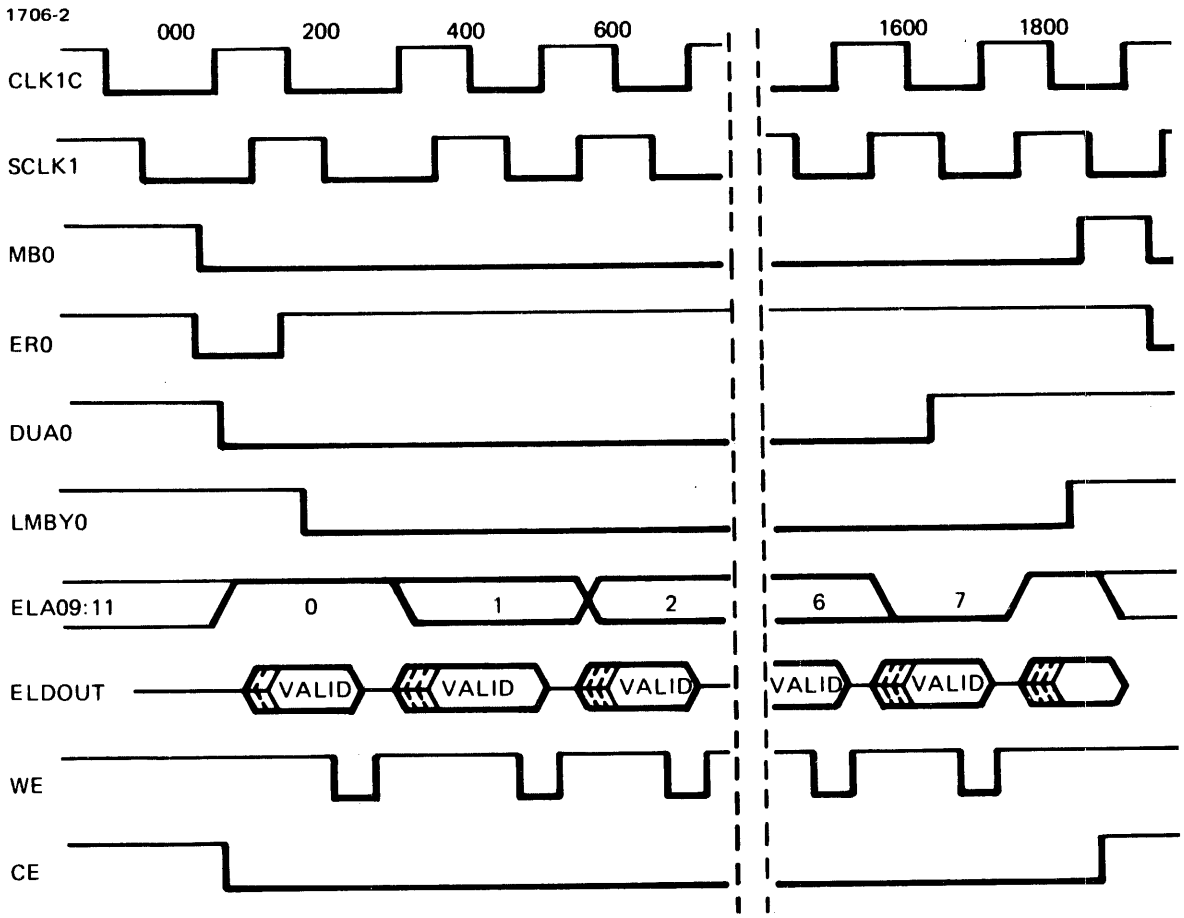


Figure 18-9 Read Error Logger

Timing diagrams for the A and B timers are provided in Figures 18-10 and 18-11. Table 18-3 provides data and address bus alignment information. The subsequent sections describe each of the seven basic functional modes.

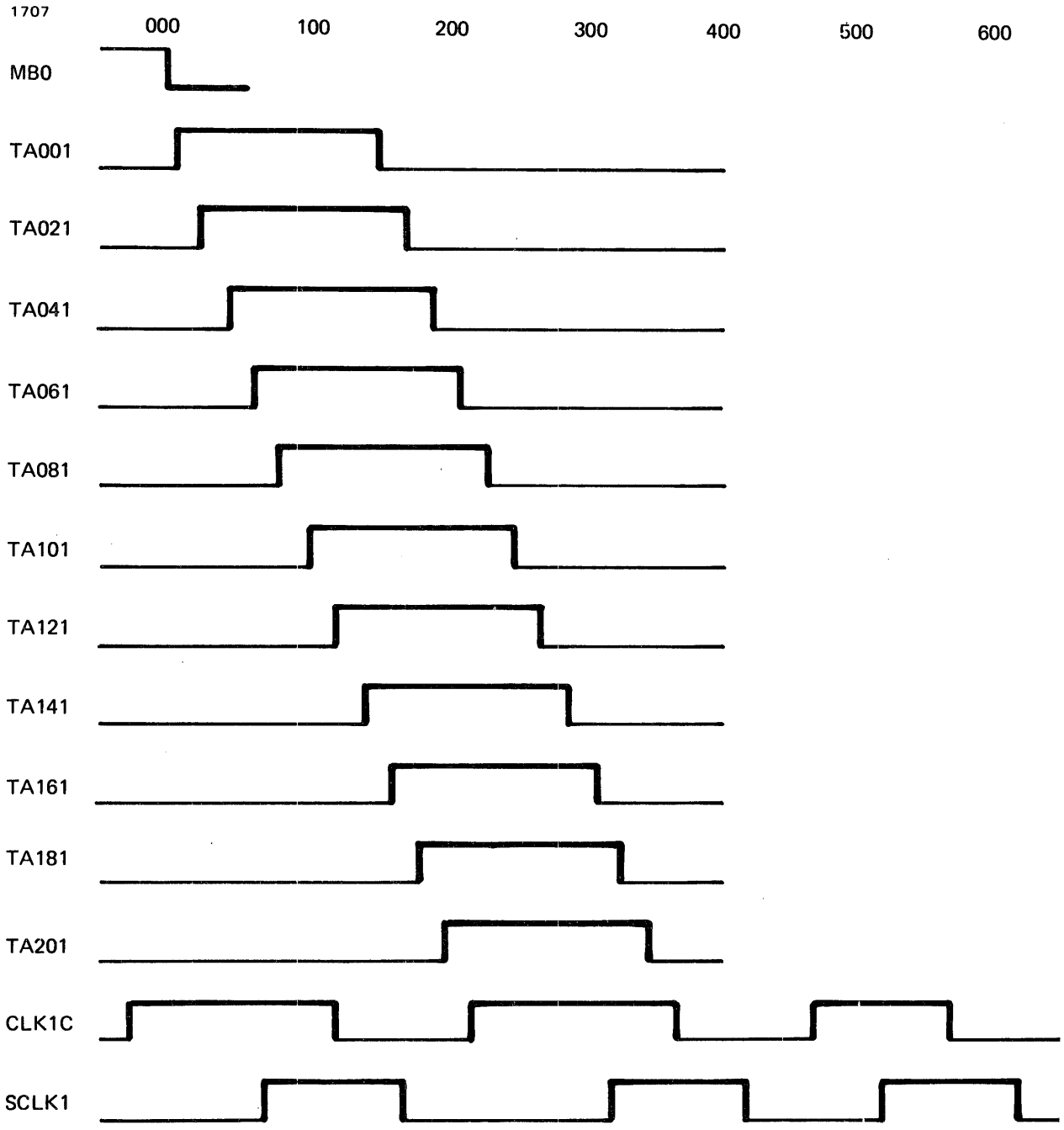


Figure 18-10 A Timer

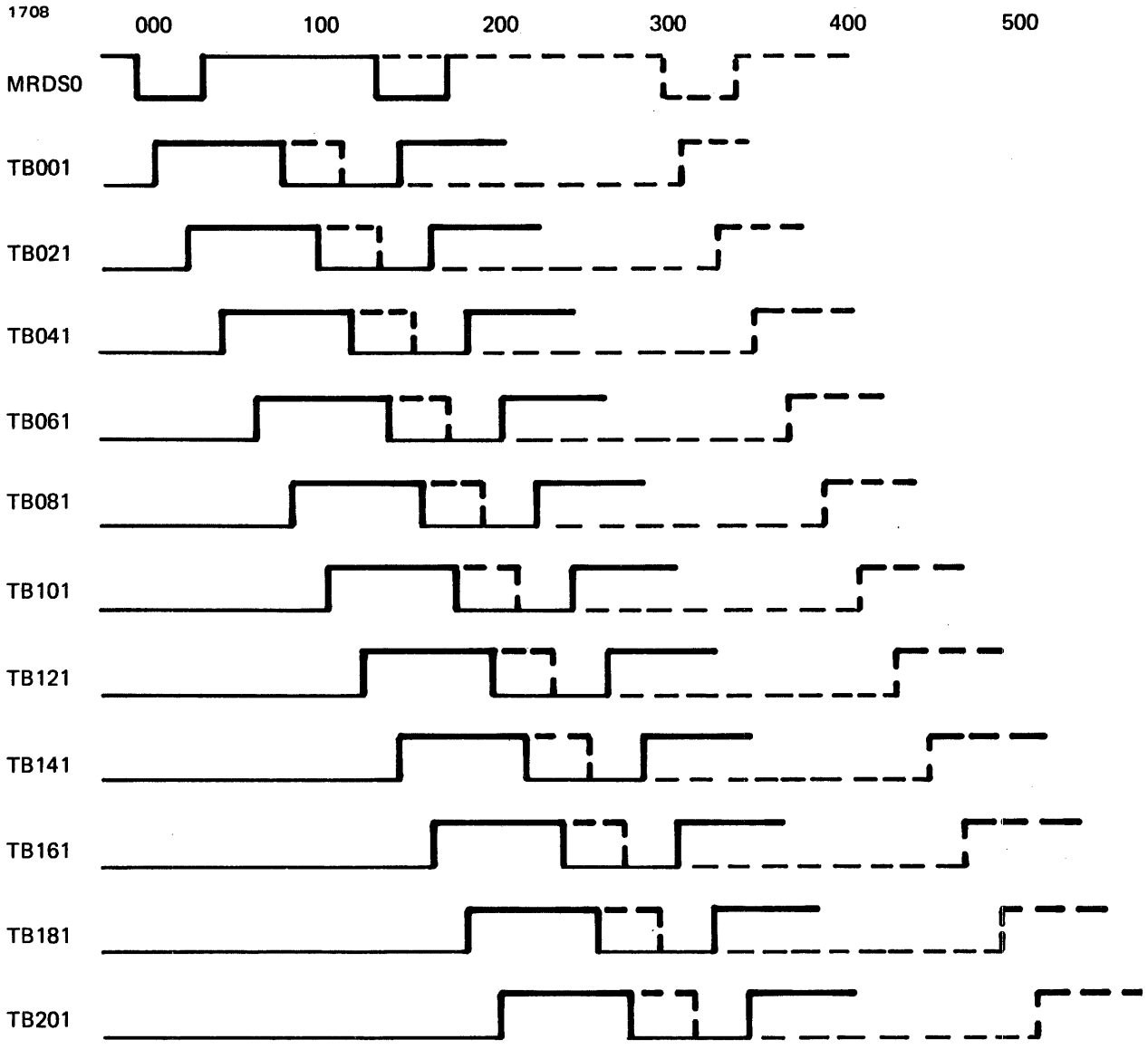


Figure 18-11 B Timer

TABLE 18-3 3230 MEMORY SYSTEM ADDRESS BUS ALIGNMENT

LMA	080	090	100	110	120	130	140	150	160	170	180	190	200	210	220	230	240	250	260	270	280	290	300	310						
LMB							001	011	021	031	041	051	061	071	081	091	101	111	121	131	141	151								
MEA (8MB)		000	010	020	030																									
MEA (16MB)	000	010	020	030																										
MX					021	011 031																								
MWA																					000	010								
ERROR LOG ADD. (8MB)		ER. LOG 1/2 SLCT.	0	1	2	3	4	5	6	7	8	ST.																		
		MODULE NO.					WORD COLUMN		S0	S1	S2	BIT																		
ERROR LOG ADD. (16MB)	0	1	2	3			4	5	6	7	8	ST.																		
	MODULE NO.						WORD COLUMN		S0	S1	S2	BIT																		

18.2.2.1 Store Fullword

A store fullword cycle is initiated at the processor by setting up the write data lines MDS000:310 (2A4), address lines LMA080:310 (3A1-3A9), write control line WRT0 (3A6), and mode control lines DMAHW0 (3A6), PSEL1 (3A6), and RD011:031 (3A7). After these lines are set up, the processor generates an ER0 (13G7), clocking the MB1 flip-flop set, thereby starting the memory cycle. MB1 going active causes write data to be latched in the input data register (2G8), addresses to be latched in the address register (3A), and the control lines in their respective registers (3A6). MB0 having set the TA timer flip-flop (16B6) causes MCI0 (16S5) to go active, latching up the address presented on LMB001:151 (3E5,3K2) into the STM selected by lines MEA030 and MEA000 (9G). After satisfying the STM address hold time, the EA0 flip-flop (16R5) is set, thereby tri-stating the LMB001:151 address drivers (3E5,3K2). TA101 (2R4 and 15B2) going active enables the input data register (2G8) and the data bus drivers (Sheets 8 and 9), placing the word to be written onto lines D000:310 and LMB000:310. Lines D000:310 are input to the parity generators (4C5,4F5), whose outputs P000:060 propagate through the write parity register (7F7) onto lines GP000:060. This causes the parity data to be placed onto lines LMB321:381 by the parity data drivers (9E8). TAA121 (15A4) causes WE0 to go low, activating MWE0 (9G3), allowing the data present on lines LMB001:381 to be written into the selected STM. Following the removal of WE1 (14J3), NCLR1 (14R4) goes active, clearing the MB1 flip-flop (13K7) which enables MCC0 (9G2). With MCC0 activated, the write cycle is completed and CLK0D (15M9) causes LMBY0 to go high, signaling to the processor that the memory is no longer busy.

18.2.2.2 Store Partial Word

A store partial word cycle is initiated in the same way as described in the store fullword description. The cycles differ in that the word to be modified must be read from the STM before performing the write. This is necessary to allow new parity data to be generated from the modified word. The following description continues from the point just prior to enabling the input data register, as described in the store fullword operation.

WDEN0 (2R4) going active enables the input data register (2G8), placing the byte (store byte operation or test error log operation) or halfword (store halfword operation) of write data onto data lines D000:310. WDEN0 (14K9) also activates LDBY01:31, causing D000:310 to be loaded into the Good Data Registers (GDR) (Sheet 6).

NOTE

WDEN0 does not go active during a read and set operation.

TA161 (15G1) going active sets the RE1 flip-flop (15J3) which, in turn, activates the Uncorrected Data Register (UDR) (Sheets 8 and 9) and MRE0 (9G1). The STM responds in 240 nanoseconds by activating MRDS0 (9G6), signaling that lines LMB001:381 have been loaded with the read data. RDS0 causes the RE1 flip-flop (15J3) to be reset, removing MRE0 (9G1), latching the UDR (Sheets 8 and 9) and starting the TB timer (16B2). Data lines D000:310 and UP000:060 propagate through the parity checkers (Sheets 4 and 5), generating the Error Check and Correction (ECC) syndrome code on lines P000:060. If no data bit errors are generated, the syndrome code lines are all low deactivating MER0 (5N2). If a single data bit is in error, MER0 goes low along with one output from the DC error decoder (5J8) and one output from the DA or DB error decoder. One of the correction lines EB000:310 (Sheet 6) or EPB000:060 (7C4) goes high, causing the data bit in error to be input to the GDR (Sheet 6) or Good Parity Register (GPR) (7F4) to be corrected (inverted). If any two data bits are in error, MER0 goes low, correction lines EB000:310 and EPB000:060 remain low (no correction), and the uncorrectable error decoder (7M5) goes low allowing the UCE0 flip-flop (7N4) to be activated. UCE0 at AOI gate 20K (15B2) prevents activating ED1 and ED0 when the modified word is written back into the STM, causing all logical ones to be stored in the STM. This is necessary because the new parity data generated could otherwise make the data appear error free on subsequent reads from this location. TB021 (14G9) going active causes LDGP1 (read and set or test error logger operation only) and select LDBY01:31 lines (14M7) to go active, thereby loading the part of the word not to be modified into the GDRs (Sheet 6). TB080 (14G9) going low deactivates LDBY01:31 and UDD0 (15L4) and activates GDD1 (15N4), placing the modified word onto lines D000:310 (Sheet 6). New parity data is generated from this word and appears on lines P000:060 (Sheets 4 and 5) which are loaded into the write parity register (7F7) and output on lines GP000:060.

NOTE

A test error logger operation does not store away new parity data, but it uses the old parity by enabling the GPR (7F4) onto lines GP000:060.

A read and set operation differs from the above description in that the entire word from the STM is loaded into the GDR and, in turn, output to the processor from the output data register (see read fullword operation for description). Additionally, the most significant bit of the halfword D000 or D160 (15G6), as addressed by LMA140, is set on write data line D000A or D160A (15K6).

TBB141 (15A2) activates ED1 and ED0, placing the modified word data and parity data onto lines LMB001:381 (Sheets 8 and 9). TB161 (15A4) causes WE0 and MWE0 (9G3) to go active, placing the STM in the write mode. WE1 (14J3) going inactive causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7), enabling MCC0 (9G2). LMBY0 (15N8), having gone high at the previous edge of CLK0D, signals to the processor that the cycle is complete and the memory is no longer busy.

A DMA read and set and MAT read and set operation is similar to a regular read and set operation, except that only bit 0 is set.

A MAT read and set dirty bit is also similar to a regular read and set operaticn except that bit 2 is set.

18.2.2.3 Read Fullword (Cache Bypassed)

The LBC operates in the cache bypassed mode for any DMA read operation, or for a CPU read operation with the cache bypass strap (16L7) removed (bypass enabled). When the LBC is not equipped with the cache buffer option, it must operate in the bypassed mode. Additionally, those equipped with the cache buffer may be operated in this mode for test or troubleshooting purposes.

A read fullword operation begins with the processor setting up the address bus and contrcl lines to their appropriate states followed by the initiation of the cycle with ER0 (13G7) being activated. ER0 sets the MB1 flip-flop (13K7), causing the address register (3B) and control registers (3B,3E) to be latched and the TA timer flip-flop (16B6) to be set. Lines MX011:031, LMB001:151, and MEA000:030 (Sheet 9) are presented with the address which is latched into the selected STM by MCI0 (16S5). After satisfying the STM address hold time, EA0 (16S4) going active tri-states the address drivers (3E5,3J3,9K9).

TA161 (15G1) going active sets the RE1 flip-flop (15J3) which, in turn, activates the UDR (Sheets 8 and 9) and MREO (9G1). The STM responds in 240 nanoseconds by activating MRDSO (9G6) signaling that lines LMB001:381 have been loaded with the read data. RDSO causes the RE1 flip-flop (15J3) to be reset, removing MREO (9G1), latching the UDR (Sheets 8 and 9) and starting the TB timer (16B2). Data lines D000:310 and UP000:060 propagate through the parity checkers (Sheets 4 and 5), generating the Error Check and Correction (ECC) syndrome code on lines P000:060. If no data bit errors are generated, the syndrome code lines are all low deactivating MERO (5N2). If a single data bit is in error, MERO goes low along with one output from the DC error decoder (5J8) and one output from the DA or DB error decoders. One of the correction lines EB000:310 (Sheet 6) or EPB000:060 (7C4) goes high, causing the data bit input to the GDR (Sheet 6) or GPR (7F4) to be corrected (inverted). If any two data bits are in error, MERO goes low, correction lines EB000:310 and EPB000:060 remain low (no correction), and the uncorrectable error decoder (7M5) goes low, allowing the UCEO flip-flop (7N4) to be activated.

TB080 causes lines LDBY01:31 and LDGP1 (14M6) to load and enable the GDRs (Sheet 6) and the GPR (7F3), placing the data (corrected) onto lines D000:310 and GP000:060. ODD1 (16N3) going active places this data onto the MDS000:310 lines (2A5) for the processor. If an error has been detected, TBB101 (15A1) activates ED1 and ED0 enabling the write data drivers (Sheets 8 and 9) onto LMB001:381; TEB121 (15A3) activates WE0, enabling MWE0 (9G4); and WE0 (14J3) going inactive causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7). If no errors were detected, NE1 (14J2) going active causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7). CLK0D (15M9) going active with DUA0 inactive raises the LMBY0 line, signaling to the processor that the memory is no longer busy.

18.2.3 Cache Option Description

The LBC may be equipped with an optional 256-word cache buffer. The following is a brief description of the cache circuit.

The cache consists of a 256x36 cache buffer (11H1-11H8) which contains byte parity logic (11L1-11L8) and a parity error indicator circuit (11R7). A 64x14 index buffer (12F6) and a 14-bit address comparator (12M3, 12M7) is used to directly map 4-word sets (quadword blocks) stored in the cache buffer. A 64x1 (1/4 of 256x1 RAM IC 26R) validator buffer (12N1) is used to qualify the contents of the index buffer.

The cache buffer is loaded with four consecutive words of data any time a CPU read operation is executed at an address which is not contained in the index buffer (MIS1 high) (12S6), or which is not qualified by the validator (NVAL1 high) (12R3). The cache buffer is also updated with the single word of a store fullword or partial word operation if the index buffer contains the address (MIS1 low) and it is qualified by the validator (NVAL1 low). In this way, the contents of a valid block (4-word set) always matches what is stored in the STM.

The memory system contains up to 16 Mb (4 M words) of storage and the cache buffer contains 256 words (64 x 4-word sets) of storage. The cache buffer is always loaded with a 4-word set as addressed by the index field (refer to Figure 18-12).

1875

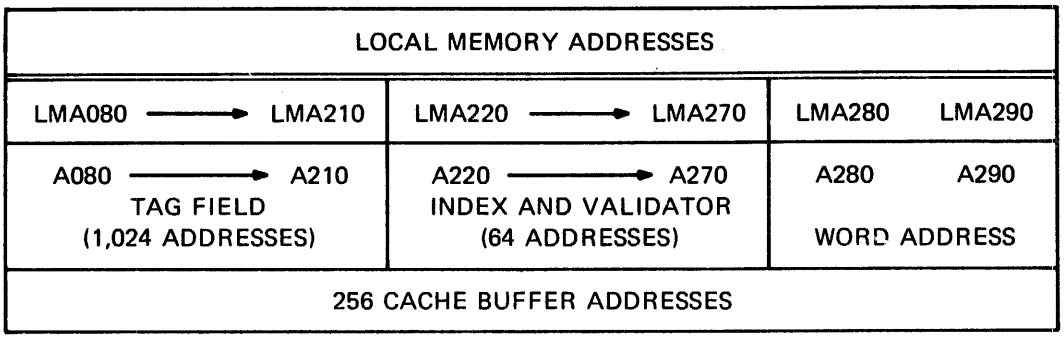


Figure 18-12 Physical Address Fields

This word set may be stored in the STM at any one of the 1,024 locations as addressed by the tag field. When the cache buffer is loaded with a 4-word set, the 14 bits of the tag field are loaded into the index buffer, and the validator bit is set at the location as addressed by the index field. A subsequent CPU read from one of the four word locations generates a match condition at the index address comparator (12M3, 12M7), causing MIS1 (Index Mismatch) to go inactive. Validator output NVAL1 (not valid) goes inactive and is ORed with MIS1, allowing the HIT1 flip-flop to be set. This is called a cache Hit and indicates that the word being addressed is contained in the cache buffer. CPU reads from word locations that are not stored in the cache buffer cause MIS1 (12S6) or NVAL1 to go active, preventing the HIT1 flip-flop from being set. This is called a cache Miss.

18.2.4 CPU Read Fullword (Cache Enabled)

18.2.4.1 Cache Miss

Upon initially powering up the system, a CPU read from any memory location must produce a Miss (refer to cache description) condition because the cache buffer is volatile, and depowering the system causes its contents to be lost. When the consolette power switch has been placed to the ON position or the INITIALIZE switch has been depressed, the main memory remains in the burst refresh mode for a period of time determined by the initialize timer. During this period of time, the validation buffer (12N2) is input with refresh addresses A150:200 from its address multiplexor (12K2), the data input VAL1 is set low (invalid), and the write enable is activated by TA061 (12N3) at IC 22C pin 05. This causes all 64 locations of the invalidator to be written to the invalid state synchronously with the performance of the burst refresh operation.

When the processor initiates the first CPU read, the validator causes NVAL1 (12S6) to go active, preventing the HIT1 flip-flop from being set and activating QWM0, QWM1, and QWE0 (16S7). QWE0 (9K8) causes LMB160 to go low, signaling to the STM that a quadword operation is to be initiated. QWM1 (16K6) allows TA101 to activate MCI0, starting a quadword read cycle. TA160 (15F4) going active sets the RE1 flip-flop (15J3) which, in turn, activates the UDR (Sheets 8 and 9) and MRE0 (9G1). The STM responds in 240 nanoseconds by activating MRDS0 (9G6), signaling that lines LMB001:381 have been loaded with the read data. RDS0 causes the RE1 flip-flop (15J3) to be reset, removing MRE0 (9G1), latching the UDR (Sheets 8 and 9), and starting the TB timer (16B2). Data lines D000:310 and UP000:060 propagate through the parity checkers (Sheets 4 and 5), generating the Error Check and Correction (ECC) syndrome code on lines P000:060. If no data bit errors are generated, the syndrome code lines are all low deactivating MER0 (5N2). If a single data bit is in error, MER0 goes low along with one output from the DC error decoder (5J8) and one output from the DA or DB error decoders. One of the correction lines EB000:310 (Sheet 6) or EPB000:060 (7C4) goes high, causing the data bit in error to be input to the GDR (Sheet 6) or GPR (7F4) to be corrected (inverted). If any two data bits are in error, MER0 goes low, correction lines EB000:310 and EPB000:060 remain low (no correction), and the uncorrectable error decoder (7M5) goes low, allowing the UCE0 flip-flop (7N4) to be activated. UCE0 (12A1) going active causes VAL1 (12N1) to go low, invalidating the word to be stored in the cache buffer.

LDGP1 and LDBY01:31 (14M5-14M9) are activated, loading the corrected word and parity bits into the GDR (Sheet 6) and GPR (7F3). RURE1 (15K4) causes UDD0 to go active and GDD1 to go inactive, disabling the UDR (Sheets 8 and 9) and enabling the GDR and GPR. The corrected word data is output to lines MDS000:310 by the ODR (Sheet 2), returning the word requested by the processor. This word is also written into the cache buffer via lines D000:310 (11J7), along with four parity bits generated by the cache parity circuits (11L2-11L8). If a memory error has been detected, ME1 (15B3) is active, allowing TB121 to activate WE0 (15F3) and MWE0 (9G4), causing the corrected data (D000:310 and GP000:060) appearing on lines LMB001:381 (Sheets 8 and 9) to be written back into the STM. WE1 (15E3) going inactive sets the EWE1 flip-flop (15F3), causing the RE1 flip-flop (15J3) to be set and the ME1 and NE1 flip-flop (15L2) to be reset. TBB040 (3H7) or NE1 (no error detected) causes the word counter (WA011 and WA001) to be advanced, placing the next word address on lines MWA001 and 011 (9G5) prior to MRE0 (9G1) being reactivated. The STM responds with the second word of data reactivating MRDS0 within 40 nanoseconds after MRE0 has gone active. The word, along with the parity bits, is processed by the ECC circuit and stored into the cache buffer at the next word address; but it is not output onto lines MDS000:310. The processor, having received the first word of data, no longer expects an output from the memory, but is waiting for the memory to go not busy.

This cyclic mode of operation continues until the fourth word has been read from the STM and has been processed. WC0 (15G2) goes active when the word address counter (3N6) has been advanced to the fourth word count, preventing the RE1 flip-flop (15J3) from generating any further MRE0 (9G1) pulses. After processing the fourth word, WCC1 (14J2) goes inactive, causing NCLR1 (13G9) to reset the MB1 flip-flop (13K7). The cache buffer (11H5) now contains the 4-word set that resides in the STM at the tag field address (A080:210), which is stored in the index buffer (12E5) at the location addressed by the index field (A220:270). If none of the four words contained uncorrectable errors, the validation buffer location, as addressed by the index field, is set (valid); otherwise, it is reset (not valid).

18.2.4.2 Cache Hit

A cache hit occurs on a CPU read operation if MIS1 (16L7), NVAL1 (16L8) and PER1 (16L8) do not go active, thereby preventing QWM1, QWM0, and QWE0 from going active. This causes the word of data to be output from the cache buffer (11H5) onto lines D000:310 which are loaded into the ODR (Sheet 2) and output onto lines MDS000:310.

A cache hit occurring on a store fullword or store partial word operation causes the new word stored in the STM to be loaded into the cache buffer. A cache hit occurring on a test error logger operation or read and set operation, and an uncorrectable error being detected on a store partial word operation cause the valid bit to be reset (not valid). Cache operation criteria is provided in Table 18-4.

TABLE 18-4 CACHE OPERATION CRITERIA

LOAD CACHE BUFFER
1. Store Fullword operation with a hit (singleword load) 2. Store Partial Word operation with a hit (singleword load) 3. CPU Read with a miss or cache parity error (quadword load)
RESET VALID BIT (INVALIDATE)
1. Test Error Logger operation with a hit. 2. Read and Set operation with a hit. 3. Store Partial Word operation with uncorrectable error and a hit. 4. Quadword load to cache buffer with uncorrectable error(s). 5. Initialization or power-up of system (invalidates all 64 locations)
SET VALID BIT
1. Quadword load to cache buffer with no uncorrectable errors detected.
LOAD INDEX BUFFER
1. Quadwcrd load

18.2.5 Read Error Logger (Including ECC Description)

The error logger consists of a 16k x 1 (four 4k x 1 RAMs) buffer (10L8), an address multiplexor (10E1), a 16-bit shift register (10K1 and 10G2), a shift address generator (10B3), a syndrome code register (10C8), two Error Status flip-flops (10K4), and control circuitry (Sheet 10).

18.2.5.1 ECC Circuit Description

The Error Check and Correction (ECC) circuitry (Sheets 4 through 7) consists of parity/syndrome generators P000:060 (Sheets 4 and 5); error detector MER0 (5M3); first-level error decoders DA0:7, DB0:7, and DC0:7 (5J7); correction bit decoders EB000:160 (Sheet 6) and EPB000:060; uncorrectable error detector (UCE0) with LED display indicator (7M5 and 7R7); and Exclusive-OR bit correction gates (Sheets 6 and 7). The ECC code implemented provides detection and correction of all single-bit errors and detection of all double-bit error combinations.

The Error Correction Code (ECC) logic is used to generate the proper parity bits (P00:P06) when writing into the STM (LMB32:LMB37) or to check the 39-bit data word read from the STM.

When writing into memory, the data to be written is available on D00:D31. The seven parity bits (UP00:UP06) are forced low. The resulting parity bit (P00:P06) outputs, along with the 32-bit data word, are written to the STM. (Refer to Table 18-5.)

Reading from the STM fetches a 39-bit data word, which is provided on the inputs of the ECC logic (D00:D31 and P00:06). The syndrome output should be all zero if there is no error. (Refer to Table 18-5.) The syndrome output bits (P00:P06) are decoded to correct any single-bit error. Refer to Table 18-6 for decoding the syndrome bits after a read operation.

TABLE 18-5 ERROR CORRECTION CODE (ECC) LOGIC TABLE

1003

PARITY TO BE WRITTEN ON WRITE

DATA TO BE WRITTEN ON WRITE

FORCED LOW ON WRITE

P00:06

D000:310 (LOW ACTIVE BUS)

UP00:06

0	1	2	3	4	5	6	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	0	1	2	3	4	5	6	PARITY TYPE
X							X	X	X		X	X	X		X					X			X					X			X					X	X		X							ODD
	X						X			X	X	X		X		X			X		X			X				X			X					X			X						EVEN
		X						X		X	X		X	X			X		X			X			X		X			X						X	X			X					ODD
			X						X			X	X	X				X		X	X	X				X		X	X	X							X			X				EVEN
				X			X	X	X	X					X	X	X	X					X	X	X	X								X					X			X				ODD
					X										X	X	X	X	X	X	X	X									X	X	X	X	X	X	X					X			EVEN
						X																	X	X	X	X	X	X	X	X	X	X	X	X										X		EVEN

X = BITS USED TO GENERATE SYNDROME

ON READ SYNDROME OUTPUTS SHOULD BE ZERO IF NO ERROR

DATA READ FROM THE STM

EXAMPLE: DATA TO BE WRITTEN = X'00000000' PARITY GENERATED = 1001000

DATA READ AFTER WRITE = X'80000000' PARITY READ = 1001000 SYNDROME RESULT = 1100100 DATA BIT 0 ERROR (SEE TABLE 13-4)

TABLE 18-6 ECC SYNDROME CODE

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION	
0	0	0	0	0	0	0	NE	0	
0	0	0	0	0	0	1	PB6	1	
0	0	0	0	0	1	0	PB5	2	
0	0	0	0	0	1	1	ME	3	
0	0	0	0	1	0	0	PB4	4	
0	0	0	0	1	0	1	ME	5	
0	0	0	0	1	1	0	ME	6	
0	0	0	0	1	1	1	DB28	7	0
0	0	0	1	0	0	0	PB3	8	
0	0	0	1	0	0	1	ME	9	
0	0	0	1	0	1	0	ME	10	
0	0	0	1	0	1	1	DB27	11	
0	0	0	1	1	0	0	ME	12	
0	0	0	1	1	0	1	DB19	13	
0	0	0	1	1	1	0	DB11	14	
0	0	0	1	1	1	1	ME	15	
0	0	1	0	0	0	0	PB2	16	
0	0	1	0	0	0	1	ME	17	
0	0	1	0	0	1	0	ME	18	
0	0	1	0	0	1	1	DB26	19	
0	0	1	0	1	0	0	ME	20	
0	0	1	0	1	0	1	DB18	21	
0	0	1	0	1	1	0	DB10	22	1
0	0	1	0	1	1	1	ME	23	
0	0	1	1	0	0	0	ME	24	
0	0	1	1	0	0	1	DB23	25	
0	0	1	1	0	1	0	DB15	26	
0	0	1	1	0	1	1	ME	27	
0	0	1	1	1	0	0	DB31	28	
0	0	1	1	1	0	1	ME	29	
0	0	1	1	1	1	0	ME	30	
0	0	1	1	1	1	1	ME	31	
0	1	0	0	0	0	0	PB1	32	
0	1	0	0	0	0	1	ME	33	
0	1	0	0	0	1	0	ME	34	
0	1	0	0	0	1	1	DB25	35	
0	1	0	0	1	0	0	ME	36	
0	1	0	0	1	0	1	DB17	37	
0	1	0	0	1	1	0	DB9	38	
0	1	0	0	1	1	1	ME	39	2
0	1	0	1	0	0	0	ME	40	
0	1	0	1	0	0	1	DB22	41	
0	1	0	1	0	1	0	DB14	42	
0	1	0	1	0	1	1	ME	43	
0	1	0	1	1	0	0	ME	44	
0	1	0	1	1	0	1	ME	45	
0	1	0	1	1	1	0	ME	46	
0	1	0	1	1	1	1	ME	47	

TABLE 18-6 ECC SYNDROME CODE (Continued)

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION
0	1	1	0	0	0	0	ME	48
0	1	1	0	0	0	1	DB20	49
0	1	1	0	0	1	0	DB12	50
0	1	1	0	0	1	1	ME	51
0	1	1	0	1	0	0	DB3	52
0	1	1	0	1	0	1	ME	53
0	1	1	0	1	1	0	ME	54
0	1	1	0	1	1	1	ME	55
0	1	1	1	0	0	0	DB7	56
0	1	1	1	0	0	1	ME	57
0	1	1	1	0	1	0	ME	58
0	1	1	1	0	1	1	ME	59
0	1	1	1	1	0	0	ME	60
0	1	1	1	1	0	1	ME	61
0	1	1	1	1	1	0	ME	62
0	1	1	1	1	1	1	ME	63
1	0	0	0	0	0	0	PB0	64
1	0	0	0	0	0	1	ME	65
1	0	0	0	0	1	0	ME	66
1	0	0	0	0	1	1	DB24	67
1	0	0	0	1	0	0	ME	68
1	0	0	0	1	0	1	DB16	69
1	0	0	0	1	1	0	DB8	70
1	0	0	0	1	1	1	ME	71
1	0	0	1	0	0	0	ME	72
1	0	0	1	0	0	1	DB21	73
1	0	0	1	0	1	0	DB13	74
1	0	0	1	0	1	1	ME	75
1	0	0	1	1	0	0	DB2	76
1	0	0	1	1	0	1	ME	77
1	0	0	1	1	1	0	ME	78
1	0	0	1	1	1	1	ME	79
1	0	1	0	0	0	0	ME	80
1	0	1	0	0	0	1	ME	81
1	0	1	0	0	1	0	DB30	82
1	0	1	0	0	1	1	ME	83
1	0	1	0	1	0	0	DB1	84
1	0	1	0	1	0	1	ME	85
1	0	1	0	1	1	0	ME	86
1	0	1	0	1	1	1	ME	87
1	0	1	1	0	0	0	DB6	88
1	0	1	1	0	0	1	ME	89
1	0	1	1	0	1	0	ME	90
1	0	1	1	0	1	1	ME	91
1	0	1	1	1	0	0	ME	92
1	0	1	1	1	0	1	ME	93
1	0	1	1	1	1	0	ME	94
1	0	1	1	1	1	1	ME	95

TABLE 18-6 ECC SYNDROME CODE (Continued)

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION	
1	1	0	0	0	0	0	ME	96	
1	1	0	0	0	0	1	ME	97	
1	1	0	0	0	1	0	DB29	98	
1	1	0	0	0	1	1	ME	99	
1	1	0	0	1	0	0	DB0	100	
1	1	0	0	1	0	1	ME	101	
1	1	0	0	1	1	0	ME	102	
1	1	0	0	1	1	1	ME	103	6
1	1	0	1	0	0	0	DB5	104	
1	1	0	1	0	0	1	ME	105	
1	1	0	1	0	1	0	ME	106	
1	1	0	1	0	1	1	ME	107	
1	1	0	1	1	0	0	ME	108	
1	1	0	1	1	0	1	ME	109	
1	1	0	1	1	1	0	ME	110	
1	1	0	1	1	1	1	ME	111	
1	1	1	0	0	0	0	DB4	112	
1	1	1	0	0	0	1	ME	113	
1	1	1	0	0	1	0	ME	114	
1	1	1	0	0	1	1	ME	115	
1	1	1	0	1	0	0	ME	116	
1	1	1	0	1	0	1	ME	117	
1	1	1	0	1	1	0	ME	118	
1	1	1	0	1	1	1	ME	119	7
1	1	1	1	0	0	0	ME	120	
1	1	1	1	0	0	1	ME	121	
1	1	1	1	0	1	0	ME	122	
1	1	1	1	0	1	1	ME	123	
1	1	1	1	1	0	0	ME	124	
1	1	1	1	1	0	1	ME	125	
1	1	1	1	1	1	0	ME	126	
1	1	1	1	1	1	1	ME	127	

NOTE

PB = Parity Bit
DB = Data Bit
ME = Multiple Bit Error

During a faulty read operation, data from the STM is input to the parity check generators causing one or more parity/syndrome lines P000:060 to go high and activating MER0 (5N2). These lines are also input to the first level decoders (5J5-5J8), whose outputs are further decoded by the correction bit generators (Sheet 6 and 7C3). If a single-bit error is detected, one correction line EB000:160 or EPB000:060 goes high (active), correcting the bit in error. If the error detected was not a single bit error, lines EB000:160 and EPB000:060 remain low (no correction) causing UCE0 (7N3) to go active and latching the address (1 of 4) of the faulty STM in the uncorrected error display (7R7).

18.2.5.2 Error Logger Description

The error logger records all detectable single and multiple bit memory errors (see Table 18-6) in two modes, 8 Mb mode and 16 Mb mode. In 8 Mb mode, the error logger is divided in two with one half covering the lower 4 Mbs of memory and the other half covering the upper 4 Mbs of memory. An error can be detected down to the 16 kth level in 8 Mb mode. In 16 Mb mode, the error logger uses its lower half to cover the entire 16 Mb range, and the upper half is not used. An error can be detected down to the 64 kth level in 16 Mb mode (only 64k RAMs are used in a 16 Mb machine).

BA090 and BA091 (3F1) are used to select which half of the error logger is to be used. These 2 signals are really opposite polarities of the same signal. In 8 Mb mode, BA090/1 are derived from A090 (3C2). In 16 Mb mode, BA090 is forced high and BA091 is forced low. BA090 and BA091 will be referred to as BA09 for simplicity.

Errors are recorded as follows: parity/syndrome lines P000:060 are latched in the syndrome register (10C8) whose outputs S001:051 are steered onto error logger address lines ELA04:11, along with the word address lines WA000 and 010, via the address multiplexors (10D1 and 10D3). Line S061 is used, along with BA09, as the error log RAM chip enable (CE) decode. In 8 Mb mode, BA09 selects between the lower 4 Mb 4k x 1 RAMs, 17k and 14k (10J6 and 10M6), and the upper 4 Mb 4k x 1 RAMs, 16k and 15k (10J6 and 10M8). In 16 Mb mode, 4k x 1 RAMs 17k and 14k are always selected by BA09. S061 selects between the two RAMs selected by BA09, placing all even errors (refer to Table 18-6) into 4k x 1 RAM 17k or 16k, and all odd errors into 4k x 1 RAM 14k or 15k. STM module select lines ELMA11:31 and ERLA01 (10J6, 10J8, 10L6, and 10L8) are input directly to the 4k x 1 RAMs as most significant addresses. ME1 (10H4) and ME0 (10N6), having gone active, cause a low to be written into the address location of the selected RAM, and set either flip-flop 02M (10K4), upper half of the error logger, or flip-flop 05K (10K5), lower half of the error logger. These two flip-flops represent the status of their respective error logger halves.

There are two operations provided for obtaining error logger information, read error logger status and read error logger. Both operations are initiated by sending the read error logger code on lines RD011:31 and setting address bit LMA190 for a read error logger status or resetting address bit LMA190 for a read error logger operation.

A read error logger status operation responds with line MDS160 being set if the error logger contains error information, or reset if no errors have been stored. In 8 Mb mode, LMA090 is used to select between the status for each error logger half; if LMA090 is reset, MDS160 returns status for the lower half of the error logger, and if LMA090 is set, MDS160 returns status for the upper half of the error logger. In 16 Mb mode, MDS160 always returns the status of the lower half of the error logger, and the state of LMA090 is a don't care. The selected status flip-flop (10K4 or 10K5) is always reset when a read error logger status is performed.

A read error logger operation reads 16 consecutive locations of the error logger, returning a halfword on lines MDS160-310. In 8 Mb mode, LMA090 selects between the upper and lower halves of the error logger. Address bits LMA100:180 are steered to the error logger RAMs (10J6, 10J8, 10M6, and 10M8) via the address multiplexor (3E1, 3E3), along with lines AD01:21 from the shift counter (10B3). The contents of eight address locations are read from each 4k x 1 RAM (operated in parallel) of the selected error logger half and loaded into their respective shift registers. Each address location is written back to a one (no error state) before reading out from the next address location. The timing used to perform this operation is derived from system clocks CLK1D and SCLK1A (10A4). After loading the shift registers, their contents are enabled onto lines D160:310, which output onto lines MDS160:310 through the output data register (Sheet 2). AD31 (14J2) going active causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7), readying it to accept the next ER0. RCAR0 (10M3), having gone active, allows the ELDUA1 flip-flop to be reset, removing DUA0 (15N7) and causing LMBY0 (15N8) to be deactivated on the next transition of CLK0D. In 16 Mb mode, everything operates the same except that the lower half of the error logger is always selected, and LMA080:110 and LMA140:180 are steered to the error logger, instead of LMA100:180.

The halfword returned during a read error logger operation is interpreted as follows: each bit in the halfword represents 1 of 16 syndrome codes created by concatinating 4 bits with the 3-bit syndrome field (A160:180) sent to the LBC during the REL instruction. For example, if A16:18 were zeros when the REL instruction was executed, the halfword returned would represent syndrome codes 0000000 - 0001111, where bit 31 represents 0000000 and bit 16 represents 0001111. For every bit in the halfword that is set, an error has occurred with the corresponding syndrome. By using Table 18-6, the type of error can then be determined. The location of a chip in error, for errors that have been determined to be single-bit errors, can then be determined using the module number bits and the word column bits in the address field of the REL instruction (see Table 18-7).

When performing a read error logger or read error logger status operation in 8 Mb mode, address bit LMA080 must be reset. If LMA080 is set, the operation will not be performed and the LBC will reset all bits on MDS160:310. This is not true in 16 Mb mode. Table 18-7 shows the addressing scheme for read error logger and read error logger status operations.

Every time P5 is turned off, the error logger is not powered; this means that every time P5 is turned on, the error logger contains invalid data and its status flip-flops may or may not be set. A read error logger status operation and a read error logger operation must be performed for all error logger addresses in order to clear out the error logger so that valid errors can then be recorded.

TABLE 18-7 ERROR LOGGER ADDRESSING SCHEME

<table>
<tr><td></td><td colspan="12">ADDRESS BUS BITS (LMA)</td></tr>
<tr><td rowspan="3">8 MB MODE</td><td colspan="3">080 090</td><td colspan="4">100 110 120 130</td><td colspan="2">140 150</td><td colspan="3">160 170 180</td><td>190</td></tr>
<tr><td>Read Error Logger</td><td>Must Be Reset</td><td>Set - Upper 1/2 Reset - Lower 1/2</td><td colspan="4">Module No. (0-15)</td><td colspan="2">Word Column (0-3)</td><td colspan="3">Syndrome Bits
S0 S1 S2</td><td>Must Be Reset</td></tr>
<tr><td>Read Error Logger Status</td><td>Must Be Reset</td><td>Set - Upper 1/2 Reset - Lower 1/2</td><td colspan="6">Not Used (Don't Cares)</td><td colspan="3"></td><td>Must Be Set</td></tr>
<tr><td rowspan="3">16 MB MODE</td><td colspan="3">080 090</td><td colspan="4">100 110 120 130</td><td colspan="2">140 150</td><td colspan="3">160 170 180</td><td>190</td></tr>
<tr><td>Read Error Logger</td><td colspan="3">Module No. (0-15)</td><td></td><td colspan="2">Not Used (Don't Cares)</td><td colspan="2">Word Column (0-3)</td><td colspan="3">Syndrome Bits
S0 S1 S2</td><td>Must Be Reset</td></tr>
<tr><td>Read Error Logger Status</td><td colspan="8">Not Used (Don't Cares)</td><td colspan="3"></td><td>Must Be Set</td></tr>
</table>

NOTE

LMA200:310 are not used (don't cares)

18.3 MNEMONICS

The following is a list of the mnemonics used on the LBC board. The meaning and 35-806D08 schematic source of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
A080:A310	Internal address bus lines	Sheet 3
AD01:AD31	Shift counter bits	10C3
BA080	Board Address 8	3F1
BA090/1	Board Address 9	3F1
BMCI0	Buffered memory cycle initiate	9M7
BMVF0	Buffered memory voltage failure line	9M9
BSCLR0	Buffered system clear	9M4
BYP0/1	Cache bypass	16K6,16L8
CAEN0/1	Cache enable flip-flop	16S6
CAR1	Refresh counter carry	13N5
CAWE0	Cache write enable	11E2
CB011:CB031	Control bits	3F8
CH1T1	Cache Hit	12S6
CLK0D	Buffered processor clock	10A4
CLK1C	Processor clock	9L7
CLK1D	Buffered prccessor clock	7N8
CLR0	Cycle steal clear	13D2
CLR0B	Clear DU circuit	15E7
CLTB1	TB timer feedback	16A1
CPER1	Buffered cache parity detect	16R8
CSTRIN00:10	Cycle steal refresh inhibit	13A3
D000:D310	Internal data bus lines	Sheets 2,6,8, 9,10,11
D000A	Test and set bit 0	15K5
D160A	Test and set bit 16	15K6
DA0:DA7	First-level error decode bits	5K6,5K7
DB0:DB7	First-level error decode bits	5K5,5K6
DC0:DC7	First-level error decode bits	5K8,5K9
DERR0	Disable error correction line	5G6
DHW0	Buffered DMA halfword line	3C6
DMAHW0	DMA halfwcrd line	3A6
DMARS0	DMA read and set	3D9
DMARST0	DMA read and set latched	3F9
DPR1	Depower line	13K2
DRFW0/1	DMA read fullword	14E7
DREL1	Data read error logger	14H5
DSFW0	DMA store fullword	14D4
DSHW0	DMA store halfword	14D3
DUA0/1	Data unavailable	15N7

MNEMONIC	MEANING	SCHEMATIC LOCATION
EA0/1	Enable address flip-flop	16S4
EB000:EB310	Data bit correction lines	Sheet 6
ED0/1	Enable data lines	15G1
ELMA00:30	Error logger and module address	3G2, 3F3
EL0	Error logger select line	14G4
ELA04:ELA11	Error logger address lines	Sheet 10
ELDUA0/1	Error logger data unavailable	10G4
ELST1	Error logger status select line	14H5
END1	Standby end flip-flop	13F5
EPB000:EPB310	Parity bit correction lines	Sheet 7
ER0	Memory cycle start	13G7
ERLA01	Error logger address 0	3F1
EWE1	End write enable flip-flop	15F3
FNPM0/1	Nonpresent memory flip-flop	14S5
GDD1	Good data disable flip-flop	15N4
GMVF0	Nonpresent memory or memory voltage fail	9N7
GP000:GP060	Good parity lines	7H2,7H4
HIT0/1	Cache hit flip-flop	12S7
LD01	Error logger RAM output	10K8
LD02	Error logger RAM output	10N7
LDBY01:LDBY31	Load byte	Sheet 14
LDGP1	Load good parity line	14M5
LDOD1	Load output data register	16K9
LMA080:310	Local memory address lines	Sheet 3
LMB001:381	Local memory bus lines	Sheets 3,8,9
LMBY0/1	Local memory busy flip-flop	15N8
MATD0	MAT read and set dirty bit latched	3F8
MATR0	MAT read and set reference bit latched	3F8
MATRSD0	MAT read and set dirty bit	3D8
MATRSR0	MAT read and set reference bit	3D8
MB0/1	Memory busy flip-flop	13K7
MB0A	Buffered memory busy lines	13N7
MB1A	Buffered memory busy lines	13N7
MB1B	Buffered memory busy lines	13N8
MB1C	Buffered memory busy lines	13N8
MCC0	Memory cycle complete line	9G2
MCI0	Memory cycle initiate line	16R5
MDS000:MDS310	Processor data bus lines	Sheet 2
ME0/1	Memory error flip-flop	15L2
MEA000:MEA030	Memory expansion address lines	9G1,4
MER0	Memory error detect line	5N2
MER1	Memory error detect line	5N6
MIS1	Cache index compare line	12S6
MRDS0	Memory read data strobe	9G6

MNEMONIC	MEANING	SCHEMATIC LOCATION
MRE0	Memory read enable control line	9G1
MREF0	Memory refresh line	9G5
MWA001	Memory word address line	9G3
MWA011	Memory word address line	9G5
MWE0	Memory write enable control line	9G3
MX01:31	Memory extension address lines	3H2
NCE0	Noncorrectable error line	7R4
NCLR1	Normal clear line	14R4
NE0/1	No error flip-flop	15N2
NPM0	Nonpresent memory line	14R4
NVAL1	Valid RAM data output	12N3
NVM0	Memory voltage failure signal	9L9
ODD1	Output data disable	16N3
P000:P060	Parity/syndrome bits	Sheets 4,5
PER1	Cache parity error line	11R5
PFSD0/1	P5 shutdown lines	9R4
PRFW0/1	Processor read fullword line	14H5
PSBY0	Processor store byte line	14D2
PSEL1	Processor select line	3A6
PSEL1A	Buffered processor select line	3C6
PSFW0	Processor store fullword line	14D4
PSHW0	Processor store halfword line	14D3
QWE0	Quadword enable line	16S7
QWM0/1	Quadword mode lines	16S8
RCARC	Ripple carry line	10E4
RCLC0/1	STM refresh clear lines	9N5
RCLR0	Internal refresh clear line	13H4
RCT0/1	Refresh clear time select lines	13L4
RD011	ROM data line	3D8
RD021	ROM data line	3D8
RD031	ROM data line	3D8
RDS0/1	Buffered memory read data strobe lines	9M5
RE0/1	Read enable flip-flop	15K3
REF0/1	Refresh mode control lines	13L3
REL1	Read error logger line	14H5
RELA1	Read error logger RAM chip select enable	10E9
REQ1	Cycle steal request flip-flop	13D2
RFA0:RFA7	Refresh address bus	13N5,13K5
RFCTLD0	Refresh counter load	13N6
RFQ1	Refresh queue flip-flop	15L7
RFW1	Read fullword control line	14G6
ROAST1	Read and/or set control line	14H6
RSEL0	Refresh cycle steal select line	13G2
RST0/1	Read and set control lines	14H2

MNEMONIC	MEANING	SCHEMATIC LOCATION
RSTDCD1	Read and set decode	14D1
RURE1	Data bus control line	14M7
S000:S060	Syndrome bit lines	10C7,10C9
SBY1	Store byte control line	14H2
SCLK0A	Buffered processor shift clock	10C4
SCLK1	Processor shift clock	9L8
SCLK1A	Buffered prccessor shift clock	9N8
SCLR0	Systems clear relay contact	13C3
SCLR0B	Buffered systems clear line	13G3
SCLR0C	Buffered systems clear line	13E3
SCLR1B	Buffered systems clear line	13D3
SFW0/1	Store fullwcrd lines	14H4
SHIFT1	Shift register advance line	10G3
SHW1	Store halfwcrd line	14H4
SPW0/1	Store partial word line	14H2,14G1
STB0/1	Standby mode flip-flop	13H2
TA001:TA201	TA timer outputs	Sheet 16
TB001:TB161	TB timer outputs	Sheet 16
TEL0/1	Test error logger control lines	14H2
TGA081:211	Cache tag RAM output lines	12A3,12A5,12A7,12A8
UCE0/1	Uncorrectable error flip-flop	7R4
UDD0/1	Uncorrectable data disable flip-flcp	15L4
UFP1	P5U pullup	13F1
UP000:UP060	Uncorrected parity bit lines	9H8
VAL0/1	Valid bit data input	12H1
WA000/1	Word address counter bits	3M6
WA010/1	Word address counter bits	3M6
WC0	Word counter carry	3M9
WCC0/1	Word counter carry	3M7
WDEN0	Write data enable line	14M9
WE0/1	Write enable lines	15E3
WRT0	Write control line	3A6
WRT0A	Buffered write control line	3C6
WRT1	Buffered write control line	14A3
XRP1	P5 pullup	15N3
XRP2	P5 pullup	14K3
XRP3	P5 pullup	3M8

APPENDIX A
HARDWARE DOCUMENTATION GENERAL DESCRIPTION

1. INTRODUCTION

The hardware documentation system establishes the guidelines for:

- number notation
- part, drawing, and publication identification
- component reference designation
- connector pin numbering
- drawing system

Hexadecimal numbering and equipment identification systems are also explained.

Component reference designations are determined by the logic board layouts. Assigned reference designations are used throughout the text and drawings when referring to components.

All logic boards have one or more header connectors to connect the board to the chassis backpanel. The boards may have one or more front edge cable connectors, allowing the boards to be interconnected. The pin numbering scheme explains the pin callouts for all connectors used.

The drawing system defines the standard format of all drawings. It specifies how net and registers are named and how ICs, flip-flops, and clocked devices are represented. Schematic drawing conventions are described.

2. SCOPE

This appendix enables the digital technician to understand the documentation system. It describes number notation, the part numbering system, and the drawing system, as well as detailed illustrations.

Also included is a cross reference list of Perkin-Elmer Computer Systems Division part numbers and standard industry part numbers for the ICs and transistors found in the equipment.

3. NUMBER NOTATION

Hexadecimal notation is the most common form of number notation used in Perkin-Elmer Computer Systems Division documentation. A single hexadecimal digit represents a group of four binary bits. Table A-1 lists the hexadecimal characters used.

Hexadecimal numbers are preceded by the letter X and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are: X'1234', X'2EC6', X'A340', X'EEFA', and X'10B9'.

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TABLE A-1 HEXADECIMAL CHARACTERS

BINARY	DECIMAL	HEXADECIMAL	BINARY	DECIMAL	HEXADECIMAL	BINARY	DECIMAL	HEXADECIMAL
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	10	A			
0101	5	5	1011	11	B			

4. PART NUMBERING SYSTEM

Perkin-Elmer Computer Systems Division parts, drawings, and publications use a common numbering system. The part number and drawing numbers for drawings which describe the part are related. Figure A-1 shows the part number format. The following paragraphs describe the different fields.

0002

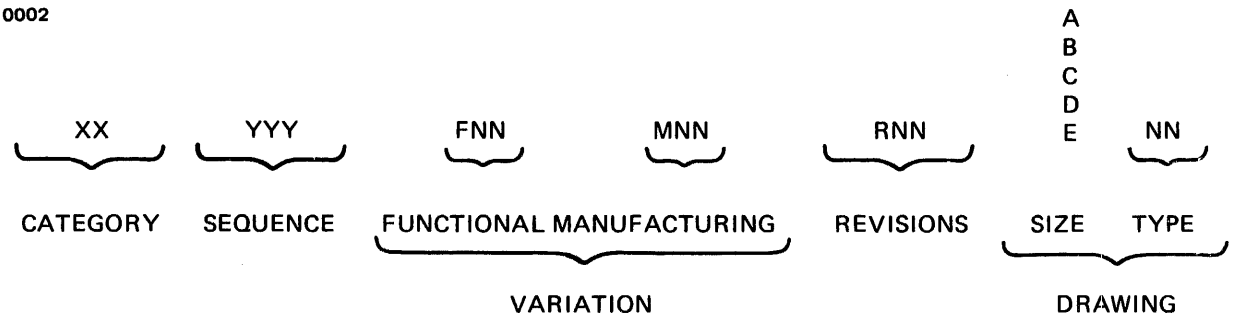


Figure A-1 Part Number Format

4.1 Category Field

The two-digit category number indicates the broad class or category to which a part belongs. Examples of category number assignments are:

01 - basic hardware systems
02 - basic hardware expansions
03 - basic software systems
04 - software packages
05 - microprograms
06 - test programs
07 - subroutines of general utility
10 - spare parts packages
12 - card file assemblies
13 - panels
17 - wire and cables
19 - integrated circuits
20 - transistors
27 - peripheral equipment
29 - manuals
34 - power supplies
35 - assembled printed circuit boards
36 - electro-mechanical devices

4.2 Sequence Field

The sequence number identifies a particular item within the category. Sequence numbers are assigned serially and have no other significance.

4.3 Functional Variation Field

The optical functional variation field consists of the letter F followed by two digits. The F field distinguishes between parts which are not necessarily electrically or mechanically equivalent, but which the same set of drawings describes. For example, a power supply may be internally strapped to operate on either 110 VAC or 220 VAC. With the exception of this strap, all power supplies of this type are identical. A note on the assembly and test specification drawings describes the strapping option.

4.4 Manufacturing Variation Field

The optional manufacturing variation field consists of the letter M followed by two digits.

The M field distinguishes between parts which are electrically and mechanically equivalent (interchangeable), but which vary in manufacture method. For example, if leads are welded instead of soldered on an assembly, the M field changes.

An exception to the M field meaning exists for software related categories. When used in software, the M field number indicates the form in which a particular program is presented. If a program is a set of machine instructions, these instructions may be presented on punched cards, paper tape, or magnetic tape and can be in symbolic, relative, or absolute binary form. Thus, the same program is presented several ways.

The format for the M field and its meaning for software is:

Mxy

where x identifies the media selection (i.e., paper tape, magnetic tape, cassette, etc.) and y identifies object or source and the format.

x		y	
conceptual	0	1	object program standard format 32-bit processor
paper tape	1		
cassette	2	4	memory image
magnetic tape (800 bpi)	3	6	object program standard format 16-bit processor
cards	4	7	object nonstandard format
disk (2.5 Mb)	5	8	object established task
disk (10 Mb)	6	9	source program
magnetic tape (1600 bpi)	7		

These numbers refer to the physical program placed on an approved media for software. A paper tape object program, in standard format for a 16-bit processor, has an M16 identifier. A magnetic tape object program, in standard format for a 32-bit processor, has an M31 identifier.

The following M numbers also have special meaning:

00 conceptual object
91 32-bit object listing
92 programming specifications
95 program description
96 16-bit object listing
98 operating procedures
99 documentation and manuals

4.5 Revision Field

The optional revision field consists of the letter R followed by two digits.

The R field indicates electrical or mechanical changes to a part. It does not change the part's original character. The R field changes often reflect improvements. A part with a revision level higher than the one specified can be used; however, a part with a revision level lower than specified cannot be used.

NOTE

A part number must contain a category number and a sequence number. All other fields are optional.

4.6 Drawing Field

The optional drawing field consists of a letter from A to E followed by two digits. The letter indicates the size of the original drawing. Each letter's size is as follows:

A - 216 mm x 279 mm (8 1/2" x 11")
B - 279 mm x 432 mm (11" x 17")
C - 432 mm x 558 mm (17" x 22")
D - 558 mm x 864 mm (22" x 34")
E - 864 mm x 1118 mm (34" x 44")

The two digits indicate the drawing type:

01 - parts list
02 - machine details
03 - assembly details
05 - art details
06 - wire run list
08 - schematic
09 - test specification
10 - purchase specification
12 - information
13 - program listing
14 - abstracts
15 - program description
16 - operating instructions
17 - program design specifications
18 - flowcharts
19 - product specification
20 - installation specification
21 - maintenance specification
22 - programming specification
24 - application information
25 - functional specifications

Examples

Some examples of the part numbering system follow. The numbers were arbitrarily selected, and in most cases, they are fictitious.

35-060 The sixtieth printed circuit board assigned a part number under this system.

35-060M01 A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in manufacture method.

35-060F01 A printed circuit board not electrically, but mechanically, interchangeable with the 35-060 and described by the same set of drawings.

35-060R01 A revised 35-060 printed circuit board which supersedes the 35-060.

35-060B01 The 279 mm x 432 mm (11" x 17") parts list for a 35-060.

35-060B08 The 279 mm x 432 mm (11" x 17") schematic for a 35-060.

06-072A13 A 216 mm x 279 mm (8 1/2" x 11") listing of the 06-072 test program.

06-072A12 A 216 mm x 279 mm (8 1/2" x 11") information drawing on the 06-072 test program. Probably a part of the program.

29-060 The sixtieth manual assigned a number under this system. This number is not referenced to the part number of equipment described in the manual.

5. DRAWING SYSTEM

This section describes the drawings provided with the equipment. Drawings provided with peripheral devices and other purchased items may vary from the system described in this section. A digital system may be divided into a collection of functionally independent circuits such as memory, processor, and I/O device controllers. These circuits could be saleable units in their own right; electrically, they are self-contained and perform their function with minimum dependence on other functional circuits in the system. Hence, a functional circuit is treated as a building block. Each schematic contains information including type and location of discrete Integrated Circuits (ICs), pin connections, all interconnections within the schematic, connector pin numbers, and connections to other boards. The schematics reflect all the logical operations performed by the circuits. Symbols used on schematics generally conform to MIL-STD-806B.

5.1 Logic Boards

Three logic boards are used in the equipment: half, regular, and oversize. All logic boards contain one or more header connectors to connect the logic board to the chassis backpanel. The boards may contain front edge cable connectors, as required, allowing boards to be interconnected. Component locations on the logic boards are determined by the board layout.

Four standard chassis house the logic boards. The chassis are either 178 mm (7") or 356 mm (14") high and are classified by the number and type of boards they hold.

The chassis and the logic boards they can accommodate are given in Table A-2.

TABLE A-2 CHASSIS/BOARD CONFIGURATIONS

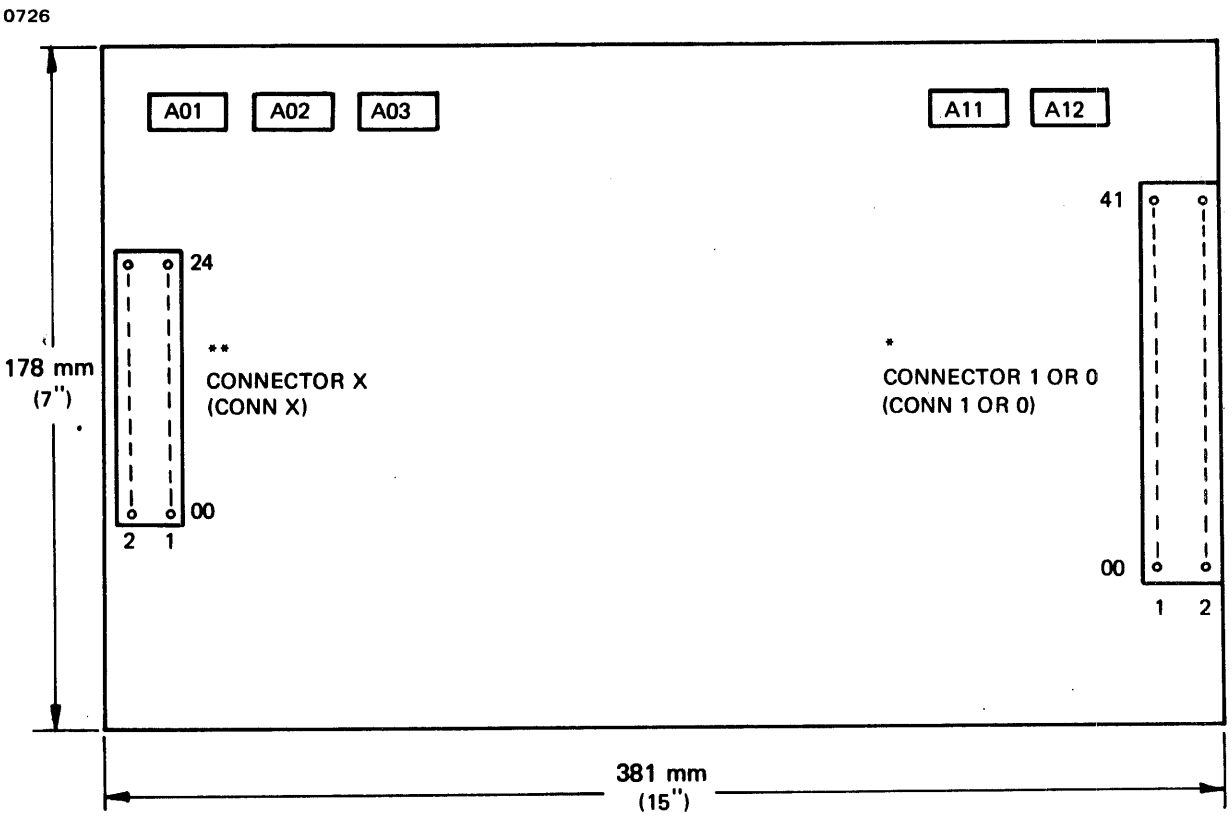
CHASSIS		BOARD MAX. NO. AND TYPE
356 mm (14 inch)	17 slot	11 Oversize, 6 Regular
178 mm (7 inch)	8 slot	8 Regular or 16 Half*
178mm (7 inch)	8 slot	8 Cversize

*MAY BE A COMBINATION CF REGULAR AND HALF-BOARDS

5.1.1 Half-Board Logic Layout

Figure A-2 illustrates a half-board 178 mm (7") logic board layout. Half-boards measure 178 mm x 381 mm (7" x 15") and can be placed in either the right or left half chassis position as required.

With the single header connector 1 or 0 (CONN 1 or CONN 0), components are numbered from left to right, starting in the upper left corner. If a front edge cable connector is required, it is located and numbered as shown in Figure A-2.



*The 178 mm (7") half-board is installed, with an adapter, in either the 1 or 0 side of a chassis slot. The backpanel connector and pins are referenced by the board location, 1 or 0.

**The front edge connector number (X) depends upon the board location in the slot as shown below:

BOARD BACKPANEL CONNECTION	FRONT EDGE CONNECTOR
0	2
1	3

Figure A-2 Half-Board Layout

Two 178 mm (7") half-boards can be inserted into a designated chassis slot via the 16-398 Half-Board Adapter Kit. (See Figure A-3.) Depending on requirements, the half-board adapter kit can strap two active 178 mm (7") boards or one active board and one blank 178 mm (7") board. Wiring does not take place between the boards and the adapter. Due to the adapter's design, the connectors on the board plug directly into the chassis slot backpanel connector.

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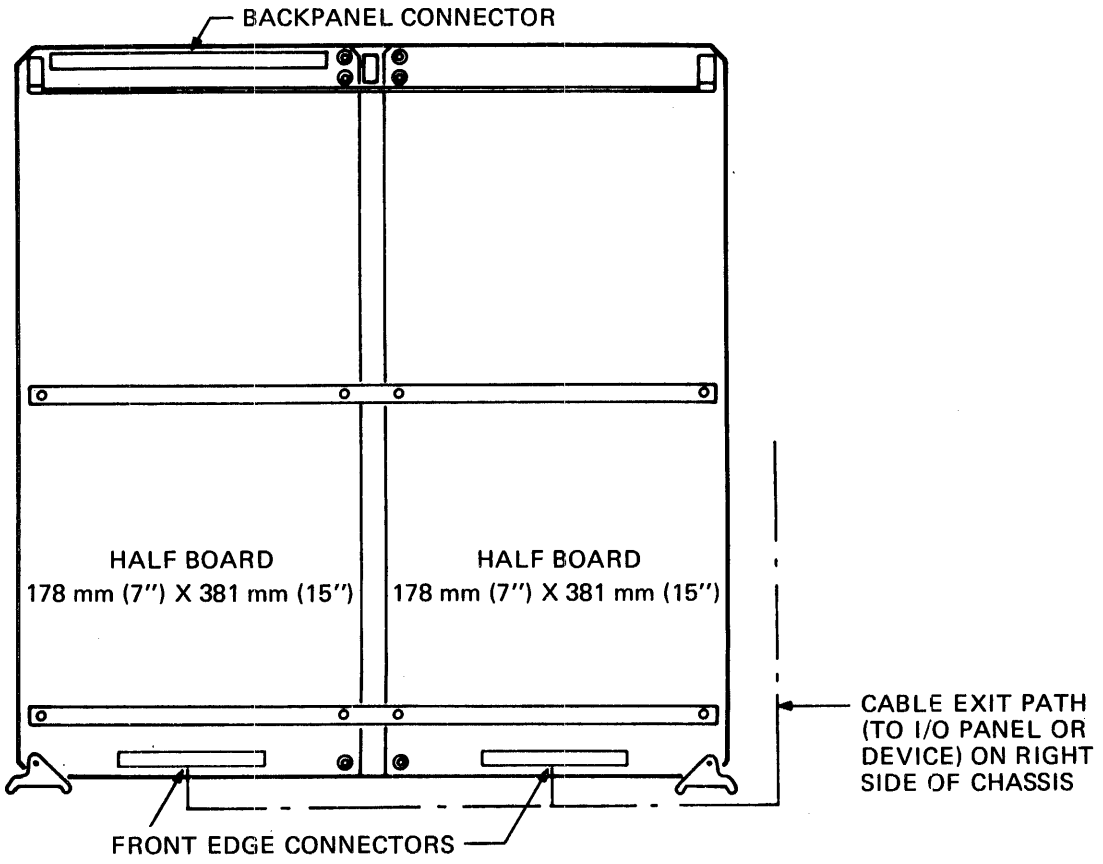


Figure A-3 16-398 Half-Board Adapter

5.1.2 Regular Logic Board Layout

Figure A-4 illustrates a regular logic board layout. Regular logic boards measure 381 mm x 381 mm (15" x 15") with header connectors (CONN 0 and CONN 1) located on the right. The first IC in the upper corner is 01 and the first capacitor is C1. Optional front edge cable connectors (CONN 2 and CONN 3) are located as shown in Figure A-4.

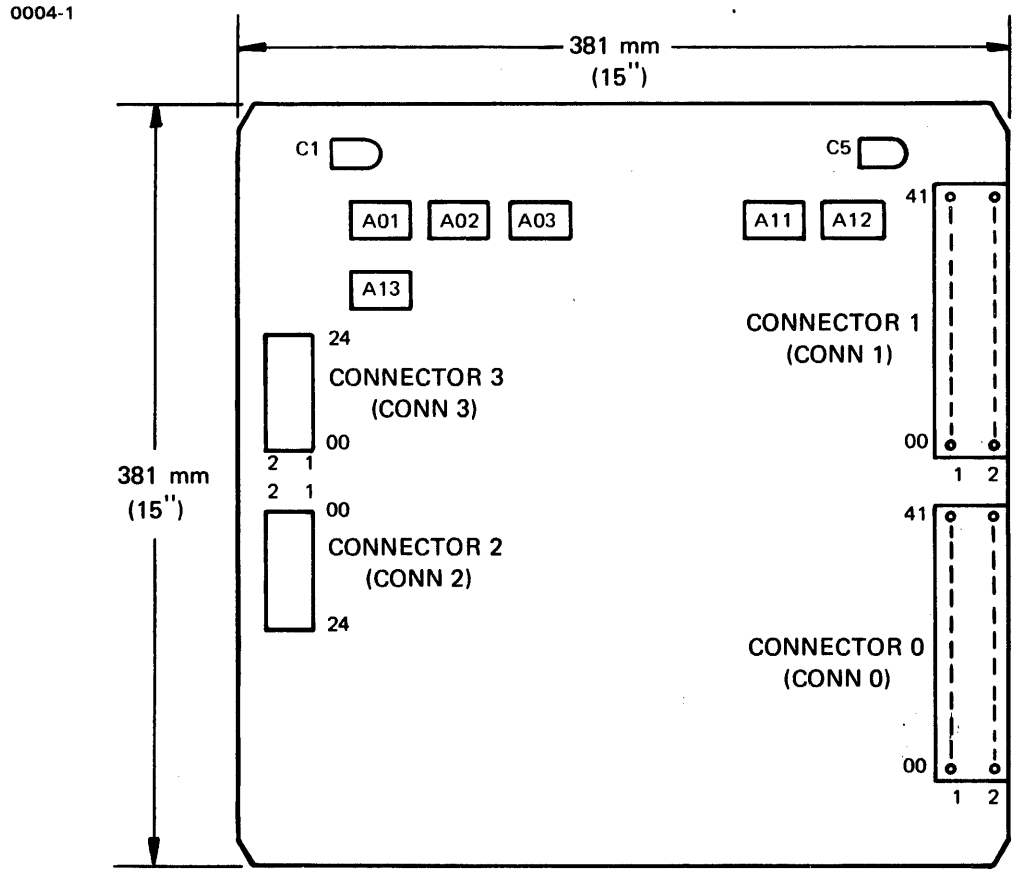
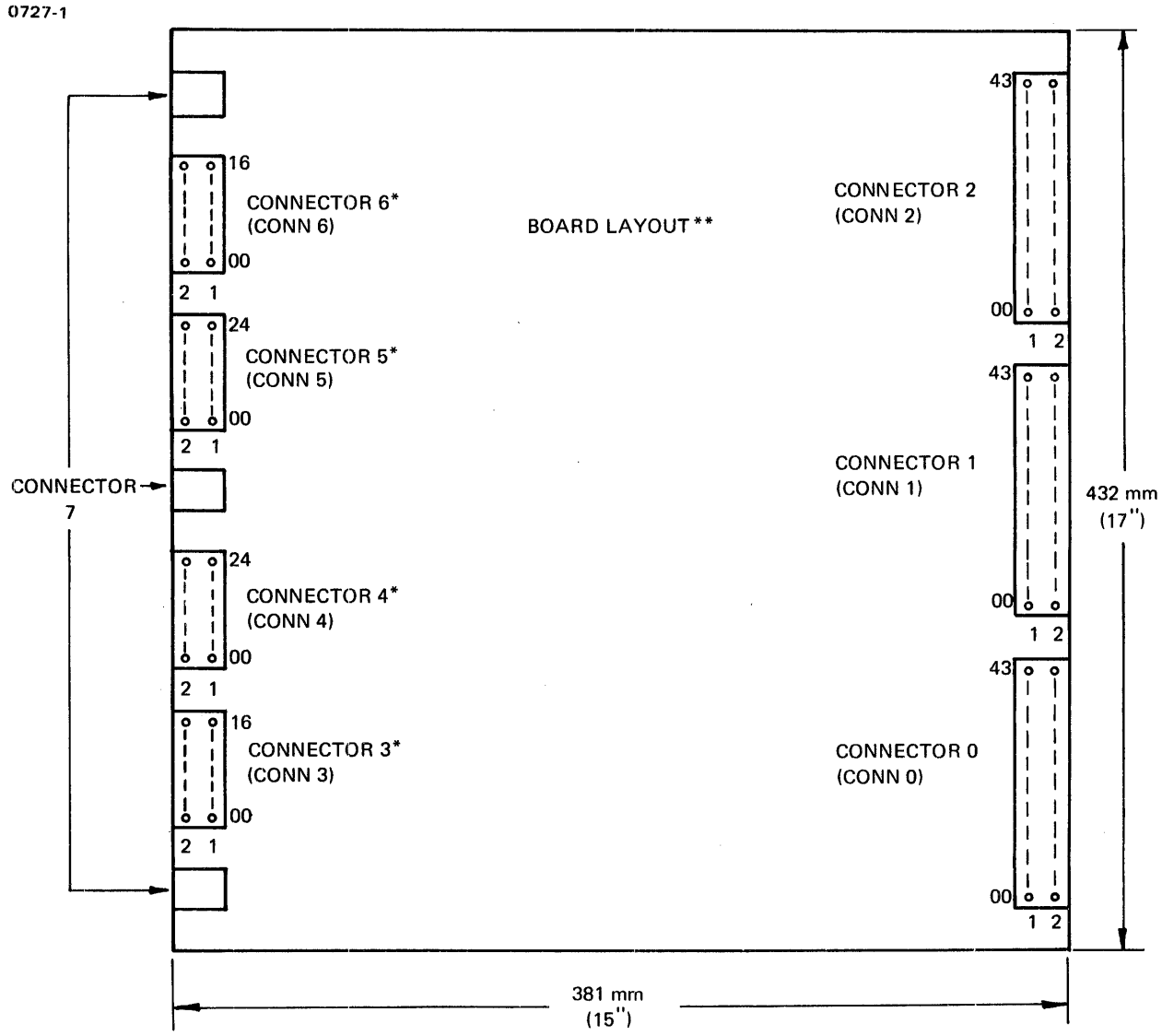


Figure A-4 Regular Logic Board Layout

5.1.3 Oversize Logic Board Layout

Figure A-5 illustrates an oversize logic board layout. Oversize logic boards measure 381 mm x 432 mm (15" x 17"). The boards have three header connectors (CONN 0, 1, and 2). Five front edge connectors (CONN 3, 4, 5, 6, and 7) are located as shown in Figure A-5. For individual board layouts, refer to the related installation manual.



*FRONT EDGE CONNECTORS AS REQUIRED.
**REFER TO APPLICABLE INSTALLATION MANUAL FOR INDIVIDUAL BOARD LAYOUT.

Figure A-5 Oversize Logic Board Layout

5.2 Connector Pin Numbers

Connector pin numbers are identified by a 4-digit number in the format rpp-c,

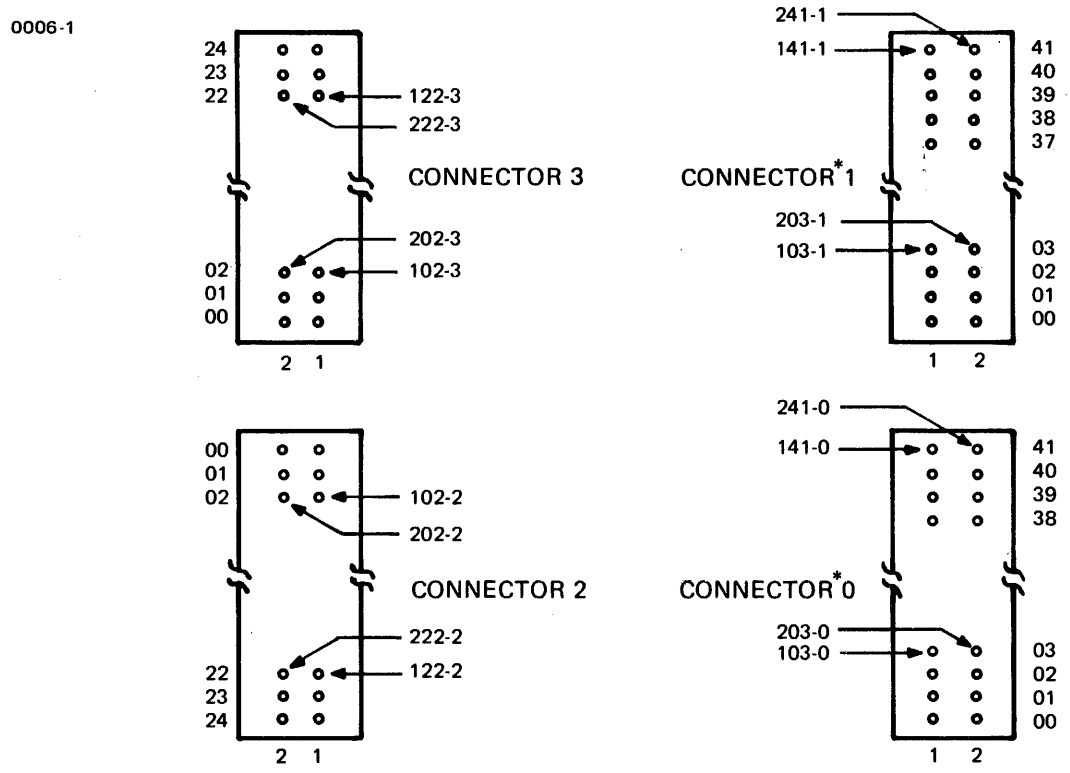
where

r is the row number
pp is the 2-digit pin number
c is the connector number

For example, connector pin number 103-1 refers to the fourth pin (03) in row 1 of connector 1. (See Figure A-6.)

5.2.1 Regular and Half-Boards

Figure A-6 shows the header and front edge cable connector's pin numbering scheme for regular and half boards. Header connectors have two rows of pins, and 42 positions. Front edge cable connectors have two rows of pins, but the pins may vary in the number of positions.



*THE HALF BOARD IS INSTALLED WITH AN ADAPTER, IN EITHER THE 1 OR 0 SIDE OF A CHASSIS SLOT. THE BACKPANEL CONNECTOR AND PINS ARE REFERENCED BY THE BOARD LOCATION, 1 OR 0.

Figure A-6 Regular and Half-Board Connector Pin Numbering

5.2.2 Oversize Boards

Figure A-7 shows the header and front edge cable connector's pin numbering scheme for oversize boards. Header connectors (CONN 0, 1, and 2) have two rows of pins and 44 positions. Front edge cable connectors (CONN 3, 4, 5, and 6) have two rows of pins, but the pins may vary in number. Connector 7 is located in three positions, as indicated.

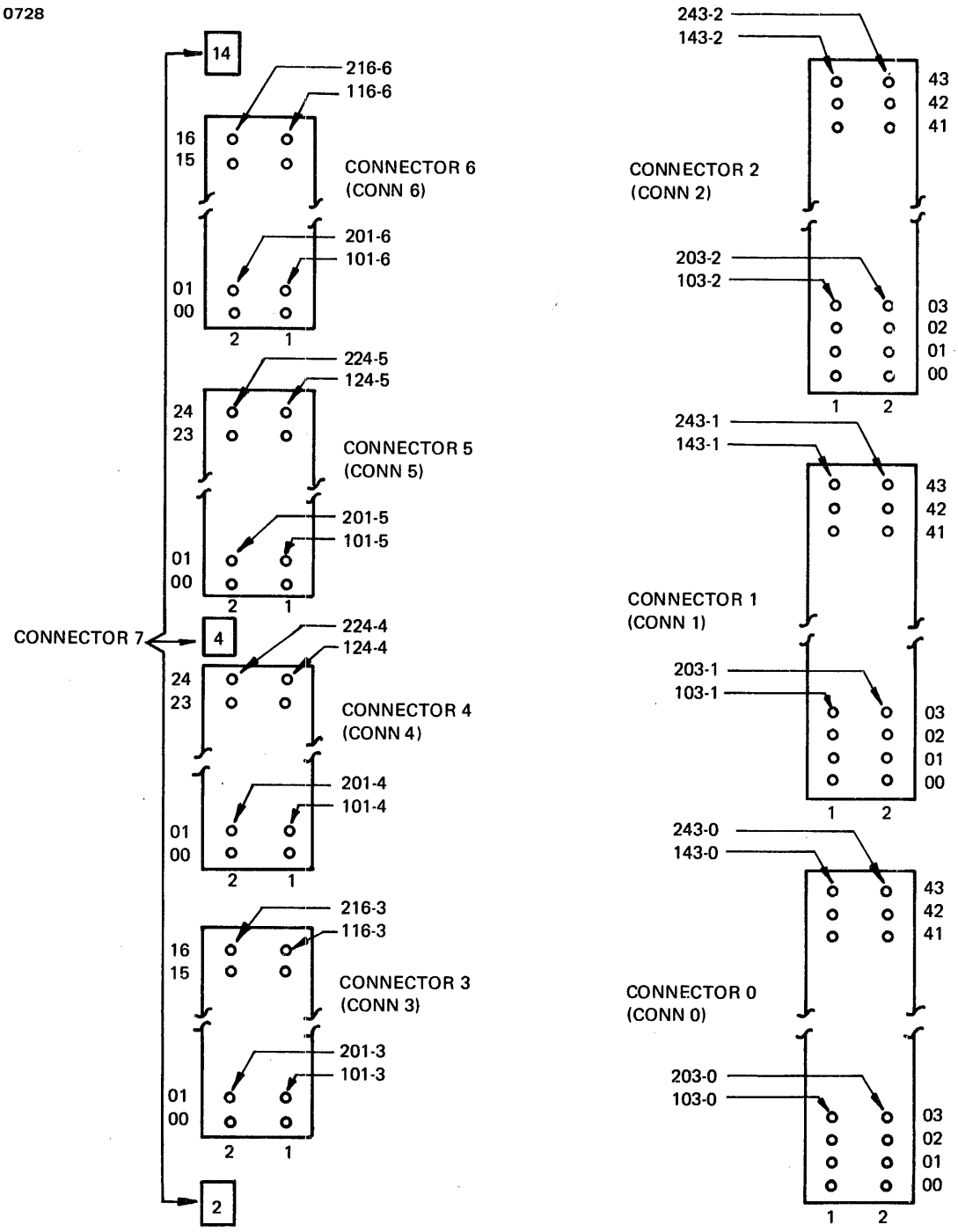


Figure A-7 Oversize Board Connector Pin Numbering

5.3 Register Naming System

The following rules are used to name registers:

1. Mnemonic names are restricted to six descriptors and a state indicator.

2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant positions, and continuing to N-1 cn the right. N is the number of bits in the register.

3. The 00 bit is the Most Significant Bit (MSB) and N-1 is the Least Significant Bit (LSB).

5.4 IC Representation

The ICs mounted directly on the logic board are represented on the schematic drawing by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol mnemonic designation. (See Figure A-8.)

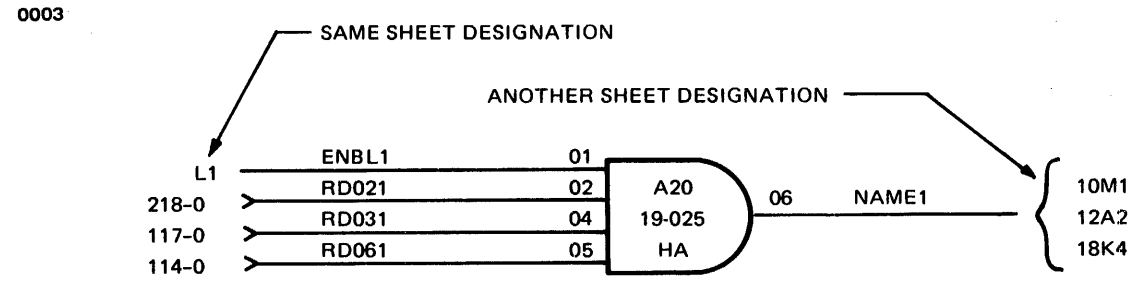


Figure A-8 High Speed AND Gate

The designations, numbers, and references shown in Figure A-8 are:

A20 Shows the component location on the logic board. (Refer to Section 5.1.)

19-025 The number 19 is the category number of ICs and the 025 is the sequence number of the component.

HA — Designates that this component is a high speed AND gate. Other common designators are:

- P - power gate
- SDF - Schottky, D flip-flop
- SG - Schottky gate
- SGO - Schottky high speed gate, open collector
- SBO - Schottky high speed buffer, open collector
- B - Buffer
- SB - Schottky high speed buffer
- LOR - Low power Schottky OR
- LN - Low power Schottky NOR
- SOR - Schottky OR
- SN - Schottky NOR
- SA - Schottky AND
- SF - Schottky J/F flip-flop

L1 — This input lead is from area L1 on the same schematic sheet.

10M1, 12A2, 18K4 — Designate outputs to other logic schematic sheets.

218-0, 117-0, 114-0 — Designate inputs from connector 0.

Pin numbers 01, 02, 04, 05, and 06 correspond directly to the actual IC pin numbers.

5.5 Flip-Flops

When possible, the immediate output from a flip-flop (1 or 0 side) has a mnemonic name preceded by an F. Usually, a flip-flop named PSEL (Processor Selected) has an output mnemonic on the 0 side of FPSEL0. (Refer to Figure A-9.) Thus, when observing a mnemonic at the terminal end of a net, the digital technician has an indication that the signal is the output from a flip-flop rather than a decoded function.

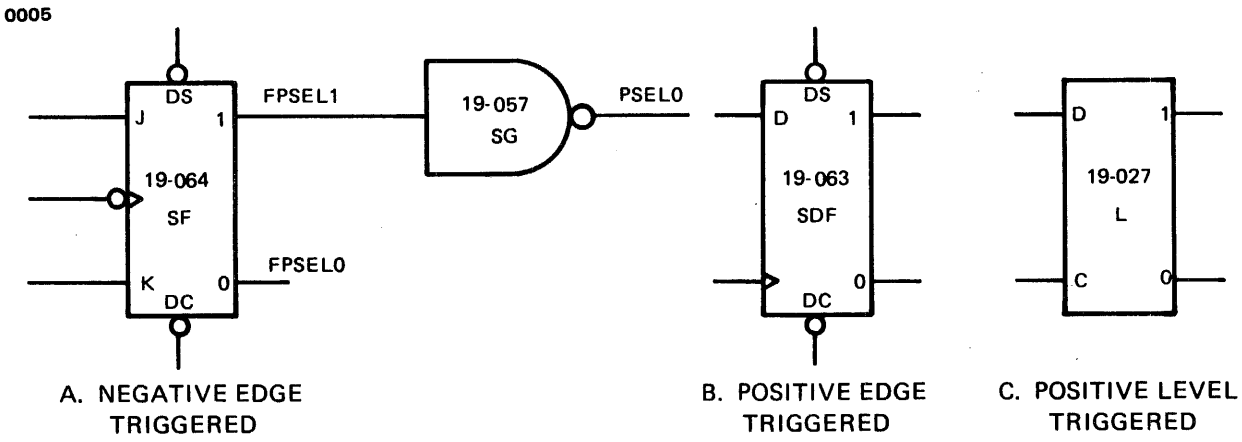


Figure A-9 Clocked Devices

5.6 Clocked Devices

Clocked devices, flip-flops, and counters in particular, are drawn to indicate information concerning their inputs. An input, having a circle adjacent to the pin designation, implies that a low active signal is needed to perform the specified operations. The symbol > at the clock input shows that the device changes state on an edge. If no circle is present, the chip is positive edge triggered. (Refer to Figure A-9.)

5.7 Nets

A net is an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end, usually a collector where the signal is generated, and one or more terminating ends. It is often convenient to assign descriptive mnemonic names to nets to identify them on schematics. Whether or not a net is named is arbitrary; however, a net is always assigned a name if:

1. The net is contained on one drawing sheet; but it is not a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

If a net is named, the following rules apply:

1. Except in special cases, mnemonic names are a maximum of six characters plus a state indicator.

2. No other characters are permitted.

3. Where possible, mnemonics are descriptive; however, descriptive names are not always possible and the danger of misinterpreting a mnemonic exists.

4. A mnemonic name can be assigned to only one net.

5. A state indicator suffixes every mnemonic. This indicator consists of the digit 1, for the logically true state, or the digit 0, for the logically false state. For example, the set side of a flip-flop normally has 1 state indicator; the reset side normally has the 0 state indicator. The state indicator for a function changes each time that function is inverted. Thus, the state indicator permits assigning the same mnemonic to functions that are identical except for an inversion. Logic 0=.5 VDC or less, logic 1=2.4 VDC or more.

6. When a logical function is inverted, an inversion indicator is added after the state indicator allowing for functionally equivalent, but electrically different nets to have the same mnemonic name. Assume a signal NAME1 may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

If a net fans out to many sheets of a schematic or to sheets on different schematics, it is assigned a mnemonic name and zoned from sheet to sheet. This zoning allows for proper identification of the originating and terminating ends of the net. The originating end of a net is the driver where a signal is generated. Terminating ends are all other points to which the net connects. When a lead leaves a sheet at the originating end, it is zoned by first indicating the sheet on which the net reappears. Assume that the gate shown in Figure A-8 is on schematic Sheet 20. The output NAME1 appears on Sheet 10, 12, and 18 of the schematic. The schematic number is implied. When a net enters a sheet from another sheet, it is labeled with the same mnemonic name and is only zoned back to the originating end of the net. In Figure A-8, the ENBL1 may have many other terminations in addition to the one shown. When a net leaves the sheet where it originates, it is generally zoned to every other sheet where the net terminates; the terminating end is zoned only to the originating sheet. On schematics, signals are coordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the backpanel map must be used.

When a lead leaves a logic board, it usually leaves through a logic board backpanel connector pin. Even if the complete net is on one drawing sheet, these connector pins must be shown on the schematic. Since the logic board location number, either in the logic symbol or the footnote, implies the connector number itself, only the connector pin number must be indicated under the pin symbol. In Figure A-8, RD061 enters the logic board on pin 114 of header connector 0.

5.8 Schematics

Figure A-10 is a schematic sheet with call-outs of the described conventions. The schematic drawings for a basic digital system are located in the rear of the appropriate digital system maintenance manual. Schematic drawings for other expansions are included with the expansion or with the publications which describe the expansion.

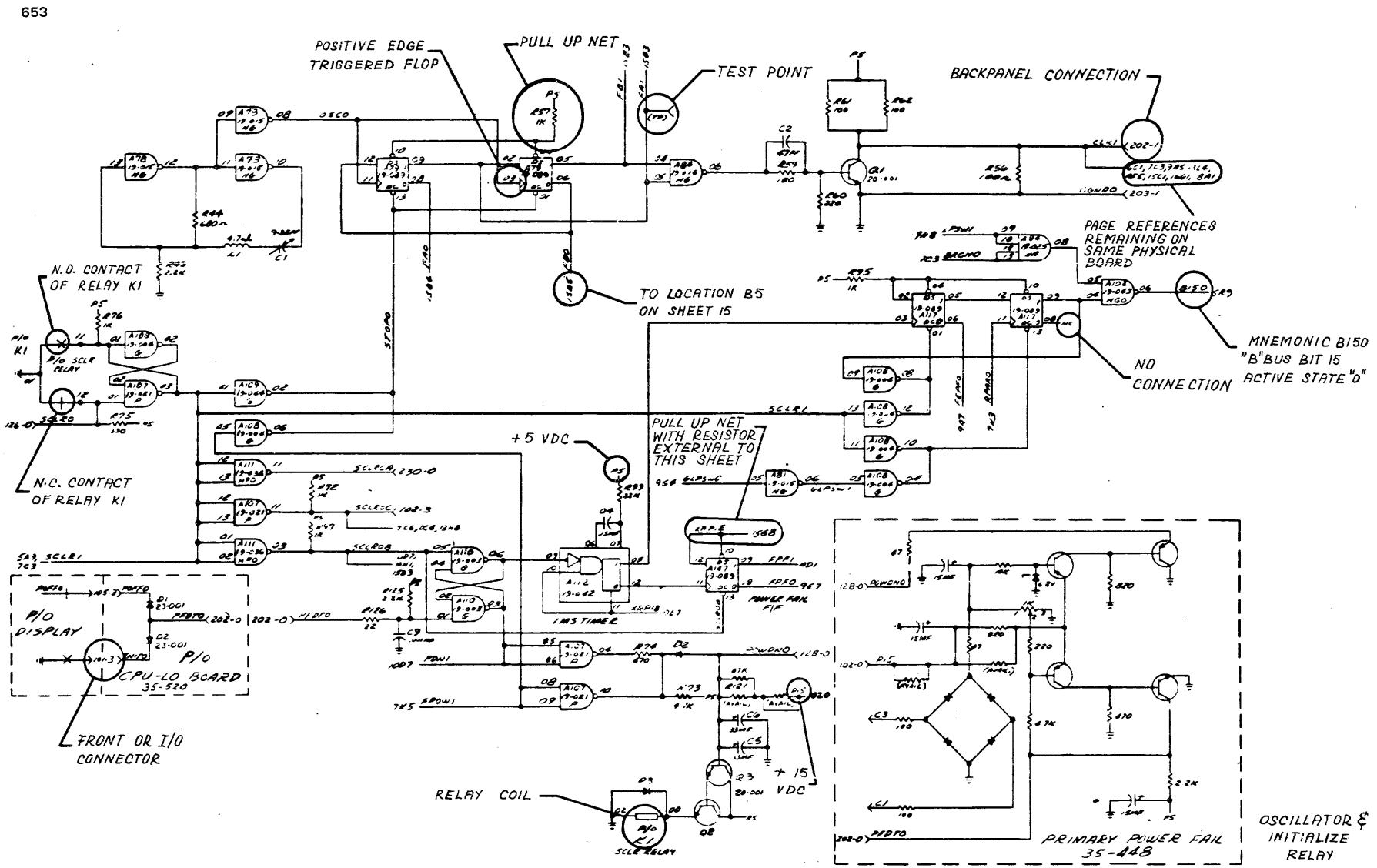


Figure A-10 Functional Schematic Format Drawing

6. PART NUMBER CROSS REFERENCE LIST

Part No.	Type	VENDOR/JEDEC Number
19-001	Dual 4 Input NAND DTL	861*
19-002	Triple 3 Input NAND DTL	863
19-003	Quad 2 Input NAND DTL	849
19-004	Hex 1 Input NAND DTL	837
19-005	Dual Power Gate DTL	844*
19-006	Dual Buffer DTL	832*
19-007	Flip-Flop DTL	848*
19-008	Gate Expander Dual 4 Input DTL	833*
19-009	8 Bit Stack DTL	930*
19-010	Differential Comparator LIN	710C
19-012	Dual 4 Input NAND Buffer TTL	74H40
19-013	Quad 2 Input NAND DTL	946
19-014	Dual J-K FLip-Flop DTL	855*
19-015	Hex Inverter 1 Input	74H04
19-016	Quad 2 Input NAND TTL	74H00
19-017	Triple 3 Input NAND TTL	74H10
19-018	Dual 4 Input NAND TTL	74H20
19-019	Single 8 Input NAND TTL	9007*
19-020	Cperational Amplifier LIN	1709*
19-021	Quad 2 Input Power DTL	1644*
19-022	Dual J-K Flip-Flop TTL	3061*
19-023	Selected Dual Buffer 19-006 with 20-30 nanosecond delay DTL	932*
19-024	Triple 3 Input AND TTL	74H11
19-025	Dual 4 Input AND TTL	74H21
19-026	2-2-2-3 Input AND/OR TTL	74H52
19-027	4 Bit Adder TTL	7475
19-028	4 Bit Serial Adder TTL	7483
19-029	Quad Exclusive - OR TTL	7486
19-030	4 Bit Shift Register TTL	7495
19-031	One Shot TTL	74121
19-032	1 of 10 Decoder Open Collector	74145
19-033	Dual Sense Amplifier LIN	7524
19-034	Retriggerable One Shot TTL	74122
19-035	4 Bit Up/Down Counter TTL	74193
19-036	Quad 2 Input Open Collector TTL	7438
19-037	High Performance Operational Amp	748393
19-038	Dual 4 line to 1 line Mux TTL	74153
19-039	4 Bit ALU TTL	74181
19-040	4 Stage Look Ahead Carry TTL	74182
19-041	4 x 4 Register Stack TTL	74170
19-042	Dual Retriggerable One Shot TTL	74123
19-043	Quad 2 Input NAND Open Collector	74H01
19-044	Hexadecimal Inverter Open Collector TTL	74H05

*Obsolete

Part No.	Type	VENDOR/JEDEC Number
19-045	Dual J-K Flip-Flop TTL	74H106*
19-046	Quad RS-232C Line Driver	ML1488
19-047	Quad RS-232C Line Receiver	MC1489A
19-048	8 Bit Shifter 24 Pin DIP	74198
19-049	1024 Bit PROM TTL	DM8587
19-050	8 Input NAND TTL	74H30
19-051	1024 Bit PROM TTL	74187
19-052	Dual 4 Input Buffer	832*
19-053	4 2-line-to-1-line Data Sel. Mux	74157/9322
19-054	Quad 2 Input NAND STTL	7400
19-055	Quad 2 Input NAND STTL	74S00
19-056	Quad 2 Input NAND Open Collector STTL	74S03
19-057	Hex 1 Input Inverter STTL	74S04
19-058	Triple 3 Input NAND STTL	74S10
19-059	Triple 3 Input AND STTL	74S11
19-060	Dual 4 Input NAND STTL	74S20
19-061	Dual 4 Input Buffer STTL	74S40
19-062	2-2-3-4 Input AND/OR Inverter STTL	74S64
19-063	Dual D Edge Triggered Flip-Flop STTL	74S74
19-064	Dual J-K Flip-Flop STTL	74S112
19-065	Quad 2:1 Mux Non-Inverting STTL	74S157
19-066	Quad 2:1 Mux Inverting STTL	74S158
19-067	4 Bit ALU STTL	74S181
19-068	4 Stage Carry Lcok Ahead Carry STTL	74S182
19-069	8 line to 1 line Mux STTL	74151
19-070	4 Bit Synchronous Counter TTL	74161
19-071	Quad D Edge Triggered Flip-Flop	74175
19-072	4 Bit Left/Right Shift Register TTL	74194
19-073	Dual 4:1 Mux Tri-State TTL	8214(NAT)
19-074	8 Bit Priority Encoder TTL	9318(F)
19-075	16 x 4 Register Stack TTL	3101(INT)
19-076	1024 Bit Memory MOS	TM54062
19-077	256 Bit Memory TTI	6531(MON)
19-078	Dual 4 Input NAND Cpen Collector	74S22
19-079	Comparator Dual	NE5211
19-080	1024 Bit PROM TTL	82S29(SIG)
19-081	Univ. Asynchronous Receiver/ Transmitters	TR1042A
19-082	2-2-3-4 Input AND/OR Invert Open Collector STTL	74S65

* Obsolete

Part No.	Type	VENDOR/JEDEC Number
19-083	9 Bit Parity Generator/Checker STTL	82S62(SIG)
19-085	Timer	MC1555
19-086	741 C DIP Operational Amplifier	741
19-087	747 DIP Operational Amplifier	747
19-088	733 C DIP Operational Amplifier	733
19-089	Dual D Edge Triggered Flip-Flop	74H74
19-090	High Speed (710) Differential Comparator DIP	710
19-091	Retriggerable Single One Shot	9600
19-092	Negative Voltage Regulator	1463
19-093	Positive Voltage Regulator	1469
19-094	Positive Voltage Regulator	723
19-095	Linear Positive Voltage Regulator	805
19-096	First In-First Out Serial Memory 64 Word 4 Bit	3341
19-097	Amplifier	LH0002* (RES)
19-098	Quad 2:1 Multiplexor Non-Inverting	74157
19-099	Dual Sense Amplifier Inverting	75234
19-100	Dual Driver 8 Pin DIP	75452
19-101	Quad-2 Input Positive NAND Buffer	7437
19-102	6-1 Input Buffer/Buffer Open Collector	7407
19-103	1 of 10 Decoder	7442
19-104	Current Switch Memory Driver	75325
19-105	Dual Differential Driver	75114/ 9614
19-106	Dual Differential Receiver	75115/ 9615
19-107	Dual Sense Amplifier	7520
19-108	Quad 2 Input NAND	7400
19-109	Hex Inverter Buffer Driver Open Collector	7406
19-110	Hex Inverter	7404
19-111	Dual 4 Input NAND Buffer	7440
19-112	Optically Coupled Isolator	4N25
19-113	360 Dual Line Driver	75123
19-114	360 Triple Line Receiver	75124
19-115	Quad 2 Input AND TTL	74H08
19-116	Dual 4:1 Multiplexor STTL	74S153
19-117	4 Bit Magnitude Comparator STTL	74S85
19-118	Quad Bus Transceiver TTL	26S12A
19-119	Expandable AND/CR Invert TTL	74H55
19-120	Dual Timer	NE556
19-121	Matched Pair 19-085 (P.S. Timing)	MC1555

* Obsclete

Part No.	Type	VENDOR/JEDEC Number
19-122	1024 Bit PROM TTL	SEE 19-051
19-123	Dual Voltage Controlled Oscillator	74S124
19-124	4-2 Input NAND Buffer STTL	74S37
19-125	4-2 Input NAND Buffer STTL	74S38
19-126	Dual 2 Wide 2 Input AND/OR Inverter STTL	74S51
19-127	4-2 Input Exclusive OR STTL	74S86
19-128	13 Input NAND, 3-State STTL	74S134
19-129	3 to 8 Line Decoder STTL	74S138
19-130	2-4 Input NAND 50 Ohm Line Driver STTL	74S140
19-131	4D FF STTL	74S175
19-132	4 2/1 Mux STTL	74S258
19-133	4 Bit Binary Full Adder TTL	74283
19-134	Hexadecimal Buffer/Inverter TTL	8T98
19-135	4 Bit Binary Counter STTL	(98S16)
19-136	1 of 10 Decoder HS & HV	74145
19-137	Dual Peripheral Positive OR Driver 8 Pin DIP	75453(SIG)
19-138	Character General	2513
19-139	Driver/Decoder	7447AN
19-140	8 Bit Latch	9334PCQM
19-141	Multi-Port Register	9338PCQM
19-142	1024 Bit PROM TTL	SEE 19-080
19-143	4K x 1 NMOS RAM	9050
19-144	4-Hysteresis Rec	8T380
19-145	Voltage Regulator +15 500 Milli-amperes	78M15AUC
19-145F01	Voltage Regulator +12 500 Milli-amperes	78M12AUC
19-145F02	Voltage Regulator -15 500 Milli-amperes	LM340T-15
19-146F00	Voltage Regulator -15 500 Milli-amperes	79M15/ LM320T-15
19-146F01	Voltage Regulator -12 500 Milli-amperes	79M12/ LM320T-15
19-146F02	Voltage Regulator -2 500 Milli-amperes	79M05
19-146F03	Voltage Regulator -5 500 Milli-amperes	7905/ LM320T-5
19-147F01	8 Channel Analog Mux	H11-181A-5
19-147F02	8 Channel Analog Mux	Analog Devices A07503JN

Part No.	Type	VENDOR/JEDEC Number
19-148	Voltage Follower	LM310D
19-149	High Speed Op Amp	HA2-2525-5
19-150	2 Channel Analog Switch	DG1828A/ IH5048 CTW
19-151	Low Level Inst Amp	AD521JD
19-152	Linear Amp	BB3660J
19-153	4-2 Input NAND LPTTL	74LS00
19-154	Hex Inverter LPTTL	74LS04
19-155	3-3 Input NAND LPTTL	74LS10
19-156	2-4 Input NAND LPTTL	74LS20
19-157	8 Input NAND LPTTL	74LS30
19-158	4-2 Input NOR LPTTL	74LS02
19-159	4-2 Input OR LPTTL	74LS32
19-160	4-2 Input AND LPTTL	74LS08
19-161	3-3 Input AND LPTTL	74LS11
19-162	2-4 Input AND LPTTL	74LS21
19-163	4-2 Input NAND Schmitt Trigger LPTTL	74LS132
19-164	4-2 Input NAND Buffer LPTTL	74LS37A
19-165	2-D FF LPTTL	74LS74
19-166	2-JK FF LPTTL	74LS112
19-167	4-D FF LPTTL	74LS175
19-168	3 to 8 Decoder Demux LPTTL	74LS138
19-169	Hex Inverter Open Collector LPTTL	74LS05
19-170	4-2 Input NAND Open Collector LPTTL	74LS03
19-171	Dual Multivibrator	74LS123
19-172	4-2 Input Exclusive OR LPTTL	74LS86
19-173	8 to 1 AND/OR Invert Mux LPTTL	74LS151
19-174	4-2 Input AND/OR Mux LPTTL	74LS257
19-175	4-2 Input AND/OR Mux LPTTL	74LS157
19-176	4-2 Input Mux LPTTL	74LS258
19-177	4-1 Input AND/OR Mux LPTTL	74LS153
19-178	3-3-2-2 Wide AND/OR Inverter LPTTL	74LS51A
19-179	4-3-3-2 AND/OR Inverter LPTTL	74LS54
19-180	4 Bit Counter LPTTL	74LS161
19-181	4 Bit Up/Down Counter LPTTL	74LS193
19-182	4 Bit Left/Right Shift Register TTL	74LS194
19-183	2-Line Driver	75110
19-184	4 Bit Micro Controller	AMD2901
19-185	4K-Bit ROM	N82S115
19-186	4K-Bit PROM	82S215N
19-187	Quad 2:1 Mux with Storage LPTTL	74LS298
19-188	ROM Chip Programmed In House 16 Bit LSU	
19-189	ROM Chip Programmed In House 32 Bit LSU	

Part No.	Type	VENDOR/JEDEC Number
19-190	Quad Comparator	LM339
19-191	Quad 2-Input NOR Gate	CD4001AE
19-192	Dual D Flip Flop	CD4013AE
19-193	1024 Bit PROM TTL	SEE 19-051
19-194	2K PROM TTL	N82S131
19-195	2K PROM TTL	SEE 19-051
19-196	Quad 2 Input 3 State Mux. Non Inverting	74S257
19-197	1024 B Dynamic RAM (NMOS)	MK4096N-16
19-198	Field Programmable Logic Array	82S00
19-200	16 x 4 First In-First Out (FIFO)	9430
19-201	6800 Micro-Processor	MC6800
19-202	Peripheral Interface Adapter (PIA)	MC6820
19-203	Sync Serial Data Adapter (SSDA)	MC6852
19-204	1K RAM	MCM6810A
19-205	2 Phase Clock	MC6870A
19-206	4 Input 3 State Line Transceiver	8T26/ 8T26A
19-207	Error Checking, Polynomiad Gen.	MC8506P
19-208	Dual VCO	MC4024P
19-209	Phase Frequency Detection	MC4044
19-210	Micro-Processor	2608-1/ MCM6830P
19-214	Asynchronous Communication Interface Adapter	MC6850
19-215	Differential Line Driver	AM26LS31
19-216	Differential Line Receiver	AM26LS33
19-217	Tri-state Line Driver/Receiver	
19-218	1024 x 1 Bi-Polar RAM	74S214A
19-219		82S181A
19-220	1024 x 8 PROM	82S181A
19-221	16,384 x 1 MOS RAM	MK4116P-2
19-222	Over-Voltage Protector	MC3423U
19-223	9 Bit Even/Odd Parity Generator/ Checker	74S280
19-224	Octal Flip-Flop	74LS377
19-225	Line Driver/Receiver	74LS244
19-226	Refresh Counter	3242
19-227	Hex Flip-Flop	74LS174
19-228	4096 x 1 MOS RAM	MK4027-2
19-229	Tri-state Hex Buffer	8T97
19-230	Shift	74S350
19-231	D Register	MC2918
19-232	8 Bit Latch	74S373
19-233	Octal Flip-Flop	74S374
19-234	Quad 2 Input NOR Gate	74S02
19-235	Quad 2 Input OR Gate	74S32
19-236	Quad 2 Input AND Gate	74S08
19-238	10 Volt Precision Reference	AD581JH
19-239	Baud Rate Generator	

Part No.	Type	VENDOR/JEDEC Number
19-240	Octal Bus Driver	74S241
19-241	Dual 5 Input NOR Gate	74S260
19-242	Optically Coupled Isolator	MCT273
19-243		
19-244	ROM	702,703 (Centronics)
19-245		
19-246	Reg Pulse Width Modulator	SG3524
19-247	3 Term Reg 1 Amp	SG78XXCK UA78XXKC
19-248	3 Term Reg 1 Amp	UA78L12, UA78C12ACDB, LM78L12AHC
19-249	Digital Delay Module	212XX(Pulse), DL-18XX(Valor)
19-250	Dual Mono Multivibrator	74221, SN74221
19-251	Hex Invert/Hysteresis	SN7414
19-252	1KX1 RAM (MOS)	2125AL, 93L425XC
19-253	2KX8 Bipolar PROM	3636-1, 76161-5
19-254	256 x 9 RAM	93479XC, N82S212
19-255		
19-256	Xtal Clock Osc.	XO-33C20 (Dale), 7401-308, 20MHZ (Spectrum)
19-258	P NAND Gate/Invert	SN74S133
19-259	2-4 Decoder/Demux	SN74S139
19-260	2-4 Decoder/Demux	SN74LS139
19-261	8-3 Encoder	SN74LS148
19-262	Octal Buffer/3 State Output	SN74LS240
19-263	Octal D Type Flip-Flop	SN74LS374
19-264	256 x 4 RAM	93422
19-265	256 x 4 RAM	93L422
19-266	4 x 4 Register File	SN74LS170
19-267	Optically Coupled Isolator	TIL102
19-268	4096 Bit High Speed RAM	52147 (Amer,Micro)
20-001	Transistor NPN High Speed Switch	2N3646
20-002	Transistor PNP 500 MA	MPS6534
20-003	Transistor	DT5-423/ 2N3902
20-004	Transistor NPN	2N5189/ 64493
20-005	Transistor	2N3056

Part No.	Type	VENDOR/JEDEC Number
20-006	Transistor NPN 15 Amps 100W T03 Case	2N3055
20-007	Transistor NPN 3 Amps	TIP31A
20-008	Transistor PNP 3 Amps	TIP32A
20-009	Transistor Triac 2 Amps 100V	A03001
20-010	Transistor NPN 500 MA Code Driver	2N5845/ 2N5845/ 74659A
20-011	Transistor Phcto	2N5777
20-012	Transistor PNP High Current Switch	2N2907/ TS3413
20-013	Transistor NPN	2N3302
20-014	Transistor NPN	2N4238
20-015	Transistor PNP	2N4235
20-016	Transistor PNP	2N3740
20-017	Transistor NPN	2N3766
20-018	Transistor, Power Silicon NPN	2N3054
20-019	Transistor	2N6038
20-020	Transistor Switching 1 Amp T05 can	2N3725
20-021	Transistor NPN Silicon	MPS3646
20-022	Transistor NPN	2N1711
20-023	Transistor PNP	2N905A/ J2N2905A
20-024	Transistor Switch	2N3776
20-025	PNP High Speed Switch	2N3467
20-026	Transistor Module, Quad	FSQ1079/ FPQ3724
20-027	Transistor	2N2369
20-029	Transistor	
20-030	Transistor	HPX002
20-031	Transistor	2N3568
20-032	Transistor NPN	SEE 2N6486 SPEC
20-033	Transistor	KE4393
20-034	Transistor	2N3904
20-035	Transistor	2N3906
20-036	Transistor	MP54356
20-037	Transistor	D45H2
20-038	Transistor	2N2520
20-039	Transistor	2N222A
20-043	MCS FET	
21-025F01	1K ohm-15 to Common DIP	898 1-1K ohm (Beckman)
21-025F02	470 ohm-15 to Common DIP	898-1-470 ohm (Beckman)
21-025F03	330 ohm-15 to Common DIP	898-1-330 ohm (Beckman)

Part No.	Type	VENDOR/JEDEC Number
23-001	Diode High Speed-High Current	1N4150
23-002	Diode 5.1 V Zener	1N4733A
23-003	Diode 10V Zener	1N4750A
23-004	Diode 6.1 V Zener	1N4735A
23-007	Diode Mot Bridge	MDA962-2
23-008	Diode Int. Rectifier	40HF-5R
23-009	Diode	1N4735
23-010	Diode Int. Rectifier	S1Y1P
23-011	Diode Rectifier	2N681
23-012	Diode Thermistor	1D2032
23-013	Diode 9.3V	1N2163
23-014	Diode	1N3880
23-015	Diode	1N3889
23-016	Diode Bridge Rectifier	YS448
23-017	Diode	1N2070
23-018	Diode 18 V Zener	1N4746
23-019	Diode	1N3615
23-020	Diode 8.2V Zener	1N756A
23-021	Diode 9.1 V Zener	1N757A
23-022	Diode 3.3V Zener	1N746A
23-023	Diode Bridge Rectifier	KDH250
23-024	Diode, Power Fast Rec. 30 Amps	1N3909
23-025	Diode, Power Fast Rec. 3 Amps	MR841/ A115A
23-026	Triac 600V 30 Amps	2N6162
23-027	Diac 32V	1N5761
23-028	Power SCR Thyristor	2N4441
23-029	Diode	1N4607
23-030	Diode	1N4156A
23-031	Diode 6.8 V Zener	1N4736A
23-032	Diode 9.1 V Zener	1N4739
23-033	16 Diode Array	45190 (Litton)
23-034R01	Switch Diode 600 MA	TSC1N4607
23-035	Diode 40A	MBA4030
23-036	Diode	MPD-400
23-037	Zener Diode 2.4V	1N4370
23-041F00	Low Voltage Zener Diode	LVA51A40114/ LVA51A22819
23-041F02	Low Voltage Zener Diode	LVA62A40098/ LVA62A22941/ LVA62A40212
23-042	Power Schottky	SD41
23-043F00	Zener Diode Avalanche 5.1V	
23-043F01	Zener Diode Avalanche 5.6V	
23-043F02	Zener Diode Avalanche 6.2V	
23-060	Bridge Rectifier, 600V,50A	
30-013	4.7uH Inductor	
30-013F02	1.5uH Inductor	
30-013F03	2.2uH Inductor	

Part No.	Type	VENDOR/JEDEC Number
30-018	100 nanoseconds Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
30-019	50 nanoseconds Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
33-032	Hexadecimal Switch	BERG or AMP

PROG= ASSEMBLED BY CAL 03-066R07-00 (32-BIT)

```
          0000 0001                1  LSU      EQU   1                                                  LSU00000
          0000 0000                2  TEST     EQU   0                                                  LSU00010
                                   3  *                                                                  LSU00020
 000000I                           4           IFZ   LSU                                                  LSU00030
                                   6           ELSE
                                   8           ENDC                                                       LSU00070
                                   9  *                                                                  LSU00080
                                  10           ERSQZ                                                      LSU00090
                                  11           NORX3                                                      LSU00100
                                  12           SQUEZ                                                      LSU00110
                                  13           CROSS                                                      LSU00120
                                  14           FREZE                                                      LSU00130
                                  15           TARGT 32                                                   LSU00140
                                  16  *                                                                  LSU00150
                                  17  * THIS PROGRAM IS DESIGNED TO RUN ON THE PERKIN-ELMER SERIES       LSU00160
                                  18  * 3200 ONLY.  IT USES INSTRUCTIONS NOT AVAILABLE ON THE           LSU00170
                                  19  * PERKIN-ELMER 7/32 OR 8/32.                                       LSU00180
                                  20  *                                                                  LSU00190
                                  21  * USING CONDITIONAL ASSEMBLY INSTRUCTIONS THIS SOURCE              LSU00200
                                  22  * WILL PRODUCE EITHER OF THE FOLLOWING PROGRAMS:                   LSU00210
                                  23  *                                                                  LSU00220
                                  24  *   SETTING                          PROGRAM                       LSU00230
                                  25  *                                                                  LSU00240
                                  26  *     LSU                                                          LSU00250
                                  27  *                                                                  LSU00260
                                  28  *      1  .....................STANDARD LSU LOADER - FOR CHIPS.      LSU00270
                                  29  *      0  .....................BOOTSTRAP LOADER (TAPE) - FOR TESTING. LSU00280
                                  30  *                                                                  LSU00290
                                  31  * IF THE LSU OPTION IS SPECIFIED THIS PROGRAM PRODUCES THE FORMAT  LSU00300
                                  32  * REQUIRED FOR LSU STORAGE AND OPERATION (SEE PROGRAMMING          LSU00310
                                  33  * SPECIFICATION 02-267R02A22 SECTION 5)                           LSU00320
                                  34  *                                                                  LSU00330
                                  35  * NOTE:  IF 'TEST' IS SET TO A NON-ZERO VALUE, THE PROGRAM(S)      LSU00340
                                  36  *        GENERATED WILL RUN ON A 7/32 OR 8/32.                     LSU00350
                                  37  *                                                                  LSU00360
                                  38  * THIS PROGRAM IS A LOADER THAT READS A CORE IMAGE OF OS/32        LSU00370
                                  39  * FROM A 5, 67, OR 256 MEGABYTE DISC, FROM A FLOPPY DISC,          LSU00380
                                  40  * OR FROM A MAGNETIC TAPE.                                        LSU00390
                                  41  *                                                                  LSU00400
                                  42  *    DEVICE CODES          DEVICE                                  LSU00410
                                  43  *                                                                  LSU00420
                                  44  *        X'32'               5MB DISC - FIXED                      LSU00430
                                  45  *        X'33'               5MB DISC - REMOVABLE                  LSU00440
                                  46  *        X'35'              67MB DISC                              LSU00450
                                  47  *        X'36'             256MB DISC                              LSU00460
                                  48  *        X'37'             FLOPPY DISC                             LSU00470
                                  49  *        X'40'              800 BPI MAG TAPE                       LSU00480
                                  50  *        X'41'             1600 BPI OR DUAL DENSITY MAG TAPE       LSU00490
                                  51  *                                                                  LSU00500
                                  52  * THE LOADER FUNCTIONS IN THE FOLLOWING MANNER:                    LSU00510
                                  53  *                                                                  LSU00520
                                  54  *        1. OUTPUT A "MENU" OF STANDARD DEVICES FROM WHICH THE O.S. LSU00530
                                  55  *           MAY BE LOADED.                                         LSU00540
```

```
*                                                                       LSU00550
*       2. IN RESPONSE TO USER'S INPUT, READ LOADER INFORMATION BLOCK   LSU00560
*          OF REQUESTED O.S. TO DETERMINE THE O.S. SIZE.                 LSU00570
*                                                                       LSU00580
*       3. TEST THE MEMORY IN WHICH THE O.S. IS TO RESIDE.              LSU00590
*                                                                       LSU00600
*       4. RELOCATE THE LOADER ABOVE THE MEMORY TO BE OCCUPIED          LSU00610
*          BY THE O.S.                                                  LSU00620
*                                                                       LSU00630
*       5. TEST THE MEMORY JUST VACATED BY THE LOADER.                  LSU00640
*                                                                       LSU00650
*       6.  LOAD AND EXECUTE THE O.S.                                   LSU00660
*                                                                       LSU00670
* THE MEMORY TEST FUNCTIONS IN THE FOLLOWING MANNER:                    LSU00680
*                                                                       LSU00690
*       1. THE ADDRESS OF EACH LOCATION TO BE TESTED IS WRITTEN TO      LSU00700
*          THAT LOCATION.  AFTER ALL ADDRESSES ARE WRITTEN, THEY ARE    LSU00710
*          READ BACK AND COMPARED TO THE ADDRESS POINTER.               LSU00720
*                                                                       LSU00730
*       2. TEST 1 IS RUN USING THE COMPLEMENT OF EACH ADDRESS AS        LSU00740
*          THE TEST DATA.                                               LSU00750
*                                                                       LSU00760
*       3. A SERIES OF BIT PATTERNS ARE THEN TESTED IN THE              LSU00770
*          FOLLOWING MANNER:                                            LSU00780
*                                                                       LSU00790
*          A. A PATTERN IS WRITTEN TO EACH LOCATION TO BE TESTED.       LSU00800
*          B. AFTER ALL LOCATIONS HAVE BEEN WRITTEN TO WITH ONE         LSU00810
*             PATTERN, THE DATA IS READ BACK AND COMPARED TO THE        LSU00820
*             PATTERN BEING TESTED.                                     LSU00830
*          C. A AND B ARE REPEATED UNTIL ALL PATTERNS HAVE BEEN USED.   LSU00840
*                                                                       LSU00850
*       IF A NON-COMPARE OCCURS DURING ANY OF THE TESTS, THE            LSU00860
*       ERROR MESSAGE "MEMTST ERR NNNNNN" IS OUTPUT, AND TESTING        LSU00870
*       IS TERMINATED.  "NNNNNN" REPRESENTS THE ADDRESS AT WHICH        LSU00880
*       THE NON-COMPARE OCCURRED.                                       LSU00890
*                                                                       LSU00900
*       THE PATTERNS AND METHOD USED IN THIS TEST ASSURE THAT:          LSU00910
*                                                                       LSU00920
*       1. ALL LOCATIONS TESTED ARE INDEPENDENTLY ADDRESSABLE;          LSU00930
*                                                                       LSU00940
*       2. NO BITS WITHIN ANY FULLWORD ARE STUCK IN THE ON OR           LSU00950
*          OFF STATE;                                                   LSU00960
*                                                                       LSU00970
*       3. NO BITS WITHIN ANY FULLWORD ARE SHORTED TOGETHER;            LSU00980
*                                                                       LSU00990
*       4. ACCESSING ANY FULLWORD WILL NOT CHANGE ANY OTHER FULLWORD    LSU01000
*          WITHIN THE TESTED RANGE.                                     LSU01010
```

GENERAL EQUATES

```
                          104  * ENTRY/EXTRN DECLARATIONS = NONE                                    LSU01030
                          105  *                                                                    LSU01040
                          106  *         COPY  DIR                                                  LSU01050
                          107  *         COPY  LIB                                                  LSU01060
                          108           NLIST                                                      LSU01070
                          111           LIST                                                       LSU01100
     0000 1000            112  LSUADDR  EQU   X'1000'          INITIAL BASE ADDRESS OF LOADER.    LSU01110
     0000 0078            113  BINDV    EQU   X'78'            BINARY DEVICE ADDRESS.             LSU01120
     0000 0060            114  OS.START EQU   X'60'            O.S. START ADDRESS.                LSU01130
     0000 000D            115  CR       EQU   X'0D'            CARRIAGE RETURN.                   LSU01140
     0000 000A            116  LF       EQU   X'0A'            LINE FEED.                         LSU01150
     0000 0008            117  BSY      EQU   8                                                    LSU01160
                          118  *                                                                    LSU01170
                          119  * REGISTER EQUATES                                                  LSU01180
                          120  *                                                                    LSU01190
     0000 0000            121  R0       EQU   0                                                    LSU01200
     0000 0001            122  R1       EQU   1                                                    LSU01210
     0000 0002            123  R2       EQU   2                                                    LSU01220
     0000 0003            124  R3       EQU   3                                                    LSU01230
     0000 0004            125  R4       EQU   4                                                    LSU01240
     0000 0005            126  R5       EQU   5                                                    LSU01250
     0000 0006            127  R6       EQU   6                                                    LSU01260
     0000 0007            128  R7       EQU   7                                                    LSU01270
     0000 0008            129  R8       EQU   8                                                    LSU01280
     0000 0009            130  R9       EQU   9                                                    LSU01290
     0000 000A            131  R10      EQU   10                                                   LSU01300
     0000 000B            132  R11      EQU   11                                                   LSU01310
     0000 000C            133  R12      EQU   12                                                   LSU01320
     0000 000D            134  R13      EQU   13                                                   LSU01330
     0000 000E            135  R14      EQU   14                                                   LSU01340
     0000 000F            136  R15      EQU   15                                                   LSU01350
000000I                   137           IFNZ  LSU                                                  LSU01360
```

LSU LOADER - PREAMBLE

```
000000I  0000                139          DCX   0                    START PSW                LSU01380
000002I  1000                140          DC    Z(LSUADDR)           START ADDRESS            LSU01390
000004I  1000                141          DC    Z(LSUADDR)           LOAD ADDRESS             LSU01400
000006I  17F4                142          DC    Z(LSUADDR+LENGTH)    END ADDRESS              LSU01410
                             143          ELSE                                                  LSU01420
                             188          ENDC                                                  LSU01870
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
          0000 0008I            190  LODRSTRT EQU   *                                                    LSU01890
 000008I  C840 0010             191           LHI   R4,X'10'          GET DEVICE # AND                   LSU01900
 00000CI  DE40 87AB =0007BBI    192           OC    R4,COM2           SET-UP PASLA.                      LSU01910
 000010I  9B47                  193           RDR   R4,R7             ISSUE DUMMY READ.                  LSU01920
 000012I  E610 8504 =00051AI    194           LA    R1,MSG            GET ADDRESS OF MESSAGE HANDLER.    LSU01930
 000016I  2480                  195           LIS   R8,0              INITIALIZE STRING REGISTER.        LSU01940
 000018I  01F1                  196           BALR  R15,R1            OUTPUT THE IDENTIFIER.             LSU01950
 00001AI  06E4                  197           DC    Z(ID-LODRSTRT)    :                                  LSU01960
 00001CI  01F1                  198           BALR  R15,R1            OUTPUT THE MENU.                   LSU01970
 00001EI  06FC                  199           DC    Z(MENU-LODRSTRT)  :                                  LSU01980
                                200  *                                GET THE REPLY.                     LSU01990
          0000 0020I            201  GETNAME  EQU   *                                                    LSU02000
 000020I  41E0 8530 =000554I    202           BAL   R14,GETC          LOOP UNTIL DELIMITER               LSU02010
*000024I  2212                  203           BNM   GETNAME           :                                  LSU02020
 000026I  E690 86E2 =00070CI    204           LA    R9,DEVTABLE       NO, GET BASE ADDR OF DEVICE TABLE. LSU02030
 00002AI  E6A0 871E =00074CI    205           LA    R10,DEVTBLND      GET END ADDRESS OF DEVICE TABLE.   LSU02040
          0000 002EI            206  CK.NAME  EQU   *                                                    LSU02050
 00002EI  5589 0000             207           CL    R8,0(R9)          MATCH?                             LSU02060
*000032I  2336                  208           BE    FOUND.NM          YES, THEN GO GET FILENAME.         LSU02070
 000034I  2698                  209           AIS   R9,8              NO, BUMP POINTER.                  LSU02080
 000036I  059A                  210           CLR   R9,R10            AT END YET?                        LSU02090
 000038I  2035                  211           BNES  CK.NAME           NO, TRY NEXT NAME.                 LSU02100
 00003AI  4300 FFCA =000008I    212           B     LODRSTRT          YES, INVALID NAME - START AGAIN.   LSU02110
                                213  *                                                                    LSU02120
          0000 003EI            214  FOUND.NM EQU   *                                                    LSU02130
 00003EI  08D9                  215           LR    R13,R9            HOLD ADDRESS OF SELECTION.         LSU02140
 000040I  E6A0 86C8 =00070CI    216           LA    R10,DEVTABLE      CALCULATE OFFSET.                  LSU02150
 000044I  0B9A                  217           SR    R9,R10            :                                  LSU02160
 000046I  2334                  218           BZS   VECTOR            IF ZERO, NO FURTHER CALCULATION.   LSU02170
 000048I  2480                  219           LIS   R8,0              ELSE, CALCULATE INDEX              LSU02180
 00004AI  2478                  220           LIS   R7,8              INTO VECTOR TABLE.                 LSU02190
 00004CI  1D87                  221           DR    R8,R7             (R9) = INDEX.                      LSU02200
          0000 004EI            222  VECTOR   EQU   *                                                    LSU02210
 00004EI  4090 89F2 =000A44I    223           STH   R9,TBNTRY         SAVE AS INDEX INTO DEVICE TABLE.   LSU02220
 000052I  E6A0 86EE =000744I    224           LA    R10,OTHER         WAS "OTHR" SELECTED?               LSU02230
 000056I  05DA                  225           CLR   R13,R10           :                                  LSU02240
 000058I  4230 806A =0000C6I    226           BNE   SET.IO            NO, SET-UP TO READ O.S.            LSU02250
                                227  *                                YES, ASK FOR SPECIFICS.            LSU02260
 00005CI  2490                  228           LIS   R9,0              INITIALIZE INDEX INTO DEVICE TABLE. LSU02270
 00005EI  24D0                  229           LIS   R13,0             INITIALIZE INDEX INTO ADDRESS TABLE. LSU02280
          0000 0060I            230  NXT.ITEM EQU   *                                                    LSU02290
 000060I  486D 867E =0006E2I    231           LH    R6,ADDRTABL(R13)  GET MESSAGE ADDRESS.               LSU02300
 000064I  4060 8002 =00006AI    232           STH   R6,NAM.ITEM       :                                  LSU02310
 000068I  01F1                  233           BALR  R15,R1            ISSUE REQUEST.                     LSU02320
 00006AI  0062                  234  NAM.ITEM DC    Z(NAM.ITEM-LODRSTRT) :                               LSU02330
 00006CI  2400                  235           LIS   R0,0              INITIALIZE FOR HEX CHARACTERS.     LSU02340
          0000 006EI            236  GET.ITEM EQU   *                                                    LSU02350
 00006EI  2480                  237           LIS   R8,0              INITIALIZE STRING REGISTER.        LSU02360
 000070I  41E0 84E0 =000554I    238           BAL   R14,GETC          GET A CHARACTER.                   LSU02370
*000074I  2116                  239           BM    CHK.ITEM          EXIT IF CARRIAGE RETURN DETECTED.  LSU02380
 000076I  41E0 8530 =0005AAI    240           BAL   R14,X.CONV        ELSE, CONVERT TO HEX NIBBLE.       LSU02390
 00007AI  1104                  241           SLLS  R0,4              CONCATENATE WITH PREVIOUS RESULTS. LSU02400
 00007CI  0608                  242           OR    R0,R8             :                                  LSU02410
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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*00007EI  2208                 243          B     GET.ITEM          GET NEXT CHARACTER.                LSU02420
                               244  *                                                                    LSU02430
          0000 0080I           245  CHK.ITEM EQU   *                                                    LSU02440
 000080I  C5D0 0008            246          CLHI  R13,8             WAS ITEM "DRV#"?                   LSU02450
*000084I  2132                 247          BNE   STR.ITEM          NO, THEN STORE AS IS.              LSU02460
 000086I  1104                 248          SLLS  R0,4              YES, THEN SHIFT BY 4.              LSU02470
          0000 0088I           249  STR.ITEM EQU   *                                                    LSU02480
 000088I  4009 864E =0006DAI   250          STH   R0,OTHR(R9)       STORE ITEM IN DEVICE TABLE.        LSU02490
 00008CI  26D2                 251          AIS   R13,2             BUMP ADDRESS TABLE POINTER.        LSU02500
 00008EI  C5D0 0004            252          CLHI  R13,4             WAS LAST ITEM "CODE"?              LSU02510
 000092I  4230 8026 =0000BCI   253          BNE   BMP.ITEM          NO, GO STORE ITEM NOW.             LSU02520
 000096I  2460                 254          LIS   R6,0              YES, CHECK VALIDITY OF DEV CODE.   LSU02530
          0000 0098I           255  NXT.CODE EQU   *                                                    LSU02540
*000098I  C560 0038            256          CLI   R6,OTHR-DTABLE    AT END OF TABLE?                   LSU02550
 00009CI  4380 FF68 =000008I   257          BNL   LODRSTRT          YES, ERROR - RESTART.              LSU02560
 0000A0I  4506 8600 =0006A4I   258          CLH   R0,DTABLE+2(R6)   VALID DEVICE CODE?                 LSU02570
*0000A4I  2333                 259          BE    END.CODE          YES, THEN EXIT.                    LSU02580
 0000A6I  2668                 260          AIS   R6,8              NO, BUMP POINTER.                  LSU02590
*0000A8I  2208                 261          B     NXT.CODE          CHECK NEXT CODE.                   LSU02600
                               262  *                                                                    LSU02610
          0000 00AAI           263  END.CODE EQU   *                                                    LSU02620
 0000AAI  C500 0037            264          CLHI  R0,X'37'          WAS CODE FOR "NORMAL" DISC?        LSU02630
*0000AEI  2187                 265          BL    BMP.ITEM          YES, NOW GET CONTROLLER.           LSU02640
 0000B0I  26D2                 266          AIS   R13,2             NO, DON'T ASK FOR "CTLR".          LSU02650
 0000B2I  2692                 267          AIS   R9,2              :                                  LSU02660
 0000B4I  C500 0037            268          CLHI  R0,X'37'          WAS CODE FOR FLOPPY?               LSU02670
*0000B8I  2132                 269          BNE   BMP.ITEM          NO, THEN ASK FOR "SLCH".           LSU02680
 0000BAI  26D2                 270          AIS   R13,2             YES, ASK FOR "DRV#".               LSU02690
*0000BCI                       271          B     BMP.ITEM          :                                  LSU02700
                               272  *                                                                    LSU02710
          0000 00BCI           273  BMP.ITEM EQU   *                                                    LSU02720
 0000BCI  2692                 274          AIS   R9,2              BUMP INDEX.                        LSU02730
 0000BEI  C590 0008            275          CLHI  R9,8              ARE WE DONE YET?                   LSU02740
 0000C2I  4280 FF9A =000060I   276          BL    NXT.ITEM          NO, GET THE NEXT ITEM.             LSU02750
*0000C6I                       277          B     SET.IO            YES, SET-UP TO READ O.S.           LSU02760
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                                279  * THE FOLLOWING CODE ACCESSES THE DISC DEFINITION TABLE                LSU02780
                                280  * AND LOADS THE SELCH, CONTROLER, AND DEVICE TYPE                      LSU02790
                                281  *                                                                     LSU02800
         0000 00C6I             282  SET.IO    EQU   *                SET-UP TO READ OPERATING SYSTEM.      LSU02810
 0000C6I 48F0 897A =000A44I     283            LH    R15,TBNTRY       CALCULATE INDEX INTO DEVICE TABLE.   LSU02820
 0000CAI 11F3                   284            SLLS  R15,3            :                                    LSU02830
 0000CCI E6FF 85D2 =0006A2I     285            LA    R15,DTABLE(R15)  GET ADDRESS OF REQUESTED ENTRY.      LSU02840
 0000D0I 732F 0006              286            LHL   R2,6(R15)        GET SELCH ADDRESS (OR FLOPPY #).     LSU02850
 0000D4I 733F 0004              287            LHL   R3,4(R15)        GET CONTROLLER ADDRESS.              LSU02860
 0000D8I 734F 0000              288            LHL   R4,0(R15)        GET DEVICE ADDRESS.                  LSU02870
 0000DCI 735F 0002              289            LHL   R5,2(R15)        GET DEVICE CODE.                     LSU02880
 0000E0I C550 0038              290            CLHI  R5,X'38'         IF DEVICE CODE IS < OR = X'38'       LSU02890
 0000E4I 4280 80EC =0001D4I     291            BL    CK.DISC          THEN DEVICE IS DISC.                 LSU02900
         0000 00E8I             292  MAGTAPE   EQU   *                                                     LSU02910
 0000E8I 2551                   293            LCS   R5,1             SET MAG TAPE SWITCH.                 LSU02920
 0000EAI 24E0                   294            LIS   R14,0            SET SWITCH TO INDICATE               LSU02930
 0000ECI 40E0 895C =000A4CI     295            STH   R14,SWITCH       READ L.I.B.                          LSU02940
 0000F0I E6E0 81E0 =0002D4I     296            LA    R14,OS.SIZE      GET VECTOR ADDRESS.                  LSU02950
 0000F4I DE40 86C5 =0007BDI     297            OC    R4,MTCLEAR       CLEAR DEVICE.                        LSU02960
 0000F8I 4240 83C6 =0004C2I     298            BTC   4,DU             IF FALSE SYNC - NOT THERE.           LSU02970
 0000FCI 9D4F                   299            SSR   R4,R15           IS DEVICE STILL AVAILABLE?           LSU02980
 0000FEI 4210 83C0 =0004C2I     300            BTC   1,DU             NO, THEN ERROR.                      LSU02990
 000102I DE40 86B9 =0007BFI     301            OC    R4,MTREWD        REWIND THE TAPE.                     LSU03000
 000106I D000 88FA =000A04I     302            STM   R0,RSAVE         SAVE ALL REGISTERS.                  LSU03010
 00010AI 01F1                   303            BALR  R15,R1           OUTPUT "FILEMARKS=".                 LSU03020
 00010CI 0779                   304            DC    Z(FMKS-LODRSTRT) :                                    LSU03030
 00010EI 2400                   305            LIS   R0,0             INITIALIZE COUNT.                    LSU03040
         0000 0110I             306  GET.FMKS  EQU   *                                                     LSU03050
 000110I 41E0 8440 =000554I     307            BAL   R14,GETC         GET # OF FILEMARKS TO SKIP.          LSU03060
*000114I 2115                   308            BM    END.FMKS         EXIT IF CARRIAGE RETURN DETECTED.    LSU03070
 000116I 2601                   309            AIS   R0,1             INCREMENT COUNT.                     LSU03080
 000118I C500 0003              310            CLHI  R0,3             IS IT 3 YET?                         LSU03090
*00011CI 2036                   311            BNE   GET.FMKS         NO, GET NEXT CHARACTER.              LSU03100
         0000 011EI             312  END.FMKS  EQU   *                                                     LSU03110
 00011EI 41E0 849C =0005BEI     313            BAL   R14,ASC.HEX      CONVERT COUNT TO HEX.                LSU03120
 000122I 5840 88EE =000A14I     314            L     R4,RSAVE+16      GET DEVICE NUMBER.                   LSU03130
         0000 0126I             315  SKIP.FM   EQU   *                                                     LSU03140
 000126I 2771                   316            SIS   R7,1             ANY FILEMARKS LEFT?                  LSU03150
*000128I 2118                   317            BM    FMKS.DON         NO, THEN DON'T SKIP ANY MORE.        LSU03160
         0000 012AI             318  WAIT.FM   EQU   *                                                     LSU03170
 00012AI 9D4F                   319            SSR   R4,R15           WAIT FOR NO MOTION.                  LSU03180
 00012CI C4F0 0010              320            NHI   R15,X'10'        :                                    LSU03190
*000130I 2233                   321            BZ    WAIT.FM          :                                    LSU03200
 000132I DE40 8686 =0007BCI     322            OC    R4,MTSKIP        SKIP 1 FILEMARK.                     LSU03210
*000136I 2208                   323            B     SKIP.FM          CONTINUE UNTIL COUNTED OUT.          LSU03220
         0000 0138I             324  FMKS.DON  EQU   *                                                     LSU03230
 000138I D100 88C8 =000A04I     325            LM    R0,RSAVE         RESTORE ALL REGISTERS.               LSU03240
 00013CI E670 87C0 =000900I     326            LA    R7,LIBBUFF       YES, GET BUFFER START ADDRESS.       LSU03250
 000140I E680 88BB =0009FFI     327            LA    R8,LIBBUFFE      :    GET BUFFER END ADDRESS.         LSU03260
*000144I                        328            B     MAG.READ         GO TO MAG TAPE HANDLER.              LSU03270
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                                330  *        MAGNETIC TAPE OS-HANDLER                                          LSU03290
                                331  *                                                                          LSU03300
                                332  *   UPON FIRST ENTRY, WILL READ FIRST BLOCK FOR VOLUME                     LSU03310
                                333  *   DESCRIPTOR CHECK.                                                     LSU03320
                                334  *      REG 7    -   START OF BUFFER ADDRESS                               LSU03330
                                335  *      REG 8    -   END OF BUFFER ADDRESS                                 LSU03340
                                336  *      SWITCH   -   CONTAINS 0 (ZERO)                                     LSU03350
                                337  *                                                                         LSU03360
                                338  *   SECOND ENTRY WILL READ ANY ADDITIONAL LIB'S TO LIBBUF                  LSU03370
                                339  *   TO BY-PASS THEM. THEN OS WILL BE STORED FROM LOC 0.                    LSU03380
                                340  *      SWITCH   -   CONTAINS 1                                            LSU03390
                                341  *                                                                         LSU03400
      0000 0144I                342  MAG.READ EQU   *                                                         LSU03410
 000144I  9D4F                  343           SSR   R4,R15          WAIT FOR 'NO MOTION' ON TAPE.              LSU03420
 000146I  C3F0 0010             344           THI   R15,X'10'       :                                          LSU03430
*00014AI  2233                  345           BZ    MAG.READ        :                                          LSU03440
 00014CI  4100 831C =00046CI    346           BAL   R0,ADSELCH      ADDRESS THE SELCH.                         LSU03450
 000150I  4800 88F8 =000A4CI    347           LH    R0,SWITCH       CHECK PROGRAM SWITCH.                      LSU03460
 000154I  2701                  348           SIS   R0,1            :                                          LSU03470
 000156I  4210 8046 =0001A0I    349           BM    READ.MAG        IF SWITCH WAS 0 THEN READ FIRST LIB.       LSU03480
 00015AI  4220 8026 =000184I    350           BP    MAGRD.OS        IF SWITCH WAS 2 THEN READ OS.              LSU03490
                                351  *                             ELSE SWITCH WAS 1, SKIP L.I.B.'S.          LSU03500
 00015EI  4800 88F2 =000A54I    352           LH    R0,NUM.LIBS     GET # OF LIB'S TO SKIP.                    LSU03510
*000162I  2339                  353           BZ    AMAGTE          IF NONE, GO READ O.S.                      LSU03520
 000164I  41E0 8038 =0001A0I    354           BAL   R14,READ.MAG    ELSE, READ A LOADER INFO BLOCK.            LSU03530
 000168I  2701                  355           SIS   R0,1            DECREMENT COUNT                            LSU03540
 00016AI  4000 88E6 =000A54I    356           STH   R0,NUM.LIBS     NO, SAVE COUNTER                           LSU03550
*00016EI  2333                  357           BZ    AMAGTE          FINISHED?                                  LSU03560
 000170I  4300 FFD0 =000144I    358           B     MAG.READ        GO READ NEXT LIB                           LSU03570
      0000 0174I                359  AMAGTE   EQU   *                                                         LSU03580
 000174I  2402                  360           LIS   R0,2            SET SWITCH TO INDICATE                     LSU03590
 000176I  4000 88D2 =000A4CI    361           STH   R0,SWITCH       READ O.S.                                  LSU03600
*00017AI  2470                  362           LI    R7,0            GET BEGINNING OF MEMORY                    LSU03610
*00017CI  C880 00FF             363           LI    R8,255          THRU 256 BYTES                             LSU03620
 000180I  4300 FFC0 =000144I    364           B     MAG.READ        GO READ FIRST OS BLOCK                     LSU03630
                                365  *                                                                         LSU03640
      0000 0184I                366  MAGRD.OS EQU   *                                                         LSU03650
 000184I  41E0 8018 =0001A0I    367           BAL   R14,READ.MAG    READ 1 SECTOR OF O.S.                      LSU03660
 000188I  5580 88C4 =000A50I    368           CL    R8,OS.END       END OF LOAD?                               LSU03670
 00018CI  4330 81D0 =000360I    369           BE    EXEC.OS         YES, EXECUTE THE O.S.                      LSU03680
 000190I  4380 8336 =0004CAI    370           BNL   UNRE            NO, THEN ERROR.                            LSU03690
*000194I  CA70 0100             371           AI    R7,256          INCREMENT START ADDRESS.                   LSU03700
*000198I  CA80 0100             372           AI    R8,256          INCREMENT END ADDRESS.                     LSU03710
 00019CI  4300 FFA4 =000144I    373           B     MAG.READ        GO SET NEXT READ                           LSU03720
                                374  *                                                                         LSU03730
      0000 01A0I                375  READ.MAG EQU   *                                                         LSU03740
 0001A0I  DE40 861A =0007BEI    376           OC    R4,MTREAD       ISSUE READ CMD TO MAG TAPE.                LSU03750
 0001A4I  DE20 8619 =0007C1I    377           OC    R2,SHGORD       ISSUE READ CMD TO SELCH.                   LSU03760
 0001A8I  9D4F                  378           SSR   R4,R15          IF NOT FALSE SYNC, CONFIG ERROR.           LSU03770
 0001AAI  C5F0 0004             379           CLHI  R15,X'04'       :                                          LSU03780
 0001AEI  4230 8320 =0004D2I    380           BNE   CNFG            :                                          LSU03790
      0000 01B2I                381  WAIT.MAG EQU   *                                                         LSU03800
 0001B2I  9D2F                  382           SSR   R2,R15          GET STATUS AND                             LSU03810
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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0001B4I  2081                 383        BTBS  BSY,WAIT.MAG      LOOP UNTIL NOT BUSY.                  LSU03820
0001B6I  DE20 8606 =0007C0I   384        OC    R2,SHCLEAR        CLEAR THE SELCH.                      LSU03830
0001BAI  9B23                 385        RDR   R2,R3             GET 1ST BYTE OF FINAL ADDRESS.        LSU03840
0001BCI  9926                 386        RHR   R2,R6             GET LAST 2 BYTES OF FINAL ADDRESS.    LSU03850
0001BEI  3433                 387        EXHR  R3,R3             COMBINE BOTH SECTIONS TO              LSU03860
0001C0I  0A63                 388        AR    R6,R3             GET FINAL ADDRESS.                    LSU03870
0001C2I  0568                 389        CLR   R6,R8             FINAL ADDRESS = END ADDRESS?          LSU03880
0001C4I  033E                 390        BER   R14               YES, RETURN TO CALLER.                LSU03890
0001C6I  9D4F                 391        SSR   R4,R15            NO, GET STATUS OF TAPE.               LSU03900
0001C8I  C3F0 0040            392        THI   R15,X'40'         NO, END-OF-FILE?                      LSU03910
0001CCI  4230 8190 =000360I   393        BNZ   EXEC.OS           YES, EXECUTE THE O.S.                 LSU03920
0001D0I  4300 82F6 =0004CAI   394        B     UNRE              ELSE, UNRECOVERABLE ERROR.            LSU03930
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                0000 01D4I                396  CK.DISC  EQU   *                                                    LSU03950
 0001D4I  CB50 0034                       397           SHI   R5,X'34'          CALCULATE INDEX TO SECTOR TABLE.  LSU03960
*0001D8I  2113                            398           BM    CK.DISC1          IF < 0 THEN 0.                   LSU03970
 0001DAI  1151                            399           SLLS  R5,1              ELSE MULTIPLY BY 2.              LSU03980
*0001DCI  2302                            400           B     VD.READ           GO READ VOLUME DESCRIPTOR.       LSU03990
                                          401  *                                                                  LSU04000
                0000 01DEI                402  CK.DISC1 EQU   *                                                    LSU04010
 0001DEI  2450                            403           LIS   R5,0              SET INDEX TO 0 (2.5 OR 5).       LSU04020
*0001E0I                                  404           B     VD.READ           GO READ VOLUME DESCRIPTOR.       LSU04030
                                          405  *                                                                  LSU04040
                0000 01E0I                406  VD.READ  EQU   *                 READ VOLUME DESCRIPTOR.          LSU04050
 0001E0I  E670 8618 =0007FCI              407           LA    R7,VDBUF          GET BUFFER START ADDRESS.        LSU04060
 0001E4I  E680 8713 =0008FBI              408           LA    R8,VDBUFE         GET BUFFER END ADDRESS.          LSU04070
 0001E8I  24C0                            409           LIS   R12,0             SET LOGICAL SECTOR NO TO 0       LSU04080
 0001EAI  41E0 8176 =000364I              410           BAL   R14,READ          READ VOLUME DESCRIPTOR.          LSU04090
 0001EEI  D000 8812 =000A04I              411           STM   R0,RSAVE          SAVE ALL REGISTERS.              LSU04100
 0001F2I  5860 8606 =0007FCI              412           L     R6,VD.VOL         GET VOLUME NAME,                 LSU04110
 0001F6I  5060 855E =000758I              413           STA   R6,VOLFIL+4       AND STORE IN MESSAGE.            LSU04120
 0001FAI  01F1                            414           BALR  R15,R1            OUTPUT "VOL=XXXX,FILE=".         LSU04130
 0001FCI  074C                            415           DC    Z(VOLFIL-LODRSTRT) :                               LSU04140
 0001FEI  F8E0 2020 2020                  416           LI    R14,C'    '       SET FILE NAME TO BLANKS.         LSU04150
 000204I  08FE                            417           LR    R15,R14           :                                LSU04160
 000206I  D0E0 8852 =000A5CI              418           STM   R14,FILENAME      :                                LSU04170
 00020AI  50E0 8856 =000A64I              419           ST    R14,EXT           SET EXTENSION TO BLANKS.         LSU04180
 00020EI  2480                            420           LIS   R8,0              SET ACCOUNT # TO ZERO.           LSU04190
 000210I  D280 8853 =000A67I              421           STB   R8,EXT+3          :                                LSU04200
 000214I  E650 8844 =000A5CI              422           LA    R5,FILENAME       GET DESTINATION ADDR FOR FILENAME. LSU04210
                0000 0218I                423  GET.FLNM EQU   *                                                    LSU04220
 000218I  41E0 8338 =000554I              424           BAL   R14,GETC          GET A CHARACTER.                 LSU04230
 00021CI  4210 804A =00026AI              425           BM    GET.FILE          EXIT IF CARRIAGE RETURN DETECTED. LSU04240
 000220I  C570 002E                       426           CLHI  R7,C'.'           IS IT A PERIOD?                  LSU04250
*000224I  2339                            427           BE    GET.EXT           YES, GET EXTENSION.              LSU04260
 000226I  C570 002F                       428           CLHI  R7,C'/'           NO, IS IT A SLASH?               LSU04270
 00022AI  4330 8022 =000250I              429           BE    GET.ACT           YES, GET ACCOUNT NUMBER.         LSU04280
 00022EI  D275 0000                       430           STB   R7,0(R5)          NO, SAVE BYTE OF FILENAME.       LSU04290
 000232I  2651                            431           AIS   R5,1              BUMP FILE NAME POINTER.          LSU04300
*000234I  220E                            432           B     GET.FLNM          AND GET NEXT CHARACTER.          LSU04310
                                          433  *                                                                  LSU04320
                0000 0236I                434  GET.EXT  EQU   *                                                    LSU04330
 000236I  E650 882A =000A64I              435           LA    R5,EXT            GET DESTINATION ADDR FOR EXTENSION. LSU04340
                0000 023AI                436  GET.EXT1 EQU   *                                                    LSU04350
 00023AI  41E0 8316 =000554I              437           BAL   R14,GETC          GET A CHARACTER.                 LSU04360
 00023EI  4210 8028 =00026AI              438           BM    GET.FILE          EXIT IF CARRIAGE RETURN DETECTED. LSU04370
 000242I  C570 002F                       439           CLHI  R7,C'/'           IS IT A SLASH?                   LSU04380
*000246I  2335                            440           BE    GET.ACT           YES, THEN GET ACCOUNT.           LSU04390
 000248I  D275 0000                       441           STB   R7,0(R5)          NO, STORE BYTE OF EXTENSION.     LSU04400
 00024CI  2651                            442           AIS   R5,1              BUMP EXTENSION POINTER,          LSU04410
*00024EI  220A                            443           B     GET.EXT1          AND GET NEXT CHARACTER.          LSU04420
                                          444  *                                                                  LSU04430
                0000 0250I                445  GET.ACT  EQU   *                                                    LSU04440
 000250I  2480                            446           LIS   R8,0              INITIALIZE CHARACTER STRING.     LSU04450
 000252I  2400                            447           LIS   R0,0              INITIALIZE COUNT.                LSU04460
                0000 0254I                448  GET.ACT1 EQU   *                                                    LSU04470
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 000254I  41E0 82FC =000554I     449            BAL   R14,GETC          GET ACCOUNT NUMBER.                    LSU04480
*000258I  2115                   450            BM    ACT.END           EXIT IF CARRIAGE RETURN DETECTED.      LSU04490
 00025AI  2601                   451            AIS   R0,1               BUMP COUNT.                            LSU04500
 00025CI  C500 0003              452            CLHI  R0,3               3 CHARACTERS YET?                      LSU04510
*000260I  2036                   453            BNE   GET.ACT1           NO, GET NEXT ONE.                      LSU04520
          0000 0262I             454  ACT.END   EQU   *                                                         LSU04530
 000262I  41E0 8358 =0005BEI     455            BAL   R14,ASC.HEX        CONVERT ACCT # TO HEX.                 LSU04540
 000266I  D270 87FD =000A67I     456            STB   R7,EXT+3           STORE THE ACCOUNT NUMBER.              LSU04550
*00026AI                         457            B     GET.FILE           GO SEE IF WE CAN FIND THE O.S.         LSU04560
                                 458  *                                                                        LSU04570
          0000 026AI             459  GET.FILE  EQU   *                  SEARCH DIRECTORY FOR PROPER O.S.       LSU04580
 00026AI  D100 8796 =000A04I     460            LM    R0,RSAVE           RESTORE ALL REGISTERS.                 LSU04590
 00026EI  58C0 8592 =000804I     461            LDA   R12,VD.FDP         IS THERE A DIRECTORY?                  LSU04600
 000272I  4330 8046 =0002BCI     462            BZ    NO.OS              NO, THEN ERROR.                        LSU04610
          0000 0276I             463  READ.DIR  EQU   *                                                         LSU04620
 000276I  E670 8582 =0007FCI     464            LA    R7,VDBUF           GET START ADDR (R8) = END ADDR.        LSU04630
 00027AI  41E0 80E6 =000364I     465            BAL   R14,READ           READ A DIRECTORY SECTOR.               LSU04640
 00027EI  E660 857E =000800I     466            LA    R6,VDBUF+4         GET POINTER TO 1ST DIRECTORY ENTRY.    LSU04650
 000282I  2405                   467            LIS   R0,5               INITIALIZE LOOP COUNTER.               LSU04660
          0000 0284I             468  CK.ENTRY  EQU   *                                                         LSU04670
 000284I  D376 0024              469            LB    R7,DIR.ATRB(R6)    GET ATTRIBUTE INFORMATION.             LSU04680
 000288I  C370 0010              470            THI   R7,DIRA.ACM        IS THIS ENTRY ACTIVE.                  LSU04690
*00028CI  233F                   471            BZ    NEXT.DIR           NO, CHECK NEXT ONE.                    LSU04700
 00028EI  C370 00E0              472            THI   R7,X'E0'           YES, IS IT A CONTIGUOUS FILE?          LSU04710
*000292I  213C                   473            BNZ   NEXT.DIR           NO, CHECK NEXT ENTRY.                  LSU04720
 000294I  D1D0 87C4 =000A5CI     474            LM    R13,FILENAME       YES, GET FILENAME.EXT/ACT.             LSU04730
 000298I  55D6 0000              475            CL    R13,DIR.FNM(R6)    IS IT POSSIBLY THIS FILE?              LSU04740
*00029CI  2137                   476            BNE   NEXT.DIR           NO, CHECK NEXT ENTRY.                  LSU04750
 00029EI  55E6 0004              477            CL    R14,DIR.FNM+4(R6)  YES, DOES THE 2ND HALF MATCH?          LSU04760
 0002A2I  2134                   478            BNES  NEXT.DIR           NO, CHECK NEXT ENTRY?                  LSU04770
 0002A4I  55F6 0008              479            CL    R15,DIR.EXT(R6)    YES, PROPER EXTENSION/ACCT?            LSU04780
*0002A8I  233C                   480            BE    OS.FOUND           YES, THEN WE'VE FOUND THE O.S.         LSU04790
          0000 02AAI             481  NEXT.DIR  EQU   *                                                         LSU04800
 0002AAI  CA60 0030              482            AHI   R6,48              NO, BUMP DIRECTORY POINTER.            LSU04810
 0002AEI  2701                   483            SIS   R0,1               DECREMENT THE ENTRY COUNTER.           LSU04820
 0002B0I  4230 FFD0 =000284I     484            BNZ   CK.ENTRY           IF NOT DONE, CHECK NEXT ENTRY.         LSU04830
 0002B4I  58C0 8544 =0007FCI     485            LDA   R12,VDBUF          WAS THIS THE LAST DIRECTORY ENTRY?     LSU04840
 0002B8I  4230 FFBA =000276I     486            BNZ   READ.DIR           NO, GET THE NEXT ONE.                  LSU04850
          0000 02BCI             487  NO.OS     EQU   *                  YES, THEN O.S. NOT FOUND.              LSU04860
 0002BCI  4300 81FA =0004BAI     488            B     FILNTFND           INDICATE O.S. NOT FOUND.               LSU04870
                                 489  *                                                                        LSU04880
          0000 02C0I             490  OS.FOUND  EQU   *                  O.S. FOUND - DETERMINE IT'S SIZE.      LSU04890
 0002C0I  58C6 000C              491            LDA   R12,DIR.FLBA(R6)   PICK UP FILE 1ST LBA                   LSU04900
                                 492  *                                                                        LSU04910
                                 493  * READ IN FIRST LIB RECORD TO DETERMINE NUMBER TO SKIP                    LSU04920
                                 494  *                                                                        LSU04930
 0002C4I  5060 8634 =0008FCI     495            ST    R6,DIRSAVE         SAVE DIRECTORY POINTER                 LSU04940
 0002C8I  E670 8634 =000900I     496            LA    R7,LIBBUFF         POINT TO START OF BUFFER               LSU04950
 0002CCI  E680 872F =0009FFI     497            LA    R8,LIBBUFFE        POINT TO END OF BUFFER                 LSU04960
 0002D0I  41E0 8090 =000364I     498            BAL   R14,READ           GET LIB RECORD                         LSU04970
          0000 02D4I             499  OS.SIZE   EQU   *                                                         LSU04980
 0002D4I  D3F0 8629 =000901I     500            LB    R15,LIBBUFF+LIB.NLIB GET # OF L.I.B.'S                   LSU04990
 0002D8I  0855                   501            LR    R5,R5              MAG TAPE O.S.?                         LSU05000
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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*0002DAI  2317                    502          BNM   DISC.OS              NO, THEN MUST BE DISC.                    LSU05010
 0002DCI  5880 862C =00090CI      503          L     R8,LIBBUFF+LIB.SEGS    GET SEGMENT SIZE.                         LSU05020
 0002E0I  2401                    504          LIS   R0,1                  SET SWITCH TO BYPASS LIB'S                LSU05030
 0002E2I  4000 8766 =000A4CI      505          STH   R0,SWITCH             IF MORE THAN ONE.                         LSU05040
*0002E6I  2309                    506          B     CALC.SIZ              GO COMPUTE OS SIZE.                       LSU05050
                                  507  *                                                                             LSU05060
         0000 02E8I               508  DISC.OS  EQU   *                                                             LSU05070
 0002E8I  5860 8610 =0008FCI      509          L     R6,DIRSAVE            RESTORE DIRECTORY POINTER                 LSU05080
 0002ECI  58C6 000C               510          L     R12,DIR.FLBA(R6)      GET 1ST SECTOR # IN FILE.                 LSU05090
 0002F0I  5886 0010               511          L     R8,DIR.LLBA(R6)       GET LAST SECTOR # IN FILE.                LSU05100
 0002F4I  0B8C                    512          SR    R8,R12                GET SIZE OF O.S. IN SECTORS.              LSU05110
 0002F6I  0ACF                    513          AR    R12,R15               ADJUST FOR L.I.B RECORDS.                 LSU05120
         0000 02F8I               514  CALC.SIZ EQU   *                                                             LSU05130
 0002F8I  27F1                    515          SIS   R15,1                 ALLOW FOR L.I.B. ALREADY READ.            LSU05140
 0002FAI  40F0 8756 =000A54I      516          STH   R15,NUM.LIBS          SAVE REMAINING # OF L.I.B.'S.             LSU05150
 0002FEI  0B8F                    517          SR    R8,R15                ADJUST SIZE FOR L.I.B. RECORDS.           LSU05160
 000300I  1188                    518          SLLS  R8,8                  SECTORS*256 = BYTES.                      LSU05170
 000302I  2781                    519          SIS   R8,1                  CALCULATE END ADDR FOR MAG READ.          LSU05180
 000304I  5080 8748 =000A50I      520          ST    R8,OS.END             SAVE BYTE LENGTH OF O.S.                  LSU05190
 000308I  2681                    521          AIS   R8,1                  READJUST FOR MEMORY TEST.                 LSU05200
                                  522  *                                                                             LSU05210
                                  523  * TEST FROM TOP OF LOADER TO TOP OF OS                                        LSU05220
                                  524  *                                                                             LSU05230
                                  525          STM   R0,RSAVE              SAVE REGISTERS                            LSU05240
 00030AI  D000 86F6 =000A04I      526          AI    R8,LODREND-LODRSTRT   ALLOW FOR LOADER RELOCATION               LSU05250
*00030EI  CA80 0A60               527          LR    R2,R8                 GET END ADDRESS.                          LSU05260
 000312I  0828                    528          LA    R13,LODREND           GET START ADDRESS.                        LSU05270
 000314I  E6D0 8750 =000A68I      529          ST    R13,ENDLODR           SAVE FOR USE AFTER RELOCATION.            LSU05280
 000318I  50D0 873C =000A58I      530          BAL   R14,MEM.TEST          TEST MEMORY                               LSU05290
 00031CI  41E0 82E2 =000602I      531  *                                                                             LSU05300
                                  532  * RELOCATE LOADER ABOVE O.S.                                                  LSU05310
                                  533  *                                                                             LSU05320
*000320I  CB80 0A60               534          SI    R8,LODREND-LODRSTRT   CORRECT UPPER LIMIT                     LSU05330
 000324I  E620 FCE0 =000008I      535          LA    R2,LODRSTRT           LOAD START ADDRESS                        LSU05340
*000328I  C830 0A60               536          LI    R3,LODREND-LODRSTRT   GET LENGTH OF MOVE.                       LSU05350
         0000 032CI               537  MOVE.LDR EQU   *                                                             LSU05360
 00032CI  5802 4300 0000          538          L     R0,0(R2,R3)           LOAD DATA                                 LSU05370
 000332I  5008 4300 0000          539          ST    R0,0(R8,R3)           STORE DATA                                LSU05380
 000338I  2734                    540          SIS   R3,4                  DECREMENT LENGTH.                         LSU05390
*00033AI  2217                    541          BNM   MOVE.LDR              AND CONTINUE UNITL COUNTED OUT.           LSU05400
 00033CI  D100 86C4 =000A04I      542          LM    R0,RSAVE              RESTORE REGISTERS.                        LSU05410
*000340I  CA80 033E               543          AAI   R8,GET.OS-LODRSTRT    GET ADDRESS OF RELOCATED LOADER.          LSU05420
 000344I  0308                    544          BR    R8                    GO TO RELOCATED LOADER.                   LSU05430
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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          0000 0346I            546  GET.OS   EQU   *                                                  LSU05450
000346I   D000 86BA =000A04I    547            STM   R0,RSAVE          SAVE ALL REGISTERS.             LSU05460
00034AI                         548            IFZ   TEST                                             LSU05470
00034AI   24D0                  549            LIS   R13,0             GET START ADDRESS.              LSU05480
                                550            ELSE                                                   LSU05490
                                552            ENDC                                                   LSU05510
00034CI   5820 8708 =000A58I    553            L     R2,ENDLODR        GET END ADDRESS.                LSU05520
000350I   41E0 82AE =000602I    554            BAL   R14,MEM.TEST      TEST MEMORY THAT HELD LOADER.   LSU05530
000354I   D100 86AC =000A04I    560            LM    R0,RSAVE          RESTORE ALL REGISTERS.          LSU05590
000358I   2781                  561            SIS   R8,1              GET END ADDRESS OF O.S.         LSU05600
00035AI   2470                  562            LIS   R7,0              GET START ADDRESS OF O.S.       LSU05610
00035CI   41E0 8004 =000364I    563            BAL   R14,READ          GO READ THE O.S.                LSU05620
          0000 0360I            564  EXEC.OS  EQU   *                                                  LSU05630
000360I   4300 0060             565            B     OS.START          EXECUTE THE O.S.                LSU05640
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                0000 0364I                  567  READ      EQU   *                                                    LSU05660
 000364I  0855                              568               LR    R5,R5              MAG TAPE O.S.?                 LSU05670
 000366I  4210 FDDA =000144I                569               BM    MAG.READ           YES, THEN READ FROM MAG TAPE.  LSU05680
 00036AI  C550 0006                         570               CLHI  R5,X'37'-X'34'*2   NO, IS IT A FLOPPY DISC?       LSU05690
 00036EI  4330 8118 =00048AI                571               BE    FLP.READ           YES, GO TO FLOPPY READ ROUTINE. LSU05700
 000372I  08AC                              572               LR    R10,R12            NO, SET-UP CYLINDER:TRACK:SECTOR. LSU05710
? 000374I  4DA5 8450 =0007C8I               573               DH    R10,SECCYL(R5)                                 LSU05720
 000378I  089B                              574               LR    R9,R11             (R9) = CYLINDER.            LSU05730
? 00037AI  4DA5 8450 =0007CEI               575               DH    R10,SECTRK(R5)     (R10) = SECTOR.             LSU05740
                                            576  *                                       (R11) = TRACK.              LSU05750
 00037EI  0855                              577               LR    R5,R5              IS IT 67 MB OR LARGER?      LSU05760
 000380I  4220 8038 =0003BCI                578               BP    RDSK2                                          LSU05770
                                            579  *                                                                   LSU05780
                                            580  * 2.5 OR 10 MB DISK INPUT ROUTINE                                   LSU05790
                                            581  *                                                                   LSU05800
 000384I  DE30 8438 =0007C0I                582               OC    R3,CTRESET         RESET CONTROLLER            LSU05810
 000388I  4240 8136 =0004C2I                583               BTC   4,DU               IF FALSE SYNC - NO CONTROLLER. LSU05820
                0000 038CI                  584  WAIT10    EQU   *                                                    LSU05830
 00038CI  9D3F                              585               SSR   R3,R15             GET CONTROLLER STATUS       LSU05840
 00038EI  2221                              586               BFBS  2,WAIT10           AND WAIT FOR IDLE.          LSU05850
                0000 0390I                  587  WAIT15    EQU   *                                                    LSU05860
 000390I  9D4F                              588               SSR   R4,R15             GET STATUS OF DEVICE.       LSU05870
 000392I  4210 812C =0004C2I                589               BTC   1,DU               IF UNAVAILABLE, THEN ERROR. LSU05880
 000396I  C3F0 0010                         590               THI   R15,X'10'                                      LSU05890
*00039AI  2035                              591               BNZ   WAIT15                                         LSU05900
 00039CI  11B5                              592               SLLS  R11,5                                          LSU05910
 00039EI  06AB                              593               OR    R10,R11                                        LSU05920
                0000 03A0I                  594  RDKLOOP1  EQU   *                                                  LSU05930
 0003A0I  9849                              595               WHR   R4,R9              SEND CYLINDER # TO DISC.    LSU05940
 0003A2I  4240 811C =0004C2I                596               BTC   4,DU               IF FALSE SYNC - NO DEVICE.  LSU05950
 0003A6I  DE40 8419 =0007C3I                597               OC    R4,D1SEEK          ELSE, ISSUE A SEEK.         LSU05960
                0000 03AAI                  598  WAIT11    EQU   *                                                    LSU05970
 0003AAI  9D3F                              599               SSR   R3,R15             GET CONTROLLER STATUS       LSU05980
 0003ACI  2221                              600               BFBS  2,WAIT11           AND WAIT FOR IDLE.          LSU05990
                0000 03AEI                  601  WAIT12    EQU   *                                                    LSU06000
 0003AEI  9D4F                              602               SSR   R4,R15             GET DEVICE STATUS.          LSU06010
 0003B0I  4270 8116 =0004CAI                603               BTC   7,UNRE             IF "SEEK INCOMPLETE" - ERROR. LSU06020
 0003B4I  2083                              604               BTBS  BSY,WAIT12         ELSE, WAIT FOR DISC READY.  LSU06030
 0003B6I  4160 805E =000418I                605               BAL   R6,DKCOMMON        GO TO DISC READ ROUTINE.    LSU06040
*0003BAI  220D                              606               B     RDKLOOP1           READ NEXT CYLINDER.         LSU06050
                                            607  *                                                                   LSU06060
                0000 03BCI                  608  RDSK2     EQU   *                  SET-UP READ FOR 67MB OR 256MB DISC. LSU06070
 0003BCI  9D4F                              609               SSR   R4,R15             GET STATUS OF DEVICE.       LSU06080
 0003BEI  C3F0 0019                         610               THI   R15,X'19'          SAFE? READY? ON-LINE?       LSU06090
 0003C2I  4230 8104 =0004CAI                611               BNZ   UNRE               NO, ERROR.                  LSU06100
 0003C6I  C5F0 0004                         612               CLHI  R15,X'04'          IS DEVICE AVAILABLE?        LSU06110
 0003CAI  4330 80F4 =0004C2I                613               BE    DU                 NO, ERROR.                  LSU06120
                0000 03CEI                  614  RDKLOOP2  EQU   *                                                  LSU06130
 0003CEI  DE40 83F2 =0007C4I                615               OC    R4,D2RATTN         RESET ATTENTION FLIP FLOP   LSU06140
                0000 03D2I                  616  WAIT21    EQU   *                                                    LSU06150
 0003D2I  9D3F                              617               SSR   R3,R15             GET CONTROLLER STATUS.      LSU06160
 0003D4I  C5F0 0004                         618               CLHI  R15,X'04'          FALSE SYNC?                 LSU06170
 0003D8I  4330 80E6 =0004C2I                619               BE    DU                 YES, THEN ERROR.            LSU06180
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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0003DCI  2225                    620          BFBS  2,WAIT21          NO, WAIT FOR CONTROLLER IDLE.          LSU06190
0003DEI  9849                    621          WHR   R4,R9             SEND CYLINDER # TO DEVICE.             LSU06200
0003E0I  DE40 83E2 =0007C6I      622          OC    R4,D2SETCYL       SET CYLINDER.                          LSU06210
         0000 03E4I              623  WAIT22  EQU   *                                                        LSU06220
0003E4I  9D3F                    624          SSR   R3,R15            GET CONTROLLER STATUS                  LSU06230
0003E6I  2221                    625          BFBS  2,WAIT22          AND WAIT FOR IDLE.                     LSU06240
0003E8I  DE40 83D9 =0007C5I      626          OC    R4,D2RHEAD        CLEAR HEAD REGISTER.                   LSU06250
         0000 03ECI              627  WAIT23  EQU   *                                                        LSU06260
0003ECI  9D3F                    628          SSR   R3,R15            GET CONTROLLER STATUS                  LSU06270
0003EEI  2221                    629          BFBS  2,WAIT23          AND WAIT FOR IDLE.                     LSU06280
0003F0I  984B                    630          WHR   R4,R11            SEND HEAD # TO DEVICE.                 LSU06290
0003F2I  DE40 83D1 =0007C7I      631          OC    R4,D2SETHED       SET HEAD.                              LSU06300
         0000 03F6I              632  WAIT24  EQU   *                                                        LSU06310
0003F6I  9D3F                    633          SSR   R3,R15            GET CONTROLLER STATUS                  LSU06320
0003F8I  2221                    634          BFBS  2,WAIT24          AND WAIT FOR IDLE.                     LSU06330
0003FAI  DE40 83C5 =0007C3I      635          OC    R4,D2SEEK         ISSUE A SEEK.                          LSU06340
         0000 03FEI              636  WAIT25  EQU   *                                                        LSU06350
0003FEI  9D3F                    637          SSR   R3,R15            GET CONTROLLER STATUS                  LSU06360
000400I  2221                    638          BFBS  2,WAIT25          AND WAIT FOR IDLE.                     LSU06370
         0000 0402I              639  WAIT26  EQU   *                                                        LSU06380
000402I  9D4F                    640          SSR   R4,R15            GET DEVICE STATUS                      LSU06390
000404I  2081                    641          BTBS  BSY,WAIT26        AND WAIT FOR NOT BUSY.                 LSU06400
000406I  C3F0 0053               642          THI   R15,X'53'         UNSAFE? SEEK INC? NOT READY?           LSU06410
00040AI  4230 80BC =0004CAI      643          BNZ   UNRE              IF ANY, THEN ERROR.                    LSU06420
00040EI  08DB                    644          LR    R13,R11           ELSE, GET TRACK #,                     LSU06430
000410I  11DA                    645          SLLS  R13,10            AND COMBINE WITH CYLINDER.             LSU06440
000412I  06D9                    646          OR    R13,R9            :                                      LSU06450
000414I  E660 FFB6 =0003CEI      647          LA    R6,RDKLOOP2       GET RETURN ADDRESS,                    LSU06460
*000418I                         648          B     DKCOMMON          AND READ FROM THE DISC.                LSU06470
                                 649  *                                                                      LSU06480
         0000 0418I              650  DKCOMMON EQU  *                 COMMON DISC READ ROUTINE.              LSU06490
000418I  4100 8050 =00046CI      651          BAL   R0,ADSELCH        ADDRESS THE SELCH.                     LSU06500
00041CI  0855                    652          LR    R5,R5             IS DISC 67MB OR LARGER?                LSU06510
00041EI  2124                    653          BPS   COMN1             YES.                                   LSU06520
000420I  9849                    654          WHR   R4,R9             NO, SEND THE CYLINDER #.               LSU06530
000422I  9A3A                    655          WDR   R3,R10            :   SEND THE SECTOR #.                 LSU06540
*000424I 2303                    656          B     COMN2                                                    LSU06550
                                 657  *                                                                      LSU06560
         0000 0426I              658  COMN1   EQU   *                                                        LSU06570
000426I  9A3A                    659          WDR   R3,R10                                                   LSU06580
000428I  983D                    660          WHR   R3,R13                                                   LSU06590
         0000 042AI              661  COMN2   EQU   *                                                        LSU06600
00042AI  DE30 8394 =0007C2I      662          OC    R3,CTREAD         READ -> CTRL                           LSU06610
00042EI  DE20 838F =0007C1I      663          OC    R2,SHGORD         GO & READ -> SELCH                     LSU06620
000432I  9D3F                    664          SSR   R3,R15            IF NOT FALSE SYNC ON CONTROLLER,       LSU06630
000434I  C5F0 0004               665          CLHI  R15,X'04'         THEN CONFIG ERROR.                     LSU06640
000438I  4230 8096 =0004D2I      666          BNE   CNFG              :                                      LSU06650
         0000 043CI              667  WAIT31  EQU   *                                                        LSU06660
00043CI  9D2F                    668          SSR   R2,R15            WAIT FOR SELCH NOT BUSY.               LSU06670
00043EI  2081                    669          BTBS  BSY,WAIT31        :                                      LSU06680
000440I  DE20 837C =0007C0I      670          OC    R2,SHCLEAR        CLEAR THE SELCH.                       LSU06690
000444I  9B20                    671          RDR   R2,R0             READ 1ST BYTE OF END ADR (0:23<-0)     LSU06700
000446I  992D                    672          RHR   R2,R13            READ THE REST OF END ADR (0:16<-0)     LSU06710
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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000448I  3400                    673           EXHR   R0,R0          SHIFT 1ST BYTE LEFT BY 1 HALFWORD.      LSU06720
00044AI  060D                    674           OR     R0,R13         GET FULL ENDING ADDRESS.                LSU06730
         0000 044CI              675  WAIT32   EQU    *                                                      LSU06740
00044CI  9D3F                    676           SSR    R3,R15         GET CONTROLLER STATUS                   LSU06750
00044EI  2221                    677           BFBS   2,WAIT32       AND WAIT FOR IDLE.                      LSU06760
000450I  4210 8076 =0004CAI      678           BTC    1,UNRE         IF DATA TRANSFER ERROR - ERROR.         LSU06770
000454I  C3F0 0010               679           THI    R15,X'10'      CYLINDER OVERFLOW?                      LSU06780
000458I  033E                    680           BZR    R14            NO, RETURN                              LSU06790
00045AI  0B07                    681           SR     R0,R7          YES, GET LENGTH OF DATA BLOCK READ.     LSU06800
00045CI  2604                    682           AIS    R0,4           :                                       LSU06810
00045EI  C400 FF00               683           NHI    R0,X'FF00'     ADJUST TO 256-BYTE BOUNDARY.            LSU06820
000462I  0A70                    684           AR     R7,R0          GET NEW START ADDRESS.                  LSU06830
000464I  2691                    685           AIS    R9,1           INCREMENT CYLINDER NUMBER.              LSU06840
000466I  24A0                    686           LIS    R10,0          INITIALIZE SECTOR.                      LSU06850
000468I  24B0                    687           LIS    R11,0          INITIALIZE TRACK.                       LSU06860
00046AI  0306                    688           BR     R6             SET-UP TO READ AGAIN.                   LSU06870
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
     0000 046CI            690  ADSELCH  EQU   *              ADDRESS SELCH SUBROUTINE.          LSU06890
00046CI DE20 8350 =0007C0I 691           OC    R2,SHCLEAR     CLEAR THE SELCH.                   LSU06900
00047OI 4240 804E =0004C2I 692           BTC   4,DU           IF FALSE SYNC, SELCH NOT THERE.    LSU06910
     0000 0474I            693  SLC.WAIT EQU   *                                                 LSU06920
00047AI 9D2F               694           SSR   R2,R15         GET SELCH STATUS AND               LSU06930
00047CI 2081               695           BTBS  BSY,SLC.WAIT   LOOP UNTIL NOT BUSY.               LSU06940
00047EI 3477               696           EXHR  R7,R7          SEND START ADDRESS TO SELCH.       LSU06950
000480I 9A27               697           WDR   R2,R7          :                                  LSU06960
000482I 3477               698           EXHR  R7,R7          :                                  LSU06970
000484I 9827               699           WHR   R2,R7          :                                  LSU06980
000486I 3488               700           EXHR  R8,R8          SEND END ADDRESS TO SELCH.         LSU06990
000488I 9A28               701           WDR   R2,R8          :                                  LSU07000
00048AI 3488               702           EXHR  R8,R8          :                                  LSU07010
00048CI 9828               703           WHR   R2,R8          :                                  LSU07020
00048EI 0300               704           BR    R0             RETURN TO CALLER.                  LSU07030
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                0000 048AI              706  FLP.READ EQU   *              FLOPPY READ ROUTINE.                    LSU07050
00048AI  9D4F                           707           SSR   R4,R15        IF FLOPPY NOT IDLE                      LSU07060
00048CI  4320 8032 =0004C2I             708           BFC   2,DU          THEN ERROR.                             LSU07070
00049OI  CACC 0001                      709           AHI   R12,1(R12)    CALCULATE RECORD NUMBER,                LSU07080
000494I  984C                           710           WHR   R4,R12        AND SEND IT TO THE FLOPPY.              LSU07090
000496I  4240 8028 =0004C2I             711           BTC   4,DU          IF FALSE SYNC - NO DEVICE.              LSU07100
00049AI  C8F2 0001                      712           LHI   R15,1(R2)     GET THE READ COMMAND,                   LSU07110
00049EI  9E4F                           713           OCR   R4,R15        AND SEND IT TO THE FLOPPY.              LSU07120
0004A0I  0B78                           714           SR    R7,R8         GET BUFFER INDEX.                       LSU07130
                0000 04A2I              715  FLP.DATA EQU   *                                                      LSU07140
0004A2I  9D4F                           716           SSR   R4,R15        GET STATUS.                             LSU07150
*0004A4I 2081                           717           BTC   BSY,FLP.DATA  LOOP UNITL NOT BUSY.                    LSU07160
0004A6I  DB48 4700 0000                 718           RD    R4,0(R8,R7)   READ A BYTE.                            LSU07170
0004ACI  2671                           719           AIS   R7,1          BUMP BUFFER INDEX,                      LSU07180
*0004AEI 2226                           720           BNP   FLP.DATA      AND READ UNTIL COUNTED OUT.             LSU07190
0004B0I  24F7                           721           LIS   R15,7         ISSUE STOP COMMAND.                     LSU07200
0004B2I  9E4F                           722           OCR   R4,R15        :                                       LSU07210
                0000 04B4I              723  FLP.WAIT EQU   *                                                      LSU07220
0004B4I  9D4F                           724           SSR   R4,R15        GET THE STATUS AND                      LSU07230
0004B6I  2221                           725           BFBS  2,FLP.WAIT    WAIT UNTIL IDLE.                        LSU07240
0004B8I  030E                           726           BR    R14                                                   LSU07250
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                                  728  * ERROR ROUTINES                                                                  LSU07270
                                  729  *                                                                                 LSU07280
                                  730  * FILE NOT FOUND                                                                  LSU07290
                                  731  *                                                                                 LSU07300
          0000 04BAI              732  FILNTFND EQU   *                                                                  LSU07310
 0004BAI  01F1                    733           BALR  R15,R1              OUTPUT "FILE NOT FOUND".                      LSU07320
 0004BCI  0791                    734           DC    Z(MSG3-LODRSTRT)    :                                             LSU07330
 0004BEI  4300 804C =00050EI      735           B     ERROR               COMMON ERROR ROUTINE                          LSU07340
                                  736  *                                                                                 LSU07350
          0000 04C2I              737  DU       EQU   *                                                                  LSU07360
 0004C2I  F870 4455 2020          738           LI    R7,C'DU  '          SET-UP ERROR MESSAGE.                         LSU07370
*0004C8I  2309                    739           B     IOERROR             :                                             LSU07380
                                  740  *                                                                                 LSU07390
          0000 04CAI              741  UNRE     EQU   *                                                                  LSU07400
 0004CAI  F870 554E 5245          742           LI    R7,C'UNRE'          UNRECOVERABLE ERROR.                          LSU07410
*0004D0I  2305                    743           B     IOERROR             :                                             LSU07420
                                  744  *                                                                                 LSU07430
          0000 04D2I              745  CNFG     EQU   *                                                                  LSU07440
 0004D2I  F870 434E 4647          746           LI    R7,C'CNFG'          CONFIGURATION ERROR.                          LSU07450
*0004D8I  2301                    747           B     IOERROR             :                                             LSU07460
                                  748  *                                                                                 LSU07470
          0000 04DAI              749  IOERROR  EQU   *                   I/O ERROR MESSAGE.                            LSU07480
 0004DAI  5070 82B6 =0007941      750           ST    R7,IO.TYPE          COMPLETE THE MESSAGE.                         LSU07490
 0004DEI  01F1                    751           BALR  R15,R1              OUTPUT "I/O ERROR...."                        LSU07500
 0004E0I  0784                    752           DC    Z(MSG1-LODRSTRT)    :                                             LSU07510
 0004E2I  4300 8028 =00050EI      753           B     ERROR               GO TO COMMON ERROR ROUTINE                    LSU07520
                                  754  *                                                                                 LSU07530
          0000 04E6I              755  MEM.ERR  EQU   *                   MEMORY TEST FAILED.                           LSU07540
 0004E6I  08FD                    756           LR    R15,R13             GET LEAST SIGNIFICANT BYTE.                   LSU07550
*0004E8I  10D8                    757           SRL   R13,8               SHIFT IT OFF.                                 LSU07560
 0004EAI  41E0 8096 =000584I      758           BAL   R14,HEX.ASC         CONVERT IT TO ASCII.                          LSU07570
 0004EEI  40F0 82C6 =0007B8I      759           STH   R15,MFAD+4          SAVE FOR ERROR MESSAGE.                       LSU07580
 0004F2I  08FD                    760           LR    R15,R13             GET MIDDLE BYTE OF ADDRESS.                   LSU07590
*0004F4I  10D8                    761           SRL   R13,8               SHIFT IT OFF.                                 LSU07600
 0004F6I  41E0 808A =000584I      762           BAL   R14,HEX.ASC         CONVERT IT TO ASCII.                          LSU07610
 0004FAI  40F0 82B8 =0007B6I      763           STH   R15,MFAD+2          SAVE IT FOR ERROR MESSAGE.                    LSU07620
 0004FEI  08FD                    764           LR    R15,R13             GET MOST SIGNIFICANT BYTE OF ADDR.            LSU07630
 000500I  41E0 8080 =000584I      765           BAL   R14,HEX.ASC         CONVERT IT TO ASCII.                          LSU07640
 000504I  40F0 82AC =0007B4I      766           STH   R15,MFAD            STORE IT FOR ERROR MESSAGE.                   LSU07650
 000508I  01F1                    767           BALR  R15,R1              OUTPUT "MEMCHK ERR NNNNNN".                   LSU07660
 00050AI  07A1                    768           DC    Z(MSG6-LODRSTRT)    :                                             LSU07670
*00050CI  2301                    769           B     ERROR               GO TO COMMON                                  LSU07680
                                  770  *                                                                                 LSU07690
                                  771  *       COMMON ERROR ROUTINE                                                      LSU07700
                                  772  *                                                                                 LSU07710
          0000 050EI              773  ERROR    EQU   *                                                                  LSU07720
 00050EI  E600 FAF6 =000008I      774           LA    R0,LODRSTRT         GET BASE ADDRESS OF LOADER.                   LSU07730
*000512I  C500 1000               775           CLI   R0,LSUADDR          HAS IT BEEN MOVED YET?                        LSU07740
 000516I  0330                    776           BER   R0                  NO, RESTART.                                  LSU07750
 000518I                          777           IFZ   TEST                                                              LSU07760
 000518I  8800                    778           HALT                      YES, THEN JUST HALT.                          LSU07770
                                  779           ENDC                                                                    LSU07780
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                0000 051AI                781  MSG       EQU   *                    OUTPUT MESSAGE TO CONSOLE.                LSU07800
00051AI  486F   0000                      782            LH    R6,0(R15)            GET MESSAGE ADDRESS.                      LSU07810
00051EI  26F2                             783            AIS   R15,2                GET RETURN ADDRESS.                       LSU07820
000520I  247D                             784            LIS   R7,CR                OUTPUT CARRIAGE RETURN.                   LSU07830
000522I  41E0   8018 =00053EI            785            BAL   R14,PUTC             :                                         LSU07840
000526I  247A                             786            LIS   R7,LF                OUTPUT LINE FEED.                         LSU07850
000528I  41E0   8012 =00053EI            787            BAL   R14,PUTC             :                                         LSU07860
                0000 052CI                788  MSG.PUT   EQU   *                                                            LSU07870
00052CI  D376   FAD8 =000008I             789            LB    R7,LODRSTRT(R6)      GET A CHARACTER,                          LSU07880
000530I  41E0   800A =00053EI            790            BAL   R14,PUTC             AND OUTPUT IT.                            LSU07890
000534I  2661                             791            AIS   R6,1                 BUMP THE MESSAGE POINTER.                 LSU07900
000536I  C570   00FF                      792            CLHI  R7,X'FF'             WAS LAST CHARACTER A TERMINATOR?           LSU07910
*00053AI 2037                             793            BNE   MSG.PUT              NO, OUTPUT NEXT CHARACTER.                LSU07920
00053CI  030F                             794            BR    R15                  YES, RETURN TO CALLER.                    LSU07930
                                          795  *                                                                           LSU07940
                0000 053EI                796  PUTC      EQU   *                    OUTPUT 1 CHARACTER TO CONSOLE.            LSU07950
00053EI  C840   0011                      797            LHI   R4,X'11'             GET CONSOLE OUTPUT ADDRESS.               LSU07960
000542I  C800   00AB                      798            LHI   R0,X'AB'             START THE CONSOLE.                        LSU07970
000546I  9E40                             799            OCR   R4,R0                :                                         LSU07980
                0000 0548I                800  PUTC.L1   EQU   *                                                            LSU07990
000548I  9D40                             801            SSR   R4,R0                LOOP TILL CONSOLE NOT BUSY.               LSU08000
00054AI  2081                             802            BTBS  BSY,PUTC.L1          :                                         LSU08010
00054CI  9A47                             803            WDR   R4,R7                OUTPUT THE DATA.                          LSU08020
                0000 054EI                804  PUTC.L2   EQU   *                                                            LSU08030
00054EI  9D40                             805            SSR   R4,R0                LOOP TILL CONSOLE NOT BUSY.               LSU08040
000550I  2081                             806            BTBS  BSY,PUTC.L2          :                                         LSU08050
000552I  030E                             807            BR    R14                  RETURN TO CALLER.                         LSU08060
                                          808  *                                                                           LSU08070
                0000 0554I                809  GETC      EQU   *                    READ 1 CHARACTER FROM CONSOLE.            LSU08080
000554I  C8F0   00B9                      810            LHI   R15,X'B9'            GET CONSOLE COMMAND.                      LSU08090
000558I  C840   0010                      811            LHI   R4,X'10'             GET ADDRESS OF CONSOLE INPUT.             LSU08100
00055CI  9E4F                             812            OCR   R4,R15               OUTPUT COMMAND TO CONSOLE.                LSU08110
                0000 055EI                813  GETC.BSY  EQU   *                                                            LSU08120
00055EI  9D4F                             814            SSR   R4,R15               LOOP UNTIL NOT BUSY.                      LSU08130
000560I  2081                             815            BTBS  BSY,GETC.BSY         :                                         LSU08140
000562I  9B47                             816            RDR   R4,R7                READ A BYTE.                              LSU08150
000564I  9D4F                             817            SSR   R4,R15               CHECK FOR FRAMING ERROR.                  LSU08160
000566I  C3F0   0020                      818            THI   R15,X'20'            IF TRUE, THEN EITHER BREAK OR             LSU08170
00056AI  4230   FA9A =000008I            819            BNZ   LODRSTRT             BAD CHARACTER - RESTART.                  LSU08180
00056EI  C470   007F                      820            NHI   R7,X'7F'             ASSURE 7 BITS.                            LSU08190
000572I  C570   000D                      821            CLHI  R7,CR                IS IT A CARRIAGE RETURN?                  LSU08200
*000576I 2133                             822            BNE   GETC.OK              NO, PUT IT IN REGISTER.                   LSU08210
000578I  25F1                             823            LCS   R15,1                YES, SET RETURN TO MINUS.                 LSU08220
00057AI  030E                             824            BR    R14                  RETURN TO CALLER.                         LSU08230
                                          825  *                                                                           LSU08240
                0000 057CI                826  GETC.OK   EQU   *                                                            LSU08250
00057CI  1188                             827            SLLS  R8,8                 PACK CHARACTER INTO REGISTER.             LSU08260
00057EI  0687                             828            OR    R8,R7                :                                         LSU08270
000580I  24F0                             829            LIS   R15,0                SET RETURN TO NON-MINUS.                  LSU08280
000582I  030E                             830            BR    R14                  RETURN TO CALLER.                         LSU08290
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                                  832  * CONVERSION ROUTINES.                                                                  LSU08310
                                  833  *                                                                                       LSU08320
         0000 0584I               834  HEX.ASC  EQU   *                  CONVERT HEX TO ASCII/HEX.                             LSU08330
 000584I 087F                     835           LR    R7,R15             SAVE ORIGINAL DIGITS.                                 LSU08340
 000586I 10F4                     836           SRLS  R15,4              GET LEFTMOST DIGIT AND                                LSU08350
 000588I 41A0 800C =000598I       837           BAL   R10,HEX01          CONVERT IT TO ASCII.                                  LSU08360
 00058CI 940F                     838           EXBR  R0,R15             SHIFT AND SAVE LEFTMOST CHARACTER.                    LSU08370
 00058EI 08F7                     839           LR    R15,R7             GET RIGHTMOST DIGIT AND                               LSU08380
 000590I 41A0 8004 =000598I       840           BAL   R10,HEX01          CONVERT IT TO ASCII.                                  LSU08390
 000594I 06F0                     841           OR    R15,R0             GET BOTH ASCII CHARACTERS.                            LSU08400
 000596I 030E                     842           BR    R14                RETURN TO CALLER.                                     LSU08410
                                  843  *                                                                                       LSU08420
         0000 0598I               844  HEX01    EQU   *                                                                      LSU08430
 000598I C4F0 000F                845           NHI   R15,X'F'                                                               LSU08440
 00059CI C6F0 0030                846           OHI   R15,X'30'          SET DIGIT ZONE                                      LSU08450
 0005A0I C9F0 003A                847           CHI   R15,X'3A'                                                              LSU08460
 0005A4I 028A                     848           BLR   R10                RETURN TO CALLER IF NUMERIC.                        LSU08470
 0005A6I 26F7                     849           AIS   R15,7              ELSE, SET ALPHA ZONE,                               LSU08480
 0005A8I 030A                     850           BR    R10                AND RETURN TO CALLER.                               LSU08490
                                  851  *                                                                                       LSU08500
         0000 05AAI               852  X.CONV   EQU   *                  CONVERT ASCII/HEX TO HEX.                           LSU08510
 0005AAI CB80 0040                853           SHI   R8,X'40'           STRIP OFF ALPHA ZONES.                              LSU08520
 0005AEI 2122                     854           BPS   X.CONV1            POSSIBLY IN RANGE A - F?                            LSU08530
 0005B0I 2687                     855           AIS   R8,7               NO, THEN ASSUME 0 - 9.                              LSU08540
         0000 05B2I               856  X.CONV1  EQU   *                                                                      LSU08550
 0005B2I 2689                     857           AIS   R8,9               NORMALIZE FOR HEX DIGIT.                            LSU08560
 0005B4I C580 0010                858           CLHI  R8,X'10'           DOES RESULT EXCEED 15 (X'F')?                       LSU08570
 0005B8I 028E                     859           BLR   R14                NO, RETURN TO CALLER.                               LSU08580
 0005BAI 4300 FA4A =000008I       860           B     LODRSTRT           YES, ERROR - RESTART.                               LSU08590
                                  861  *                                                                                       LSU08600
         0000 05BEI               862  ASC.HEX  EQU   *                  CONVERT ASCII/DECIMAL TO HEX.                       LSU08610
 0005BEI 245A                     863           LIS   R5,10              INITIALIZE MULTIPLIER.                              LSU08620
 0005C0I C890 0030                864           LHI   R9,X'30'           MASK FOR ASCII CODED DECIMAL.                       LSU08630
 0005C4I C8A0 00FF                865           LHI   R10,X'FF'          MASK TO ISOLATE RIGHT BYTE.                         LSU08640
 0005C8I 2701                     866           SIS   R0,1               DECREMENT COUNT.                                    LSU08650
*0005CAI 2313                     867           BNM   ASC.UNIT           IF NOT MINUS, CONVERT UNITS.                        LSU08660
 0005CCI 2470                     868           LIS   R7,0               ELSE SET VALUE TO ZERO,                             LSU08670
 0005CEI 030E                     869           BR    R14                AND RETURN TO CALLER.                               LSU08680
                                  870  *                                                                                       LSU08690
         0000 05D0I               871  ASC.UNIT EQU   *                                                                      LSU08700
 0005D0I 0878                     872           LR    R7,R8              GET UNITS POSITION.                                 LSU08710
 0005D2I 047A                     873           NR    R7,R10             :                                                   LSU08720
 0005D4I 0B79                     874           SR    R7,R9              :                                                   LSU08730
 0005D6I 2701                     875           SIS   R0,1               DECREMENT COUNT.                                    LSU08740
 0005D8I 4210 801C =0005F8I       876           BM    END.CONV           IF MINUS, UNITS ONLY.                               LSU08750
 0005DCI 9468                     877           EXBR  R6,R8              GET TENS POSITION.                                  LSU08760
 0005DEI 046A                     878           NR    R6,R10             :                                                   LSU08770
 0005E0I 0B69                     879           SR    R6,R9              :                                                   LSU08780
? 0005E2I 0C65                    880           MHR   R6,R5              MULTIPLY IT BY 10.                                  LSU08790
 0005E4I 0A76                     881           AR    R7,R6              ADD TO RESULT.                                      LSU08800
 0005E6I 2701                     882           SIS   R0,1               DECREMENT COUNT.                                    LSU08810
*0005E8I 2118                     883           BM    END.CONV           IF MINUS, NO HUNDREDS.                              LSU08820
 0005EAI 3468                     884           EXHR  R6,R8              GET HUNDREDS POSITION.                              LSU08830
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  0005ECI  046A                    885           NR    R6,R10          :                                  LSU08840
  0005EEI  0B69                    886           SR    R6,R9           :                                  LSU08850
? 0005F0I  0C65                    887           MHR   R6,R5           MULTIPLY IT BY 100.                LSU08860
? 0005F2I  0C65                    888           MHR   R6,R5           :                                  LSU08870
  0005F4I  0A76                    889           AR    R7,R6           ADD TO RESULT.                     LSU08880
 *0005F6I  2301                    890           B     END.CONV        CONVERSION DONE.                   LSU08890
                                   891  *                                                                LSU08900
           0000 05F8I              892  END.CONV EQU   *                                                  LSU08910
  0005F8I  C570 0100               893           CLHI  R7,256          IS NUMBER <= 255?                  LSU08920
  0005FCI  4380 FA08 =000008I      894           BNL   LODRSTRT        NO, THEN ERROR - RESTART.          LSU08930
  000600I  030E                    895           BR    R14             RETURN TO CALLER.                  LSU08940
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PREVIOUS WARNING ON PAGE 21

LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                                897 *                                   TEST MEMORY.                                LSU08960
          0000 0602I            898 MEM.TEST EQU   *                   ENTER WITH R13 = START ADDRESS.             LSU08970
                                899 *                                             R02 = END ADDRESS.                LSU08980
                                900 *                                                                               LSU08990
                                901 * WRITE ADDRESSES TO MEMORY.                                                   LSU09000
                                902 *                                                                               LSU09010
 000602I  50D0 83FA =000A00I    903           ST    R13,STARTA          SAVE START ADDRESS.                       LSU09020
          0000 0606I            904 WRT.ADR   EQU   *                                                             LSU09030
 000606I  50DD 0000             905           ST    R13,0(R13)          STORE ADDRESS IN ITSELF.                  LSU09040
 00060AI  05D2                  906           CLR   R13,R2              AT END YET?                               LSU09050
*00060CI  2383                  907           BNL   READ.SET            YES, READ THE ADDRESSES.                  LSU09060
 00060EI  26D4                  908           AIS   R13,4               BUMP THE POINTER,                         LSU09070
*000610I  2205                  909           B     WRT.ADR             AND WRITE NEXT ADDRESS.                   LSU09080
                                910 *                                                                               LSU09090
                                911 * READ ADDRESSES FROM MEMORY AND COMPARE.                                     LSU09100
                                912 *                                                                               LSU09110
          0000 0612I            913 READ.SET EQU   *                   SET-UP FOR READS.                         LSU09120
 000612I  58D0 83EA =000A00I    914           L     R13,STARTA          GET START ADDRESS.                        LSU09130
          0000 0616I            915 READ.ADR EQU   *                                                             LSU09140
 000616I  583D 0000             916           L     R3,0(R13)           RETRIEVE DATA (ADDRESS?).                 LSU09150
 00061AI  05D3                  917           CLR   R13,R3              IS IT CORRECT?                            LSU09160
 00061CI  4230 FEC6 =0004E6I    918           BNE   MEM.ERR             NO, THEN ABORT NOW.                       LSU09170
 000620I  0803                  919           LR    R0,R3               ASSURE FROM MEMORY AND NOT CACHE.         LSU09180
 000622I                        920           IFZ   TEST                                                          LSU09190
 000622I  DF7D 0003             921           XSTB  3(R13)              :                                         LSU09200
                                922           ENDC                                                              LSU09210
 000626I  05D2                  923           CLR   R13,R2              AT END YET?                               LSU09220
*000628I  2383                  924           BNL   WRC.SET             YES, WRITE ADDRESS COMPLEMENTS.           LSU09230
 00062AI  26D4                  925           AIS   R13,4               NO, BUMP ADDRESS POINTER.                 LSU09240
*00062CI  220B                  926           B     READ.ADR            AND CHECK NEXT LOCATION.                  LSU09250
                                927 *                                                                               LSU09260
                                928 * WRITE ADDRESS COMPLEMENT TO MEMORY.                                         LSU09270
                                929 *                                                                               LSU09280
          0000 062EI            930 WRC.SET  EQU   *                   SET-UP FOR WRITE ADDRESS COMPLEMENT.      LSU09290
*00062EI  2541                  931           LI    R4,-1               GET MASK FOR COMPLEMENT.                  LSU09300
 000630I  58D0 83CC =000A00I    932           L     R13,STARTA          GET START ADDRESS.                        LSU09310
          0000 0634I            933 WRC.ADR  EQU   *                                                             LSU09320
 000634I  083D                  934           LR    R3,R13              GET THE ADDRESS,                          LSU09330
 000636I  0734                  935           XR    R3,R4               COMPLEMENT IT.                            LSU09340
 000638I  503D 0000             936           ST    R3,0(R13)           STORE ADDRESS COMPLEMENT                  LSU09350
 00063CI  05D2                  937           CLR   R13,R2              AT END YET?                               LSU09360
*00063EI  2383                  938           BNL   RDC.SET             YES, READ ADDRESS COMPLEMENTS.            LSU09370
 000640I  26D4                  939           AIS   R13,4               NO, BUMP ADDRESS POINTER.                 LSU09380
*000642I  2207                  940           B     WRC.ADR             AND WRITE NEXT LOCATION.                  LSU09390
                                941 *                                                                               LSU09400
                                942 * READ ADDRESS COMPLEMENT FROM MEMORY AND COMPARE.                           LSU09410
                                943 *                                                                               LSU09420
          0000 0644I            944 RDC.SET  EQU   *                   SET-UP FOR READ ADDRESS COMPLEMENT.       LSU09430
 000644I  58D0 83B8 =000A00I    945           L     R13,STARTA          GET START ADDRESS.                        LSU09440
          0000 0648I            946 RDC.ADR  EQU   *                                                             LSU09450
 000648I  580D 0000             947           L     R0,0(R13)           RETRIEVE DATA (ADDRESS COMPLEMENT?).      LSU09460
 00064CI  0704                  948           XR    R0,R4               COMPLEMENT IT.                            LSU09470
 00064EI  050D                  949           CLR   R0,R13              IS IT CORRECT?                            LSU09480
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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000650I  4230 FE92 =0004E6I    950            BNE   MEM.ERR          NO, THEN ABORT NOW.                    LSU09490
000654I  0704                  951            XR    R0,R4            ASSURE FROM MEMORY AND NOT CACHE.      LSU09500
000656I                        952            IFZ   TEST                                                    LSU09510
000656I  DF7D 0003             953            XSTB  3(R13)           :                                      LSU09520
                               954            ENDC                                                          LSU09530
00065AI  05D2                  955            CLR   R13,R2           AT END YET?                            LSU09540
*00065CI 2383                  956            BNL   PAT.MTCH         YES, TRY PATTERN MATCHING NOW.         LSU09550
00065EI  26D4                  957            AIS   R13,4            NO, BUMP ADDRESS POINTER.              LSU09560
*000660I 220C                  958            B     RDC.ADR          AND CHECK NEXT LOCATION.               LSU09570
                               959  *                                                                       LSU09580
                               960  * TEST WITH DATA PATTERNS.                                             LSU09590
                               961  *                                                                       LSU09600
         0000 0662I            962  PAT.MTCH EQU   *                                                       LSU09610
000662I  C840 0024             963            LHI   R4,36            INITIALIZE INDEX TO PATTERN TABLE.     LSU09620
         0000 0666I            964  PAT.NEW  EQU   *                 GET NEW PATTERN.                       LSU09630
000666I  58D0 8396 =000A00I    965            L     R13,STARTA       GET START ADDRESS.                     LSU09640
00066AI  5804 8166 =0007D4I    966            L     R0,PATTERNA(R4)  GET A PATTERN.                         LSU09650
         0000 066EI            967  PAT.WRT  EQU   *                                                       LSU09660
00066EI  500D 0000             968            ST    R0,0(R13)        STORE THE PATTERN.                     LSU09670
000672I  05D2                  969            CLR   R13,R2           AT END YET?                            LSU09680
*000674I 2383                  970            BNL   PAT.RDST         YES, READ THEM BACK.                   LSU09690
000676I  26D4                  971            AIS   R13,4            NO, BUMP ADDRESS POINTER,              LSU09700
*000678I 2205                  972            B     PAT.WRT          AND WRITE AT NEXT LOCATION.            LSU09710
                               973  *                                                                       LSU09720
         0000 067AI            974  PAT.RDST EQU   *                 SET-UP TO READ PATTERN.                LSU09730
00067AI  58D0 8382 =000A00I    975            L     R13,STARTA       GET START ADDRESS.                     LSU09740
         0000 067EI            976  PAT.READ EQU   *                                                       LSU09750
00067EI  583D 0000             977            L     R3,0(R13)        RETRIEVE THE PATTERN.                  LSU09760
000682I  0530                  978            CLR   R3,R0            IS IT VALID?                           LSU09770
000684I  4230 FE5E =0004E6I    979            BNE   MEM.ERR          NO, THEN ABORT NOW.                    LSU09780
000688I                        980            IFZ   TEST                                                    LSU09790
000688I  DF7D 0003             981            XSTB  3(R13)           SHUT OFF CACHE.                        LSU09800
                               982            ENDC                                                          LSU09810
00068CI  2744                  983            SIS   R4,4             YES, DECREMENT PATTERN INDEX,          LSU09820
00068EI  05D2                  984            CLR   R13,R2           AT END YET?                            LSU09830
*000690I 2385                  985            BNL   PAT.CKND         YES, SEE IF ALL PATTERNS USED.         LSU09840
000692I  50ED 0000             986            ST    R14,0(R13)       ASSURE DATA BUS CLEAN.                 LSU09850
000696I  26D4                  987            AIS   R13,4            NO, BUMP ADDRESS POINTER.              LSU09860
*000698I 220D                  988            B     PAT.READ         AND CHECK NEXT LOCATION.               LSU09870
                               989  *                                                                       LSU09880
         0000 069AI            990  PAT.CKND EQU   *                                                       LSU09890
00069AI  2744                  991            SIS   R4,4             DECREMENT PATTERN INDEX.               LSU09900
00069CI  4310 FFC6 =000666I    992            BNM   PAT.NEW          AND LOOP UNTIL ALL PATTERNS USED.      LSU09910
0006A0I  030E                  993            BR    R14              RETURN TO CALLER WHEN THRU.            LSU09920
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
                          995  * DEVICE TABLE FOR CONVERTING MNEMONICS TO ADDRESSES                LSU09940
                          996  *                                                                   LSU09950
      0000 06A2I          1000 DTABLE  EQU  *                                                      LSU09990
0006A2I 0085              1001 MAG85   DC   X'85',X'40',X'00',X'F0'                               LSU10000
0006A4I 0040
0006A6I 0000
0006A8I 00F0
0006AAI 00C5              1002 MAGC5   DC   X'C5',X'41',X'00',X'F0'                               LSU10010
0006ACI 0041
0006AEI 0000
0006B0I 00F0
0006B2I 00C6              1003 MB5R    DC   X'C6',X'33',X'B6',X'F0'                               LSU10020
0006B4I 0033
0006B6I 00B6
0006B8I 00F0
0006BAI 00C7              1004 MB5F    DC   X'C7',X'32',X'B6',X'F0'                               LSU10030
0006BCI 0032
0006BEI 00B6
0006C0I 00F0
0006C2I 00EC              1005 MB67    DC   X'EC',X'35',X'EB',X'F0'                               LSU10040
0006C4I 0035
0006C6I 00EB
0006C8I 00F0
0006CAI 00E6              1006 MB256   DC   X'E6',X'36',X'E5',X'F0'                               LSU10050
0006CCI 0036
0006CEI 00E5
0006D0I 00F0
0006D2I 00C1              1007 FLPY    DC   X'C1',X'37',X'00',X'00'                               LSU10060
0006D4I 0037
0006D6I 0000
0006D8I 0000
0006DAI 0000              1008 OTHR    DC   X'0',X'0',X'0',X'0'                                   LSU10070
0006DCI 0000
0006DEI 0000
0006E0I 0000
                          1009 *                                                                  LSU10080
      0000 06E2I          1010 ADDRTABL EQU  *                                                    LSU10090
0006E2I 075B              1011         DC   Z(DNUM-LODRSTRT)                                      LSU10100
0006E4I 0761              1012         DC   Z(CODE-LODRSTRT)                                      LSU10110
0006E6I 0767              1013         DC   Z(CTLR-LODRSTRT)                                      LSU10120
0006E8I 076D              1014         DC   Z(SLCH-LODRSTRT)                                      LSU10130
0006EAI 0773              1015         DC   Z(DRNO-LODRSTRT)                                      LSU10140
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
                                1017  * MESSAGES                                                                  LSU10160
                                1018  *                                                                           LSU10170
0006ECI  3332 3030 204C 5355    1019  ID        DB    C'3200 LSU LOADER R00-00',X'FF'                             LSU10180
0006F4I  204C 4F41 4445 5220
0006FCI  5230 302D 3030 FF
                                1020  *                                                                           LSU10190
000703I                         1021        IFO   *                                                             LSU10200
000703I  00                     1022        DB    0                                                             LSU10210
                                1023        ENDC                                                                LSU10220
000704I                         1024        CNOP  4                                                             LSU10230
         0000 0704I             1025  MENU  EQU   *                                                             LSU10240
000704I  4445 5653 2020 0D0A    1026        DB    C'DEVS  ',CR,LF                                               LSU10250
         0000 070CI             1027  DEVTABLE EQU *                                                            LSU10260
00070CI  4D47 3835 2020 0D0A    1028        DB    C'MG85  ',CR,LF                                               LSU10270
000714I  4D47 4335 2020 0D0A    1029        DB    C'MGC5  ',CR,LF                                               LSU10280
00071CI  4453 3552 2020 0D0A    1030        DB    C'DS5R  ',CR,LF                                               LSU10290
000724I  4453 3546 2020 0D0A    1031        DB    C'DS5F  ',CR,LF                                               LSU10300
00072CI  4453 3637 2020 0D0A    1032        DB    C'DS67  ',CR,LF                                               LSU10310
000734I  4432 3536 2020 0D0A    1033        DB    C'D256  ',CR,LF                                               LSU10320
00073CI  464C 5059 2020 0D0A    1034        DB    C'FLPY  ',CR,LF                                               LSU10330
000744I  4F54 4852 2020 0D0A    1035  OTHER DB    C'OTHR  ',CR,LF                                               LSU10340
         0000 074CI             1036  DEVTBLND EQU  *                                                           LSU10350
00074CI  4445 5649 4345 3DFF    1037        DB    C'DEVICE=',X'FF'                                              LSU10360
000754I                         1041        CNOP  4                                                             LSU10400
         0000 0754I             1042  VOLFIL  EQU   *                                                           LSU10410
000754I  564F 4C3D 5858 5858    1043        DB    C'VOL=XXXX,FILE=',X'FF'                                       LSU10420
00075CI  2C46 494C 453D FF
000763I  4445 5623 3DFF         1044  DNUM  DB    C'DEV#=',X'FF'                                                LSU10430
000769I  434F 4445 3DFF         1045  CODE  DB    C'CODE=',X'FF'                                                LSU10440
00076FI  4354 4C52 3DFF         1046  CTLR  DB    C'CTLR=',X'FF'                                                LSU10450
000775I  534C 4348 3DFF         1047  SLCH  DB    C'SLCH=',X'FF'                                                LSU10460
00077BI  4452 5623 3DFF         1048  DRNO  DB    C'DRV#=',X'FF'                                                LSU10470
                                1049  *                                                                         LSU10480
         0000 0781I             1050  FMKS  EQU   *                                                             LSU10490
000781I  4649 4C45 4D41 524B    1051        DB    C'FILEMARKS=',X'FF'                                           LSU10500
000789I  533D FF
                                1052  *                                                                         LSU10510
00078CI                         1056        CNOP  4                                                             LSU10550
00078CI  494F 4552 524F 5220    1057  MSG1  DB    C'IOERROR '                                                   LSU10560
000794I  5858 5858 FF           1058  IO.TYPE DB  C'XXXX',X'FF'                                                 LSU10570
000799I  4649 4C45 204E 4F54    1059  MSG3  DB    C'FILE NOT FOUND',X'FF'                                       LSU10580
0007A1I  2046 4F55 4E44 FF
0007A8I                         1060        IFE   *                                                             LSU10590
0007A8I  00                     1061        DB    0                                                             LSU10600
                                1062        ENDC                                                                LSU10610
0007A9I  4D45 4D54 5354 2045    1063  MSG6  DB    C'MEMTST ERR '                                                LSU10620
0007B1I  5252 20
0007B4I  5858 5959 5A5A FF      1064  MFAD  DB    C'XXYYZZ',X'FF'                                               LSU10630
                                1065  *                                                                         LSU10640
0007BBI                         1066        IFZ   TEST                                                          LSU10650
0007BBI  EE                     1067  COM2  DB    X'EE'             PASLA, 8-BIT, HI SPD, 2 STOP, EVEN        LSU10660
                                1068        ELSE                                                                LSU10670
                                1070        ENDC                                                                LSU10690
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
0007BCI  A3                    1071  MTSKIP   DB    X'A3'              SKIP FILEMARK (MAG TAPE).                LSU10700
0007BDI  A0                    1072  MTCLEAR  DB    X'A0'              CLEAR CONTROL UNIT (MAG TAPE).           LSU10710
0007BEI  A1                    1073  MTREAD   DB    X'A1'              READ COMMAND (MAG TAPE).                 LSU10720
0007BFI  B8                    1074  MTREWD   DB    X'B8'              REWIND COMMAND (MAG TAPE).               LSU10730
0007C0I  48                    1075  SHCLEAR  DB    X'48'              SELCH CLEAR COMMAND.                     LSU10740
0007C1I  70                    1076  SHGORD   DB    X'70'              SELCH READ/GO COMMAND                    LSU10750
         0000 07C0I            1077  CTRESET  EQU   SHCLEAR           CONTROLLER RESET COMMAND                 LSU10760
0007C2I  C1                    1078  CTREAD   DB    X'C1'                                                       LSU10770
                               1079  * DISC COMMANDS                                                          LSU10780
0007C3I  C2                    1080  D1SEEK   DB    X'C2'                                                       LSU10790
         0000 07C3I            1081  D2SEEK   EQU   D1SEEK                                                     LSU10800
0007C4I  C8                    1082  D2RATTN  DB    X'C8'                                                       LSU10810
0007C5I  C4                    1083  D2RHEAD  DB    X'C4'                                                       LSU10820
0007C6I  D0                    1084  D2SETCYL DB    X'D0'                                                       LSU10830
0007C7I  E0                    1085  D2SETHED DB    X'E0'                                                       LSU10840
                               1089  *                                                                        LSU10880
0007C8I  0030                  1090  SECCYL   DC    H'48'              <= 10                                    LSU10890
0007CAI  0140                  1091         DC    H'320'             67                                       LSU10900
0007CCI  04C0                  1092         DC    H'1216'            256                                      LSU10910
                               1093  *                                                                        LSU10920
0007CEI  0018                  1094  SECTRK   DC    H'24'              <= 10                                    LSU10930
0007D0I  0040                  1095         DC    H'64'              67                                       LSU10940
0007D2I  0040                  1096         DC    H'64'              256                                      LSU10950
                               1097  *                                                                        LSU10960
0007D4I                        1098         CNOP  4                                                          LSU10970
0007D4I  0000 0000             1099  PATTERNA DCY   0,11111111,33333333,77777777                             LSU10980
0007D8I  1111 1111
0007DCI  3333 3333
0007E0I  7777 7777
0007E4I  FFFF 0000             1100         DCY   FFFF0000,FFFF,F000F000,FF00FF00                            LSU10990
0007E8I  0000 FFFF
0007ECI  F000 F000
0007F0I  FF00 FF00
0007F4I  FFF0 FFF0             1101         DCY   FFF0FFF0,FFFFFFFF                                          LSU11000
0007F8I  FFFF FFFF
                               1102  *                                                                        LSU11010
         0000 07F4             1103  LENGTH   EQU   *-LODRSTRT                                               LSU11020
0007FCI                        1104         CNOP  4                                                          LSU11030
         0000 07FCI            1105  VDBUF    EQU   *                                                         LSU11040
         0000 08FBI            1106  VDBUFE   EQU   VDBUF+255                                                LSU11050
         0000 07FCI            1107  VD.VOL   EQU   VDBUF                                                    LSU11060
         0000 0800I            1108  VD.ATRB  EQU   VD.VOL+4                                                 LSU11070
         0000 0804I            1109  VD.FDP   EQU   VD.ATRB+4                                                LSU11080
         0000 0808I            1110  VD.OSP   EQU   VD.FDP+4                                                 LSU11090
         0000 080CI            1111  VD.OSS   EQU   VD.OSP+4                                                 LSU11100
         0000 0810I            1112  VD.MAP   EQU   VD.OSS+4                                                 LSU11110
         0000 08FCI            1113  DIRSAVE  EQU   VDBUFE+1                                                 LSU11120
         0000 0900I            1114  LIBBUFF  EQU   DIRSAVE+4                                                LSU11130
         0000 09FFI            1115  LIBBUFFE EQU   LIBBUFF+255                                              LSU11140
         0000 0A00I            1116  STARTA   EQU   LIBBUFFE+1                                              LSU11150
         0000 0A04I            1117  RSAVE    EQU   STARTA+4                                                 LSU11160
         0000 0A44I            1118  TBNTRY   EQU   RSAVE+64                                                 LSU11170
         0000 0A48I            1119  TPOFF    EQU   TBNTRY+4                                                 LSU11180
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
0000 0A4CI          1120  SWITCH    EQU   TPOFF+4                    LSU11190
0000 0A50I          1121  OS.END    EQU   SWITCH+4                   LSU11200
0000 0A54I          1122  NUM.LIBS  EQU   OS.END+4                   LSU11210
0000 0A58I          1123  ENDLODR   EQU   NUM.LIBS+4                 LSU11220
0000 0A5CI          1124  FILENAME  EQU   ENDLODR+4                  LSU11230
0000 0A64I          1125  EXT       EQU   FILENAME+8                 LSU11240
0000 0A68I          1126  LODREND   EQU   EXT+4                      LSU11250
```

SYMBOL TABLE / CROSS-REFERENCE

0007FCI 1128 END LSU11270

SYMBOL TABLE / CROSS-REFERENCE

ASSEMBLED BY CAL 03-066R07-00 (32-BIT)

START OPTIONS: NDISC,NLSTC

NO CAL ERRORS
5 CAL WARNINGS PREVIOUS WARNING ON PAGE 22
10 PASSES

ABSTOP	0000 0000												
ACT.END	0000 0262I	450	454*										
ADC	0000 0004												
ADDRTABL	0000 06E2I	231	1010*										
ADSELCH	0000 046CI	346	651	690*									
AMAGTE	0000 0174I	353	357	359*									
ASC.HEX	0000 05BEI	313	455	862*									
ASC.UNIT	0000 05D0I	867	871*										
BINDV	0000 0078	113*											
BMP.ITEM	0000 00BCI	253	265	269	271	273*							
BSY	0000 0008	117*	383	604	641	669	695	717	802	806	815		
CALC.SIZ	0000 02F8I	506	514*										
CHK.ITEM	0000 0080I	239	245*										
CK.DISC	0000 01D4I	291	396*										
CK.DISC1	0000 01DEI	398	402*										
CK.ENTRY	0000 0284I	468*	484										
CK.NAME	0000 002EI	206*	211										
CNFG	0000 04D2I	380	666	745*									
CODE	0000 0769I	1012	1045*										
COM2	0000 07BBI	192	1067*										
COMN1	0000 0426I	653	658*										
COMN2	0000 042AI	656	661*										
CR	0000 000D	115*	784	821	1026	1028	1029	1030	1031	1032	1033	1034	1035
CTLR	0000 076FI	1013	1046*										
CTREAD	0000 07C2I	662	1078*										
CTRESET	0000 07C0I	582	1077*										
D1SEEK	0000 07C3I	597	1080*	1081									
D2RATTN	0000 07C4I	615	1082*										
D2RHEAD	0000 07C5I	626	1083*										
D2SEEK	0000 07C3I	635	1081*										
D2SETCYL	0000 07C6I	622	1084*										
D2SETHED	0000 07C7I	631	1085*										
DEVTABLE	0000 070CI	204	216	1027*									
DEVTBLND	0000 074CI	205	1036*										
DIR	0000 0030	109*	109										
DIR.ACT	0000 000B	109*											
DIR.ATRB	0000 0024	109*	469										
DIR.BKSZ	0000 0025	109*											
DIR.CSEC	0000 0028	109*											
DIR.DATE	0000 0018	109*											
DIR.EXN	0000 0028	109*											
DIR.EXT	0000 0008	109*	479										
DIR.FLBA	0000 000C	109*	491	510									
DIR.FNM	0000 0000	109*	475	477									
DIR.INBS	0000 0026	109*											

SYMBOL TABLE / CROSS-REFERENCE

```
DIR.KEYS   0000 0014        109*
DIR.LLBA   0000 0010        109*   511
DIR.LRCL   0000 0016        109*
DIR.LUSE   0000 001C        109*
DIR.MEFX   0000 0027        109*
DIR.MFLG   0000 0026        109*
DIR.PSWD   0000 002C        109*
DIR.PVOL   0000 002C        109*
DIR.RCNT   0000 0022        109*
DIR.RKEY   0000 0015        109*
DIR.RSAS   0000 00F4        109*
DIR.WCNT   0000 0020        109*
DIR.WKEY   0000 0014        109*
DIRA.ACB   0000 0003        109*
DIRA.ACM   0000 0010        109*   470
DIRA.ALB   0000 0007        109*
DIRA.ALM   0000 0001        109*
DIRA.FTM   0000 00E0        109*
DIRA.UPB   0000 0006        109*
DIRA.UPM   0000 0002        109*
DIRSAVE    0000 08FCI       495    509   1113*  1114
DISC.OS    0000 02E8I       502    508*
DKCOMMON   0000 0418I       605    648    650*
DNUM       0000 0763I      1011   1044*
DRNO       0000 077BI      1015   1048*
DTABLE     0000 06A2I       256    258    285   1000*
DU         0000 04C2I       298    300    583    589    596    613    619    692    708    711    737*
END.CODE   0000 00AAI       259    263*
END.CONV   0000 05F8I       876    883    890    892*
END.FMKS   0000 011EI       308    312*
ENDLODR    0000 0A58I       529    553   1123*  1124
ERROR      0000 050EI       735    753    769    773*
EXEC.OS    0000 0360I       369    393    564*
EXT        0000 0A64I       419    421    435    456   1125*  1126
FILENAME   0000 0A5CI       418    422    474   1124*  1125
FILNTFND   0000 04BAI       488    732*
FLP.DATA   0000 04A2I       715*   717    720
FLP.READ   0000 048AI       571    706*
FLP.WAIT   0000 04B4I       723*   725
FLPY       0000 06D2I      1007*
FMKS       0000 0781I       304   1050*
FMKS.DON   0000 0138I       317    324*
FOUND.NM   0000 003EI       208    214*
GET.ACT    0000 0250I       429    440    445*
GET.ACT1   0000 0254I       448*   453
GET.EXT    0000 0236I       427    434*
GET.EXT1   0000 023AI       436*   443
GET.FILE   0000 026AI       425    438    457    459*
GET.FLNM   0000 0218I       423*   432
GET.FMKS   0000 0110I       306*   311
GET.ITEM   0000 006EI       236*   243
GET.OS     0000 0346I       543    546*
GETC       0000 0554I       202    238    307    424    437    449    809*
```

SYMBOL TABLE / CROSS-REFERENCE

```
GETC.BSY   0000 055EI      813*   815
GETC.OK    0000 057CI      822    826*
GETNAME    0000 0020I      201*   203
HEX.ASC    0000 0584I      758    762    765    834*
HEX0i      0000 0598I      837    840    844*
ID         0000 06ECI      197   1019*
IMPTOP     0000 07FCI     1128
IO.TYPE    0000 0794I      750   1058*
IOERROR    0000 04DAI      739    743    747    749*
LADC       0000 0002
LENGTH     0000 07F4       142   1103*
LF         0000 000A       116*   786   1026   1028   1029   1030   1031   1032   1033   1034   1035
LIB        0000 0100       110*   110
LIB.CTOP   0000 0064       110*
LIB.DATE   0000 0050       110*
LIB.DUMN   0000 002C       110*
LIB.FW2    0000 0010       110*   110
LIB.FW3    0000 0014       110*
LIB.HIS    0000 003C       110*
LIB.IPRI   0000 0005       110*
LIB.IRN    0000 0001       110*
LIB.ITSW   0000 0018       110*
LIB.MPRI   0000 0004       110*
LIB.NASN   0000 0003       110*   110
LIB.NCOM   0000 0007       110*
LIB.NIOQ   0000 0060       110*
LIB.NLIB   0000 0001       110*   110    500
LIB.NLSG   0000 0008       110*
LIB.NLU    0000 0002       110*
LIB.OPT    0000 000A       110*
LIB.OPT0   0000 0010       110*   110
LIB.OPT1   0000 0012       110*
LIB.OV     0000 0005       110*
LIB.PREG   0000 0006       110*
LIB.PRN    0000 0024       110*
LIB.PSIZ   0000 0020       110*
LIB.RL     0000 0003       110*
LIB.RREG   0000 0003       110*
LIB.SEGN   0000 0020       110*   110    110
LIB.SEGS   0000 000C       110*   503
LIB.SEGT   0000 0000       110*
LIB.TA     0000 0001       110*
LIB.TATR   0000 0009       110*
LIB.TC     0000 0004       110*
LIB.TIME   0000 0058       110*
LIB.UTOP   0000 0068       110*
LIB.VARL   0000 006C       110*
LIBBUFF    0000 0900I      326    496    500    503   1114*  1115
LIBBUFFE   0000 09FFI      327    497   1115*  1116
LODREND    0000 0A68I      526    528    534    536   1126*
LODRSTRT   0000 0008I      190*   197    199    212    234    257    304    415    526    534    535    536    543
                           734    752    768    774    789    819    860    894   1011   1012   1013   1014   1015
                          1103
```

SYMBOL TABLE / CROSS-REFERENCE

LOPT.ACB	0000 0001	110*						
LOPT.ACM	0000 4000	110*	110					
LOPT.ALM	0000 FFC3	110*						
LOPT.CMB	0000 0005	110*						
LOPT.CMM	0000 0400	110*	110					
LOPT.CTB	0000 0004	110*						
LOPT.CTM	0000 0800	110*	110					
LOPT.DFB	0000 0007	110*						
LOPT.DFM	0000 0100	110*	110					
LOPT.ETB	0000 0000	110*						
LOPT.ETM	0000 8000	110*	110					
LOPT.FPB	0000 0002	110*						
LOPT.FPM	0000 2000	110*	110					
LOPT.HWB	0000 000F	110*						
LOPT.HWM	0000 0001	110*	110					
LOPT.MRB	0000 0003	110*						
LOPT.MRM	0000 1000	110*	110					
LOPT.OM1	0000 F000	110*	110					
LOPT.OM2	0000 0F00	110*	110					
LOPT.OM3	0000 00C0	110*	110					
LOPT.OM4	0000 0003	110*	110					
LOPT.OVB	0000 0009	110*						
LOPT.OVM	0000 0040	110*	110					
LOPT.RLB	0000 0008	110*						
LOPT.RLM	0000 0080	110*	110					
LOPT.S6B	0000 0006	110*						
LOPT.S6M	0000 0200	110*	110					
LOPT.UVB	0000 000E	110*						
LOPT.UVM	0000 0002	110*	110					
LSU	0000 0001	1*	4	137				
LSUADDR	0000 1000	112*	140	141	142	775		
MAG.READ	0000 0144I	328	342*	345	358	364	373	569
MAG85	0000 06A2I	1001*						
MAGC5	0000 06AAI	1002*						
MAGRD.OS	0000 0184I	350	366*					
MAGTAPE	0000 00E8I	292*						
MB256	0000 06CAI	1006*						
MB5F	0000 06BAI	1004*						
MB5R	0000 06B2I	1003*						
MB67	0000 06C2I	1005*						
MEM.ERR	0000 04E6I	755*	918	950	979			
MEM.TEST	0000 0602I	530	554	898*				
MENU	0000 0704I	199	1025*					
MFAD	0000 07B4I	759	763	766	1064*			
MOVE.LDR	0000 032CI	537*	541					
MSG	0000 051AI	194	781*					
MSG.PUT	0000 052CI	788*	793					
MSG1	0000 078CI	752	1057*					
MSG3	0000 0799I	734	1059*					
MSG6	0000 07A9I	768	1063*					
MTCLEAR	0000 07BDI	297	1072*					
MTREAD	0000 07BEI	376	1073*					
MTREWD	0000 07BFI	301	1074*					

SYMBOL TABLE / CROSS-REFERENCE

SYMBOL TABLE / CROSS-REFERENCE

SYMBOL TABLE / CROSS-REFERENCE

```
VD.ATRB    0000 0800I      1108*  1109
VD.FDP     0000 0804I       461   1109*  1110
VD.MAP     0000 0810I      1112*
VD.OSP     0000 0808I      1110*  1111
VD.OSS     0000 080CI      1111*  1112
VD.READ    0000 01E0I       400    404    406*
VD.VOL     0000 07FCI       412   1107*  1108
VDBUF      0000 07FCI       407    464    466    485   1105*  1106   1107
VDBUFE     0000 08FBI       408   1106*  1113
VECTOR     0000 004EI       218    222*
VCLFIL     0000 0754I       413    415   1042*
WAIT.FM    0000 012AI       318*   321
WAIT.MAG   0000 01B2I       381*   383
WAIT10     0000 038CI       584*   586
WAIT11     0000 03AAI       598*   600
WAIT12     0000 03AEI       601*   604
WAIT15     0000 0390I       587*   591
WAIT21     0000 03D2I       616*   620
WAIT22     0000 03E4I       623*   625
WAIT23     0000 03ECI       627*   629
WAIT24     0000 03F6I       632*   634
WAIT25     0000 03FEI       636*   638
WAIT26     0000 0402I       639*   641
WAIT31     0000 043CI       667*   669
WAIT32     0000 044CI       675*   677
WRC.ADR    0000 0634I       933*   940
WRC.SET    0000 062EI       924    930*
WRT.ADR    0000 0606I       904*   909
X.CONV     0000 05AAI       240    852*
X.CONV1    0000 05B2I       854    856*
```

PROG= M3230.01 ASSEMBLED BY MICROCAL II (32-BIT)

```
                                1          SCRAT                                                                32300000
                                2  *       EDITED 012082                                                        32300010
                                3          TARGT 3230                                                           32300030
                                4  * MODEL 3230 PROCESSOR EMULATOR                                              32300040
                                5          CROSS                                                                32300050
                                6          SQCHK                                                                32300060

                                8  * COPYRIGHT PERKIN-ELMER, INC. SEPTEMBER 1979, JANUARY 1982                  32300080
                                9  * ASSEMBLER EXTENSION AND EMULATOR CODE                                      32300090
                               10  * WRITTEN BY KARL STEES KLEIN                                                32300100


 0000 0800                     12  WCSLO    EQU   '800'              WCS STARTING ADDRESS                      32300120
 0000 0000                     13  FREEWORD EQU   0                  TRACER                                    32300130


                               15  *  DROM B20:23 - 19-195F86R01(BITS 20:23)                                    32300150
                               16  *  DROM B23:27 - 19-195F87R01(BITS 24:27)                                    32300160
                               17  *  DROM B28:31 - 19-195F88R01(BITS 28:31)                                    32300170
                               18  *                                                                           32300180
                               19  *  CONTROL STORE ROMS                                                        32300190
                               20  *       B00:07 - 19-220F20R01(BITS 00:07 PAGE 0)                            32300200
                               21  *       B08:15 - 19-220F21R01(BITS 08:15 PAGE 0)                            32300210
                               22  *       B16:23 - 19-220F22R01(BITS 16:23 PAGE 0)                            32300220
                               23  *       B24:31 - 19-220F23R01(BITS 24:31 PAGE 0)                            32300230
                               24  *                                                                           32300240
                               25  *       B00:07 - 19-220F24   (BITS 00:07 PAGE 1)                            32300250
                               26  *       B08:15 - 19-220F25   (BITS 08:15 PAGE 1)                            32300260
                               27  *       B16:23 - 19-220F26   (BITS 16:23 PAGE 1)                            32300270
                               28  *       B24:31 - 19-220F27R01(BITS 24:31 PAGE 1)                            32300280
                               29  *                                                                           32300290
                               30  * FOLLOWING DESCRIPTION FOR ROMSAT/DIO SUPPORT PROG                         32300300
                               31  PAGE0    PARTS 19-220F20R01,19-220F21R01,19-220F22R01,19-220F23R01 R01*     32300310
                               32  PAGE1    PARTS 19-220F24R00,19-220F25R00,19-220F26R00,19-220F27R01 R01*     32300320
                               33           PARTS 19-195F00R00,19-195F00R00,19-195F00R00,19-195F00R00          32300330
                               34           PARTS 19-195FXXR00,19-195F86R00,19-195F87R01,19-195F88R01 R01*     32300340
                               35  *  FORMAT ROM    19-188F26R01                                               32300350
                               36  *                                                                           32300360
                               37  *  PRIVILEGED/ILLEGAL ROM                                                   32300370
                               38  *                19-188F25   NO WCS                                         32300380
                               39  *                19-188F27   WITH WCS                                       32300390
```

OPERATION SUPPORT

```
0000  D00E 5550          41  START   A     SR,YS,MDR,EXT+IR   VECTOR IF INTERRUPT QUEUED,          32300410
                         42  *                                USING TABLE AT '07'. LOC IS NOT     32300420
                         43  *                                INCREMENTED ON INTERRUPT.  IF       32300430
                         44  *                                MAT+MPE+BOUND, LOC HAS BEEN INCREMENT32300440
                         45  *                                BY (LENGTH) FOR INTERRUPT ON PREVIOUS32300450
                         46  *                                USER INSTRUCTION.                   32300460
                         47  *                                CALCULATE ADDRESS IS AS FOLLOWS:    32300470
                         48  *                                FOR RR, RI, 2ND OPERAND IN MAR&SR.  32300480
                         49  *                                FOR SF, YS IN MAR&SP.               32300490
                         50  *                                FOR RX, A(2ND OPERAND) IN MAR&SR.   32300500
                         51  *                                FOR RXRX, SR = A1, MAR = A2;        32300510
                         52  *                                XOP, YDI2, YSI2 RETURNED ON FIRST   32300520
                         53  *                                UNLOAD OF YDI, YSI, SR, OR LR.      32300530
                         54  *                                LOC IS INCREMENTED BY LENGTH.       32300540
                         55  *                                A HARDWARE VECTOR IS TAKEN TO '07'  32300550
                         56  *                                IF INSTRUCTION READ CAUSED ANY      32300560
                         57  *                                OF: ILLEGAL,MAT,MPE;                32300570
                         58  *                                OTHERWISE, VECTOR VIA DROM1.        32300580

                         60  * ********************************************** 32300600
                         61  *                                                32300610
                         62  *        UN-INTERRUPTABLE IDLE LOOP              32300620
                         63  *                                                32300630
                         64  * ********************************************** 32300640

0001  0CC8 4010          66  IDLE    BT    CATN+PPF,CONSER    ENTER HERE FOR WCS ESCAPE           32300660
0002  0E00 0011          67          B     IDLE,CYD&SWA       LOOP UNTIL CATN OR PPF.             32300670
0003  0000 0000          68          DC    FREEWORD                                               32300680

                         70  * FOLLOWING RELEASE OF SYSTEM CLEAR, CSAR INCREMENTS TO LOCATION 4:  32300700
                         71  *                                                32300710
0004                     72          ORG   '04'                              32300720
0004  5E00 019D          73          B     SELFTEST,ENACLK+RFAULT TEST PROCESSOR AND POWER UP     32300730

0005  0E00 3190          75  ABS.LHI B     LHI                *FOR TEST SOFTWARE. ALWAYS @'005'.* 32300750
0006  0000 0000          76          DC    FREEWORD                                               32300760
```

OPERATION SUPPORT

```
0007                    78          ORG   '07'            HARDWARE INTERRUPT VECTOR TABLE      32300780
0007  5E00 0BD0        79  IV07    B     ILEGF,ENACLK     ENTERED WHEN IR FAULTS, OR ILLEGAL.  32300790
                        80  *                              LOC IS PLUS (LENGTH)                 32300800
                        81  *                                                                   32300810
0008  5E00 0EE0        82  IV08    B     ALIGN,ENACLK     ALIGN FAULT, CURRENT INSTRUCTION;    32300820
                        83  *                              LOC IS PLUS (LENGTH).                32300830
0009  5E00 0AF0        84  IV09    B     MAT,ENACLK       MAT OR MPE, CURRENT INSTRUCTION      32300840
                        85  *                              LOC IS PLUS (LENGTH).                32300850
000A  0E00 401B        86  IV0A    B     CONSER,RCATN     CONSOLE ATTENTION, SNGL, OR PPF      32300860
                        87  *                              LOC IS CORRECT.                      32300870
000B  5E00 0880        88  IV0B    B     EPF,ENACLK       EARLY POWER FAIL                     32300880
                        89  *                              LOC IS CORRECT.                      32300890
000C  0E00 14F0        90  IV0C    B     LEVEL0           I/O INTERRUPT, ATN0.                 32300900
                        91  *                              LOC IS CORRECT.                      32300910
000D  0E00 14D0        92  IV0D    B     LEVEL1           I/O ATTENTION, ATN1.                 32300920
                        93  *                              LOC IS CORRECT.                      32300930
000E  0E00 14B0        94  IV0E    B     LEVEL2           I/O ATTENTION, ATN2.                 32300940
                        95  *                              LOC IS CORRECT.                      32300950
000F  0061 8030        96  IV0F    LI    MR1,'30'         I/O INTERRUPT, ATN3.                 32300960
0010  0E00 1500        97          B     IOINT            LOC IS CORRECT.                      32300970

                        99  * ********************************************                     32300990
                       100  *                                                                  32301000
                       101  *       INTERRUPTABLE WAIT LOOP                                    32301010
                       102  *                                                                  32301020
                       103  * ********************************************                     32301030

0011  002C F480       105  TWAIT   NI    NULL,PSW,'80',EXB  TEST PSW B16:                     32301050
0012  DC1C 0121       106  WAIT    BT    G+L,WAIT,CYD&SWA+IVJE+IR WAIT IF SET; ELSE EXIT.      32301060

0013  D05C 0050       108  EXIT    L     NULL,MDR,IR      GLOBAL EXIT.                         32301080
                       109  *                              IF MEMORY READING AT TERMINATION,    32301090
                       110  *                              FAULTS LEFT QUEUED UNTIL IR.         32301100
                       111  * ****************************************************             32301110

0014  0000 0000       113          DC    FREEWORD                                             32301130
0015  0000 0000       114          DC    FREEWORD                                             32301140
0016  0000 0000       115          DC    FREEWORD                                             32301150
                       119          ENDC                                                       32301190

0017                   121          ORG   '17'                                                32301210
0017  5E00 0C20       122  IV17    B     IIINT,ENACLK     NEVER USED                           32301220
                       123  *                              LOC IS PLUS (LENGTH)                 32301230
0018  DC20 0D10       124  IV18    BT    V,AFAUL2,IR      M3230 FLOATING PT ARITH FAULT        32301240
                       125  *                              LOC IS PLUS (LENGTH)                 32301250
                       126  *                              FLAGS ARE SAME AS RETURNED BY RCC.   32301260
```

OPERATION SUPPORT

```
                        128  * AFTER POWER IS FIRST APPLIED TO THE MACHINE, A MICROCODE BRANCH      32301280
                        129  * IS MADE TO SELFTEST. THE "FAIL" LAMP ON THE INDICATOR               32301290
                        130  * PANEL IS LIT. IF SELFTEST DOES NOT DETECT A HARDWARE ERROR, IT      32301300
                        131  * IS ASSUMED THAT THE MACHINE IS BASICALLY FUNCTIONAL. IN THIS CASE,  32301310
                        132  * A BRANCH IS TAKEN TO 'PWRUP', WHERE THE "FAIL" LAMP IS PUT OUT.     32301320
                        133  *                                                                     32301330
                        134  * IF, HOWEVER, AN ERROR IS DETECTED BY SELFTEST, THE MICROCODE        32301340
                        135  * ATTEMPTS TO LOOP ON THE INSTRUCTION WHICH DETECTED THE ERROR.       32301350
                        136  * IN THIS CASE, THE "FAIL" LAMP REMAINS LIT, WITH THE "WAIT"          32301360
                        137  * LAMP DIMLY LIT.                                                    32301370

0000 0019               139  SELFTEST EQU   *                 HARDWARE START-UP DIAGNOSTIC       32301390
0019   0E02 01A0        140           LINK  TXA1                LOAD RETURN ADDRESS                32301400
001A   009E 60D1        141  TXA1     S     SR,SR,SR,CYD&SWA+JAM SR = YDI = CC = 0; SET WAIT     32301410
001B   0C79 00E1        142           RETNT C+V+G+L,CYD&SWA     BRANCH: FLAGS WOULD NOT CLEAR      32301420
001C   0060 830F        143           LI    MR0,15,SLHA         FLAGS SHOULD BE 0010               32301430
001D   0C69 00E1        144           RETNT C+V+L,CYD&SWA       BRANCH: FLAGS SHOULD BE ZERO       32301440
001E   0E11 00E1        145           RETNF G,CYD&SWA           BRANCH: FLAG SHOULD BE SET         32301450
001F   00EF 070F        146           SBHA  FLR,MR0,LYSI+JAM    FLR = PSW = YSI = 'F'              32301460
0020   0E41 00E1        147           RETNF C,CYD&SWA           BRANCH: FLAG NOT SET               32301470
0021   0E21 00E1        148           RETNF V,CYD&SWA           BRANCH: FLAG NOT SET               32301480
0022   0E11 00E1        149           RETNF G,CYD&SWA           BRANCH: FLAG NOT SET               32301490
0023   0E09 00E1        150           RETNF L,CYD&SWA           BRANCH: FLAG NOT SET               32301500
0024   0D21 00E3        151           RETNT MSK,YDM1            BRANCH: MSK TEST SHOULD BE FALSE   32301510
0025   0F21 00E2        152           RETNF MSK,YDP1            BRANCH: MASK TEST SHOULD BE TRUE   32301520
0026   006B 00BF        153           L     CNTR,YSI,LYSI       EXECUTE NEXT INSTRUCTION 15 TIMES: 32301530
0027   008E 6D02        154           A     SR,SR,MR0,RRL+YDP1+JAM SR = 'E1', YDI = 15, CC = 2     32301540
0028   0F89 00E2        155           RETNF YDC,YDP1            BRANCH: FLAG SHOULD BE SET         32301550
0029   0D89 00E0        156           RETNT YDC                 BRANCH: FLAG SHOULD NOT BE SET     32301560
002A   00C7 E0E1        157           XI    PSW,SR,'E1',JAM     PSW = 0; FLAGS = 0000.             32301570
002B   0C79 00E0        158           RETNT C+V+G+L             BRANCH: FLAGS SHOULD NOT SET       32301580

002C   0000 70B5        160           A     MR0,PSW,YSI,JAMCI   MR0 = 1 (YSI=0)                   32301600
002D   0001 0005        161           A     MR1,MR0,MR0,JAMCI   MR1 = 3                            32301610
002E   0002 1015        162           A     MR2,MR1,MR1,JAMCI   MR2 = 7                            32301620
002F   0003 2025        163           A     MR3,MR2,MR2,JAMCI   MR3 = 'F'                          32301630
0030   004E 3020        164           X     SR,MR3,MR2          SR = 8                             32301640
0031   004E 6010        165           X     SR,SR,MR1           SR = B                             32301650
0032   004E 6000        166           X     SR,SR,MR0           SR = A                             32301660
0033   004E 20D0        167           X     SR,MR2,SR           SR = D                             32301670
0034   004E 6030        168           X     SR,SR,MR3           SR = 2                             32301680
0035   001E E002        169           SI    SR,SR,'02'          SR = 0                             32301690
0036   0C79 00E0        170           RETNT C+V+G+L             BRANCH: PROBABLY MICRO-REG FAILURE 32301700
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```
                          172  * ************************************************                32301720
                          173  *                                                              32301730
                          174  *       P O W E R   U P   S E Q U E N C E                      32301740
                          175  *                                                              32301750
                          176  * ************************************************             32301760

0037   5D10 065D          178  PWRUP    BT    MVF,COLDSTRT,RFAULT+ENACLK BRANCH: MEMORY POWER LOST.  32301780

0000 0038                 180  WARMSTRT EQU   *                  MEMORY STILL INTACT.         32301800
0038   0E02 0520          181           LINK  MEMTEST            TEST BASIC MEMORY            32301810
0039   0066 8084          182           LI    MAR,'84'           A(REG SAVE POINTER)          32301820
003A   E0E7 8420          183           LI    PSW,'20',EXB+JAM+PR4 SELECT REG SET 0, ENABLE MPE 32301830
003B   006E 8003          184           LI    SR,3               MASK                         32301840
003C   002E 6050          185           N     SR,SR,MDR          FORCE ALIGN 4                32301850
003D   004E 6051          186           X     SR,SR,MDR,CYD&SWA  DONE; POINT R0               32301860
003E   0006 F008          187           AI    MAR,SR,8           ADVANCE PAST STORED PSW      32301870
003F   FE02 3274          188  WARM.1   LINK  LM.ENT,DR4+I4      LOAD GENERAL REGISTER SET    32301880
0040   0087 F011          189           AI    PSW,PSW,'11',JAM   ADVANCE TO NEXT SET          32301890
0041   5C90 0AB0          190           BT    MPE,HARDSTOP,ENACLK BRANCH: SOMETHING RELOADED WRONG! 32301900
0042   0E40 03F0          191           BF    C,WARM.1           CONTINUE FOR 8 SETS.         32301910
                          192  *                                                              32301920
0043   FE02 5194          193           LINK  LM71,DR4+I4        LOAD SCRATCHPADS             32301930
                          194  *                                                              32301940
0044   0D92 57D1          195           LINKT FPP,LME.ENT,CYD&SWA LOAD SPFP REGISTERS          32301950
0045   0D92 59E1          196           LINKT FPP,LMD.ENT,CYD&SWA LOAD DPFP REGISTERS          32301960
                          197  *                                                              32301970
0046   0066 00D0          198           L     MAR,SR             POINT TO POWER-DOWN PSW      32301980
0047   F063 8440          199           LI    MR3,'40',EXB+DR4   QUEUE MALFUNCTION STATUS BIT 32301990
0048   0060 0054          200           L     MR0,MDR,I4         MR0 = PSW                    32302000
0049   F066 8028          201           LI    MAR,'28',DR4       A(CONSOLE STATUS); FETCH LOC 32302010
004A   0064 0050          202           L     LOC,MDR            LOAD NEW LOC                 32302020
004B   00E7 0000          203           L     PSW,MR0,JAM        NEW PSW (MAT DISABLED UNTIL LPSTD) 32302030
004C   5E02 1010          204           LINK  TLSU,ENACLK        TEST IF LSU ENABLED          32302040
004D   A06C 0170          205           L     NULL,NULL,PR2      FETCH CONSOLE STATUS         32302050
004E   006C 0550          206           EXT   NULL,MDR           MAKE SURE IT'S GOTTEN, THEN: 32302060
004F   5C90 0AB0          207           BT    MPE,HARDSTOP,ENACLK BRANCH: SOMETHING RELOADED WRONG! 32302070
0050   0C08 401B          208           BT    L,CONSER,RCATN     BRANCH: WAS IN CONSOLE ROUTINE. 32302080
                          209  *                                TURN OFF FAIL LIGHT.         32302090
0051   0E00 0980          210           B     TMMF               CHECK IF MALFUNCTION ENABLED. 32302100

                          212  * TEST BASIC MEMORY             (PSW = 0 HERE)               32302120
0000 0052                 213  MEMTEST  EQU   *                                              32302130
0052   0060 8000          214           LI    MR0,0              LOW MEMORY LIMIT             32302140
0053   0065 0000          215  MEMLOOP  L     MAR,MR0            TEST CELL ADDRESS            32302150
0054   E064 0060          216           L     LOC,MAR,PR4        READ DATA, SET LOC = (MAR)   32302160
0055   0061 0050          217           L     MR1,MDR            AND PRESERVE.                32302170
0056   0C88 4010          218  MEM.1    BT    CATN,CONSER        IF HUNG IN MEMORY TEST,      32302180
                          219  *                                CAN LEAVE BY DEPRESSING HALT/RUN. 32302190
                          220  *                                FAIL LAMP IS TURNED OFF.     32302200
0057   0015 8C01          221           SI    MDR,MR0,'01',EXH   WRITE DATA PATTERN          32302210
0058   6046 8404          222           XI    MAR,MR0,'04',EXB+PW4 WRITE; SET FOR READ 1K BYTES AWAY 32302220
0059   E066 0000          223           L     MAR,MR0,PR4        RE-ADDRESS TEST CELL         32302230
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OPERATION SUPPORT

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005A  E012 8C01   224          SI    MR2,MR0,'01',EXH+PR4 AND READ CONTENTS.                    32302240
005B  00CE 2050   225          X     SB,MR2,MDR,JAM       TEST DATA READ, SET CC=SR=0 (?)       32302250
005C  0C18 0550   226          BT    G+L,MEM.1            BRANCH: DID NOT RETAIN TEST DATA.     32302260
005D  0065 0010   227          L     MDR,MR1              RESTORE ORIGINAL CONTENTS             32302270
005E  6000 8004   228          AI    MR0,MR0,4,PW4        ADVANCE TO NEXT CELL                  32302280
005F  001C 8C04   229          SI    NULL,MR0,'04',EXH    AT 256 KB LIMIT ?                     32302290
0060  0C10 0530   230          BT    G,MEMLOOP            BRANCH: NOT YET.                      32302300
0061  0060 8440   231          LI    MR0,'40',EXB         SET 'POWER RESTORE'                   32302310
0062  0065 0C00   232          EXH   MDR,MR0              TO STATUS WORD @ '40'                 32302320
0063  0066 8040   233          LI    MAR,'40'             .                                     32302330
0064  6E01 00E0   234          RETN  PW4                  RETURN TO CALLER.                     32302340

0000 0065                      236  COLDSTRT EQU   *                  MEMORY POWER WAS LOST     32302360
0065    0066 0171              237           L     MAR,NULL,CYD&SWA                            32302370
0066    0065 0060              238  COLD.1   L     MDR,MAR           ADDRESS AS DATA;          32302380
0067    006F 0C60              239           EXH   FLR,MAR           AT LIMIT YET ?            32302390
0068    0C20 05A0              240           BT    V,COLD.1A         BRANCH: YES ('0004 0000') 32302400
0069    6E00 0664              241           B     COLD.1,PW4+I4     STORE, ADVANCE.           32302410
006A    0E02 0520              242  COLD.1A  LINK  MEMTEST           TEST BASIC MEMORY         32302420
                               243  *                                                           32302430
006B    0F90 06F0              244  COLD.2   BF    FPP,COLD.3        BRANCH: NO FPP.           32302440
006C    012C 00DA              245           LE    YD,SR,UNNLD       INITIALIZE SPFP REGISTERS 32302450
006D    020C 00D0              246           LW    YD,SR             INITIALIZE DPFP REGISTERS 32302460
006E    022C 00DA              247           LD    YD,SR,UNNLD       .                         32302470
006F    0468 80C2              248  COLD.3   LI    ARSYD,IIINT       INITIALIZE SCRATCHPAD REGISTERS 32302480
0070    0038 7CA0              249           O     YD,PSW,YDI,EXH    INITIALIZE GENERAL REGISTERS 32302490
0071    0F88 06B2              250           BF    YDC,COLD.2,YDP1   DO WHOLE SET               32302500
0072    0087 F011              251           AI    PSW,PSW,'11',JAM  ADVANCE TO NEXT SET       32302510
0073    0E40 06B0              252           BF    C,COLD.2          BRANCH: SETS 0:7 NOT DONE 32302520
                               253  *                                                           32302530
0074    5E02 1010              254           LINK  TLSU,ENACLK       TEST IF LSU ENABLED       32302540
0075    0014 0005              255  COLD.4   SDEC  LOC,MR0,MR0       MACHINE IN INITIAL STATE - 32302550
0076    00E7 8480              256           LI    PSW,'80',EXB+JAM  SET PSW = '00008000', LOC = 'FFFFFE' 32302560
0077    0E00 401B              257  COLD.5   B     CONSER,RCATN      AND GET USER INTERVENTION. 32302570
                               258  *                                TURN OFF FAIL LIGHT.      32302580
```

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                        260 * ************************************************** 32302600
                        261 *                                                    32302610
                        262 *       P O W E R   D O W N                          32302620
                        263 *                                                    32302630
                        264 * ************************************************** 32302640

0000 0078               266 PPF      EQU   *                  ENTERED VIA IVOA OR THROUGH CONSER 32302660
                        267 *                                 OR BY BRANCH TEST.  32302670
0078   506C 00BD        268 PWRDWN   L     NULL,YSI,RFAULT+ENACLK UNLOAD RXRX XOP  32302680
0079   0066 8084        269          LI    MAR,'84'           READ PWR FAIL PSW SAVE POINTER 32302690
007A   E06E 8003        270          LI    SR,'03',PR4        BITS TO BE IGNORED  32302700
007B   002E 6050        271          N     SR,SR,MDR          CAPTURE,            32302710
007C   0046 6050        272          X     MAP,SR,MDR         FULLWORD-ALIGNED POINTER 32302720
007D   0075 7000        273          L     MDR,PSW                                32302730
007E   6065 0044        274          L     MDR,LOC,PW4+I4     STORE CURRENT PSW   32302740
007F   60E7 0174        275          L     PSW,NULL,PW4+I4+JAM STORE CURRENT LOC, ZERO PSW 32302750
0080   0E02 3681        276 PWRDWN1  LINK  STM.ENT,CYD&SWA    SAVE GENERAL REGISTER SET 32302760
0081   0087 F011        277          AI    PSW,PSW,'11',JAM   ADVANCE TO NEXT SET. 32302770
0082   0E40 0800        278          BF    C,PWRDWN1          BRANCH: STORE ANOTHER SET. 32302780
                        279 *                                                    32302790
0083   0E02 51D0        280          LINK  STM71              SAVE SCRATCHPADS.   32302800
                        281 *                                                    32302810
0084   0D92 5771        282          LINKT FPP,STME.ENT,CYD&SWA SAVE SPFP REGISTER SET 32302820
0085   0D92 5941        283          LINKT FPP,STMD.ENT,CYD&SWA SAVE DPFP REGISTER SET 32302830
                        284 *                                                    32302840
0086   006A 8003        285 POW      LI    YDI,3              POW IS STEERED BY YDI 32302850
0087   0E00 0879        286          B     *,YDFF             POWER DOWN.         32302860


                        288 * ************************************************** 32302880
                        289 *                                                    32302890
                        290 *       MACHINE MALFUNCTION STATUS WORD BITS         32302900
                        291 *                                                    32302910
                        292 * ************************************************** 32302920

                        294 *       8000 0000 - POWER FAIL                       32302940
                        295 *       4000 0000 - POWER RESTORE                    32302950
                        296 *       2000 0000 - NON-CORRECTABLE ERROR, DATA FETCH 32302960
                        297 *       1000 0000 - NON-CORRECTABLE ERROR, INSTRUCTION FETCH 32302970
                        298 *       0800 0000 - NON-CORRECTABLE ERROR, AUTO-DRIVER CHANNEL 32302980
                        299 *       0400 0000 - NON-CONFIGURED MEMORY, DATA FETCH 32302990
                        300 *       0200 0000 - NON-CONFIGURED MEMORY, INSTRUCTION FETCH 32303000
                        301 *       0100 0000 - NON-CONFIGURED MEMORY, AUTO-DRIVER CHANNEL 32303010
                        302 *       0000 0002 - SHARED MEMORY POWER FAIL         32303020
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                        304  * ************************************************                32303040
                        305  *                                                               32303050
                        306  *        MACHINE MALFUNCTION INTERRUPT                          32303060
                        307  *                                                               32303070
                        308  * ************************************************              32303080

                        310  *                                                               32303100
                                                                 EARLY POWER FAIL INTERRUPT    32303110
0000 0088               311  EPF       EQU   *                 ENTERED VIA IV0B              32303120
0088   006A 8004        312            LI    YDI,4             SET FOR YDFF RESET EPF        32303130
0089   0063 8480        313            LI    MR3,'80',EXB      QUEUE PF REASON CODE          32303140
008A   0DA0 08D0        314            BT    EPF,EPF1          BRANCH: EPF                   32303150
0000 008B               315  SMEPF     EQU   *                 SHARED MEMORY EARLY POWER FAIL32303160
008B   006A 8005        316            LI    YDI,5             SET FOR YDFF 'RESET SMEPF'    32303170
008C   0063 8C02        317            LI    MR3,'02',EXH      QUEUE SMPF REASON CODE        32303180
008D   0E00 0989        318  EPF1      B     TMMF,YDFF         RESET EPF OR SMEPF.

                                                                 MEMORY PARITY ERROR IN CHANNEL32303200
0000 008E               320  CHANMMF   EQU   *                 QUEUE REASON CODE             32303210
008E   0063 8408        321            LI    MR3,'08',EXB      TAKE PSW SWAP.                32303220
008F   0E00 0950        322            B     MEMMF1

                                                                 MPE ON INSTRUCTION FETCH      32303240
0000 0090               324  IFETCHE   EQU   *                 ENTERED VIA IV07 THROUGH ILEGF32303250
                        325  *                                                               32303260
0090   0E02 0FC0        326            LINK  MINUSLEN          GET (LOC-LENGTH)              32303270
0091   0063 8410        327            LI    MR3,'10',EXB      QUEUE REASON CODE             32303280
0092   0E00 0950        328            B     MEMMF1            ATTEMPT SWAP.

                                                                 MPE ON DATA FETCH             32303300
0000 0093               330  DFETCHE   EQU   *                 GET (LOC-LENGTH)              32303310
0093   0E02 0FC0        331            LINK  MINUSLEN          FAULT ON SUPERVISORY DATA FETCH32303320
0000 0094               332  MEMMF     EQU   *                 ENTER HERE WHEN LOC NOT TO BE CHANGED32303330
                        333  *                                 FOR EXAMPLE, ON NEW PSW FAULT.32303340
                        334  *                                                               32303350
0094   0063 8420        335            LI    MR3,'20',EXB      QUEUE REASON CODE             32303360
0095   0F10 098D        336  MEMMF1    BF    MVF,TMMF,RFAULT   BRANCH: NOT NON-EXISTENT MEMORY32303370
0096   005B 8003        337            LI    CNTR,3                                          32303380
0097   0063 0E30        338            SRL   MR3,MR3           SHIFT FAULT CODE RIGHT 3 PLACES

0098   002C F420        340  TMMF      NI    NULL,PSW,'20',EXB TEST IF MMFINT ENABLED IN PSW 32303400
0099   0E1C 0110        341            BF    G+L,TWAIT,IVJE    BRANCH: NOT ENABLED. TEST WAIT BIT.32303410

009A   0062 0060        343  MMFINT    L     MR2,ZMAR          MEMORY FAULT ADDRESS          32303430
009B   0066 00D0        344            L     MAR,SR            TRUNCATE LM FAULT ADRS        32303440
009C   006E 0060        345            L     SR,MAR                                          32303450
009D   0066 8020        346            LI    MAR,'20'          A(MMF OLD PSW)                32303460
009E   0075 700D        347            L     MDR,PSW,RFAULT    (20-23) = OLD PSW             32303470
009F   6065 0044        348            L     MDR,LOC,PW4+I4    (24-27) = OLD LOC             32303480
00A0   6065 00D4        349            L     MDR,SR,PW4+I4     (2C-2F) = LM BLOCK START ADRS 32303490
00A1   006C 0174        350            L     NULL,NULL,I4                                    32303500
00A2   6066 8038        351            LI    MAR,'38',PW4      A(MMF NEW PSW)                32303510
00A3   E06C 0174        352            L     NULL,NULL,PR4+I4  (38-3B) = NEW PSW             32303520
00A4   E060 0054        353            L     MR0,MDR,PR4+I4    (3C-3F) = NEW LOC             32303530
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OPERATION SUPPORT

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00A5   0064 0050          354           L     LOC,MDR                                                  32303540
00A6   0065 0C30          355           EXH   MDR,MR3                  (40-43) = MMSW                    32303550
00A7   6065 0024          356           L     MDR,MR2,PW4+I4           (44-47) = MEMORY FAULT ADRS       32303560
00A8   606C 0170          357           L     NULL,NULL,PW4                                              32303570
00A9   00E7 0000          358           L     PSW,MR0,JAM              LOAD NEW PSW                      32303580
00AA   5E90 0110          359           BF    MPE,TWAIT,ENACLK         BRANCH: SWAP OK (NO IVJE ALLOWED) 32303590
00AB   0064 8040          360 HARDSTOP  LI    LOC,'40'                 POINT TO MALFUNCTION STATUS WORD  32303600
00AC   5E00 401D          361           B     CONSER,ENACLK+RFAULT DOUBLE FAULT; STOP MACHINE.           32303610

                          363 * ********************************************** 32303630
                          364 *                                                32303640
                          365 *       LOAD MULTIPLE (GEN REG) FAULT SUPPORT    32303650
                          366 *                                                32303660
                          367 * ********************************************** 32303670

0000 00AD                 369 LMFAULT   EQU   *                  FAULT IN LOAD MULTIPLE                  32303690
00AD   003E ED01          370           OI    SR,SR,'01',RRL     A(LM BLOCK), FORM 80XXXXXX              32303700
00AE   0CA0 0B10          371           BT    MAT,MAT1A          BRANCH: MAT ERROR                       32303710

                          373 * ********************************************** 32303730
                          374 *                                                32303740
                          375 *       MEMORY ACCESS CONTROLLER INTERRUPT       32303750
                          376 *                                                32303760
                          377 * ********************************************** 32303770

0000 00AF                 379 MAT       EQU   *                  ENTERED VIA IV09                        32303790
                          380 *                                  OR FROM IV07 THROUGH ILEGF.             32303800
00AF   0EA0 0930          381           BF    MAT,DFETCHE        BRANCH: REALLY PARITY ERROR             32303810
00B0   006E 0170          382 MAT1      L     SR,NULL            NOT SERVICING LM FAULT HERE -           32303820
00B1   0066 8090          383 MAT1A     LI    MAR,'90'           MEMORY READS FROM NEW PSW -             32303830
00B2   AE02 0FCD          384           LINK  MINUSLEN,PR2+RFAULT RESET FAULT; GET (LOC-LENGTH).         32303840
00B3   0063 0060          385           L     MR3,ZMAR           MR3 = FAULT ADRS FROM ZMAR              32303850
00B4   0052 0850          386           LHL   MR2,MDR            FAULT CODE, MINUS 1                     32303860
00B5   EE02 0C64          387           LINK  COMSWAP,PR4+I4     DO PSW SWAP                             32303870
00B6   0008 2175          388           AINC  YD,MR2,NULL        R13 = FAULT CODE, FORM 000000XX         32303880
00B7   006C 0173          389           L     NULL,NULL,YDM1     POINT R12                               32303890
00B8   0068 0033          390           L     YD,MR3,YDM1        R12 = FAULT ADDRESS, FORM 00XXXXXX      32303900
00B9   0066 00D0          391           L     MAR,SR             FLAG SET BY LMFAULT ?                   32303910
00BA   0E0C 0110          392           BF    L,TWAIT,IVJE       BRANCH: NO.                             32303920
00BB   0068 0060          393           L     YD,MAR             R11 = A(LM BLOCK START)                 32303930
00BC   0E04 0110          394           B     TWAIT,IVJE         GO TEST WAIT BIT.                       32303940
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                    396  * ********************************************** 32303960
                    397  *                                                32303970
                    398  *        ILLEGAL INSTRUCTION INTERRUPT           32303980
                    399  *                                                32303990
                    400  * ********************************************** 32304000

                    402  ILEGF    EQU   *                  ENTERED VIA IV07 ON D1-TIME ABORT  32304020
00BD   5CA0 0B00    403           BT    MAT,MAT1,ENACLK    BRANCH: REALLY MAT ERROR           32304030
00BE   0C90 0900    404           BT    MPE,IFETCHE        BRANCH: MPE OR NON-EXISTENT MEMORY; 32304040
                    405  *                                 ON INSTRUCTION READ.               32304050

00BF   006C 0050    407  IIINTA   L     NULL,MDR           MEMORY WAS READING AT ABORT        32304070
00C0   5EA0 0C2D    408           BF    MAT,IIINT,RFAULT+ENACLK BRANCH: NO MAT FAULT          32304080
00C1   A06C 017D    409           L     NULL,NULL,PR2+RFAULT RESET MAT FAULT                  32304090
00C2                410  IIINT    EQU   *                  ENTER FROM EMULATION OR D1 VECTOR  32304100
00C2   0E02 0FC0    411           LINK  MINUSLEN           GET (LOC-LENGTH)                   32304110
00C3   0066 8030    412  IIINT1   LI    MAR,'30'           ADRS OF ILLEGAL INSTR NEW PSW      32304120
00C4   EE02 0C64    413           LINK  COMSWAP,PR4+I4     DO PSW SWAP                        32304130
00C5   0E04 0110    414           B     TWAIT,IVJE         GO TEST WAIT BIT.                  32304140

                    416  * COMMON R14/R15 INTERRUPT PSW FETCH/SWAP ROUTINE                    32304160

00C6                418  COMSWAP  EQU   *                  MEMORY NOW READING NEW PSW         32304180
00C6   0070 7001    419           L     MR0,PSW,CYD&SWA    MR0 = OLD PSW. POINT R0.           32304190
00C7   E061 0053    420           L     MR1,MDR,PR4+YDM1   MR1 = NEW PSW. POINT R15.         32304200
00C8   006C 0050    421           L     NULL,MDR           FORCE CLOCK STOP IF FAULT          32304210
00C9   00E7 0010    422           L     PSW,MR1,JAM        LOAD NEW PSW                       32304220
00CA   0068 0043    423           L     YD,LOC,YDM1        R15 = OLD LOC                      32304230
00CB   0064 0050    424           L     LOC,MDR            LOAD NEW LOC                       32304240
00CC   0068 0003    425           L     YD,MR0,YDM1        R14 = OLD PSW                      32304250
00CD   0E91 00E0    426           RETNF MPE                RETURN TO CALLER                   32304260
00CE   5E00 0940    427           B     MEMMF,ENACLK       UNLESS SERVICE FAULT.              32304270

                    432           ENDC                                                        32304320
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                          434  * ************************************************                32304340
                          435  *                                                              32304350
                          436  *        ARITHMETIC FAULT INTERRUPT                            32304360
                          437  *                                                              32304370
                          438  * ************************************************             32304380

00CF                      440          ORG   'CF'              ALIGNS LINK ADDRESS           32304400

00CF   0E02 0D60          442  AFAUL0  LINK  AFAULT            FIX POINT DIV-BY-0            32304420
00D0   0E02 0D60          443  AFAUL1  LINK  AFAULT            FIX POINT QUOTIENT O'FLOW     32304430
00D1   0C42 0D60          444  AFAUL2  LINKT C,AFAULT          BRANCH: FLOAT DIV-BY-0.       32304440
00D2   0E1A 0D40          445  AFAUL3  LINKF G+L,UFAULT        BRANCH: FLOAT EXP UNDERFLOW   32304450
00D3   0E02 0D60          446  AFAUL4  LINK  AFAULT            FLOAT POINT EXP O'FLOW        32304460

00D4   002C F410          448  UFAULT  NI    NULL,PSW,'10',FXB AFAULT ENABLED ?              32304480
00D5   DC18 0D60          449          BT    G+L,AFAULT,IR     EXIT IF NO, ELSE:             32304490

0000 00D6                 451  AFAULT  EQU   *                                               32304510
00D6   006E 00E0          452          L     SR,LR             SR = FAULT CODE + MORE        32304520
00D7   0E02 0FC0          453          LINK  MINUSLEN          GET (LOC-LENGTH)              32304530
00D8   0066 8048          454          LI    MAR,'48'          MAR = A(ARITH FAULT NEW PSW)  32304540
00D9   EE02 0C64          455          LINK  COMSWAP,PR4+I4    DO PSW SWAP                   32304550
00DA   006A 800F          456          LI    YDI,15            POINT R15                     32304560
00DB   0060 0080          457          L     MR0,YD            MR0 = A(FAULTED INSTRUCTION)  32304570
00DC   006A 800C          458          LI    YDI,12                                          32304580
00DD   0008 00F2          459          A     YD,MR0,LENGTH,YDP1 R12 = 'NEXT LOC'; POINT R13. 32304590
00DE   0028 E007          460          NI    YD,SR,'07'        R13 = FAULT CODE              32304600
00DF   0E04 0110          461          B     TWAIT,IVJE        GO TEST WAIT BIT              32304610


                          463  *   P R I V I L E G E D   S Y S T E M   F U N C T I O N   T A B L E   32304630

00F0                      465          ORG   'E0'              ALIGNS TABLE MODULO 16        32304650
0000 00E0                 466  PSFTAB  EQU   *                 PRIVILEGED SYSTEM FUNCTION VECTORS 32304660
00E0   0E00 4EA0          467          B     REL               CODE 0                        32304670
00E1   EE00 4E90          468  LPSTD   B     LSTD1,PR4         CODE 1                        32304680
00E2   EE00 4E92          469  LSSTD   B     LSTD1,YDP1+PR4    CODE 2                        32304690
00E3   0E00 4EE3          470          B     STPS,YDM1         CODE 3                        32304700
00E4   FE00 4FD4          471          B     LDPS,DR4+I4       CODE 4                        32304710
00E5   0E00 5120          472          B     ISSV              CODE 5                        32304720
00E6   FE00 5164          473          B     ISRST,DR4+I4      CODE 6                        32304730
00E7   0065 0480          474  XSTB    EXB   MDR,YD            CODE 7                        32304740
00E8   4E00 0130          475          B     EXIT,TEL          STORE BYTE, NO ECC; GO EXIT.  32304750


                          480          ENDC                                                32304800
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                        482  * ************************************************** 32304820
                        483  *                                                    32304830
                        484  *       D A T A   F O R M A T   F A U L T            32304840
                        485  *                                                    32304850
                        486  * ************************************************** 32304860

00E9                    488          ORG   'E9'              ALIGNS LINKS        32304880

00E9   0E02 0F20        490  FORFAUL2 LINK  SPECFAUL          INVALID SIGN DIGIT, PACKED DATA 32304900
00EA   0E02 0F20        491  FORFAUL3 LINK  SPECFAUL          INVALID DATA DIGIT, PACKED DATA 32304910
00EB   0000 0000        492          DC    FREEWORD          RESERVED CODE       32304920
00EC   0000 0000        493          DC    FREEWORD          RESERVED CODE       32304930
00ED   0E02 0F40        494  FORFAUL6 LINK  FORFAULT          FULLWORD ALIGNMENT FAULT 32304940
                        495  *                                 NOTE - ALL ALIGN FAULTS TREATED AS 32304950
                        496  *                                 FULLWORD ALIGN FAULTS BY PROCESSOR. 32304960


0000 00EE               498  ALIGN    EQU   *                 ENTERED VIA IV08    32304980
00EE   0E02 0FCD        499          LINK  MINUSLEN,RFAULT     GET (LOC-LENGTH), RESET ALIGN FAULT 32304990
00EF   0063 0060        500          L     MR3,ZMAR            MEMORY ADDRESS ON FAULT 32305000
00F0   0066 80C8        501          LI    MAR,'C8'            WILL READ FROM ALIGN NEW PSW 32305010
00F1   AE00 0EDD        502          B     FORFAUL6,PR2+RFAULT RESET ANY MAT FAULT QUEUED, 32305020
                        503  *                                 GO PICK UP FAULT CODE. 32305030

0000 00F2               505  SPECFAUL EQU   *                 EMULATED FAULTS ONLY, HERE 32305050
00F2   0060 00F0        506          L     MR0,LENGTH                            32305060
00F3   0014 0040        507          S     LOC,MR0,LOC         POINT TO FAULTED INSTRUCTION 32305070

0000 00F4               509  FORFAULT EQU   *                 COMMON ROUTINE      32305090
00F4   006E 00E0        510          L     SR,LR               SAVE LINK           32305100
00F5   0066 80C8        511          LI    MAR,'C8'            A(FAULT NEW PSW)    32305110
00F6   EE02 0C64        512          LINK  COMSWAP,PR4+I4      DO PSW SWAP         32305120
00F7   0028 E007        513          NI    YD,SR,'07'          R13 = FAULT CODE    32305130
00F8   001C C005        514          SI    NULL,YD,5           ALIGNMENT FAULT ?   32305140
00F9   0E44 0113        515          BF    C,TWAIT,IVJE+YDM1   BRANCH: NO. POINT R12. 32305150
                        516  *                                 IF CODE 6 OR 7,     32305160
00FA   0068 0030        517          L     YD,MR3              R12 = FAULT ADDRESS FROM ZMAR 32305170
00FB   0E04 0110        518          B     TWAIT,IVJE          GO TEST WAIT BIT    32305180

0000 00FC               520  MINUSLEN EQU   *                 SUBTRACTS LENGTH FROM LOC, INTERRUPT 32305200
00FC   506C 0050        521          L     NULL,MDR,ENACLK     CLOCK STOP FOR MAT FAULT SERVICE 32305210
00FD   006C 00B0        522          L     NULL,YSI            ENSURE XOP FOR RXRX UNLOADED 32305220
00FE   0060 00F0        523          L     MR0,LENGTH          GET INSTRUCTION LENGTH 32305230
00FF   0014 0040        524          S     LOC,MR0,LOC         DECREMENT LOC BY LENGTH 32305240
0100   0E01 00E0        525          RETN                      RETURN TO CALLER    32305250
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                        527  * ********************************************** 32305270
                        528  *                                                32305280
                        529  *       L O A D E R   S T O R A G E   U N I T    S U P P O R T  32305290
                        530  *                                                32305300
                        531  * ********************************************** 32305310

                        533  TLSU     EQU   *                  TEST LSU PRESENT, ENABLED      32305330
0000 0101               534           BT    HW,BOOT,ENACLK     BRANCH: ON-BOARD LSU ENABLED.  32305340
0101   5D08 1060        535           LI    YDI,5              LSU ADDRESS                    32305350
0102   006A 8005        536           ADRS  YDI                ADDRESS IT                     32305360
0103   006D 00A4        537           SS    FLR                TEST FOR FALSE SYNC            32305370
0104   006F 00C2        538           RETNT V                  RETURN IF V FLAG (NO LSU).     32305380
0105   0C21 00E0

                        540  * LSU REQUIRES THAT START AND END ADDRESSES OF LOAD MODULE      32305400
                        541  * REFLECT HALFWORD ALIGNMENT OF DATA.                          32305410

                        543  BOOT     EQU   *                  LSU HAS BEEN ADDRESSED.        32305430
0000 0106               544           LINK  RDHALF,RFAULT      READ PSW HALFWORD              32305440
0106   0E02 118D        545           LHL   MR2,MDR            NEW PSW                        32305450
0107   0062 0850        546           LINK  RDHALF             READ LOC HALFWORD              32305460
0108   0E02 1180        547           LHL   LOC,MDR            NEW LOC                        32305470
0109   0064 0850        548           LINK  RDHALF             READ LOAD START ADRS HALFWORD  32305480
010A   0E02 1180        549           LHL   MAR,MDR            START ADDRESS (MUST BE ALIGNED) 32305490
010B   0066 0850        550           LINK  RDHALF             READ LOAD END ADRS HALFWORD    32305500
010C   0E02 1180        551           LHL   MR0,MDR            END ADDRESS (MUST BE ODD)      32305510
010D   0060 0850        552           S     NULL,MR0,MAR       TEST (START LESS END)          32305520
010E   001C 0060        553           BT    G,COLD.5           BRANCH: ADDRESS ERROR. END < START. 32305530
010F   0C10 0770        554           LI    MR1,2              CONSTANT                       32305540
0110   0061 8002        555  *                                                                32305550
                        556  LOADLOOP LINK  RDHALF             GET HALFWORD OF LSU DATA       32305560
0111   0E02 1180        557           A     MAR,MR1,MAR,PW2    STORE; ADVANCE MAR BY 2        32305570
0112   2006 1060        558           S     NULL,MR0,MAR       DONE ?                         32305580
0113   001C 0060        559           BT    C,LOADLOOP         BRANCH: NOT DONE.              32305590
0114   0C40 1110        560           L     PSW,MR2,JAM        LOAD NEW PSW AND CC            32305600
0115   00E7 0020        561           BF    MPE,TMMF,RCATN     BRANCH: LOAD SUCCESSFUL.       32305610
0116   0E90 098B        562  *                                 TURN OFF FAULT LAMP.           32305620
                        563           B     COLD.5,RFAULT+ENACLK BRANCH: UNSUCCESSFUL BOOT.  32305630
0117   5E00 077D

                        565  * ROUTINE READS ONE HALFWORD FROM THE LSU                       32305650
                        566  RDHALF   RD    MDR                MS BYTE                      32305660
0118   0065 00C1        567           RETNT HW                 BRANCH: GOT A HALFWORD.      32305670
0119   0D09 00E0        568           EXB   SR,MDR             ELSE, SWAP BYTE TO B16:23    32305680
011A   006E 0450        569           RD    MDR                INPUT LS BYTE                32305690
011B   0065 00C1        570           O     MDR,SR,MDR         FORM A HALFWORD              32305700
011C   0035 6050        571           RETN                     AND RETURN.                  32305710
011D   0E01 00E0
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STATUS SWITCHING AND I/O SUPPORT

```
0000 011E                574  EPSR     EQU   *                ENTERED VIA DROM1              * 95 * 32305740
011E   0078 7000          575           L     YD,PSW           COPY PSW STATUS TO YD;                32305750
011F   08E7 0090          576           L     PSW,YS,JAM+D2    LOAD NEW PSW & CC,                    32305760
                         577  *                                VECTOR TO QTEST1.                     32305770

0000 0120                579  LPSWR    EQU   *                ENTERED VIA DROM1              * 18 * 32305790
0120   006C 00BF         580           L     NULL,YSI,LYSI    INCREMENT YSI BY 1                    32305800
0121   0864 0090         581           L     LOC,YS,D2        LOAD NEW LOC FROM USER R2+1,          32305810
                         582  *                                VECTOR TO QTEST.                      32305820

0000 0122                584  LPSW     EQU   *                ENTERED VIA DROM1              * C2 * 32305840
0122   F06C 0174         585           L     NULL,NULL,DR4+I4 FETCH NEW PSW STATUS                  32305850
0123   F06E 0050         586           L     SR,MDR,DR4       SR = NEW PSW; FETCH LOC               32305860
0124   0064 0050         587           L     LOC,MDR          WON'T LOAD IF FAULT -                 32305870
0125   DEB0 1260         588           BF    MAT+MPE,*+1,IR   TAKE INTERRUPT IF FAULT, ELSE         32305880

                         590  * ENTERED VIA DROM2 FROM EPSR, LPSWR                                   32305900
                         591  * OR BY BRANCH FROM LDPS (OPCODE DF4)                                  32305910
                         592  *                                                                      32305920
0126   00E7 00D0         593  QTEST    L     PSW,SR,JAM       LOAD NEW PSW & CC                     32305930
0127   002C F402         594  QTEST1   NI    NULL,PSW,'02',EXB IS QUEUE SERVICE INTPT ENABLED ?     32305940
0128   0E1C 0110         595           BF    G+L,TWAIT,IVJE   EXIT IF NO.                          32305950
0129   0066 8080         596           LI    MAR,'80'         A(SYSTEM QUEUE POINTER)               32305960
012A   E06C 0170         597           L     NULL,NULL,PR4    FETCH POINTER                         32305970
012B   0066 0050         598           L     MAR,MDR          AND READ SYSTEM QUEUE HEADER:         32305980
012C   E06E 0060         599           L     SR,MAR,PR4       SR = A(QUEUE), TRUNCATED AS REQ'D.    32305990
012D   0066 808C         600           LI    MAR,'8C'         A(SYSQ INTERRUPT NEW LOC)             32306000
012E   005C 0850         601           LHL   NULL,MDR         HAVE ANY ENTRIES BEEN USED ?          32306010
012F   5C90 0940         602           BT    MPE,MEMMF,ENACLK BRANCH: QUEUE TEST FAULTED.           32306020
0130   0E1C 0110         603           BF    G+L,TWAIT,IVJE   EXIT IF NO.                          32306030

                         605  * ********************************************                         32306050
                         606  *                                                                      32306060
                         607  *        SYSTEM QUEUE SERVICE INTERRUPT                                32306070
                         608  *                                                                      32306080
                         609  * ********************************************                         32306090

0131   E066 8088         611  SYSQINT  LI    MAR,'88',PR4     READ NEW LOC                          32306110
0132   0070 7001         612           L     MR0,PSW,CYD&SWA  PSW JUST LOADED                       32306120
0133   E063 0053         613           L     MR3,MDR,YDM1+PR4 MR3 = NEW LOC; FETCH NEW PSW          32306130

                         615  * THIS CODE SHARED BY SVC,EPSR,LPSWR,LPSW,LDPS                         32306150
                         616  *                                                                      32306160
0000 0134                617  CONSWAP2 EQU   *                ENTERED WITH YDI = 15                 32306170
0134   00E7 0050         618           L     PSW,MDR,JAM      SELECT NEW PSW                        32306180
0135   0068 0043         619           L     YD,LOC,YDM1      R15 = OLD LOC                         32306190
0136   0068 0003         620           L     YD,MR0,YDM1      R14 = OLD PSW                         32306200
0137   0068 00D0         621           L     YD,SR            R13 = SYSTEM QUEUE POINTER            32306210
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STATUS SWITCHING AND I/O SUPPORT

```
                        622  *                                    (OR SVC PARAM BLK ADDRESS)          32306220
                        623           L     LOC,MR3                NEW LOC                             32306230
0138  0064 0030        624           BF    MPE,TWAIT,IVJE         TEST WAIT BIT, UNLESS SWAP FAULTED. 32306240
0139  0E94 0110        625           B     MEMMF,ENACLK           FAULTED PSW FETCH                   32306250


                        627  * ********************************************                          32306270
                        628  *                                                                       32306280
                        629  *        SUPERVISOR CALL (SVC) INTERRUPT                                32306290
                        630  *                                                                       32306300
                        631  * ********************************************                          32306310

0000 013B               633  SVC      EQU   *                      ENTERED VIA DROM1          * E1 * 32306330
013B  006E 0060         634           L     SR,MAR                 SR = TRUNCATED ADDRESS              32306340
013C  0061 0AA1         635           SLL   MR1,YDI,CYD&SWA        MR1 = INDEX INTO SVC VECTOR TABLE   32306350
013D  0006 909C         636           AI    MAR,MR1,'9C'           READ VECTOR,                        32306360
013E  A066 8098         637           LI    MAR,'98',PR2           ADDRESS OF SVC NEW PSW              32306370
013F  0070 7003         638           L     MR0,PSW,YDM1           OLD PSW                             32306380
0140  E863 0850         639           LHL   MR3,MDR,PR4+D2         NEW LOC FROM SVC TABLE              32306390
                        640  *                                    VECTOR TO COMSWAP2 PSW SWAP.        32306400

                        642  * ********************************************                          32306420
                        643  *                                                                       32306430
                        644  *        SIMULATED IMMEDIATE INTERRUPT (SINT)                           32306440
                        645  *                                                                       32306450
                        646  * ********************************************                          32306460

0000 0141               648  SINT     EQU   *                      ENTERED VIA DROM1          * F2 * 32306480
0141  0020 E4FC         649           NI    MR0,SR,'FC',EXB        GET 10-BIT DEVICE ADDRESS           32306490
0142  004E 08D0         650           X     SR,MR0,SR,LHL          .                                   32306500
0143  0061 0AAC         651           SLL   MR1,YDI,DWSHFT         TIMES 2; TEST YDI FIELD.            32306510
0144  0E18 1490         652           BF    G+L,SINT.1             BRANCH: ASSUME LEVEL 0.             32306520
0145  006A 0A80         653           SLL   YDI,YD                 MAX LEVEL = 3; MOVE TO REG SEL FIELD 32306530
0146  006A 0AA0         654           SLL   YDI,YDI                .                                   32306540
0147  0061 0AA0         655           SLL   MR1,YDI                .                                   32306550
0148  0061 0A10         656           SLL   MR1,MR1                .                                   32306560
0149  0072 7001         657  SINT.1   L     MR2,PSW,CYD&SWA        SAVE CURRENT PSW                    32306570
014A  08B7 9428         658           OI    PSW,MR1,'28',EXB+JAM+D2 PSW = '000028N0'                   32306580
                        659  *                                    VECTOR TO IOINT1.                   32306590
```

STATUS SWITCHING AND I/O SUPPORT

```
                          661  * ********************************************** 32306610
                          662  *                                                32306620
                          663  *        I/O (IMMEDIATE) INTERRUPT               32306630
                          664  *                                                32306640
                          665  * ********************************************** 32306650

014B   0061 8020          667  LEVEL2   LI     MR1,'20'          I/O INTERRUPT, ATN2     32306670
014C   0E00 1500          668           B      IOINT                                    32306680

014D   0061 8010          670  LEVEL1   LI     MR1,'10'          I/O INTERRUPT, ATN1     32306700
014E   0E00 1500          671           B      IOINT                                    32306710

014F   0061 0170          673  LEVEL0   L      MR1,NULL          I/O INTERRUPT, ATN0     32306730

0150   0072 7001          675  IOINT    L      MR2,PSW,CYD&SWA   SAVE OLD PSW STATUS, POINT R0  32306750
0151   00B7 9428          676           DI     PSW,MR1,'28',EXB+JAM PSW = '000028N0'    32306760
0152   006E 0AC4          677           ACK    SR,SLL            MR0 = INTERRUPT DEVICE ADDRESS*2  32306770
0153   006D 0ED4          678  IOINT1   ADRS   SR,SRL            ADDRESS THE DEVICE      32306780
0154   0006 E0D0          679           AI     MAR,SR,'D0'       MAR = (2*DEV ADRS)+'D0'  32306790
0155   B068 0022          680           L      YD,MR2,YDP1+DR2   USER R0 GETS OLD PSW;   32306800
0156   0068 0042          681           L      YD,LOC,YDP1       .    R1 GETS CLD LOC    32306810
0157   0068 0ED2          682           SRL    YD,SR,YDP1        .    R2 GETS DEVICE ADDRESS  32306820
0158   0068 00C2          683           SS     YD                .    R3 GETS STATUS     32306830
0159   0068 0080          684           L      YD,YD             MAKE BOTH STACKS SAME   *R01 1/82*  32306840
015A   0064 0850          685           LHL    LOC,MDR           LOAD I.S.P. TABLE ENTRY;  32306850
015B   5C90 0940          686           BT     MPE,MEMMF,ENACLK  BRANCH: SWAP FAULTED.  32306860
015C   006C 0E50          687           SRL    NULL,MDR          IF ENTRY ODD,           32306870
015D   0C40 15F0          688           BT     C,CHANEL          ENTER AUTO-DRIVER CHANNEL;  32306880
015E   D0EF 0080          689           L      FLR,YD,IR+JAM     ELSE, CC GETS DEVICE STATUS; EXIT.  32306890
                          690  *                                 IF MPE BEFORE ENTERING CHANEL,  32306900
                          691  *                                 ERROR EXIT IS HERE.     32306910
```

AUTO DRIVER CHANNEL

```
                        693  * ********************************************** 32306930
                        694  *                                                32306940
                        695  *        AUTO-DRIVER CHANNEL SUPPORT             32306950
                        696  *                                                32306960
                        697  * ********************************************** 32306970

                        699  EBIT     EQU   '80'              EXECUTE BIT                              32306990
0000 0080               700  SBIT     EQU   '20'              CRC CHECK TYPE: 0=CRC16; 1 = SDLC        32307000
0000 0020               701  CBIT     EQU   '10'              CHECK TYPE: 0 = LRC; 1 = CRC             32307010
0000 0010               702  BBIT     EQU   '08'              BUFFER SWITCH BIT                        32307020
0000 0008               703  RWBIT    EQU   '04'              READ/WRITE (0/1)                         32307030
0000 0004               704  TBIT     EQU   '02'              TRANSLATE = 1                            32307040
0000 0002               705  FBIT     EQU   '01'              FAST MODE = 1                            32307050
0000 0001

                        707  CHANEL   LHL   MAR,LOC,YDP1       FETCH CHANNEL COMMAND WORD               32307070
015F  0066 0842         708           L     YD,LOC,PR4        R4 = A(CCB), FORCED EVEN                 32307080
0160  E068 0040         709           L     NULL,YDI,LYSI     SELECT R4 AS YS                          32307090
0161  006C 00AF         710           EXH   MR2,MDR,I4        MR2 = CCW = CHANNEL COMMAND WORD         32307100
0162  0062 0C54         711           NI    NULL,MR2,EBIT,JAM TEST EXECUTE BIT:                        32307110
0163  00AC A080         712           BF    G+L,EXSUB0,YDM1   BRANCH: NO EXECUTE, ABORT.              32307120
0164  0E18 1833         713  *                                                                         32307130
0165  00AC 4420         714           N     NULL,YD,MR2,EXB+JAM TEST STATUS (R3) AGAINST MASK:         32307140
                        715  *                                (ASSUMES 8-BIT STATUS RETURNED)          32307150
0166  0C18 1852         716           BT    G+L,EXSUB1,YDP1   BRANCH; BAD STATUS ABORT. POINT R4.     32307160
                        717  *                                                                         32307170
0167  002C A001         718           NI    NULL,MR2,FBIT     TEST FAST MODE BIT:                      32307180
0168  0E18 1880         719           BF    G+L,NORMAL        BRANCH: NOT FAST MODE                    32307190

0169  E061 0550         721  FASTMODE EXT   MR1,MDR,PR4       MR1 = BUF0 BYTE COUNT                    32307210
                        722  *                                FETCH BUF0 END ADDRESS.                  32307220
016A  0C10 17E1         723           BT    G,EXAUTO,CYD&SWA  BRANCH: EXIT ON POSITIVE COUNT          32307230
                        724  *                                                                         32307240
                        725  *        NOTE: HALFWORD DATA MUST BE ALIGNED !                            32307250
016B  0006 1050         726           A     MAR,MR1,MDR       ADDRESS DATA BYTE/HALFWORD               32307260
016C  002C A004         727           NI    NULL,MR2,RWBIT    TEST R/W BIT:                            32307270
016D  0C18 1752         728           BT    G+L,OUTPUT,YDP1   BRANCH: R/W=1=WRITE; INCREMENT IS 1.    32307280
016E  0D08 1710         729           BT    HW,HWINP          BRANCH: HALFWORD DEVICE.                 32307290
016F  0065 04C1         730           RD    MDR,EXB           INPUT DATA, WRITE TO MEMORY.             32307300
0170  1E00 1770         731           B     COMMON,DW1                                                 32307310
                        732  *                                                                         32307320
0171  0065 00C1         733  HWINP    RD    MDR               INPUT HALFWORD                           32307330
0172  2E00 1772         734           B     COMMON,PW2+YDP1   WRITE TO MEMORY; INCREMENT IS 2.         32307340
                        735  *                                                                         32307350
0173  006D 0051         736  HWOUTP   WD    MDR               OUTPUT HALFWORD                          32307360
0174  0E00 1772         737           B     COMMON,YDP1       INCREMENT IS 2.                          32307370
                        738  *                                                                         32307380
0175  AD08 1730         739  OUTPUT   BT    HW,HWOUTP,PR2     BRANCH: HALFWORD DEVICE.                 32307390
0176  006D 0451         740           WD    MDR,EXB           OUTPUT DATA                              32307400
```

AUTO DRIVER CHANNEL

```
0177  0006 D002   742  COMMON   AI    MAR,YS,2              ADDRESS BUFFER 0 BYTE COUNT                32307420
0178  0005 10A1   743           A     MDR,MR1,YDI,CYD&SWA   INCREMENT COUNT (MR1) BY 1 OR 2             32307430
0179  2E10 17F2   744           BF    G,EXAUTO2,PW2+YDP1    BRANCH: NORMAL EXIT. POINT R1.             32307440

                  746  * EXIT TO SUBROUTINE AT BUFFER END (BYTE COUNT POSITIVE):                        32307460
                  747  *                                                                                32307470
017A  0006 D014   748  EXSUB2   AI    MAR,YS,20             FETCH SUBROUTINE ADDRESS                   32307480
017B  A0EF 8002   749           LI    FLR,'02',JAM+PR2      CC = 2                                     32307490

017C  0064 0850   751  EXSUB    LHL   LOC,MDR               SUBROUTINE ADDRESS                         32307510
017D  DC90 1820   752           BT    MPE,EXAUTMMF,IR       BRANCH: FAULT IN CHANNEL. ELSE, EXIT.      32307520

                  754  * NORMAL EXIT FROM AUTO-DRIVER CHANNEL                                           32307540
                  755  *                                                                                32307550
017E  006C 0052   756  EXAUTO   L     NULL,MDR,YDP1         MEMORY WAS READING ? POINT R1.             32307560
017F  0064 0083   757  EXAUTO2  L     LOC,YD,YDM1           RESTORE ENTRY LOC, POINT R0.               32307570
0180  00E7 0080   758           L     PSW,YD,JAM            RESTORE ENTRY PSW                          32307580
0181  0E90 0110   759           BF    MPE,TWAIT             TEST WAIT (NO IVJE ALLOWED)                32307590
0182  5E00 08E0   760  EXAUTMMF B     CHANMMF,ENACLK        BRANCH: FAULT IN CHANNEL                   32307600

                  762  * UNCONDITIONAL EXIT TO SUBROUTINE (EXECUTE BIT = 0)                             32307620
                  763  *                                                                                32307630
0183  0006 D014   764  EXSUB0   AI    MAR,YS,20             FETCH SUBROUTINE ADDRESS                   32307640
0184  AE00 17C0   765           B     EXSUB,PR2             AND GO EXIT.                               32307650

                  767  * EXIT TO SUBROUTINE ON STATUS ERROR:                                            32307670
                  768  *                                                                                32307680
0185  0006 D014   769  EXSUB1   AI    MAR,YS,20             FETCH SUBROUTINE ADDRESS                   32307690
0186  A0EF 8001   770           LI    FLR,'01',JAM+PR2      CC = 1                                     32307700
0187  0E00 17C0   771           B     EXSUB                                                            32307710
```

AUTO DRIVER CHANNEL

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                                773  * MR1 = BUFFER BYTE COUNT          MR2 = COPY OF COMMAND WORD          32307730
                                774  * MR0 = WORK REGISTER              MR3 = BYTE/TRANSLATED BYTE          32307740
                                775  * R4 = ADDRESS OF COMMAND BLOCK    LOC = ADDRESS OF BYTE COUNT         32307750
                                776  * S3 = BYTE ADDRESS                                                   32307760
                                777  *                                                                     32307770
                                778  NORMAL   NI    MR1,MR2,BBIT       GET 0 OR 8                          32307780
0188  0021 A008                 779           A     MAR,YS,MR1         ADDRESS BYTE COUNT @ +2 OR +10      32307790
0189  0006 5010                 780           L     LOC,MAR,PR4+I4     LOC = A(BUFFER BYTE COUNT) - 2      32307800
018A  E064 0064                 781           EXT   MR1,MDR,PR4        MR1 = BUFFER BYTE COUNT             32307810
018B  E061 0550                 782  *                                 FETCH BUFFER END ADRS.              32307820
                                783           BT    G,EXAUTO,CYD&SWA   BRANCH: BYTE COUNT POSITIVE.        32307830
018C  0C10 17E1                 784           A     MAR,MR1,MDR        ADDRESS CURRENT BYTE .              32307840
018D  0006 1050                 785  *                                                                     32307850
                                786  * NOTE: IN NON-FAST MODE, ONLY BYTE TRANSFERS ARE ALLOWED.           32307860
                                787  *                                                                     32307870
                                788           NI    NULL,MR2,RWBIT     TEST R/W BIT:                       32307880
018E  002C A004                 789           BT    G+L,NFWRIT         BRANCH: R/W = 1 = WRITE.            32307890
018F  0C18 1970                 790  NFREAD   RD    MR3                MR3 = DATA BYTE INPUT (RAW)         32307900
0190  0063 00C1                 791           NI    MR0,MR3,'FF'       KEEP A COPY                         32307910
0191  0020 B0FF                 792           NI    NULL,MR2,TBIT      TRANSLATION REQ'D ?                 32307920
0192  002C A002                 793           LINKT G+L,RTRANSL        BRANCH: YES.                        32307930
0193  0C1A 1BA0                 794           EXB   MDR,MR3            WRITE BYTE TO MEMORY                32307940
0194  0065 0430                 795           L     MR3,MR0,DW1        TRANSFERRED BYTE IN MR3; WRITE IT.  32307950
0195  1063 0000                 796           B     REDCHK             DO CHKSUM.                          32307960
0196  0E00 19C0

                                798  NFWRIT   LI    MR3,'FF',PR2        MASK; FETCH DATA.                   32307980
0197  A063 80FF                 799           N     MR3,MR3,MDR,EXB    MR3 = DATA BYTE TO OUTPUT (RAW)     32307990
0198  0023 3450                 800           NI    NULL,MR2,TBIT      TRANSLATION REQ'D ?                 32308000
0199  002C A002                 801           LINKT G+L,TRANSL         IF YES, DO IT.                      32308010
019A  0C1A 1BB0                 802           WD    MR3                OUTPUT DATA BYTE                    32308020
019B  006D 0031

                                804  * THE ACTUAL BYTE TRANSFERRED IS FIGURED IN THE CHECKSUM.           32308040
                                805  *                                                                     32308050
019C  0006 D008                 806  REDCHK   AI    MAR,YS,8           ADDRESS CHECKWORD                   32308060
019D  A020 A030                 807           NI    MR0,MR2,CBIT+SBIT,PR2 CRC REQUIRED ?                  32308070
019E  0C18 1AB0                 808           BT    G+L,CRCCK          BRANCH: YES.                        32308080
                                809  *                                                                     32308090
019F  0023 B0FF                 810  LRCCK    NI    MR3,MR3,'FF'       FORCE TO 8-BIT DATA BYTE            32308100
01A0  0045 3050                 811           X     MDR,MR3,MDR        EXCLUSIVE-OR CHECKSUM               32308110
01A1  0E00 1B30                 812           B     COMMON2            GO UPDATE CHECKWORD, BYTE COUNT     32308120

                                814  CRCKA    LI    MR0,'A0',EXB                                           32308140
01A2  0060 84A0                 815           OI    SR,MR0,1           (SR) = 'A001'                       32308150
01A3  003E 8001                 816           NI    MR3,MR3,'FF'       FORCE DATA TO 8-BITS                32308160
01A4  0023 B0FF                 817           X     MDR,MR3,MDR,LHL+CYD&SWA XOR-IN RESIDUAL                32308170
01A5  0045 3851                 818  CRCKB    SRL   MDR,MDR            SHIFT                               32308180
01A6  0065 0E50                 819           BF    C,CRCKC,YDP1       8 PASSES                            32308190
01A7  0E40 1A92                 820           X     MDR,SR,MDR         XOR-IN FEEDBACK ON CARRY            32308200
01A8  0045 5050                 821  CRCKC    BF    YDC,CRCKB,YDP1     BRANCH: CONTINUE UNTIL YDCARRY      32308210
01A9  0F88 1A62                 822           B     COMMON2            GO UPDATE CHECKWORD, BYTE COUNT.    32308220
01AA  0E00 1B30
```

AUTO DRIVER CHANNEL

```
01AB  0FC0 1A20          824  CRCCK    BF    COMM,CRCKA          BRANCH: NO COMM ASSIST                32308240
01AC  0020 8020          825           NI    MR0,MR0,SBIT        SDLC REQ'D ?                          32308250
01AD  0E18 1AF0          826           BF    G+L,CRCK1           BRANCH: CRC16                         32308260
01AE  0060 9001          827           LI    MR0,1               SDLC CODE                             32308270
01AF  006C 0008          828  CRCK1    L     NULL,MR0,COMM       CODE TO COMM ASSIST UNIT              32308280
01B0  006C 0058          829           L     NULL,MDR,COMM       OLD RESIDUAL                          32308290
01B1  006C 0038          830           L     NULL,MR3,COMM       NEW DATA                              32308300
01B2  0055 00CC          831           ACK0  MDR                 NEW RESIDUAL                          32308310

01B3  2060 0041          833  COMMON2  L     MR0,LOC,CYD&SWA+PW2 A(BUFFER BYTE COUNT) - 2;             32308330
                         834  *                                 UPDATE CHECKWORD, POINT R0.           32308340
01B4  0006 8002          835           AI    MAR,MR0,2           MAR = A(BYTE COUNT)                   32308350
01B5  0005 9001          836           AI    MDR,MR1,1           INCREMENT BYTE COUNT                  32308360
01B6  2E10 17F2          837           BF    G,EXAUTO2,PW2+YDP1  BRANCH: NOT YET POSITIVE; POINT R1    32308370

                         839  * POSITIVE BYTE COUNT                                                    32308390
                         840  *                                                                        32308400
01B7  0045 A008          841  BUFSW    XI    MDR,MR2,BBIT        COMPLEMENT BUFFER BIT                 32308410
01B8  0066 0090          842           L     MAR,YS              RESTORE CCW                           32308420
01B9  2E00 17A0          843           B     EXSUB2,PW2          EXIT TO SUBROUTINE WITH CC = 2        32308430

                         845  * TRANSLATE THE BYTE                                                     32308450
                         846  *                                                                        32308460
01BA  005E 0060          847  RTRANSL  L     SR,MAR              ADDRESS OF CURRENT BYTE               32308470
01BB  0006 D010          848  TRANSL   AI    MAR,YS,16           POINT TO TRANSLATION TABLE ADRS       32308480
01BC  E063 0A31          849           SLL   MR3,MR3,PR4+CYD&SWA FETCH ADDRESS, DOUBLE DATA BYTE      32308490
01BD  0023 BAFF          850           NI    MR3,MR3,'FF',SLL    LIMIT 8-BIT BYTE                      32308500
01BE  0005 3052          851           A     MAR,MR3,MDR,YDP1    ADD INDEX TO BASE                     32308510
01BF  A060 0E32          852           SRL   MR0,MR3,PR2+YDP1    MR0 = 8-BIT BYTE; FETCH ENTRY.        32308520
01C0  0066 00D0          853           L     MAR,SR              RE-ADDRESS CURRENT BYTE               32308530
01C1  0063 0552          854           EXT   MR3,MDR,YDP1        IS ENTRY NEGATIVE ?                   32308540
01C2  0C09 00E0          855           RETNT L                   IF YES, RETURN WITH BYTE IN MR3.      32308550
01C3  0064 0A30          856           SLL   LOC,MR3             LOAD NEW LOC,                         32308560
01C4  0068 0000          857           L     YD,MR0              R3 GETS UNTRANSLATED CHARACTER        32308570
01C5  DC90 1820          858           BT    MPE,EXAUTMMF,IR     BRANCH: FAULT IN CHANNEL  ELSE EXIT   32308580
                         859  *                                 WITH CC = 0.                          32308590
```

INPUT/OUTPUT INSTRUCTIONS

```
01C6   B05C 0170          861  RXIO    L      NULL,NULL,DR2     READ ADDRESSED BYTE OR HALFWORD        32308610
01C7   086D 0084          862  RRIO    ADRS   YD,.D2            ADDRESS THE DEVICE,                    32308620
                          863  *                                VECTOR VIA DROM2.                      32308630

0000 01C8                 865  OC      EQU    *                 ENTERED VIA DROM2 (RXIO)      * DE -   32308650
01C8   006E 0450          866         EXB    SR,.MDR           GET COMMAND BYTE.                      32308660
0000 01C9                 867  OCR     EQU    *                 ENTERED VIA DROM2  (RRIO)     * 9E -   32308670
01C9   00ED 00D2          868         OC     SR,.JAM           COMMAND TO ADDRESSED DEVICE            32308680
01CA   006B 8003          869  AL.300  LI     CNTR,3            (COMMON EXIT FOR AL WITH SELCH)        32308690
01CB   005C 0170          870         L      NULL,NULL                                                32308700
01CC   D06C 0170          871         L      NULL,NULL,IR      DELAY FOR 1 USEC.                      32308710

0000 01CD                 873  SS      EQU    *                 ENTERED VIA DROM2 (RRIO)      * DD -   32308730
01CD   0065 04C2          874         SS     MDR,EXB           SENSE STATUS                           32308740
01CE   10EF 0450          875         EXB    FLR,MDR,DW1+JAM   STORE IT, UPDATE CC                   32308750
01CF   D06C 0170          876         L      NULL,NULL,IR      EXIT.                                  32308760

0000 01D0                 878  SSR     EQU    *                 ENTERED VIA DROM2 (RRIO)      * 9D -   32308780
01D0   0069 00C2          879         SS     YS                SENSE DEVICE STATUS                    32308790
01D1   0069 0090          880         L      YS,YS             MAKE BOTH STACKS SAME   *R01 1/82*     32308800
01D2   D0EF 0090          881         L      FLR,YS,IR+JAM     SET CC, EXIT.                          32308810

0000 01D3                 883  RH      EQU    *                 ENTERED VIA DROM2 (RRIO)      * D9 -   32308830
01D3   00E5 00C1          884         RD     MDR,JAM           INPUT DATA, SET CC                     32308840
01D4   3D08 0130          885         BT     HW,EXIT,DW2       BRANCH: HALFORD DEVICE.                32308850
01D5   0060 0050          886         L      MR0,MDR           DATA, FORM 000000XX                    32308860
01D6   00E5 00C1          887         RD     MDR,JAM           DATA, FORM 000000YY                    32308870
01D7   0065 0400          888         EXB    MDR,MR0           COMBINE, FORM 0000XXYY                 32308880
01D8   3E00 0130          889         B      EXIT,DW2          STORE; GO EXIT.                        32308890

0000 01D9                 891  RHR     EQU    *                 ENTERED VIA DROM2 (RRIO)      * 99 -   32308910
01D9   00E9 00C1          892         RD     YS,.JAM           INPUT DATA, SET CC                     32308920
01DA   DF08 1DB0          893         BF     HW,.RHBR,IR       BRANCH: BYTE-ORIENTED DEVICE           32308930
01DB   0060 00C1          894  RHBR    RD     MR0               INPUT LS DATA BYTE                     32308940
01DC   D039 0490          895         O      YS,.MR0,YS,EXB+IR APPEND LOW BYTE, EXIT.                 32308950

0000 01DD                 897  WH      EQU    *                 ENTERED VIA DROM2 (RRIO)      * D8 -   32308970
01DD   BD08 1DF0          898         BT     HW,WHH,DR2        BRANCH IF HALFWORD-ORIENTED DEVICE     32308980
01DE   006D 0451          899  WHB     WD     MDR,.EXB          BYTE DEVICE: OUTPUT HIGH BYTE          32308990
01DF   00ED 0051          900  WHH     WD     MDR,.JAM          OUTPUT LOW BYTE (OR THE HALFWORD)      32309000
01E0   D06C 0170          901         L      NULL,NULL,IR      EXIT.                                  32309010

0000 01E1                 903  WHR     EQU    *                 ENTERED VIA DROM2 (RRIO)      * 98 -   32309030
01E1   0D08 1E30          904         BT     HW,.WHRH          BRANCH: HALFWORD-ORIENTED DEVICE.      32309040
01E2   006D 0491          905  WHRB    WD     YS,.EXB           HIGH BYTE                              32309050

0000 01E3                 907  WDR     EQU    *                 ENTERED VIA DROM2 (RRIO)      * 9A -   32309070
01E3   00ED 0091          908  WHRH    WD     YS,.JAM           OUTPUT DATA, EXIT.                     32309080
```

INPUT/OUTPUT INSTRUCTIONS

```
01E4   D06C 0170          909          L     NULL,NULL,IR                                                  32309090


0000 01E5                 911  RD      EQU   *                ENTERED VIA DROM2 (RRIO)      * DB *  32309110
01E5   00E5 04C1          912          RD    MDR,EXB+JAM      INPUT DATA BYTE, SET CC, STORE DATA  32309120
01E6   1E00 0130          913          B     EXIT,DW1         WRITE TO MEMORY, GO EXIT.            32309130


0000 01E7                 915  RDR     EQU   *                ENTERED VIA DROM2  (RRIO)     * 9B *  32309150
01E7   00E9 00C1          916          RD    YS,JAM           YD = INPUT DATA BYTE; EXIT.          32309160
01E8   D06C 0170          917          L     NULL,NULL,IR                                          32309170


0000 01E9                 919  WD      EQU   *                ENTERED VIA DROM2  (RXIO)     * DA *  32309190
01E9   00ED 0451          920          WD    MDR,EXB+JAM      OUTPUT DATA BYTE, SET CC, EXIT.      32309200
01EA   D06C 0170          921          L     NULL,NULL,IR                                          32309210


0000 01EB                 923  AL      EQU   *                ENTERED VIA DROM1             * D5 *  32309230
01EB   006E 0060          924          L     SR,MAR           RX FINAL ADDRESS CALCULATED          32309240
01EC   0063 8080          925          LI    MR3,'80'         STANDARD AUTOLOAD START              32309250
01ED   006C 00AF          926          L     NULL,YDI,LYSI    YDI <> 0 ?                           32309260
01EE   0E18 1F12          927          BF    G+L,AL.001,YDP1  BRANCH: USE STANDARD START, RX END.  32309270
01EF   006E 0080          928          L     SR,YD            END ADDRESS FROM R1+1                32309280
01F0   0063 0090          929          L     MR3,YS           START ADDRESS FROM R1                32309290
01F1   001C 30D0          930  AL.001  S     NULL,MR3,SR      TEST END LESS START:                 32309300
01F2   0C40 2250          931          BT    C,SETCC0         BRANCH: ABORT INSTRUCTION.           32309310
                          932  *                                                                    32309320
01F3   0066 8078          933          LI    MAR,'78'         CONTROLLER ADDRESS SPECIFIED HERE -  32309330
01F4   A060 80FF          934          LI    MR0,'FF',PR2     FETCH.                               32309340
01F5   0066 807C          935          LI    MAR,'7C'         FETCH CTRLR ADRS:CMD                 32309350
01F6   A062 0850          936          LHL   MR2,MDR,PR2      MR2 = CTRLR ADRS:CMD                 32309360
01F7   0021 0050          937          N     MR1,MR0,MDR      SELCH ADRS ZERO ?                    32309370
01F8   0C18 20C0          938          BT    G+L,AL.100       BRANCH: ADDRESS NOT ZERO, WILL USE.  32309380
                          939  *                                                                    32309390
                          940  * SELCH NOT TO BE USED                                              32309400
                          941  *                                                                    32309410
01F9   0066 0030          942          L     MAR,MR3          START ADDRESS; (SR) = END ADDRESS.   32309420
01FA   0021 0420          943          N     MR1,MR0,MR2,EXB  MR1 = CONTROLLER ADDRESS             32309430
01FB   006D 0014          944          ADRS  MR1              ADDRESS THE DEVICE CONTROLLER        32309440
01FC   0063 8001          945          LI    MR3,1            CONSTANT                             32309450
01FD   006D 0022          946          OC    MR2              SEND COMMAND                         32309460


                          948  * SENSE DEVICE STATUS; BYPASS LEADER BYTES.                          32309480
                          949  *                                                                    32309490
01FE   00EF 00C2          950  AL.010  SS    FLR,JAM          SENSE DEVICE STATUS - ADJUST CC.     32309500
01FF   0E78 2010          951          BF    C+V+G+L,AL.015   BRANCH: DATA READY.                  32309510
0200   DE38 1FE0          952          BF    V+G+L,AL.010,IR  EXIT IF BAD STATUS                   32309520
0201   0062 00C1          953  AL.015  RD    MR2              INPUT DATA BYTE                      32309530
0202   0065 0420          954          EXB   MDR,MR2          POSITION BYTE - IS IT NON-ZERO ?     32309540
0203   0C18 2090          955          BT    G+L,AL.030       BRANCH: STORE FIRST NON-ZERO BYTE.   32309550
0204   0E00 1FE0          956          B     AL.010           LOOP FOR NEXT.                       32309560
                          957  *                                                                    32309570
```

INPUT/OUTPUT INSTRUCTIONS

```
0205   00EF 00C2          958  AL.020   SS    FLR,JAM              SENSE DEVICE STATUS, ADJUST CC        32309580
0206   0E78 2080          959           BF    C+V+G+L,AL.025       BRANCH: DATA READY.                   32309590
0207   DE38 2050          960           BF    V+G+L,AL.020,IR      EXIT ON BAD STATUS.                   32309600
0208   0065 04C1          961  AL.025   RD    MDR,EXB              MDR = DATA BYTE.                      32309610
0209   1006 3050          962  AL.030   A     MAR,MR3,MAR,DW1      STORE; READY FOR NEXT BYTE            32309620
020A   001C 6060          963           S     NULL,SR,MAR          A(NEXT BYTE) > END ?                  32309630
020B   DE10 2050          964           BF    G,AL.020,IR          BRANCH: NOT DONE; ELSE, EXIT CC = 0.  32309640

                          966  * SELECTOR CHANNEL TO BE USED FOR AUTOLOAD                                 32309660
                          967  * THE SELCH AND CONTROLLER MUST BE READY FOR THE TRANSFER                   32309670
                          968  * THE SELCH IS ASSUMED TO BE A BYTE DEVICE ON MUX BUS                       32309680
                          969  * INTERRUPTS MAY BE QUEUED.                                                 32309690
                          970  *                                                                           32309700
0000 020C                 971  AL.100   EQU   *                                                           32309710
020C   0060 0020          972           L     MR0,MR2              MR0 = DEV ADRS:CMD                    32309720
020D   0062 0010          973           L     MR2,MR1              MR2 = SELCH ADDRESS                   32309730
020E   006D 0024          974           ADRS  MR2                  ADDRESS THE SELCH                     32309740
020F   0061 8008          975           LI    MR1,'08'             SELCH 'STOP' COMMAND                  32309750
0210   006D 0012          976           OC    MR1                  STOP THE SELCH                        32309760
0211   006D 0C31          977           WD    MR3,EXH              BYTE 0, START ADDRESSS                32309770
0212   006D 0431          978           WD    MR3,EXB              BYTE 1                                32309780
0213   006D 0031          979           WD    MR3                  BYTE 2                                32309790
0214   006D 0CD1          980           WD    SR,EXH               BYTE 0, END ADDRESSS                  32309800
0215   006D 04D1          981           WD    SR,EXB               BYTE 1                                32309810
0216   006D 00D1          982           WD    SR                   BYTE 2                                32309820
0217   0021 84FF          983           NI    MR1,MR0,'FF',EXB     DEVICE ADDRESS (WAS IN '78')          32309830
0218   006D 0414          984           ADRS  MR1,EXB              ADDRESS THE DEVICE                    32309840
0219   006D 0002          985           OC    MR0                  SEND DEVICE COMMAND (WAS IN '79')     32309850
021A   006D 0024          986           ADRS  MR2                  ADDRESS THE SELCH                     32309860
021B   0061 8030          987           LI    MR1,'30'             SELCH 'GO/READ' COMMAND               32309870
021C   006D 0012          988           OC    MR1                  START SELCH                           32309880
021D   00EF 00C2          989  AL.110   SS    FLR,JAM              SENSE SELCH STATUS                    32309890
021E   0C38 2210          990           BT    V+G+L,AL.120         BRANCH: BAD DEVICE STATUS.            32309900
021F   0CC0 4000          991           BT    PPF,BRK              BRANCH: LOSING POWER;                 32309910
                          992  *                                  DECREMENT LOC BEFORE PWRDWN.          32309920
0220   0C40 21DC          993           BT    C,AL.110             BRANCH: SELCH STILL BUSY              32309930
0221   006D 0024          994  AL.120   ADRS  MR2                  ADDRESS SELCH (SET MSC1)              32309940
0222   006E 8008          995           LI    SR,'08'              SELCH 'STOP' CMD                      32309950
0223   006D 00D2          996           OC    SR                   STOP SELCH                            32309960
0224   0E90 1CA0          997           B     AL.300               DELAY, EXIT.                          32309970
```

GLOBAL PRE- AND POST-PROCESSING - MISCELLANEOUS

```
0225  D0EF 0170          1000  SETCC0   L     FLR,NULL,IR+JAM     SET CC = 0, EXIT.                          32310000

0226  D0EF 8001          1002  SETCC1   LI    FLR,1,IR+JAM        SET CC = 1, EXIT.                          32310020

0227  D0EF 8002          1004  SETCC2   LI    FLR,2,IR+JAM        SET CC = 2, EXIT.                          32310040

0228  006C 0050          1006  SETCC4A  L     NULL,MDR            MEMORY WAS READING                         32310060
0229  D0EF 8004          1007  SETCC4   LI    FLR,4,IR+JAM        SET CC = 4, EXIT.                          32310070

022A  006C 0050          1009  SETCC8A  L     NULL,MDR            MEMORY WAS READING                         32310090
022B  D0EF 8008          1010  SETCC8   LI    FLR,8,IR+JAM        SET CC = 8, EXIT.                          32310100

022C  D0BF F001          1012  ADDCC1   OI    FLR,PSW,1,IR+JAM    TURN ON L FLAG, EXIT.                      32310120

022D  D0BF F004          1014  ADDCC4   OI    FLR,PSW,4,IR+JAM    TURN ON V FLAG, EXIT.                      32310140

                         1016  * RX BYTE OPERATION SETUP - ENTERED VIA DROM1.                                 32310160
022E  B86E 80FF          1017  RXBYTE   LI    SR,'FF',DR2+D2      READ HALFWORD                              32310170
                         1018  *                                  VECTOR VIA DROM2                           32310180

                         1020  * RX HALFWORD OPERATION SETUP - ENTERED VIA DROM1.                             32310200
022F  B820 C0FF          1021  RXH      NI    MRO,YD,'FF',DR2+D2  READ HALFWORD                              32310210
                         1022  *                                  VECTOR VIA DPOM2                           32310220

0230  B020 C0FF          1024  RXH2     NI    MRO,YD,'FF',DR2     READ HALFWORD                              32310240
0231  086E 0550          1025  RXH1     EXT   SR,MDR,D2           EXTEND SIGN IN SR, VECTOR VIA DROM2        32310250

                         1027  * RX FULLWORD OPERATION SETUP - ENTERED VIA DROM1.                             32310270
0232  F820 C0FF          1028  RXF      NI    MRO,YD,'FF',DR4+D2  READ FULLWORD                              32310280
                         1029  *                                  VECTOR VIA DROM2                           32310290

0233  F020 C0FF          1031  RXF2     NI    MRO,YD,'FF',DR4     READ FULLWORD                              32310310
0234  086E 0050          1032  RXF1     L     SR,MDR,D2           COPY TO SR, VECTOR VIA DROM2               32310320

                         1034  * RX STORE INSTRUCTION TERMINATION - ENTERED VIA DROM2 OR BRANCH               32310340
0235  1E00 0130          1035  STB.D2   B     EXIT,DW1            STORE BYTE, EXIT.                          32310350

0236  3E00 0130          1037  STH.D2   B     EXIT,DW2            STORE HALFWORD, EXIT                       32310370

0237  7E00 0130          1039  STF.D2   B     EXIT,DW4            STORE FULLWORD, EXIT                       32310390
```

LIST INSTRUCTIONS

```
0000 0238                1041  ATL       EQU   *                 ENTERED VIA DROM1                  * 64 * 32310410
0238   F063 0174         1042            L     MR3,NULL,DR4+I4   CONSTANT; FETCH (SIZE:USED)              32310420
0239   B050 0054         1043            L     MR0,MDR,DR2+I4    GOT IT; FETCH CURR TOP                   32310430
023A   001C 0C00         1044            S     NULL,MR0,MR0,EXH  (USED:SIZE) - (SIZE:USED)               32310440
023B   0E40 2280         1045            BF    C,SETCC4A         BRANCH: NO ROOM AT THE INN.              32310450
023C   0060 0C00         1046            EXH   MR0,MR0           MR0 = USED:SIZE                          32310460
023D   0012 3855         1047            SDEC  MR2,MR3,MDR,LHL   GET (CURR TOP) - 1                       32310470
023E   0E40 2400         1048            BF    C,ATL.010         BRANCH: NO LIST WRAP                     32310480
023F   0012 3805         1049            SDEC  MR2,MR3,MR0,LHL   WRAP: SET CURR TOP = (SIZE-1)            32310490
0240   0065 0080         1050  ATL.010   L     MDR,YD            DATA TO STORE IN LIST                    32310500
0241   0061 0A20         1051            SLL   MR1,MR2           COMPUTE A(SLOT)                          32310510
0242   0061 0A10         1052            SLL   MR1,MR1           .                                        32310520
0243   0006 1060         1053            A     MAR,MR1,MAR       .                                        32310530
0244   7066 00D0         1054            L     MAR,SR,DW4        STORE; POINT TO NUMBER USED              32310540
0245   0005 3C05         1055            AINC  MDR,MR3,MR0,EXH   INCREMENT NUMBER USED                    32310550
0246   7065 0024         1056            L     MDR,MR2,DW4+I4    STORE; MDR = NEW CURR TOP                32310560
0247   3E00 2250         1057            B     SETCC0,DW2        STORE; GO SET CC=0, EXIT.                32310570


0000 0248                1059  ABL       EQU   *                 ENTERED VIA DROM1                  * 65 * 32310590
0248   F063 0174         1060            L     MR3,NULL,DR4+I4   CONSTANT; FETCH (SIZE:USED)              32310600
0249   F060 0054         1061            L     MR0,MDR,DR4+I4    FETCH (CURR TCP:NEXT BOTT)               32310610
024A   001C 0C00         1062            S     NULL,MR0,MR0,EXH  (USED:SIZE) - (SIZE:USED)               32310620
024B   0E40 2280         1063            BF    C,SETCC4A         BRANCH: NO ROOM AT THE INN.              32310630
024C   0062 0850         1064            LHL   MR2,MDR           MR2 = NEXT BOTT                          32310640
024D   0065 0080         1065            L     MDR,YD            DATA TO STORE                            32310650
024E   0061 0A20         1066            SLL   MR1,MR2           COMPUTE A(SLOT)                          32310660
024F   0061 0A10         1067            SLL   MR1,MR1           .                                        32310670
0250   0006 1060         1068            A     MAR,MR1,MAR       .                                        32310680
0251   7006 E002         1069            AI    MAR,SR,2,DW4      STORE; POINT (NUMBER USED)               32310690
0252   0005 3005         1070            AINC  MDR,MR3,MR0       INCREMENT NUMBER USED                    32310700
0253   3005 3025         1071            AINC  MDR,MR3,MR2,DW2   STORE; INCREMENT NEXT BOTT               32310710
0254   0060 0C04         1072            EXH   MR0,MR0,I4        (USED:SIZE)                              32310720
0255   0060 0800         1073            LHL   MR0,MR0           (0:SIZE)                                 32310730
0256   001C 0050         1074            S     NULL,MR0,MDR      (0:NEXT BOTT) - (0:SIZE)                 32310740
0257   3C40 2250         1075            BT    C,SETCC0,DW2      BRANCH: NO LIST WRAP.                    32310750
0258   08E5 0170         1076            L     MDR,NULL,JAM+D2   SET NEXT BOTT = 0,                      32310760
                         1077  *                                 SET CC = 0, VECTOR TO STH.D2.            32310770
```

LIST INSTRUCTIONS

```
0000 0259                1079  RTL      EQU   *                    ENTERED VIA DROM1              * 66 * 32310790
0259   F053 0174         1080           L     MR3,NULL,DR4+I4      CONSTANT; FETCH (SIZE:USED)             32310800
025A   B060 0054         1081           L     MR0,MDR,DR2+I4       FETCH (CURR TCP)                        32310810
025B   009C 3805         1082           SDEC  NULL,MR3,MR0,LHL+JAM TEST NUMBER USED, SET CC = 0 OR 2       32310820
025C   0C40 2280         1083           BT    C,SETCC4A            BRANCH: LIST ALREADY EMPTY.             32310830
025D   0062 0850         1084           LHL   MR2,MDR              MR2 = (CURR TCP)                        32310840
025E   0061 0A20         1085           SLL   MR1,MR2              COMPUTE A(SLOT)                         32310850
025F   0061 0A10         1086           SLL   MR1,MR1              .                                       32310860
0260   0006 1060         1087           A     MAR,MR1,MAR          .                                       32310870
0261   F066 00D0         1088           L     MAR,SR,DR4           READ; POINT TO (SIZE:USED)              32310880
0262   0061 0050         1089           L     MR1,MDR              DATA FROM LIST SLOT                     32310890
0263   0015 3005         1090           SDEC  MDR,MR3,MR0          DECREMENT NUMBER USED                   32310900
0264   7005 3025         1091           AINC  MDR,MR3,MR2,DW4      STORE; INCREMENT CURR TCP               32310910
0265   0060 0C00         1092           EXH   MR0,MR0              MR0 = (USED:SIZE)                       32310920
0266   001C 2805         1093           SDEC  NULL,MR2,MR0,LHL     (0:SIZE) - (OLD CURR TOP + 1)           32310930
0267   0C10 2694         1094           BT    G,RTL.010,I4         BRANCH: NO LIST WRAP.                   32310940
0268   0065 0170         1095           L     MDR,NULL             LIST WRAP - SET CURR TOP = 0.           32310950
0269   30AF F002         1096  RTL.010  NI    FLR,PSW,2,DW2+JAM    STORE NEW CURR TOP, CC=0 OR 2           32310960
026A   D068 0010         1097           L     YD,MR1,IR            YD = DATA FROM LIST; EXIT.              32310970


0000 026B                1099  RBL      EQU   *                    ENTERED VIA DROM1              * 67 * 32310980
026B   F063 0174         1100           L     MR3,NULL,DR4+I4      CONSTANT; FETCH (SIZE:USED)             32311000
026C   F060 0054         1101           L     MR0,MDR,DR4+I4       MR0 = (SIZE:USED)                       32311010
026D   009C 3805         1102           SDEC  NULL,MR3,MR0,LHL+JAM TEST NUMBER USED; SET CC = 0 OR 2       32311020
026E   0C40 2280         1103           BT    C,SETCC4A            BRANCH: LIST ALREADY EMPTY.             32311030
026F   0012 3855         1104           SDEC  MR2,MR3,MDR,LHL      MR2 = (NEXT BOTT) - 1                   32311040
0270   0E40 2730         1105           BF    C,RBL.010            BRANCH: NO LIST WRAP.                   32311050
0271   0062 0C00         1106           EXH   MR2,MR0              GIVING (USED:SIZE)                      32311060
0272   0012 3825         1107           SDEC  MR2,MR3,MR2,LHL      LIST WRAP. SET NEXT BOTT = (SIZE) -1    32311070
0273   0061 0A20         1108  RBL.010  SLL   MR1,MR2              COMPUTE A(SLOT)                         32311080
0274   0061 0A10         1109           SLL   MR1,MR1              .                                       32311090
0275   0006 1060         1110           A     MAR,MR1,MAR          .                                       32311100
0276   F006 E002         1111           AI    MAR,SR,2,DR4         FETCH DATA; POINT NUMBER USED           32311110
0277   0061 0050         1112           L     MR1,MDR              MR1 = DATA FROM LIST BODY               32311120
0278   0015 3005         1113           SDEC  MDR,MR3,MR0          DECREMENT NUMBER USED                   32311130
0279   3065 0024         1114           L     MDR,MR2,DW2+I4       STORE; POINT TO NEXT BOTT               32311140
027A   30AF F002         1115           NI    FLR,PSW,2,DW2+JAM    STORE NEW NEXT BOTT, CC=0 OR 2          32311150
027B   D058 0010         1116           L     YD,MR1,IR            YD = DATA FROM LIST; EXIT.              32311160
```

SHIFT INSTRUCTIONS

```
027C   00EC 0080   1118  SFSHFTF  L     NULL,YD,JAM      SET CC FOR 32-BIT VALUE                  32311180
027D   086B 00B0   1119            L     CNTR,YSI,D2      LOAD SHIFT COUNT;                        32311190
                   1120  *                                VECTOR TO SLLS, SRLS                     32311200

027E   0065 0080   1122  SFSHFTH  L     MDR,YD           SET CC FOR 16-BIT VALUE                  32311220
027F   00EC 0550   1123            EXT   NULL,MDR,JAM     .                                        32311230
0280   086B 00B0   1124            L     CNTR,YSI,D2      LOAD SHIFT COUNT;                        32311240
                   1125  *                                VECTOR TO SLHLS, SRHLS                   32311250

0281   00EC 0080   1127  RISHFTF  L     NULL,YD,JAM      SET CC FOR 32-BIT VALUE                  32311270
0282   082B E01F   1128            NI    CNTR,SR,31,D2    LOAD SHIFT COUNT,                        32311280
                   1129  *                                VECTOR TO SLL,SRL,SLA,SRA,RLL,RRL        32311290

0283   0065 0080   1131  RISHFTH  L     MDR,YD           SET CC FOR 16-BIT VALUE                  32311310
0284   00EC 0550   1132            EXT   NULL,MDR,JAM     .                                        32311320
0285   082B E00F   1133            NI    CNTR,SR,15,D2    LOAD SHIFT COUNT,                        32311330
                   1134  *                                VECTOR TO SLHL,SRHL,SLHA,SRHA            32311340

0000 0286          1136  SRHLS    EQU   *                ENTERED VIA DROM2 (SFSHFTH)   * 90 *      32311360
0000 0286          1137  SRHL     EQU   *                ENTERED VIA DROM2 (RISHFTH)   * CC *      32311370
0286   D0E8 0680   1138            SRHL  YD,YD,IR+JAM     REPEATS (CNTR) TIMES                     32311380
                   1139  *                                ALL SHIFTS - CC UPDATED.                 32311390

0000 0287          1141  SLHLS    EQU   *                ENTERED VIA DROM2 (SFSHFTH)   * 91 *      32311410
0000 0287          1142  SLHL     EQU   *                ENTERED VIA DROM2 (RISHFTH)   * CD *      32311420
0287   D0E8 0280   1143            SLHL  YD,YD,IR+JAM     REPEATS (CNTR) TIMES                     32311430

0000 0288          1145  SRHA     EQU   *                ENTERED VIA DROM2 (RISHFTH)   * CE *      32311450
0288   D0E8 0780   1146            SRHA  YD,YD,IR+JAM     REPEATS (CNTR) TIMES                     32311460

0000 0289          1148  SLHA     EQU   *                ENTERED VIA DROM2 (RISHFTH)   * CF *      32311480
0289   D0E8 0380   1149            SLHA  YD,YD,IR+JAM     REPEATS (CNTR) TIMES                     32311490

0000 028A          1151  SRA      EQU   *                ENTERED VIA DROM2 (RISHFTF)   * DD *      32311510
028A   D0E8 0F80   1152            SRA   YD,YD,IR+JAM     REPEATS (CNTR) TIMES                     32311520
```

SHIFT INSTRUCTIONS

```
0000 028B                    1154  RRL     EQU   *                ENTERED VIA DROM2 (RISHFTF)   * EA * 32311540
028B   D0E8 0D80             1155          RRL   YD,YD,IR+JAM     REPEATS (CNTR) TIMES                       32311550

0000 028C                    1157  RLL     EQU   *                ENTERED VIA DROM2 (RISHFTF)   * EB * 32311570
028C   D0E8 0980             1158          RLL   YD,YD,IR+JAM     REPEATS (CNTR) TIMES.                      32311580

0000 028D                    1160  SRLS    EQU   *                ENTERED VIA DROM2 (SFSHFTF)   * 10 * 32311600
0000 028D                    1161  SRL     EQU   *                ENTERED VIA DROM2 (RISHFTF)   * EC * 32311610
028D   D0E8 0E80             1162          SRL   YD,YD,IR+JAM     REPEATS (CNTR) TIMES                       32311620

0000 028E                    1164  SLLS    EQU   *                ENTERED VIA DROM2 (SFSHFTF)   * 11 * 32311640
0000 028E                    1165  SLL     EQU   *                ENTERED VIA DROM2 (RISHFTF)   * ED * 32311650
028E   D0E8 0A80             1166          SLL   YD,YD,IR+JAM     REPEATS (CNTR) TIMES                       32311660

0000 028F                    1168  SLA     EQU   *                ENTERED VIA DROM2  (RISHFTF)  * EF * 32311680
028F   D0E8 0B80             1169          SLA   YD,YD,IR+JAM     REPEATS (CNTR) TIMES                       32311690
```

BRANCH INSTRUCTIONS

```
0000 0290                1171  BALR    EQU   *                ENTERED VIA DROM1                * 01 * 32311710
0000 0290                1172  BAL     EQU   *                ENTERED VIA DROM1                * 41 * 32311720
0290   0068 0040         1173          L     YD,LOC           COPY INCREMENTED LOC TO YD              32311730
0291   0064 00D0         1174  BC      L     LOC,SR           EXECUTE INSTRUCTION AT BRANCH DEST.     32311740
0292   D06C 0170         1175          L     NULL,NULL,IR                                             32311750

0000 0293                1177  BTCR    EQU   *                ENTERED VIA DROM1                * 02 * 32311770
0000 0293                1178  BTC     EQU   *                ENTERED VIA DROM1                * 42 * 32311780
0293   DD20 2910         1179          BT    MSK,BC,IR        BRANCH IF MASK TRUE, ELSE EXIT.         32311790

0000 0294                1181  BFCR    EQU   *                ENTERED VIA DROM1                * 03 * 32311810
0000 0294                1182  BFC     EQU   *                ENTERED VIA DROM1                * 43 * 32311820
0294   DF20 2910         1183          BF    MSK,BC,IR        BRANCH IF MASK FALSE, ELSE EXIT.        32311830

0000 0295                1185  BTBS    EQU   *                ENTERED VIA DROM1                * 20 * 32311850
0295   DD20 29C0         1186          BT    MSK,BBS,IR       BRANCH IF MASK TRUE, ELSE EXIT.         32311860

0000 0296                1188  BTFS    EQU   *                ENTERED VIA DROM1                * 21 * 32311880
0296   DD20 2990         1189          BT    MSK,BFS,IR       BRANCH IF MASK TRUE, ELSE EXIT.         32311890

0000 0297                1191  BFBS    EQU   *                ENTERED VIA DROM1                * 22 * 32311910
0297   DF20 29C0         1192          BF    MSK,BBS,IR       BRANCH IF MASK FALSE, ELSE EXIT.        32311920

0000 0298                1194  BFFS    EQU   *                ENTERED VIA DROM1                * 23 * 32311940
0298   DF20 2990         1195          BF    MSK,BFS,IR       BRANCH IF MASK FALSE, ELSE EXIT.        32311950

0299   0061 8002         1197  BFS     LI    MR1,2            SET UP FOR DECREMENT:                   32311970
029A   0010 1AB0         1198          S     MR0,MR1,YSI,SLL  COMPUTE DISPLACEMENT                   32311980
029B   0804 0040         1199          A     LOC,MR0,LOC,D2   ADD TO LOC & EXIT.                     32311990

029C   0060 0AB0         1201  BBS     SLL   MR0,YSI          COMPUTE DECREMENT                       32312010
029D   0814 0045         1202          SDEC  LOC,MR0,LOC,D2   DECREMENT LOC & EXIT.                   32312020

0000 029E                1204  BXLH    EQU   *                ENTERED VIA DROM1                       32312040
029E   0060 00AF         1205          L     MR0,YDI,LYSI     YSI = MR0 = R1 SELECT FIELD             32312050
029F   000A 8001         1206          AI    YDI,MR0,1        POINT R1+1                              32312060
02A0   0009 5082         1207          A     YS,YS,YD,YDP1    R1 = (R1) + (R1+1) = NEW COUNT          32312070
02A1   081C 5080         1208          S     NULL,YS,YD,D2    SUBTRACT NEW COUNT FROM LIMIT;          32312080
                         1209  *                              VECTOR TO BXH, BXLE.                    32312090

0000 02A2                1211  BXH     EQU   *                ENTER VIA DROM2 (BXLH)           * C0 * 32312110
02A2   DC40 2910         1212          BT    C,BC,IR          BRANCH IF > LIMIT, ELSE EXIT.           32312120

0000 02A3                1214  BXLE    EQU   *                ENTER VIA DROM2 (BXLH)           * C1 * 32312140
02A3   DE40 2910         1215          BF    C,BC,IR          BRANCH IF NOT > LIMIT, ELSE EXIT.       32312150
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ARITHMETIC & LOGICAL INSTRUCTIONS

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0000 02A4                1217  AM       EQU   *                    ENTERED VIA DROM2 (RXF2)      * 51 * 32312170
02A4   0085 4050         1218           A     MDR,YD,MDR,JAM       ADD, SET CC                          32312180
02A5   7E00 0130         1219           B     EXIT,DW4             WRITE TO MEMORY, EXIT.               32312190

0000 02A6                1221  AHM      EQU   *                    ENTERED VIA DROM1             * 61 * 32312210
02A6   B061 0880         1222           LHL   MR1,YD,DR2          KEEP USER R1 B16:B31, GET 2ND OP.    32312220
02A7   0051 0C10         1223           EXH   MR1,MR1              MOVE TO B0:B15.                      32312230
02A8   0060 0850         1224           LHL   MR0,MDR              KEEP B16:B31 OF 2ND OP               32312240
02A9   0080 1C00         1225           A     MR0,MR1,MR0,EXH+JAM  ADD, SET CC,                         32312250
02AA   0865 0C00         1226           EXH   MDR,MR0,D2           DATA TO MDR16:31; VECTOR TO STH.D2    32312260

0000 02AB                1228  CHVR     EQU   *                    ENTERED VIA DROM1             * 12 * 32312280
02AB   0023 F008         1229           NI    MR3,PSW,8            SAVE PREVIOUS CARRY STATE            32312290
02AC   0065 00D0         1230           L     MDR,SR                                                    32312300
02AD   00E8 0550         1231           EXT   YD,MDR,JAM           EXTEND SIGN IN YD, ADJUST CC G&L.    32312310
02AE   004E 40D0         1232           X     SR,YD,SR             SET CHANGED BITS TO 1'S -            32312320
02AF   002C EC01         1233           NI    NULL,SR,'01',EXH     TEST MR0 B15 AGAINST RESULT SIGN     32312330
02B0   0E18 2B20         1234           BF    G+L,CHVR.010         BRANCH: NO OVERFLOW.                 32312340
02B1   0033 B004         1235           OI    MR3,MR3,4            SET OVERFLOW BIT                     32312350
02B2   D0BF 7030         1236  CHVR.010 O     FLR,PSW,MR3,IR+JAM   EXIT WITH CC SET.                   32312360

0000 02B3                1238  THI      EQU   *                    ENTERED VIA DROM1             * C3 * 32312380
0000 02B3                1239  TI       EQU   *                    ENTERED VIA DROM1             * F3 * 32312390
02B3   D0AC 40D0         1240           N     NULL,YD,SR,IR+JAM    SET CC, EXIT.                        32312400

0000 02B4                1242  NH       EQU   *                    ENTERED VIA DROM2  (RXH)     * 44 * 32312420
02B4   D0A8 4550         1243           N     YD,YD,MDR,EXT+IR+JAM YD = RESULT; SET CC, EXIT.           32312430
0000 02B5                1244  N        EQU   *                    ENTERED VIA DROM2  (RXF)     * 54 * 32312440
02B5   D0A8 4050         1245           N     YD,YD,MDR,IR+JAM     YD = RESULT; SET CC, EXIT.           32312450
0000 02B6                1246  NR       EQU   *                    ENTERED VIA DROM1             * 04 * 32312460
0000 02B6                1247  NHI      EQU   *                    ENTERED VIA DROM1             * C4 * 32312470
0000 02B6                1248  NI       EQU   *                    ENTERED VIA DROM1             * F4 * 32312480
02B6   D0A8 40D0         1249           N     YD,YD,SR,IR+JAM      YD = RESULT; SET CC, EXIT.           32312490

0000 02B7                1251  CLR      EQU   *                    ENTERED VIA DROM1             * 05 * 32312510
0000 02B7                1252  CLH      EQU   *                    ENTERED VIA DROM2  (RXH2)     * 45 * 32312520
0000 02B7                1253  CL       EQU   *                    ENTERED VIA DROM2  (RXF2)     * 55 * 32312530
0000 02B7                1254  CLHI     EQU   *                    ENTERED VIA DROM1             * C5 * 32312540
0000 02B7                1255  CLI      EQU   *                    ENTERED VIA DROM1             * F5 * 32312550
02B7   D09C 6080         1256           S     NULL,SR,YD,IR+JAM    SET CC, EXIT.                        32312560
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ARITHMETIC & LOGICAL INSTRUCTIONS

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0000 02B8                1258  OH      EQU   *                        ENTERED VIA DROM2  (RXH)       * 46 * 32312580
02B8   D038 4550         1259          O     YD,YD,MDR,EXT+IR+JAM     YD = RESULT; SET CC, EXIT.              32312590
0000 02B9                1260  O       EQU   *                        ENTERED VIA DROM2  (RXF)       * 56 * 32312600
02B9   D0B8 4050         1261          O     YD,YD,MDR,IR+JAM         YD = RESULT; SET CC, EXIT.              32312610
0000 02BA                1262  OR      EQU   *                        ENTERED VIA DROM1              * 06 * 32312620
0000 02BA                1263  OHI     EQU   *                        ENTERED VIA DROM1              * C6 * 32312630
0000 02BA                1264  OI      EQU   *                        ENTERED VIA DROM1              * F6 * 32312640
02BA   D0B8 40D0         1265          O     YD,YD,SR,IR+JAM          YD = RESULT; SET CC, EXIT.              32312650

0000 02BB                1267  XH      EQU   *                        ENTERED VIA DROM2  (RXH)       * 47 * 32312670
02BB   D0C8 4550         1268          X     YD,YD,MDR,EXT+IR+JAM     YD = RESULT; SET CC, EXIT.              32312680
0000 02BC                1269  X       EQU   *                        ENTERED VIA DROM2  (RXF)       * 57 * 32312690
02BC   D0C8 4050         1270          X     YD,YD,MDR,IR+JAM         YD = RESULT; SET CC, EXIT.              32312700
0000 02BD                1271  XR      EQU   *                        ENTERED VIA DROM1              * 07 * 32312710
0000 02BD                1272  XHI     EQU   *                        ENTERED VIA DROM1              * C7 * 32312720
0000 02BD                1273  XI      EQU   *                        ENTERED VIA DROM1              * F7 * 32312730
02BD   D0C8 40D0         1274          X     YD,YD,SR,IR+JAM          YD = RESULT; SET CC, EXIT.              32312740

0000 02BE                1276  CH      EQU   *                        ENTERED VIA DROM1              * 49 * 32312760
02BE   B06E 0F80         1277          SRA   SR,YD,DR2                PROPAGATE 1ST OP SIGN, FETCH 2ND        32312770
02BF   008C 60D5         1278          AINC  NULL,SR,SR,JAM           SET CC = 2 OR 9                         32312780
02C0   004C 4550         1279          X     NULL,YD,MDR,EXT          TEST IF SIGNS SAME, 2 OPERANDS          32312790
02C1   DE08 2310         1280          BF    L,RXH1,IR                BRANCH: SIGNS SAME; ELSE EXIT.          32312800
                         1281  *                                      (VECTORS TO CLH)                        32312810

0000 02C2                1283  C       EQU   *                        ENTERED VIA DROM1              * 59 * 32312830
02C2   F06E 0F80         1284          SRA   SR,YD,DR4                PROPAGATE 1ST OP SIGN, FETCH 2ND        32312840
02C3   008C 60D5         1285          AINC  NULL,SR,SR,JAM           SET CC = 2 OR 9                         32312850
02C4   004C 4050         1286          X     NULL,YD,MDR              TEST IF SIGNS SAME, 2 OPERANDS          32312860
02C5   DE08 2340         1287          BF    L,RXF1,IR                BRANCH: SIGNS SAME; ELSE EXIT.          32312870
                         1288  *                                      (VECTORS TO CL)                         32312880

0000 02C6                1290  CR      EQU   *                        ENTERED VIA DROM1              * 09 * 32312900
0000 02C6                1291  CHI     EQU   *                        ENTERED VIA DROM1              * C9 * 32312910
0000 02C6                1292  CI      EQU   *                        ENTERED VIA DROM1              * F9 * 32312920
02C6   004C 40D0         1293          X     NULL,YD,SR               TEST IF SAME SIGN, YD:YS                32312930
02C7   0E08 2B70         1294          BF    L,CLR                    BRANCH: SIGNS ALIKE.                    32312940
02C8   006E 0F80         1295          SRA   SR,YD                    PROPAGATE 1ST OP SIGN                   32312950
02C9   D08C 60D5         1296          A     NULL,SR,SR,IR+JAM+JAMCI  COMPARE, SET CC, EXIT.                  32312960
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ARITHMETIC & LOGICAL INSTRUCTIONS

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0000 02CA                1298  AH       EQU   *                    ENTERED VIA DROM2  (RXH)      * 4A * 32312980
02CA   D088 4550         1299           A     YD,YD,MDR,EXT+IR+JAM YD = RESULT; SET CC, EXIT.          32312990
0000 02CB                1300  A        EQU   *                    ENTERED VIA DROM2  (RXF)      * 5A * 32313000
02CB   D088 4050         1301           A     YD,YD,MDR,IR+JAM     YD = RESULT; SET CC, EXIT.          32313010
0000 02CC                1302  AR       EQU   *                    ENTERED VIA DROM1             * 0A * 32313020
0000 02CC                1303  AHI      EQU   *                    ENTERED VIA DROM1             * CA * 32313030
0000 02CC                1304  AI       EQU   *                    ENTERED VIA DROM1             * FA * 32313040
02CC   D088 40D0         1305           A     YD,YD,SR,IR+JAM      YD  = RESULT; SET CC, EXIT.         32313050

0000 02CD                1307  AIS      EQU   *                    ENTERED VIA DROM1             * 26 * 32313070
02CD   D088 40B0         1308           A     YD,YD,YSI,IR+JAM     YD = RESULT; SET CC, EXIT.          32313080

0000 02CE                1310  SIS      EQU   *                    ENTERED VIA DROM1             * 27 * 32313100
02CE   006E 00B0         1311           L     SR,YSI               GET VALUE TO SUBTRACT               32313110

0000 02CF                1313  SR       EQU   *                    ENTERED VIA DROM1             * 0B * 32313130
0000 02CF                1314  SH       EQU   *                    ENTERED VIA DROM2  (RXH2)     * 4B * 32313140
0000 02CF                1315  S        EQU   *                    ENTERED VIA DROM2  (RXF2)     * 5B * 32313150
0000 02CF                1316  SHI      EQU   *                    ENTERED VIA DROM1             * CB * 32313160
0000 02CF                1317  SI       EQU   *                    ENTERED VIA DROM1             * FB * 32313170
02CF   D098 6080         1318           S     YD,SR,YD,IR+JAM      YD = RESULT; SET CC, EXIT.          32313180

0000 02D0                1320  MHR      EQU   *                    ENTERED VIA DROM1           * 0C *  32313200
0000 02D0                1321  MH       EQU   *                    ENTERED VIA DROM2  (RXH2)   * 4C *  32313210
                         1322  *                                  (SR) = MULTIPLIER                   32313220
02D0   0060 0880         1323           LHL   MR0,YD                                                   32313230
02D1   0060 0C00         1324           EXH   MR0,MR0              MR0 = MULTIPLICAND, FORM XXXX0000   32313240
02D2   0068 0170         1325           L     YD,NULL              INITIALIZE PARTIAL SUMMING REGISTER 32313250
02D3   006B 8010         1326           LI    CNTR,16              SET LOOP COUNT                      32313260
02D4   0008 0E86         1327  MHLOOP   MPY   YD,MR0,YD           REPEATS; QUEUE LAST CARRY           32313270
02D5   D068 0E80         1328           SRL   YD,YD,IR             YD = RESULTS                        32313280

0000 02D6                1330  MR       EQU   *                    ENTERED VIA DROM1           * 1C *  32313300
0000 02D6                1331  M        EQU   *                    ENTERED VIA DROM2  (RXF2)   * 5C *  32313310
                         1332  *                                  (SR) = MULTIPLIER.                  32313320
02D6   0068 0172         1333           L     YD,NULL,YDP1         PARTIAL = 0; POINT R1+1.            32313330
02D7   0060 0083         1334           L     MR0,YD,YDM1          MR0 = MULTIPLICAND                  32313340
02D8   006B 8020         1335           LI    CNTR,32              SET LOOP COUNT                      32313350
02D9   0008 0E86         1336  MLOOP    MPY   YD,MR0,YD           REPEATS; QUEUE LAST CARRY           32313360
02DA   0068 0E82         1337           SRL   YD,YD,YDP1           (R1,P1+1) = RESULT.                 32313370
02DB   D068 00D0         1338           L     YD,SR,IR             LOAD ISR RESULT, EXIT.              32313380
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ARITHMETIC & LOGICAL INSTRUCTIONS

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0000 02DC                1340  DHR       EQU   *                ENTERED VIA DROM1              * 0D *   32313400
02DC   0860 08D0         1341            LHL   MR0,SR,D2        DIVISOR; VECTOR TO DH.005                32313410
0000 02DD                1342  DH        EQU   *                ENTERED VIA DROM2  (RXH)       * 4D *   32313420
02DD   0060 0850         1343            LHL   MR0,MDR          DIVISOR                                  32313430
02DE   0041 4C00         1344  DH.005    X     MR1,YD,MR0,EXH   MR1 BIT 0 = SGN(QUOT)                    32313440
02DF   0060 0C00         1345            EXH   MR0,MR0          DIVISOR, FORM XXXX0000                   32313450
02E0   0C08 2E30         1346            BT    L,DH.010         BRANCH: ALREADY NEGATIVE                 32313460
02E1   0E10 0CF0         1347            BF    G,AFAUL0         BRANCH: DIVIDE-BY-ZERO.                  32313470
02E2   0010 8000         1348            SI    MR0,MR0,0        FORCE NEGATIVE (2'S COMP)                32313480
02E3   0062 0080         1349  DH.010    L     MR2,YD           DIVIDEND                                 32313490
02E4   0E08 2E60         1350            BF    L,DH.020                                                  32313500
02E5   0012 A000         1351            SI    MR2,MR2,0        FORCE POSITIVE (2'S COMP)                32313510
02E6   000C 0020         1352  DH.020    A     NULL,MR0,MR2     TEST O'FLO: MSB DVD LESS DVSR            32313520
02E7   0C40 0D00         1353            BT    C,DHFAULT        BRANCH: OVERFLOW WILL OCCUR.             32313530
02E8   006E 0170         1354            L     SR,NULL          CONSTRAIN DIVD TO 32 BITS                32313540
02E9   006B 8010         1355            LI    CNTR,16          SET FOR 16 ITERATIONS                    32313550
02EA   0002 0A27         1356  DHLOOP    DIV   MR2,MR0,MR2      DO HALFWORD DIVISION                     32313560
02EB   006C 0010         1357            L     NULL,MR1         RESULT SHOULD BE NEGATIVE ?              32313570
02EC   0E08 2EF0         1358            BF    L,DH.025         BRANCH: SHOULD BE POSITIVE.              32313580
02ED   001E E000         1359            SI    SR,SR,0          2'S COMPLEMENT                           32313590
02EE   0E18 2F10         1360            BF    G+L,DH.030       BRANCH: ZERO DOESN'T CHANGE SIGN.        32313600
02EF   004C 1CD0         1361  DH.025    X     NULL,MR1,SR,EXH  GET EXPECTED SIGN ?                     32313610
02F0   0C08 0D00         1362            BT    L,DHFAULT        BRANCH: NO; FAULT.                       32313620
02F1   004C 4C20         1363  DH.030    X     NULL,YD,MR2,EXH  REMAINDER HAS CORRECT SIGN ?             32313630
02F2   0E08 2F40         1364            BF    L,DH.040         BRANCH: YES.                             32313640
02F3   0012 A000         1365            SI    MR2,MR2,0        2'S COMPLEMENT.                          32313650
02F4   0065 0C20         1366  DH.040    EXH   MDR,MR2          REMAINDER FORM 0000XXXX                  32313660
02F5   0068 0552         1367            EXT   YD,MDR,YDP1      COPY REMAINDER TO R1                     32313670
02F6   0065 00D0         1368            L     MDR,SR                                                    32313680
02F7   D068 0550         1369            EXT   YD,MDR,IR        COPY QUOTIENT, EXIT.                     32313690

0000 00D0                1371  DHFAULT   EQU   AFAUL1           QUOTIENT OVERFLOW                        32313710
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ARITHMETIC & LOGICAL INSTRUCTIONS

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0000 02F8                1373  DR      EQU   *                 ENTERED VIA DROM1           * 1D *   32313730
0000 02F8                1374  D       EQU   *                 ENTERED VIA DROM2  (RXF2)   * 5D *   32313740
02F8   0010 6172         1375          S     MR0,SR,NULL,YDP1  COMPLEMENT DIVISOR, POINT R1+1      32313750
02F9   0C08 2FC0         1376          BT    L,D.010           BRANCH: ALREADY NEGATIVE.          32313760
02FA   0E10 0CF0         1377          BF    G,AFAUL0          BRANCH: DIVIDE-BY-ZERO.            32313770
02FB   0010 8000         1378          SI    MR0,MR0,0         FORCE NEGATIVE (2'S COMP)          32313780
02FC   0065 0083         1379  D.010   L     MDR,YD,YDM1       COPY LSB DIVD, POINT R1            32313790
02FD   0041 6080         1380          X     MR1,SR,YD         MR1 = RESULT SIGN                  32313800
02FE   0062 0080         1381          L     MR2,YD            COPY MSB DIVIDEND                  32313810
02FF   0E08 3050         1382          BF    L,D.020           BRANCH: ALREADY POSITIVE.          32313820
0300   0018 4172         1383          S     YD,YD,NULL,YDP1   2'S COMPLEMENT; POINT R1+1.         32313830
0301   0018 4173         1384          S     YD,YD,NULL,YDM1   COMPLEMENT LOW HALF               32313840
0302   0E18 3050         1385          BF    G+L,D.020         BRANCH: NO BORROW PROPAGATION      32313850
0303   0063 8001         1386          LI    MR3,1                                                32313860
0304   0018 3080         1387          S     YD,MR3,YD         PROPAGATE BORROW                   32313870
0305   000C 0080         1388  D.020   A     NULL,MR0,YD       O'FLOW? MSB DIVD LESS DVSR (USED)  32313880
0306   0C40 3142         1389          BT    C,DFAULT,YDP1     BRANCH: OVERFLOW WILL OCCUR        32313890
0307   006E 0083         1390          L     SR,YD,YDM1        SR = 32 LSB DIVIDEND               32313900
0308   005B 8020         1391          LI    CNTR,32           SET FOR 32 ITERATIONS              32313910
0309   0008 0A87         1392  DLOOP   DIV   YD,MR0,YD         DO FULLWORD DIVISION               32313920
030A   006C 0012         1393          L     NULL,MR1,YDP1     RESULT SHOULD BE NEGATIVE ?        32313930
030B   0E08 30E0         1394          BF    L,D.025           BRANCH: NO.                        32313940
030C   001E E000         1395          SI    SR,SR,0           2'S COMPLEMENT                     32313950
030D   0E18 3100         1396          BF    G+L,D.030         BRANCH: ZERO DOESN'T CHANGE SIGN   32313960
030E   004C 6010         1397  D.025   X     NULL,SR,MR1       GET EXPECTED SIGN ?                32313970
030F   0C08 3140         1398          BT    L,DFAULT          BRANCH: NO; OVERFLOW.              32313980
0310   0068 00D3         1399  D.030   L     YD,SR,YDM1        COPY QUOTIENT, POINT R1            32313990
0311   004C 2080         1400          X     NULL,MR2,YD       REMAINDER HAS CORRECT SIGN ?       32314000
0312   DC08 3130         1401          BT    L,*+1,IR          EXIT IF YES; ELSE                  32314010
0313   D018 C000         1402          SI    YD,YD,0,IR        2'S COMPLEMENT REMAINDER, EXIT.    32314020

0314   0068 0053         1404  DFAULT  L     YD,MDR,YDM1       RESTORE LSB DIVIDEND               32314040
0315   0068 0020         1405          L     YD,MR2            RESTORE MSB DIVIDEND               32314050
0316   0E00 0D00         1406          B     AFAUL1            TAKE PSW SWAP                      32314060
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LOADS AND STORES

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0000 0317                1408  LH       EQU   *                ENTERED VIA DROM2  (RXH)      * 48 * 32314080
0317   D0E8 0550         1409           EXT   YD,MDR,IR+JAM    YD = RESULT; SET CC, EXIT.              32314090
0000 0318                1410  L        EQU   *                ENTERED VIA DROM2  (RXF)      * 58 * 32314100
0318   D0E8 0050         1411           L     YD,MDR,IR+JAM    YD = RESULT; SET CC, EXIT.              32314110
0000 0319                1412  LR       EQU   *                ENTERED VIA DROM1             * 08 * 32314120
0000 0319                1413  LHI      EQU   *                ENTERED VIA DROM1             * C8 * 32314130
0000 0319                1414  LI       EQU   *                ENTERED VIA DROM1             * F8 * 32314140
0319   D0E8 00D0         1415           L     YD,SR,IR+JAM     YD = RESULT; SET CC, EXIT.              32314150

0000 031A                1417  LIS      EQU   *                ENTERED VIA DROM1             * 24 * 32314170
031A   D0E8 00B0         1418           L     YD,YSI,IR+JAM    COPY YSI TO YD; SET CC, EXIT.           32314180

0000 031B                1420  LCS      EQU   *                ENTERED VIA DROM1             * 25 * 32314200
031B   0068 00B0         1421           L     YD,YSI                                                 32314210
031C   0018 C000         1422           SI    YD,YD,0          2'S COMPLEMENT TO YD;                  32314220
031D   D0EC 0080         1423           L     NULL,YD,IR+JAM   SET CC, EXIT.                          32314230

0000 031E                1425  LHL      EQU   *                ENTERED VIA DROM2  (RXH)      * 73 * 32314250
031E   D0E8 0850         1426           LHL   YD,MDR,IR+JAM    LOAD B16:B31, SET CC, EXIT.             32314260

0000 031F                1428  EXHR     EQU   *                ENTERED VIA DROM1             * 34 * 32314280
031F   D068 0CD0         1429           EXH   YD,SR,IR         SWAP B0:B15 & B16:B31, EXIT.            32314290

0000 0320                1431  LM       EQU   *                ENTERED VIA DROM1             * D1 * 32314310
0320   FD88 3244         1432           BT    YDC,LM1,DR4+I4   BRANCH: LOADING R15                   32314320
0321   0060 00A0         1433           L     MR0,YDI                                                32314330
0322   001B 800F         1434           SI    CNTR,MR0,15      CALCULATE STEPS REQ'D                  32314340
0323   F068 0052         1435  LMLOOP   L     YD,MDR,DR4+YDP1  (AUTO-I4) LOAD DATA                   32314350
0324   0068 0050         1436  LM1      L     YD,MDR           LOAD LAST DATA TO R15                  32314360
0325   DCB0 3260         1437           BT    MAT+MPE,*+1,IR   BRANCH: ERROR; ELSE EXIT.             32314370
0326   5E00 0AD0         1438           B     LMFAULT,ENACLK   GO REPORT FAULT TO USER.               32314380

0000 0327                1440  LM.ENT   EQU   *                MEMORY READING FIRST DATA              32314400
0327   006B 800F         1441           LI    CNTR,15                                                32314410
0328   F068 0052         1442           L     YD,MDR,YDP1+DR4  (AUTO-I4)                             32314420
0329   0068 0052         1443           L     YD,MDR,YDP1      LOAD R15                              32314430
032A   0E01 00E0         1444           RETN                   AND RETURN.                           32314440

0000 032B                1446  LA       EQU   *                ENTERED VIA DROM1             * E6 * 32314460
032B   D068 0060         1447           L     YD,MAR,IR        YD = CALCULATED ADDRESS.                32314470
```

LOADS AND STORES

```
0000 032C                1449  LRA       EQU   *                 ENTERED VIA DROM1                * 63 * 32314490
032C   F020 CCFF         1450            NI    MR0,YD,'FF',EXH+DR4 MR0 = SEGMENT # FORM 00XX0000;          32314500
032D   0013 3035         1451            SDEC  MR3,MR3,MR3       FETCH PSTD WHILE FORMING               32314510
032E   0063 0834         1452            LHL   MR3,MR3,I4        CONSTANT '0001FFFF'                    32314520
032F   0033 3A30         1453            O     MR3,MR3,MR3,SLL   .                                      32314530
0330   F061 0050         1454            L     MR1,MDR,DR4       MR1 = PSTD; FETCH SSTD                 32314540
0331   001C 0E10         1455            S     NULL,MR0,MR1,SRL  (PST SIZE - 1) LESS SEGMENT #          32314550
0332   0C40 22A0         1456            BT    C,SETCC8A         BRANCH: PST SIZE EXCEEDED; UNMAPPED.   32314560
0333   002E 3050         1457            N     SR,MR3,MDR        SR = A(SST)/128                        32314570
0334   0062 0050         1458            L     MR2,MDR           MR2 = SSTD                             32314580
0335   0026 3010         1459            N     MAR,MR3,MR1       MAR = A(PST)/128                       32314590
0336   006B 8007         1460            LI    CNTR,7                                                   32314600
0337   0066 0A6C         1461            SLL   MAR,MAR,DWSHFT    MULTIPLY BOTH BY 128.                  32314610
0338   0060 0C00         1462            EXH   MR0,MR0           COMPUTE A(PSTE)                        32314620
0339   006B 8003         1463            LI    CNTR,3            .                                      32314630
033A   0060 0A00         1464            SLL   MR0,MR0           .                                      32314640
033B   0006 0060         1465            A     MAR,MR0,MAR       .                                      32314650
033C   F060 8080         1466            LI    MR0,'80',DR4      FETCH PSTE; MR0 = '00000080'           32314660
033D   006C 0A50         1467            SLL   NULL,MDR          PSTE B01 SET ?                         32314670
033E   0E08 2290         1468            BF    L,SETCC4          BRANCH: SEGMENT NOT PRESENT.           32314680
033F   002C 0C50         1469  LRA.SHAR  N     NULL,MR0,MDR,EXH  STE B08 SET (SHARED) ?                 32314690
0340   0E18 3500         1470            BF    G+L,LRA.PRI       BRANCH: NO. PRIVATE SEGMENT.           32314700
0341   0026 3050         1471            N     MAR,MR3,MDR       EXTRACT PSTE OFFSET/RELOC FIELD        32314710
0342   0020 2030         1472            N     MR0,MR2,MR3       EXTRACT ENCODED SST SIZE               32314720
0343   0040 0020         1473            X     MR0,MR0,MR2       .                                      32314730
0344   0060 0C00         1474            EXH   MR0,MR0           GET IN FORM 0000XXXX                   32314740
0345   0060 0A00         1475            SLL   MR0,MR0           SCALE SIZE (8 BYTES/ENTRY)             32314750
0346   001C 0E65         1476            SDEC  NULL,MR0,MAR,SRL  SST SIZE EXCEEDED ?                    32314760
0347   0E40 22B0         1477            BF    C,SETCC8          BRANCH: SST SIZE EXCEEDED; UNMAPPED.   32314770
0348   0006 6060         1478            A     MAR,SR,MAR        A(SST)+BYTE OFFSET                     32314780
0349   0062 0050         1479            L     MR2,MDR           COPY OF PSTE                           32314790
034A   F011 1015         1480            SDEC  MR1,MR1,MR1,DR4   FETCH SSTE, BUILD CONSTANT:           32314800
034B   0041 941C         1481            XI    MR1,MR1,'1C',EXB  MR1 = 'FFFFE3FF'                      32314810
034C   0032 2C10         1482            O     MR2,MR2,MR1,EXH   SET ALL PSTE BITS BUT ACCESS MODES    32314820
034D   006C 0A50         1483            SLL   NULL,MDR          SSTE B01 SET ?                         32314830
034E   0E08 2290         1484            BF    L,SETCC4          BRANCH: SEGMENT NOT PRESENT.           32314840
034F   0822 2050         1485            N     MR2,MR2,MDR,D2    'AND' SSTE, PSTE ACCESS MODE BITS      32314850
0350   0062 0050         1486  LRA.PRI   L     MR2,MDR           COPY PSTE                              32314860
0351   0020 AC3E         1487  LRA.SH2   NI    MR0,MR2,'3E',EXH  EXTRACT STE SEGMENT LIMIT FIELD        32314870
0352   0021 C4F8         1488            NI    MR1,YD,'F8',EXB   SEGMENT FIELD FROM PRESENTED ADDRESS  32314880
0353   0060 0A00         1489            SLL   MR0,MR0           ALIGN..                                32314890
0354   0060 0C00         1490            EXH   MR0,MR0           .                                      32314900
0355   0060 0400         1491            EXB   MR0,MR0           .                                      32314910
0356   001C 1A00         1492            S     NULL,MR1,MR0,SLL  SEGMENT LIMIT EXCEEDED ?               32314920
0357   0C40 22B0         1493            BT    C,SETCC8          BRANCH: SEG LIM VIOLATION (UNMAPPED)   32314930
0358   0020 2030         1494            N     MR0,MR2,MR3       EXTRACT STE SRF FIEL)                  32314940
0359   006B 8007         1495            LI    CNTR,7                                                   32314950
035A   0060 0A00         1496            SLL   MR0,MR0           MULTIPLY BY 128                        32314960
035B   0008 0880         1497            A     YD,MR0,YD,LHL     TRANSLATE ADDRESS                      32314970
035C   0062 0C20         1498            EXH   MR2,MR2           TO TEST ACCESS PRIVILEGES -            32314980
035D   0042 A41C         1499            XI    MR2,MR2,'1C',EXB  CONVERT ACCESS PRIV'S TO PROTECT KEYS  32314990
035E   00AC A408         1500            NI    NULL,MR2,'08',EXB+JAM CC = 2 IF WRITE-PROTECT            32315000
035F   002C A414         1501            NI    NULL,MR2,'14',EXB TEST READ, EXECUTE PROTECT             32315010
0360   DC18 22C0         1502            BT    G+L,ADDCC1,IR     BRANCH: READ OR EXECUTE PROTECTED.     32315020
```

LOADS AND STORES

```
0000 0361                1504  TS       EQU  *                ENTERED VIA DROM1                * E0 * 32315040
0361   906C 0170         1505           I    NULL,NULL,RAS    READ HALFWORD, WRITE BACK NEGATIVE.  32315050
0362   D0EC 0550         1506           EXIT NULL,MDR,IR+JAM  TEST HALFWORD READ, EXIT.            32315060

0000 0363                1508  STH      EQU  *                ENTERED VIA DROM1                * 40 * 32315080
0000 0363                1509  ST       EQU  *                ENTERED VIA DROM1                * 50 * 32315090
0363   0865 0080         1510           I    MDR,YD,D2        DATA TO MDR; VECTOR TO STH.D2, STF.D232315100

0000 0364                1512  STM      EQU  *                ENTERED VIA DROM1                * D0 * 32315120
0364   0065 0080         1513           I    MDR,YD           DATA TO STORE                        32315130
0365   0060 00A2         1514           I    MR0,YDI,YDP1                                          32315140
0366   0013 8010         1515           SC   CNTR,MR0,16      STEPS REQUIRED                       32315150
0367   7865 0082         1516  STMLOOP  I    MDR,YD,DW4+YDP1+D2 STORE, READY FOR NEXT (AUTO-I4)    32315160
                         1517  *                               LOOP THROUGH R15, VECTOR TO EXIT     32315170

                         1519  STM.ENT  EQU  *                STORES 16 REGISTERS                  32315190
0000 0368                1520           I    MDR,YD,YDP1      FIRST DATA TO STORE                  32315200
0368   0065 0082         1521           SC   CNTR,15          STEPS REQUIRED                       32315210
0369   006B 800F         1522           I    MDR,YD,DW4+YDP1  STORE, READY FOR NEXT (AUTO-I4)      32315220
036A   7065 0082         1523           RETN DW4+I4           STORE LAST, RETURN.                  32315230
036B   7E01 00E4
```

BIT INSTRUCTIONS

```
0000 036C                1525  RXBIT   EQU   *                    ENTERED VIA DROM1                        32315250
036C   0061 0E80         1526         SRL   MR1,YD               BIT POINTER:                             32315260
036D   0061 0E10         1527         SRL   MR1,MR1                                                       32315270
036E   0006 6E10         1528         A     MAR,SR,MR1,SRL       FETCH APPROPRIATE HALFWORD.              32315280
036F   B061 8080         1529         LI    MR1,'80',DR2         SET MASK BIT = '00000080'                32315290
0370   002B C007         1530         NI    CNTR,YD,7            LOAD COUNTER WITH SHIFT COUNT            32315300
0371   0861 0E10         1531         SRL   MR1,MR1,D2           (REPEATS) POSITION MASK BIT              32315310
                         1532  *                                 VECTOR TO SBT,RBT,CBT,TBT.               32315320

0000 0372                1534  SBT     EQU   *                    ENTERED VIA DROM2  (RXBIT)    * 75 *     32315340
0372   00AC 1450         1535         N     NULL,MR1,MDR,EXB+JAM TEST OLD STATE, ADJUST G FLAG            32315350
0373   DE10 3740         1536         BF    G,*+1,IR             EXIT IF ALREADY SET, ELSE:               32315360
0374   0031 1450         1537         O     MR1,MR1,MDR,EXB      SET ADDRESSED BIT                        32315370
0375   0065 0410         1538         EXB   MDR,MR1              POSITION BYTE                            32315380
0376   1E00 0130         1539         B     EXIT,DW1             STORE BYTE, GO EXIT.                     32315390

0000 0377                1541  RBT     EQU   *                    ENTERED VIA DROM2  (RXBIT)    * 76 *     32315410
0377   00A2 1450         1542         N     MR2,MR1,MDR,EXB+JAM TEST OLD STATE, ADJUST G FLAG            32315420
0378   DC10 3790         1543         BT    G,*+1,IR             EXIT IF ALREADY ZERO, ELSE:              32315430
0379   0041 2450         1544         X     MR1,MR2,MDR,EXB      RESET ADDRESSED BIT                      32315440
037A   0065 0410         1545         EXB   MDR,MR1              POSITION BYTE                            32315450
037B   1E00 0130         1546         B     EXIT,DW1             STORE BYTE, GO EXIT.                     32315460

0000 037C                1548  CBT     EQU   *                    ENTERED VIA DROM2  (RXBIT)    * 77 *     32315480
037C   0042 1450         1549         X     MR2,MR1,MDR,EXB      COMPLEMENT ADDRESSED BIT                 32315490
037D   0065 0420         1550         EXB   MDR,MR2              POSITION BYTE TO STORE                   32315500
037E   1022 1020         1551         N     MR2,MR1,MR2,DW1      STORE; EXTRACT BIT (NEW STATE)           32315510
037F   D0CC 2010         1552         X     NULL,MR2,MR1,IR+JAM SET G FLAG FOR OLD STATE, EXIT.          32315520

0000 0380                1554  TBT     EQU   *                    ENTERED VIA DROM2  (RXBIT)    * 74 *     32315540
0380   D0AC 1450         1555         N     NULL,MR1,MDR,EXB+IR+JAM TEST BIT, SET CC, EXIT.              32315550
```

BYTE INSTRUCTIONS

```
0000 0381                1557  LB        EQU   *                ENTERED VIA DROM2  (RXBYTE)   * D3 * 32315570
0381   D028 6450         1558            N     YD,SR,MDR,EXB+IR YD = BYTE; EXIT.                      32315580

0000 0382                1560  LBR       EQU   *                ENTERED VIA DROM1                  * 93 * 32315600
0382   D028 E0FF         1561            NI    YD,SR,'FF',IR    MASK TO 8 BITS IN YD, EXIT.              32315610

0000 0383                1563  STB       EQU   *                ENTERED VIA DROM1                  * D2 * 32315630
0383   0865 0480         1564            EXB   MDR,YD,D2        POSITION BYTE; VECTOR TO STB.D2.         32315640

0000 0384                1566  STBR      EQU   *                ENTERED VIA DROM1                  * 92 * 32315660
0384   0040 4090         1567            X     MR0,YD,YS        GET DIFFERENCE,                          32315670
0385   0020 80FF         1568            NI    MR0,MR0,'FF'     CONSTRAIN TO LOW BYTE.                   32315680
0386   D049 5000         1569            X     YS,YS,MR0,IR     SWAP YD B24:31 TO YS B24:31, EXIT.       32315690

0000 0387                1571  CLB       EQU   *                ENTERED VIA DROM2  (RXBYTE)   * D4 * 32315710
0387   0020 40D0         1572            N     MR0,YD,SR        EXTRACT B24:31 (MASK = 'FF')             32315720
0388   0021 5450         1573            N     MR1,SR,MDR,EXB   RX BYTE IN MR1 B24:31                   32315730
0389   D09C 1000         1574            S     NULL,MR1,MR0,IR+JAM SET CC, EXIT.                        32315740

0000 038A                1576  EXBR      EQU   *                ENTERED VIA DROM1                  * 94 * 32315760
038A   004E 4490         1577            X     SR,YD,YS,EXB     FORM LOGICAL DIFFERENCE                  32315770
038B   D048 48D0         1578            X     YD,YD,SR,LHL+IR  STORE EXB(YS) TO YD B16:31, EXIT.        32315780

0000 038C                1580  CRC12     EQU   *                ENTERED VIA DROM1                  * 5E * 32315800
038C   B020 C03F         1581            NI    MR0,YD,'3F',DR2  MASK TO 6 BITS, READ RESIDUAL            32315810
038D   0061 840F         1582            LI    MR1,'0F',EXB     TO BUILD '0F01' CONSTANT                 32315820
038E   006A 800A         1583            LI    YDI,10           SET COUNT = 6                            32315830
038F   0E00 3940         1584            B     CRCA                                                      32315840

0000 0390                1586  CRC16     EQU   *                ENTERED VIA DROM1                  * 5F * 32315860
0390   BDC0 39B0         1587            BT    COMM,CRC16AST,DR2 BRANCH: USE COMM ASSIST UNIT.            32315870
0391   0020 C0FF         1588            NI    MR0,YD,'FF'      MASK DATA TO 8 BITS.                     32315880
0392   0061 84A0         1589            LI    MR1,'A0',EXB     TO BUILD 'A001' CONSTANT                 32315890
0393   006A 8008         1590            LI    YDI,8            SET COUNT = 8                            32315900
                         1591  *                                                                         32315910
0394   0031 9001         1592  CRCA      OI    MR1,MR1,1        BUILD POLYNOMIAL CHECK CONSTANT          32315920
0395   0045 0850         1593            X     MDR,MR0,MDR,LHL  XOR IN RESIDUAL                         32315930
0396   0065 0E50         1594  CRCB      SRL   MDR,MDR          SHIFT                                    32315940
0397   0E40 3990         1595            BF    C,CRCC                                                    32315950
0398   0045 1050         1596            X     MDR,MR1,MDR      XOR IN FEEDBACK ON CARRY                 32315960
0399   0F88 3962         1597  CRCC      BF    YDC,CRCB,YDP1    LOOP UNTIL YDCARRY                       32315970
039A   3E00 0130         1598            B     EXIT,DW2         STORE NEW RESIDUAL; GO EXIT.             32315980

039B   006C 0178         1600  CRC16AST  L     NULL,NULL,COMM   'CRC16' CMD TO COMM ASSIST              32316000
039C   006C 0058         1601            L     NULL,MDR,COMM    OLD RESIDUAL                             32316010
039D   006C 0088         1602            L     NULL,YD,COMM     NEW DATA                                 32316020
039E   0865 00CC         1603            ACK0  MDR,D2           NEW RESIDUAL; VECTOR TO STH.D2.          32316030
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BYTE INSTRUCTIONS

```
0000 039F                1605  TLATE   EQU   *                 ENTERED VIA DROM1              * E7 * 32316050
039F   F020 C0FF         1606          NI    MR0,YD,'FF',DR4   EXTRACT BYTE, READ TRTBL ADDRESS      32316060
03A0   0060 0A00         1607          SLL   MR0,MR0           COMPUTE ENTRY ADDRESS                32316070
03A1   0006 0050         1608          A     MAR,MR0,MDR       .                                    32316080
03A2   B06C 0170         1609          L     NULL,NULL,DR2     FETCH ENTRY                          32316090
03A3   006E 0550         1610          EXT   SR,MDR                                                 32316100
03A4   0C08 3820         1611          BT    L,LBR             IF NEGATIVE, USE SR B24:B31; ELSE,   32316110
03A5   0864 0AD0         1612          SLL   LOC,SR,D2         EXECUTE AT TRANSLATION ROUTINE.      32316120

0000 03A6                1614  SCP     EQU   *                 ENTERED VIA DROM1              * E3 * 32316140
03A6   B062 0060         1615          L     MR2,MAR,DR2       MR2 = A(CCW)                         32316150
03A7   006E 0850         1616          LHL   SR,MDR            SR = CCW                             32316160
03A8   0021 E008         1617          NI    MR1,SR,BBIT       TEST BUFFER SWITCH BIT:              32316170
03A9   0031 9002         1618          OI    MR1,MR1,2         GET 2 OR 10                          32316180
03AA   0006 1020         1619          A     MAR,MR1,MR2       READ BUFFER BYTE COUNT               32316190
03AB   B040 1AD0         1620          X     MR0,MR1,SR,SLL+DR2 MR0 BIT 30 = FALSE(CCW FBIT)        32316200
03AC   0063 0550         1621          EXT   MR3,MDR           MR3 = BYTE COUNT                     32316210
03AD   0C10 2290         1622          BT    G,SETCC4          IF POSITIVE, SET CC = 4, EXIT.       32316220
03AE   0085 B001         1623          AI    MDR,MR3,1,JAM     WRITE  INCREMENTED COUNT             32316230
03AF   00EC 0550         1624          EXT   NULL,MDR,JAM      TEST HALFWORD BYTE COUNT:            32316240
                         1625  *                               IF NOW NEGATIVE, CC = 1              32316250
                         1626  *                               IF NOW ZERO,     CC = 0              32316260
                         1627  *                               IF NOW POSITIVE  CC = 2              32316270
03B0   002F 7000         1628          N     FLR,PSW,MR0       TEST IF BUFFER TO BE SWITCHED.       32316280
03B1   0E10 3B40         1629          BF    G,SCP.2           BRANCH: NOT NECESSARY..              32316290
03B2   3066 0020         1630          L     MAR,MR2,DW2       RESTORE CCW.                         32316300
03B3   0045 E008         1631          XI    MDR,SR,BBIT       WITH SWITCHED BUFFER BIT             32316310
                         1632  *                                                                    32316320
03B4   3006 9002         1633  SCP.2   AI    MAR,MR1,2,DW2     SET TO FETCH BUFFER END ADDRESS      32316330
03B5   0006 2060         1634          A     MAR,MR2,MAR       .                                    32316340
03B6   F02C E004         1635          NI    NULL,SR,RWBIT,DR4 FETCH; TEST READ/WRITE               32316350
03B7   0C18 3BB0         1636          BT    G+L,SCP.3         BRANCH: R/W = 1 = WRITE              32316360
03B8   0006 3050         1637          A     MAR,MR3,MDR       R/W = 0 = READ; ADDRESS BYTE         32316370
03B9   0065 0480         1638          EXB   MDR,YD            POSITION DATA BYTE                   32316380
03BA   1E00 0130         1639          B     EXIT,DW1          STORE; GO EXIT.                      32316390
                         1640  *                                                                    32316400
03BB   0006 3050         1641  SCP.3   A     MAR,MR3,MDR       R/W = 1 = WRITE; ADDRESS BYTE        32316410
03BC   B86E 80FF         1642          LI    SR,'FF',DR2+D2    MASK; FETCH DATA BYTE                32316420
                         1643  *                               VECTOR TO LB                         32316430
```

WRITABLE CONTROL STORE INSTRUCTIONS

```
0000 03BD                1645  ECS     EQU   *                ENTERED VIA DROM1                * E9 *  32316450
03BD   006E 8408         1646          LI    SR,H(WCSLO),EXB  WCS START ADDRESS                        32316460
03BE   003E 60A0         1647          O     SR,SR,YDI        DESIRED ENTRY ADDRESS                   32316470

0000 03BF                1649  BDCS    EQU   *                ENTERED VIA DROM1                * F5 *  32316480
03BF   006C 00DE         1650          L     NULL,SR,LLINK    LOAD LINK REGISTER                      32316500
03C0   0E01 00E0         1651          RETN                   TRANSFER TO WCS                         32316510
                         1652  *                              NOTE THAT LOC IS ALREADY INCREMENTED    32316520
                         1653  *                              BY (LENGTH).                            32316530

0000 03C1                1655  RWDCS   EQU   *                (ENTERED VIA DROM1 - *E8*)              32316550
03C1   006F 00A0         1656          L     FLR,YDI          LEGAL SUBFUNCTION ?                     32316560
03C2   0C68 0C20         1657          BT    C+V+L,IIINT      BRANCH: NO.                             32316570
03C3   0060 0082         1658          L     MR0,YD,YDP1      *R0 = WCS START ADRS                    32316580
03C4   0063 8004         1659          LI    MR3,4            CONSTANT                                32316590
03C5   0000 0080         1660          A     MR0,MR0,YD       WCS END ADRS                            32316600
03C6   0061 0A83         1661          SLL   MR1,YD,YDM1      FETCH COUNT                             32316610
03C7   DE40 3C80         1662          BF    C,*+1,IR         EXIT IF ALREADY NEGATIVE.               32316620
03C8   0006 5A10         1663          A     MAR,YS,MR1,SLL   MAR = 4 X COUNT + START                32316630
03C9   0062 0EA2         1664          SRL   MR2,YDI,YDP1     'E80' OPCODE ?                          32316640
03CA   0E18 3D30         1665          BF    G+L,WDCS         BRANCH: YES. ELSE, 'E82' OPCODE.        32316650

0000 03CB                1667  RDCS    EQU   *                .                          *E82*        32316670
03CB   006C 000E         1668          L     NULL,MR0,LLINK                                          32316680
03CC   0065 0050         1669          L     MDR,MDR          CREATE CLOCK STOP       *R01 1/82*      32316690
03CD   0365 0070         1670          L     MDR,CBUS,RDCS    READ FROM WCS                           32316700
03CE   7016 3060         1671          S     MAR,MR3,MAR,DW4  WRITE TO MEMORY, DECREMENT ADDRESS      32316710
03CF   0010 2000         1672          S     MR0,MR2,MR0      DECREMENT WCS POINTER                   32316720
03D0   0018 2080         1673          S     YD,MR2,YD        DECREMENT COUNT                         32316730
03D1   5D40 7350         1674          BT    INT,INTRPT3,ENACLK CHECK QUEUED INTERRUPTS -             32316740
03D2   DE08 3CB0         1675          BF    L,RDCS,IR        CONTINUE IF NONE.                       32316750

0000 03D3                1677  WDCS    EQU   *                .                          *E80*        32316770
03D3   F016 3060         1678          S     MAR,MR3,MAR,DR4  FETCH DATA; DECREMENT ADDRESS          32316780
03D4   006C 000E         1679          L     NULL,MR0,LLINK   SET WCS POINTER                         32316790
03D5   006C 0050         1680          L     NULL,MDR         CREATE CLOCK STOP       *R01 1/82*      32316800
03D6   5D40 7350         1681          BT    INT,INTRPT3,ENACLK CHECK QUEUED INTERRUPTS               32316810
03D7   03EC 0050         1682          L     NULL,MDR,WDCS    WRITE MEMORY DATA TO WCS                32316820
03D8   0010 2005         1683          SDEC  MR0,MR2,MR0      DECREMENT WCS POINTER                   32316830
03D9   0018 2085         1684          SDEC  YD,MR2,YD        DECREMENT COUNT                         32316840
03DA   DE08 3D30         1685          BF    L,WDCS,IR        CONTINUE IF NOT DONE.                   32316850
```

HIGH-SPEED DATA HANDLING INSTRUCTIONS

```
0000 03DB                    1687  PB      EQU   *                 ENTERED VIA DROM1              * 62 * 32316870
03DB   BFC0 0BF0             1688          BF    COMM,IIINTA,DR2   BRANCH: ILLEGAL. FETCH RESIDUAL.      32316880
03DC   006C 0C88             1689          EXH   NULL,YD,COMM      COMMAND FROM YD                      32316890
03DD   006C 0058             1690          L     NULL,MDR,COMM     OLD RESIDUAL FROM MEMORY             32316900
03DE   006C 0088             1691          L     NULL,YD,COMM      NEW DATA FROM YD                     32316910
03DF   0865 00CC             1692          ACK0  MDR,D2            NEW RESIDUAL; VECTOR TO STH.D2.      32316920

0000 03E0                    1694  PBR     EQU   *                 ENTERED VIA DROM1              * 32 * 32316940
03E0   0FC0 0C20             1695          BF    COMM,IIINT        BRANCH: ILLEGAL.                     32316950
03E1   006C 0C88             1696          EXH   NULL,YD,COMM      COMMAND FROM YD                      32316960
03E2   006C 0098             1697          L     NULL,YS,COMM      OLD RESIDUAL FROM YS                 32316970
03E3   006C 0088             1698          L     NULL,YD,COMM      NEW DATA FROM YD                     32316980
03E4   0869 00CC             1699          ACK0  YS,D2             NEW RESIDUAL TO YS; EXIT.            32316990
```

FREE SPACE

```
03E5                    1701    IFP   '400'-*                          32317010
03E5                    1702    DO    '400'-*                          32317020
03E5  0000 0000         1703    DC    FREEWORD                         32317030
03E6  0000 0000         1703    DC    FREEWORD                         32317030
03E7  0000 0000         1703    DC    FREEWORD                         32317030
03E8  0000 0000         1703    DC    FREEWORD                         32317030
03E9  0000 0000         1703    DC    FREEWORD                         32317030
03EA  0000 0000         1703    DC    FREEWORD                         32317030
03EB  0000 0000         1703    DC    FREEWORD                         32317030
03EC  0000 0000         1703    DC    FREEWORD                         32317030
03ED  0000 0000         1703    DC    FREEWORD                         32317030
03EE  0000 0000         1703    DC    FREEWORD                         32317030
03EF  0000 0000         1703    DC    FREEWORD                         32317030
03F0  0000 0000         1703    DC    FREEWORD                         32317030
03F1  0000 0000         1703    DC    FREEWORD                         32317030
03F2  0000 0000         1703    DC    FREEWORD                         32317030
03F3  0000 0000         1703    DC    FREEWORD                         32317030
03F4  0000 0000         1703    DC    FREEWORD                         32317030
03F5  0000 0000         1703    DC    FREEWORD                         32317030
03F6  0000 0000         1703    DC    FREEWORD                         32317030
03F7  0000 0000         1703    DC    FREEWORD                         32317030
03F8  0000 0000         1703    DC    FREEWORD                         32317030
03F9  0000 0000         1703    DC    FREEWORD                         32317030
03FA  0000 0000         1703    DC    FREEWORD                         32317030
03FB  0000 0000         1703    DC    FREEWORD                         32317030
03FC  0000 0000         1703    DC    FREEWORD                         32317030
03FD  0000 0000         1703    DC    FREEWORD                         32317030
03FE  0000 0000         1703    DC    FREEWORD                         32317030
03FF  0000 0000         1703    DC    FREEWORD                         32317030
                        1704    ENDC                                   32317040
```

ASCII CONSOLE SUPPORT

```
0000 0010                1706  INDEV    EQU   '10'              FDX RECEIVER                                    32317060
0000 0011                1707  OUTDEV   EQU   '11'              FDX TRANSMITTER                                 32317070
0000 0021                1708  INCMD    EQU   '21'              DTR, READ                                       32317080
0000 0023                1709  OUTCMD   EQU   '23'              DTR, WRITE                                      32317090
0000 00EE                1710  FMTCMD   EQU   'EE'              ASYNCHRONOUS INTERFACE FORMAT CMD               32317100
                         1711  *                                 FAST CLK, 7 DATA BITS, 2 STOP BITS,          32317110
                         1712  *                                 EVEN PARITY.                                 32317120
0000 003C                1713  PROMPTC  EQU   C'<'              PROMPT CHARACTER                                32317130
0000 003E                1714  SNGLC    EQU   C'>'              SINGLE-STEP CHARACTER                           32317140
                         1715  *                                                                               32317150
                         1716  * MDR:SR = ACCUMULATOR; MR0 = I/O CHARACTER;                                    32317160
                         1717  * YDI = DIGIT COUNTER FOR 'PRNTREG'                                             32317170

0000 0400                1719  BRK      EQU   *                 ENTERED VIA DROM1      * 88 *                   32317190
0400   5E02 0FC0         1720           LINK  MINUSLEN,ENACLK   GET UNINCREMENTED LOC                          32317200

0000 0401                1722  CATN     EQU   *                 ENTERED VIA IVOA OR THRU COLDSTRT               32317220
0401   506C 00BB         1723  CONSER   L     NULL,YSI,ENACLK+RCATN ENSURE XOP UNLOADED FOR RXBX,              32317230
                         1724  *                               ENABLE CLOCKS, RESET CATN.                      32317240
0402   006A 8002         1725           LI    YDI,2             LOAD YDI FOR YDFF FUNCTION                      32317250
0403   5CC0 0780         1726           BT    PPF,PWRDWN,ENACLK BRANCH: POWER GONE.                             32317260
0404   0062 8010         1727           LI    MR2,INDEV                                                         32317270
0405   006D 0024         1728           ADRS  MR2               ADDRESS INPUT DEVICE                            32317280
0406   0062 80EE         1729           LI    MR2,FMTCMD                                                        32317290
0407   006D 0022         1730           OC    MR2               SET BAUD RATE & FORMAT                          32317300
0408   006B 8003         1731           LI    CNTR,3                                                            32317310
0409   0066 8028         1732           LI    MAR,'28'          A(CONSOLE STATUS); DELAY.                       32317320
040A   0062 8021         1733           LI    MR2,INCMD                                                         32317330
040B   006D 0022         1734           OC    MR2               COMMAND READ MODE                               32317340
040C   006B 8003         1735           LI    CNTR,3                                                            32317350
040D   0065 8DFF         1736           LI    MDR,'FF',RRL      SET NEGATIVE FLAG                               32317360
040E   006C 00C1         1737           RD    NULL              DUMMY READ TO SET BSY                           32317370
040F   606C 0179         1738           L     NULL,NULL,PW4+YDFF RESET MVF, SET 'IN CONSER' FLAG                32317380
0410   0CC8 4DC0         1739  CONS.1   BT    PPF+CATN,PPFCHK   BRANCH: POWER FAIL OR HALT/RUN                  32317390
0411   006C 0170         1740           L     NULL,NULL         (FOR DROM COMPATIBILITY)                        32317400
0412   006F 00C2         1741           SS    FLR               GET INPUT DEVICE STATUS                         32317410
0413   0E40 4100         1742           BF    C,CONS.1          WAIT FOR BSY = 1                                32317420
0414   0062 8011         1743           LI    MR2,OUTDEV                                                        32317430
0415   006D 0024         1744           ADRS  MR2               ADDRESS OUTPUT DEVICE                           32317440
0416   0062 8023         1745           LI    MR2,OUTCMD                                                        32317450
0417   006D 0022         1746           OC    MR2               COMMAND WRITE MODE                              32317460
                         1747  * FULL-DUPLEX DEVICE IS ASSUMED.                                                32317470

0418   0E02 4850         1749  ENTRY    LINK  CRLF              DO CARRIAGE RETURN, LINE FEED                   32317490

0419   007E 7000         1751  SHOWPSW  L     SR,PSW            WILL PRINT PSW                                  32317510
041A   0E02 4710         1752           LINK  PRNTREG6          PRINT PSW VALUE                                 32317520

041B   006E 0040         1754  SHOWLOC  L     SR,LOC            WILL PRINT LOC                                  32317540
041C   0E02 4710         1755           LINK  PRNTREG6          PRINT LOC VALUE                                 32317550
                         1756  *                                                                               32317560
041D   0E02 4340         1757  NEXTREQ  LINK  PROMPT            SHOW PROMPT, READ 1ST CHAR                      32317570
```

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```
041E  001C 803C  1759 DECODE  SI    NULL,MRO,PROMPTC     CHARACTER = PROMPTC ?                32317590
041F  0E18 4DB0  1760         BF    G+L,IS.PRMPT         BRANCH: YES.                         32317600
0420  001C 803E  1761         SI    NULL,MRO,SNGLC       CHARACTER = SNGLC ?                  32317610
0421  0E18 4D9B  1762         BF    G+L,IS.SNGLC,RCATN   BRANCH: YES.                         32317620
0422  001C 8040  1763         SI    NULL,MRO,C'@'        CHARACTER = @ ?                      32317630
0423  0E18 4980  1764         BF    G+L,IS.AT            BRANCH: YES.                         32317640
0424  001C 802B  1765         SI    NULL,MRO,C'+'        CHARACTER = + ?                      32317650
0425  0E18 49B0  1766         BF    G+L,IS.PLUS          BRANCH: YES.                         32317660
0426  001C 802D  1767         SI    NULL,MRO,C'-'        CHARACTER = - ?                      32317670
0427  0E18 4A90  1768         BF    G+L,IS.MINUS         BRANCH: YES.                         32317680
0428  001C 8052  1769         SI    NULL,MRO,C'R'        CHARACTER = R ?                      32317690
0429  0E18 4AC0  1770         BF    G+L,IS.R             BRANCH: YES.                         32317700
042A  001C 8046  1771         SI    NULL,MRO,C'F'        CHARACTER = F ?                      32317710
042B  0E18 4B40  1772         BF    G+L,IS.F             BRANCH: YES.                         32317720
042C  001C 8044  1773         SI    NULL,MRO,C'D'        CHARACTER = D ?                      32317730
042D  0E18 4BF0  1774         BF    G+L,IS.D             BRANCH: YES.                         32317740
042E  001C 8050  1775         SI    NULL,MRO,C'P'        CHARACTER = P ?                      32317750
042F  0E18 4CE0  1776         BF    G+L,IS.P             BRANCH: YES.                         32317760
                 1777 *                                                                       32317770
                 1778 *                                                                       32317780
0430  0E02 4850  1779 QUESTN   LINK  CRLF                                                     32317790
0431  0060 803F  1780         LI    MRO,C'?'             QUESTION INPUT DATA VALIDITY         32317800
0432  0E02 48C0  1781         LINK  OUTCHR                                                     32317810
0433  0E00 41D0  1782         B     NEXTREQ              GET NEXT REQUEST                     32317820
                 1783 *                                                                       32317830
                 1784 * DISPLAY PROMPT                                                        32317840
0434  006E 00E0  1785 PROMPT   L     SR,LR                SAVE LINK                            32317850
0435  0E02 485D  1786         LINK  CRLF,RFAULT          RESET MAT,MPE,BOUND FAULTS.          32317860
0436  0060 803C  1787         LI    MRO,PROMPTC          PROMPT CHARACTER                     32317870
0437  0E02 48C0  1788         LINK  OUTCHR                                                     32317880
0438  006C 00DE  1789         L     NULL,SR,LLINK        RESTORE LINK                         32317890
                                                        RETURNS VIA LINK
                 1791 * READ CHARACTER FROM CONSOLE DEVICE                                    32317910
                 1792 INCHR    LI    MR2,INDEV                                              32317920
0439  0062 8010  1793         ADRS  MR2                  ADDRESS INPUT DEVICE                 32317930
043A  006D 0024  1794 IN.2     SSIB  FLR                  SENSE STATUS, PER TEST STRAP         32317940
043B  006F 00CA  1795         BT    CATN+PPF,PPFCHK,RCATN IF BAD-STATUS HANG                   32317950
043C  0CC8 4DCB  1796 *                                  FROM INPUT DEVICE, DEPRESSING THE    32317960
                 1797 *                                  RUN SWITCH CAUSES THE PROCESSOR      32317970
                 1798 *                                  TO ENTER THE RUN MODE AT THE         32317980
                 1799 *                                  ADDRESS SPECIFIED BY LOC.            32317990
                 1800         BT    C,IN.2,CYD&SWA       WAIT FOR INPUT.                      32318000
043D  0C40 43B1  1801         RD    MRO                  INPUT CHARACTER                      32318010
043E  0060 00C1  1802         SS    FLR                                                       32318020
043F  006F 00C2  1803         BF    C,*-1                WAIT FOR BSY = 1                     32318030
0440  0E40 43F0  1804         LI    MR2,OUTDEV                                             32318040
0441  0062 8011  1805         ADRS  MR2                  ADDRESS OUTPUT DEVICE                32318050
0442  006D 0024  1806         SS    FLR                                                       32318060
0443  006F 00C2  1807         BT    C,*-1                WAIT FOR NOT BUSY                    32318070
0444  0C40 4430  1808         WD    MRO                  ECHO RECEIVED CHARACTER              32318080
0445  006D 0001  1809         SS    FLR                                                       32318090
0446  006F 00C2  1810         BT    C,*-1                WAIT FOR NOT BUSY                    32318100
0447  0C40 4460  1811 *                                                                       32318110
```

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```
0448  0020 807F  1812           NI    MR0,MR0,'7F'      MASK TO 7-BITS                                  32318120
0449  001C 8020  1813           SI    NULL,MR0,C' '     BLANK/SPACE ?                                   32318130
044A  0E18 4390  1814           BF    G+L,INCHR         BRANCH: YES; IGNORE.                            32318140
044B  001C 8060  1815           SI    NULL,MR0,'60'     LOWER CASE ASCII ?                              32318150
044C  0C10 44F0  1816           BT    G,IF.DELE         BRANCH: NO.                                     32318160
044D  0063 8020  1817           LI    MR3,'20'                                                          32318170
044E  0010 3000  1818           S     MR0,MR3,MR0       YES. CONVERT TO UPPER CASE.                     32318180
044F  004C 805F  1819  IF.DELE  XI    NULL,MR0,'5F'     BACK ARROW/UNDERLINE/DELETE ?                   32318190
0450  0E18 4530  1820           BF    G+L,IS.DELE       BRANCH: YES.                                    32318200
0451  004C 8008  1821           XI    NULL,MR0,'08'     BACKSPACE ?                                     32318210
0452  0C19 00E0  1822           RETNT G+L               RETURN IF NOT (NORMAL EXIT).                    32318220
0000 0453        1823  IS.DELE  EQU   *                 BACKSPACE, CTRL-H, BACKARROW, DELETE            32318230
                                                                                                         32318240
0453  006B 8004  1824           LI    CNTR,4                                                            32318250
0454  0065 0E5C  1825           SRL   MDR,MDR,DWSHFT    SHIFT NUMBER IN (MDR:SR) RIGHT 4                32318260
0455  0E00 4390  1826           B     INCHR             TRY AGAIN
                                                                                                         32318280
0456  0061 00E0  1828  TRYMOD   L     MR1,LR            SAVE LINK                                       32318290
0457  0E02 4340  1829           LINK  PROMPT            SHOW PROMPT, READ 1ST CHAR                      32318300
0458  001C 803D  1830           SI    NULL,MR0,C'='     EQUAL SIGN ?                                    32318310
0459  0C18 41E0  1831           BT    G+L,DECODE        BRANCH: NO.                                     32318320
045A  006C 001E  1832           L     NULL,MR1,LLINK    RESTORE LINK                                    32318330
                 1833  *                                RETURNS VIA LINK
                                                                                                         32318350
                 1835  * ACCUMULATE HEXADECIMAL INPUT                                                   32318360
                 1836  * USES CHAINED (MDR:SR) AS 64-BIT ACCUMULATOR                                    32318370
045B  006E 0170  1837  ACCUM   L     SR,NULL           CLEAR ACCUMULATOR                               32318380
045C  0065 0170  1838           L     MDR,NULL                                                          32318390
045D  0061 00E0  1839           L     MR1,LR            SAVE LINK                                       32318400
045E  0E02 4390  1840  ACCUM1  LINK  INCHR                                                             32318410
045F  006C 001E  1841           L     NULL,MR1,LLINK    RESTORE LINK                                    32318420
0460  004C 800D  1842           XI    NULL,MR0,'0D'     CARRIAGE RETURN ENTERED ?                       32318430
0461  0E19 00E0  1843           RETNF G+L               BRANCH: YES, RETURN TO CALLER.                  32318440
0462  0063 8030  1844           LI    MR3,'30'                                                          32318450
0463  0010 3000  1845           S     MR0,MR3,MR0       KEY LESS THAN A ZERO ?                          32318460
0464  0C40 4300  1846           BT    C,QUESTN          BRANCH: NOT HEXADECIMAL INPUT                   32318470
0465  001C 8009  1847           SI    NULL,MR0,'09'     0 - 9 ?                                         32318480
0466  0E40 46D0  1848           BF    C,HEX             BRANCH: YES.                                    32318490
0467  0063 8007  1849           LI    MR3,'07'                                                          32318500
0468  0010 3000  1850           S     MR0,MR3,MR0       A - F ?                                         32318510
0469  001C 8010  1851           SI    NULL,MR0,'10'                                                     32318520
046A  0E10 4300  1852           BF    G,QUESTN          BRANCH: NO.                                     32318530
046B  001C 8009  1853           SI    NULL,MR0,'09'     CHECK FURTHER -                                 32318540
046C  0E40 4300  1854           BF    C,QUESTN          SPECIAL CHAR NOT RECOGNIZED.                    32318550
046D  005B 8004  1855  HEX      LI    CNTR,4                                                            32318560
046E  0065 0A5C  1856           SLL   MDR,MDR,DWSHFT    SHIFT ACCUMULATOR LEFT 4 BITS                   32318570
046F  003E 6000  1857           O     SR,SR,MR0         APPEND NEW DIGIT                                32318580
0470  0E00 45E0  1858           B     ACCUM1            TRY NEXT DIGIT
```

ASCII CONSOLE SUPPORT

```
                                1860  * PRINT REGISTER CONTENTS                                                  32318600
                                1861  PRNTREG6 LI    YDI,6                                                       32318610
0471  006A 8006                 1862           B     PRNTREG                                                     32318620
0472  0E00 4740                 1863  PRNTREG8 LI    YDI,8                                                       32318630
0473  006A 8008                 1864  PRNTREG  L     MR1,LR          SAVE LINK                                   32318640
0474  0061 00E0                 1865  PREG.0   L     MR0,SB,YDM1     DECREMENT DIGIT COUNT                       32318650
0475  0060 00D3                 1866           BT    YDC,PREG.2      BRANCH: ALL DIGITS PRINTED.                 32318660
0476  0D88 4810                 1867           SLL   MR2,YDI         SET UP COUNTER,                             32318670
0477  0062 0AA0                 1868           SLL   CNTR,MR2        SHIFT HIGH-ORDER DIGIT                      32318680
0478  006B 0A20                 1869           SRL   MR0,MR0         TO MR0 B28:31.                              32318690
0479  0060 0E00                 1870  *                               (NO SHIFT IF CNTR = 0)                      32318700
                                1871  PREG.05  NI    MR0,MR0,'0F'    EXTRACT HEXADECIMAL DIGIT;                  32318710
047A  0020 800F                 1872           AI    MR0,MR0,'30'    CONVERT TO ASCII.                           32318720
047B  0000 8030                 1873           SI    NULL,MR0,'3A'   # 0-9 ?                                     32318730
047C  001C 803A                 1874           BT    G,PREG.1        BRANCH: YES.                                32318740
047D  0C10 47F0                 1875           AI    MR0,MR0,'07'    # A-F.                                     32318750
047E  0000 8007                 1876  PREG.1   LINK  OUTCHR                                                     32318760
047F  0E02 48C0                 1877           B     PREG.0          CONTINUE                                    32318770
0480  0E00 4750                 1878  *                                                                         32318780
                                1879  PREG.2   LI    MR0,C' '                                                    32318790
0481  0060 8020                 1880           LINK  OUTCHR          OUTPUT A SPACE                              32318800
0482  0E02 48C0                 1881           L     NULL,MR1,LLINK  RESTORE LINK                               32318810
0483  006C 001E                 1882           RETN                  RETURN                                      32318820
0484  0E01 00E0

                                1884  * PERFORM CARRIAGE RETURN/LINE FEED                                       32318840
                                1885  CRLF     LI    MR0,'0A'        LINE FEED                                   32318850
0485  0060 800A                 1886           L     MDR,LR          SAVE LINK                                   32318860
0486  0065 00E0                 1887           LINK  OUTCHR                                                      32318870
0487  0E02 48C0                 1888           LI    MR0,'0D'        CARRIAGE RETURN                             32318880
0488  0060 800D                 1889           LINK  OUTCHR                                                      32318890
0489  0E02 48C0                 1890           L     NULL,MDR,LLINK  RESTORE LINK                                32318900
048A  006C 005E                 1891           RETN                  RETURN                                      32318910
048B  0E01 00E0

                                1893  * OUTPUT CHARACTER TO CONSOLE                                             32318930
                                1894  OUTCHR   LI    MR2,OUTDEV                                                  32318940
048C  0062 8011                 1895           ADRS  MR2             ADDRESS OUTPUT DEVICE                       32318950
048D  006D 0024                 1896  OUT.1    SS    FLR                                                       32318960
048E  006F 00C2                 1897           BT    CATN+PPF,PPFCHK MUST RETRY IF BAD STATUS                  32318970
048F  0CC8 4DC0                 1898           BT    C,OUT.1         WAIT FOR NOT BUSY                           32318980
0490  0C40 48E0                 1899           WD    MR0             OUTPUT CHARACTER                            32318990
0491  006D 0001                 1900           SS    FLR                                                       32319000
0492  006F 00C2                 1901           BT    C,*-1           WAIT FOR NOT BUSY                           32319010
0493  0C40 4920                 1902           WD    NULL            OUTPUT NULL                                 32319020
0494  006D 0171                 1903           SS    FLR                                                       32319030
0495  006F 00C2                 1904           BT    C,*-1           WAIT FOR NOT BUSY                           32319040
0496  0C40 4950                 1905           RETN                  RETURN TO CALLER                            32319050
0497  0E01 00E0

                                1907  * MODIFY LOCATION COUNTER                                                 32319070
                                1908  IS.AT    LINK  ACCUM           GO GET DATA                                 32319080
0498  0E02 45B0                 1909           L     LOC,SR          UPDATE LOC                                  32319090
0499  0064 00D0                 1910           B     IS.PLO          ENTER COMMON ROUTINE.                       32319100
049A  0E00 49D0
```

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```
049B  006E 0040
049C  0004 E002
049D  5E02 485D
049E  006E 0040
049F  0E02 4710
04A0  0066 0040
04A1  B06A 8004
04A2  006E 0850
04A3  5EB2 4740
04A4  0EB2 4560
04A5  0065 00D0
04A6  3EB0 49B0
04A7  5EA0 401D
04A8  AE00 401D

04A9  006E 8002
04AA  0014 6040
04AB  0E00 49D0

04AC  0E02 45B0
04AD  006A 00DF
04AE  006E 0080
04AF  0E02 4850
04B0  0E02 4730
04B1  0E02 4560
04B2  0069 00D0
04B3  0E00 4B10

04B4  0F90 4300
04B5  0E02 45B0
04B6  006A 0ED0
04B7  006A 0AAF
04B8  011E 0070
04B9  0E02 4850
04BA  0E02 4730
04BB  0E02 4560
04BC  006A 00B0
04BD  012C 00DA
04BE  0E00 4BB0
```

```
1912  * PROCEED TO NEXT CELL                                          32319120
1913  IS.PLUS  L      SR,LOC                  COPY LOC                32319130
1914           AI     LOC,SR,2                INCREMENT BY 2          32319140
1915  IS.PL0   LINK   CRLF,RFAULT+ENACLK                             32319150
1916           L      SR,LOC                  MOVE LOC TO PRINT REGISTER 32319160
1917           LINK   PRNTREG6                DISPLAY UPDATED LOC     32319170
1918           L      MAR,LOC                 READ CONTENTS OF CURRENT CELL 32319180
1919           LI     YDI,4,DR2               SET DIGIT COUNT = 4     32319190
1920           LHI    SR,MDR                  COPY TO ACCUMULATOR     32319200
1921           LINKF  MAT+MPE,PRNTREG,ENACLK DISPLAY MEMORY HALFWORD  32319210
1922           LINKF  MAT+MPE,TRYMOD          SEE IF USER WANTS CHANGE 32319220
1923           L      MDR,SR                  STORE IN MEMORY         32319230
1924           BF     MAT+MPE,IS.PLUS,DW2 OPEN + CELL, DISPLAY IF NO ERROR 32319240
1925           BF     MAT,CONSER,RFAULT+ENACLK 'ABORT' CONSER IF MPE   32319250
1926           B      CONSER,PR2+RFAULT       OR IF MAT, RESET MAT ERROR. 32319260

1928  * PROCEED TO PREVIOUS CELL                                      32319280
1929  IS.MINUS LI     SR,2                    COPY LOC                32319290
1930           S      LOC,SR,LOC              DECREMENT BY 2          32319300
1931           B      IS.PL0                  ENTER COMMON ROUTINE.   32319310

1933  * DISPLAY GENERAL REGISTER                                      32319330
1934  IS.R     LINK   ACCUM                   GET REGISTER NUMBER     32319340
1935           L      YDI,SR,LYSI             SELECT REGISTER         32319350
1936           L      SR,YD                   COPY CONTENTS TO PRINT REGISTER 32319360
1937           LINK   CRLF                                            32319370
1938           LINK   PRNTREG8                DISPLAY REGISTER        32319380
1939  IS.R0    LINK   TRYMOD                  SEE IF USER WANTS CHANGE 32319390
1940           L      YS,SR                   LOAD WITH NEW DATA      32319400
1941           B      IS.R0                   GET NEXT REQUEST.       32319410

1943  * DISPLAY SPFP REGISTER                                         32319430
1944  IS.F     BF     FPP,QUESTN              BRANCH: NO FLOATING POINT. 32319440
1945           LINK   ACCUM                   GET REGISTER NUMBER     32319450
1946           SRL    YDI,SR                  FORCE REGISTER SELECT EVEN 32319460
1947           SLL    YDI,YDI,LYSI            .                       32319470
1948           RRE    SR                      AND READ IT.            32319480
1949           LINK   CRLF                                            32319490
1950           LINK   PRNTREG8                SHOW REGISTER CONTENTS  32319500
1951  IS.F00   LINK   TRYMOD                  SEE IF USER WANTS CHANGE 32319510
1952           L      YDI,YSI                 RESELECT REGISTER       32319520
1953           LE     YD,SR,UNNLD             LOAD REGISTER, UNNORMALIZED 32319530
1954           B      IS.F00                                          32319540
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```
                                1956  * DISPLAY DPFP REGISTER                                                  32319560
04BF   0F90 4300                1957  IS.D      BF    FPP,QUESTN      BRANCH: NO FLOATING POINT.             32319570
04C0   0E02 45B0                1958            LINK  ACCUM           GET REGISTER NUMBER                    32319580
04C1   006A 0ED0                1959            SRL   YDI,SR          FORCE REGISTER SELECT EVEN             32319590
04C2   006A 0AAF                1960            SLL   YDI,YDI,LYSI    .                                      32319600
04C3   021E 0070                1961            RRD   SR              READ HIGH HALF                         32319610
04C4   0E02 4852                1962            LINK  CRLF,YDP1                                              32319620
04C5   0215 0070                1963            RRD   MDR             SAVE LOW HALF IN MDR                   32319630
04C6   0E02 4730                1964            LINK  PRNTREG8        SHOW HIGH HALF                         32319640
04C7   006E 0050                1965            L     SR,MDR          RETRIEVE LOW HALF                      32319650
04C8   0E02 4730                1966            LINK  PRNTREG8        SHOW LOW HALF                          32319660
04C9   0E02 4560                1967  IS.D00    LINK  TRYMOD          SEE IF USER WANTS CHANGE               32319670
04CA   006A 00B0                1968            L     YDI,YSI         RESELECT REGISTER                      32319680
04CB   020C 0050                1969            LW    YD,MDR          LOAD HIGH                              32319690
04CC   022C 00DA                1970            LD    YD,SR,UNNLD     LOAD LOW HALF, UNNORMALIZED            32319700
04CD   0E00 4C90                1971            B     IS.D00          GET NEXT REQUEST.                      32319710

                                1973  * MODIFY PSW                                                            32319730
04CE   0E02 4390                1974  IS.P      LINK  INCHR           GET NEXT CHARACTER                     32319740
04CF   004C 800D                1975            XI    NULL,MRO,'0D'   CARRIAGE RETURN ?                     32319750
04D0   0C18 4300                1976            BT    G+L,QUESTN      BRANCH: NO.                            32319760
04D1   0E02 4850                1977            LINK  CRLF                                                   32319770
04D2   007E 7000                1978            L     SR,PSW                                                 32319780
04D3   0E02 4710                1979            LINK  PRNTREG6        DISPLAY PSW                            32319790
04D4   006E 0040                1980            L     SR,LOC                                                 32319800
04D5   0E02 4710                1981            LINK  PRNTREG6        DISPLAY LOC                            32319810
04D6   0E02 4560                1982            LINK  TRYMOD          SEE IF USER WANTS CHANGE               32319820
04D7   00E7 00DC                1983            L     PSW,SR,JAM      UPDATE PSW                             32319830
04D8   0E00 4180                1984            B     ENTRY           SHOW NEW PSW, AND LOC.                 32319840

                                1986  * SINGLE-STEP ONE INSTRUCTION                                           32319860
04D9   006A 8006                1987  IS.SNGLC  LI    YDI,6           SET FOR YDFF FUNCTION                  32319870
04DA   0E00 4DC9                1988            B     PPFCHK,YDFF     SET SINGLE-STEP FLIP-FLOP              32319880

                                1990  * ENTER RUN MODE                                                        32319900
                                1991  IS.PRMPT  EQU   *                                                     32319910
0000 04DB                       1992            LINK  CRLF,RCATN      KICK DOWN CURSOR                       32319920
04DB   0E02 485B                1993  PPFCHK    EQU   *                                                     32319930
0000 04DC                       1994            BT    PPF,PPF,RFAULT+ENACLK BRANCH: POWER GONE.             32319940
04DC   5CC0 078D                1995            L     NULL,ZMAR       ENSURE ZMAR UNLOADED IF FAULT          32319950
04DD   006C 0060                1996            LI    MAR,'28'        A(CONSOLE STATUS)                      32319960
04DE   0066 8028                1997            NI    MRO,PSW,'80',EXB  RESET WAIT BIT                       32319970
04DF   0020 F480                1998            X     PSW,PSW,MRO,JAM .                                      32319980
04E0   00C7 7000                1999            L     MDR,NULL        SET STATUS WORD TO ZERO                32319990
04E1   0065 0170                2000            B     EXIT,PW4        OPEN THE GATES OF HELL.                32320000
04E2   6E00 0130
```

PRIVILEGED SYSTEM FUNCTION (PSF)

```
0000 04E3                2002  PSF     EQU   *                    ENTERED VIA DROM1        * DF *     32320020
04E3   0063 80E0         2003          LI    MR3,PSFTAB           BASE ADDRESS OF BRANCH TABLE        32320030
04E4   0033 30A0         2004          O     MR3,MR3,YDI          ADD CODE                            32320040
04E5   006F 003E         2005          L     FLR,MR3,LLINK        BRANCH ADDRESS; TEST SUBFUNCTION:   32320050
04E6   0E41 00E1         2006          RETNF C,CYD&SWA            BRANCH: CODES 0-7 OK.               32320060
04E7   0C38 0C20         2007          BT    V+G+L,IIINT          ILLEGAL SUBFUNCTION.                32320070

04E8   006A 8002         2009  RMVF    LI    YDI,2                CODE 8 - RESET MEM VOLTAGE FAILURE  32320090
                         2010  *                                  FALL THROUGH LSTD1 FOR YDFF FUNCTION.32320100

04E9   086C 0059         2012  LSTD1   L     NULL,MDR,YDFF+D2     LOAD DATA FOR LSSTD, LPSTD FUNCTION 32320120
                         2013  *                                  VECTOR TO EXIT.                     32320130

0000 04EA                2015  REL     EQU   *                    CODE 0 - READ ERROR LOGGER          32320150
04EA   0036 D002         2016          OI    MAR,YS,'02'          'ERROR LOGGER ADDRESS' ON HW BOUND  32320160
04EB   C06A 00B0         2017          L     YDI,YSI,REL          READ ERROR LOGGER                   32320170
04EC   00EC 0552         2018          EXT   NULL,MDR,JAM+YDP1    STATUS TEST IS ON MDR BIT 16        32320180
04ED   D068 0850         2019          LHL   YD,MDR,IR            R2+1 = LOGGER DATA; EXIT, CC SET.   32320190

0000 04EE                2021  STPS    EQU   *                    CODE 3 - SAVE PROCESS STATE         32320210
04EE   0073 7003         2022          L     MR3,PSW,YDM1         COPY PSW, POINT R14.                32320220
04EF   0062 0080         2023          L     MR2,YD               COPY PROCESS PSW FROM R14           32320230
04F0   0065 0082         2024          L     MDR,YD,YDP1          STORE PROCESS PSW, POINT R15        32320240
04F1   7040 7054         2025          X     MR0,PSW,MDR,DW4+I4   WILL SELECT USER REGISTER SET        32320250
04F2   0065 0082         2026          L     MDR,YD,YDP1          STORE PROCESS-OLD-LOC, POINT R0     32320260
04F3   7020 80F0         2027          NI    MR0,MR0,'F0',DW4     ONLY THESE BITS CHANGE -            32320270
04F4   0047 7004         2028          X     PSW,PSW,MR0,I4       SELECT USER REGISTER SET.           32320280
04F5   0E02 3684         2029          LINK  STM.ENT,I4           STORE GENERAL REGISTER SET @+12     32320290
04F6   00E7 0030         2030          L     PSW,MR3,JAM          RESTORE ENTRY PSW                   32320300
04F7   002C AC02         2031          NI    NULL,MR2,'02',EXH    INTERRUPTIBLE STATE EXISTS ?        32320310
04F8   0C1A 51D1         2032          LINKT G+L,STM71,CYD&SWA    BRANCH: YES.                        32320320
04F9   002C AC04         2033          NI    NULL,MR2,'04',EXH    FLOATING POINT LEGAL ?              32320330
04FA   DE18 4FB0         2034          BF    G+L,STPS1,IR         BRANCH: YES. ELSE, EXIT.            32320340
04FB   DD92 5771         2035  STPS1   LINKT FPP,STME.ENT,CYD&SWA+IR BRANCH: FPP EQUIPPED.           32320350
04FC   0E00 58F1         2036          B     STMD,CYD&SWA         STORE DPFP REGISTER SET             32320360


0000 04FD                2038  LDPS    EQU   *                    CODE 4 - LOAD PROCESS STATE         32320380
04FD   0063 0054         2039          L     MR3,MDR,I4           SAVE COPY OF PROCESS PSW            32320390
04FE   0040 7034         2040          X     MR0,PSW,MR3,I4       SELECT USER REGISTER SET, ONLY:     32320400
04FF   0020 80F0         2041          NI    MR0,MR0,'F0'         EXTRACT REG SELECT FIELD            32320410
0500   0047 7000         2042          X     PSW,PSW,MR0          SELECT PROCESS REGISTER SET         32320420
0501   FE02 3274         2043          LINK  LM.ENT,DR4+I4        LOAD GENERAL REGISTERS @+12         32320430
0502   002C BC02         2044          NI    NULL,MR3,'02',EXH    INTERRUPTIBLE STATE EXISTS ?        32320440
0503   0E18 5050         2045          BF    G+L,LDPS0            BRANCH: NO.                         32320450
0504   FE02 5194         2046          LINK  LM71,DR4+I4          LOAD SCRATCHPADS                    32320460
0505   002C BC04         2047  LDPS0   NI    NULL,MR3,'04',EXH    FLOATING POINT LEGAL ?              32320470
0506   0C18 5090         2048          BT    G+L,LDPS1            BRANCH: NO.                         32320480
0507   0D92 57D1         2049          LINKT FPP,LME.ENT,CYD&SWA  RESTORE SPFP REGISTER SET           32320490
0508   0D92 59E1         2050          LINKT FPP,LMD.ENT,CYD&SWA  RESTORE DPFP REGISTER SET           32320500
0509   0006 E004         2051  LDPS1   AI    MAR,SR,4             POINT TO NEW LOC @ +4               32320510
050A   F06E 0034         2052          L     SR,MR3,DR4+I4        SR = NEW PSW; FETCH LOC, POINT +8   32320520
050B   F060 0050         2053          L     MR0,MDR,DR4          MR0 = NEW LOC; FETCH PSTD           32320530
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PRIVILEGED SYSTEM FUNCTION (PSF)

```
050C   006C 0050          2054          L     NULL,MDR              ENSURE DATA READY                      32320540
050D   002C B404          2055          NI    NULL,MR3,'04',EXB     NEW PSW B21 SET ?                      32320550
050E   0E18 5101          2056          BF    G+L,LDPS3,CYD&SWA     BRANCH: NO. DON'T LOAD PSTD.           32320560
050F   006C 0059          2057          L     NULL,MDR,YDFF         LOAD PSTD (YDI=0)                      32320570
0510   0064 0000          2058  LDPS3   L     LOC,MR0               LOAD NEW LOC                           32320580
0511   DEB0 1260          2059          BF    MAT+MPE,QTEST,IR      BRANCH: WHOLE LOAD SUCCESSFUL          32320590
                          2060  *                                   GO LOAD PSW, CC, TEST QUEUE SERVICE.   32320600
                          2061  *                                   ELSE, TAKE QUEUED FAULT INTERRUPT.     32320610

0000 0512                 2063  ISSV    EQU   *                     CODE 5 - SAVE INTERRUPTIBLE STATE      32320630
0512   0465 0082          2064          L     MDR,ARSYD,YDP1        DATA TO STORE                          32320640
0513   006B 800F          2065          LI    CNTR,15               STEPS REQUIRED                         32320650
0514   7465 0082          2066          L     MDR,ARSYD,YDP1+DW4    STORE; READY NEXT (AUTO-I4)            32320660
0515   7E00 0130          2067          B     EXIT,DW4              STORE ARS R15, EXIT.                   32320670

0000 0516                 2069  ISRST   EQU   *                     CODE 6 - RESTORE INTERRUPTIBLE STATE   32320690
0516   006B 800F          2070          LI    CNTR,15               STEPS REQ'D (MEMORY READING)           32320700
0517   F468 0052          2071          L     ARSYD,MDR,YDP1+DR4    LOAD DATA, FETCH NEXT (AUTO-I4)        32320710
0518   D468 0050          2072          L     ARSYD,MDR,IR          LOAD ARS R15, EXIT.                    32320720

0000 0519                 2074  LM71    EQU   *                     LOADS 16 SCRATCHPAD REGISTERS          32320740
0519   006B 800F          2075          LI    CNTR,15               STEPS REQ'D (MEMORY READING)           32320750
051A   F468 0052          2076          L     ARSYD,MDR,YDP1+DR4    LOAD DATA, FETCH NEXT (AUTO-I4)        32320760
051B   0468 0052          2077          L     ARSYD,MDR,YDP1        LOAD ARS R15,                          32320770
051C   0E01 00E0          2078          RETN                        RETURN.                                32320780

0000 051D                 2080  STM71   EQU   *                     STORES 16 SCRATCHPAD REGISTERS         32320800
051D   0465 0082          2081          L     MDR,ARSYD,YDP1        DATA TO STORE                          32320810
051E   006B 800F          2082          LI    CNTR,15               STEPS REQUIRED                         32320820
051F   7465 0082          2083          L     MDR,ARSYD,DW4+YDP1    STORE, READY NEXT (AUTO-I4)            32320830
0520   7E01 00E4          2084          RETN  DW4+I4                STORE ARS R15, RETURN.                 32320840
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FLOATING POINT INSTRUCTIONS

```
0000 0521                2086  LER       EQU   *                ENTERED VIA DROM1              * 28 * 32320860
0521   092C 0090          2087            LE    YD,YS,D2         LOAD, VECTOR TO EEXIT                 32320870

0000 0522                2089  CER       EQU   *                ENTERED VIA DROM1              * 29 * 32320890
0522   013C 0090          2090            CER   YD,YS            COMPARE                               32320900
0523   D18F 0070          2091            RCC   FLR,IR+JAM       SET CC, EXIT (CAN'T INTERRUPT)        32320910

0000 0524                2093  AER       EQU   *                ENTERED VIA DROM1              * 2A * 32320930
0524   094C 0090          2094            AER   YD,YS,D2         ADD, VECTOR TO EEXIT                  32320940

0000 0525                2096  SER       EQU   *                ENTERED VIA DROM1              * 2B * 32320960
0525   095C 0090          2097            SER   YD,YS,D2         SUBTRACT, VECTOR TO EEXIT             32320970

0000 0526                2099  MER       EQU   *                ENTERED VIA DROM1              * 2C * 32320990
0526   096C 0090          2100            MER   YD,YS,D2         MULTIPLY, VECTOR TO EEXIT             32321000

0000 0527                2102  DER       EQU   *                ENTERED VIA DROM1              * 2D * 32321020
0527   097C 0090          2103            DER   YD,YS,D2         DIVIDE, VECTOR TO EEXIT               32321030


0000 0528                2105  FXR       EQU   *                ENTERED VIA DROM1              * 2E * 32321050
0528   0060 00A0          2106            L     MR0,YDI          SAVE YDI                              32321060
0529   006A 00B0          2107            L     YDI,YSI                                                32321070
052A   006E 000F          2108            L     SR,MR0,LYSI      AND MAKE SWAP COMPLETE -              32321080
                          2109  *                                PUT VERY SMALL NUMBER IN SR           32321090
052B   0199 0070          2110            RRE   YS,JAM           GET VALUE, SET CC G,L                 32321100
052C   0061 84FF          2111  FXR.010   LI    MR1,'FF',EXB     MASK                                  32321110
052D   0023 1C90          2112            N     MR3,MR1,YS,EXH   MR3 = SIGN&EXPONENT, FORM 0000XX00   32321120
052E   0049 5C30          2113            X     YS,YS,MR3,EXH    YS = FRACTION ONLY.                   32321130
052F   0023 B47F          2114            NI    MR3,MR3,'7F',EXB MR3 NOW = EXPONENT, FORM 0000XX00     32321140
0530   0061 8482          2115            LI    MR1,'82',EXB     TEST EQUALIZATION:                    32321150
0531   0012 1A30          2116            S     MR2,MR1,MR3,SLL  MR2 = EXPONENT DELTA.                 32321160
0532   0C40 5420          2117            BT    C,UNDRFLO        BRANCH: EXPONENT UNDERFLOW            32321170
0533   0061 800A          2118            LI    MR1,10           TEST FOR SHIFT:                       32321180
0534   0012 1420          2119            S     MR2,MR1,MR2,EXB  MR2 = DIGITS TO SHIFT * 2;           32321190
0535   0C08 5470          2120            BT    L,RIGHT          BRANCH: EXPONENT BETWEEN 41,46.       32321200
0000 0536                2121  LEFT      EQU   *                                                      32321210
0536   001C A004          2122            SI    NULL,MR2,4       TO SHIFT OFF LEFT OF REGISTER ?       32321220
0537   0C40 5430          2123            BT    C,OVERFLO        BRANCH: YES (49100000 OR GREATER)     32321230
0538   006B 0A20          2124            SLL   CNTR,MR2         FOUR SHIFTS PER HEX DIGIT             32321240
0539   0069 0A9C          2125            SLL   YS,YS,DWSHFT     SHIFT (YS:SR) BY HEX DIGITS           32321250
053A   003F 7990          2126  PUTAWAY   O     FLR,PSW,YS,RLL   POSITIVE, EXPECT POSITIVE ?           32321260
053B   DC08 53C0          2127            BT    L,FXR.25,IR      BRANCH: NO; MUST ADJUST.              32321270
053C   006C 0A90          2128  FXR.25    SLL   NULL,YS          RESULT SHIFTED INTO BIT 0 ?           32321280
053D   0E40 5410          2129            BF    C,FXR.30         BRANCH: NO - JUST NEEDS NEGATION.     32321290
053E   0C18 5430          2130            BT    G+L,OVERFLO      BRANCH: CANNOT REPRESENT COMPLEMENT   32321300
053F   007F 7000          2131            L     FLR,PSW          WAS SUPPOSED TO BE NEGATIVE ?         32321310
0540   0E08 5430          2132            BF    L,OVERFLO        BRANCH: NO. POSITIVE OVERFLOW.        32321320
0541   D019 D000          2133  FXR.30    SI    YS,YS,0,IR       2'S COMPLEMENT, EXIT.                 32321330
                          2134  *                                                                      32321340
0542   D0E9 0170          2135  UNDRFLO   L     YS,NULL,IR+JAM   EXIT, R1 = CC = 0.                   32321350
                          2136  *                                                                      32321360
0543   0020 F001          2137  OVERFLO   NI    MR0,PSW,'01'     CAPTURE 'L' FLAG FROM CC              32321370
                          2138  *                                +:00000000   -:00000001              32321380
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FLOATING POINT INSTRUCTIONS

```
0544   0040 8D03          2139           XI    MR0,MR0,'03',RRL     +:80000001   -:80000000                32321390
0545   0019 8000          2140           SI    YS,MR0,0             +:7FFFFFFF   -:80000000                32321400
0546   D0BF F004          2141           OI    FLR,PSW,'04',IR+JAM  SET CC OVERFLOW (V) FLAG, EXIT.         32321410
                          2142   *                                                                         32321420
0547   0012 A000          2143   RIGHT   SI    MR2,MR2,C            GET POSITIVE SHIFT COUNT                 32321430
0548   006B 0A20          2144           SLL   CNTR,MR2                                                    32321440
0549   0069 0E90          2145           SRL   YS,YS                SHIFT BY HEX DIGITS                      32321450
054A   007F 7000          2146           L     FLR,PSW              SHOULD BE NEGATIVE ?                     32321460
054B   DC08 5410          2147           BT    L,FXR.30,IR          BRANCH: YES. ELSE, EXIT.                 32321470

0000 054C                 2149   FLR     EQU   *                    ENTERED VIA DROM1              * 2F *    32321490
0000 054C                 2150   FLDR    EQU   *                    ENTERED VIA DROM1              * 3F *    32321500
054C   0020 ED01          2151           NI    MR0,SR,'01',RRL      CAPTURE R2 SIGN BIT                      32321510
054D   0061 844E          2152           LI    MR1,'4E',EXB         FOR POSITIVE CONSTANT                    32321520
054E   0045 0C10          2153           X     MDR,MR0,MR1,EXH      GET '4E...' OR 'CE...'                   32321530
054F   0E08 5510          2154           BF    L,FLR1               BRANCH: NOT NEGATIVE                     32321540
0550   001E E000          2155           SI    SR,SR,0              MAKE (SR) POSITIVE                       32321550
0551   0A0C 0050          2156   FLR1    LW    YD,MDR,D2            LOAD +/- 4E000000,                       32321560
                          2157   *                                  VECTOR TO FLR.020, FLDR.020.             32321570

                                                                                                            32321590
0552   012C 00D0          2159   FLR.020 LE    YD,SR                LOAD (CAN'T INTERRUPT)                   32321600
0553   D18F 0070          2160           RCC   FLR,IR+JAM           CC = 0,1, OR 2. EXIT.                    32321610
                          2161   *                                                                         32321620
0554   022C 00D0          2162   FLDR.020 LD   YD,SR                LOAD (CAN'T INTERRUPT)                   32321630
0555   D18F 0070          2163           RCC   FLR,IR+JAM           CC = 0,1, OR 2. EXIT.

0000 0556                 2165   LDR     EQU   *                    ENTERED VIA DROM1              * 38 *    32321650
0556   0A2C 0090          2166           LD    YD,YS,D2             LOAD, VECTOR TO EEXIT                    32321660

0000 0557                 2168   CDR     EQU   *                    ENTERED VIA DROM1              * 39 *    32321680
0557   023C 0090          2169           CDR   YD,YS                COMPARE                                  32321690
0558   D18F 0070          2170           RCC   FLR,IR+JAM           SET CC, EXIT (CAN'T INTERRUPT)           32321700

0000 0559                 2172   ADR     EQU   *                    ENTERED VIA DROM1              * 3A *    32321720
0559   0A4C 0090          2173           ADR   YD,YS,D2              ADD, VECTOR TO EEXIT                     32321730

0000 055A                 2175   SDR     EQU   *                    ENTERED VIA DROM1              * 3B *    32321750
055A   0A5C 0090          2176           SDR   YD,YS,D2              SUBTRACT, VECTOR TO EEXIT                32321760

0000 055B                 2178   MDR     EQU   *                    ENTERED VIA DROM1              * 3C *    32321780
055B   0A6C 0090          2179           MDR   YD,YS,D2              MULTIPLY, VECTOR TO EEXIT                32321790

0000 055C                 2181   DDR     EQU   *                    ENTERED VIA DROM1              * 3D *    32321810
055C   0A7C 0090          2182           DDR   YD,YS,D2              DIVIDE, VECTOR TO EEXIT.                 32321820

0000 055D                 2184   FXDR    EQU   *                    ENTERED VIA DROM1              * 3E *    32321840
055D   0060 00A0          2185           L     MR0,YDI              SAVE YDI                                 32321850
055E   006A 00B0          2186           L     YDI,YSI                                                       32321860
055F   006C 000F          2187           L     NULL,MR0,LYSI        AND COMPLETE SWAP.                       32321870
0560   0299 0070          2188           RRD   YS,JAM               GET HIGH HALF, SET CC G,L                32321880
0561   DC18 5622          2189           BT    G+L,FXDR1,YDP1+IR    EXIT IF TRUE ZERO HIGH HALF              32321890
0562   0A1E 0070          2190   FXDR1   RRD   SR,D2               GET LOW HALF; VECTOR TO FXR.010.          32321900
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FLOATING POINT INSTRUCTIONS

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0000 0563                2192  STE       EQU   *                ENTERED VIA DROM1            * 60 * 32321920
0563   0915 0070          2193            RRE   MDR,D2           GET DATA, VECTOR TO STF.D2           32321930

0000 0564                2195  LE        EQU   *                ENTERED VIA DROM2  (RXF)    * 68 * 32321950
0564   012C 0050          2196            LE    YD,MDR           LOAD REGISTER,                       32321960
0565   D18F 0070          2197            RCC   FLR,IR+JAM       SET CC, EXIT.                        32321970

0000 0566                2199  CE        EQU   *                ENTERED VIA DROM2  (RXF)    * 69 * 32321990
0566   013C 0050          2200            CER   YD,MDR           COMPARE                              32322000
0567   D18F 0070          2201            RCC   FLR,IR+JAM       SET CC,EXIT (CAN'T INTERRUPT)        32322010

0000 0568                2203  AE        EQU   *                ENTERED VIA DROM2  (RXF)    * 6A * 32322030
0568   014C 0050          2204            AER   YD,MDR           ADD                                  32322040
0569   D18F 0070          2205  EEXIT     RCC   FLR,IR+JAM       SET CC, EXIT.                        32322050
                          2206  *                                IF ENABLED FPP FAULT,                32322060
                          2207  *                                INTERRUPT THROUGH IV18 OCCURS.       32322070
                          2208  *                                FLAGS ARE STILL VALID IN THAT CASE.  32322080

0000 056A                2210  SE        EQU   *                ENTERED VIA DROM2  (RXF)    * 6B * 32322100
056A   015C 0050          2211            SER   YD,MDR           SUBTRACT                             32322110
056B   D18F 0070          2212            RCC   FLR,IR+JAM       SET CC, EXIT.                        32322120

0000 056C                2214  ME        EQU   *                ENTERED VIA DROM2  (RXF)    * 6C * 32322140
056C   016C 0050          2215            MER   YD,MDR           MULTIPLY                             32322150
056D   D18F 0070          2216            RCC   FLR,IR+JAM       SET CC, EXIT.                        32322160

0000 056E                2218  DE        EQU   *                ENTERED VIA DROM2  (RXF)    * 6D * 32322180
056E   017C 0050          2219            DER   YD,MDR           DIVIDE                               32322190
056F   D18F 0070          2220            RCC   FLR,IR+JAM       SET CC, EXIT.                        32322200

0000 0570                2222  STD       EQU   *                ENTERED VIA DROM1            * 70 * 32322220
0570   0215 0072          2223            RRD   MDR,YDP1         FETCH HIGH HALF DPFP DATA            32322230
0571   7A15 0074          2224            RRD   MDR,DW4+I4+D2    STORE; FETCH LOW; VECTOR TO STF.D2   32322240

0000 0572                2226  STME      EQU   *                ENTERED VIA DROM1            * 71 * 32322260
0572   005F 00A0          2227            L     FLR,YDI          MUST BE EVEN R1 SELECT               32322270
0573   DE08 5740          2228            BF    L,*+1,IR         ELSE, EXIT.                          32322280
0574   0115 0072          2229  STME1     RRE   MDR,YDP1         FETCH SPFP DATA                      32322290
0575   7F88 5742          2230            BF    YDC,STME1,DW4+YDP1 LOOP THROUGH R15 (AUTO-I4)        32322300
0576   D06C 0170          2231            L     NULL,NULL,IR     THEN EXIT.                           32322310

0577   0115 0072          2233  STME.ENT  RRE   MDR,YDP1         FETCH SPFP DATA                      32322330
0578   7F88 5772          2234            BF    YDC,STME.ENT,DW4+YDP1 STORE THROUGH R14 (AUTO-I4)    32322340
0579   0E01 00E0          2235            RETN                   THEN RETURN.                         32322350
```

FLOATING POINT INSTRUCTIONS

```
0000 057A                2237  LME       EQU   *                 ENTERED VIA DROM1                * 72 * 32322370
057A   FD88 0132          2238            BT    YDC,EXIT,DR4+YDP1 FETCH DATA (AUTO-I4);                    32322380
057B   012C 005A          2239            LE    YD,MDR,UNNLD      LOAD SPFP, UNNORMALIZED                   32322390
057C   DF88 57A2          2240            BF    YDC,LME,YDP1+IR   LOOP THROUGH R15, EXIT.                  32322400

057D   F06C 0172          2242  LME.ENT   L     NULL,NULL,DR4+YDP1 FETCH SPFP DATA (AUTO-I4)               32322420
057E   012C 005A          2243            LE    YD,MDR,UNNLD      LOAD SPFP, UNNORMALIZED                   32322430
057F   0F88 57D2          2244            BF    YDC,LME.ENT,YDP1  LOOP THROUGH R15                         32322440
0580   0E01 00E0          2245            RETN                    AND RETURN.                               32322450

0000 0581                2247  CDADSDMD  EQU   *                 ENTERED VIA DROM1                         32322470
0581   F06C 0174          2248            L     NULL,NULL,DR4+I4  FETCH HIGH HALF DPFP DATA                 32322480
0582   FA0C 0050          2249            LW    YD,MDR,DR4+D2     HIGH HALF; FETCH NEXT;                    32322490
                          2250  *                                 VECTOR TO LD,CD,AD,SD,MD,DD,LED.          32322500

0000 0583                2252  LD        EQU   *                 ENTERED VIA DROM2  (CDADSDMD) * 78 * 32322520
0583   022C 0050          2253            LD    YD,MDR            LOW HALF                                  32322530
0584   D18F 0070          2254            RCC   FLR,IR+JAM        SET CC, EXIT.                             32322540

0000 0585                2256  CD        EQU   *                 ENTERED VIA DROM2  (CDADSDMD) * 79 * 32322560
0585   023C 0050          2257            CDR   YD,MDR            COMPARE                                   32322570
0586   D18F 0070          2258            RCC   FLR,IR+JAM        SET CC, EXIT (CAN'T INTERRUPT)            32322580

0000 0587                2260  AD        EQU   *                 ENTERED VIA DROM2  (CDADSDMD) * 7A * 32322600
0587   024C 0050          2261            ADR   YD,MDR            ADD                                       32322610
0588   D18F 0070          2262            RCC   FLR,IR+JAM        SET CC, EXIT.                             32322620

0000 0589                2264  SD        EQU   *                 ENTERED VIA DROM2  (CDADSDMD) * 7B * 32322640
0589   025C 0050          2265            SDR   YD,MDR            SUBTRACT                                  32322650
058A   D18F 0070          2266            RCC   FLR,IR+JAM        SET CC, EXIT.                             32322660

0000 058B                2268  MD        EQU   *                 ENTERED VIA DROM2  (CDADSDMD) * 7C * 32322680
058B   026C 0050          2269            MDR   YD,MDR            MULTIPLY                                  32322690
058C   D18F 0070          2270            RCC   FLR,IR+JAM        SET CC, EXIT.                             32322700

0000 058D                2272  DD        EQU   *                 ENTERED VIA DROM2  (CDADSDMD) * 7D * 32322720
058D   027C 0050          2273            DDR   YD,MDR            DIVIDE                                    32322730
058E   D18F 0070          2274            RCC   FLR,IR+JAM        SET CC, EXIT.                             32322740

0000 058F                2276  STMD      EQU   *                 ENTERED VIA DROM1                * 7E * 32322760
058F   0215 0070          2277            RRD   MDR               READ HIGH HALF, DPFP DATA                 32322770
0590   0060 00A2          2278            L     MR0,YDI,YDP1      COMPUTE STEPS REQUIRED                    32322780
0591   001B 800F          2279            SI    CNTR,MR0,15       .                                         32322790
0592   7215 0072          2280            RRD   MDR,DW4+YDP1      STORE; READ NEXT (AUTO-I4)                32322800
0593   7E00 0130          2281            B     EXIT,DW4          STORE LAST, EXIT.                         32322810

0594   0215 0072          2283  STMD.ENT  RRD   MDR,YDP1          FETCH DPFP DATA HALF                      32322830
0595   006B 800F          2284            LI    CNTR,15           STEPS REQUIRED                            32322840
0596   7215 0072          2285            RRD   MDR,DW4+YDP1      STORE; FETCH NEXT (AUTO-I4)               32322850
0597   7E01 00E4          2286            RETN  DW4+I4            STORE LAST, RETURN.                       32322860


0000 0598                2288  LMD       EQU   *                 ENTERED VIA DROM1                * 7F * 32322880
0598   F06F 00A4          2289            L     FLR,YDI,DR4+I4    FETCH FIRST DATA                          32322890
```

FLOATING POINT INSTRUCTIONS

```
0599  0C08 0130          2290           BT    L,EXIT              EXIT IF ODD YDI SPEC, ELSE:      32322900
059A  F20C 0052          2291  LMD.010  LW    YD,MDR,DR4+YDP1     LOAD MSB (AUTO-I4)               32322910
059B  022C 005A          2292           LD    YD,MDR,UNNLD        LOAD LSB, UNNORMALIZED           32322920
059C  0D88 0132          2293           BT    YDC,EXIT,YDP1       EXIT AT R15                      32322930
059D  FE00 59A4          2294           B     LMD.010,DR4+I4      FETCH NEXT DATA, LOOP.           32322940

059E  F06C 0174          2296  LMD.ENT  L     NULL,NULL,DR4+I4    FETCH DATA, READY FOR NEXT       32322950
059F  F20C 0052          2297           LW    YD,MDR,DR4+YDP1     LOAD MSB, FETCH NEXT DATA        32322970
05A0  022C 005A          2298           LD    YD,MDR,UNNLD        LOAD LSB, UNNORMALIZED           32322980
05A1  0F88 59E2          2299           BF    YDC,LMD.ENT,YDP1    LOOP THROUGH R15,                32322990
05A2  0E01 00E0          2300           RETN                      RETURN.                          32323000
```

MIXED-MODE/MAGNITUDE FLOATING POINT INSTRUCTIONS

```
0000 05A3                2302  SWAP    EQU   *                 ENTERED VIA DROM1                          32323020
05A3   0060 00A0         2303          L     MR0,YDI           REMEMBER R1 SELECT                         32323030
05A4   006A 00B0         2304          L     YDI,YSI           SWAP R2 SELECT TO R1 SELECT                32323040
05A5   086C 000F         2305          L     NULL,MR0,LYSI+D2  COMPLETE SWAP;                            32323050
                         2306  *               VECTOR TO LGER, LGDR                                       32323060


0000 05A6                2308  LGER    EQU   *                 ENTERED VIA DROM2  (SWAP)     * 15 *       32323080
05A6   0199 0070         2309          RRE   YS,JAM            COPY SPFP TO GENERAL REGISTER,             32323090
05A7   D06C 0170         2310          L     NULL,NULL,IR      EXIT WITH CC = 0, 1, OR 2                  32323100

0000 05A8                2312  LGDR    EQU   *                 ENTERED VIA DROM2  (SWAP)     * 16 *       32323120
05A8   0299 0072         2313          RRD   YS,YDP1+JAM       LOAD HIGH HALF, SET CC                     32323130
05A9   006C 00BF         2314          L     NULL,YSI,LYSI     POINT USER'S R1+1                          32323140
05AA   0219 0070         2315          RRD   YS                LOAD LOW HALF                              32323150
05AB   D06C 0170         2316          L     NULL,NULL,IR      EXIT WITH CC = 0, 1, OR 2                  32323160

0000 05AC                2318  STDE    EQU   *                 ENTERED VIA DROM1             * 82 *       32323180
05AC   0215 0070         2319          RRD   MDR               GET HIGH HALF DPFP DATA                    32323190
05AD   0E18 2372         2320          BF    G+L,STF.D2,YDP1   BRANCH: STORE ZERO. POINT R1+1.             32323200
05AE   021F 0070         2321          RRD   SR                LOW HALF                                   32323210
05AF   0113 0070         2322          RRE   MR3               SAVE 'OLD' REGISTER CONTENTS               32323220
05B0   020C 0050         2323          LW    YD,MDR            HIGH HALF, NEW DATA                        32323230
05B1   012C 00D0         2324          LE    YD,SR             LOW HALF, NEW DATA. ROUND IT.              32323240
05B2   0102 0070         2325          RCC   MR2               GET RESULTING FLAGS                        32323250
05B3   0115 0070         2326          RRE   MDR               AND ROUNDED RESULT.                        32323260
05B4   006E 0030         2327          L     SR,MR3            RESTORE 'OLD' DATA                         32323270
05B5   012C 00DA         2328          LE    YD,SR,UNNLD                                                  32323280
05B6   006F 0020         2329          L     FLR,MR2           TEST FLAGS RESULTING FROM ROUND:           32323290
05B7   0E20 2370         2330          BF    V,STF.D2          BRANCH: NO ERROR. GO STORE.                32323300
05B8   0E18 2370         2331          BF    G+L,STF.D2        IGNORE UNDERFLOW, GO STORE ZERO            32323310
05B9   0E00 0D30         2332          B     AFAUL4            BRANCH: OVERFLOW.                          32323320

0000 0564                2334  LED     EQU   LE                ENTERED VIA DROM2 (CDADSDND)  * 84 *       32323340

0000 05BA                2336  LDE     EQU   *                 ENTERED VIA DROM1             * 87 *       32323360
05BA   F06E 0170         2337          L     SR,NULL,DR4       FETCH SPFP DATA                            32323370
05BB   020C 0050         2338          LW    YD,MDR            LOAD HIGH-HALF TO DOUBLE REG.              32323380
05BC   0A2C 00D0         2339          LD    YD,SR,D2          FOLLOWED BY ZEROS; GO TO EEXIT.            32323390
```

MIXED-MODE/MAGNITUDE FLOATING POINT INSTRUCTIONS

```
0000 05BD                2341  LEDR    EQU   *          ENTERED VIA DROM1                  * A4 * 32323410
05BD   0060 00A0         2342          L     MR0,YDI    REMEMBER R1 SELECT                        32323420
05BE   006A 00B0         2343          L     YDI,YSI    SELECT R2                                 32323430
05BF   0215 0072         2344          RRD   MDR,YDP1   HIGH HALF                               32323440
05C0   021E 0070         2345          RRD   SR         LOW HALF                                  32323450
05C1   006A 0000         2346          L     YDI,MR0    RESELECT R1                               32323460
05C2   020C 0050         2347          LW    YD,MDR     LOAD HIGH HALF                            32323470

0000 05C3                2349  LEGR    EQU   *          ENTERED VIA DROM1                  * A5 * 32323490
05C3   092C 00D0         2350          LE    YD,SR,D2   LOAD R2 DATA TO SPFP REG,                 32323500
                         2351  *                        VECTOR TO EEXIT.                          32323510

0000 05C4                2353  LDGR    EQU   *          ENTERED VIA DROM1                  * A6 * 32323530
05C4   020C 00D0         2354          LW    YD,SR      HIGH HALF                                 32323540
05C5   006C 00BF         2355          L     NULL,YSI,LYSI INCREMENT YSI BY 1                     32323550
05C6   086E 0090         2356          L     SR,YS,D2   LOW HALF DATA; VECTOR TO LDGR1.           32323560

0000 05C7                2358  LDER    EQU   *          ENTERED VIA DROM2  (EVALU)         * A7 * 32323580
05C7   020C 00D0         2359          LW    YD,SR      HIGH HALF                                 32323590
05C8   006E 0170         2360          L     SR,NULL    FOLLOWED BY ZEROS                         32323600
05C9   022C 00D0         2361  LDGR1   LD    YD,SR      LOAD LOW HALF,                            32323610
05CA   D18F 0070         2362          RCC   FLR,IR+JAM SET CC, EXIT.                             32323620

0000 05CB                2364  EVALU   EQU   *          ENTERED VIA DROM1                         32323640
05CB   0060 00A0         2365          L     MR0,YDI    REMEMBER R1 SELECT                        32323650
05CC   005A 00B0         2366          L     YDI,YSI    SELECT R2                                 32323660
05CD   011E 0070         2367          RRE   SR         GET SPFP DATA                             32323670
05CE   086A 0000         2368          L     YDI,MR0,D2 RESELECT R1,                              32323680
                         2369  *                        VECTOR TO LPER, LCER, LDER.               32323690

0000 05CF                2371  LPER    EQU   *          ENTERED VIA DROM2 (EVALU)          * 13 * 32323710
05CF   006E 0AD0         2372          SLL   SR,SR      FORCE POSITIVE                            32323720
05D0   006E 0ED0         2373          SRL   SR,SR      .                                         32323730
05D1   012C 00D0         2374          LE    YD,SR      LOAD SPFP DATA                            32323740
05D2   D18F 0070         2375          RCC   FLR,IR+JAM SET CC, EXIT.                             32323750

0000 05D3                2377  LCER    EQU   *          ENTERED VIA DROM2 (EVALU)          * 17 * 32323770
05D3   004E ED01         2378          XI    SR,SR,'01',RRL COMPLEMENT SIGN BIT                   32323780
05D4   012C 00D0         2379          LE    YD,SR      LOAD SPFP DATA                            32323790
05D5   D18F 0070         2380          RCC   FLR,IR+JAM SET CC, EXIT.                             32323800

0000 05D6                2382  DVALU   EQU   *          ENTERED VIA DROM1                         32323820
05D6   0060 00A0         2383          L     MR0,YDI    REMEMBER R1 SELECT                        32323830
05D7   006A 00B0         2384          L     YDI,YSI    SELECT R2                                 32323840
05D8   021E 0072         2385          RRD   SR,YDP1     GET MS HALF DPFP DATA                     32323850
05D9   0215 0070         2386          RRD   MDR        GET LS HALF DPFP DATA                     32323860
05DA   086A 0000         2387          L     YDI,MR0,D2 RESELECT R1; GO TO LPDR, LCDR             32323870
```

MIXED-MODE/MAGNITUDE FLOATING POINT INSTRUCTIONS

```
0000 05DB
05DB   006E 0AD0   2389 LPDR   EQU  *          ENTERED VIA DROM2 (DVALU)   * 33 *   32323890
05DB   006E 0AD0   2390         SLL  SR,SR      FORCE POSITIVE                        32323900
05DC   006E 0ED0   2391         SRL  SR,SR      .                                     32323910
05DD   020C 00D0   2392         LW   YD,SR      LOAD MS HALF MAGNITUDE                32323920
05DE   022C 0050   2393         LD   YD,MDR     LOAD LOW HALF,                        32323930
05DF   D18F 0070   2394         RCC  FLR,IR+JAM SET CC, EXIT.                         32323940

0000 05E0                                       ENTERED VIA DROM2 (DVALU)   * 37 *   32323960
05E0   004E ED01   2396 LCDR   EQU  *          FLIP SIGN BIT                         32323970
05E1   020C 00D0   2397         XI   SR,SR,'01',RRL LOAD HIGH HALF COMPLEMENT          32323980
05E2   022C 0050   2398         LW   YD,SR      LOAD LOW HALF                         32323990
05E3   D18F 0070   2399         LD   YD,MDR     SET CC, EXIT.                         32324000
                   2400         RCC  FLR,IR+JAM                                       32324010

                   2402 * ERROR ROUTINE CALLED BY ROUTINE 'STBPSTOR'                  32324020
05E4   0CB0 5E60   2403 STBPS.2 BT   MAT+MPE,STBPS.3 BRANCH: ERROR. ELSE,            32324030
05E5   DC10 72F0   2404         BT   G,SET.RTN,IR EXIT IF DONE NOW, OR SET INTPT PETURN32324040
05E6   0013 00E0   2405 STBPS.3 S    MR3,MR0,LR  POINT BACK TO LINK INSTRUCTION      32324050
05E7   006C 003E   2406         L    NULL,MR3,LLINK POINT (LR) TO CALLING INSTRUCTION 32324060
05E8   0E00 72F0   2407         B    SET.RTN     AND SERVICE INTERRUPT.                32324070

05E9                2409         IFP  '600'-*                                       32324090
05F9                2410         DO   '600'-*                                       32324100
05E9   0000 0000    2411         DC   FREEWORD                                      32324110
05EA   0000 0000    2411         DC   FREEWORD                                      32324110
05EB   0000 0000    2411         DC   FREEWORD                                      32324110
05EC   0000 0000    2411         DC   FREEWORD                                      32324110
05ED   0000 0000    2411         DC   FREEWORD                                      32324110
05EE   0000 0000    2411         DC   FREEWORD                                      32324110
05EF   0000 0000    2411         DC   FREEWORD                                      32324110
05F0   0000 0000    2411         DC   FREEWORD                                      32324110
05F1   0000 0000    2411         DC   FREEWORD                                      32324110
05F2   0000 0000    2411         DC   FREEWORD                                      32324110
05F3   0000 0000    2411         DC   FREEWORD                                      32324110
05F4   0000 0000    2411         DC   FREEWORD                                      32324110
05F5   0000 0000    2411         DC   FREEWORD                                      32324110
05F6   0000 0000    2411         DC   FREEWORD                                      32324110
05F7   0000 0000    2411         DC   FREEWORD                                      32324110
05F8   0000 0000    2411         DC   FREEWORD                                      32324110
05F9   0000 0000    2411         DC   FREEWORD                                      32324110
05FA   0000 0000    2411         DC   FREEWORD                                      32324110
05FB   0000 0000    2411         DC   FREEWORD                                      32324110
05FC   0000 0000    2411         DC   FREEWORD                                      32324110
05FD   0000 0000    2411         DC   FREEWORD                                      32324110
05FE   0000 0000    2411         DC   FREEWORD                                      32324110
05FF   0000 0000    2411         DC   FREEWORD                                      32324110
                    2412         ENDC                                               32324120
```

STRING INSTRUCTIONS

```
0600                    2414          ORG   '600'              MUST BE ON '100' BOUNDARY          32324140
0000 0600               2415  RXRXTAB EQU   *                                                    32324150
0600   0E00 61D0        2416          B     MVTU               CODE 0                             32324160
0601   0E00 61D0        2417          B     MOVE               CODE 1                             32324170
0602   0E00 6540        2418          B     CPAN               CODE 2                             32324180
0603   0E00 5850        2419          B     PMV                CODE 3                             32324190
0604   0E00 6FC0        2420          B     UMV                CODE 4                             32324200


0000 0605               2422  RXRX    EQU   *                  ENTERED VIA DROM1          * 8C *  32324220
0605   0063 00B0        2423          L     MR3,YSI            GETS XOP, YD2, YS2                 32324230
0606   0060 00AF        2424          L     MR0,YDI,LYSI       SAVE YD1                           32324240
0607   002A FC02        2425          NI    YDI,PSW,'02',EXH   TEST IIP BIT                      32324250
0608   0C18 72A2        2426          BT    G+L,IIPRESUM,YDP1  BRANCH: IN PROGRESS NOW. POINT R1  32324260
0609   0468 00D2        2427          L     ARSYD,SR,YDP1      ARS R1 = OP1 STRING POINTER        32324270
060A   0468 00E2        2428          L     ARSYD,MAR,YDP1     ARS R2 = OP2 STRING POINTER        32324280
060B   002C B480        2429          NI    NULL,MR3,'80',EXB  IMMEDIATE LEN1 SPEC'D ?            32324290
060C   0C18 60E2        2430          BT    G+L,RXRX1,YDP1     BRANCH: YES.                       32324300
060D   0060 0090        2431          L     MR0,YS             GET LENGTH FROM LEN1 REGISTER      32324310
060E   0468 0C02        2432  RXRX1   L     ARSYD,MP0,YDP1     ARS R4 = LEN1                      32324320
060F   0020 B0F0        2433          NI    MR0,MR3,'F0'       YD2 SELECT                         32324330
0610   006B 8004        2434          LI    CNTR,4                                                32324340
0611   0060 0E0F        2435          SRL   MR0,MR0,LYSI       POSITION LEN2 SELECT               32324350
0612   002C B440        2436          NI    NULL,MR3,'40',EXB  IMMEDIATE LEN2 SPEC'D ?            32324360
0613   0C18 6150        2437          BT    G+L,RXRX2          BRANCH: YES.                       32324370
0614   0060 0090        2438          L     MR0,YS             GET LENGTH                         32324380
0615   0468 0001        2439  RXRX2   L     ARSYD,MR0,CYD&SWA  ARS R5 = LEN2                      32324390
0616   0468 0430        2440          EXB   ARSYD,MR3          ARS R0 HAS XOP BYTE IN BITS 24:31. 32324400
0617   0420 C01F        2441          NI    MR0,ARSYD,'1F'     GET FUNCTION CODE                  32324410
0618   0031 8406        2442          OI    MR1,MR0,H(RXRXTAB),EXB                               32324420
0619   006C 001E        2443          L     NULL,MR1,LLINK                                        32324430
061A   001C 8004        2444          SI    NULL,MR0,4         VALID FUNCTION CODE ?              32324440
061B   0E41 00E0        2445          RETNF C                  BRANCH THROUGH TABLE IF YES.       32324450
061C   0E00 0C20        2446          B     IIINT              ILLEGAL CODE                       32324460
```

STRING INSTRUCTIONS

```
                        2448  * FOR THE FOLLOWING MOVE ROUTINES, THE FOLLOWING CONVENTIONS HOLD:      32324480
                        2449  * MVTU: AT INPUT, GR0 CONTAINS AN 'ESCAPE' OR 'UNTIL' CHARACTER.       32324490
                        2450  *                GR2 MAY CONTAIN THE ADDRESS OF A TRANS. TABLE.        32324500
                        2452  * ALL: AT OUTPUT, GR1 IS LOADED WITH THE ADDRESS OF THE NEXT           32324520
                        2453  *                BYTE TO BE PROCESSED IN THE SECOND OPERAND STRING.    32324530
                        2454  *                IF THIS STRING IS OF ZERO LENGTH, THE ADDRESS        32324540
                        2455  *                OF THE SPECIFIED STRING START IS RETURNED.           32324550

0000 061D               2457  MVTU     EQU   *                    (8C/00)                          32324570
0000 061D               2458  MOVE     EQU   *                    (8C/01)                          32324580
0000 061D               2459  MOVEP    EQU   *                    (8C/21)                          32324590
061D   0052 0002        2460           L     MR2,MR0,YDP1         FUNCTION CODE; POINT R1          32324600
061E   0C18 6222        2461           BT    G+L,MOVE0,YDP1       BRANCH: MOVE OR MOVEP            32324610
061F   0062 0080        2462           L     MR2,YD               A(TRTBL) FROM GR2                32324620
0620   0E18 6220        2463           BF    G+L,MOVE0            BRANCH: TRTBL NOT TO BE USED.    32324630
0621   0032 AD01        2464           OI    MR2,MR2,'01',RRL     MR2 = 80XXXXXX - USING TRTBL.    32324640
0622   0E02 67A0        2465  MOVE0    LINK  GET.END              GET PAD CHARACTER IN R0          32324650
                        2466  *                                  R1 = R1+R4; R2 = R2+R5;          32324660
                        2467  *                                  FUNCTION CODE TO R3.             32324670
0623   5E02 72F0        2468           LINK  SET.RTN,ENACLK       LOAD INTERRUPT RETURN IN R11     32324680
0624   0062 80FF        2469           LI    MR2,'FF'             BYTE MASK                        32324690
0625   006E 8001        2470           LI    SR,1                 CONSTANT                         32324700
0626   0460 0080        2471  MOVE1    L     MR0,ARSYD            LEN(OPERAND 2) FROM R5           32324710
0627   0E10 6400        2472           BF    G,PADIT              BRANCH: LEN2 DONE (SOURCE)       32324720
0628   006A 8002        2473           LI    YDI,2                                                 32324730
0629   0416 0082        2474  MOVE1A   S     MAR,MR0,ARSYD,YDP1   (END2-LEN2) USING R2 IS LOW BYTE 32324740
062A   B46C 008F        2475           L     NULL,ARSYD,LYSI+DR2  'FUNCTION CODE' FROM R3; FETCH.  32324750
062B   0C10 6352        2476           BT    G,MOVE2A,YDP1        BRANCH: MOVE OR MOVEP; POINT R4  32324760
062C   0E08 6300        2477           BF    L,MVTU2              BRANCH: MVTU, NOT USING TRTBL    32324770
062D   0023 2453        2478           N     MR3,MR2,MDR,EXB+YDP1 EXTRACT DATA BYTE                32324780
062E   0405 3082        2479           A     MAR,MR3,ARSYD,YDP1   DATA BYTE + A(TRTBL)             32324790
062F   B06C 017F        2480           L     NULL,NULL,LYSI+DP2   FETCH XLATION DATA; YSI = 0      32324800
0630   0023 2450        2481  MVTU2    N     MR3,MR2,MDR,EXB      EXTRACT ARGUMENT BYTE            32324810
0631   004C 3090        2482           X     NULL,MR3,YS          SAME AS 'UNTIL' BYTE IN GR0 ?    32324820
0632   0C18 6360        2483           BT    G+L,MOVE2            BRANCH: NO. CONTINUE.            32324830

0633   00EF 8008        2485  TERMCHAR LI    FLR,8,JAM            SET CC = 8                       32324850
0634   0E00 6500        2486           B     OUTPUT.A             OUTPUT A(STR2 BYTE) = TERM CHAR  32324860

0635   0023 2450        2488  MOVE2A   N     MR3,MR2,MDR,EXB      STR2 BYTE (MOVE OR MOVEP)        32324880
0636   0461 0081        2489  MOVE2    L     MR1,ARSYD,CYD&SWA    LEN1 FROM R4                     32324890
0637   0E10 64F2        2490           BF    G,OUTPUT.Z,YDP1      BRANCH: LEN1 EXHAUSTED.          32324900

0638   0416 1080        2492           S     MAR,MR1,ARSYD        (END1-LEN1) USING R1             32324920
0639   0065 0430        2493           EXB   MDR,MR3              POSITION DEST'N BYTE             32324930
063A   106A 8004        2494           LI    YDI,4,DW1            STORE BYTE, POINT R4             32324940
063B   0418 6082        2495           S     ARSYD,SR,ARSYD,YDP1  DECREMENT LEN1 IN R4,            32324950
063C   0418 6080        2496           S     ARSYD,SR,ARSYD       DECREMENT LEN2 IN R5.            32324960
063D   0460 0081        2497           L     MR0,ARSYD,CYD&SWA    LEN(OPERAND 2) FROM R5           32324970
063E   5D40 7342        2498           BT    INT,INTRPT5,ENACLK+YDP1 BRANCH: SERVICE ANY INTERRUPT; 32324980
063F   0C10 6292        2499           BT    G,MOVE1A,YDP1        BRANCH: LEN2 NOT EXHAUSTED. ELSE PAD:32324990
```

STRING INSTRUCTIONS

```
0000 0640                2501  PADIT    EQU   *                    FILLS OUT DESTINATION WITH PADC      32325010
0640   0E02 72F0         2502           LINK  SET.RTN                                                   32325020
0641   006A 8005         2503  PAD.0    LI    YDI,5                                                    32325030
0642   0460 0083         2504           L     MR0,ARSYD,YDM1       GET LEN2 FROM R5 (FOR OUTPUT.A)     32325040
0643   006C 00AF         2505           L     NULL,YDI,LYSI        SELECT R4 AS YS                     32325050
0644   04E1 0080         2506           L     MR1,ARSYD,JAM        GET LEN1 FROM R4                    32325060
0645   0E10 6503         2507           BF    G,OUTPUT.A,YDM1      BRANCH: ALL DONE.                   32325070
0646   046C 0083         2508           L     NULL,ARSYD,YDM1      CODE FROM R3 - MVTU ?               32325080
0647   0E10 6503         2509           BF    G,OUTPUT.A,YDM1      BRANCH: YES. TERMINATE.             32325090
0648   0416 5081         2510  PAD.1    S     MAR,ARSYS,ARSYD,CYD&SWA (END1-LEN1) USING (R1-R4)        32325100
0649   0465 0462         2511           EXB   MDR,ARSYD,YDP1       PADC FROM R0                        32325110
064A   1061 8001         2512           LI    MR1,1,DW1                                                32325120
064B   0499 1090         2513           S     ARSYS,MR1,ARSYS,JAM  DECREMENT LEN1 BY 1                 32325130
064C   5D40 7340         2514           BT    INT,INTRPT5,ENACLK   SERVICE INTERRUPT                   32325140
064D   0C10 6480         2515           BT    G,PAD.1              LOOP IF LEN1 NOT EXHAUSTED.         32325150
064E   0E00 6410         2516           B     PAD.0                GO OUTPUT (END2-LEN2) = END2.       32325160

064F   00EF 8004         2518  OUTPUT.Z LI    FLR,4,JAM            DEST'N OVERFLOW - SET CC = 4        32325180
0650   5CB0 7340         2519  OUTPUT.A BT    MAT+MPE,INTRPT5,ENACLK SERVICE ERROR BEFORE LEAVING      32325190
0651   006A 8002         2520           LI    YDI,2                TELL USER WHERE TO RESUME IN STR2:  32325200
0652   0410 0083         2521           S     MR0,MR0,ARSYD,YDM1   (END2-LEN2) USING R2                32325210
0653   0068 0000         2522           L     YD,MR0,IR            THE ADDRESS OF THE NEXT STR2 BYTE   32325220
                         2523  *                                   TO BE PROCESSED IS RETURNED IN GR1. 32325230


                         2525  * FOR THE FOLLOWING COMPARE ROUTINES, THE FOLLOWING CONVENTIONS HOLD:    32325250
                         2526  * ALL: AT OUTPUT, GR1 IS LOADED WITH THE OFFSET OF THE LAST BYTE         32325260
                         2527  *                 PROCESSED IN THE SECOND OPERAND STRING. FOR           32325270
                         2528  *                 A NON-EQUAL COMPARE, THIS INDICATES THE FIRST         32325280
                         2529  *                 (LOWEST-ADDRESSED) STRING 2 BYTE WHICH DOES NOT       32325290
                         2530  *                 EQUAL THE CORRESPONDING STRING 1 BYTE; PROVIDED       32325300
                         2531  *                 THAT STRING 2 IS NOT SHORTER THAN STRING 1.           32325310
                         2532  *                 IF STRING 2 IS OF LENGTH ZERO BYTES, ZERO OFFSET      32325320
                         2533  *                 IS RETURNED.                                          32325330


0000 0654                2535  CPAN     EQU   *                    (8C/02)                             32325350
0000 0654                2536  CPANP    EQU   *                    (8C/22)                             32325360
0654   0E02 67A0         2537           LINK  GET.END              GET PADC IN R0;                     32325370
                         2538  *                                   R1 = R1+R4; R2 = R2+R5;             32325380
0655   006A 8003         2539           LI    YDI,3                                                    32325390
0656   0468 0060         2540           L     ARSYD,MAR            R3 = A(STR2) FOR OFFSET             32325400
0657   006A 8001         2541           LI    YDI,1                                                    32325410
0658   0068 0060         2542           L     YD,MAR               R1 = A(STR2), ALSO FOR OFFSET       32325420
0659   0E02 72F0         2543           LINK  SET.RTN              SET INTERRUPT RETURN IN R11         32325430
065A   0063 80FF         2544           LI    MR3,'FF'             BYTE MASK                           32325440
065B   00EF 017F         2545           L     FLR,NULL,LYSI+JAM    YSI = CC = 0                        32325450
065C   0062 8001         2546           LI    MR2,1                CONSTANT                            32325460

0000 065D                2548  CPAN1    EQU   *                                                        32325480
065D   0461 0083         2549           L     MR1,ARSYD,YDM1       GET LEN2 FROM R5                    32325490
065E   0E10 6740         2550           BF    G,CPAN20             BRANCH: LEN2 EXHAUSTED. PAD LEN2.   32325500
```

STRING INSTRUCTIONS

```
065F   046E 0083   2551           L     SR,ARSYD,YDM1       GET LEN1 FROM R4                          32325510
0660   0E10 6663   2552           BF    G,CPAN10,YDM1       BRANCH: LEN1 EXHAUSTED. PAD LEN1.         32325520
0661   0416 1083   2553           S     MAR,MR1,ARSYD,YDM1  A(BYTE2)=A(END2)-LEN2 USING R2             32325530
0662   B068 0060   2554           L     YD,MAR,DR2          TO RETURN OFFSET2 IN GR1 AT MISMATCH      32325540
                   2555   *                                 THIS REFLECTS FIRST MISMATCH ON           32325550
                   2556   *                                 'FIND STR1 IN STR2' OPERATION, BUT        32325560
                   2557   *                                 REQUIRES LEN2 >= LEN1 FOR SENSIBLE        32325570
                   2558   *                                 RESULT.                                   32325580
0663   0021 3450   2559           N     MR1,MR3,MDR,EXB     (BYTE2)                                   32325590
0664   0416 6082   2560           S     MAR,SR,ARSYD,YDP1   A(BYTE1) USING R1                        32325600
0665   BE00 6782   2561           B     CPAN21,DR2+YDP1                                               32325610
                   2562   *                                                                           32325620
0000 0666          2563   CPAN10  EQU   *                   STRING 1 EXHAUSTED (DEST'N)               32325630
0666   0416 1081   2564           S     MAR,MR1,ARSYD,CYD&SWA A(BYTE2)=A(END2)-LEN2 USING R2          32325640
0667   B460 0082   2565           L     MR0,ARSYD,DR2+YDP1  GET PADC FROM R0, FETCH BYTE2             32325650
0668   0068 0062   2566           L     YD,MAR,YDP1         TO RETURN OFFSET2 IN GR1 AT MISMATCH      32325660

0669   0021 3452   2568   CPAN2   N     MR1,MR3,MDR,EXB+YDP1 EXTRACT BYTE2, POINT R3                  32325680
066A   003C 1002   2569   CPAN3   S     NULL,MR1,MR0,JAM+YDP1 (BYTE1-BYTE2); CC = 0, 2, OR 9.         32325690
066B   0E18 6702   2570           BF    G+L,CPAN4,YDP1      BRANCH: STILL EQUAL.                      32325700

066C   005A 8003   2572   MISMATCH LI   YDI,3               RETURN STR2 OFFSET OF 1ST MISMATCH:       32325720
066D   0460 0083   2573           L     MR0,ARSYD,YDM1      A(STR2) FROM R3                           32325730
066E   5CE0 7343   2574           BT    MAT+MPE,INTRPT5,ENACLK+YDM1 SERVICE ERROR INTERRUPT           32325740
066F   D016 0080   2575           S     YD,MR0,YD,IR        RETURN A(BYTE2) - A(STR2) IN R1.          32325750

0670   0418 2083   2577   CPAN4   S     ARSYD,MR2,ARSYD,YDM1 DECREMENT LEN2 IN R5                     32325770
0671   0418 2082   2578           S     ARSYD,MR2,ARSYD,YDP1 DECREMENT LEN1 IN R4                     32325780
0672   0F40 65D0   2579           BF    INT,CPAN1           LOOP, UNLESS                              32325790
0673   5E00 7340   2580           B     INTRPT5,ENACLK      SERVICE ANY INTERRUPT.                    32325800

0000 0674          2582   CPAN20  EQU   *                   STRING 2 EXHAUSTED (SOURCE)               32325820
0674   046E 0081   2583           L     SR,ARSYD,CYD&SWA    LEN1 FROM R4                              32325830
0675   0E10 66C2   2584           BF    G,MISMATCH,YDP1     BRANCH: LEN1 ALSO EXHAUSTED.              32325840
0676   0416 6082   2585           S     MAR,SR,ARSYD,YDP1   A(BYTE1) = END1-LEN1 USING R1              32325850
0677   B461 0092   2586           L     MR1,ARSYS,DR2+YDP1  PADC FROM R0; FETCH BYTE                 32325860
0678   0020 3450   2587   CPAN21  N     MR0,MR3,MDR,EXB     EXTRACT BYTE1                             32325870
0679   0E00 66A0   2588           B     CPAN3               AND GO COMPARE WITH PADC IN MR1.          32325880

                   2590   * ROUTINE CALCULATES (STR1+LEN1), (STR2+LEN2).                              32325900
                                                                                                      32325910
067A   006A 8005   2591   GET.END LI    YDI,5                                                         32325920
067B   0451 0083   2592           L     MR1,ARSYD,YDM1      LEN(OPERAND 2) FROM R5                    32325930
067C   0450 0083   2593           L     MR0,ARSYD,YDM1      LEN(OPERAND 1) FROM R4                    32325940
067D   0468 0023   2594           L     ARSYD,MR2,YDM1      FLAG TO R3                                32325950
067E   0408 1083   2595           A     ARSYD,MR1,ARSYD,YDM1 R2 = END(OPERAND 2)                      32325960
067F   0408 0083   2596           A     ARSYD,MR0,ARSYD,YDM1 R1 = END(OPERAND 1)

                   2598   * ROUTINE GETS PAD CHARACTER IN R0.                                         32325980
0000 0680          2599   GETPAD  EQU   *                   GET REQUIRED PAD CHARACTER                32325990
0680   0428 C020   2600           NI    ARSYD,ARSYD,'20'    XOP BYTE (IN R0) SAYS DEFAULT PAD ?       32326000
0681   0C19 00E0   2601           RETNT G+L                 BRANCH: RETURN DEFAULT PAD '20'           32326010
0682   0022 C0FF   2602           NI    MR2,YD,'FF'         GET BYTE FROM GR0 B24:31.                 32326020
0683   0468 0020   2603           L     ARSYD,MR2           PADC SAVED IN R0                          32326030
0684   0E01 00E0   2604           RETN                      RETURN TO CALLER                          32326040
```

STRING INSTRUCTIONS

```
                        2606  * FOR THE FOLLOWING PACK ROUTINES, THE FOLLOWING CONVENTIONS HOLD:      32326060
                        2607  * ALL: AT INPUT, STRING LENGTHS ONE GREATER THAN SPECIFIED IN           32326070
                        2608  *               THE USER-LEVEL INSTRUCTION ARE ASSUMED. NO             32326080
                        2609  *               MAXIMUM IS IMPOSED. PACK PROCEEDS RIGHT-TO-LEFT.       32326090
                        2610  *               AN ODD NUMBER OF PACKED DATA DIGITS IS ALWAYS          32326100
                        2611  *               PRODUCED.                                              32326110
                        2613  *               NO INTERRUPT RESULTS FROM AN INVALID SIGN OR           32326130
                        2614  *               DATA DIGIT.                                            32326140
                        2616  *               STANDARD SIGN DIGITS 'C' OR 'D' ARE PRODUCED.          32326160
                        2617  *               A STRING REPRESENTING ZERO HAS SIGN DIGIT 'C'.         32326170

0000 0685               2619  PMV     EQU   *                  (8C/03)                              32326190
0000 0685               2620  PMVA    EQU   *                  (8C/23)                              32326200
0685   5E02 72F0        2621          LINK  SET.RTN,ENACLK     SET INTERRUPT RETURN IN R11          32326210
0686   006A 8003        2622          LI    YDI,3                                                   32326220
0687   04E8 0170        2623          L     ARSYD,NULL,JAM     PRESET FLAGS = 0                     32326230
0688   0E02 6B03        2624          LINK  GETBYT.1,YDM1      GET UNPACKED SIGNED BYTE FROM STR2   32326240
0689   0060 30D0        2625          L     MR0,SR             MR0:SR = DATA, BOTH FORM 00000CSD    32326250
068A                    2626          DO    4                  GET MR0:SR = C000000S:D000000S       32326260
068A   0060 0E0C        2627          SRL   MR0,MR0,DWSHFT     .                                    32326270
068B   0060 0E0C        2627          SRL   MR0,MR0,DWSHFT     .                                    32326270
068C   0060 0E0C        2627          SRL   MR0,MR0,DWSHFT     .                                    32326270
068D   0060 0E0C        2627          SRL   MR0,MR0,DWSHFT     .                                    32326270
068E   0E02 6CD0        2628          LINK  SGN.CHK            CHECK (MR0) FOR VALID SIGN DIGIT     32326280
068F   0E02 6C70        2629          LINK  DIGITCK            CHECK (MR2) FOR VALID DECIMAL        32326290
0690   006E 0CD0        2630          EXH   SR,SR              DATA FORM = 000SD000                 32326300
0691   003E 04D1        2631          O     SR,MR0,SR,EXB+CYD&SWA FORM PACKED SIGNED BYTE (DS)      32326310
0692   0E02 6B92        2632          LINK  STORBYTE,YDP1      AND STORE @ (STR1+LEN1)              32326320
0693   0418 3082        2633          S     ARSYD,MR3,ARSYD,YDP1 DECREMENT LEN1 IN R4 BY 1,         32326330
0694   0418 3080        2634          S     ARSYD,MR3,ARSYD    DECREMENT LEN2 IN R5 BY 1            32326340
0695   0E02 72F0        2635          LINK  SET.RTN            SET NEW INTERRUPT RETURN             32326350
                        2636  *                                IF FAULT, RETRY FROM SIGNED BYTE     32326360

0000 0696               2638  PMVLP1  EQU   *                  PACK LOOP. ENTERED WITH YDI=5.       32326380
                        2639  *                                OPERATES RIGHT-TO-LEFT.              32326390
0696   0460 0081        2640          L     MR0,ARSYD,CYD&SWA  LEN2 (IN R5) EXHAUSTED ?            32326400
0697   0C08 6DE2        2641          BT    L,PUSHP,YDP1       BRANCH: YES. OUTPUT '00'             32326410
0698   0E02 6B02        2642          LINK  GETBYT.1,YDP1      GET (LOW) ZONED BYTE                 32326420
0699   0E02 6C70        2643          LINK  DIGITCK            CHECK (MR2) FOR VALID DECIMAL        32326430
069A   006E 0021        2644          L     SR,MR2,CYD&SWA     (LOW) DECIMAL DIGIT                  32326440
069B   0063 0172        2645          L     MR3,NULL,YDP1      IN CASE OF FLUSH                     32326450
069C   0013 3005        2646          SDEC  MR3,MR3,MR0        DECR'D LEN2 < 0 ?                    32326460
069D   0C08 6A72        2647          BT    L,PMVL002,YDP1     BRANCH: YES, BUT WE HAVE ONE DIGIT NO32326470
069E   0406 3082        2648          A     MAR,MR3,ARSYD,YDP1 A(HIGH BYTE) USING R2                32326480
069F   B062 800F        2649          LI    MR2,'0F',DR2       DIGIT MASK; FETCH (HIGH) ZONED BYTE  32326490
06A0   0022 2452        2650          N     MR2,MR2,MDR,EXB+YDP1 EXTRACT DATA DIGIT                 32326500
06A1   0E18 6A80        2651          BF    G+L,PMVL002A       BRANCH: NEEDN'T PROCESS ZERO DIGIT   32326510
06A2   0E02 6C70        2652          LINK  DIGITCK            CHECK (MR2) FOR VALID DECIMAL        32326520
06A3   0062 0A20        2653          SLL   MR2,MR2            POSITION HIGH DIGIT                  32326530
06A4   0062 0A20        2654          SLL   MR2,MR2            .                                    32326540
06A5   0062 0A20        2655          SLL   MR2,MR2            .                                    32326550
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STRING INSTRUCTIONS

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06A6   003E 6A20          2656           O     SR,SR,MR2,SLL       PACK                                        32326560
06A7   006A 8004          2657  PMVL002  LI    YDI,4                                                           32326570
06A8   046C 0080          2658  PMVL002A L     NULL,ARSYD          LEN1 < 0 ?                                  32326580
06A9   0C08 6EA1          2659           BT    L,FLUSHP,CYD&SWA    BRANCH: YES. (SR) DATA MUST BE ZERO.        32326590
06AA   0E02 6B92          2660           LINK  STORBYTE,YDP1       STORE PACKED OUTPUT BYTE IN STR1            32326600
06AB   0418 3082          2661           S     ARSYD,MR3,ARSYD,YDP1 DECREMENT LEN1 IN R4 BY 1                   32326610
06AC   0418 3085          2662           SDEC  ARSYD,MR3,ARSYD     DECREMENT LEN2 IN R5 BY 2                   32326620
06AD   0F40 6960          2663           BF    INT,PMVLP1          LOOP, UNLESS                                32326630
06AE   5E00 7340          2664           B     INTRPT5,ENACLK      SERVICE ANY INTERRUPT.                      32326640

                          2666  * ROUTINE GETS BYTE FROM MEMORY @ END2                                          32326650
                          2667  GETBYTE  EQU   *                                                              32326660
0000 06AF                 2668           LI    YDI,2                                                           32326670
06AF   006A 8002          2669  GETBYT.1 L     MAR,ARSYD           A(STR2)                                     32326680
06B0   0466 0080          2670           LI    YDI,5                                                           32326690
06B1   006A 8005          2671           A     MAR,ARSYD,MAR       A(BYTE2) = A(STR2) + LEN2                   32326700
06B2   0406 4060          2672           LI    SR,'FF',DR2         BYTE MASK                                   32326710
06B3   B06E 80FF          2673           N     SR,SR,MDR,EXB       EXTRACT BYTE                                32326720
06B4   002E 6450          2674           NI    MR2,SR,'0F'         LOW DIGIT                                   32326730
06B5   0022 E00F          2675           NI    MR3,SR,'F0'         HIGH DIGIT                                  32326740
06B6   0023 E0F0          2676           RETNF MAT+MPE             RETURN                                      32326750
06B7   0EB1 00E0          2677           B     INTRPT5,ENACLK      SERVICE ERROR INTERRUPT.                    32326760
06B8   5E00 7340                                                                                               32326770

                          2679  * ROUTINE STORES BYTE IN MEMORY @ END1                                          32326780
                          2680  STORBYTE EQU   *                  EXPECTS YDI=1 @ ENTRY                       32326790
0000 06B9                 2681           L     MAR,ARSYD           A(STR1) FROM R1                             32326800
06B9   0466 0080          2682           LI    YDI,4                                                           32326810
06BA   005A 8004          2683           A     MAR,ARSYD,MAR       A(BYTE1) = A(STR1) + LEN1                   32326820
06BB   0406 4060          2684           EXB   MDR,SR                                                          32326830
06BC   0065 04D0          2685           LI    MR3,1,DW1           CONSTANT; STORE BYTE.                       32326840
06BD   1063 8001          2686           RETNF MAT+MPE                                                         32326850
06BE   0EB1 00E0          2687           B     INTRPT5,ENACLK      SERVICE ERROR INTERRUPT                     32326860
06BF   5E00 7340                                                                                               32326870

                          2689  * ROUTINE ADJUSTS CC ACCORDING TO QUEUED DATA IN R3                             32326880
                          2690  PMVFLAGS EQU   *                                                              32326890
0000 06C0                 2691           LI    YDI,3               FLAG REGISTER IS R3                         32326900
06C0   006A 8003          2692           NI    NULL,ARSYD,'0F',EXB ANY SIGNIFICANCE ?                          32326910
06C1   042C CC0F          2693           RETNF G+L                 BRANCH: NO.                                 32326920
06C2   0E19 00E0          2694           O     FLR,PSW,ARSYD,JAM   GET QUEUED FLAGS                            32326930
06C3   04BF 7080          2695           RETNT L                   BRANCH: ALREADY NEGATIVE                    32326940
06C4   0C09 00E0          2696           OI    FLR,PSW,2,JAM       SET G FLAG                                  32326950
06C5   00BF F002          2697           RETN                      AND RETURN.                                 32326960
06C6   0E01 00E0                                                                                               32326970

                          2699  * ROUTINE ACCUMULATES SIGNIFICANCE, TESTS FOR VALID DATA                        32326980
                          2700  DIGITCK  EQU   *                  CHECKS MR2(28:31) FOR VALID DECIMAL          32326990
0000 06C7                 2701           LI    YDI,3               FLAG REGISTER IS R3                         32327000
06C7   006A 8003                                                                                              32327010
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STRING INSTRUCTIONS

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06C8   001C A009          2702  DIGITCK1 SI    NULL,MR2,'09'          VALID DECIMAL NIBBLE ?                 32327020
06C9   0E40 6C30          2703           BF    C,DIGC1                BRANCH: YES.                           32327030
06CA   0438 C008          2704           OI    ARSYD,ARSYD,'08'       QUEUE C-FLAG                           32327040
06CB   0438 4C20          2705  DIGC1    O     ARSYD,ARSYD,MR2,EXH    ACCUMULATE SIGNIF. IN HIGH HALF        32327050
06CC   0E01 00E2          2706           RETN  YDP1                   POINT R4, RETURN.                      32327060



                          2708  * ROUTINE CHECKS (MRO) FOR VALID SIGN DIGIT, QUEUES FLAGS.                   32327080
                          2709  * STANDARD SIGN DIGIT RETURNED IN MRO.                                       32327090
0000 06CD                 2710  SGN.CHK  EQU   *                                                            32327100
06CD   004C 8003          2711           XI    NULL,MRO,'03'          PLUS ?                                 32327110
06CE   0E18 6DC1          2712           BF    G+L,SGPLUS,CYD&SWA     BRANCH: YES.                           32327120
06CF   001C 8009          2713           SI    NULL,MRO,'09'          ILLEGAL SIGN DIGIT ?                   32327130
06D0   0C40 6D20          2714           BT    C,SGN.CK1              BRANCH: A, B, C, D, E, OR F            32327140
06D1   00BF F008          2715           OI    FLR,PSW,'08',JAM       ILLEGAL. SET C FLAG.                   32327150
06D2   042C C020          2716  SGN.CK1  NI    NULL,ARSYD,'20'        "ABSOLUTE" SPEC'D BY C BIT OF XCP ?    32327160
06D3   0C18 6DC0          2717           BT    G+L,SGPLUS             BRANCH: YES.                           32327170
06D4   004C 800B          2718           XI    NULL,MRO,'0B'          NEGATIVE ?                             32327180
06D5   0E18 6D80          2719           BF    G+L,SGMINUS            BRANCH: YES.                           32327190
06D6   004C 800D          2720           XI    NULL,MRO,'0D'          NEGATIVE ?                             32327200
06D7   0C18 6DC0          2721           BT    G+L,SGPLUS             BRANCH: NO.                            32327210
                          2722  *                                      ILLEGAL TREATED AS PLUS HERE.          32327220
06D8   0060 800D          2723  SGMINUS  LI    MRO,'0D'               SIGN DIGIT                             32327230
06D9   006A 8003          2724           LI    YDI,3                                                         32327240
06DA   0438 C001          2725           OI    ARSYD,ARSYD,1          QUEUE L FLAG IN R3                     32327250
06DB   0E01 00E0          2726           RETN                         RETURN                                 32327260
06DC   0060 800C          2727  SGPLUS   LI    MRO,'0C'               POSITIVE SIGN DIGIT                    32327270
06DD   0E01 00E0          2728           RETN                         RETURN                                 32327280
                          .

                          2730  * ROUTINES STORE REPRESENTATION OF ZERO TO OUTPUT STRING                      32327300
06DE   0E02 72F0          2731  PUSHP    LINK  SET.RTN                SET INTERRUPT RETURN                   32327310
                          2732  *                                      IF FAULT, RETRY FROM PREVIOUS BYTE     32327320
06DF   006E 0170          2733           L     SR,NULL                DATA '00'                              32327330
06E0   0E00 6E30          2734           B     PUSH                                                          32327340

06E1   0E02 72F0          2736  PUSHU    LINK  SET.RTN                SET INTERRUPT RETURN                   32327360
                          2737  *                                      IF FAULT, RETRY FROM PREVIOUS BYTE     32327370
06E2   006E 8030          2738           LI    SR,'30'                DATA '30'                              32327380

06E3   0E02 6C00          2740  PUSH     LINK  PMVFLAGS               GET QUEUED FLAGS                       32327400
06E4   006A 8004          2741           LI    YDI,4                                                         32327410
06E5   046C 0081          2742           L     NULL,ARSYD,CYD&SWA     LEN1 EXHAUSTED ?                       32327420
06E6   DE0A 5B92          2743  PUSH.1   LINKF L,STORBYTE,YDP1+IR     BRANCH: NO.                            32327430
06E7   0418 3080          2744           S     ARSYD,MR3,ARSYD        DECREMENT LEN1 BY 1 IN R4              32327440
06E8   0F40 5E61          2745           BF    INT,PUSH.1,CYD&SWA     LOOP UNLESS                            32327450
06E9   5E00 7340          2746           B     INTRPTS,ENACLK         SERVICE ANY INTERRUPT.                 32327460
                          2747  *                                      IF NOT ERROR, COUNT HAS DECREMENTED.   32327470
```

STRING INSTRUCTIONS

```
                                2749  * ROUTINES TEST INPUT DATA FOR ZERO WHEN LEN2 >=0, LEN1 <0.          32327490
                                2750  FLUSHP  EQU   *                 CALLED BY PMV. FLUSHES INPUT DATA.    32327500
0000 06EA                       2751          LINK  PMVFLAGS          COLLECT QUEUED FLAGS                  32327510
06EA   0E02 6C00                2752          L     NULL,SR           TEST CURRENT DATA                     32327520
06EB   006C 00D0                2753          BT    G+L,ADDCC4,CYD&SWA BRANCH: OVERFLOW CASE.               32327530
06EC   0C18 22D1                2754          LI    ARSYD,'0F'        BYTE MASK TO R0                       32327540
06ED   0468 800F                2755          B     FLUSH                                                   32327550
06EE   0E00 6F30
                                2757  FLUSHU  EQU   *                 CALLED BY UMV. FLUSHES INPUT DATA.    32327570
0000 06EF                       2758          LINK  PMVFLAGS          COLLECT QUEUED FLAGS                  32327580
06EF   0E02 6C00                2759          L     NULL,MR2          TEST CURRENT DATA                     32327590
06F0   006C 0020                2760          BT    G+L,ADDCC4,CYD&SWA BRANCH: OVERFLOW CASE.               32327600
06F1   0C18 22D1                2761          LI    ARSYD,'FF'        BYTE MASK TO R0                       32327610
06F2   0468 80FF
                                2763  FLUSH   LINK  SET.RTN           SET INTERRUPT RETURN                  32327630
06F3   0E02 72F0                2764          L     MR0,NULL,LYSI     FOR DECREMENT; SELECT R0 AS YS        32327640
06F4   0060 017F                2765          L     NULL,ARSYD        LEN2 > 0 IN R5 ?                      32327650
06F5   046C 0080                2766  FLUSH.1 LINKT G,GETBYTE,IR      BRANCH: MORE DATA.                    32327660
06F6   DC12 6AF0                2767          N     MR0,SR,ARSYS      TEST INPUT DATA WITH MASK (R0)        32327670
06F7   0420 6090                2768          BT    G+L,ADDCC4        BRANCH: OVERFLOW CASE.                32327680
06F8   0C18 22D0                2769          SDEC  ARSYD,MR0,ARSYD   DECREMENT LEN2 BY 1 IN R5             32327690
06F9   0418 0085                2770          BF    INT,FLUSH.1                                             32327700
06FA   0F40 6F60                2771          B     INTRPT5,ENACLK    SERVICE ANY INTERRUPT                 32327710
06FB   5E00 7340
```

STRING INSTRUCTIONS

```
                        2773  * FOR THE FOLLOWING UNPACK ROUTINES, THE FOLLOWING CONVENTIONS HOLD:    32327730
                        2774  * ALL: AT INPUT, STRING LENGTHS ONE GREATER THAN SPECIFIED IN           32327740
                        2775  *                THE USER-LEVEL INSTRUCTION ARE ASSUMED. NO            32327750
                        2776  *                MAXIMUM IS IMPOSED. UNPACK PROCEEDS RIGHT-TO-LEFT.    32327760
                        2777  *                AN ODD NUMBER OF PACKED DATA DIGITS IS ALWAYS         32327770
                        2778  *                PROCESSED.                                            32327780
                        2780  *                NO INTERRUPT RESULTS FROM AN INVALID SIGN OR          32327800
                        2781  *                DATA DIGIT.                                           32327810
                        2783  *                STANDARD SIGN DIGITS 'C' OR 'D' ARE PRODUCED.         32327830
                        2784  *                A STRING REPRESENTING ZERO HAS SIGN DIGIT 'C'.        32327840

0000 06FC               2786  UMV     EQU   *                    (8C/04)                            32327860
0000 06FC               2787  UMVA    EQU   *                    (8C/24)                            32327870
06FC   5E02 72F0        2788          LINK  SET.RTN,ENACLK       SET INTERRUPT RETURN IN R11        32327880
06FD   006A 8003        2789          LI    YDI,3                                                   32327890
06FE   04E8 0170        2790          L     ARSYD,NULL,JAM       PRESET FLAGS = 0                   32327900
06FF   0E02 6B03        2791          LINK  GETBYT.1,YDM1        GET SIGNED BYTE @ (STR2+LEN2)      32327910
0700   0060 0020        2792          L     MR0,MR2              SIGN DIGIT, FORM 0000000S          32327920
0701   0E02 6CD0        2793          LINK  SGN.CHK              CHECK (MR0) FOR VALID SIGN DIGIT   32327930
0702                    2794          DO    4                    GET MR0:SR IN FORM 00000000:S000000D 32327940
0702   0060 0E0C        2795          SRL   MR0,MR0,DWSHFT       .                                  32327950
0703   0060 0E0C        2795          SRL   MR0,MR0,DWSHFT       .                                  32327950
0704   0060 0E0C        2795          SRL   MR0,MR0,DWSHFT       .                                  32327950
0705   0060 0E0C        2795          SRL   MR0,MR0,DWSHFT       .                                  32327950
0706   0062 08D0        2796          LHL   MR2,SR               MR2 = DATA DIGIT, FORM 0000000D    32327960
0707   0E02 6C70        2797          LINK  DIGITCK              CHECK (MR2) FOR VALID DECIMAL      32327970
0708   003E 6CD0        2798          O     SR,SR,SR,EXH         DATA, FORM S00DS00D                32327980
0709   003E 64D1        2799          O     SR,SR,SR,EXB+CYD&SWA DATA, FORM S00DSDSD                32327990
070A   0E02 6B92        2800          LINK  STORBYTE,YDP1        STORE IN OUTPUT STRING @(STR1+LEN1) 32328000
070B   0418 3082        2801          S     ARSYD,MR3,ARSYD,YDP1 DECREMENT LEN1 BY 1 IN R4          32328010
070C   0418 3080        2802          S     ARSYD,MR3,ARSYD      DECREMENT LEN2 BY 1 IN R5          32328020
070D   0E02 72F0        2803          LINK  SET.RTN              SET NEW INTERRUPT RETURN           32328030
                        2804  *                                  IF FAULT, RETRY FROM SIGNED BYTE.  32328040
070E   0060 8001        2805          LI    MR0,1                CONSTANT                           32328050

0000 070F               2807  UMVLP1  EQU   *                    UNPACK DATA BYTES                  32328070
                        2808  *                                  OPERATES FROM RIGHT TO LEFT        32328080
070F   046C 0081        2809          L     NULL,ARSYD,CYD&SWA   LEN2 < 0  IN R5 ?                  32328090
0710   0C08 6E12        2810          BT    L,PUSHU,YDP1         BRANCH: YES. OUTPUT '30'.          32328100
0711   0E02 6B02        2811          LINK  GETBYT.1,YDP1        GET BYTE @(STR2+LEN2)              32328110
0712   0E02 6C70        2812          LINK  DIGITCK              CHECK (LOW) DIGIT FOR VALID DECIMAL 32328120
0713   0456 0081        2813          L     MAR,ARSYD,CYD&SWA    LEN1 < 0 ? USING R4.               32328130
0714   0E08 7172        2814          BF    L,UMVLP2,YDP1        BRANCH: MORE TO DO.                32328140
0715   0062 00D0        2815          L     MR2,SR               COPY BOTH DIGITS TO MR2 FOR FLUSH  32328150
0716   0E00 6EF0        2816          B     FLUSHU               GO CHECK FOR ZERO DATA REMAINING.  32328160
0717   003E A030        2817  UMVLP2  OI    SR,MR2,'30'          APPEND ZONE                        32328170
0718   0406 4062        2818          A     MAR,ARSYD,MAR,YDP1   A(BYTE), USING R1                 32328180
0719   0065 04D2        2819          EXB   MDR,SR,YDP1          POSITION BYTE                      32328190
071A   1062 0E32        2820          SRL   MR2,MR3,DW1+YDP1     HIGH (PACKED) DIGIT TO MR2         32328200
071B   0E18 7200        2821          BF    G+L,UMVLP3           BRANCH: NEED NOT PROCESS ZERO DIGIT 32328210
071C   0062 0E20        2822          SRL   MR2,MR2              POSITION                           32328220
```

STRING INSTRUCTIONS

```
071D  0062 0E20          2823           SRL   MR2,MR2                .                                  32328230
071E  0062 0E20          2824           SRL   MR2,MR2                .                                  32328240
071F  0E02 5C83          2825           LINK  DIGITCK1,YDM1          CHECK (MR2) FOR VALID DECIMAL      32328250
0720  0413 0081          2826  UMVLP3   S     MR3,MR0,ARSYD,CYD&SWA  (LEN1-1) USING R4                  32328260
0721  0C08 6EF2          2827           BT    L,FLUSHU,YDP1          BRANCH: LEN1 EXHAUSTED.            32328270
0722  0406 3080          2828           A     MAR,MR3,ARSYD          A(STR1) + (LEN1-1), USING R1       32328280
0723  003E A030          2829           OI    SR,MR2,'30'            APPEND ZONE                        32328290
0724  0065 04D0          2830           EXB   MDR,SR                 POSITION OUTPUT BYTE               32328300
0725  106A 8005          2831           LI    YDI,5,DW1              STORE ZONED BYTE                   32328310
0726  0418 0083          2832           S     ARSYD,MR0,ARSYD,YDM1   DECREMENT LEN2 BY 1 IN R5          32328320
0727  0418 0085          2833           SDEC  ARSYD,MR0,ARSYD        DECREMENT LEN1 BY 2 IN R4          32328330
0728  0F40 70F2          2834           BF    INT,UMVLP1,YDP1        LOOP, UNLESS                       32328340
0729  5E00 7340          2835           B     INTRPT5,ENACLK         SERVICE ANY INTERRUPT.             32328350
```

STRING INSTRUCTIONS

```
                        2837  * THIS ROUTINE RESUMES AN INTERRUPTED STRING INSTRUCTION.                32328370
                        2838  * FOR THIS PROCESSOR, PSW BIT 14 IS SET ONLY WHEN SUSPENDING             32328380
                        2839  * A STRING INSTRUCTION TO SERVICE AN INTERRUPT. THIS BIT IS              32328390
                        2840  * ZERO DURING EXECUTION OF THE INSTRUCTION.                              32328400

0000 072A               2842  IIPRESUM EQU   *                    RESUME INTERRRUPTED INSTRUCTION      32328420
072A   00C7 FC02        2843          XI     PSW,PSW,'02',EXH+JAM ZERO IIP BIT                         32328430
072B   006A 800B        2844          LI     YDI,11               ARS R11 HAS INTERRUPT RETURN -       32328440
072C   046C 008E        2845          L      NULL,ARSYD,LLINK     GET IT,                              32328450
072D   006A 8005        2846          LI     YDI,5                POINT R5,                            32328460
072E   0E01 00E0        2847          RETN                        AND RESUME.                          32328470


                        2849  * THESE ROUTINES ESTABLISH THE CONTROL STORE ADDRESS AT WHICH            32328490
                        2850  * AN INTERRUPTED STRING INSTRUCTION IS TO BE RESUMED, AND                32328500
                        2851  * PERFORM NECESSARY PSW AND LOC ADJUSTMENT PRIOR TO SERVICING            32328510
                        2852  * ANY INTERRUPT.                                                        32328520

0000 072F               2854  SET.RTN  EQU   *                    SET INTERRUPT RETURN ADDRESS         32328540
072F   006A 800B        2855          LI     YDI,11                                                    32328550
0730   0468 00E0        2856          L      ARSYD,LR             COPY LINK ADDRESS                    32328560
0731   006A 8005        2857          LI     YDI,5                POINT R5,                            32328570
0732   5F41 00E0        2858          RETNF  INT,ENACLK           RETURN IF NO INTERRUPT               32328580

0000 0733               2860  INTRPT7  EQU   *                    MEMORY WAS READING AT INTERRUPT      32328600
0733   506C 0050        2861          L      NULL,MDR,ENACLK                                           32328610

                        2863  INTRPT5  EQU   *                    AN INTERRUPT MUST BE SERVICED.       32328630
0000 0734               2864          OI     PSW,PSW,'02',EXH+JAM SET IIP BIT                          32328640
0734   00B7 FC02        2865  INTRPT3  EQU   *                    ENTER HERE FROM RDCS/WDCS            32328650
0000 0735               2866          LINKF  MAT+MPE,MINUSLEN,IR IF NOT ERROR, POINT LOC BACK HERE    32328660
0735   DEB2 0FC0        2867  *                                  FOR ERROR, DECREMENTS LATER.         32328670

0736   0E04 0130        2868          B      EXIT,IVJE            OPEN INTERRUPT WINDOW.               32328680
```

STRING INSTRUCTIONS

```
                        2870  * FOR THE FOLLOWING LPB ROUTINE, THE FOLLOWING CONVENTIONS HOLD:          32328700
                        2871  *          THE PACKED DECIMAL STRING IS ASSUMED TO BE OF LENGTH          32328710
                        2872  *          16 BYTES, CONTAINING 31 DATA DIGITS AND A TRAILING            32328720
                        2873  *          SIGN DIGIT.                                                  32328730

                        2875  *          LEGAL DATA DIGITS ARE ALL BCD DIGITS 0 THROUGH 9.            32328750
                        2876  *          LEGAL POSITIVE SIGN DIGITS ARE 3, A, C, E, F.                32328760
                        2877  *          LEGAL NEGATIVE SIGN DIGITS ARE B, D.                         32328770
                        2878  *          A STRING REPRESENTING ZERO MAY HAVE EITHER A POSITIVE        32328780
                        2879  *          OR NEGATIVE SIGN DIGIT.                                      32328790

                        2881  *          IF CONVERSION OF THE PACKED DECIMAL NUMBER RESULTS            32328810
                        2882  *          IN ARITHMETIC OVERFLOW, THE DESTINATION REGISTERS             32328820
                        2883  *          ARE UNCHANGED, BUT NO INTERRUPT OCCURS.                      32328830

                        2885  *          IF AN INVALID SIGN DIGIT IS ENCOUNTERED, A DATA              32328850
                        2886  *          FORMAT FAULT, REASON = 2, OCCURS.                            32328860

                        2888  *          IF AN INVALID DATA DIGIT IS ENCOUNTERED, A DATA              32328880
                        2889  *          FORMAT FAULT, REASON = 3, OCCURS.                            32328890

                        2891  *          THE LARGEST NUMBER THAT MAY BE PROCESSED IS                  32328910
                        2892  *          +/- 9 223 372 036 854 775 807.                               32328920

0000 0737               2894  LPB   EQU  *                    ENTERED VIA DROM1          * 6F *  32328940
0737   0060 00A0        2895        L    MR0,YDI              SAVE ENTRY YD SELECT                 32328950
0738   002A FC02        2896        NI   YDI,PSW,'02',EXH     TEST IIP BIT                         32328960
0739   0C18 72A0        2897        BT   G+L,IIPRESUM         BRANCH: INSTRUCTION IN PROGRESS.     32328970
073A   0468 0003        2898        L    ARSYD,MR0,YDM1       YD SELECT TO R0                      32328980
073B   04E8 0173        2899        L    ARSYD,NULL,JAM+YDM1  ZERO CC, ACCUMULATOR R15            32328990
073C   0468 0173        2900        L    ARSYD,NULL,YDM1      AND R14.                             32329000
073D   0468 0063        2901        L    ARSYD,MAR,YDM1       A(STRING) TO R13                     32329010
073E   0468 8010        2902        LI   ARSYD,16             R12 COUNT = (31 DIGITS+SIGN)/2       32329020
073F   0418 4170        2903        S    ARSYD,ARSYD,NULL     2'S COMPLEMENT COUNT                 32329030
                        2904  *                               ONLY 19 DIGITS MAY CONTAIN DATA      32329040
0740   5E02 72F0        2905        LINK SET.RTN,ENACLK       SET INTERRUPT RETURN IN R11          32329050
0741   006A 800D        2906        LI   YDI,13                                                    32329060
0742   0466 0080        2907        L    MAR,ARSYD            A(OPERAND BYTE) FROM R13             32329070
0743   B061 80FF        2908        LI   MR1,'FF',DR2         MASK; FETCH DATA                     32329080

0000 0744               2910  LPB1  EQU  *                                                        32329100
0744   0022 145F        2911        N    MR2,MR1,MDR,EXB+LYSI EXTRACT DATA; YSI HOLDS LS DIGIT     32329110
0745   0E18 74A3        2912        BF   G+L,LPB1A,YDM1       BRANCH: ZERO DATA NEED NOT SHIFT.    32329120
0746   0062 0E20        2913        SRL  MR2,MR2              GET MS DIGIT OF BYTE                 32329130
0747   0062 0E20        2914        SRL  MR2,MR2              .                                    32329140
0748   0062 0E20        2915        SRL  MR2,MR2              .                                    32329150
0749   0062 0E20        2916        SRL  MR2,MR2              .                                    32329160
074A   0408 4175        2917  LPB1A AINC ARSYD,ARSYD,NULL     INCREMENT COUNT IN R12               32329170
074B   0E08 7542        2918        BF   L,LPB2,YDP1          BRANCH: SIGN NIBBLE COMING           32329180
074C   0408 4175        2919        AINC ARSYD,ARSYD,NULL     INCREMENT A(STRING) IN R13           32329190
074D   0466 0080        2920        L    MAR,ARSYD            READY FOR FETCH                      32329200
074E   0E02 76B1        2921        LINK TENXPLUS,CYD&SWA     GET (ACCUMULATOR*10)+(MR2)           32329210
074F   0062 00B0        2922        L    MR2,YSI              LS DIGIT OF BYTE                     32329220
```

STRING INSTRUCTIONS

```
0750   0E02 76B1          2923           LINK  TENXPLUS,CYD&SWA    GET (ACCUMULATOR*10)+(MR2)                32329230
0751   B06A 800D          2924           LI    YDI,13,DR2          FETCH NEXT BYTE                           32329240
0752   0F40 7440          2925           BF    INT,LPB1            LOOP, UNLESS INTERRUPT                    32329250
0753   5E00 7330          2926           B     INTRPT7,ENACLK      SERVICE INTERRUPT                         32329260

0000 0754                 2928  LPB2     EQU   *                   PROCESS SIGN NIBBLE, DO OUTPUT            32329280
0754   0E02 76B1          2929           LINK  TENXPLUS,CYD&SWA    GET (ACCUMULATOR*10)+(MR2)                32329290
0755   0062 00E0          2930           L     MR2,YSI             MR2 = SIGN DIGIT                          32329300
0756   5CB0 7341          2931           BT    MAT+MPE,INTRPT5,ENACLK+CYD&SWA SERVICE ONLY ERROR             32329310
                          2932  *                                 RETRY IS FROM FAULTED BYTE                32329320
0757   004C A003          2933           XI    NULL,MR2,'03'       POSITIVE SIGN ?                           32329330
0758   0E18 7633          2934           BF    G+L,PLUSBIN,YDM1    RECOGNIZE '03' AS POSITIVE                32329340
0759   001C A009          2935           SI    NULL,MR2,'09'       VALID SIGN ?                              32329350
075A   0E40 0E90          2936           BF    C,FORFAUL2          BRANCH: INVALID SIGN DIGIT, PACKED.       32329360
075B   004C A00B          2937           XI    NULL,MR2,'0B'       MINUS ?                                   32329370
075C   0E18 75F0          2938           BF    G+L,MINUSBIN        BRANCH: IS 'B'                            32329380
075D   004C A00D          2939           XI    NULL,MR2,'0D'       MINUS ?                                   32329390
075E   0C18 7630          2940           BT    G+L,PLUSBIN         BRANCH: NOT 'D'                           32329400
0000 075F                 2941  MINUSBIN EQU   *                                                             32329410
075F   0418 4173          2942           S     ARSYD,ARSYD,NULL,YDM1 COMPLEMENT (R15)                        32329420
0760   0E40 7620          2943           BF    C,MINB1             BRANCH: NO CARRY PROPAGATE                32329430
0761   0408 C001          2944           AI    ARSYD,ARSYD,1       PROPAGATE FOR A 'BORROW'                  32329440
0762   0418 4172          2945  MINB1    S     ARSYD,ARSYD,NULL,YDP1 COMPLEMENT R14                          32329450

                          2947  PLUSBIN  EQU   *                                                             32329470
0000 0763                 2948           L     MR3,ARSYD,YDM1      LS DATA FROM R15                          32329480
0763   0463 0083          2949           L     MR1,ARSYD,CYD&SWA   MS DATA FROM R14                          32329490
0764   0461 0081          2950           AI    YDI,ARSYD,1         FIGURE  ENTRY R1+1 FROM R0                32329500
0765   040A C001          2951           L     YD,MR3,YDM1         LS HALF OUTPUT DATA                       32329510
0766   0068 0033          2952           L     YD,MR1,JAM          MS HALF OUTPUT DATA                       32329520
0767   00E8 0010          2953           BF    G+L,*+1,IR          EXIT IF MS HALF SETS G OR L               32329530
0768   DE18 7690          2954           L     NULL,MR3,JAM        ELSE TEST LS HALF SIGNIFICANCE            32329540
0769   00EC 0030          2955           BT    L,SETCC2,IR         EXIT IF CC = 2 OR 0.                      32329550
076A   DC08 2270
```

STRING INSTRUCTIONS

```
0000 076B                    2958  TENXPLUS EQU   *                    ACCUMULATES BCD AS BINARY.          32329580
                             2959  * LARGEST NUMBER IS:   +9 223 372 036 854 775 807.                      32329590
                             2960  *                                                                       32329600
076B   001C A009             2961          SI     NULL,MR2,'09'        VALID DECIMAL DIGIT IN MR2 ?        32329610
076C   0C40 0EA0             2962          BT     C,FORFAUL3           BRANCH: INV DATA DIGIT, PACKED.     32329620
076D   043F 2480             2963          O      FLR,MR2,ARSYD,EXB    ANY NON-ZERO DATA YET (USING R0) ?  32329630
076E   0E79 00E0             2964          RETNF  C+V+G+L              BRANCH: ACCUMULATOR, DATA ZERO      32329640
076F   0438 4423             2965          O      ARSYD,ARSYD,MR2,EXB+YDM1 ACCUMULATE CURRENT DATA         32329650
0770   046E 0083             2966          L      SR,ARSYD,YDM1        GET LS HALF FROM R15                32329660
0771   0468 0A8C             2967          SLL    ARSYD,ARSYD,DWSHFT   (ARS R14:SR)*2                    32329670
0772   0C48 7810             2968          BT     C+L,TENXOVF          BRANCH: OVERFLOW.                   32329680
0773   0460 0080             2969          L      MR0,ARSYD            REMEMBER MS HALF,                   32329690
0774   0065 00D0             2970          L      MDR,SR               LS HALF OF (*2)                     32329700
0775   0468 0A8C             2971          SLL    ARSYD,ARSYD,DWSHFT   (ARS R14:SR)*4                    32329710
0776   0468 0A8C             2972          SLL    ARSYD,ARSYD,DWSHFT   (ARS R14:SR)*8                    32329720
0777   0C48 7812             2973          BT     C+L,TENXOVF,YDP1     BRANCH: OVERFLOW                    32329730
0778   0408 6050             2974          A      ARSYD,SR,MDR         ADD TO MAKE (*10) LOW HALF          32329740
0779   0E40 77B3             2975          BF     C,TENXPL1,YDM1       POINT TO R14                        32329750
077A   0408 C001             2976          AI     ARSYD,ARSYD,1        PROPAGATE CARRY                     32329760
077B   0408 0082             2977  TENXPL1 A      ARSYD,MR0,ARSYD,YDP1 ADD TO MAKE (*10) HIGH HALF         32329770
077C   0C48 7810             2978          BT     C+L,TENXOVF          BRANCH: OVERFLOW                    32329780
077D   0408 4020             2979          A      ARSYD,ARSYD,MR2      ADD NEW DIGIT                       32329790
077E   0E41 00E3             2980          RETNF  C,YDM1               RETURN IF NO CARRY PROP             32329800
077F   0408 C001             2981          AI     ARSYD,ARSYD,1        PROPAGATE CARRY                     32329810
0780   0E49 00E0             2982          RETNF  C+L                  RETURN IF NO OVERFLOW.              32329820
                             2983  *                                                                       32329830
0781   D0EF 8004             2984  TENXOVF LI     FLR,4,IR+JAM         SET CC = 4, EXIT.                   32329840
```

STRING INSTRUCTIONS

```
                        2986  * FOR THE FOLLOWING STBP INSTRUCTION, THE FOLLOWING CONVENTIONS APPLY:  32329860
                        2987  *              ANY BINARY NUMBER WHICH MAY BE CONTAINED IN 64           32329870
                        2988  *              BITS MAY BE CONVERTED TO DECIMAL AND OUTPUT TO           32329880
                        2989  *              A PACKED DECIMAL STRING, OF LENGTH 16 BYTES.             32329890
                        2990  *              THIS STRING CONSISTS OF 31 BCD DATA DIGITS, FOLLOWED     32329900
                        2991  *              BY A SIGN DIGIT.                                        32329910
                        2993  *              THE SIGN DIGIT IS 'C' FOR ZERO OR POSITIVE DATA,        32329930
                        2994  *              AND 'D' FOR NEGATIVE DATA.                              32329940

0000 0782               2996  STBP     EQU   *                 ENTERED VIA DROM1            * 6E * 32329960
0782   0063 00A0        2997           L     MR3,YDI           SAVE ENTRY YD SELECT                   32329970
0783   002A FC02        2998           NI    YDI,PSW,'02',EXH  TEST IIP BIT                          32329980
0784   0C18 72A2        2999           BT    G+L,IIPRESUM,YDP1 BRANCH: IN PROGRESS. POINT R1          32329990
0785   0468 0063        3000           L     ARSYD,MAR,YDM1    WORKING ADDRESS TO P1                  32330000
0786   006B 8005        3001           LI    CNTR,5                                                   32330010
0787   0468 0173        3002           L     ARSYD,NULL,YDM1   CLEAR ACCUMULATOR (R12:13:14:15)       32330020

0788   000A B001        3004           AI    YDI,MR3,1         SELECT INPUT R1+1                      32330040
0789   006E 0083        3005           L     SR,YD,YDM1        LS HALF INPUT DATA                     32330050
078A   00E1 0081        3006           L     MR1,YD,CYD&SWA+JAM MS HALF INPUT DATA SETS CC            32330060
                        3007  *                               CC USED TO GENERATE SIGN DIGIT.        32330070
078B   0E08 7912        3008           BF    L,STBP.POS,YDP1   BRANCH: ALREADY 'POSITIVE'; POINT R1  32330080
0000 078C               3009  STBP.NEG EQU   *                 MUST 2'S COMPLEMENT                    32330090
078C   001E 6170        3010           S     SR,SR,NULL        COMPLEMENT LOW HALF                    32330100
078D   0E40 78F0        3011           BF    C,STBP.N1         BRANCH: NO CARRY PROP                  32330110
078E   0001 9001        3012           AI    MR1,MR1,1         PROPAGATE FOR A 'BORROW'               32330120
078F   0011 1170        3013  STBP.N1  S     MR1,MR1,NULL      COMPLEMENT HIGH HALF                   32330130
0790   0E00 7940        3014           B     STBP.001                                                 32330140

0791   003C 10D0        3016  STBP.POS O     NULL,MR1,SR       ANY POSITIVE DATA ?                    32330160
0792   0E18 7D42        3017           BF    G+L,STBP.ZIP,YDP1 BRANCH: "FAST EXIT" FOR ZERO.          32330170
0793   00EF 8002        3018           LI    FLR,2,JAM         SET CC = 2                             32330180

0000 0794               3020  STBP.001 EQU   *                 CONVERT TO BASE (10**8)                32330200
0794   006A 8007        3021           LI    YDI,7                                                    32330210
0795   0468 00D3        3022           L     ARSYD,SR,YDM1     LS HALF POS DATA (W2) TO R7            32330220
0796   0468 0173        3023           L     ARSYD,NULL,YDM1   ZERO TO R6                            32330230
0797   0468 0013        3024           L     ARSYD,MR1,YDM1    MS HALF POS DATA (W1) TO R5            32330240
0798   0468 0170        3025           L     ARSYD,NULL        ZERO TO R4                             32330250
0799   5D42 72F0        3026           LINKT INT,SET.RTN,ENACLK GET INTERRUPT RETURN TO R11           32330260

079A   006A 8003        3028           LI    YDI,3             R3 TO HOLD DIVISOR, 10                 32330280
079B   0062 800A        3029           LI    MR2,'0A'          BUILD 'FA0A1F00' CONSTANT = 10**8      32330290
079C   0418 2172        3030           S     ARSYD,MR2,NULL,YDP1 DIVISOR TO R3, 2'S COMP FORM         32330300
079D   0032 A4FA        3031           OI    MR2,MR2,'FA',EXB  CONTINUE BUILDING CONSTANT             32330310
079E   0062 0C22        3032           EXH   MR2,MR2,YDP1      .                                      32330320
079F   0032 A41F        3033           OI    MR2,MR2,'1F',EXB  AND WE HAVE IT.                        32330330
                        3034  *                               YDI = 5, POINTS TO SAVED DATA (W1)     32330340
07A0   0E02 7EB0        3035           LINK  DIVIDE            DIVIDE (0:W1) IN (R4:R5) BY            32330350
                        3036  *                               (10**8) IN MR2.                        32330360
                        3037  *                               RETURNS (RE1:Q1) IN (R4:R5)            32330370
07A1   006C 00AF        3038           L     NULL,YDI,LYSI     SELECT R4 AS YS                        32330380
```

STRING INSTRUCTIONS

```
07A2   046C 0090          3039           L     NULL,ARSYS          TO DO ARITHMETIC COMPARE:                  32330390
07A3   0C08 7A72          3040           BT    L,STBP.002,YDP1     BRANCH: NEGATIVE LESS THAN (10**8)/2       32330400
                          3041  *                                   POINT R5.                                  32330410
07A4   040C 5F20          3042           A     NULL,ARSYS,MR2,SRA  COMPARE RE1:(10**8)/2 USING R4            32330420
                          3043  *                                   REMEMBER, MR2 HAS A NEGATIVE NUMBER.       32330430
07A5   0C08 7A70          3044           BT    L,STBP.002          BRANCH: RE1 < COMPARAND.                   32330440
07A6   0409 2090          3045           A     ARSYS,MR2,ARSYS     GET (RE1-10**8), AVOID O'FLOW, R4          32330450
0000 07A7                 3046  STBP.002 EQU   *                                                              32330460
07A7   0465 0082          3047           L     MDR,ARSYD,YDP1      SAVE Q1 TO USE BELOW - POINT R6            32330470
07A8   0468 0090          3048           L     ARSYD,ARSYS         LOAD R6 WITH RE1 FROM R4                   32330480
07A9   0E02 7EB2          3049           LINK  DIVIDE,YDP1         DIVIDE (RE1:W2) IN (R6:R7) BY              32330490
                          3050  *                                   (10**8) IN MR2.                            32330500
                          3051  *                                   RETURNS (RE2:Q2) IN (R6:R7)                32330510
                          3052  STBP.003 EQU   *                                                              32330520
0000 07AA                 3053           L     MR3,ARSYD           RE2 FROM R6                                32330530
07AA   0463 0080          3054           BF    L,STBP.004          IF NEGATIVE, NEEDS CORRECTION              32330540
07AB   0E08 7AF0          3055           S     MR3,MR2,ARSYD       RE2 + (10**8) USING R6                     32330550
07AC   0413 2080          3056           LI    MR1,1                                                          32330560
07AD   0061 8001          3057           S     SR,MR1,SR           Q2 - 1 IN SR                               32330570
07AE   001E 10D0          3058  STBP.004 EQU   *                                                              32330580
0000 07AF                 3059           L     ARSYD,MDR           SAVED Q1 TO R6                             32330590
07AF   0468 0050          3060           LINK  DIVIDE1             DIVIDE (Q1:Q2) IN (R6:SR) BY 10**8         32330600
07B0   0E02 7EC0          3061  *                                   RETURNS (RE3:Q3) IN (R6:R7).               32330610
                          3062           L     MDR,ARSYD           MOVE (RE3:Q3) TO (R14,R13)                 32330620
07B1   0465 0080          3063           LI    YDI,15                                                         32330630
07B2   006A 800F          3064           L     ARSYD,MR3,YDM1      RE2 TO R15                                 32330640
07B3   0468 0033          3065           L     ARSYD,MDR,YDM1      RE3 TO R14                                 32330650
07B4   0468 0053          3066           L     ARSYD,SR,CYD&SWA    Q3 TO R13                                  32330660
07B5   0468 00D1          3067  * *                                 FOR '7FFF FFFF FFFF FFFF' INPUT,           32330670
                          3068  * *                                 R15 = 0343 CFFF                            32330680
                          3069  * *                                 R14 = 0202 8830                            32330690
                          3070  * *                                 R13 = 0000 039A                            32330700
07B6   0468 801F          3071           LI    ARSYD,31            COUNT FOR 31 DIGITS & SIGN TO R0           32330710
07B7   5D42 72F0          3072           LINKT INT,SET.RTN,ENACLK  SERVICE ANY INTERRUPT                      32330720
07B8   0061 80FF          3073           LI    MR1,'FF'            SET 'BYTE READY TO OUTPUT'                 32330730
07B9   0E00 7BC1          3074           B     STBPLP2,CYD&SWA     START DIGIT CONVERSION                     32330740
                          3076  STBPL2.1 LINK  STBPSTOR                                                       32330750
07BA   0E02 7D70          3077           L     MR1,NULL            OUTPUT LEAST SIGNIF DATA BYTE              32330760
07BB   0061 0170          3078  STBPLP2  EQU   *                   SET 'BYTE NOT READY'                       32330770
0000 07BC                 3079           L     MR2,NULL,CYD&SWA                                               32330780
07BC   0062 0171          3080           OI    SR,ARSYD,'E0'       SET MSB DIVIDEND = 0 FOR DIVIDE            32330790
07BD   043E C0E0          3081           SRL   SR,SR,YDP1          'SIGN-EXTEND' COUNT FROM R0                32330800
07BE   006E 0ED2          3082           SRL   SR,SR,YDP1          GET DATA REGISTER 12, 13, 14, OR 15        32330810
07BF   006E 0ED2          3083           L     ARSYD,NULL,YDP1     .                                          32330820
07C0   0468 0172          3084           L     MR0,ARSYD,CYD&SWA   PRE-ZERO OUTPUT REGISTER (R2)              32330830
07C1   0460 0081          3085  STBPLP2B EQU   *                   DIVISOR = 10 (2'S COMP)                    32330840
0000 07C2                 3086           SRL   SR,SR,LYSI          ENTERED VIA DROM2                          32330850
07C2   006E 0EDF          3087           L     SR,ARSYS,YDP1       GET DATA REGISTER 12, 13, 14, OR 15        32330860
07C3   046E 0092          3088           BF    G+L,STBPLP2C,YDP1   ACCESS DATA REGISTER                        32330870
07C4   0E18 7C92          3089  *                                   BRANCH: DATA ZERO. AVOID DIVIDE.           32330880
                          3090           LI    CNTR,32             (MR2:SR) = (0:ARGUMENT)                    32330890
07C5   006B 8020          3091           DIV   MR2,MR0,MR2         YDI CONTAINS 2 HERE.                       32330900
07C6   0002 0A27          3092  *                                   DIVIDE BY 10                               32330910
                                                                   RETURNS (REM:QUOT) IN (MR2:SR)             32330920
```

STRING INSTRUCTIONS

```
07C7   0438 2080          3093           O      ARSYD,MR2,ARSYD     APPEND CURRENT DECIMAL DIGIT TO R2   32330930
07C8   0469 00D0          3094           L      ARSYS,SR            RETAIN QUOTIENT IN DATA REGISTER    32330940
0000 07C9                 3095  STBPLP2C EQU    *                   ENTRY WHEN ZERO DIVIDEND            32330950
07C9   0041 90FF          3096           XI     MR1,MR1,'FF'        REVERSE FLAG                        32330960
07CA   0E18 7BA0          3097           BF     G+L,STBPL2.1        BRANCH: GOT A BYTE                  32330970
07CB   0062 017F          3098           L      MR2,NULL,LYSI       MSB DIVIDEND = 0 FOR DIVIDE; YSI = 0 32330980
07CC   041C D00C          3099           SI     NULL,ARSYS,12       ANY SIGNIFICANCE LEFT ?             32330990
07CD   0E40 7D60          3100           BF     C,STBP.Z1           BRANCH: NEED NOT CONVERT FURTHER.   32331000
07CE   041E 2095          3101           SDEC   SR,MR2,ARSYS        COMPUTE (COUNT-1)                   32331010
07CF   0468 0D8C          3102           RRL    ARSYD,ARSYD,DWSHFT  MOVE DIGIT FOR NEXT; SCALE COUNT   32331020
07D0   0468 0D8C          3103           RRL    ARSYD,ARSYD,DWSHFT  .                                   32331030
07D1   0468 0D80          3104           RRL    ARSYD,ARSYD         .                                   32331040
07D2   0468 0D81          3105           RRL    ARSYD,ARSYD,CYD&SWA .   POINT R0                        32331050
07D3   083E E0F8          3106           OI     SR,SR,'F8',D2       'SIGN EXTEND' COUNT, VECTOR STBPLP2B 32331060


0000 07D4                 3109  STBP.ZIP EQU    *                   'FAST EXIT' FOR ZERO                32331090
07D4   0468 0171          3110           L      ARSYD,NULL,CYD&SWA  ZERO OUTPUT REGISTER (R2)           32331100
07D5   0468 801F          3111           LI     ARSYD,31            COUNT FOR 31 DIGITS & SIGN TO R0    32331110
0000 07D6                 3112  STBP.Z1  EQU    *                                                       32331120
07D6   5D42 72F0          3113           LINKT  INT,SET.RTN,ENACLK  SERVICE ANY INTERRUPT               32331130


                          3115  * ROUTINE DECIDES IF SIGNED BYTE OR DATA BYTE. STORES BYTE              32331150
                          3116  * AT A(STRING)+(COUNT/2). EXITS WHEN COUNT EXHAUSTED.                   32331160
0000 07D7                 3117  STBPSTOR EQU    *                                                       32331170
07D7   006A 8002          3118           LI     YDI,2               SELECT OUTPUT REGISTER              32331180
07D8   046E 0981          3119           RLL    SR,ARSYD,CYD&SWA    ACCESS DATA                         32331190
07D9   0E18 7DD0          3120           BF     G+L,STBPS.0         BRANCH: ZERO DATA                   32331200
07DA   006E 09D0          3121           RLL    SR,SR               POSITION BYTE TO B24:31 AS REQ'D    32331210
07DB   006E 09D0          3122           RLL    SR,SR               .                                   32331220
07DC   006E 09D0          3123           RLL    SR,SR               .                                   32331230
07DD   044C C01F          3124  STBPS.0  XI     NULL,ARSYD,31       SIGNED BYTE ?                       32331240
07DE   0C18 7E30          3125           BT     G+L,STBPS.1         BRANCH: NO.                         32331250
0000 07DF                 3126  STBP.SGN EQU    *                   OUTPUT SIGNED BYTE                  32331260
07DF   0023 F001          3127           NI     MR3,PSW,'01'        CAPTURE CC L FLAG                   32331270
07E0   0033 B00C          3128           OI     MR3,MR3,'0C'        FORM SIGN DIGIT, '0C' OR '0D'       32331280
07E1   003E 30D0          3129           O      SR,MR3,SR           APPEND FIRST DATA DIGIT             32331290
07E2   0408 C001          3130           AI     ARSYD,ARSYD,1       SET COUNT TO 32 TEMPORARILY IN R0   32331300
0000 07E3                 3131  STBPS.1  EQU    *                   OUTPUT BYTE TO DEST'N STRING        32331310
07E3   0060 8001          3132           LI     MR0,1               CONSTANT                            32331320
07E4   0413 0082          3133           S      MR3,MR0,ARSYD,YDP1  GET (COUNT-1) FROM R0, POINT R1    32331330
07E5   0406 4E30          3134           A      MAR,ARSYD,MR3,SRL   COMPUTE A(STRING BYTE)             32331340
07E6   0065 04D1          3135           EXB    MDR,SR,CYD&SWA      POSITION BYTE TO OUTPUT             32331350
07E7   106C 0170          3136           L      NULL,NULL,DW1       STORE BYTE                          32331360
07E8   0418 0085          3137           SDEC   ARSYD,MR0,ARSYD     DECREMENT COUNT IN R0 BY 2          32331370
07E9   5D40 5E40          3138           BT     INT,STBPS.2,ENACLK  SERVICE ANY INTERRUPT              32331380
07EA   DC11 00E0          3139           RETNT  G,IR                RETURN IF COUNT STILL POSITIVE.     32331390
```

STRING INSTRUCTIONS

```
                        3142  * ROUTINES DO FULLWORD DIVISION. ASSUME NEGATIVE DIVISOR.                32331420
                        3143  * ROUTINE 'DIVIDE' EXPECTS YDI SELECTING ODD REGISTER                    32331430
                        3144  *   INPUT: (YD:YDP1)=DIVIDEND; MR2=DIVISOR                              32331440
                        3145  * ROUTINE 'DIVIDE1' EXPECTS YDI SELECTING EVEN REGISTER                   32331450
                        3146  *   INPUT: (YD:SR)=DIVIDEND; MR2=DIVISOR                                32331460
                        3147  * OUTPUT:YDP1=SR=QUOTIENT; YD=REMAINDER                                  32331470
                        3148  *                                                                        32331480
                        3149  * NOTE THAT SIGN ADJUSTMENT IMPOSED PRESUMES THAT THE POSITIVE          32331490
                        3150  * DIVISOR IS ALREADY NEGATED.  AS A RESULT, THE SIGN OF                 32331500
                        3151  * THE REMAINDER AND OF THE QUOTIENT ARE THE SAME AS THE SIGN            32331510
                        3152  * OF THE DIVIDEND.                                                      32331520

                                                                                                       32331540
07EB   046E 0083        3155          L     SR,ARSYD,YDM1       SR GETS LS INPUT DATA                32331550
                                                                                                       32331560
07EC   0460 0080        3157          L     MR0,ARSYD           CAPTURE SGN(DIVD) FROM MS HALF       32331570
07ED   0E08 7F20        3158          BF    L,DV001             BRANCH: ALREADY POSITIVE             32331580
07EE   001E 6170        3159          S     SR,SR,NULL          2'S COMPLEMENT LOW HALF              32331590
07EF   0E40 7F10        3160          BF    C,DV002             BRANCH: NO CARRY PROP                32331600
07F0   0408 C001        3161          AI    ARSYD,ARSYD,1       PROPAGATE FOR A 'BORROW'             32331610
07F1   0418 4170        3162  DV002   S     ARSYD,ARSYD,NULL    2'S COMPLEMENT HIGH HALF             32331620
07F2   0065 8020        3163  DV001   LI    CNTR,32                                                  32331630
07F3   0408 2A87        3164          DIV   ARSYD,MR2,ARSYD     DIVIDE (YD:SR) BY (MR2)              32331640
07F4   044C 0080        3165          X     NULL,MR0,ARSYD      SGN(REMAINDER) CORRECT ?             32331650
07F5   0E08 7F70        3166          BF    L,DV003             BRANCH: IS NOW SAME AS SGN(DIVIDEND).32331660
07F6   0418 4170        3167          S     ARSYD,ARSYD,NULL    2'S COMPLEMENT REMAINDER             32331670
07F7   004C 00D0        3168  DV003   X     NULL,MR0,SR         SGN(QUOTIENT) CORRECT ?              32331680
07F8   0E08 7FA2        3169          BF    L,DV004,YDP1        BRANCH: SGN(QUOTIENT) CORRECT.       32331690
07F9   001E 6170        3170          S     SR,SR,NULL          2'S COMPLEMENT QUOTIENT              32331700
07FA   0469 00D3        3171  DV004   L     ARSYD,SR,YDM1       ADJUSTED QUOTIENT. SELECT EVEN YD.   32331710
07FB   0E01 00E0        3172          BETN                      AND RETURN.                          32331720
```

FREE SPACE

```
07FC                        3175        IFP   '800'-*                    32331750
07FC                        3176        DO    '800'-*                    32331760
07FC   0000 0000            3177        DC    FREEWORD                   32331770
07FD   0000 0000            3177        DC    FREEWORD                   32331770
07FE   0000 0000            3177        DC    FREEWORD                   32331770
07FF   0000 0000            3177        DC    FREEWORD                   32331770
                            3178        ENDC                             32331780
```

DROM1 VECTOR TABLE & PRIV/ILEG TABLE

```
0000 40C2                3180  ILEG     EQU   IIINT+'4000'        ILLEGAL INSTRUCTION FLAG&VECTOR     32331800
0000 8000                3181  PRIV     EQU   '8000'              PRIVILEGED INSTRUCTION FLAG         32331810
0000 2000                3182  FLOAT    EQU   '2000'              FLOATING POINT INSTRUCTION FLAG     32331820
0000 1000                3183  WCSENA   EQU   '1000'              ENABLES WCS ACCESS ABOVE '7FF'      32331830

                         3185  * BITS 00:15 OF ROM WORDS SHOWN ARE NOT USED.                          32331850
                         3186  * BITS 16:19  CONTAIN THE FLAG INFORMATION FOR PRIV/ILLEGAL ROM        32331860
                         3187  *         PRIV/ILLEGAL ROM 19-188F27 SHOWN (WITH WCS).                 32331870
                         3188  *         PRIV/ILLEGAL ROM 19-188F25 (NO WCS) CONTAINS                 32331880
                         3189  *         X'4' FOR OPCODES E5, E8, AND E9.                             32331890
                         3190  * BITS 20:31 CONTAIN THE INSTRUCTION'S DROM1 ENTRY ADDRESS.            32331900
0800                     3191           ORG   WCSLO                                                   32331910

0800   0000 40C2         3193           DC    ILEG          00  --                                    32331930
0801   0000 0290         3194           DC    BALR          01  BALR                                  32331940
0802   0000 0293         3195           DC    BTCR          02  BTCR                                  32331950
0803   0000 0294         3196           DC    BFCR          03  BFCR                                  32331960
0804   0000 02B6         3197           DC    NR            04  NR                                    32331970
0805   0000 02B7         3198           DC    CLR           05  CLR                                   32331980
0806   0000 02BA         3199           DC    OR            06  OR                                    32331990
0807   0000 02BD         3200           DC    XR            07  XR                                    32332000
0808   0000 0319         3201           DC    LR            08  LR                                    32332010
0809   0000 02C6         3202           DC    CR            09  CR                                    32332020
080A   0000 02CC         3203           DC    AR            0A  AR                                    32332030
080B   0000 02CF         3204           DC    SR            0B  SR                                    32332040
080C   0000 02D0         3205           DC    MHR           0C  MHR                                   32332050
080D   0000 02DC         3206           DC    DHR           0D  DHR                                   32332060
080E   0000 40C2         3207           DC    ILEG          0E  --                                    32332070
080F   0000 40C2         3208           DC    ILEG          0F  --                                    32332080
                         3209  *                                                                      32332090
0810   0000 027C         3210           DC    SFSHFTF       10  SRLS                                  32332100
0811   0000 027C         3211           DC    SFSHFTF       11  SLLS                                  32332110
0812   0000 02AB         3212           DC    CHVR          12  CHVR                                  32332120
0813   0000 25CB         3213           DC    EVALU+FLOAT   13  LPER                                  32332130
0814   0000 40C2         3214           DC    ILEG          14  --                                    32332140
0815   0000 25A3         3215           DC    SWAP+FLOAT    15  LGER                                  32332150
0816   0000 25A3         3216           DC    SWAP+FLOAT    16  LGDR                                  32332160
0817   0000 25CB         3217           DC    EVALU+FLOAT   17  LCER                                  32332170
0818   0000 8120         3218           DC    LPSWR+PRIV    18  LPSWR                                 32332180
0819   0000 40C2         3219           DC    ILEG          19  --                                    32332190
081A   0000 40C2         3220           DC    ILEG          1A  --                                    32332200
081B   0000 40C2         3221           DC    ILEG          1B  --                                    32332210
081C   0000 02D6         3222           DC    MR            1C  MR                                    32332220
081D   0000 02F8         3223           DC    DR            1D  DR                                    32332230
081E   0000 40C2         3224           DC    ILEG          1E  --                                    32332240
081F   0000 40C2         3225           DC    ILEG          1F  --                                    32332250
                         3226  *                                                                      32332260
0820   0000 0295         3227           DC    BTBS          20  BTBS                                  32332270
0821   0000 0296         3228           DC    BTFS          21  BTFS                                  32332280
0822   0000 0297         3229           DC    BFBS          22  BFBS                                  32332290
0823   0000 0298         3230           DC    BFFS          23  BFFS                                  32332300
0824   0000 031A         3231           DC    LIS           24  LIS                                   32332310
0825   0000 031B         3232           DC    LCS           25  LCS                                   32332320
```

DROM1 VECTOR TABLE & PRIV/ILEG TABLE

```
0826  0000 02CD   3233          DC   AIS          26  AIS          32332330
0827  0000 02CE   3234          DC   SIS          27  SIS          32332340
0828  0000 2521   3235          DC   LER+FLOAT    28  LER          32332350
0829  0000 2522   3236          DC   CER+FLOAT    29  CER          32332360
082A  0000 2524   3237          DC   AER+FLOAT    2A  AER          32332370
082B  0000 2525   3238          DC   SER+FLOAT    2B  SER          32332380
082C  0000 2526   3239          DC   MER+FLOAT    2C  MER          32332390
082D  0000 2527   3240          DC   DER+FLOAT    2D  DER          32332400
082E  0000 2528   3241          DC   FXR+FLOAT    2E  FXR          32332410
082F  0000 254C   3242          DC   FLR+FLOAT    2F  FLR          32332420
                  3243  *                                         32332430
0830  0000 40C2   3244          DC   ILEG         30  --           32332440
0831  0000 40C2   3245          DC   ILEG         31  --           32332450
0832  0000 03E0   3246          DC   PBR          32  PBR          32332460
0833  0000 25D6   3247          DC   DVALU+FLOAT  33  LPDR         32332470
0834  0000 031F   3248          DC   EXHR         34  EXHR         32332480
0835  0000 40C2   3249          DC   ILEG         35  --           32332490
0836  0000 40C2   3250          DC   ILEG         36  --           32332500
0837  0000 25D6   3251          DC   DVALU+FLOAT  37  LCDR         32332510
0838  0000 2556   3252          DC   LDR+FLOAT    38  LDR          32332520
0839  0000 2557   3253          DC   CDR+FLOAT    39  CDR          32332530
083A  0000 2559   3254          DC   ADR+FLOAT    3A  ADR          32332540
083B  0000 255A   3255          DC   SDR+FLOAT    3B  SDR          32332550
083C  0000 255B   3256          DC   MDR+FLOAT    3C  MDR          32332560
083D  0000 255C   3257          DC   DDR+FLOAT    3D  DDR          32332570
083E  0000 255D   3258          DC   FXDR+FLOAT   3E  FXDR         32332580
083F  0000 254C   3259          DC   FLDR+FLOAT   3F  FLDR         32332590
                  3260  *                                         32332600
0840  0000 0363   3261          DC   STH          40  STH          32332610
0841  0000 0290   3262          DC   BAL          41  BAL          32332620
0842  0000 0293   3263          DC   BTC          42  BTC          32332630
0843  0000 0294   3264          DC   BFC          43  BFC          32332640
0844  0000 022F   3265          DC   RXH          44  NH           32332650
0845  0000 0230   3266          DC   RXH2         45  CLH          32332660
0846  0000 022F   3267          DC   RXH          46  OH           32332670
0847  0000 022F   3268          DC   RXH          47  XH           32332680
0848  0000 022F   3269          DC   RXH          48  LH           32332690
0849  0000 02BE   3270          DC   CH           49  CH           32332700
084A  0000 022F   3271          DC   RXH          4A  AH           32332710
084B  0000 0230   3272          DC   RXH2         4B  SH           32332720
084C  0000 0230   3273          DC   RXH2         4C  MH           32332730
084D  0000 022F   3274          DC   RXH          4D  DH           32332740
084E  0000 40C2   3275          DC   ILEG         4E  --           32332750
084F  0000 40C2   3276          DC   ILEG         4F  --           32332760
                  3277  *                                         32332770
0850  0000 0363   3278          DC   ST           50  ST           32332780
0851  0000 0233   3279          DC   RXF2         51  AM           32332790
0852  0000 40C2   3280          DC   ILEG         52  --           32332800
0853  0000 40C2   3281          DC   ILEG         53  --           32332810
0854  0000 0232   3282          DC   RXF          54  N            32332820
0855  0000 0233   3283          DC   RXF2         55  CL           32332830
0856  0000 0232   3284          DC   RXF          56  O            32332840
0857  0000 0232   3285          DC   RXF          57  X            32332850
0858  0000 0232   3286          DC   RXF          58  L            32332860
```

DROM1 VECTOR TABLE & PRIV/ILEG TABLE

```
0859  0000 02C2          3287          DC    C                   59  C          32332870
085A  0000 0232          3288          DC    RXF                 5A  A          32332880
085B  0000 0233          3289          DC    RXF2                5B  S          32332890
085C  0000 0233          3290          DC    RXF2                5C  M          32332900
085D  0000 0233          3291          DC    RXF2                5D  D          32332910
085E  0000 038C          3292          DC    CRC12               5E  CRC12      32332920
085F  0000 0390          3293          DC    CRC16               5F  CRC16      32332930
                         3294  *                                               32332940
0860  0000 2563          3295          DC    STE+FLOAT           60  STE        32332950
0861  0000 02A6          3296          DC    AHM                 61  AHM        32332960
0862  0000 03DB          3297          DC    PB                  62  PB         32332970
0863  0000 032C          3298          DC    LRA                 63  LRA        32332980
0864  0000 0238          3299          DC    ATL                 64  ATL        32332990
0865  0000 0248          3300          DC    ABL                 65  ABL        32333000
0866  0000 0259          3301          DC    RTL                 66  RTL        32333010
0867  0000 026B          3302          DC    RBL                 67  RBL        32333020
0868  0000 2232          3303          DC    RXF+FLOAT           68  LE         32333030
0869  0000 2232          3304          DC    RXF+FLOAT           69  CE         32333040
086A  0000 2232          3305          DC    RXF+FLOAT           6A  AE         32333050
086B  0000 2232          3306          DC    RXF+FLOAT           6B  SE         32333060
086C  0000 2232          3307          DC    RXF+FLOAT           6C  ME         32333070
086D  0000 2232          3308          DC    RXF+FLOAT           6D  DE         32333080
086E  0000 0782          3309          DC    STBP                6E  STBP       32333090
086F  0000 0737          3310          DC    LPB                 6F  LPB        32333100
                         3311  *                                               32333110
0870  0000 2570          3312          DC    STD+FLOAT           70  STD        32333120
0871  0000 2572          3313          DC    STME+FLOAT          71  STME       32333130
0872  0000 257A          3314          DC    LME+FLOAT           72  LME        32333140
0873  0000 022F          3315          DC    RXH                 73  LHL        32333150
0874  0000 036C          3316          DC    RXBIT               74  TBT        32333160
0875  0000 036C          3317          DC    RXBIT               75  SBT        32333170
0876  0000 036C          3318          DC    RXBIT               76  RBT        32333180
0877  0000 036C          3319          DC    RXBIT               77  CBT        32333190
0878  0000 2581          3320          DC    CDADSDMD+FLOAT      78  LD         32333200
0879  0000 2581          3321          DC    CDADSDMD+FLOAT      79  CD         32333210
087A  0000 2581          3322          DC    CDADSDMD+FLOAT      7A  AD         32333220
087B  0000 2581          3323          DC    CDADSDMD+FLOAT      7B  SD         32333230
087C  0000 2581          3324          DC    CDADSDMD+FLOAT      7C  MD         32333240
087D  0000 2581          3325          DC    CDADSDMD+FLOAT      7D  DD         32333250
087E  0000 258F          3326          DC    STMD+FLOAT          7E  STMD       32333260
087F  0000 2598          3327          DC    LMD+FLOAT           7F  LMD        32333270
                         3328  *                                               32333280
0880  0000 40C2          3329          DC    ILEG                80  --         32333290
0881  0000 40C2          3330          DC    ILEG                81  --         32333300
0882  0000 25AC          3331          DC    STDE+FLOAT          82  STDE       32333310
0883  0000 40C2          3332          DC    ILEG                83  --         32333320
0884  0000 2581          3333          DC    CDADSDMD+FLOAT      84  LED        32333330
0885  0000 40C2          3334          DC    ILEG                85  --         32333340
0886  0000 40C2          3335          DC    ILEG                86  --         32333350
0887  0000 25BA          3336          DC    LDE+FLOAT           87  LDE        32333360
0888  0000 8400          3337          DC    BRK+PRIV            88  BRK        32333370
0889  0000 40C2          3338          DC    ILEG                89  --         32333380
088A  0000 40C2          3339          DC    ILEG                8A  --         32333390
088B  0000 40C2          3340          DC    ILEG                8B  --         32333400
```

DROM1 VECTOR TABLE & PRIV/ILEG TABLE

```
088C   0000 0605          3341          DC   RXRX              8C   RXRX          32333410
088D   0000 40C2          3342          DC   ILEG              8D   --            32333420
088E   0000 40C2          3343          DC   ILEG              8E   --            32333430
088F   0000 40C2          3344          DC   ILEG              8F   --            32333440
                          3345  *                                                  32333450
0890   0000 027E          3346          DC   SFSHFTH           90   SRHLS         32333460
0891   0000 027E          3347          DC   SFSHFTH           91   SLHLS         32333470
0892   0000 0384          3348          DC   STBR              92   STBR          32333480
0893   0000 0382          3349          DC   LBR               93   LBR           32333490
0894   0000 038A          3350          DC   EXBR              94   EXBR          32333500
0895   0000 811E          3351          DC   EPSR+PRIV         95   EPSR          32333510
0896   0000 40C2          3352          DC   ILEG              96   --            32333520
0897   0000 40C2          3353          DC   ILEG              97   --            32333530
0898   0000 81C7          3354          DC   RRIO+PRIV         98   WHR           32333540
0899   0000 81C7          3355          DC   RRIO+PRIV         99   RHR           32333550
089A   0000 81C7          3356          DC   RRIO+PRIV         9A   WDR           32333560
089B   0000 81C7          3357          DC   RRIO+PRIV         9B   RDR           32333570
089C   0000 40C2          3358          DC   ILEG              9C   --            32333580
089D   0000 81C7          3359          DC   RRIO+PRIV         9D   SSR           32333590
089E   0000 81C7          3360          DC   RRIO+PRIV         9E   OCR           32333600
089F   0000 40C2          3361          DC   ILEG              9F   --            32333610
                          3362  *                                                  32333620
08A0   0000 40C2          3363          DC   ILEG              A0   --            32333630
08A1   0000 40C2          3364          DC   ILEG              A1   --            32333640
08A2   0000 40C2          3365          DC   ILEG              A2   --            32333650
08A3   0000 40C2          3366          DC   ILEG              A3   --            32333660
08A4   0000 25BD          3367          DC   LEDR+FLOAT        A4   LEDR          32333670
08A5   0000 25C3          3368          DC   LEGR+FLOAT        A5   LEGR          32333680
08A6   0000 25C4          3369          DC   LDGR+FLOAT        A6   LDGR          32333690
08A7   0000 25CB          3370          DC   EVALU+FLOAT       A7   LDER          32333700
08A8   0000 40C2          3371          DC   ILEG              A8   --            32333710
08A9   0000 40C2          3372          DC   ILEG              A9   --            32333720
08AA   0000 40C2          3373          DC   ILEG              AA   --            32333730
08AB   0000 40C2          3374          DC   ILEG              AB   --            32333740
08AC   0000 40C2          3375          DC   ILEG              AC   --            32333750
08AD   0000 40C2          3376          DC   ILEG              AD   --            32333760
08AE   0000 40C2          3377          DC   ILEG              AE   --            32333770
08AF   0000 40C2          3378          DC   ILEG              AF   --            32333780
                          3379  *                                                  32333790
08B0   0000 40C2          3380          DC   ILEG              B0   --            32333800
08B1   0000 40C2          3381          DC   ILEG              B1   --            32333810
08B2   0000 40C2          3382          DC   ILEG              B2   --            32333820
08B3   0000 40C2          3383          DC   ILEG              B3   --            32333830
08B4   0000 40C2          3384          DC   ILEG              B4   --            32333840
08B5   0000 40C2          3385          DC   ILEG              B5   --            32333850
08B6   0000 40C2          3386          DC   ILEG              B6   --            32333860
08B7   0000 40C2          3387          DC   ILEG              B7   --            32333870
08B8   0000 40C2          3388          DC   ILEG              B8   --            32333880
08B9   0000 40C2          3389          DC   ILEG              B9   --            32333890
08BA   0000 40C2          3390          DC   ILEG              BA   --            32333900
08BB   0000 40C2          3391          DC   ILEG              BB   --            32333910
08BC   0000 40C2          3392          DC   ILEG              BC   --            32333920
08BD   0000 40C2          3393          DC   ILEG              BD   --            32333930
08BE   0000 40C2          3394          DC   ILEG              BE   --            32333940
```

DROM1 VECTOR TABLE & PRIV/ILEG TABLE

```
08BF   0000 40C2          3395          DC    ILEG                BF   --                32333950
                          3396  *                                                        32333960
08C0   0000 029E          3397          DC    BXLH                C0   BXH               32333970
08C1   0000 029E          3398          DC    BXLH                C1   BXLE              32333980
08C2   0000 8122          3399          DC    LPSW+PRIV           C2   LSPW              32333990
08C3   0000 02B3          3400          DC    THI                 C3   THI               32334000
08C4   0000 02B6          3401          DC    NHI                 C4   NHI               32334010
08C5   0000 02B7          3402          DC    CLHI                C5   CLHI              32334020
08C6   0000 02BA          3403          DC    OHI                 C6   OHI               32334030
08C7   0000 02BD          3404          DC    XHI                 C7   XHI               32334040
08C8   0000 0319          3405          DC    LHI                 C8   LHI               32334050
08C9   0000 02C6          3406          DC    CHI                 C9   CHI               32334060
08CA   0000 02CC          3407          DC    AHI                 CA   AHI               32334070
08CB   0000 02CF          3408          DC    SHI                 CB   SHI               32334080
08CC   0000 0283          3409          DC    RISHFTH             CC   SRHL              32334090
08CD   0000 0283          3410          DC    RISHFTH             CD   SLHL              32334100
08CE   0000 0283          3411          DC    RISHFTH             CE   SRHA              32334110
08CF   0000 0283          3412          DC    RISHFTH             CF   SLHA              32334120
                          3413  *                                                        32334130
08D0   0000 0364          3414          DC    STM                 D0   STM               32334140
08D1   0000 0320          3415          DC    LM                  D1   LM                32334150
08D2   0000 0383          3416          DC    STB                 D2   STB               32334160
08D3   0000 022E          3417          DC    RXBYTE              D3   LB                32334170
08D4   0000 022E          3418          DC    RXBYTE              D4   CLB               32334180
08D5   0000 81EB          3419          DC    AL+PRIV             D5   AL                32334190
08D6   0000 40C2          3420          DC    ILEG                D6   --                32334200
08D7   0000 40C2          3421          DC    ILEG                D7   --                32334210
08D8   0000 81C7          3422          DC    RRIO+PRIV           D8   WH                32334220
08D9   0000 81C7          3423          DC    RRIO+PRIV           D9   RH                32334230
08DA   0000 81C6          3424          DC    RXIO+PRIV           DA   WD                32334240
08DB   0000 81C7          3425          DC    RRIO+PRIV           DB   RD                32334250
08DC   0000 40C2          3426          DC    ILEG                DC   --                32334260
08DD   0000 81C7          3427          DC    RRIO+PRIV           DD   SS                32334270
08DE   0000 81C6          3428          DC    RXIO+PRIV           DE   OC                32334280
08DF   0000 84E3          3429          DC    PSF+PRIV            DF   PSF               32334290
                          3430  *                                                        32334300
08E0   0000 0361          3431          DC    TS                  E0   TS                32334310
08E1   0000 013B          3432          DC    SVC                 E1   SVC               32334320
08E2   0000 8141          3433          DC    SINT+PRIV           E2   SINT              32334330
08E3   0000 83A6          3434          DC    SCP+PRIV            E3   SCP               32334340
08E4   0000 40C2          3435          DC    ILEG                E4   --                32334350
08E5   0000 93BF          3436          DC    BDCS+PRIV+WCSENA    E5   BDCS              32334360
08E6   0000 032B          3437          DC    LA                  E6   LA                32334370
08E7   0000 039F          3438          DC    TLATE               E7   TLATE             32334380
08E8   0000 83C1          3439          DC    RWDCS+PRIV          E8   RDCS,WDCS         32334390
08E9   0000 13BD          3440          DC    ECS+WCSENA          E9   ECS               32334400
08EA   0000 0281          3441          DC    RISHFTF             EA   RRL               32334410
08EB   0000 0281          3442          DC    RISHFTF             EB   RLL               32334420
08EC   0000 0281          3443          DC    RISHFTF             EC   SRL               32334430
08ED   0000 0281          3444          DC    RISHFTF             ED   SLL               32334440
08EE   0000 0281          3445          DC    RISHFTF             EE   SRA               32334450
08EF   0000 0281          3446          DC    RISHFTF             EF   SLA               32334460
                          3447  *                                                        32334470
08F0   0000 40C2          3448          DC    ILEG                F0   --                32334480
```

DROM1 VECTOR TABLE & PRIV/ILEG TABLE

```
08F1  0000 40C2   3449  DC  ILEG   F1  --   32334490
08F2  0000 40C2   3450  DC  ILEG   F2  --   32334500
08F3  0000 02B3   3451  DC  TI     F3  TI   32334510
08F4  0000 02B6   3452  DC  NI     F4  NI   32334520
08F5  0000 02B7   3453  DC  CLI    F5  CLI  32334530
08F6  0000 02BA   3454  DC  OI     F6  OI   32334540
08F7  0000 02BD   3455  DC  XI     F7  XI   32334550
08F8  0000 0319   3456  DC  LI     F8  LI   32334560
08F9  0000 02C6   3457  DC  CI     F9  CI   32334570
08FA  0000 02CC   3458  DC  AI     FA  AI   32334580
08FB  0000 02CF   3459  DC  SI     FB  SI   32334590
08FC  0000 40C2   3460  DC  ILEG   FC  --   32334600
08FD  0000 40C2   3461  DC  ILEG   FD  --   32334610
08FE  0000 40C2   3462  DC  ILEG   FE  --   32334620
08FF  0000 40C2   3463  DC  ILEG   FF  --   32334630
```

DROM2 VECTOR TABLE & FORMAT TABLE

```
                        3465  * FORMAT ROM INFORMATION:                                          32334650
                        3466  * WEIGHT 1 - RR   - ACTIVE 1                                      32334660
                        3467  *        2 - RXRX - ACTIVE 1                                      32334670
                        3468  *        4 - RI2  - ACTIVE 0                                      32334680
                        3469  *        8 - RX   - ACTIVE 1                                      32334690
                        3470  * NOTE - ALL UNDEFINED SPECIFIED AS RR.                           32334700

0000 C000               3472  RX       EQU   'C000'                                           32334720
0000 0000               3473  RI2      EQU   '0000'                                           32334730
0000 4000               3474  RI1      EQU   '4000'                                           32334740
0000 E000               3475  RX.RX    EQU   'E000'                                           32334750
0000 5000               3476  RR       EQU   '5000'                                           32334760

                        3478  * BITS 00:15 OF ROM WORDS SHOWN ARE NOT USED.                    32334780
                        3479  * BITS 16:19 CONTAIN THE FLAG INFORMATION FOR THE FORMAT ROM.    32334790
                        3480  * BITS 20:31 CONTAIN THE INSTRUCTION'S DROM2 ENTRY ADDRESS.      32334800

0900  0000 5000         3482           DC    RR+0              00  --                        32334820
0901  0000 5000         3483           DC    RR+0              01  BALR                      32334830
0902  0000 5000         3484           DC    RR+0              02  BTCR                      32334840
0903  0000 5000         3485           DC    RR+0              03  PFCR                      32334850
0904  0000 5000         3486           DC    RR+0              04  NR                        32334860
0905  0000 5000         3487           DC    RR+0              05  CLR                       32334870
0906  0000 5000         3488           DC    RR+0              06  OR                        32334880
0907  0000 5000         3489           DC    RR+0              07  XR                        32334890
0908  0000 5000         3490           DC    RR+0              08  LR                        32334900
0909  0000 5000         3491           DC    RR+0              09  CR                        32334910
090A  0000 5000         3492           DC    RR+0              0A  AR                        32334920
090B  0000 5000         3493           DC    RR+0              0B  SR                        32334930
090C  0000 5000         3494           DC    RR+0              0C  MHR                       32334940
090D  0000 52DE         3495           DC    RR+DH.005         0D  DHR                       32334950
090E  0000 5000         3496           DC    RR+0              0E  --                        32334960
090F  0000 5000         3497           DC    RR+0              0F  --                        32334970
                        3498  *                                                              32334980
0910  0000 528D         3499           DC    RR+SRLS           10  SRLS                      32334990
0911  0000 528E         3500           DC    RR+SLLS           11  SLLS                      32335000
0912  0000 5000         3501           DC    RR+0              12  CHVR                      32335010
0913  0000 55CF         3502           DC    RR+LPER           13  LPER                      32335020
0914  0000 5000         3503           DC    RR+0              14  --                        32335030
0915  0000 55A6         3504           DC    RR+LGER           15  LGER                      32335040
0916  0000 55A8         3505           DC    RR+LGDR           16  LGDR                      32335050
0917  0000 55D3         3506           DC    RR+LCER           17  LCER                      32335060
0918  0000 5126         3507           DC    RR+QTEST          18  LPSWR                     32335070
0919  0000 5000         3508           DC    RR+0              19  --                        32335080
091A  0000 5000         3509           DC    RR+0              1A  --                        32335090
091B  0000 5000         3510           DC    RR+0              1B  --                        32335100
091C  0000 5000         3511           DC    RR+0              1C  MR                        32335110
091D  0000 5000         3512           DC    RR+0              1D  DR                        32335120
091E  0000 5000         3513           DC    RR+0              1E  --                        32335130
091F  0000 5000         3514           DC    RR+0              1F  --                        32335140
                        3515  *                                                              32335150
0920  0000 5013         3516           DC    RR+EXIT           20  BTBS                      32335160
0921  0000 5013         3517           DC    RR+EXIT           21  BTFS                      32335170
```

DROM2 VECTOR TABLE & FORMAT TABLE

```
0922  0000 5013          3518          DC    RR+EXIT          22  BFBS          32335180
0923  0000 5013          3519          DC    RR+EXIT          23  BFFS          32335190
0924  0000 5000          3520          DC    RR+0             24  LIS           32335200
0925  0000 5000          3521          DC    RR+0             25  LCS           32335210
0926  0000 5000          3522          DC    RR+0             26  AIS           32335220
0927  0000 5000          3523          DC    RR+0             27  SIS           32335230
0928  0000 5569          3524          DC    RR+EEXIT         28  LER           32335240
0929  0000 5000          3525          DC    RR+0             29  CER           32335250
092A  0000 5569          3526          DC    RR+EEXIT         2A  AER           32335260
092B  0000 5569          3527          DC    RR+EEXIT         2B  SER           32335270
092C  0000 5569          3528          DC    RR+EEXIT         2C  MER           32335280
092D  0000 5569          3529          DC    RR+EEXIT         2D  DER           32335290
092E  0000 5000          3530          DC    RR+0             2E  FXR           32335300
092F  0000 5552          3531          DC    RR+FLR.020       2F  FLR           32335310
                         3532  *                                                 32335320
0930  0000 5000          3533          DC    RR+0             30  --            32335330
0931  0000 5000          3534          DC    RR+0             31  --            32335340
0932  0000 5013          3535          DC    RR+EXIT          32  PBR           32335350
0933  0000 55DB          3536          DC    RR+LPDR          33  LPDR          32335360
0934  0000 5000          3537          DC    RR+0             34  EXHR          32335370
0935  0000 5000          3538          DC    RR+0             35  --            32335380
0936  0000 5000          3539          DC    RR+0             36  --            32335390
0937  0000 55E0          3540          DC    RR+LCDR          37  LCDR          32335400
0938  0000 5569          3541          DC    RR+EEXIT         38  LDR           32335410
0939  0000 5000          3542          DC    RR+0             39  CDR           32335420
093A  0000 5569          3543          DC    RR+EEXIT         3A  ADR           32335430
093B  0000 5569          3544          DC    RR+EEXIT         3B  SDR           32335440
093C  0000 5569          3545          DC    RR+EEXIT         3C  MDR           32335450
093D  0000 5569          3546          DC    RR+EEXIT         3D  DDR           32335460
093E  0000 552C          3547          DC    RR+FXR.010       3E  FXDR          32335470
093F  0000 5554          3548          DC    RR+FLDR.020      3F  FLDR          32335480
                         3549  *                                                 32335490
0940  0000 C236          3550          DC    RX+STH.D2        40  STH           32335500
0941  0000 C000          3551          DC    RX+0             41  BAL           32335510
0942  0000 C000          3552          DC    RX+0             42  BTC           32335520
0943  0000 C000          3553          DC    RX+0             43  BFC           32335530
0944  0000 C2B4          3554          DC    RX+NH            44  NH            32335540
0945  0000 C2B7          3555          DC    RX+CLH           45  CLH           32335550
0946  0000 C2B8          3556          DC    RX+OH            46  OH            32335560
0947  0000 C2BB          3557          DC    RX+XH            47  XH            32335570
0948  0000 C317          3558          DC    RX+LH            48  LH            32335580
0949  0000 C2B7          3559          DC    RX+CLH           49  CH            32335590
094A  0000 C2CA          3560          DC    RX+AH            4A  AH            32335600
094B  0000 C2CF          3561          DC    RX+SH            4B  SH            32335610
094C  0000 C2D0          3562          DC    RX+MH            4C  MH            32335620
094D  0000 C2DD          3563          DC    RX+DH            4D  DH            32335630
094E  0000 5000          3564          DC    RR+0             4E  --            32335640
094F  0000 5000          3565          DC    RR+0             4F  --            32335650
                         3566  *                                                 32335660
0950  0000 C237          3567          DC    RX+STF.D2        50  ST            32335670
0951  0000 C2A4          3568          DC    RX+AM            51  AM            32335680
0952  0000 5000          3569          DC    RR+0             52  --            32335690
0953  0000 5000          3570          DC    RR+0             53  --            32335700
0954  0000 C2B5          3571          DC    RX+N             54  N             32335710
```

DROM2 VECTOR TABLE & FORMAT TABLE

```
0955   0000 C2B7          3572          DC    RX+CL              55   CL          32335720
0956   0000 C2B9          3573          DC    RX+0               56   0           32335730
0957   0000 C2BC          3574          DC    RX+X               57   X           32335740
0958   0000 C318          3575          DC    RX+L               58   L           32335750
0959   0000 C2B7          3576          DC    RX+CL              59   C           32335760
095A   0000 C2CB          3577          DC    RX+A               5A   A           32335770
095B   0000 C2CF          3578          DC    RX+S               5B   S           32335780
095C   0000 C2D6          3579          DC    RX+M               5C   M           32335790
095D   0000 C2F8          3580          DC    RX+D               5D   D           32335800
095E   0000 C236          3581          DC    RX+STH.D2          5E   CRC12       32335810
095F   0000 C236          3582          DC    RX+STH.D2          5F   CRC16       32335820
                          3583   *                                                 32335830
0960   0000 C237          3584          DC    RX+STF.D2          60   STF         32335840
0961   0000 C236          3585          DC    RX+STH.D2          61   AHM         32335850
0962   0000 C236          3586          DC    RX+STH.D2          62   PB          32335860
0963   0000 C351          3587          DC    RX+LRA.SH2         63   LRA         32335870
0964   0000 C000          3588          DC    RX+0               64   ATL         32335880
0965   0000 C236          3589          DC    RX+STH.D2          65   ABL         32335890
0966   0000 C000          3590          DC    RX+0               66   RTL         32335900
0967   0000 C000          3591          DC    RX+0               67   RBL         32335910
0968   0000 C564          3592          DC    RX+LE              68   LE          32335920
0969   0000 C566          3593          DC    RX+CE              69   CE          32335930
096A   0000 C568          3594          DC    RX+AE              6A   AE          32335940
096B   0000 C56A          3595          DC    RX+SE              6B   SE          32335950
096C   0000 C56C          3596          DC    RX+ME              6C   ME          32335960
096D   0000 C56E          3597          DC    RX+DE              6D   DE          32335970
096E   0000 C7C2          3598          DC    RX+STBPLP2B        6E   STBP        32335980
096F   0000 C000          3599          DC    RX+0               6F   LPB         32335990
                          3600   *                                                 32336000
0970   0000 C237          3601          DC    RX+STF.D2          70   STD         32336010
0971   0000 C000          3602          DC    RX                 71   STME        32336020
0972   0000 C000          3603          DC    RX+0               72   LME         32336030
0973   0000 C31E          3604          DC    RX+LHL             73   LHI         32336040
0974   0000 C380          3605          DC    RX+TBT             74   TBT         32336050
0975   0000 C372          3606          DC    RX+SBT             75   SBT         32336060
0976   0000 C377          3607          DC    RX+RBT             76   RBT         32336070
0977   0000 C37C          3608          DC    RX+CBT             77   CBT         32336080
0978   0000 C583          3609          DC    RX+LD              78   LD          32336090
0979   0000 C585          3610          DC    RX+CD              79   CD          32336100
097A   0000 C587          3611          DC    RX+AD              7A   AD          32336110
097B   0000 C589          3612          DC    RX+SD              7B   SD          32336120
097C   0000 C58B          3613          DC    RX+MD              7C   MD          32336130
097D   0000 C58D          3614          DC    RX+DD              7D   DD          32336140
097E   0000 C000          3615          DC    RX+0               7E   STMD        32336150
097F   0000 C000          3616          DC    RX+0               7F   LMD         32336160
                          3617   *                                                 32336170
0980   0000 5000          3618          DC    RR+0               80   --          32336180
0981   0000 5000          3619          DC    RR+0               81   --          32336190
0982   0000 C013          3620          DC    RX+EXIT            82   STDE        32336200
0983   0000 5000          3621          DC    RR+0               83   --          32336210
0984   0000 C564          3622          DC    RX+LED             84   LED         32336220
0985   0000 5000          3623          DC    RR+0               85   --          32336230
0986   0000 5000          3624          DC    RR+0               86   --          32336240
0987   0000 C569          3625          DC    RX+EEXIT           87   LDE         32336250
```

DROM2 VECTOR TABLE & FORMAT TABLE

```
0988  0000 5000          3626          DC    RR+0          88  BRK       32336260
0989  0000 5000          3627          DC    RR+0          89  --        32336270
098A  0000 5000          3628          DC    RR+0          8A  --        32336280
098B  0000 5000          3629          DC    RR+0          8B  --        32336290
098C  0000 5000          3630          DC    RX.RX+0       8C  RXRX      32336300
098D  0000 5000          3631          DC    RR+0          8D  --        32336310
098E  0000 5000          3632          DC    RR+0          8E  --        32336320
098F  0000 5000          3633          DC    RR+0          8F  --        32336330
                         3634  *                                         32336340
0990  0000 5286          3635          DC    RR+SRHLS      90  SRHLS     32336350
0991  0000 5287          3636          DC    RR+SLHLS      91  SLHLS     32336360
0992  0000 5000          3637          DC    RR+0          92  STBR      32336370
0993  0000 5000          3638          DC    RR+0          93  LBR       32336380
0994  0000 5000          3639          DC    RR+0          94  EXBR      32336390
0995  0000 5127          3640          DC    RR+QTEST1     95  EPSR      32336400
0996  0000 5000          3641          DC    RR+0          96  --        32336410
0997  0000 5000          3642          DC    RR+0          97  --        32336420
0998  0000 51E1          3643          DC    RR+WHR        98  WHR       32336430
0999  0000 51D9          3644          DC    RR+RHR        99  RHR       32336440
099A  0000 51E3          3645          DC    RR+WDR        9A  WDR       32336450
099B  0000 51E7          3646          DC    RR+RDR        9B  RDR       32336460
099C  0000 5000          3647          DC    RR+0          9C  --        32336470
099D  0000 51D0          3648          DC    RR+SSR        9D  SSR       32336480
099E  0000 51C9          3649          DC    RR+OCR        9E  OCR       32336490
099F  0000 5000          3650          DC    RR+0          9F  --        32336500
                         3651  *                                         32336510
09A0  0000 5000          3652          DC    RR+0          A0  --        32336520
09A1  0000 5000          3653          DC    RR+0          A1  --        32336530
09A2  0000 5000          3654          DC    RR+0          A2  --        32336540
09A3  0000 5000          3655          DC    RR+0          A3  --        32336550
09A4  0000 5569          3656          DC    RR+EEXIT      A4  LEDR      32336560
09A5  0000 5569          3657          DC    RR+EEXIT      A5  LEGR      32336570
09A6  0000 55C9          3658          DC    RR+LDGR1      A6  LDGR      32336580
09A7  0000 55C7          3659          DC    RR+LDER       A7  LDER      32336590
09A8  0000 5000          3660          DC    RR+0          A8  --        32336600
09A9  0000 5000          3661          DC    RR+0          A9  --        32336610
09AA  0000 5000          3662          DC    RR+0          AA  --        32336620
09AB  0000 5000          3663          DC    RR+0          AB  --        32336630
09AC  0000 5000          3664          DC    RR+0          AC  --        32336640
09AD  0000 5000          3665          DC    RR+0          AD  --        32336650
09AE  0000 5000          3666          DC    RR+0          AE  --        32336660
09AF  0000 5000          3667          DC    RR+0          AF  --        32336670
                         3668  *                                         32336680
09B0  0000 5000          3669          DC    RR+0          B0  --        32336690
09B1  0000 5000          3670          DC    RR+0          B1  --        32336700
09B2  0000 5000          3671          DC    RR+0          B2  --        32336710
09B3  0000 5000          3672          DC    RR+0          B3  --        32336720
09B4  0000 5000          3673          DC    RR+0          B4  --        32336730
09B5  0000 5000          3674          DC    RR+0          B5  --        32336740
09B6  0000 5000          3675          DC    RR+0          B6  --        32336750
09B7  0000 5000          3676          DC    RR+0          B7  --        32336760
09B8  0000 5000          3677          DC    RR+0          B8  --        32336770
09B9  0000 5000          3678          DC    RR+0          B9  --        32336780
09BA  0000 5000          3679          DC    RR+0          BA  --        32336790
```

DROM2 VECTOR TABLE & FORMAT TABLE

```
09BB  0000 5000          3680          DC    RR+0              BB  --          32336800
09BC  0000 5000          3681          DC    RR+0              BC  --          32336810
09BD  0000 5000          3682          DC    RR+0              BD  --          32336820
09BE  0000 5000          3683          DC    RR+0              BE  --          32336830
09BF  0000 5000          3684          DC    RR+0              BF  --          32336840
                         3685  *                                               32336850
09C0  0000 C2A2          3686          DC    RX+BXH            C0  BXH         32336860
09C1  0000 C2A3          3687          DC    RX+BXLE           C1  BXLE        32336870
09C2  0000 C126          3688          DC    RX+QTEST          C2  LPSW        32336880
09C3  0000 4000          3689          DC    RI1+0             C3  THI         32336890
09C4  0000 4000          3690          DC    RI1+0             C4  NHI         32336900
09C5  0000 4000          3691          DC    RI1+0             C5  CLHI        32336910
09C6  0000 4000          3692          DC    RI1+0             C6  CHI         32336920
09C7  0000 4000          3693          DC    RI1+0             C7  XHI         32336930
09C8  0000 4000          3694          DC    RI1+0             C8  LHI         32336940
09C9  0000 4000          3695          DC    RI1+0             C9  CHI         32336950
09CA  0000 4000          3696          DC    RI1+0             CA  AHI         32336960
09CB  0000 4000          3697          DC    RI1+0             CB  SHI         32336970
09CC  0000 4286          3698          DC    RI1+SRHL          CC  SRHL        32336980
09CD  0000 4287          3699          DC    RI1+SLHL          CD  SLHL        32336990
09CE  0000 4288          3700          DC    RI1+SRHA          CE  SRHA        32337000
09CF  0000 4289          3701          DC    RI1+SLHA          CF  SLHA        32337010
                         3702  *                                               32337020
09D0  0000 C013          3703          DC    RX+EXIT           D0  STM         32337030
09D1  0000 C000          3704          DC    RX+0              D1  LM          32337040
09D2  0000 C235          3705          DC    RX+STB.D2         D2  STB         32337050
09D3  0000 C381          3706          DC    RX+LB             D3  LB          32337060
09D4  0000 C387          3707          DC    RX+CLB            D4  CLB         32337070
09D5  0000 C000          3708          DC    RX+0              D5  AL          32337080
09D6  0000 5000          3709          DC    RR+0              D6  --          32337090
09D7  0000 5000          3710          DC    RR+0              D7  --          32337100
09D8  0000 C1DD          3711          DC    RX+WH             D8  WH          32337110
09D9  0000 C1D3          3712          DC    RX+RH             D9  RH          32337120
09DA  0000 C1E9          3713          DC    RX+WD             DA  WD          32337130
09DB  0000 C1E5          3714          DC    RX+RD             DB  RD          32337140
09DC  0000 5000          3715          DC    RR+0              DC  --          32337150
09DD  0000 C1CD          3716          DC    RX+SS             DD  SS          32337160
09DE  0000 C1C8          3717          DC    RX+OC             DE  OC          32337170
09DF  0000 C013          3718          DC    RX+EXIT           DF  PSF         32337180
                         3719  *                                               32337190
09E0  0000 C013          3720          DC    RX+EXIT           E0  TS          32337200
09E1  0000 C134          3721          DC    RX+COMSWAP2       E1  SVC         32337210
09E2  0000 4153          3722          DC    RI1+IOINT1        E2  SINT        32337220
09E3  0000 C381          3723          DC    RX+LB             E3  SCP         32337230
09E4  0000 5000          3724          DC    RR+0              E4  --          32337240
09E5  0000 C000          3725          DC    RX+0              E5  BDCS        32337250
09E6  0000 C000          3726          DC    RX+0              E6  LA          32337260
09E7  0000 C013          3727          DC    RX+EXIT           E7  TLATE       32337270
09E8  0000 5000          3728          DC    RR+0              E8  RDCS,WDCS   32337280
09E9  0000 4000          3729          DC    RI1+0             E9  ECS         32337290
09EA  0000 428B          3730          DC    RI1+RRL           EA  RRL         32337300
09EB  0000 428C          3731          DC    RI1+RLL           EB  RLL         32337310
09EC  0000 428D          3732          DC    RI1+SRL           EC  SRL         32337320
09ED  0000 428E          3733          DC    RI1+SLL           ED  SLL         32337330
```

DROM2 VECTOR TABLE & FORMAT TABLE

```
09EE   0000 428A          3734          DC    RI1+SRA          EE   SRA          32337340
09EF   0000 428F          3735          DC    RI1+SLA          EF   SLA          32337350
                          3736  *                                                32337360
09F0   0000 5000          3737          DC    RR+0             F0   --           32337370
09F1   0000 5000          3738          DC    RR+0             F1   --           32337380
09F2   0000 5000          3739          DC    RR+0             F2   --           32337390
09F3   0000 0000          3740          DC    RI2+0            F3   TI           32337400
09F4   0000 0000          3741          DC    RI2+0            F4   NI           32337410
09F5   0000 0000          3742          DC    RI2+0            F5   CLI          32337420
09F6   0000 0000          3743          DC    RI2+0            F6   OI           32337430
09F7   0000 0000          3744          DC    RI2+0            F7   XI           32337440
09F8   0000 0000          3745          DC    RI2+0            F8   LI           32337450
09F9   0000 0000          3746          DC    RI2+0            F9   CI           32337460
09FA   0000 0000          3747          DC    RI2+0            FA   AI           32337470
09FB   0000 0000          3748          DC    RI2+0            FB   SI           32337480
09FC   0000 5000          3749          DC    RR+0             FC   --           32337490
09FD   0000 5000          3750          DC    RR+0             FD   --           32337500
09FE   0000 5000          3751          DC    RR+0             FE   --           32337510
09FF   0000 5000          3752          DC    RR+0             FF   --           32337520


0A00                      3754          END                                      32337540
```

DROM2 VECTOR TABLE & FORMAT TABLE

ASSEMBLED BY MICROCAL II (32BIT) NO ASSEMBLY ERRORS

DROM2 VECTOR TABLE & FORMAT TABLE

BTC	0000 0293	3263							
BTCR	0000 0293	3195							
BTFS	0000 0296	3228							
BUFSW	0000 01B7								
BXH	0000 02A2	3686							
BXLE	0000 02A3	3687							
BXLH	0000 029E	3397	3398						
C	0000 02C2	3287							
CATN	0000 0401								
CBIT	0000 0010	807							
CBT	0000 037C	3608							
CD	0000 0585	3610							
CDADSDMD	0000 0581	3320	3321	3322	3323	3324	3325	3333	
CDR	0000 0557	3253							
CE	0000 0566	3593							
CER	0000 0522	3236							
CH	0000 02BE	3270							
CHANEL	0000 015F	688							
CHANMMF	0000 008E	760							
CHI	0000 02C6	3406							
CHVR	0000 02AB	3212							
CHVR.010	0000 02B2	1234							
CI	0000 02C6	3457							
CL	0000 02B7	3572	3576						
CLB	0000 0387	3707							
CLH	0000 02B7	3555	3559						
CLHI	0000 02B7	3402							
CLI	0000 02B7	3453							
CLR	0000 02B7	1294	3198						
COLD.1	0000 0066	241							
COLD.1A	0000 006A	240							
COLD.2	0000 006B	250	252						
COLD.3	0000 006F	244							
COLD.4	0000 0075								
COLD.5	0000 0077	553	563						
COLDSTRT	0000 0065	178							
COMMON	0000 0177	731	734	737					
COMMON2	0000 01B3	812	822						
COMSWAP	0000 00C6	387	413	455	512				
COMSWAP2	0000 0134	3721							
CONS.1	0000 0410	1742							
CONSER	0000 0401	66	86	208	218	257	361	1925	1926
CPAN	0000 0654	2418							
CPAN1	0000 065D	2579							
CPAN10	0000 0666	2552							
CPAN2	0000 0669								
CPAN20	0000 0674	2550							
CPAN21	0000 0678	2561							
CPAN3	0000 066A	2588							
CPAN4	0000 0670	2570							
CPANP	0000 0654								
CR	0000 02C6	3202							
CRC12	0000 038C	3292							
CRC16	0000 0390	3293							

DROM2 VECTOR TABLE & FORMAT TABLE

CRC16AST	0000	039B	1587									
CRCA	0000	0394	1584									
CRCB	0000	0396	1597									
CRCC	0000	0399	1595									
CRCCK	0000	01AB	808									
CRCK1	0000	01AF	826									
CRCKA	0000	01A2	824									
CRCKB	0000	01A6	821									
CRCKC	0000	01A9	819									
CRLF	0000	0485	1749	1778	1785	1915	1937	1949	1962	1977	1992	
D	0000	02F8	3580									
D.010	0000	02FC	1376									
D.020	0000	0305	1382	1385								
D.025	0000	030E	1394									
D.030	0000	0310	1396									
DD	0000	058D	3614									
DDR	0000	055C	3257									
DE	0000	056E	3597									
DECODE	0000	041E	1831									
DER	0000	0527	3240									
DFAULT	0000	0314	1389	1398								
DFETCHE	0000	0093	381									
DH	0000	02DD	3563									
DH.005	0000	02DE	3495									
DH.010	0000	02E3	1346									
DH.020	0000	02E6	1350									
DH.025	0000	02EF	1358									
DH.030	0000	02F1	1360									
DH.040	0000	02F4	1364									
DHFAULT	0000	00D0	1353	1362								
DHLOOP	0000	02EA										
DHR	0000	02DC	3206									
DIGC1	0000	06CB	2703									
DIGITCK	0000	06C7	2629	2643	2652	2797	2812					
DIGITCK1	0000	06C8	2825									
DIVIDE	0000	07EB	3035	3049								
DIVIDE1	0000	07EC	3060									
DLOOP	0000	0309										
DR	0000	02F8	3223									
DV001	0000	07F2	3158									
DV002	0000	07F1	3160									
DV003	0000	07F7	3166									
DV004	0000	07FA	3169									
DVALU	0000	05D6	3247	3251								
EBIT	0000	0080	711									
ECS	0000	03BD	3440									
EEXIT	0000	0569	3524	3526	3527	3528	3529	3541	3543	3544	3545	3546	3625	3656
			3657									
ENTRY	0000	0418	1984									
EPF	0000	0088	88									
EPF1	0000	008D	314									
EPSR	0000	011E	3351									
EVALU	0000	05CB	3213	3217	3370							
EXAUTMNF	0000	0182	752	858								

DROM2 VECTOR TABLE & FORMAT TABLE

EXAUTO	0000 017E	723	783										
EXAUTO2	0000 017F	744	837										
EXBR	0000 038A	3350											
EXHR	0000 031F	3248											
EXIT	0000 0013	475	885	889	913	1035	1037	1039	1219	1539	1546	1598	1639
		2000	2067	2238	2281	2290	2293	2868	3516	3517	3518	3519	3535
		3620	3703	3718	3720	3727							
EXSUB	0000 017C	765	771										
EXSUB0	0000 0183	712											
EXSUB1	0000 0185	716											
EXSUB2	0000 017A	843											
FASTMODE	0000 0169												
FBIT	0000 0001	718											
FLDR	0000 054C	3259											
FLDR.020	0000 0554	3548											
FLOAT	0000 2000	3213	3215	3216	3217	3235	3236	3237	3238	3239	3240	3241	3242
		3247	3251	3252	3253	3254	3255	3256	3257	3258	3259	3295	3303
		3304	3305	3306	3307	3308	3312	3313	3314	3320	3321	3322	3323
		3324	3325	3326	3327	3331	3333	3336	3367	3368	3369	3370	
FLR	0000 054C	3242											
FLR.020	0000 0552	3531											
FLR1	0000 0551	2154											
FLUSH	0000 06F3	2755											
FLUSH.1	0000 06F6	2770											
FLUSHP	0000 06EA	2659											
FLUSHU	0000 06EF	2816	2827										
FMTCMD	0000 00EE	1729											
FORFAUL2	0000 00E9	477	2936										
FORFAUL3	0000 00EA	2962											
FORFAUL6	0000 00ED	502											
FORFAULT	0000 00F4	494											
FREEWORD	0000 0000	68	76	113	114	115	492	493	1703	1703	1703	1703	1703
		1703	1703	1703	1703	1703	1703	1703	1703	1703	1703	1703	1703
		1703	1703	1703	1703	1703	1703	1703	1703	1703	1703	2411	2411
		2411	2411	2411	2411	2411	2411	2411	2411	2411	2411	2411	2411
		2411	2411	2411	2411	2411	2411	2411	2411	2411	3177	3177	3177
		3177											
FXDR	0000 055D	3258											
FXDR1	0000 0562	2189											
FXR	0000 0528	3241											
FXR.010	0000 052C	3547											
FXR.25	0000 053C	2127											
FXR.30	0000 0541	2129	2147										
GET.END	0000 067A	2465	2537										
GETBYT.1	0000 06B0	2624	2642	2791	2811								
GETBYTE	0000 06AF	2766											
GETPAD	0000 0680												
HARDSTOP	0000 00AB	190	207										
HEX	0000 046D	1848											
HWINP	0000 0171	729											
HWOUTP	0000 0173	739											
IDLE	0000 0001	67											
IF.DELE	0000 044F	1816											
IFETCHE	0000 0090	404											

DROM2 VECTOR TABLE & FORMAT TABLE

IIINT	0000 00C2	122	248	408	1657	1695	2007	2446	3180				
IIINT1	0000 00C3												
IIINTA	0000 00BF	1688											
IIPRESUM	0000 072A	2426	2897	2999									
ILEG	0000 40C2	3193	3207	3208	3214	3219	3220	3221	3224	3225	3244	3245	3249
		3250	3275	3276	3280	3281	3329	3330	3332	3334	3335	3338	3339
		3340	3342	3343	3344	3352	3353	3358	3361	3363	3364	3365	3366
		3371	3372	3373	3374	3375	3376	3377	3378	3380	3381	3382	3383
		3384	3385	3386	3387	3388	3389	3390	3391	3392	3393	3394	3395
		3420	3421	3426	3435	3448	3449	3450	3460	3461	3462	3463	
ILEGF	0000 00BD	79											
IN.2	0000 043B	1800											
INCHR	0000 0439	1814	1826	1840	1974								
INCMD	0000 0021	1733											
INDEV	0000 0010	1727	1792										
INTRPT3	0000 0735	1674	1681										
INTRPT5	0000 0734	2498	2514	2519	2574	2580	2664	2677	2687	2746	2771	2835	2931
INTRPT7	0000 0733	2926											
IOINT	0000 0150	97	668	671									
IOINT1	0000 0153	3722											
IS.AT	0000 0498	1764											
IS.D	0000 04BF	1774											
IS.D00	0000 04C9	1971											
IS.DELE	0000 0453	1820											
IS.F	0000 04B4	1772											
IS.F00	0000 04BB	1954											
IS.MINUS	0000 04A9	1768											
IS.P	0000 04CE	1776											
IS.PL0	0000 049D	1910	1931										
IS.PLUS	0000 049B	1766	1924										
IS.PRMPT	0000 04DB	1760											
IS.R	0000 04AC	1770											
IS.R0	0000 04B1	1941											
IS.SNGLC	0000 04D9	1762											
ISRST	0000 0516	473											
ISSV	0000 0512	472											
IV07	0000 0007												
IV08	0000 0008												
IV09	0000 0009												
IV0A	0000 000A												
IV0B	0000 000B												
IV0C	0000 000C												
IV0D	0000 000D												
IV0E	0000 000E												
IV0F	0000 000F												
IV17	0000 0017	116											
IV18	0000 0018												
L	0000 0318	3575											
LA	0000 032B	3437											
LB	0000 0381	3706	3723										
LBR	0000 0382	1611	3349										
LCDR	0000 05E0	3540											
LCER	0000 05D3	3506											

DROM2 VECTOR TABLE & FORMAT TABLE

LCS	0000 031B	3232		
LD	0000 0583	3609		
LDE	0000 05BA	3336		
LDER	0000 05C7	3659		
LDGR	0000 05C4	3369		
LDGR1	0000 05C9	3658		
LDPS	0000 04FD	471		
LDPS0	0000 0505	2045		
LDPS1	0000 0509	2048		
LDPS3	0000 0510	2056		
LDR	0000 0556	3252		
LE	0000 0564	2334	3592	
LED	0000 0564	3622		
LEDR	0000 05BD	3367		
LEFT	0000 0536			
LEGR	0000 05C3	3368		
LER	0000 0521	3235		
LEVEL0	0000 014F	90		
LEVEL1	0000 014D	92		
LEVEL2	0000 014B	94		
LGDR	0000 05A8	3505		
LGER	0000 05A6	3504		
LH	0000 0317	3558		
LHI	0000 0319	75	3405	
LHL	0000 031E	3604		
LI	0000 0319	3456		
LIS	0000 031A	3231		
LM	0000 0320	3415		
LM.ENT	0000 0327	188	2043	
LM1	0000 0324	1432		
LM71	0000 0519	193	2046	
LMD	0000 0598	3327		
LMD.010	0000 059A	2294		
LMD.ENT	0000 059E	196	2050	2299
LME	0000 057A	2240	3314	
LME.ENT	0000 057D	195	2049	2244
LMFAULT	0000 00AD	1438		
LMLOOP	0000 0323			
LOADLOOP	0000 0111	559		
LPB	0000 0737	3310		
LPB1	0000 0744	2925		
LPB1A	0000 074A	2912		
LPB2	0000 0754	2918		
LPDR	0000 05DB	3536		
LPER	0000 05CF	3502		
LPSTD	0000 00E1			
LPSW	0000 0122	3399		
LPSWR	0000 0120	3218		
LR	0000 0319	3201		
LRA	0000 032C	3298		
LRA.PRI	0000 0350	1470		
LRA.SH2	0000 0351	3587		
LRA.SHAR	0000 033F			
LRCCK	0000 019F			

DROM2 VECTOR TABLE & FORMAT TABLE

LSSTD	0000 00E2								
LSTD1	0000 04E9	468	469						
M	0000 02D6	3579							
MAT	0000 00AF	84							
MAT1	0000 00B0	403							
MAT1A	0000 00B1	371							
MD	0000 058B	3613							
MDR	0000 055B	3256							
ME	0000 056C	3596							
MEM.1	0000 0056	226							
MEMLOOP	0000 0053	230							
MEMMF	0000 0094	427	602	625	686				
MEMMF1	0000 0095	322	328						
MEMTEST	0000 0052	181	242						
MER	0000 0525	3239							
MH	0000 02D0	3562							
MHLOOP	0000 02D4								
MHR	0000 02D0	3205							
MINB1	0000 0762	2943							
MINUSBIN	0000 075F	2938							
MINUSLEN	0000 00FC	326	331	384	411	453	499	1720	2866
MISMATCH	0000 066C	2584							
MLOOP	0000 02D9								
MMFINT	0000 009A								
MOVE	0000 061D	2417							
MOVE0	0000 0622	2461	2463						
MOVE1	0000 0626								
MOVE1A	0000 0629	2499							
MOVE2	0000 0636	2483							
MOVE2A	0000 0635	2476							
MOVEP	0000 061D								
MR	0000 02D6	3222							
MVTU	0000 061D	2416							
MVTU2	0000 0630	2477							
N	0000 02B5	3571							
NEXTREQ	0000 041D	1781							
NFREAD	0000 0190								
NFWRIT	0000 0197	789							
NH	0000 02B4	3554							
NHI	0000 02B6	3401							
NI	0000 02B6	3452							
NORMAL	0000 0188	719							
NR	0000 02B6	3197							
O	0000 02B9	3573							
OC	0000 01C8	3717							
OCR	0000 01C9	3649							
OH	0000 02B8	3556							
OHI	0000 02BA	3403							
OI	0000 02BA	3454							
OR	0000 02BA	3199							
OUT.1	0000 048E	1898							
OUTCHR	0000 048C	1780	1787	1876	1880	1887	1889		
OUTCMD	0000 0023	1745							
OUTDEV	0000 0011	1743	1804	1894					

DROM2 VECTOR TABLE & FORMAT TABLE

OUTPUT	0000	0175	728										
OUTPUT.A	0000	0650	2486	2507	2509								
OUTPUT.Z	0000	064F	2490										
OVERFLO	0000	0543	2123	2130	2132								
PAD.0	0000	0641	2516										
PAD.1	0000	0648	2515										
PADIT	0000	0640	2472										
PB	0000	03DB	3297										
PBR	0000	03E0	3246										
PLUSBIN	0000	0763	2934	2940									
PMV	0000	0685	2419										
PMVA	0000	0685											
PMVFLAGS	0000	06C0	2740	2751	2758								
PMVL002	0000	06A7	2647										
PMVL002A	0000	06A8	2651										
PMVLP1	0000	0696	2663										
POW	0000	0086											
PPF	0000	0078	1994										
PPFCHK	0000	04DC	1739	1795	1897	1988							
PREG.0	0000	0475	1877										
PREG.05	0000	047A											
PREG.1	0000	047F	1874										
PREG.2	0000	0481	1866										
PRIV	0000	8000	3218	3337	3351	3354	3355	3356	3357	3359	3360	3399	3419	3422
			3423	3424	3425	3427	3428	3429	3433	3434	3436	3439		
PRNTREG	0000	0474	1862	1921										
PRNTREG6	0000	0471	1752	1755	1917	1979	1981							
PRNTREG8	0000	0473	1938	1950	1964	1966								
PROMPT	0000	0434	1757	1829										
PROMPTC	0000	003C	1759	1786										
PSF	0000	04E3	3429											
PSFTAB	0000	00E0	2003											
PUSH	0000	06E3	2734											
PUSH.1	0000	06E6	2745											
PUSHP	0000	06DE	2641											
PUSHU	0000	06E1	2810											
PUTAWAY	0000	053A												
PWRDWN	0000	0078	1726											
PWRDWN1	0000	0080	278											
PWRUP	0000	0037												
QTEST	0000	0126	2059	3507	3688									
QTEST1	0000	0127	3640											
QUESTN	0000	0430	1846	1852	1854	1944	1957	1976						
RBL	0000	026B	3302											
RBL.010	0000	0273	1105											
RBT	0000	0377	3607											
RD	0000	01E5	3714											
RDCS	0000	03CB	1675											
RDHALF	0000	0118	544	546	548	550	556							
RDR	0000	01E7	3646											
REDCHK	0000	019C	796											
REL	0000	04EA	457											
RH	0000	01D3	3712											
RHBR	0000	01DB	893											

DROM2 VECTOR TABLE & FORMAT TABLE

RHR	0000 01D9	3644
RI1	0000 4000	3689 3690 3691 3692 3693 3694 3695 3696 3697 3698 3699 3700
		3701 3722 3729 3730 3731 3732 3733 3734 3735
RI2	0000 0000	3740 3741 3742 3743 3744 3745 3746 3747 3748
RIGHT	0000 0547	2120
RISHFTF	0000 0281	3441 3442 3443 3444 3445 3446
RISHFTH	0000 0283	3409 3410 3411 3412
RLL	0000 026C	3731
RMVF	0000 04F8	
RR	0000 5000	3482 3483 3484 3485 3486 3487 3488 3489 3490 3491 3492 3493
		3494 3495 3496 3497 3499 3500 3501 3502 3503 3504 3505 3506
		3507 3508 3509 3510 3511 3512 3513 3514 3516 3517 3518 3519
		3520 3521 3522 3523 3524 3525 3526 3527 3528 3529 3530 3531
		3533 3534 3535 3536 3537 3538 3539 3540 3541 3542 3543 3544
		3545 3546 3547 3548 3564 3565 3569 3570 3618 3619 3621 3623
		3624 3626 3627 3628 3629 3631 3632 3633 3635 3636 3637 3638
		3639 3640 3641 3642 3643 3644 3645 3646 3647 3648 3649 3650
		3652 3653 3654 3655 3656 3657 3658 3659 3660 3661 3662 3663
		3664 3665 3666 3667 3669 3670 3671 3672 3673 3674 3675 3676
		3677 3678 3679 3680 3681 3682 3683 3684 3709 3710 3715 3724
		3728 3737 3738 3739 3749 3750 3751 3752
RRIO	0000 01C7	3354 3355 3356 3357 3359 3360 3422 3423 3425 3427
RRL	0000 028B	3730
RTL	0000 0259	3301
RTL.010	0000 0269	1094
RTRANSL	0000 01BA	793
RWBIT	0000 0004	727 738 1635
RWDCS	0000 03C1	3439
RX	0000 C000	3550 3551 3552 3553 3554 3555 3556 3557 3558 3559 3560 3561
		3562 3563 3567 3568 3571 3572 3573 3574 3575 3576 3577 3578
		3579 3580 3581 3582 3584 3585 3586 3587 3588 3589 3590 3591
		3592 3593 3594 3595 3596 3597 3598 3599 3601 3602 3603 3604
		3605 3606 3607 3608 3609 3610 3611 3612 3613 3614 3615 3616
		3620 3622 3625 3686 3687 3688 3703 3704 3705 3706 3707 3708
		3711 3712 3713 3714 3716 3717 3718 3720 3721 3723 3725 3726
		3727
RX.RX	0000 E000	3630
RXBIT	0000 036C	3316 3317 3318 3319
RXBYTE	0000 022E	3417 3418
RXF	0000 0232	3282 3284 3285 3286 3288 3303 3304 3305 3306 3307 3308
RXF1	0000 0234	1287
RXF2	0000 0233	3279 3283 3289 3290 3291
RXH	0000 022F	3265 3267 3268 3269 3271 3274 3315
RXH1	0000 0231	1280
RXH2	0000 0230	3266 3272 3273
RXIO	0000 01C6	3424 3428
RXRX	0000 0605	3341
RXRX1	0000 060E	2430
RXRX2	0000 0615	2437
RXRXTAB	0000 0600	2442
S	0000 02CF	3578
SBIT	0000 0020	807 825
SBT	0000 0372	3606
SCP	0000 03A6	3434

DROM2 VECTOR TABLE & FORMAT TABLE

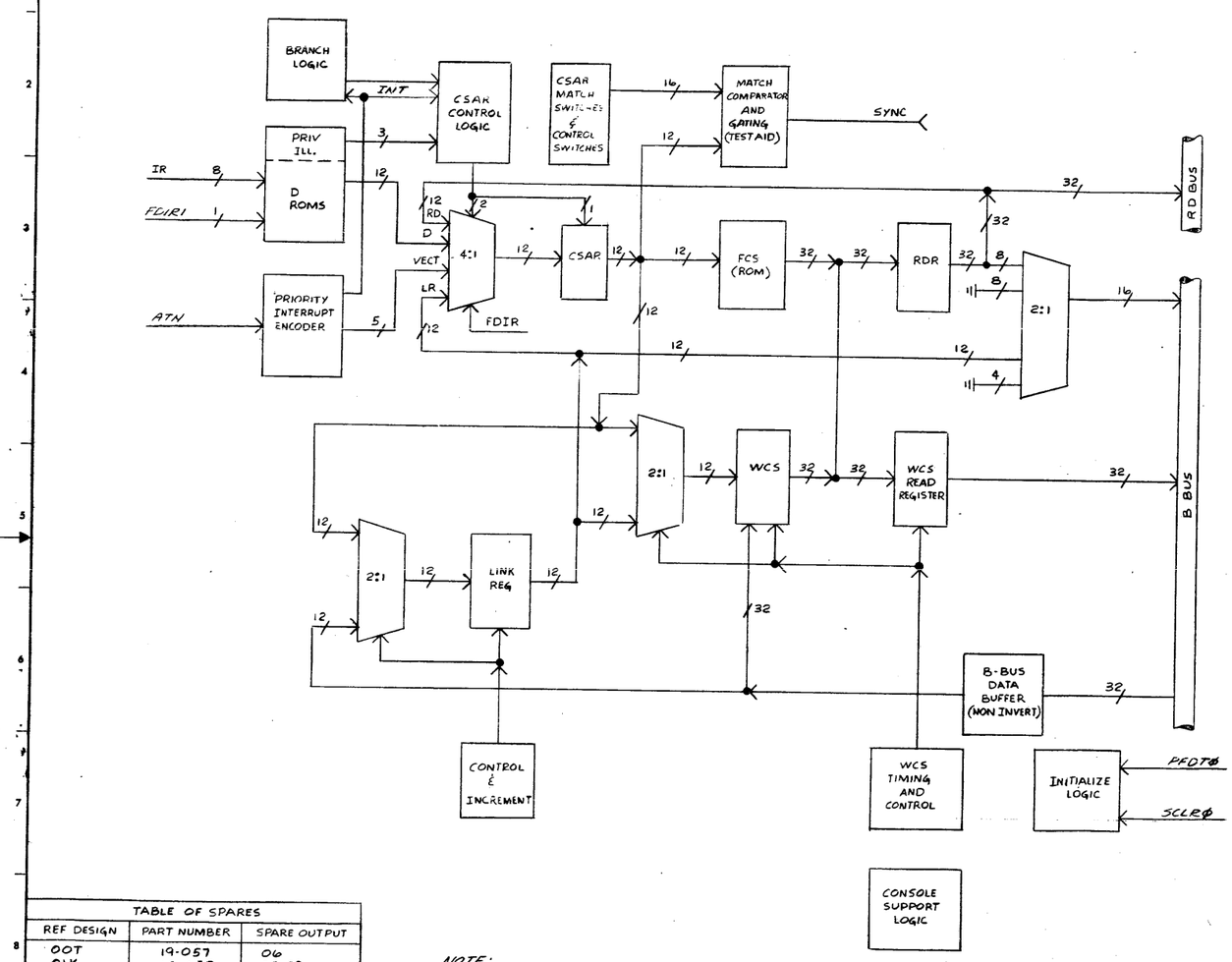
SCP.2	0000 03B4	1629
SCP.3	0000 03BB	1636
SD	0000 0589	3612
SDR	0000 055A	3255
SE	0000 056A	3595
SELFTEST	0000 0019	73
SER	0000 0525	3238
SET.RTN	0000 072F	2404 2407 2468 2502 2543 2621 2635 2731 2736 2763 2788 2803 2905 3026 3072 3113
SETCC0	0000 0225	931 1057 1075
SETCC1	0000 0226	
SETCC2	0000 0227	2955
SETCC4	0000 0229	1468 1484 1622
SETCC4A	0000 0228	1045 1063 1083 1103
SETCC8	0000 022B	1477 1493
SETCC8A	0000 022A	1456
SFSHFTF	0000 027C	3210 3211
SFSHFTH	0000 027E	3346 3347
SGMINUS	0000 06D8	2719
SGN.CHK	0000 06CD	2628 2793
SGN.CK1	0000 06D2	2714
SGPLUS	0000 06DC	2712 2717 2721
SH	0000 02CF	3561
SHI	0000 02CF	3408
SHOWLOC	0000 041B	
SHOWPSW	0000 0419	
SI	0000 02CF	3459
SINT	0000 0141	3433
SINT.1	0000 0149	652
SIS	0000 02CE	3234
SLA	0000 028F	3735
SLHA	0000 0289	3701
SLHL	0000 0287	3699
SLHLS	0000 0287	3636
SLL	0000 028E	3733
SLLS	0000 028E	3500
SMEPF	0000 008B	
SNGLC	0000 003E	1761
SPECFAUL	0000 00F2	490 491
SR	0000 02CF	3204
SRA	0000 028A	3734
SRHA	0000 0288	3700
SRHL	0000 0286	3698
SRHLS	0000 0286	3635
SRL	0000 028D	3732
SRLS	0000 028D	3499
SS	0000 01CD	3716
SSR	0000 01D0	3648
ST	0000 0363	3278
START	0000 0000	
STB	0000 0383	3415
STB.D2	0000 0235	3705
STBP	0000 0782	3309
STBP.001	0000 0794	3014

DROM2 VECTOR TABLE & FORMAT TABLE

STBP.002	0000 07A7	3040	3044					
STBP.003	0000 07AA							
STBP.004	0000 07AF	3054						
STBP.N1	0000 078F	3011						
STBP.NEG	0000 078C							
STBP.POS	0000 0791	3008						
STBP.SGN	0000 07DF							
STBP.Z1	0000 07D6	3100						
STBP.ZIP	0000 07D4	3017						
STBPL2.1	0000 07BA	3097						
STBPLP2	0000 07BC	3074						
STBPLP2B	0000 07C2	3598						
STBPLP2C	0000 07C9	3088						
STBPS.0	0000 07DD	3120						
STBPS.1	0000 07E3	3125						
STBPS.2	0000 05E4	3138						
STBPS.3	0000 05E6	2403						
STBPSTOR	0000 07D7	3076						
STBR	0000 0384	3348						
STD	0000 0570	3312						
STDE	0000 05AC	3331						
STE	0000 0563	3295						
STF.D2	0000 0237	2320	2330	2331	3567	3584	3601	
STH	0000 0363	3261						
STH.D2	0000 0236	3550	3581	3582	3585	3586	3589	
STM	0000 0364	3414						
STM.ENT	0000 0368	276	2029					
STM71	0000 051D	280	2032					
STMD	0000 058F	2036	3326					
STMD.ENT	0000 0594	283						
STME	0000 0572	3313						
STME.ENT	0000 0577	282	2035	2234				
STME1	0000 0574	2230						
STMLOOP	0000 0367							
STORBYTE	0000 06B9	2632	2660	2743	2800			
STPS	0000 04EE	470						
STPS1	0000 04FB	2034						
SVC	0000 013B	3432						
SWAP	0000 05A3	3215	3216					
SYSQINT	0000 0131							
TBIT	0000 0302	792	800					
TBT	0000 0380	3605						
TENXOVF	0000 0781	2968	2973	2978				
TENXPL1	0000 077B	2975						
TENXPLUS	0000 076B	2921	2923	2929				
TERMCHAR	0000 0633							
THI	0000 02B3	3400						
TI	0000 02B3	3451						
TLATE	0000 039F	3438						
TLSU	0000 0101	204	254					
TMMF	0000 0098	210	318	336	561			
TRANSL	0000 01BB	801						
TRYMOD	0000 0456	1922	1939	1951	1967	1982		
TS	0000 0361	3431						

DROM2 VECTOR TABLE & FORMAT TABLE

TWAIT	0000 0011	341	359	392	394	414	461	515	518	595	603	624	759
TXA1	0000 001A	140											
UFAULT	0000 00D4	445											
UMV	0000 06FC	2420											
UMVA	0000 06FC												
UMVLP1	0000 070F	2834											
UMVLP2	0000 0717	2814											
UMVLP3	0000 0720	2821											
UNDRFLO	0000 0542	2117											
WAIT	0000 0012	106											
WARM.1	0000 003F	191											
WARMSTRT	0000 0038												
WCSENA	0000 1000	3436	3440										
WCSLO	0000 0800	1646	3191										
WD	0000 01E9	3713											
WDCS	0000 03D3	1665	1685										
WDR	0000 01E3	3645											
WH	0000 01DD	3711											
WHB	0000 01DE												
WHH	0000 01DF	898											
WHR	0000 01E1	3643											
WHRB	0000 01E2												
WHRH	0000 01E3	904											
X	0000 02BC	3574											
XH	0000 02BB	3557											
XHI	0000 02BD	3404											
XI	0000 02BD	3455											
XR	0000 02BD	3200											
XSTB	0000 00E7												



NOTE;
FOR NET #, MNEMONIC, & LOCATION TO SCHEMATIC SEE SHT 16.

TABLE OF SPARES		
REF DESIGN	PART NUMBER	SPARE OUTPUT
00T	19-057	06
01K	19-055	03,08
06S	19-060	06
11E	19-063	09/08
12S	19-062	01
16T	19-124	03,06,08

REVISION	2	1	1	0	0	0	0	0	1	0	1	0	1	2	1	1
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

FUNCTIONAL VARATION TABLE		
PART #	DESCRIPTION	
35-767F01 35-767 F03	WITHOUT WCS FUNCT.	AS SHOWN, LESS ICS AND DISCRETE COMPONENTS IDENTIFIED WITH AN ASTERISK.(*)
35-767F02 35-767 F04	WITH WCS FUNCTION	AS SHOWN, WITH ICS AND DISCRETE COMPONENTS IDENTIFIED WITH AN ASTERISK. (*)

CONN	TERM. NO.	CABLE CONNECTOR MAP ROW 2	CABLE CONNECTOR MAP ROW 1
5	16	MEXTØ	GND
	15	MWCSØ	GND
	14	MSNGLØ	GND
	13	MATCHØ	GND
	12	MAT20I	GND
	11	MAT21I	GND
	10	MAT22I	GND
	09	MAT23I	GND
	08		
	07	MAT24I	GND
	06	MAT25I	GND
	05	MAT26I	GND
	04	MAT27I	GND
	03	MAT28I	GND
	02	MAT29I	GND
	01	MAT30I	GND
	00	MAT31I	GND
4	24		
	23		
	22		
	21		
	20		
	19		
	18		
	17		
	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		
3	24	GND	GND
	23	CSAR30Ø	CSAR31Ø
	22	CSAR28Ø	CSAR29Ø
	21	GND	CSAR27Ø
	20	CSAR26Ø	CSAR25Ø
	19	CSAR24Ø	
	18	CSAR22Ø	CSAR23Ø
	17	GND	CSAR21Ø
	16	CSAR20Ø	CSAR19Ø
	15	GND	GND
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		P5
	02		
	01		
	00		
2	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		

CONN	TERM. NO.	BACK PANEL MAP ROW 1	BACK PANEL MAP ROW 2
1	41	P5	P5
	40	GND	GND
	39	SR1Ø	SRØØ
	38	MPYØ	SMØ
	37	DIVØ	ULSRØ
	36	GRDI01	ENBSØ
	35	GRDØ91	GRD111
	34	RD221	RD231
	33	RD201	RD211
	32	RDI9Ø	RD191
	31	RDI7Ø	RD181
	30	RD27Ø	RD271
	29	RD251	RD261
	28	RD240	RD121
	27	RD141	RD131
	26	RD15Ø	RD161
	25	RDØ01	RDØ11
	24	RDØ21	RDØ31
	23	RDØ41	RDØ51
	22	RD301	RD311
	21	GND	GND
	20	RDØ9Ø	RD100
	19	RD11Ø	FDØ20
	18	RD281	RD291
	17	PSW201	PSW231
	16	PSW261	PSW271
	15	PSW131	PSW231
	14	PSW171	PSW181
	13	AENHØ	AENLØ
	12	IRØ7Ø	IRØ60
	11	IRØ5Ø	IRØ4Ø
	10	IR Ø3Ø	IRØ2Ø
	09	IR Ø1Ø	IRØØØ
	08	YDØ81	YDØ91
	07	YD101	YD111
	06	FLR281	FLR291
	05	FLR301	FLR311
	04	GFLR291	LFLRØ
	03	EPPFLTØ	BSTKSØ
	02	SMINTØ	JAMCIØ
	01	GND	GND
	00	P5	GND
0	41	P5	GND
	40	GND	GND
	39	CLKIA	CLKPSWØ
	38	CLKCCØ	SCLKI
	37	GND	GND
	36	GDIRØ	SVØ
	35	OPSTOPØ	DSTOPØ
	34	FPPFØ	RSTOPØ
	33	CLØ7Ø	UNNLDØ
	32	PFDTØ	WAITI
	31	SFTENØ	DFTENØ
	30	ATNØØØ	ATNØ1Ø
	29	ATNØ2Ø	ATNØ3Ø
	28	GND	GND
	27	BØØ1	BØ11
	26	BØ21	BØ31
	25	BØ41	BØ51
	24	BØ61	BØ71
	23	BØ81	BØ91
	22	B101	B111
	21	B121	B131
	20	B141	B151
	19	B161	B171
	18	B181	B191
	17	B201	B211
	16	B221	B231
	15	B241	B251
	14	B261	B271
	13	B281	B291
	12	B301	B311
	11	GND	GND
	10	HWØ	RCATNØ
	09	SCATNØ	TRAPØ
	08	SINGLØ	NVESØ
	07	MATØ	SCLR0
	06	DEXTØ	SCLES1
	05	FNCEØ	SCLR08
	04	DEXBØ	ALGNØ
	03	GMVFØ	DISAØ
	02	PRDY1	DISBØ
	01	GND	GND
	00	P5	GND

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

PRE PRODUCTION APPROVAL	INIT.	DATE
DEV PROD	JAC	6/30/82

WFA 49, REVISED SHEET REVISION1 RECORD; AREA 5B, 35-1467 F01-F04 WAS R00; SHEET 2, AREA AS REVISED SHEET 16, ANCHOR PADS WERE REVISED.

AW	4490	M	7-26-82	KO1	

RELEASED FOR PRODUCTION
ENG. JAC DATE 11/17/82

SPARE GATE LIST, ADDED 01K08 & DELETED 03M06. 4 02W08. REVISED SHTS 1, 3, 9, 11, 13 & 16.

KR	5114	MS	7-23-82	R02	

USED IN MANUAL 47-004

35-767 F04	R05
35-767 F03	R05
35-767 F02	R01
35-767 F01	R01
BOARD	REV. LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BEAT LEAST THE FOLLOWING REVISION LEVEL

SCALE	NAME	TITLE	DATE
TOLERANCE .XXX ± .025, .XX ± .02, .X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	D STINE	DRFT	4-27-78
	E GREENFIELD	SYS TEST	11-19-80
	R CLEAD	CHK	11-19-80
	E MARSH	ENGR	11-19-80
	R ABARKER	QC	11-19-80
	J FRANKENBERGER	MGR	11-19-80

TITLE FUNCTIONAL SCHEMATIC CPU-A

TASK NO. 03976 SHEET OF 1—16
DWG NO. 35-767R02D08

BRUNING 44-231-24538

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS					
AREA A5; 102-7 & 103-7 WERE 202-7 & 203-7 RESP.					
	UP	4490	M	9-29-80	R01

B A
0 0 LINK
0 1 RD
1 0 INT
1 1 DD

INPUT2 / INPUT1 4 TO 1 MUX 19-116
06H 3K9 LR20L 3K9 LD16L 9C9 DD28L 10F9 GDTEIA 3E6 VSELA0 3L2 VSELB0 3E3
06J 3K9 LR22L 3K9 LD18L 9D9 DD22L 10F9
07H 3F9 LR23L 3K9 LD19L 9D9 DD23L 10F9
07J 3F9 LE24L 3F9 LD20L 9E9 DD24L 10H9 4DTRL 3E5
08H 3M9 LE25L 3L9 LD21L 9F9 DD25L 10H9
08J 3N9 LE26L 3M9 LD22L 9G9 DD26L 10H9
3N9 LR27L 3N9 LD28L 9H9 FRFELT 13A8 DD27L 10H9
3N9 LE28L 3N9 LD24L 9H9 VECT2L 13H7 DD28L 10J9
3N9 LR29L 3N9 LD25L 9J9 VECT1L 13H6 DD29L 10J9
3N9 LR30L 3N9 LD26L 9H9 VECT2L 13H6 DD30L 10J9
3N9 LR31L 3N9 LD27L 9K9 VECT3L 13H5 DD31L 10J9

3E8 FESCAP0
14M3 SCLR0D
12D2 ECLK1
3E4 LDCSAR0
102-7 TP3 ENCSAR1
103-7 TP4
P5 42 05E 1K 01
C1-C10 P5 15μF, 25V .1μF
101 CAPS UNSPECIFIED DECOUPLING

06F 07F 08F 19-135 4 BIT CNTR OUTPUTS D C B A INPUTS
NC.
SCLR0D 14M3

380,482,3J3, CSAR20L 104B,15D7,15G6
216-3 CSAR20H
15D6 104B,481,3J3, CSAR21L
116-3 CSAR21H
382,SAR2,482,3K3, CSAR22L 15D6
218-3 CSAR22H
382,SAR3,482,3K3, CSAR23L 15D5
117-3 CSAR23H
382,SAR4,482,3L3, CSAR24L 15D5
219-3 CSAR24H
382,SAR5,482,3L3, CSAR25L 15D4
116-3 CSAR25H
383,SAR3,483,3L3 CSAR26L 15D4
220-3 CSAR26H
384,SAR4,483,3M3 CSAR27L 15D4
120-3 CSAR27H
SR1 RDCLR0
384,SAR4,483,3M3 CSAR28L 15D3
222-3 CSAR28H
384,SAR4,483,3N3 CSAR29L 15D2
121-3 CSAR29H
15D2, SAR5,483,3N3 CSAR30L
223-3 CSAR30H
15D2, SAR5,483,3N5 CSAR31L
122-3 CSAR31H

NOTE
1, X'007' - ILLEGAL
X'004' - POWER UP

SCALE –
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

	NAME	TITLE	DATE
	J HELVATY	DRAFT	4-27-78
	W LIMPERT	CHK	
		ENGR	

TITLE CPU-A CONTROL STORE ADDRESS REG. (CSAR)
TABS NO. 03976
DWG NO. 35-767201 DOB
SHEET OF 2 — 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA F4, DELETED 11M4 FROM BRANCH1.				
KR 411	SSIA	MS	7-23-82	R01

9F4 RD06Ø
11R3 TBRCH1
9N4 RD15Ø
09 10 09Q 19-236 SA 08
11R2 TBRCHØ
9G5 RD06Ø1
9F4,B4 RD05Ø
9E4 RD04Ø1
13E9 MACMPEØ
E8 FDIR1
11 12 13 01 04 05 06 09 10 02 03 BRANCH FALSE; BRANCH TRUE; D2; D1 MACMPE
08 09H 19-062 SG
9M4 RD13Ø 12
13H8 INT1 13
01K 19-055 SG 11
11R4 GBRCH1
03 08 05 09S 19-058 SG 06 VSELBØ 2B1
05 04 01K 19-055 SG 06
9F4 RD05Ø1
11 10 10D 19-057 SG 10 BRANCH1 12K6,13B2
04 09Q 19-236 SA 06
9F4,B2 RD05Ø
05 03
11R3 FBRCH1
11R4 TBRCH1
13 01 04K 19-041 SN 05 LOCSAEØ 2A5
09 08 10D 19-057 SG
02 03 12 13 01 02 04 09F 19-241 SN 05 GDIR1 2F1
13H8 INT1
11D5 DIREØ
9B4 RD04Ø1 09
9C4 RD01Ø 10
9C4 RD02Ø 12
9E4 RD03Ø 13
06S 19-060 SG 08
11 12 13 01 02 04 10 09 08 09F 19-241 SN 06 GDIR1A 2B1
13 16K 19-057 SG 12 GDIREØ 136-Ø
XRPB 10J4
10 12 DS D 09 02H 19-063 SDF DC FDIR1 F1,10D8,13E9,R3
11 DC D 08 FDIREØ 11B4,13H7
13
12D3 RCLKØA
14M3 SCLREØD
01 03 06 FESCAPO 2A4
DC D 02H 19-063 SDF
02 05 NC
DS D
04
11A4 SNGL1A 03
11F4 CATN1 04
2C9 CSAR2Ø1 05
07S 19-059 SA 06

10K9 FLTILL1
11S-1 PSW13Ø 01
04J 19-057 SG 09
10 11 08J 19-058 SG 08
11H5 FPP1
E8 FDIR1
10K9 PRIV1
21S-1 PSW23Ø
10K9 COMILL1
11 12 13 01 04 05 06 09 10 02 03 D1 FLT; D1 PRIV; D1 ILL; EXPANSION
08 VSELAØ 2B2
09J 19-062 SG

8B2 LDLR1
12J4 LDLRØ
05 06 10D 19-057 SG LDLR1
09 08 09G 19-236 SA
01 02 10C 19-055 SG 03 10 09E 19-236 SA 08
12 09E 19-236 SA 11
9M5 RD14Ø 13
12D3 RCLKØA
12D5 SCLKØA
10F3 WCS1
11 12 13 01 02 03 04 05 06 09 10 LINK; WCS INC; LINK INC; LOAD LINK
08 09D 19-062 SG
12D5 SCLK1A
12D2 RCLK1
LRCLKØ
14M3 SCLREØD

CSAR2Ø1 2C9; B2ØIA 7K4; CSAR211 2D9; B211A 7L4; CSAR221 2D9; B221A 7M4; CSAR231 2E9; B231A 7N4
CSAR241 2G9; B241A 8E4; CSAR251 2H9; B251A 8F4; CSAR261 2H9; B261A 8G4; CSAR271 2J9; B271A 8J4
CSAR281 2L9; B281A 8K4; CSAR291 2M9; B291A 8L4; CSAR3Ø1 2N9; B3Ø1A 8M4; CSAR311 2N9; B311A 8N4
02 03 05 06 11 10 14 13 1A 1B 2A 2B 3A 3B 4A 4B
01 SEL 06E 19-065 2TO1 MUX ENB 15
SEL 07E 19-065 2TO1 MUX
SEL 08E 19-065 2TO1 MUX
1Y 2Y 3Y 4Y
04 07 09 12
07 10 02 06 05 04 03 ENP ENT CLK D C B A INPUTS
09 LD CAR 06D 4 BIT CNTR OUTPUTS 15 11 12 13 14 NC
07D 4 BIT CNTR OUTPUTS
08D 4 BIT CNTR OUTPUTS
19-135 CL 01
XRPB 10J4
LR2Ø1 12K3,1043,2B1; LR211 10K3,12K9,2C1; LR221 7M1,12K3,5A1,2D1; LR231 12K9,7A2,5A2,2E1
LR241 12K5,7A2,5A2,2F1; LR251 12K5,7A2,5B2,2G1; LR261 12K5,7A3,5A3,2H1; LR271 12K10,7A3,5A3,2J1
LR281 12K6,7A4,5A4,2K1; LR291 12K7,7A4,5B4,2L1; LR2301 12K7,5A5,2M1; LR311 12K7,5A5,2N1

SCALE—
TOLERANCE: XXX ± .005; XX ± .02; X ± .03; ANGLES ± 1°; UNLESS OTHERWISE SPECIFIED

	NAME	TITLE	DATE
	D STINE	DRAFT	4-27-78
		CHK	
		ENGR	

TITLE CPU-A
LINK REGISTER
TASK NO. 03976
DWG. NO. 35-767 R01 D08
SHEET OF 3—16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

SEE NOTE 1
TYP. 8 PLACES

02B * 19-220 (F12)(F20) 1024 x 8 ROM
02F * 19-220 (F13)(F21) 1024 x 8 ROM
11B * 19-220 (F14)(F22) 1024 x 8 ROM
11F * 19-220 (F15)(F23) 1024 x 8 ROM
05B * 19-220 (F16)(F24) 1024 x 8 ROM
05F * 19-220 (F17)(F25) 1024 x 8 ROM
14B * 19-220 (F18)(F26) 1024 x 8 ROM
14F * 19-220 (F19)(F27) 1024 x 8 ROM

CSAR211 2D9
CSAR201 2C9
CSAR221 2D9
CSAR231 2E9
CSAR241 2G9
CSAR251 2H9
CSAR261 2H9
CSAR271 2J9
CSAR281 2L9
CSAR291 2M9
CSAR301 2M9
CSAR311 2N9

P5
05E
DISDEM1 10E6
DISCS0 10N2
FWCSEX1 10N8
WCSSEL0 10E5
10K
1K
1K
09E 19-236 5A

FCS PAGE 0 '000'X - '3FF'X

FCS PAGE 1 '400'X - '7FF'X

STRAP OPTIONS - LOCATION 05E	
PIN TO PIN	FUNCTION
02 NC	D AND PEIV/ILL ROMS DISABLED
02 08	D AND PEIV/ILL ROMS ENABLED
03 NC	ALL CONTROL STORE ENABLED
03 08	ALL CONTROL STORE DISABLED

NOTE : SRD'S 'OE' TIED AS FOLLOWED
SRD000 - SRD071 SHEET 5
SRD081 - SRD151 SHEET 6
SRD161 - SRD231 SHEET 7
SRD241 - SRD311 SHEET 8

NOTES:
1. 19-220 F12 THRU F19 USED WITH 35-767 F01 & F02
   19-220 F20 THRU F27 USED WITH 35-767 F03 & F04

SCALE—
TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

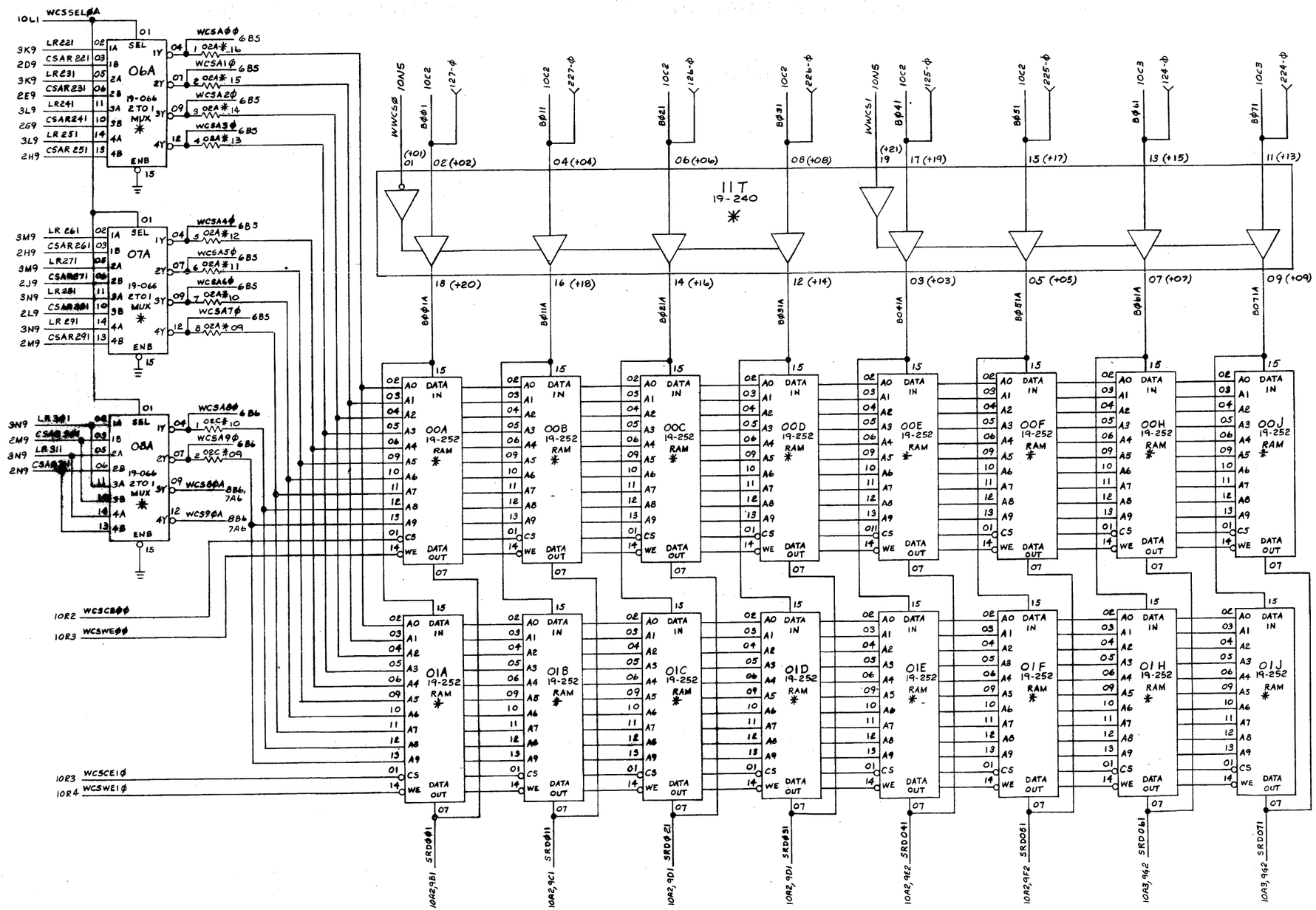
NAME	TITLE	DATE
TD STINE	DRAFT	4-27-78
	CHK	
	ENGR	

TITLE
CPU-A
FIXED CONTROL STORE

TASK NO. 03976
DWG NO. 35-767 DOB
SHEET 4 OF 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 47 OHM
2. "SRD" ØØ1-"SRD"Ø71 "OR" TIED TO SHT. 4 SRD'S.
3. PARTS MARKED WITH "*" NOT EQUIPPED WITH 35-767 F01 AND F03

SCALE – ~

	NAME	TITLE	DATE
	A. WILLIAMS/D.S.	DRAFT	4-27-78
		CHK	
		ENGR	

TOLERANCE: XXX ± .005; XX ± .02; X ± .03; ANGLES ± 1°; UNLESS OTHERWISE SPECIFIED

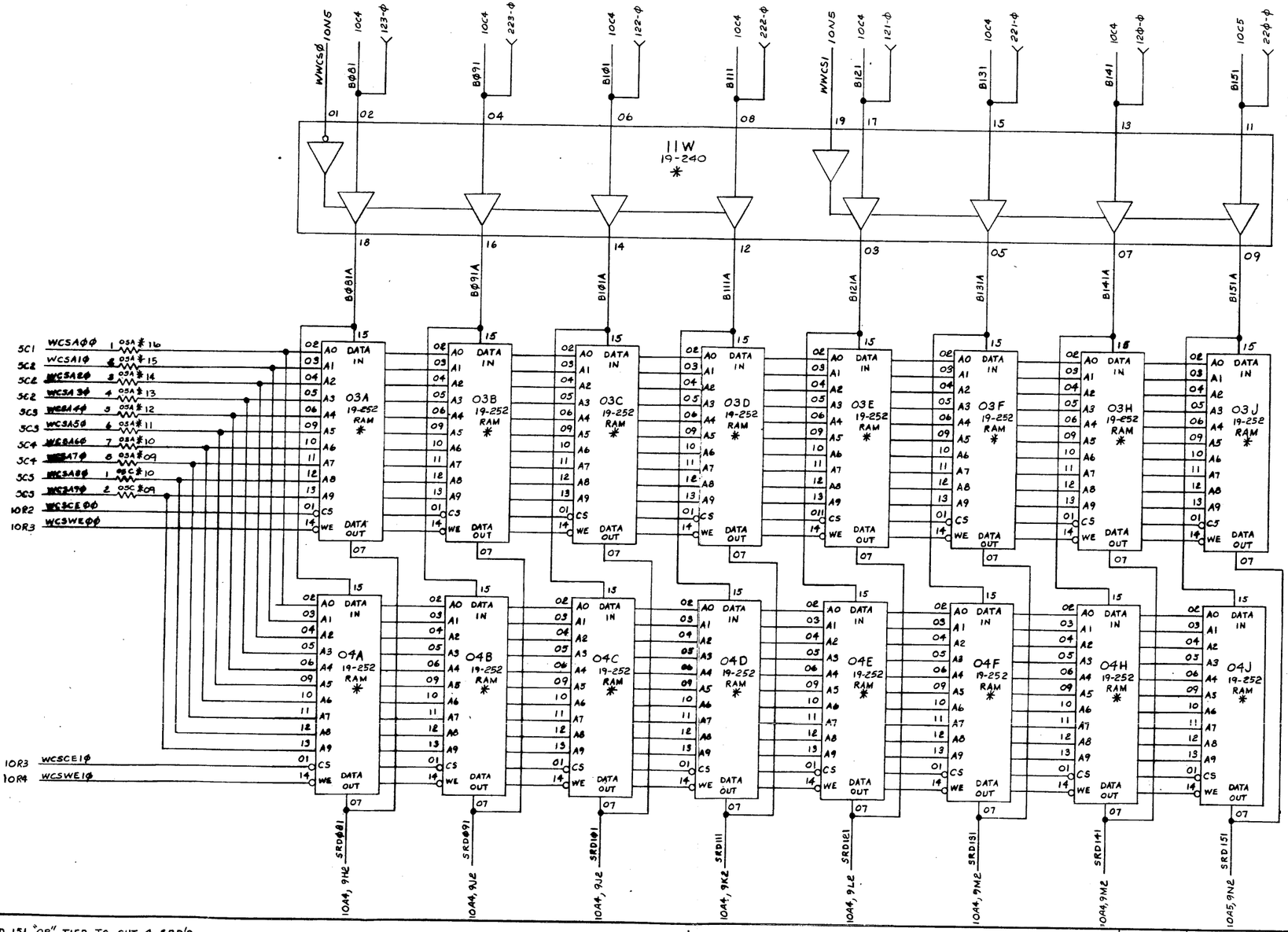
TITLE: CPU-A WCS

TASK NO. 03976 | SHEET OF 5–16

DWG NO. 35-767 D08

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



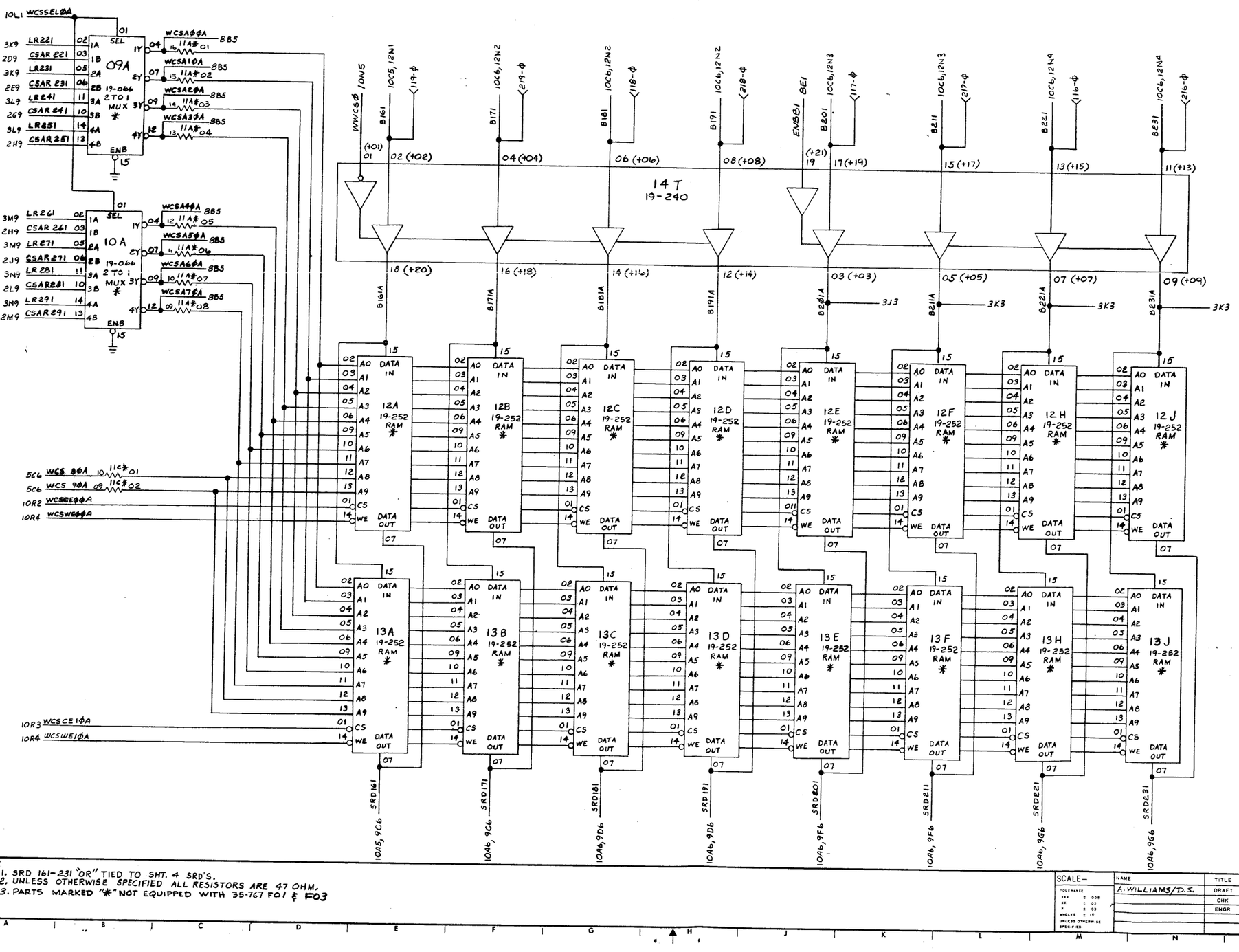
NOTES:
1. SRD Ø81–SRD 151 "OR" TIED TO SHT. 4 SRD'S.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 47 OHM.
3. PARTS MARKED WITH "*" NOT EQUIPPED WITH 35-767F01 AND F03

SCALE–	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .05, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	TESTINE	DRAFT	4-27-78
		CHK	
		ENGR	

TITLE: CPU-A WCS
CLASS NO. 03976
DWG NO. 36-767 D08
SHEET 6 OF 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



NOTES:
1. SRD 161-231 "OR" TIED TO SHT. 4 SRD'S.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 47 OHM.
3. PARTS MARKED "*" NOT EQUIPPED WITH 35-767 F01 & F03

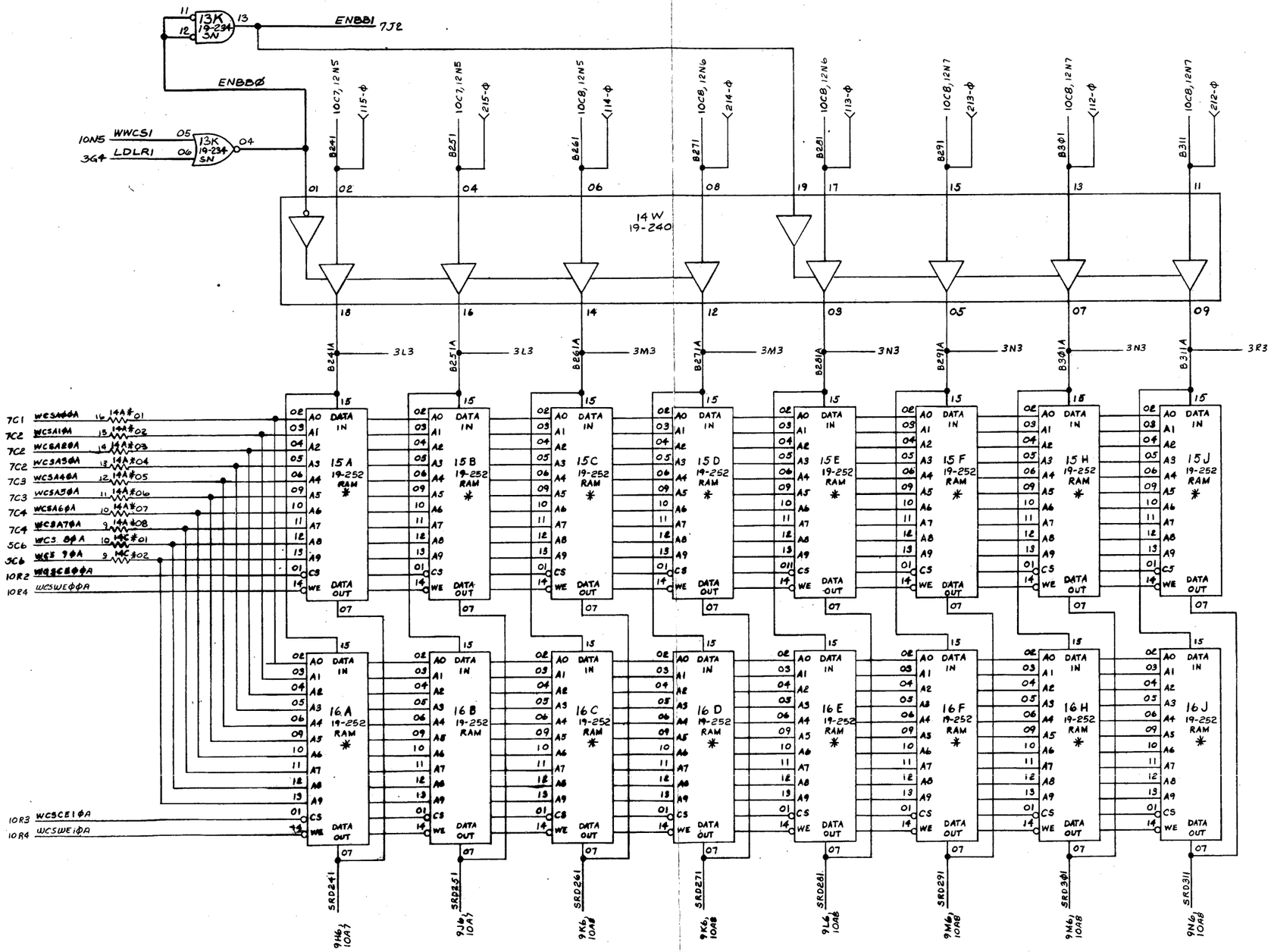
SCALE–	NAME	TITLE	DATE
TOLERANCE .XX ± .005, .X ± .02, .# ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	A. WILLIAMS/D.S.	DRAFT	4-27-78
		CHK	
		ENGR	

TITLE: CPU-A WCS

DWG. NO. 03976
DWG. NO. 35-767 D08
SHEET OF 7 — 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



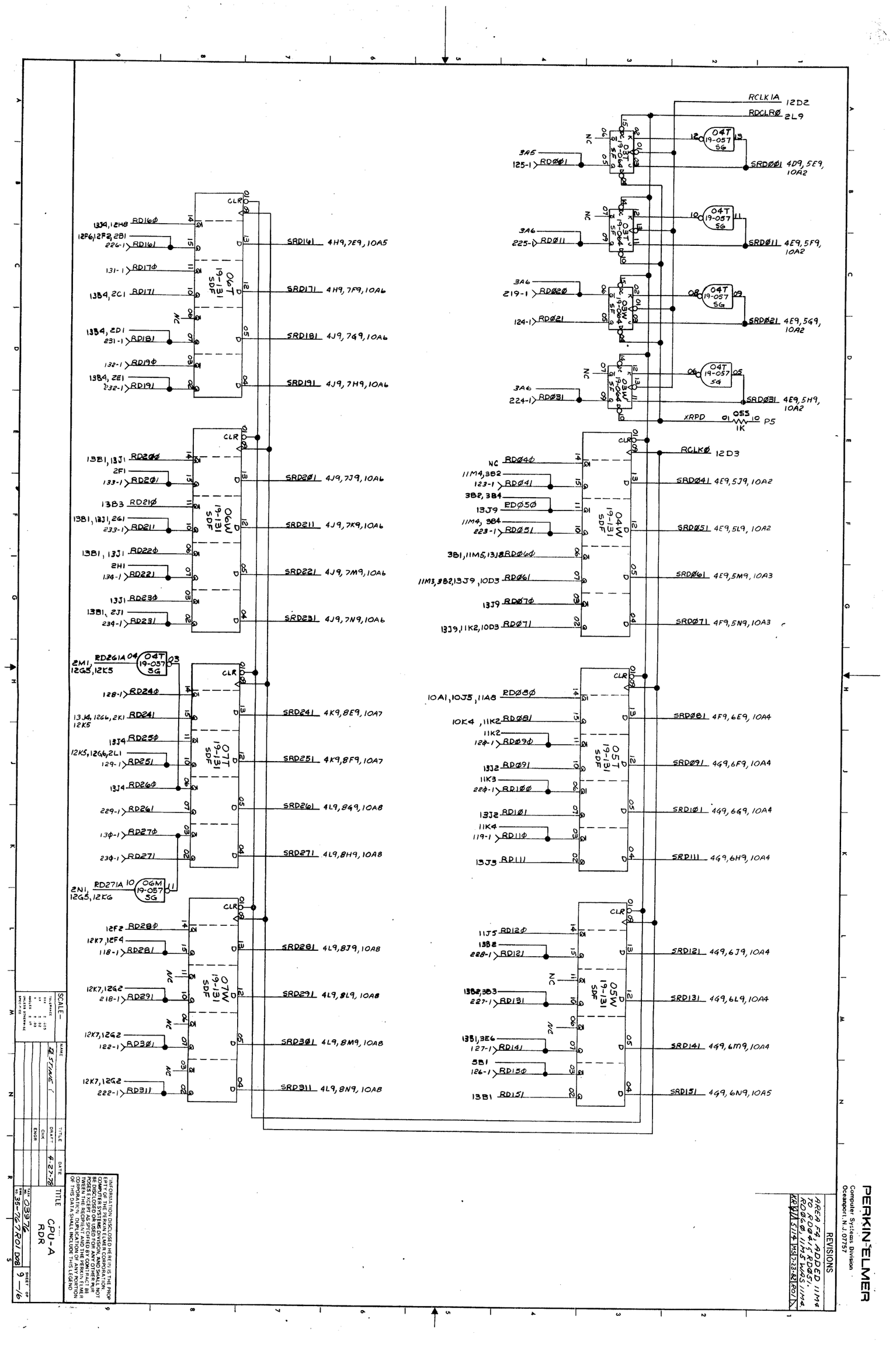
NOTES:
1. SRD 241-251 "OR" TIED TO SHT. 4 SRD'S.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 47 OHM.
3. PARTS MARKED WITH "*" NOT EQUIPPED WITH 35-767 F01 & F03

SCALE –
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

	NAME	TITLE	DATE
	TESTING	DRAFT	4-27-78
		CHK	
		ENGR	

TITLE
CPU-A
WCS

FSCM NO. 03376
DWG NO. 35-767 D08
SHEET 8 OF 16



PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS		
AREA FX, ADDED 11M4 TO RD04-15 RD05-, RD06-0, 11M5 WAS 11M4.	KRM	5/14/82

SCALE—

NAME	DATE
R. STONE	4-27-82
DRAFT	
CHK	
ENGR	

TITLE
CPU-A
RDR

REV	DWG NO
033-76	36-076 ROI D08

SHEET OF 9 —16

REVISIONS

WCS
TIMING & CONTROL

19-188 F25 WITHOUT WCS OPTION
19-188 F27 WITH WCS OPTION

35-767 F01 & F02 USES	35-767 F03 & F04 USES
POSITION	POSITION
10E = FB3	10E = FB6
10F = FB4	10F = FB7
10H = FB5	10H = FB8

NOTES:
1. PARTS MARKED WITH "*" NOT EQUIPPED WITH 35-767 F01 & F03
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 47 OHMS

SCALE – ~
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
A. WILLIAMS/D.S	DRAFT	4-27-78
	CHK	
	ENGR	

TITLE: CPU-A
WCS
CONTROL & LATCH AND DROM

TASK NO. 03976 | SHEET OF 10—16
DWG NO. 35-767 D08

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA M4, ADDED 03M06 & 02W08. DELETED 01K08 WHICH WAS TO 13K09				
KR	1	S114	MS	7-23-82

214-1 PSW181
1464 FSMINTØ
14H1 FEPFØ
14H2 FPPF1
13D9
1Ø5-Ø ENCED
12J3 CCATNØ
12D3 BCLKØA
14M3 SCLRØD
1Ø8-Ø SNGLØ
14F7 SETSNGLØ
3B9 SNGLIA
3E8 FDIRØ
1Ø9-Ø SCATNØ
21Ø-Ø RCATNØ
1Ø3-Ø GMVFØ
11Ø-Ø HWØ
P5
16M 1K, ¼W
10K 19-131 SDF
10M 19-055 SG
15M 19-153 LG
16K 19-057 SG
10S 19-235 SOR
12M 19-059 SA
16S 19-055 SG
08T 19-058 SG
12K 19-165 LDF
10S 19-235 SOR
16K 19-057 SG
16K 19-057 SG
14E2 XRPJ
GSNGLØ 13F9, 13D9
DIRØ 3B5
CATNI 3B9
NC
N.C.
FSPPFØ 13D8
FSMPEØ N.C.
FSCATNØ 13D8
MATØ 1Ø7-Ø
13D9, 13F9
E8 1Ø6-1 FLR281
SEE NOTE 05M1 (A) (G) 13
COMMI 05M P5 01 1K 16
13H8 INTI
13J2 2Ø6-1 FLR291
MATI
14H1 FEPFI
E7 1Ø5-1 FLR3Ø1
SEE NOTE 2 05M (C) FPPI (G) P5 03 1K 14
3F1
E7 2Ø5-1 FLR311
FCATNI
1Ø8-1 YDØØ1
2Ø8-1 YDØ091
1Ø7-1 YD1Ø1
2Ø7-1 YD111
14B6 YDØØ1
14B6 YDØ091
14B6 YD1Ø1
14B6 YD111
07K 19-116 4 TO 1 MUX
08K 19-116 4 TO 1 MUX
9J5 RDØ9Ø
9G5 RDØ71
9H5 RDØ81
9J5 RDI ØØ
9K5 RDI1Ø
9L5 RDI2Ø
STB 1
SEL B
SEL A
STB 2
1Y 07
2Y 09
HW1
09K 19-131 SDF
H5 FLR311
H4 FLR3Ø1
13N1 GFLR291
H1 FLR281
APSW311
APSW3Ø1
APSW291
APSW281
N.C.
07M 19-062 SG
08 03 06M 19-057 SG 04 MSK1
AUX PSW
BRANCHØ 3E4
TBRCHØ 3B2
TBRCHI 3B1
FBRCHI 3B4
GBRCHI 3C3
TRBRCHI 3B4
3B2 RDØ61
9F4 RDØ41
9F4 RDØ51
RDØ6ØA
9F4 RDØ6Ø
10D 19-057 SG
09C 19-236 SA
08M 19-235 SOR
13K 19-234 SN
03M 19-058 SG
02W 19-236 SA
06K A-291 SN
14E2 XRPJ
RDØ5Ø
10F3 WCS1
12D4 DCLKØ
13M 19-165 LDF
13K 19-234 SN
12E5 SCLKØA
10M 19-055 SG
138-Ø CLKCCØ
14M3 SCLRØD

NOTES,
1. STRAP A TO G FOR COMM OPTION NOT PRESENT LEAVE OPEN FOR COMM OPTION PRESENT.
2. STRAP C TO G, FOR FLOATING POINT PROCESSOR NOT PRESENT, LEAVE OPEN FOR FPP PRESENT.

SCALE— TOLERANCE .XXX ± .005 .XX ± .02 .X ± .03 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
D STINE	DRAFT	4-27-78
	CHK	
	ENGR	

TITLE CPU-A CONSOLE SYNC & BRANCH CONDITIONING

TASK NO. 03376 SHEET 11 OF 16
DWG NO. 35-767 R01 DOB

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

P5 03 — 02S 1K — 08
B5,15D7 XEPK
139-Ø CLKIA
02T 19-058 SG — 04, 05 — 06 BCLKØ → 10F5, 15G5
01
234-Ø ESTOPØ
02T 22 — 31 32 — 21 — 220µF, 100Ω
02W 19-236 SA — 02 — 03 RCLK1 → 2A4, 3E7
04
02W 19-236 SA — 05 — 06 RCLK1A → 9A1, 14B7
01
01W 19-124 SB — 02 — 03 RCLKØ → 9E2
04
01W 19-124 SB — 05 — 06 ECLKØA → 3B8, 3F6, 11B3, 13B8, 14J1
235-Ø DSTOPØ
09
01W 19-124 SB — 10 — 08 DCLKØ → 11B9, 13B3
B2 XRPK 13
238-Ø SCLK1 12
02W 19-236 SA — 11 SCLK1A → 3E6, 10L5
13
10D 19-057 SG — 12 SCLKØA → 3E6, 10H5, 11D8

9N9 RD311
9M9 RD301
9M9 RD291
9C9 RD161
3E5 BRANCHØ
9L9 RD280
09T 19-129 3TO8 DECODER — SEL B C, ENB G2A G2B G1
Y0 N.C. · Y1 SWAØ → 14J1 · Y2 N.C. · Y3 N.C. · Y4 N.C. · Y5 JAMCIØ → 2Ø2-1 · Y6 MPYØ → 13B-1 · Y7 MPYØ 13B3 → 13J-1
09W 19-236 SA — 03
09W 19-129 3TO8 DECODER — SEL B C, ENB G2A G2B G1
Y0 DIVØ 13B3 · Y1 YOFENØ 14B6 · Y2 UNNLDØ 233-Ø · Y3 CCATNØ 11B2 · Y4 DWSHFTØ 13A3 · Y5 N.C. · Y6 LDLRØ 3F4 · Y7 N.C.
9L9 RD281
13E2 LDIOØ
10W 19-055 SG — 12, 13 — 11
08M 19-235 SOR — 05, 04 — 06
3G4 BRANCH1

9K9 RD271A
9H9 RD261A
9H9 RD241
9C9 RD161
9J9 RD251
10T 19-129 3TO8 DECODER — SEL A B C, ENB G2A G2B G1
Y0 N.C. · Y1 N.C. · Y2 N.C. · Y3 N.C. · Y4 · Y5 ULSRØ → 237-1 · Y6 ULLRØ · Y7 N.C.
9B9 RD160
10W 19-055 SG — 01, 02 — 03
10W 19-055 SG — 05, 04 — 06 ENB
10M 19-055 SG — 13, 12 — 11
09S 19-058 SG — 01, 02, 13 — 12
10W 19-055 SG — 09, 10 — 08 ENBSØ → 236-1
10M 19-055 SG — 10, 09 — 08

12T 19-196 2 TO 1 MUX — SEL, ENB 15
1A 1B 2A 2B 3A 3B 4A 4B — 1Y 2Y 3Y 4Y
N.C. N.C. N.C. N.C.
B161 7E2 · B171 7F2 · B181 7G2 · B191 7H2

12W 19-196 2 TO 1 MUX — SEL, ENB 15
3K9 LR201 · 3K9 LR211 · 3K9 LR221 · 3K9 LR231
B201 7J2 · B211 7K2 · B221 7M2 · B231 7N2

13T 19-196 2 TO 1 MUX — SEL, ENB 15
3L9 LR241 · 9H9 RD241 · 3L9 LR251 · 9J9 RD251 · 3M9 LR261 · 9H9 RD261A · 3M9 LR271 · 9K9 RD271A
B241 8E2 · B251 8F2 · B261 8G2 · B271 8H2

13W 19-196 2 TO 1 MUX — SEL, ENB 15
3N9 LR281 · 9L9 RD281 · 3N9 LR291 · 9M9 RD291 · 3N9 LR301 · 9M9 RD301 · 3N9 LR311 · 9N9 RD311
B281 8J2 · B291 8K2 · B301 8M2 · B311 8N2

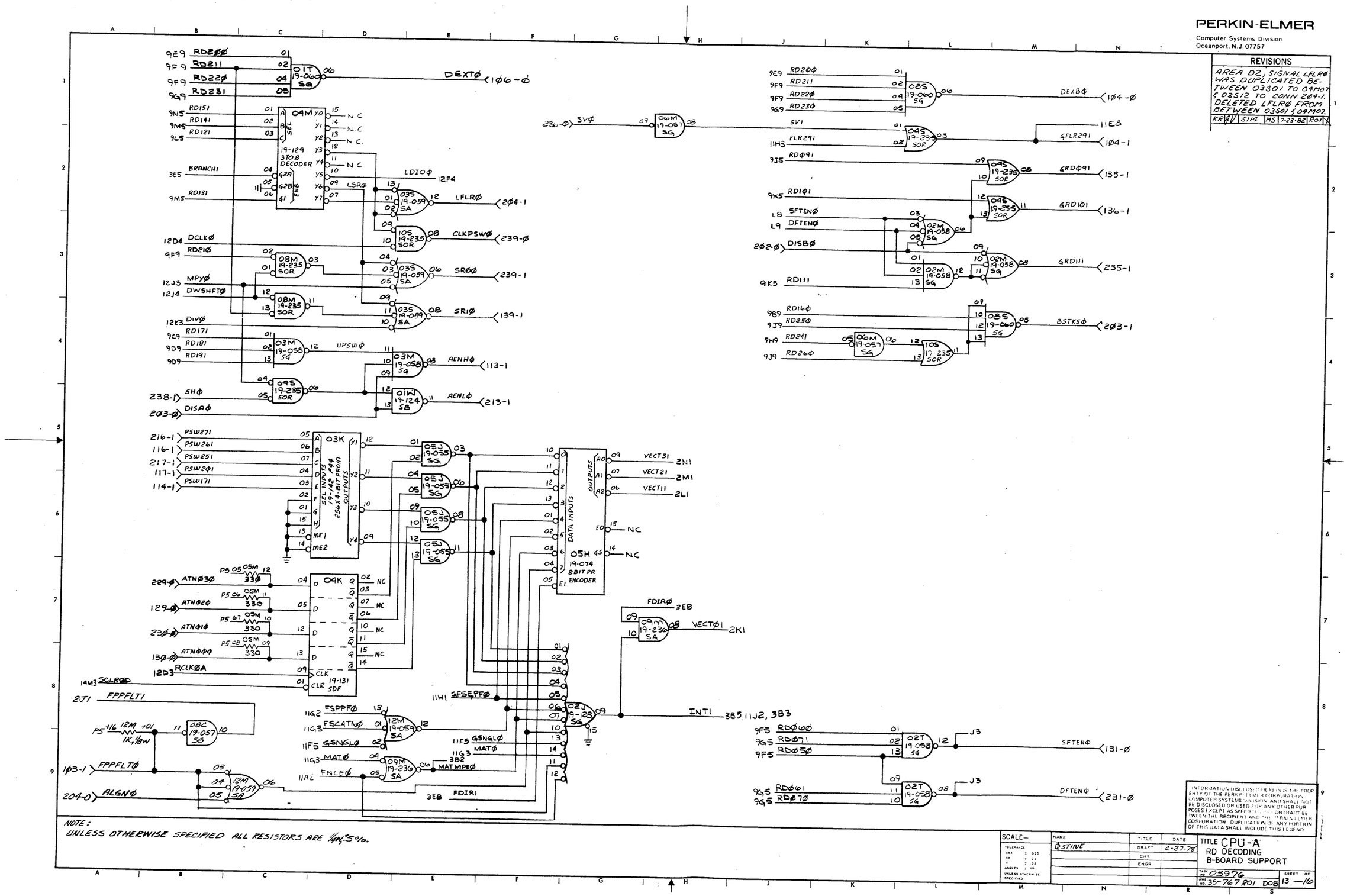
SCALE—
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

	NAME	DATE
DRAFT	R STINE	9-27-78
CHK		
ENGR		

TITLE: CPU-A E-FIELD DECODE & B-BUS DRIVERS
TASK NO. 03976
DWG NO. 35-767 D08
SHEET OF 12—16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA D2, SIGNAL LFLRØ WAS DUPLICATED BETWEEN 03501 TO 04M07 & 03512 TO CONN 204-1. DELETED LFLRØ FROM BETWEEN 03501 & 04M07.				
KRW	5114	MS	7-23-82	R01



NOTE:
UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/4W, 5%.

SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	D STINE	DRAFT	4-27-78
		CHK	
		ENGR	

TITLE CPU-A
RD DECODING
B-BOARD SUPPORT

TASK NO. 03976 SHEET OF
DWG NO. 35-767 R01 D08 13 —16

REVISIONS

NOTES
1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/4W, ±5%.
2. + INDICATES COMPONENT IN OUTSIDE POW OF BOARD I.C. PATTERN.

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
	DES / DFT	
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
CPU-A
POWER FAIL CONTROL LOGIC

TASK 03976	SHT
DWG 35-767 D08	14 - 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
AREA 09, 100-7 WAS 200-7; AREA 05, 101-7 WAS 201-7.
(2007) VJP 4490 M 9-29-80 R01

PS

S1 33-035 8-POS DIP SWITCH

S2 33-035 8-POS DIP SWITCH

00K 21-025 FQ1

1K RESISTOR NET

MAT311 (200-5)
MAT301 (201-5)
MAT291 (202-5)
MAT281 (203-5)
MAT271 (204-5)
MAT261 (205-5)
MAT251 (206-5)
MAT241 (207-5)
MAT231 (209-5)
MAT221 (210-5)
MAT211 (211-5)
MAT201 (212-5)
MATCHØ (213-5)
MSNGLØ (214-5)
MWCSØ (215-5)
MEXTØ (216-5)

00M 19-117 4-BIT MAG. COMP.
01M 19-117 4-BIT MAG. COMP.
01S 19-117 4-BIT MAG. COMP.

DATA IN
CASCADING INPUTS
A>B A=B A<B
N.C.

2N9 CSAR311
2M9 CSAR301
2M9 CSAR291
2L9 CSAR281
2J9 CSAR271
2H9 CSAR261
2H9 CSAR251
2G9 CSAR241
2E9 CSAR231
2D9 CSAR221
2D9 CSAR211
2C9 CSAR201
12A1 XRPK

1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
EXT-MEM	MWC	MSNG	MTCH	CSAR											
MATCH CONDITION				CSAR MATCH AXX.											
ON = ENABLE				ON = Ø											

005 19-082 SGO

BCLKØ 12D2
SYNØ TP1 1Ø1-7
TRAPØ 2Ø9-Ø
P5 025 10K

EXTRAPØ TP2 1Ø0-7
025 1000 pf

SCALE— TO ERASE FRACTIONS ± .005, XX ± .02, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
DESTINE	DRAFT	4-27-78
	CHK	
	ENGR	

TITLE CPU-A TEST AID

TASK NO. 03976
DWG. NO. 35-767R01 D08
SHEET OF 15—16

PERKIN-ELMER

Interdata Division

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
001	CLKIA	11	063	05A42	06	126	GFLRE91	13	187	15K05	14	249	B171A	07	311	CSAR291	15	373	GND05M		435	10B09	10	497	P516K		559	06E12	03	621	SRD281	09	683	07508	02	745			807		
002	CLKCCO	11	064	05C09	06	126	HWO	11	188	15T03	14	250	B181	07	312	CSAR300	02	374	GND06A	05	436	MAC1	11	498	P516M		560	06F10	02	622	SRD291	09	684	08B06	10	746			808		
003	CLKPSWO	13	065	05C10	06	127	09E12	04	189	15M02	11	251	B181A	07	313	CSAR301	15	375	GND06E	03	437	10C03	03	499	P516S		561	06H07	02	623	SRD301	09	685	YDC1	11	747			809		
004	DSTOPO	12	066	05E09	04	128	09E08	03	190	15M03	11	252	B191	07	314	CSAR310	02	376	GND06H	02	438	MSK1	11	500	P516T		562	06H09	02	624	SRD311	09	686	P500T		748			810		
005	RSTOPO	12	067	05E10	04	129	09E11	03	191	15M08	14	253	B191A	07	315	CSAR311	15	377	GND06J	02	439	10C12	02	501	P516W		563	06J07	02	625	07H09	02	687	RD210	09	749			811		
006	SCLK1	12	068	05E11	04	130	IR000	10	192	VREF	14	254	B201	07	316	FDIR1	3	378	GND07A	05	440	10K02	11	502	10K07	11	564	06J09	02	626	07J07	02	688	WCSEX1	10	750			812		
007	RCLK0	12	069	RD181	09	131	IR010	10	193	15S02	14	255	B201A	07	317	MAT301	15	379	GND07E	03	441	SCLRS1	14	503	P0W0	12	565	06M01	11	627	SV1	13	689	08M03	13	751			813		
008	RCLK0A	03	070	RD190	09	132	IR020	10	194	15T04	14	256	B211	07	318	MAT311	15	380	GND07H	02	442	P500S		504	PRIV1	03	566	06M06	13	628	SWA0	12	690	08M11	13	752			814		
009	RCLK1	12	071	RD191	09	133	IR030	10	195	15W11	14	257	B211A	07	319	DD201	10	381	GND07J	02	443	P501K		505	10K10	11	567	DIR0	11	629	SYN0	15	691	FPPF0	14	753			815		
010	RCLK1A	12	072	RD200	13	134	IR040	10	196	16K04	11	258	B221	07	320	DD211	02	382	GND08A	05	444	P501T		506	10M08	12	568	FBRCH1	11	630	TBRCH0	11	692	GND10T	12	754			816		
011	DCLK0	12	073	RD201	09	135	IR050	10	197	16K10	10	259	B221A	07	321	DD221	02	383	GND08E	03	445	P501W		507	10M11	12	569	07B03	10	631	TRAP0	15	693	RCTERM		755			817		
012		12	074	RD211	13	136	IR060	10	198	15S01	14	260	B231	07	322	DD231	02	384	14M03	10	446	P502M	15	508	10S03	11	570	07B06	10	632	DLLR0	12	694	GND02T		756			818		
013	BCLK0	15	075	RD220	13	137	IR070	10	199	15S14	14	261	B231A	07	323	DD241	02	385	GND09A	07	447	P503M		509	10S11	13	571	07B08	10	633	07J09	02	695	FSMINT0	14	757			819		
014	SCLK0A	03	076	RD221	09	138	JAMCI0	12	200	SCLR1	14	262	B241	08	324	DD251	02	386			448	P503S		510	10W03	12	572	07B11	10	634	07K07	11	696	08T08	14	758			820		
015	RD001	09	077	RD230	09	139	LFLR0	13	201	16S11	14	263	B241A	08	325	DD261	02	387	GND10A	07	449	P504S		511	10W11	12	573	07D10	03	635	07K09	11	697	RMVF0	14	759			821		
016	RD011	09	078	RD231	09	140	MACO	11	202	16S12	14	264	B251	08	326	DD271	02	388	GND11M	14	450	P504T		512	10T11	12	574	07E04	03	636	VECT01	02	698	12S14	14	760			822		
017	RD020	09	079	RD240	09	141	MPY0	12	203	AENH0	13	265	B251A	08	327	DD281	02	389	SCLK1A	12	451	P505C	10	513	RCATN0	11	575			637	VECT11	13	699	12S15	14	761			823		
018	RD021	09	080	RD241	12	142	10C06	10	204	AENL0	13	266	B261	08	328	DD291	02	390	WWCS0	10	452	P505E		514	MAT261	15	576	TBRCH1		638	VECT21	13	700	12S13	14	762			824		
019	RD031	09	081	RD250	09	143	MVF0	11	205	ALGN0	13	267	B261A	08	329	DD301	02	391	GND12T	12	453	P505M		515	MAT271	15	577	MAT241	15	639	VECT31	13	701	11M15	14	763			825		
020	09C08	03	082	RD251	09	144	OPSTOPO	10	206	APSW281	11	268	B271	08	330	DD311	02	392	GND12W	12	454	P505S		516	MAT281	15	578	SCATN0	11	640	VSELA0	03	702	NVRS0	14	764			826		
021	RD041	03	083	RD260	09	145	PFDT0	14	207	APSW291	11	269	B271A	08	331	08C12	10	393	GND14S	14	455	P506B		517	MAT291	15	579	MSNGL0	15	641	WAIT1	14	703	GND08A	2	765			827		
022	RD050	13	084	RD261	09	146	PSW131	03	208	APSW301	11	270	B281	08	332	08E04	03	394	ENBB0	09	456	P506C		518	MWCS0	15	580	MAT251	15	642	WCS1	10	704	FEPF0	14	766			828		
023	RD051	03	085	RD261A	12	147	PSW171	13	209	APSW311	11	271	B281A	08	333	08E07	03	395	ENBB1	09	457	P506K		519	00M06	15	581	SCLR0	14	643	WCS80A	05	705	15M11	11	767			829		
024	RD060	13	086	RD270	09	148	PSW181	11	210	ATN000	13	272	B291	08	334	GDIR1A	02	396	GND15S	14	458	P506M		520	00T02	15	582	14S06	14	644	WCS90A	05	706	08M06	12	768			830		
025	02A35	05	087	RD271	09	149	PSW201	13	211	ATN010	13	273	B291A	08	335	GDIR1	02	397	GND15W	14	459	P506S		521	00T04	15	583	SCLR0B	14	645	WCSA00	05	707	REPF0	14	769			831		
026	02A36	05	088	RD271A	02	150	PSW231	03	212	ATN020	13	274	B301	08	336	08E09	03	398	GRD091	13	460	P507B		522	00T08	15	584	PS14M	14	646	WCSA00A	07	708	SMINT0	14	770			832		
027	02A37	05	089	RD280	09	151	PSW251	13	213	ATN030	13	275	B301A	08	337	08E12	03	399	GRD101	13	461	P507C		523	00T10	15	585	SCLR0D	03	647	WCSA10	05	709	RD660A	11	771			833		
028	02A38	05	090	RD281	09	152	PSW261	13	214	B001	05	276	B311	08	338	DISC50	04	400	GRD111	13	462	P507M		524	00T12	15	586	07E07	03	648	WCSA10A	07	710			772			834		
029	02A39	05	091	RD291	09	153	PSW271	13	215	B001A	05	277	B311A	08	339	DISDRM1	04	401	GSNGL0	11	463	P507S		525	01K11	03	587	07E09	03	649	WCSA20	05	711			773			835		
030	02A40	05	092	RD301	09	154	11A01	07	216	B011	05	278	00K13	15	340	08H07	02	402	03M06	11	464	P508B		526	01M06	15	588	SNGL0	11	650	WCSA80A	07	712			774			836		
031	02A41	05	093	RD311	09	155	11A02	07	217	B011A	05	279	BRANCH0	03	341	08H09	02	403	WWCS1	10	465	P508C		527	01S06	15	589	SNGL1A	03	651	WCSA30	05	713			775			837		
032	02A42	05	094	RDCLR0	09	156	11A03	07	218	B021	05	280	BRANCH1	03	342	MAT231	15	404	HWI	11	466	P508M		528	09H08	03	590	07E12	03	652	WCSA30A	07	714			776			838		
033	02C09	05	095	SFTEN0	13	157	11A04	07	219	B021A	05	281	08C02	10	343	FWCSEX1	04	405	INTI	03	467	P508S		529			591	07F10	02		WCSA40	05	715			777			839		
034	02C10	05	096	SH0	13	158	11A05	07	220	B031	05	282	BCLK1	10	344	ENB	12	406	GDIR0	03	468	P508T		530	02M06	13	592	07H07	02	654	WCSA40A	07	716			778			840		
035	RD061	13	097	16S06	11	159	11A06	07	221	B031A	05	283	CATN1	03	345	08J07	02	407	10D08	03	469	GND14M	14	531	02M12	13	593	SRD001	05	655	WCSA50	05	717			779			841		
036	RD070	13	098	SR00	13	160	11A07	07	222	B041	05	284	CCATN0	12	346	ENCSAR1	04	408	09M03	12	470	P509B		532	MEXT0	15	594	SRD011	05	656	WCSA50A	07	718			780			842		
037	RD071	13	099	SR10	13	161	11A08	07	223	B041A	05	285	CKWCR0	10	347	EXTRAP0	15	409	MACMPE0	13	471	P509C		533	03K09	13	595	SRD021	05	657	WCSA60	05	719			781			843		
038	RD080	04	100	SETSNGL0	11	162	11C01	07	224	B051	05	286	08B08	10	348	FCATN1	11	410	09M11	14	472	P509D		534	03K10	13	596	SRD031	05	658	WCSA60A	07	720			782			844		
039	RD081	04	101	SV0	13	163	11C02	07	225	B051A	05	287	MAT201	15	349	FDIR0	03	411	TRBRCH1	11	473	P509E		535	03K11	13	597	SRD041	05	659	WCSA70	05	721			783			845		
040	RD090	09	102	ULSR0	12	164	ALGN0	13	226	B061	05	288	MAT211	15	350	GBRCH1	11	412	09S08	03	474	P509F		536	03K12	13	598	SRD051	05	660	WCSA70A	07	722			784			846		
041	RD091	13	103	UNNLD0	12	165	12K06	11	227	B061A	05	289	MAT221	15	351	FEPF1	14	413	09S12	12	475	P509H		537	04K03	13	599	SRD061	05	661	WCSA80	05	723			785			847		
042	RD100	09	104	UPSW0	13	166	12M08	11	228	B071	05	290	COMILL1	10	352	FESCAP0	03	414	09W10	12	476	P509J		538	04K06	13	600	SRD071	05	662	WCSA90	05	724			786			848		
043	RD101	13	105	YD008	11	167	12M12	13	229	B071A	05	291	COMM1	11	353	08J09	02	415	09E06	03	477	P509M		539	04K11	13	601	SRD081	04	663	WCSE00	05	725			787			849		
044	RD110	09	106	YD091	11	168	12S05	14	230	B081	06	292	CSAR200	02	354	08K07	11	416	LDCSARO	02	478	P509S		540	04K14	13	602	SRD091	04	664	WCSE00A	07	726			788			850		
045	RD111	13	107	YD101	11	169	12S06	14	231	B081A	06	293	CSAR201	15	355	08K09	11	417	LDI00	13	479	P510B		541	04M07	13	603	SRD101	04	665	WCSE10	05	727			789			851		
046	RD120	09	108	YD111	11	170	12S07	14	232	B091	06	294	CSAR210	02	356	09B08	10	418	LDLR0	12	480	P510C		542	04M12	13	604	SRD111	04	666	WCSE10A	07	728			790			852		
047	RD121	09	109	CL070	14	171	12S12	14	233	B091A	06	295	CSAR211	15	357	FLTILL1	03	419	LDLR1	03	481	P510D		543	04S06	13	605	SRD121	04	667	WCSSELO	04	729			791			853		
048	RD131	03	110	YDFEN0	14	172	13K01	11	234	B101	06	296	CSAR220	02	358	09B12	10	420	DWSHFT0	12	482	P510M		544	04T02	03	606	SRD131	04	668	WCSSELOA	05	730			792			854		
049	RD141	13	111	BSTKS0	13	173	13M09	11	235	B101A	06	297	CSAR221	15	359	FPPF1	11	421	LR201	10	483	P510S		545	04T06	09	607	SRD141	04	669	WCSWE00	05	731			793			855		
050	RD150	03	112	DEXB0	13	174	14A01	08	236	B111	06	298	CSAR230	02	360	FSCATN0	11	422	LR211	10	484	P510W		546	04T08	09	608	SRD151	04	670	WCSWE00A	07	732			794			856		
051	RD151	13	113	DEXT0	13	175	14A02	08	237	B111A	06	299	CSAR231	15	361			423	LR221	07	485	P511M		547	04T10	09	609	SRD161	09	671	WCSWE10	05	733			795			857		
052	RD160	09	114	DFTEN0	13	176	14A03	08	238	B121	06	300	CSAR240	02	362	FSPPF0	11	424	LR231	07	486	P511S		548	04T12	09	610	SRD171	09	672	WCSWE10A	07	734			796			858		
053	RD161	09	115	DISA0	13	177	14A04	08	239	B121A	06	301	CSAR241	15	363	VSELB0	02	425	LR241	07	487	P512K		549	05J03	13	611	SRD181	09	673	XRPB	03	735			797			859		
054	RD170	09	116	DISB0	13	178	14A05	08	240	B131	06	302	CSAR250	02	364	09C03	10	426	LR251	07	488	P512M		550	05J06	13	612	SRD191	09	674			736			798			860		
055	RD171	02	117	DIV0	12	179	14A06	08	241	B131A	06	303	CSAR251	15	365	GFSEPF0	13	427	LR261	07	489	P513K		551	05J08	13	613	SRD201	09	675	XRPD	09	737			799			861		
056	05A35	06	118	FPP1	11	180	14A07	08	242	B141	06	304	CSAR260	02	366	GND00M		428	LR271	07	490	P513M		552	05J11	13	614	SRD211	09	676	XRPE	10	738			800			862		
057	05A36	06	119	ENBS0	12	181	14A08	08	243	B141A	06	305	CSAR261	15	367	GND01M		429	LR281	07	491	P513S		553	06B06	10	615	SRD221	09	677		14	739			801			863		
058	05A37	06	120	FLR281	11	182	14C01	08	244	B151	06	306	CSAR270	02	368	GND01S		430	LR291	07	492	PRDY1	14	554	06B08	10	616	SRD231	09	678	FSMINT0	14	740			802			864		
059	05A38	06	121	FLR291	11	183	14C02	08	245	B151A	06	307	CSAR271	15	369	GND02J		431	LR301	05	493	P515K		555	06D10	03	617	SRD241	09	679	XRPJ	14	741			803			865		
060	05A39	06	122	FLR301	11	184	FPPFLT0	13	246	B161	07	308	CSAR280	02	370	GND02S	15	432	LR311	05	494	P515M		556	06E04	03	618	SRD251	09	680	XRPK	12	742			804			866		
061	05A40	06	123	FLR311	11	185	FPPFLT1	13	247	B161A	07	309	CSAR281	15	371	GND03K	13	433	LRCLK0	03	495	P515T		557	06E07	03	619	SRD261	09	681	07M08	11	743			805			867		
062	05A41	06	124	FMPE0	11	186	16S03	14	248	B171	07	310	CSAR290	02	372	GND04M	13	434	LSR0	13	496	P515W		558	06E09	03	620	SRD271	09	682	07S06	03	744			806			868		

NOTES,
1. CROSS REF LIST OF MNEMONICS REFLECTS THE SCHEMATIC, NOT THE MULTIWIRE LISTING.

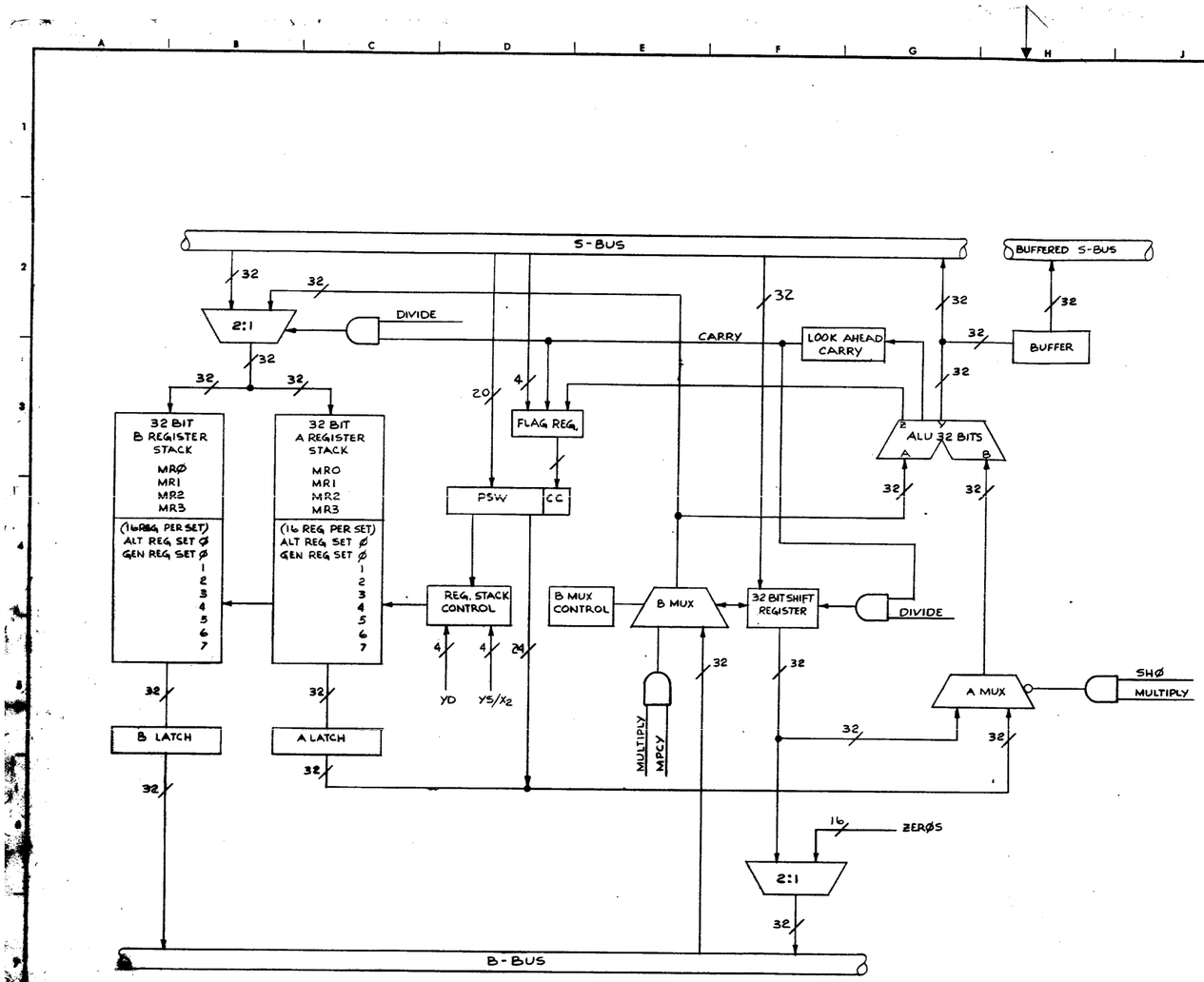
REVISIONS

NET 402 WAS 01K08. ADDED NET 709.
KR 11/1 | 5114 | MS | 7-23-82 | R01

SCALE–	NAME	TITLE	DATE
TOLERANCE .XX ± .005, .X ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	D. STINE	DRAFT	11-1-78
	R. CERO	CHK	
	G. JOYCE	ENGR	
	R. BARKER	QC	
	N. LEMONDE	MGR	

TITLE MULTIWIRE CPU-A CROSS REF.

TASK NO. | DWG NO. 35-767TR01D08 | SHEET OF 16—16



NOTE;
FOR NET #, MNEMONIC & LOCATION TO SCHEMATIC, SEE SMT 16.

REF. DESIGN.	PART NUMBER	SPARE OUTPUT
16M	19-126	08
14M	19-235	11
13H	19-057	12,
13B	19-057	06,08
12S	19-057	04,10,12
11M	19-126	06
03E	19-057	04

TABLE OF SPARES

CONN	TERM. NO.	CABLE CONNECTOR MAP ROW 2	ROW 1
5	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		
4	24	5301	5311
	23	5281	5291
	22	GND	5271
	21	5261	5251
	20	5241	
	19	5221	5231
	18	GND	5211
	17	5201	5191
	16	5181	
	15	5161	5171
	14	GND	5151
	13	5141	5131
	12	5121	
	11	5101	5111
	10	GND	5091
	09	5081	5071
	08	5061	
	07	5041	5051
	06	GND	5021
	05	5021	5011
	04	5001	
	03	GND	
	02	GND	
	01	GND	
	00	GND	GND
3	24	GND	GND
	23	5011	5001
	22	5031	5021
	21	GND	GND
	20	5051	5041
	19	5071	5061
	18	GND	GND
	17	5091	5081
	16	5111	5101
	15	GND	GND
	14	5131	5121
	13	5151	5141
	12	GND	GND
	11	5171	5161
	10	5191	5181
	09	GND	GND
	08	5211	5201
	07	5231	5221
	06	GND	GND
	05	5251	5241
	04	5271	5261
	03	GND	GND
	02	5291	5281
	01	5311	5301
	00	GND	GND
2	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		

CONN	BACK PANEL MAP ROW 1	ROW 2	TERM. NO.
1	P5	P5	41
	GND	GND	40
	SR10	SR00	39
	MPY0	SH1	38
	DIV0	ULSR0	37
	GRD101	ENBS0	36
	GRD091	GRD111	35
	RD221	RD231	34
	RD201	RD211	33
	RD190	RD191	32
	RD170	RD181	31
	RD270	RD271	30
	RD251	RD261	29
	RD240	RD121	28
	RD141	RD131	27
	RD160	RD161	26
			25
			24
		RD051	23
			22
	GND	GND	21
	YS01	YS11	20
	YS21	YS31	19
	PSW101	PSW111	18
	PSW201	PSW251	17
	PSW261	PSW271	16
	PSW131	PSW231	15
	PSW171	PSW181	14
	AENH0	AENL0	13
	PSW121	PSW211	12
	PSW191	PSW151	11
	CLFR0	PSW141	10
	GND	GND	09
	YD081	YD091	08
	YD101	YD111	07
	FLR281	FLR291	06
	FLR301	FLR311	05
	GFLR291	LFLR1	04
		BSTKS0	03
		JAMC10	02
	GND	GND	01
	P5	GND	00
0	P5	GND	41
	GND	GND	40
	CLKCC0	CLKPSW0	39
	CLK1B	SCLK1	38
	GND	GND	37
			36
		DSTOP0	35
			34
	GND	GND	33
	S160	S170	32
	S180	S190	31
	S200	S210	30
	S220	S230	29
	GND	GND	28
	B001	B011	27
	B021	B031	26
	B041	B051	25
	B061	B071	24
	B081	B091	23
	B101	B311	22
	B121	B131	21
	B141	B151	20
	B161	B171	19
	B181	B191	18
	B201	B211	17
	B221	B231	16
	B241	B251	15
	B261	B271	14
	B281	B291	13
	B301	B311	12
	GND	GND	11
	S240	S250	10
	S260	S270	09
	S280	S290	08
	S300	S310	07
	GND	GND	06
		SCLR0B	05
		EXB0	04
			03
			02
	GND	GND	01
	P5	GND	00

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

SCALE—

TOLERANCE
FRAC ± .005
.XX ± .02
.X ± .05
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
D STINE	DRAFT	
E. GREENSTIEN	SYS TEST	
R. CERO	CHK	
D. BALAS	ENGR	
R.A BARKER	QC	
B.FRANKENBERGER	MGR	

PERKIN-ELMER

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	CJ	1/4/80
PROD		

RELEASED FOR PRODUCTION
DEV
MFG. ENG. [illegible] DATE 7/3/80

AREA 5A: BOARD KEY WAS 1000. REVISED SMT5 147

JLV	5094	K	7-19-82	R01 X

USED IN MANUAL 47-011

35-768 R02
BOARD REV. LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REV. LEV.

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE CPU-B CONNECTOR MAP

TABR NO.
DWG NO. 35-768 R01 D08
SHEET OF 1 — 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

065 19-082 SG0
MPY SRL
RRL
RLL SLL
SLA SRA
067 19-132 2701 MUX
06W 19-132 2701 MUX
03C 19-066 2701 MUX
077 19-132 2701 MUX
07W 19-132 2701 MUX
03D 19-066 2701 MUX
02C 470 1K 1K 1K
05H 1K 1K 1K 1K
04B 19-068 LOOK AHEAD CAR. GEN.
02B 19-067 4-BIT ALU
02F 19-067 4-BIT ALU
04C 19-068 LOOK AHEAD CAR. GEN.
05C 330
034 19-057
038 19-057

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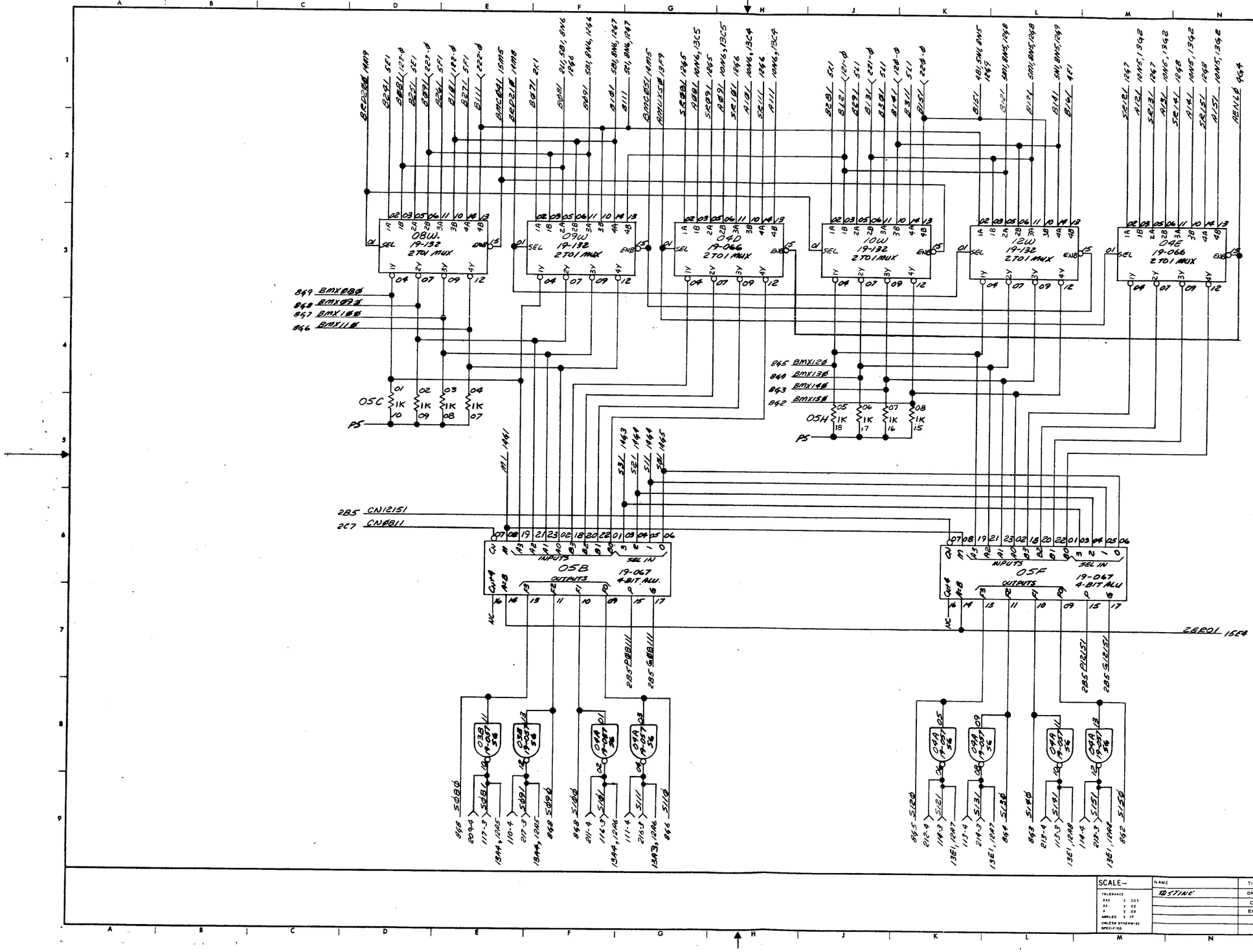
	NAME	TITLE	DATE
SCALE–	ADSTINE	DRAFT	4-13-78
TOLERANCE .XXX ± .005 .XX ± .02 .X ± .03 ANGLES ± 1/2° UNLESS OTHERWISE SPECIFIED		CHK	
		ENGR	

TITLE CPU-B BITS 0-7
TASK NO.
DWG NO 35-766 D08
SHEET OF 2 —16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



	NAME	TITLE	DATE
SCALE—	TOSTINE	DRAFT	4-13-78
TOLERANCE XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		CHK	
		ENGR	

TITLE CPU-B BITS 8-15

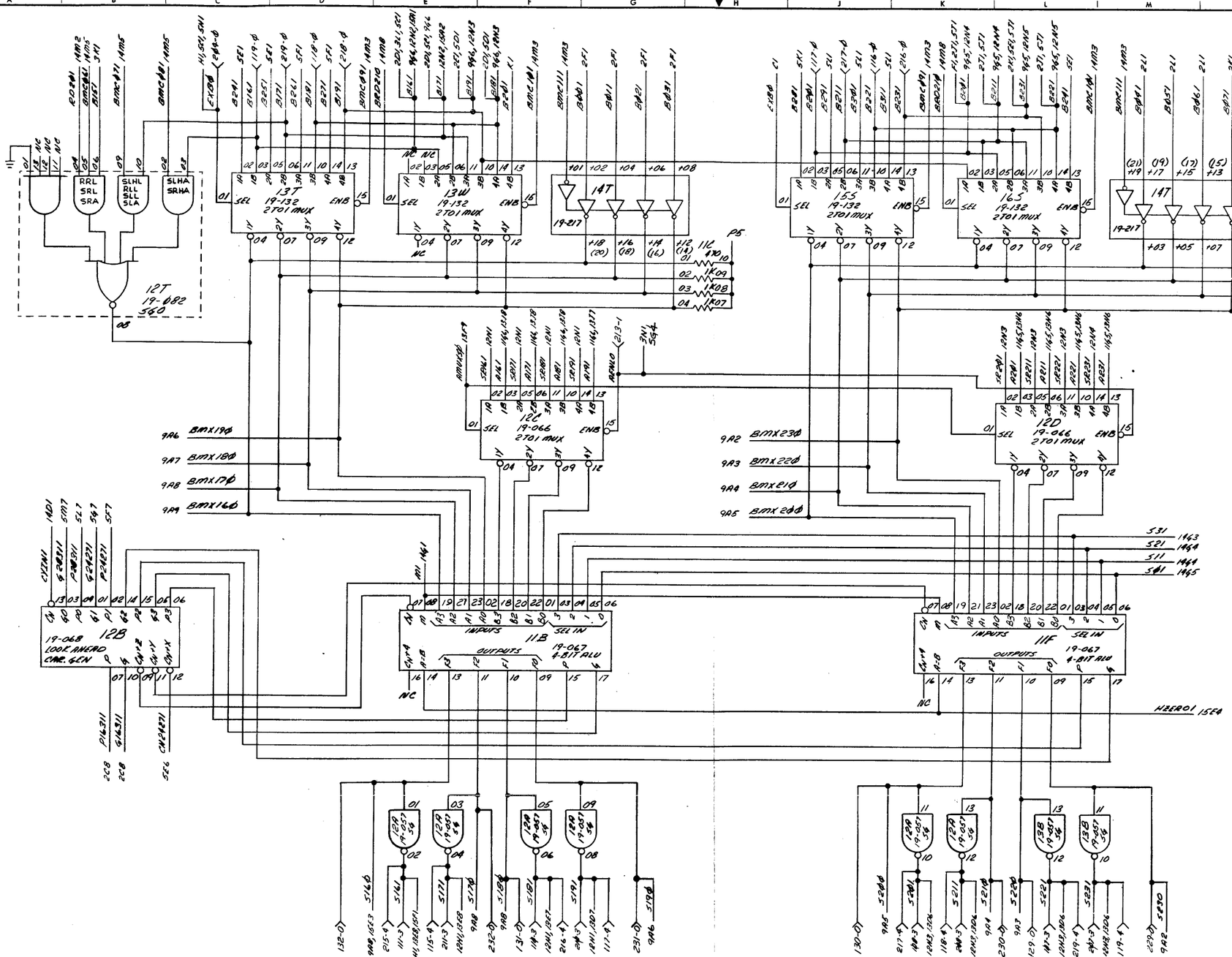
TASK NO.

DWG. NO. 35-768 D08

SHEET OF 3—16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	DSTINE	DRAFT	4-13-78
		CHK	
		ENGR	

TITLE CPU-B BITS 16-23

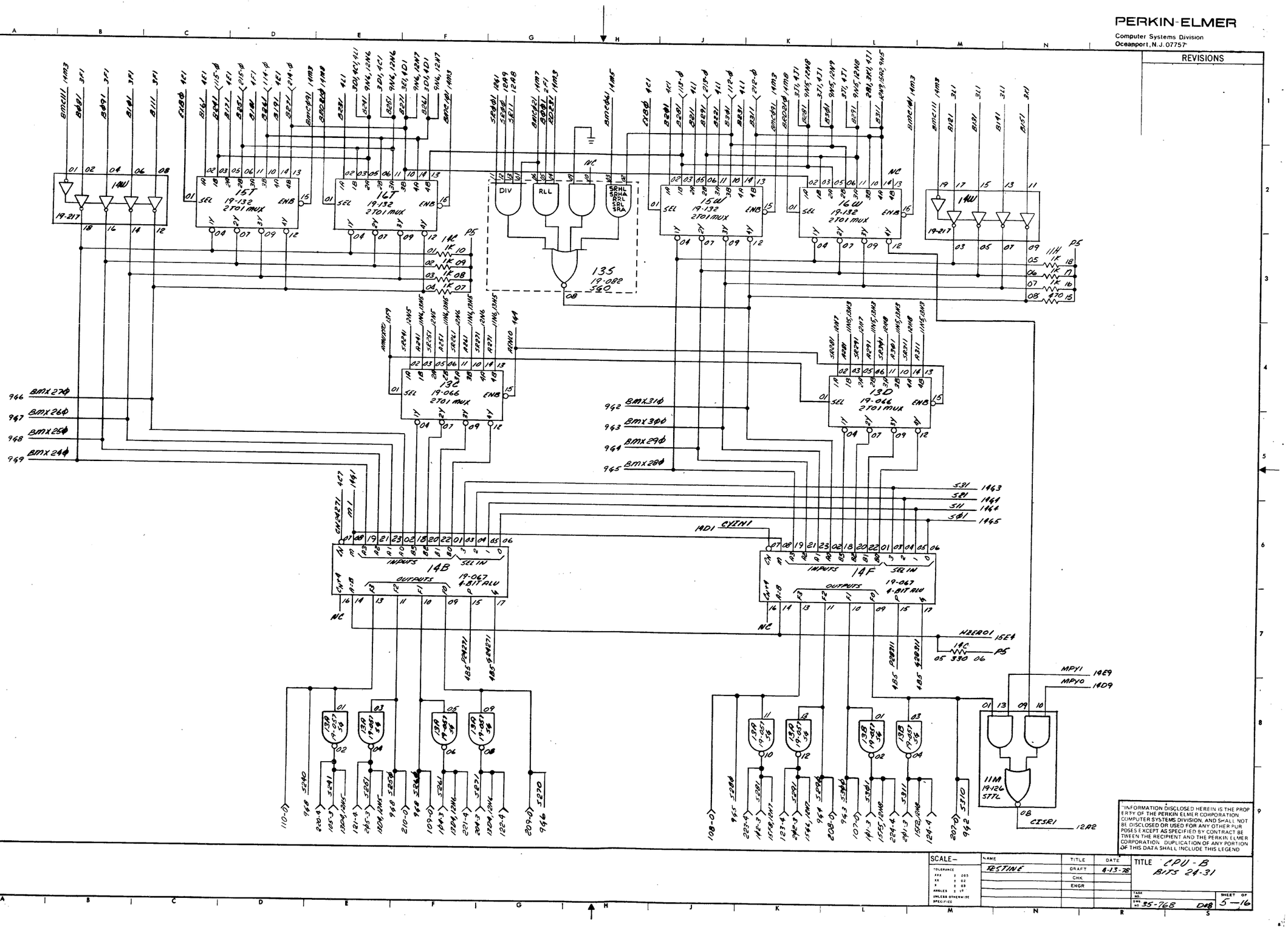
TASK NO.

DWG NO. 35-768 D08

SHEET 4 OF 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



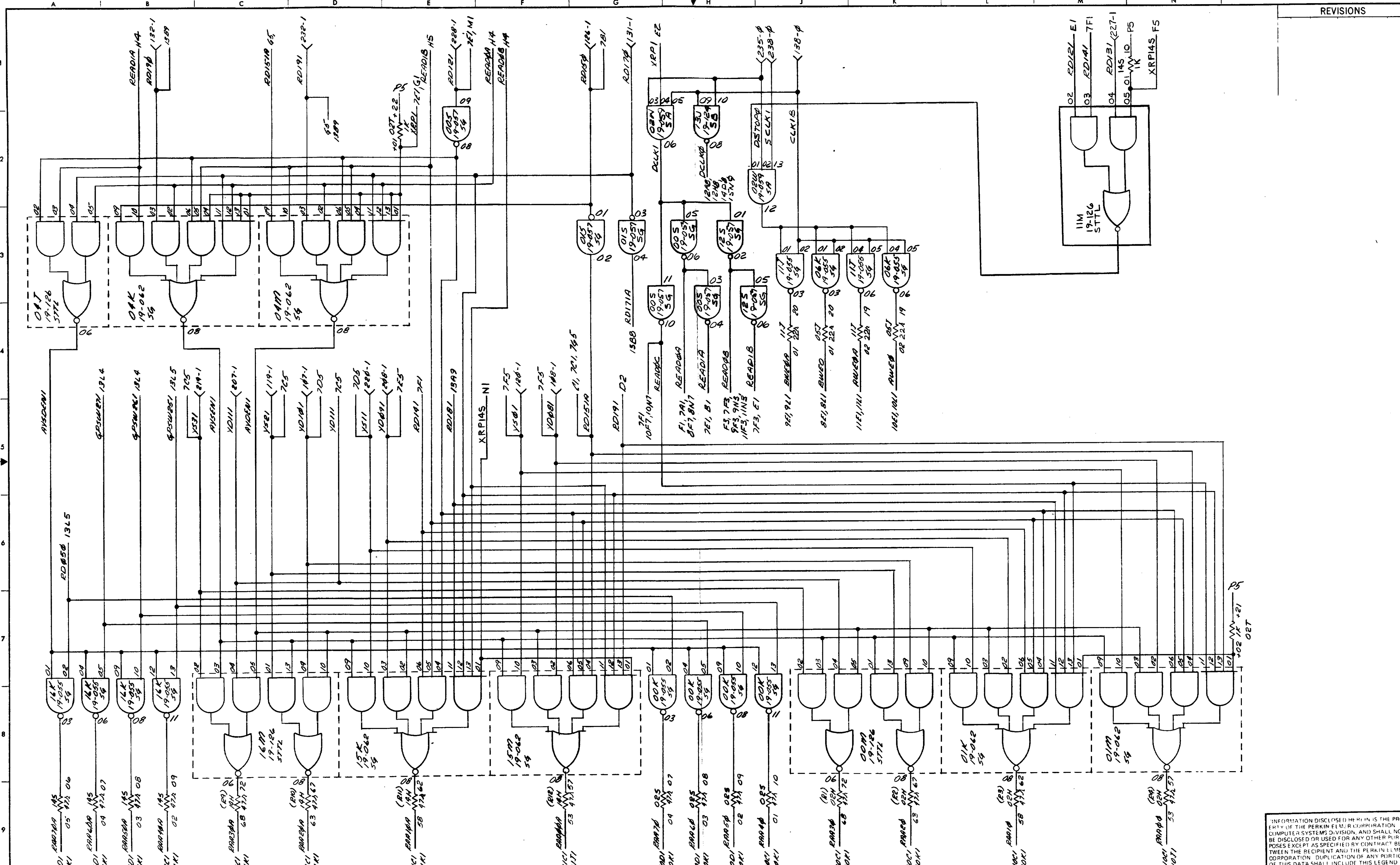
SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	RESTINE	DRAFT	4-13-76
		CHK	
		ENGR	

TITLE C.P.U - B BITS 24-31

TASK NO. 35-768 DWG NO 048 SHEET 5 OF 16

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



SCALE—	NAME	TITLE	DATE	TITLE CPU-B
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	DJ STINE	DRAFT	4-13-78	A-FIELD RD DECODE
		CHK		
		ENGR		TASK NO.
				DWG. NO. 35-768 D08 — SHEET 6 OF 16

PERKIN-ELMER

REVISIONS				
AREA L1-L5 REVISED REG TABLE INFO. SEE KOD MICROFILM FOR PREVIOUS REV LEVEL				
LV	W	5094	R	7-19-82 ROI

RA3	RA2	RA1	RA0	RB3	RB2	RB1	RB0	
1	1	1	1	1	1	1	1	MR0
1	1	1	1	1	1	1	0	MR1
1	1	1	1	1	1	0	1	MR2
1	1	1	1	1	1	0	0	MR3
1	0	0	0					ALT REG SET
0	1	1	1					REG SET 0
0	0	1	1					REG SET 1
0	1	0	1					REG SET 2
0	0	0	1					REG SET 3
0	1	1	0					REG SET 4
0	0	1	0					REG SET 5
0	1	0	0					REG SET 6
0	0	0	0					REG SET F
				1	1	1	1	GEN REG 0
				0	1	1	1	GEN REG 1
				1	0	1	1	GEN REG 2
				0	0	1	1	GEN REG 3
				1	1	0	1	GEN REG 4
				0	1	0	1	GEN REG 5
				1	0	0	1	GEN REG 6
				0	0	0	1	GEN REG 7
				1	1	1	0	GEN REG 8
				0	1	1	0	GEN REG 9
				1	0	1	0	GEN REG A
				0	0	1	0	GEN REG B
				1	1	0	0	GEN REG C
				0	1	0	0	GEN REG D
				1	0	0	0	GEN REG E
				0	0	0	0	GEN REG F

SCALE—	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	RESTINE	DRAFT	4-13-78
		CHK	
		ENGR	

TITLE CPU-B B-FIELD RD DECODE

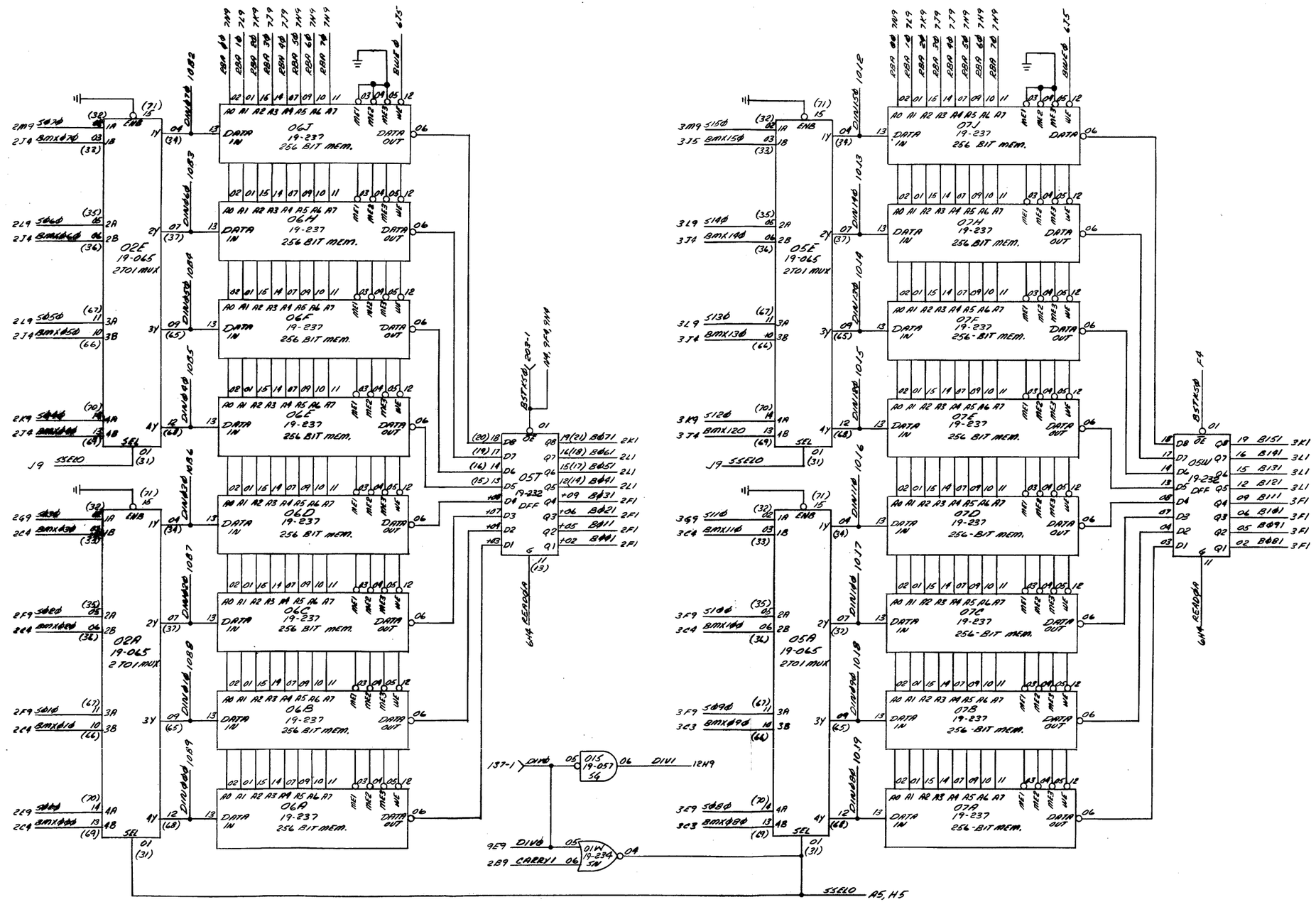
TASK NO.

DWG. NO. 35-768 ROI D08

SHEET OF 7—16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



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SCALE—	NAME	TITLE	DATE	TITLE CPU-B B-STACK 0-15"
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	RSTINE	DRAFT	4-13-78	
		CHK		
		ENGR		
				TASK NO.
				DWG NO. 35-768 D08 SHEET OF 8-16

PERKIN-ELMER

REVISIONS

09J 19-237 256 BIT MEM.
09H 19-237 256 BIT MEM.
09F 19-237 256 BIT MEM.
09E 19-237 256 BIT MEM.
09D 19-237 256 BIT MEM.
09C 19-237 256 BIT MEM.
09B 19-237 256 BIT MEM.
09A 19-237 256 BIT MEM.
11E 19-065 2T01 MUX
11A 19-065 2T01 MUX
10J 19-237 256 BIT MEM.
10H 19-237 256 BIT MEM.
10F 19-237 256-BIT MEM.
10E 19-237 256 BIT MEM.
10D 19-237 256-BIT MEM.
10C 19-237 256-BIT MEM.
10B 19-237 256-BIT MEM.
10A 19-237 256-BIT MEM.
01H 19-234 STA
19-232 DFF
SSELOA A5, H5

SCALE—

TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
DSTINE	DRAFT	4-13-78
	CHK	
	ENGR	

TITLE CPU-B
B-STACK 16-31

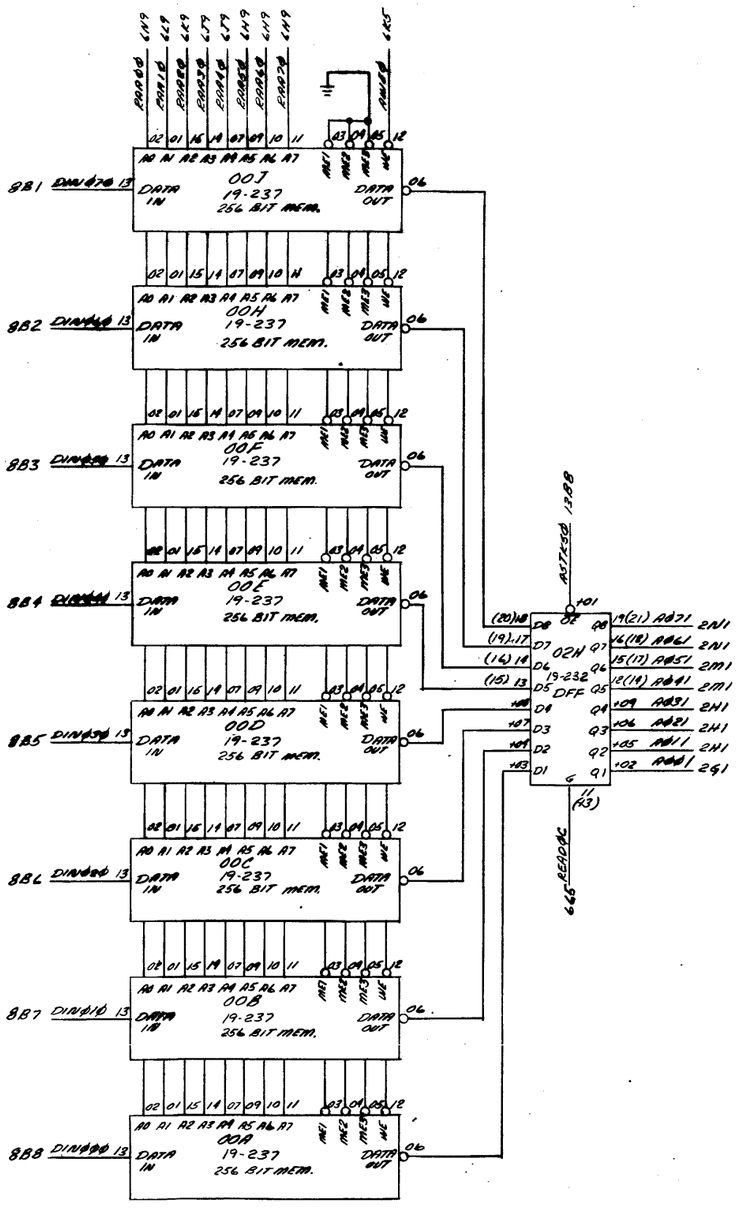
TASK NO.

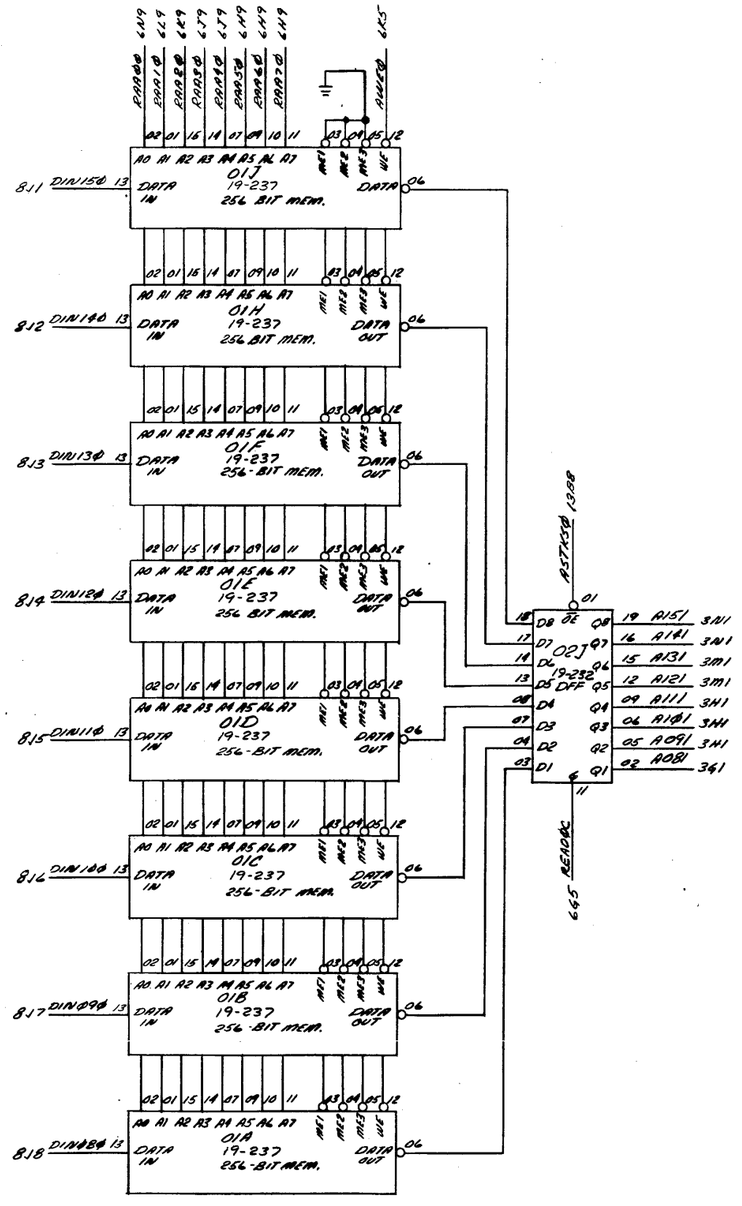
DWG. NO. 35-768 D08

SHEET 9 OF 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

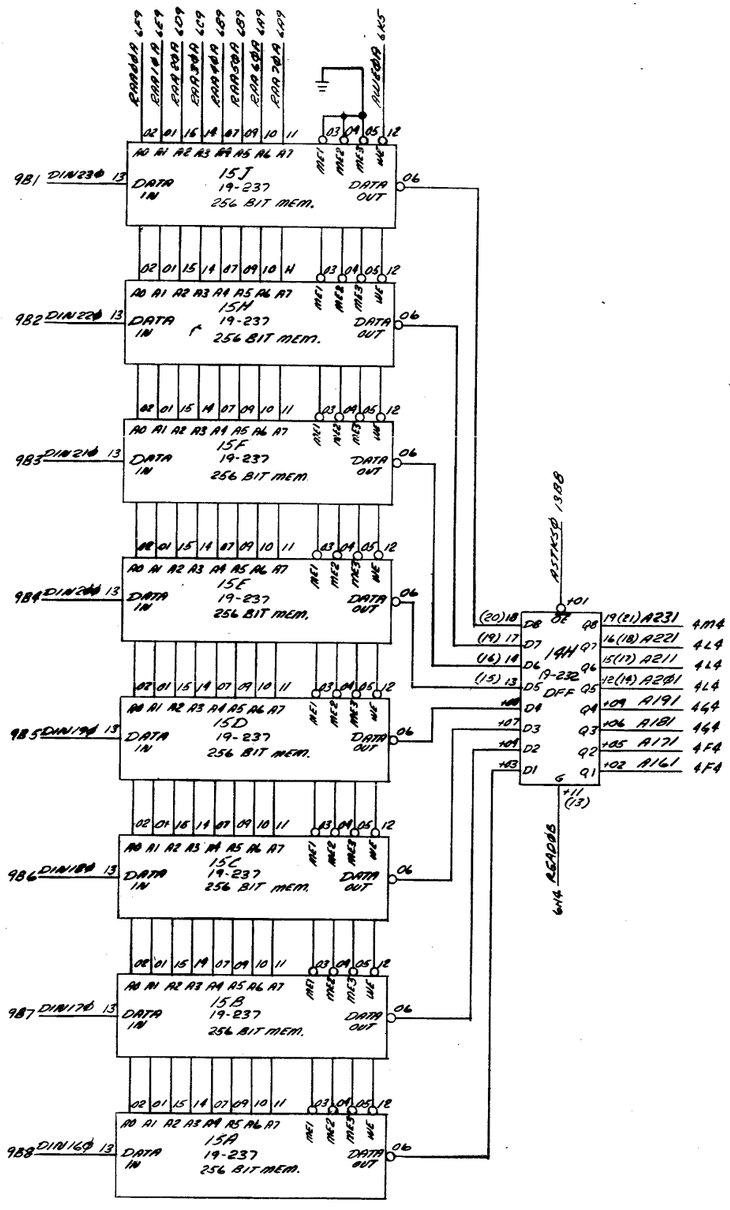


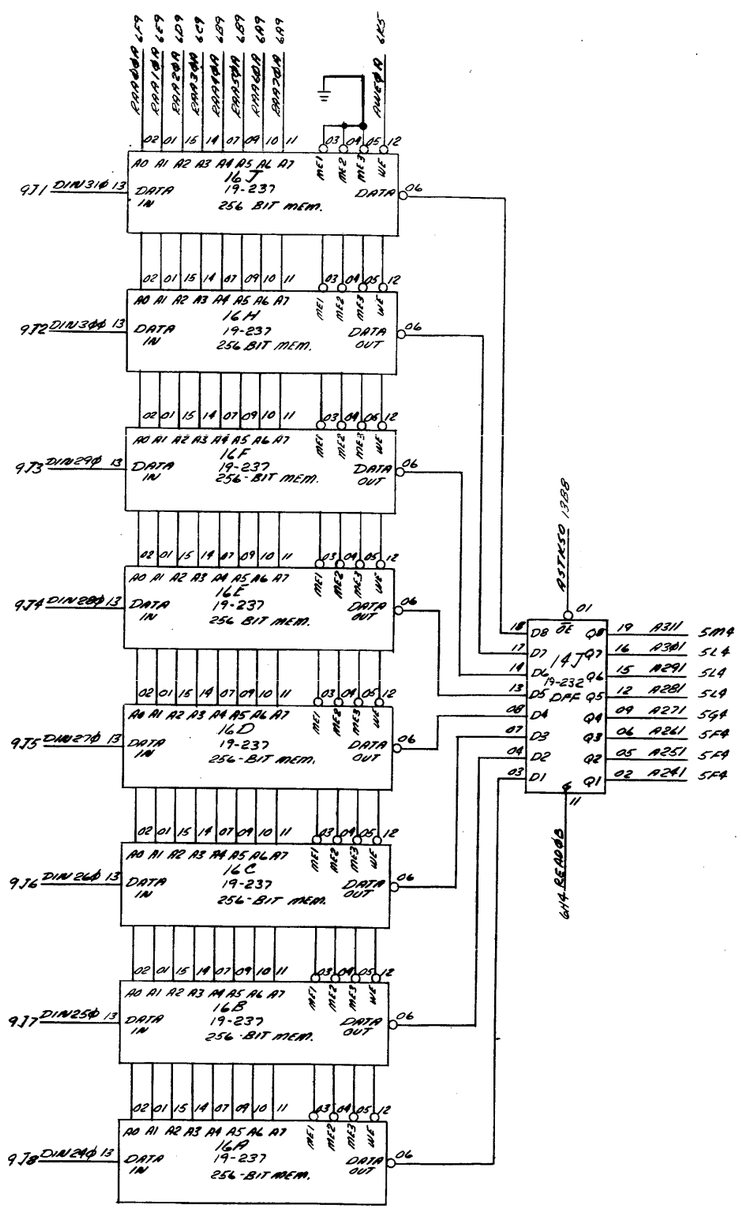


SCALE–	NAME	TITLE	DATE	TITLE CPU-B A-STACK 0-15
TOLERANCE XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	TESTINE	DRAFT	4-13-78	
		CHK		
		ENGR		
				TASK NO.
				DWG NO. 35-768 D08
				SHEET 07 10–16

PERKIN ELMER

REVISIONS





SCALE—	NAME	TITLE	DATE	TITLE: CPU-B A-STACK 16-31
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	D STING	DRAFT	4-13-78	
		CHK		
		ENGR		
				TASK NO.
				DWG NO. 35-768 D08 SHEET 11 OF 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

237-1 ULSR0
205-0 SCLR0B

OBA 19-182 4 BIT L/R SHIFT REG
2E9 S001
2F9 S011
2G9 S021
2G9 S031
6N9 CISR1
SR001 2G1, 5G1
SR011 2G1
SR021 2H1
SR031 2H1

OBB 19-182 4 BIT L/R SHIFT REG
2K9 S041
2L9 S051
2L9 S061
2M9 S071
SR041 2M1
SR051 2M1
SR061 2N1
SR071 2N1

OBC 19-182 4 BIT L/R SHIFT REG
3E9 S081
3F9 S091
3G9 S101
3G9 S111
SR081 3G1
SR091 3G1
SR101 3H1
SR111 3H1

OBD 19-182 4 BIT L/R SHIFT REG
3K9 S121
3L9 S131
3L9 S141
3M9 S151
SR121 3M1
SR131 3M1
SR141 3N1
SR151 HZ, 3N1

075 19-196 2 TO 1 MUX (STTL)
B001 2F1
B011 2F1
B021 2F1
B031 2F1

OBS 19-196 2 TO 1 MUX (STTL)
B041 2L1
B051 2L1
B061 2L1
B071 2K1

OBT 19-196 2 TO 1 MUX (STTL)
B081 3F1
B091 3F1
B101 3F1
B111 3F1

093 19-196 2 TO 1 MUX (STTL)
B121 3L1
B131 3L1
B141 3L1
B151 3K1

$CLR0B
SR101 OA
DCLK0 SR11
SR001
13H 19-057 5G 0B
13H 19-057 5G 10
SR00
ENB50

OBE 19-182 4 BIT L/R SHIFT REG
4E9 S161
4F9 S171
4F9 S181
4G9 S191
GB SR151
SR161 AB, 4F4
SR171 4F4
SR181 4F4
SR191 4G4

09T 19-229
B161 4E1
B171 4E1
B181 4F1
B191 4E1

OBF 19-182 4 BIT L/R SHIFT REG
4K9 S201
4K9 S211
4L9 S221
4M9 S231
SR201 4L4
SR211 4L4
SR221 4L4
SR231 4M4

09T 19-229
B201 4K1
B211 4L1

105 19-229
B221 4L1
B231 4L1

OBJ 19-182 4 BIT L/R SHIFT REG
5E9 S241
5F9 S251
5F9 S261
5G9 S271
SR241 5F4
SR251 5F4
SR261 5F4
SR271 5G4

105 19-229
B241 5E1
B251 5E1
B261 5F1
B271 5F1

OBJ 19-182 4 BIT L/R SHIFT REG
5K9 S281
5K9 S291
5L9 S301
5M9 S311
SR281 5L4
SR291 5L4
SR301 5L4
SR311 5M4, 14DB
6H3 DCLK0
AB SR11
A9 SR01
2B9 CARRY1
B48 DIN1
12W 19-059 5A

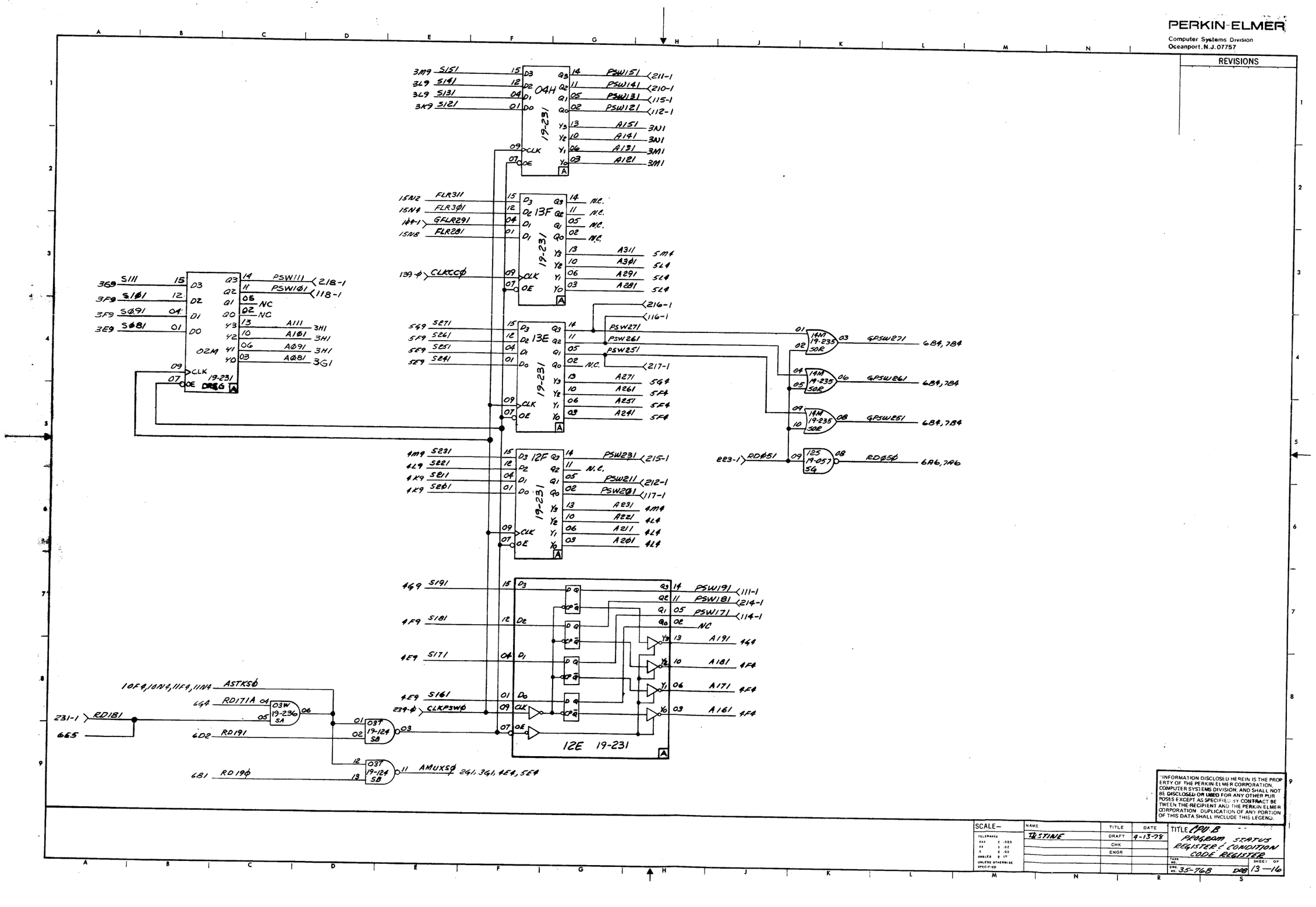
10T 19-229
B281 5K1
B291 5L1
B301 5L1
B311 5L1

SI	SO
0	0 - HOLD DATA
0	1 - SHIFT RIGHT
1	0 - SHIFT LEFT
1	1 - LOAD

	NAME	TITLE	DATE
SCALE—	D STINE	DRAFT	4-13-78
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	W. LIMPERT	CHK	
		ENGR	

TITLE CPU-B SHIFT REGISTER
TASK NO.
DWG NO. 85-768 DOB
SHEET 12 OF 16

REVISIONS



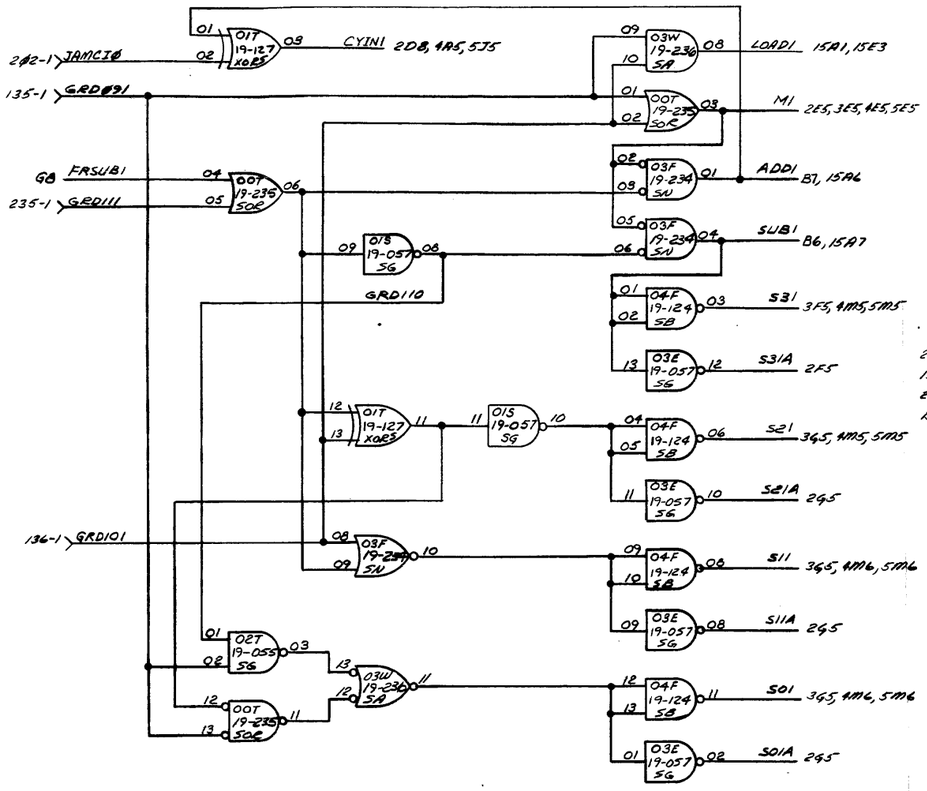
SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1Ø, UNLESS OTHERWISE SPECIFIED	R STINE	DRAFT	4-13-78
		CHK	
		ENGR	

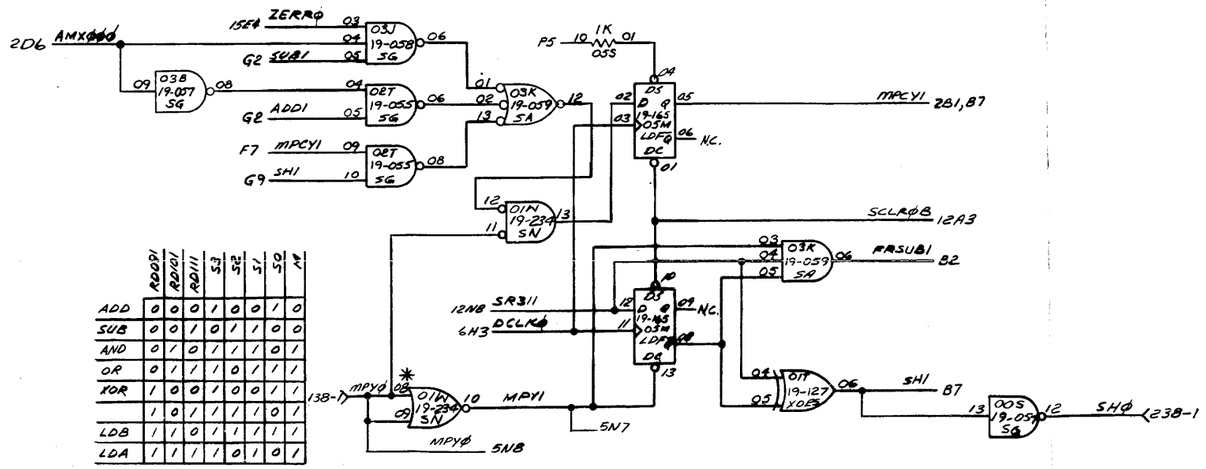
TITLE CPU:B -- PROGRAM STATUS REGISTER / CONDITION CODE REGISTER

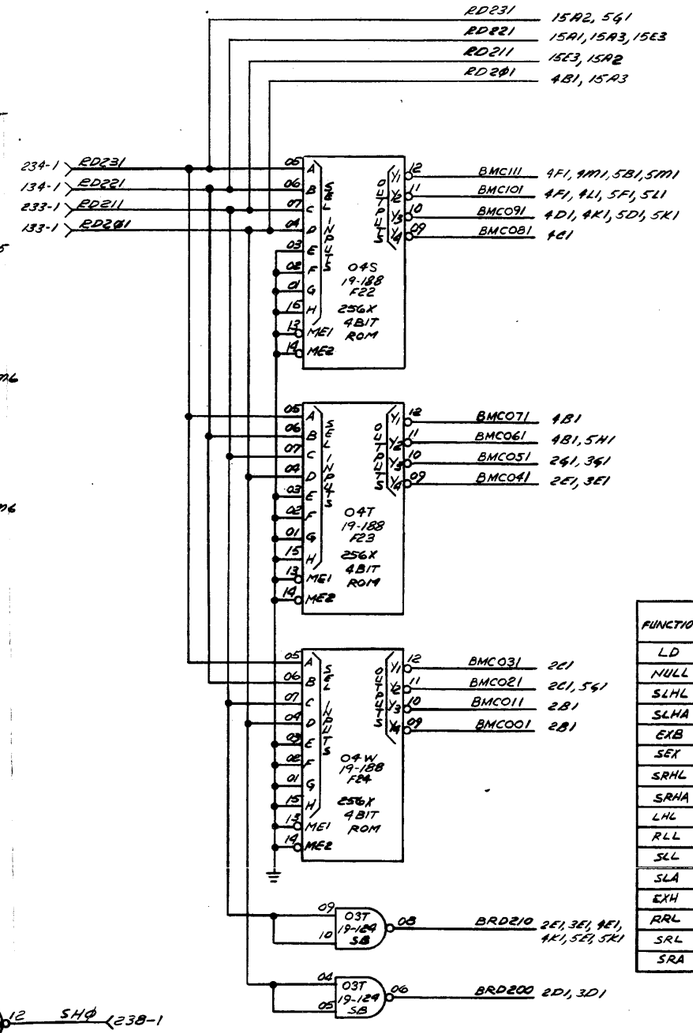
TASK NO. —
DWG NO. 35-768 DOB
SHEET OF 13—16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS







FUNCTION	RDBIT 2 2 2 2 0 1 2 3	BMC 0 0 0 0 0 1 2 3	BMC 0 0 0 0 4 5 6 7	BMC 0 0 1 1 8 9 0 1
LD	0 0 0 0	0 0 0 0	0 1 0 0	0 0 1 1
NULL	0 0 0 1	0 0 0 0	1 1 0 0	0 1 1 1
SLHL	0 0 1 0	0 0 0 0	0 1 0 1	0 1 0 1
SLHA	0 0 1 1	0 0 0 0	0 1 0 0	1 1 0 1
EXB	0 1 0 0	0 0 0 0	0 1 0 0	0 0 1 1
SEX	0 1 0 1	0 0 0 0	0 1 0 0	0 0 1 1
SRHL	0 1 1 0	0 0 0 0	0 1 1 0	0 1 0 1
SRHA	0 1 1 1	0 0 0 0	0 1 1 0	1 1 0 1
LHL	1 0 0 0	0 0 0 0	1 1 0 0	0 0 1 1
RLL	1 0 0 1	0 0 1 0	1 0 0 1	0 1 0 1
SLL	1 0 1 0	0 0 1 0	1 0 0 1	0 1 0 1
SLA	1 0 1 1	0 0 0 1	1 0 0 1	0 1 0 1
EXH	1 1 0 0	0 0 0 0	0 1 0 0	0 1 1 0
RRL	1 1 0 1	0 1 0 0	1 0 1 0	0 1 0 1
SRL	1 1 1 0	1 0 0 0	1 0 1 0	0 1 0 1
SRA	1 1 1 1	0 0 0 1	1 0 1 0	0 1 0 1

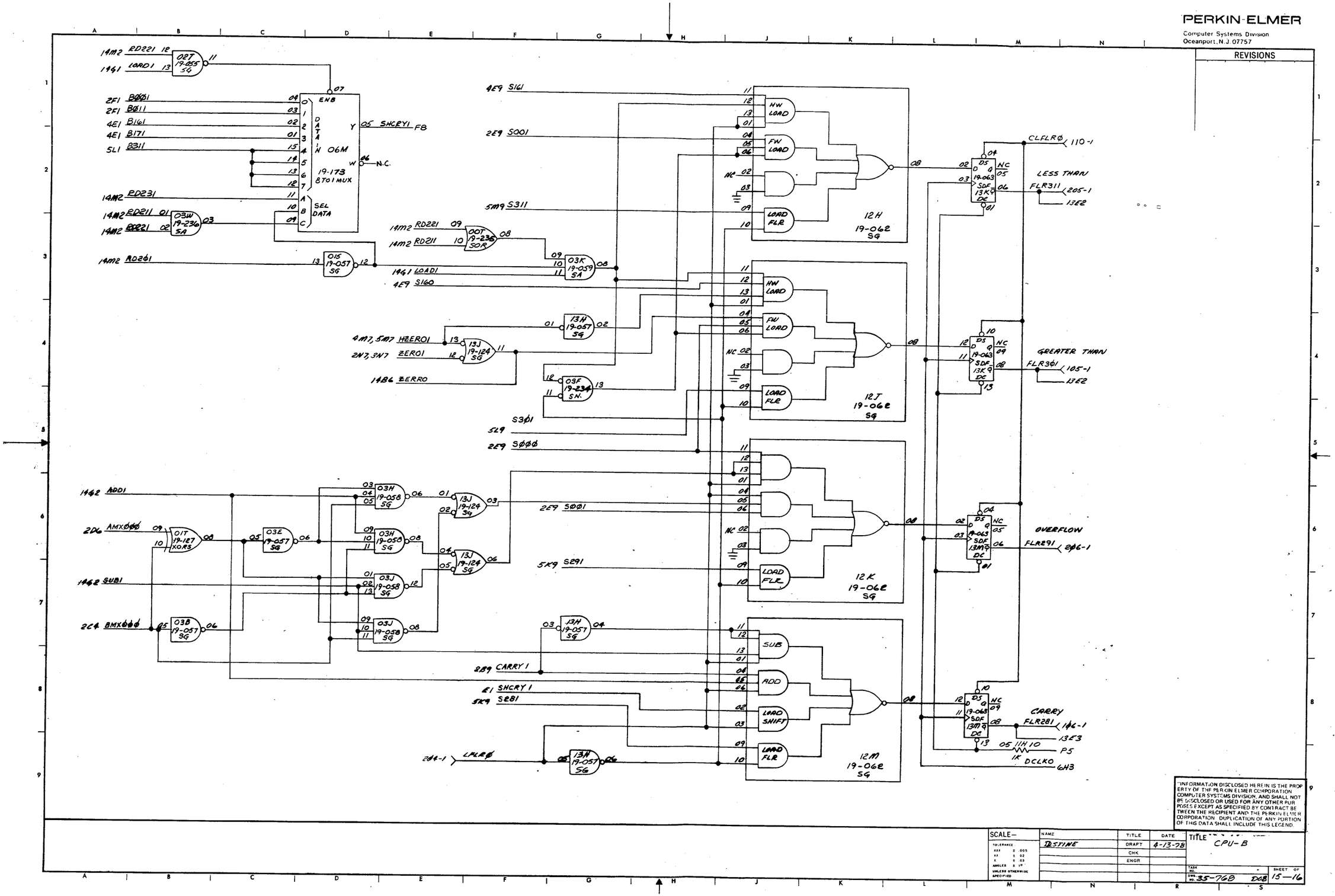
* SEE CPU-A SCHEMATICS SHEET 3B13 FOR ADDITIONAL INFORMATION.

SCALE—	NAME	TITLE	DATE	TITLE
TOLERANCE .XX ± .005, .X ± .02, X ± .09, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	TOSTINE	DRAFT	4-13-78	CPU-B
		CHK		
		ENGR		

TASK NO.
DWG NO. 35-768 2D8
SHEET OF 14—16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



SCALE—	NAME	TITLE	DATE	TITLE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	DESIGNED	DRAFT	4-13-78	CPU-B
		CHK		
		ENGR		
				TASK NO. —
				DWG. NO. 35-760 D08
				SHEET OF 15—16

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
001	CLKIB	06	063	YD081	06	125	09M08	07	187	16H06	11	249	B081	03	311	BMX240	09	373	00B06	10	435	GND09F	09	497	P502C		559	03D07	02	621	S001	02	683	S281	05	745	03T03	13	807		
002	DSTOPO	06	064	YD091	06	126	10A06	09	188	16J06	11	250	B091	03	312	BMX250	09	374	01H06	10	436	GND09H	09	498	P502T	06	560	03D09	02	622	S01	14	684	S190	05	746	03W03	15	808		
003	SCLK1	06	065	YD101	06	127	10B06	09	189	14S01	06	251	B101	03	313	BMX260	09	375	01J06	10	437	GND09J	09	499	P503A		561	03D12	02	623	S010	02	685	S191	05	747	04B10	02	809		
004	RD121	06	066	YD111	06	128	10C06	09	190	16K03	06	252	B111	03	314	BMX270	09	376	01K08	06	438	GND09S	12	500	P503B		562	03E06	15	624	S011	02	686	S300	05	748	ZERRO	14	810		
005	RD141	07	067	HZERO1	15	129	10D06	09	191	16K06	06	253	B121	03	315	BMX280	09	377	01M08	06	439	GND10A	09	501	P503E		563	03F10	14	625	S01A	02	687	S301	05	749	12C04	04	811		
006	RD150	06	068	ZERO1	02	130	10E06	09	192	16K08	06	254	B131	03	316	BMX290	09	378	01S10	14	440	GND10B	09	502	P503F		564	03F13	15	626	S020	02	688	S31	14	750	02W08	12	812		
007	RD170	06	069	READOA	06	131	10F06	09	193	16K11	06	255	B141	03	317	BMX300	09	379	01S12	15	441	GND10C	09	503	P503H		565	03H06	15	627	S021	02	689	S310	05	751	16W12	05	813		
008	RD181	06	070	READOB	06	132	10H06	09	194	16M06	06	256	B151	03	318	BMX310	09	380	FRSUB1	14	442	GND10D	09	504	P503J		566	RAA00	10	628	S030	08	690	S311	05	752	CISR1	05	814		
009	RD190	06	071	READOC	06	133	10J06	09	195	16M08	06	257	B161	04	319	BRD200	14	381	G08111	02	443	GND10E	09	505	P503K		567	ARR00A	11	629	S031	02	691	S31A	02	753	RD050	13	815		
010	RD191	06	072	READIA	06	134	10K08	07	196	A001	10	258	B171	04	320	BRD210	14	382	G18151	02	444	GND10F	09	506	P503M		568	RAA10	10	630	S040	02	692	00C06	10	754	PSW251	13	816		
011	RD201	04	073	READIB	06	135	10M08	07	197	A011	10	259	B181	04	321	01A06	10	383	G16311	02	445	GND10H	09	507	P503S		569	RAA10A	11	631	S041	02	693	SCLROB	12	755	PSW261	13	817		
012	RD211	14	074	DCLKO	12	136	11J03	06	198	A021	10	260	B191	04	322	01B06	10	384	G24271	04	446	GND10J	09	508	P503T		570	RAA20	10	632	S050	02	694	03H08	15	756	PSW271	13	818		
013	RD221	14	075	04D12	03	137	11J06	06	199	A031	10	261	B201	04	323	BWE0	08	385	G28311	04	447	GND11A	09	509	P503W		571	RAA20A	11	633	S051	02	695	SH1	14	757	RD051	13	819		
014	RD231	14	076	04E04	03	138			200	A041	10	262	B211	04	324	BWEØA	09	386	01T08	15	448	GND11E	09	510	P504A		572	RAA30	10	634	S060	02	696	SHCRY1	15	758			820		
015	RD240	07	077	04E07	03	139			201	A051	10	263	B221	04	325	BYDEN1	07	387	GND00A	10	449	GND12H	14	511	P504F		573	RAA30A	11	635	S061	02	697	03H12	06	759			821		
016	RD261	07	078	04E09	03	140	12B05	04	202	A061	10	264	B231	04	326	BYSDEN1	07	388	GND00B	10	450	GND12J	14	512	P504J		574	RAA40	10	636	S070	02	698	SR001	02	760			822		
017	RD270	07	079	04E12	03	141	12B06	04	203	A071	10	265	B241	05	327	BYSEN1	07	389	GND00C	10	451	GND12K	14	513	P504K		575	RAA40A	11	637	S071	02	699	SR01	12	761			823		
018	RD271	07	080	05M08	14	142	12B09	04	204	A081	10	266	B251	05	328	CARRY	08	390	GND00D	10	452	GND12T	05	514	P504M		576	RAA50	10	638	S080	03	700	SR011	02	762			824		
019	AENH0	02	081	05S01	14	143	12B11	04	205	A091	10	267	B261	05	329	01C06	10	391	GND00C	10	453	GND13S	05	515	P505C	03	577	RAA50A	11	639	S081	03	701	SR021	02	763			825		
020	AENL0	03	082	06A06	08	144	12B14	04	206	A101	10	268	B271	05	330	00A06	10	392	GND00F	10	454	GND14A	09	516	P505H	03	578	RAA60	10	640	S090	03	702	SR031	02	764			826		
021	RD131	06	083	06B06	08	145	12B15	04	207	A111	10	269	B281	05	331	01D06	10	393	GND00H	10	455	GND14E	09	517	P505M		579	RAA60A	11	641	S091	03	703	SR041	02	765			827		
022	BSTKS0	08	084	06C06	08	146	12C07	04	208	A121	10	270	B291	05	332	01E06	10	394	GND00J	10	456	GND15A	11	518	P505S	07	580	RAA70	10	642	S100	03	704	SR051	02	766			828		
023	CLFLR0	15	085	06D06	08	147	12C09	04	209	A131	10	271	B301	05	333	CN0811	02	395	GND01A	10	457	GND15B	11	519	P506K		581	RAA70A	11	643	S101	03	705	SR061	02	767			829		
024	CLKCC0	13	086	06E06	08	148	12C12	04	210	A141	10	272	B311	05	334	CN12151	02	396	GND01B	10	458	GND15C	11	520	P5065		582	RBA00	08	644	S11	14	706	SR071	02	768			830		
025	CLKPSW0	13	087	06F06	08	149	12D04	04	211	A151	10	273	BCS0	08	335	CN2471	04	397	GND01C	10	459	GND15D	11	521	P507K		583	RBA00A	09	645	S110	03	707	SR081	03	769			831		
026	DIV0	08	088	06H06	08	150	12D07	04	212	A161	04	274	BCS0A	09	336	CYIN1	05	398	GND01D	10	460	GND15E	11	522	P507M		584	RBA10	08	646	S111	03	708	SR091	03	770			832		
027	ENBS0	12	089	06J06	08	151	12D09	04	213	A171	04	275	BMC001	14	337	04D09	03	399	GND01E	10	461	GND15F	11	523	P508K		585	RBA10A	09	647	S11A	02	709	03J06	14	771			833		
028	EXB0	04	090	06K03	06	152	12D12	04	214	A181	04	276	BMC011	14	338	DCLK1	06	400	GND01F	10	462	GND15H	11	524	P508M		586	RBA20	08	648	S120	03	710	SR101	03	772			834		
029	FLR281	18	091	06K06	06	153	12H08	15	215	A191	04	277	BMC021	14	339	DIN000	10	401	GND01H	10	463	GND15J	11	525	P509K		587	RBA20A	09	649	S121	03	711	SR11	12	773			835		
030	FLR291	15	092	PSW101	13	154	12J08	15	216	A201	04	278	BMC031	14	340	DIN010	10	402	GND01J	10	464	GND16A	11	526	P509M		588	RBA30	08	650	S130	03	712	SR111	03	774			836		
031	FLR301	15	093	PSW11	13	155	12K08	15	217	A211	04	279	BMC041	14	341	DIN020	10	403	GND02A	08	465	GND16B	11	527	P510K		589	RBA30A	09	651	S131	03	713	SR121	03	775			837		
032	FLR311	15	094	07A06	08	156	12M08	15	218	A221	04	280	BMC051	14	342	DIN030	08	404	GND02B	08	466	GND16C	11	528	P510M		590	RBA40	08	652	S140	03	714	SR131	03	776			838		
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036	GRD110	14	098	07E06	08	160	13C12	05	222	A261	05	284	BMC091	14	346	DIN070	08	408	GND04W	14	470	GND16H	11	532	P511S	07	594	RBA60	08	656	S160	15	718	SR171	12	780			842		
037	GRD111	14	099	07F06	08	161	13D04	05	223	A271	05	285	BMC101	14	347	DIN080	10	409	GND05A	08	471	GND16J	11	533	P512A		595	RBA60A	09	657	S161	04	719	SR181	12	781			843		
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040	MPY0	14	102	07K08	07	164	13D12	05	226	A301	05	288	BMX010	08	350	DIN110	10	412	GND06B	08	474	02T03	14	536	P512K		598	00D06	10	660	S180	04	722	SR211	12	784			846		
041	PSW121	13	103	07M08	07	165	13H02	15	227	A311	05	289	BMX020	02	351	DIN120	10	413	GND06C	08	475	02T06	14	537	P512M		599	00E06	10	661	S181	04	723	SR221	12	785			847		
042	PSW131	13	104	08K02	07	166	13H04	15	228	ACS0	10	290	BMX030	08	352	DIN130	10	414	GND06D	08	476	04B09	02	538	P512S		600	00F06	10	662	S190	04	724	SR231	12	786			848		
043	PSW141	13	105	08K03	07	167	13H06	15	229	ACS0A	11	291	BMX040	08	353	DIN140	10	415	GND06E	08	477			539	P512T		601	RD151A	06	663	S191	04	725	SR241	12	787			849		
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045	PSW171	13	107	08K08	07	169	13J06	15	231	00T08	15	293	BMX060	02	355	DIN160	09	417	GND06H	08	479	02T11	15	541	P513B		603	RD171A	06	665	S201	04	727	SR261	12	789			851		
046	PSW181	13	108	08K11	07	170	13M13	15	232	00T11	14	294	BMX070	08	356	DIN170	09	418	GND06J	08	480	LOAD1	15	542	P513H		604	00J06	10	666	S21	14	728	SR271	12	790			852		
047	PSW191	13	109	08M06	07	171	15A06	11	233	AMUXS0	13	295	BMX080	08	357	DIN180	09	419	GND07A	08	481	M1	14	543	P513J		605	00K02	06	667	S210	04	729	SR281	12	791			853		
048	PSW201	13	110	08M08	07	172	15B06	11	234	AMX000	15	296	BMX090	08	358	DIN190	09	420	GND07B	08	482	MPCY1	14	544	P513K		606	00K03	06	668	S211	04	730	SR291	12	792			854		
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058	ULSR0	12	120	09K03	07	182	16B06	11	244	B031	08	306	BMX190	09	368	DIN290	09	430	GND09A	09	492	P500T		554	03B08	14	616	04B14	02	678	S260	05	740	04B05	02	802			864		
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060	YS11	06	122	09K08	07	184	16D06	11	246	B051	08	308	BMX210	09	370	DIN310	09	432	GND09C	09	494	P501M		556	03C09	02	618	04D04	03	680	S270	05	742	04B07	02	804			866		
061	YS21	06	123	09K11	07	185	16E06	11	247	B061	02	309	BMX220	04	371	01F06	10	433	GND09D	09	495	P501T		557	03C12	02	619	04D07	03	681	S271	05	743	03K08	15	805			867		
062	YS31	06	124	09M06	07	186	16F06	11	248	B071	02	310	BMX230	09	372	DIV1	08	434	GND09E	09	496	P501W		558	03D04	02	620	S000	08	682	S280	05	744	03K12	02	806			868		

NOTES
1 CROSS REF LIST OF MNEMONICS REFLECTS THE SCHEMATIC
NOT THE MULTIWIRE LISTING

REVISIONS

SCALE—

TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
D STINE	DRAFT	10-30-78
R CERO	CHK	
G JOYCE	ENGR	
P A BARKER		
N. LEMONDE		

TITLE MULTIWIRE CPU-B CROSS REF.

TASK NO.
DWG NO. 35-768 DOB
SHEET OF 16—16

CONN	TERM. NO.	CABLE CONNECTOR MAP ROW 2	ROW 1
6	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		
5	24	GND	GND
	23		
	22		
	21		
	20		
	19		
	18		
	17		CWRØ
	16	MDHSAI	ENMAAØ
	15	CAMAØ	PA3Ø1
	14	MDRSØ	DISEXTØ
	13	LHWRTØ	LWRTØ
	12	PSBCØ	MSBCØ
	11	PMEMI	MFAULTØ
	10	MDLCKØ	MDHCKØ
	09	MDSBØ	MDLSAI
	08		HALTØ
	07	GND	GND
	06	FSCLKI	FSCLKØ
	05	GND	GND
	04	LPSTDØ	LSSTDØ
	03	CLSTAØ	MATSTOPØ
	02	RFAULTØ	MARSTPØ
	01	ILOCØ	IMARØ
	00	GND	GND
4	24	GND	GND
	23	S011	S001
	22	S031	S021
	21	GND	GND
	20	S051	S041
	19	S071	S061
	18	GND	GND
	17	S091	S081
	16	S111	S101
	15	GND	GND
	14	S131	S121
	13	S151	S141
	12	GND	GND
	11	S171	S161
	10	S191	S181
	09	GND	GND
	08	S211	S201
	07	S231	S221
	06	GND	GND
	05	S251	S241
	04	S271	S261
	03	GND	GND
	02	S291	S281
	01	S311	S301
	00	GND	GND
3	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		

16A12	16A44	13
16A10	16A12	13
16A09	16A10	13
16A08	16A09	13
16A05	16A08	13
16A03	16A05	13
16A02	16A03	13
16A01	16A02	13
FROM	TO	SHT

STRAPPING INFORMATION

PART NO.	REF DESIGNATION	SPARE OUTPUT NO.
19-055	01B	11
19-055	19B	03,06
19-236	20J	11
19-236	15R	06
19-236	10K	11
19-236	05H	11
19-235	00A	08,11
19-234	19F	01
19-127	19H	08,11
19-126	14C	08
19-126	09E	08
19-124	23K	08,11
19-124	12H	11
19-064	10C	07
19-063	04D	08
19-060	11C	08
19-059	03B	06,08
19-059	01C	08
19-059	00R	08
19-058	20H	08
19-058	10R	08,12
19-058	06B	06
19-058	04C	12
19-057	22D	02,10,12
19-057	18A	02,04,06
19-057	11R	12
19-057	04H	02,04,06,08
19-057	02H	02
19-057	02B	02,04,08
19-057	01D	04,06
19-124	22K	06
19-055	18B	11
19-055	16H	08
19-055	13R	11
19-055	11H	11
19-055	06C	03,06,08
19-055	01R	03,06,08
19-055	00B	03,11

CONN	TERM. NO.	BACK PANEL MAP ROW 1	ROW 2
2	43	GND	GND
	42		
	41		
	40		
	39		
	38		
	37		
	36		
	35		
	34	GND	GND
	33	GND	GND
	32		
	31		
	30		
	29		
	28		
	27		
	26		
	25		
	24	GND	GND
	23	GND	GND
	22		MATRSDØ
	21		MATRSRØ
	20	GND	GND
	19	GND	GND
	18	MDS300Ø	MDS310Ø
	17	MDS280Ø	MDS290Ø
	16	MDS260Ø	MDS270Ø
	15	MDS240Ø	MDS250Ø
	14	MDS220Ø	MDS230Ø
	13	MDS200Ø	MDS210Ø
	12	MDS180Ø	MDS190Ø
	11	MDS160Ø	MDS170Ø
	10	GND	GND
	09	GND	GND
	08	MDS140Ø	MDS150Ø
	07	MDS120Ø	MDS130Ø
	06	MDS100Ø	MDS110Ø
	05	MDS080Ø	MDS090Ø
	04	MDS060Ø	MDS070Ø
	03	MDS040Ø	MDS050Ø
	02	MDS020Ø	MDS030Ø
	01	MDS000Ø	MDS010Ø
	00	GND	GND

BACK PANEL MAP ROW 1	ROW 2	TERM. NO.	CONN.
GND	GND	43	1
		42	
		41	
		40	
		39	
		38	
		37	
		36	
		35	
GND	GND	34	
GND	GND	33	
		32	
		31	
		30	
	RD271	29	
RD251	RD261	28	
RD240Ø	RD121	27	
RD141	RD131	26	
RD150Ø	RD161	25	
GND	GND	24	
GND	GND	23	
RD0001	RD011	22	
RD0021	RD031	21	
GND	GND	20	
GND	GND	19	
	RD020Ø	18	
		17	
	PSW211	16	
PSW101	PSW111	15	
		14	
	MSTOPØ	13	
	DSTOPØ	12	
		11	
GND	GND	10	
GND	GND	09	
		08	
SCLRØ		07	
		06	
	MCLKI	05	
		04	
	DEXTØ	03	
EXBØ	DEXBØ	02	
ALGNØ	MATØ	01	
GND	GND	00	
GND	GND	43	2
B001	B011	42	
B021	B031	41	
B041	B051	40	
B061	B071	39	
B081	B091	38	
B101	B111	37	
B121	B131	36	
B141	B151	35	
GND	GND	34	
GND	GND	33	
B161	B171	32	
B181	B191	31	
B201	B211	30	
B221	B231	29	
B241	B251	28	
B261	B271	27	
B281	B291	26	
B301	B311	25	
GND	GND	24	
GND	GND	23	
		22	
CLKIC	SCLKI	21	
GND	GND	20	
GND	GND	19	
	FNCEØ	18	
DUAØ	PSELI	17	
		16	
		15	
LMA300	LMA310	14	
LMA280	LMA290	13	
LMA260	LMA270	12	
LMA240	LMA250	11	
GND	GND	10	
GND	GND	09	
LMA220	LMA230	08	
LMA200	LMA210	07	
LMA180	LMA190	06	
LMA160	LMA170	05	
LMA140	LMA150	04	
LMA120	LMA130	03	
LMA100	LMA110	02	
LMA080	LMA090	01	
GND	GND	00	

REVISIONS				
PRE PRODUCTION APPROVAL	DEV Gpl	INIT	DATE 4/16/80	
SPARE OUTPUT PIN 01 ON 14H WAS REMOVED. REVISED AREA N9 & R9 REVISED REV. BLOCK IN AREA A9. REVISED SHTS. 1,5,8,9,11,15,19,& 25.				
E.C.J.	4494	M	10-23-80	R01
RELEASED FOR PRODUCTION ENG. GPL DATE 11/17/80				
REVISED SHTS 1,5,8,9,10				
JAT	4623	D	2-27-81	R02
DELETED: "19-234 14H 10,13" FROM SPARE GATE TABLE. AREA M9: BOARD REV LEVEL WAS R01. REVISED "STRAPPING INFORMATION" TO ADD 16AD9. REVISED SHT 1, 5 & 13				
JLV	4907	MS	12-28-81	R03 X

REVISION	3			3		2	2	1	1	1	1			1							1
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

USED IN MANUAL;

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

35-769 BOARD R05 REV LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

UNLESS OTHERWISE SPECIFIED

SCALE:

TOLERANCE:

DIMENSIONS ARE IN INCHES

.XXX ±.005 .X ±.03
.XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
E. JOHNSON	DES/DFT	11-19-80
R. CERO	SUPV	11-19-80
	CHK	11-19-80
E. MARCH	ENG	11-19-80
D. FRANKENBERGER	MGR	11-19-80
R. BARKER	QC	11-19-80

PERKIN-ELMER

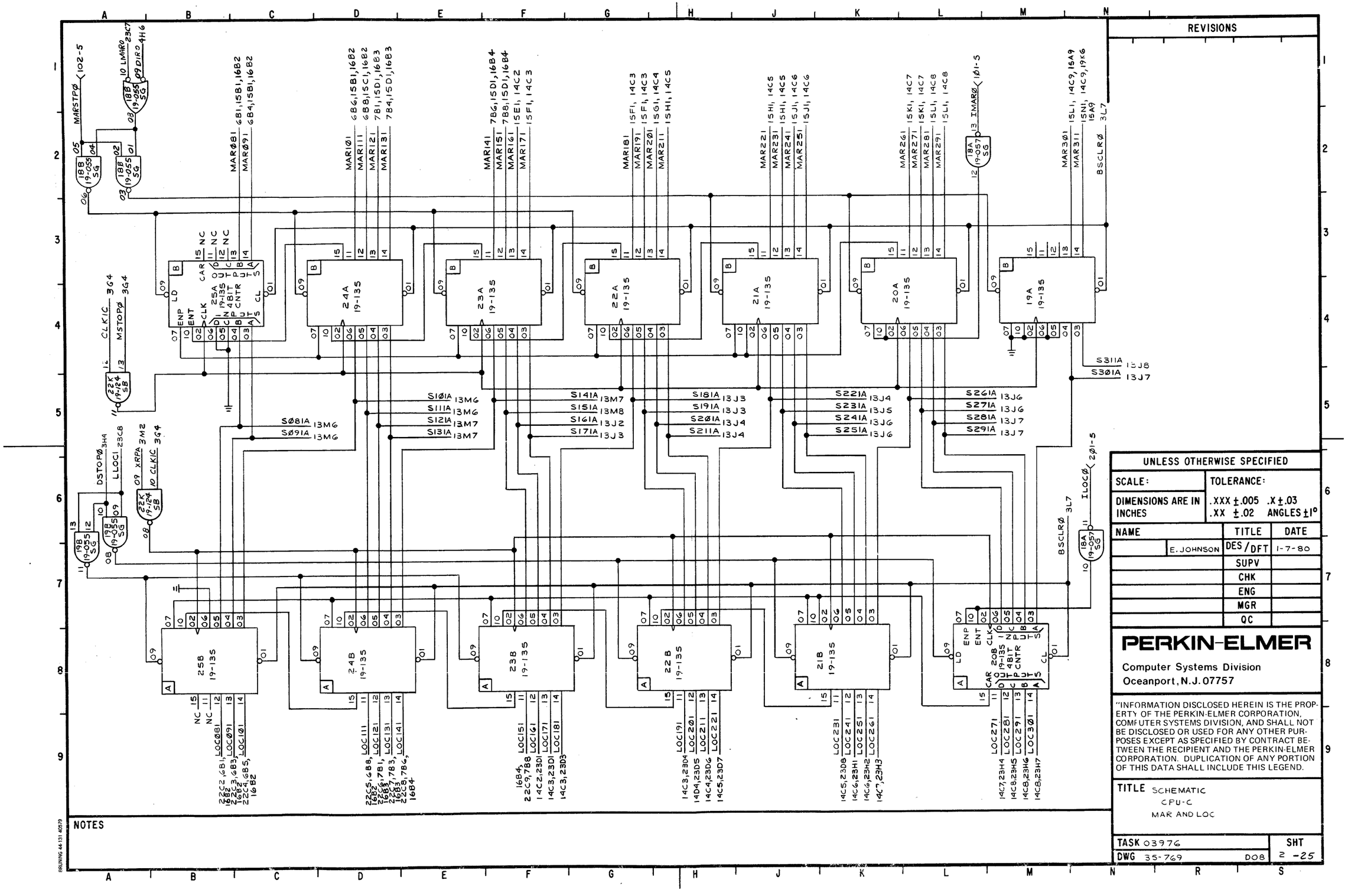
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C

TASK 03976

SHT 1 - 25

DWG 35-769 R03 D08



REVISIONS

NOTES

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
E. JOHNSON	DES/DFT	1-7-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
MAR AND LOC

TASK 03976

SHT 2-25

DWG 35-769 D08

BRUNING 44-131 40579

REVISIONS

14M 19-233 A
13M 19-233 A
12M 19-233 A
09H 19-231 DREG
11J 19-117 4-BIT MAG COMP
10J 19-117 4BIT MAG COMP.
DATA IN
DATA OUT
A<B A=B A>B
MDR071 17J5
MDR081 17F9
MDR091 17F9
MDR101 17G9
MDR111 17G9
MDR121 17G9
MDR131 17H9
MDR141 17H9
MDR161 18D7
MDR171 18E7
MDR181 18E7
MDR191 18F7
MDR201 18G7
MDR211 18G7
MDR221 18H7
MDR231 18H7
MDR241 19E7
MDR251 19F7
MDR261 19F7
MDR271 19G7
MDR281 19G7
MDR291 19G7
MDR301 19H7
MDR311 19H7
LPSTD0 2B45
LPSTD1 5G9
DCLK1 H7
LPSTDCK0 9A3
MDR151 17J9
XRPA J5, D7, 2A5
GETSSTE1 9N6
STD161 10B3
STD171 10B3
STD181 10B3
STD191 10D3
STD201 10D3
STD211 10D3
STD221 10E3
STD231 10E3
STD241 10F3
STD251 10F3
STD261 10G3
STD271 10H3
STD281 10H3
STD291 10J3
STD301 10J3
STD311 10L1
STD151 10B3
MSTOP0 2A4
CLKIC 12I-1, 2A4, 2B6
SCLK1 22I-0, 9A6
DSTOP0 21I-1, 2A6
SCLR0C 10-1
MCLK1 2B5-1
MCLK1A 15C9
A1B11 9N3, 15E6, 5F9
DCLK1 4L5, L1, 15A7
CLK1 15A7, 5N3, 5N9, 9A3, 11G6, 11J2,
BSCLR0A 9A2, 11M2, 15A7, 5A1, 9H4
BSCLR0 2N6, 2N2
PA081 6F3
PA091 6F5
PA101 6F7
PA111 6F9
PA121 7F3
PA131 7F5
PA141 7F7
PA151 7F9
EPSTD1 11A2
XRPA M2
09K 70 1K
TYPICAL "A" BOX CONFIGURATION 3 PLACES

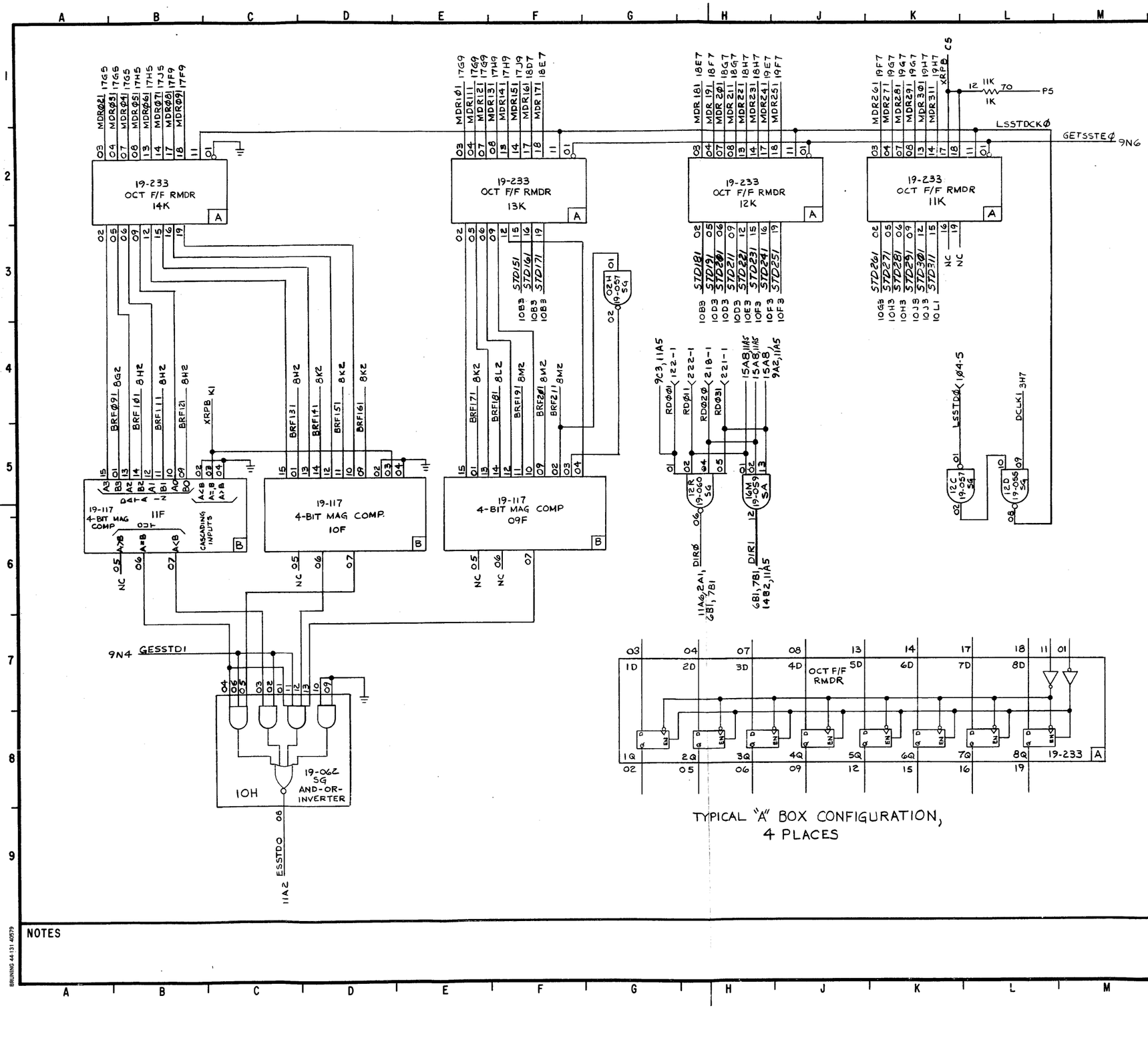
NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	A.WILLIAMS	DES/DFT	2-11-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
PROCESS SEGMENT TABLE DESCRIPTOR AND SEGMENT SIZE COMPARITOR

TASK 03976
DWG 35-769 D08
SHT 3 -25



NOTES

REVISIONS

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

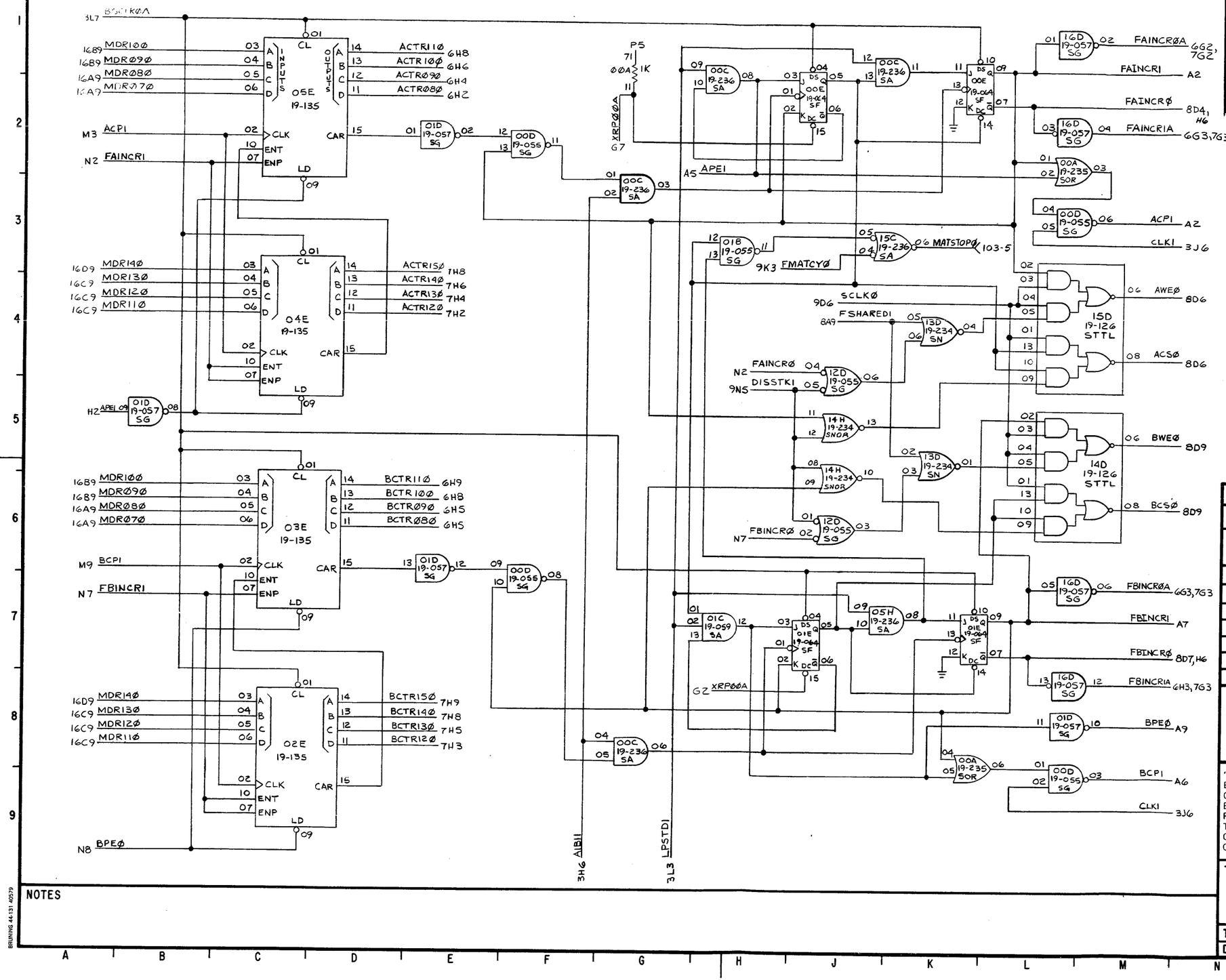
NAME		TITLE	DATE
	A. WILLIAMS	DES / DFT	2-11-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
SHARED SEGMENT TABLE DESCRIPTOR
AND SHARED SEGMENT SIZE COMPARITOR

TASK 03976	SHT 4 -25
DWG 35-769 D08	



NOTES

BRUNING 44-131-40579

REVISIONS				
REV. 15C TO ALT. LOGIC SYMBOL IN AREA J3				
E.C. J		4494	M	10-23-80 R01
AREA NB; REF GH: WH, 6C3				
JAT		4623	D	2-27-81 R02
EXTENSIVE CHANGES: FOR PREVIOUS REVISION SEE R02 MICROFILM. ADDED 2 SPARE GATES (14H 13 & 14H10) AREA J5.				
JLV		4907	MS	12-28-81 R03 X

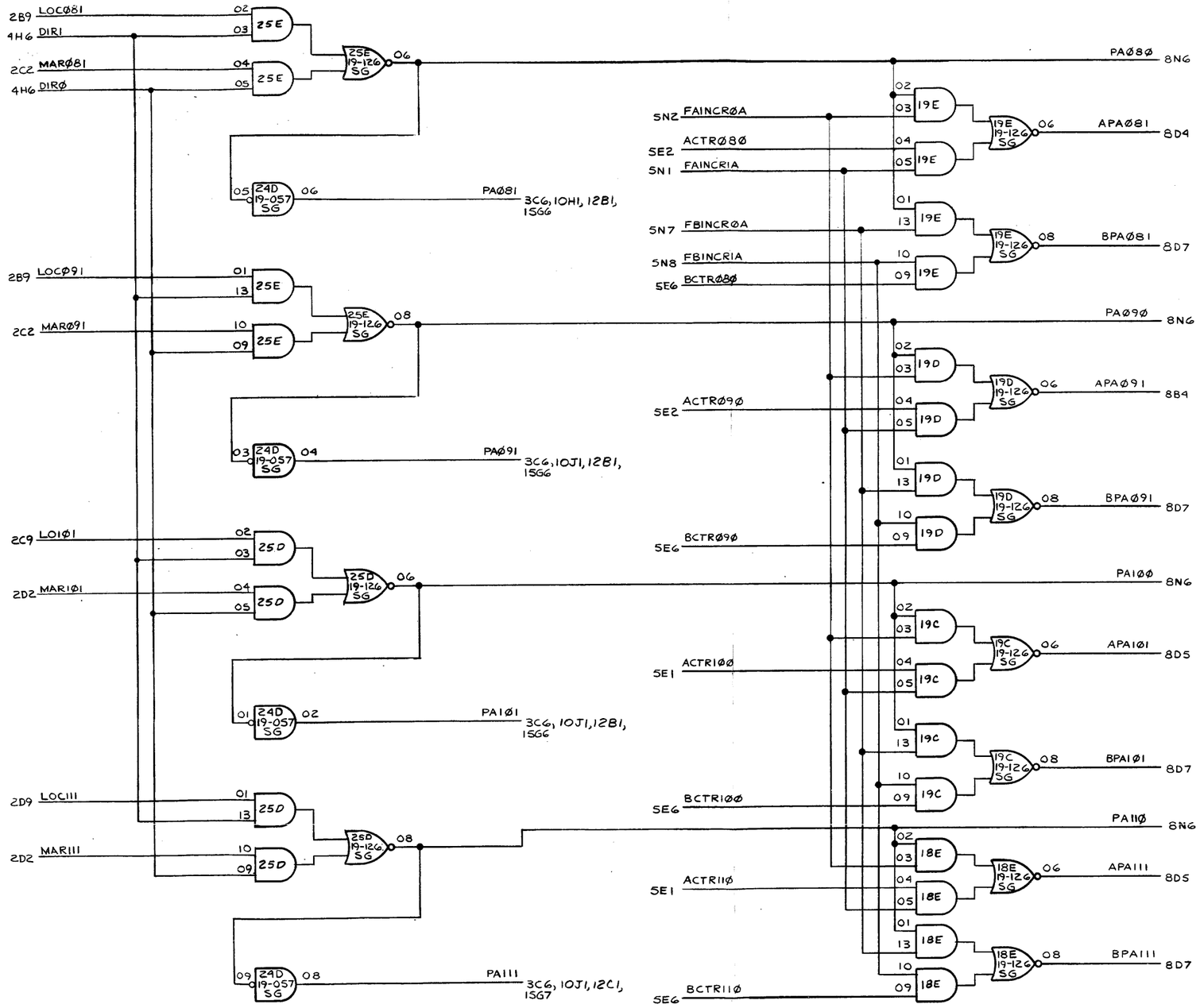
UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	A. WILLIAMS	DES/DFT	2-7-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE
SCHEMATIC
CPU-C
PRESENCE BIT INITIALIZATION

TASK 03976	SHT
DWG 35-769 RC3 D08	5 -25



REVISIONS

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .XX ±.02	.X ±.03 ANGLES ±1°
NAME	TITLE	DATE
A.WILLIAMS	DES/DFT	2-7-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

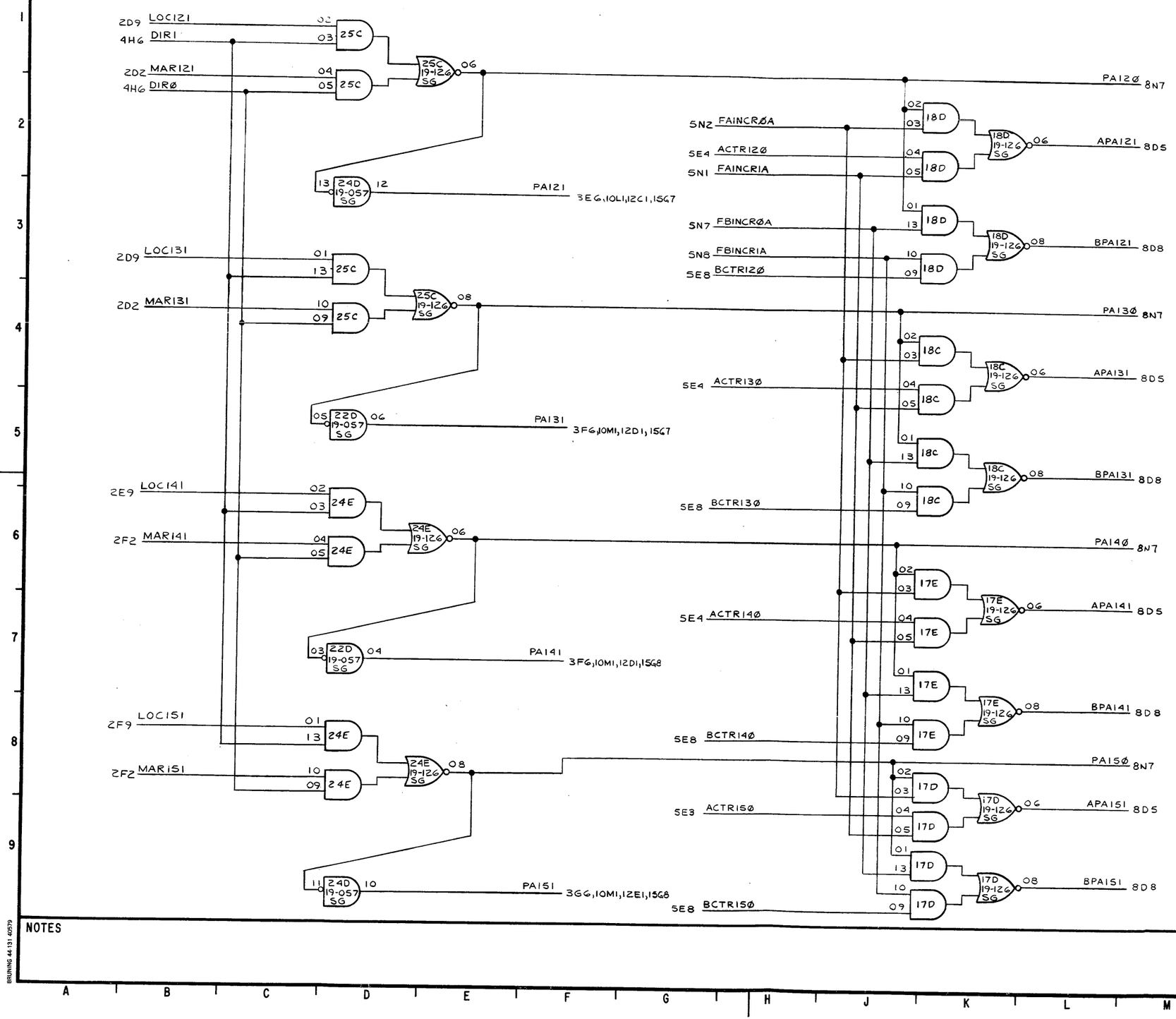
PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
PA LATCH 8-11

TASK 03976 SHT 6-25
DWG 35-769 D08

NOTES



REVISIONS

NOTES

BRUNING 44-131 40579

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	E.JOHNSON	DES/DFT	1-24-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
PA LATCH 12-15

TASK 03976 SHT 7 -25
DWG 35-769 D08

REVISIONS

AREA E6, I.C. 17F WAS 19-077, REV'D LOGIC SYMBOLS OF PINS 03,04,05,12 AREA E8, I.C. 16F WAS 19-077, REV'D LOGIC SYMBOLS OF PINS 03,04,05,12				
EJ	Bulk	4494	M	10-23-80 R01
AREA A9: DELETED FROM "FSHAREDI" REF 19A7				
JAT		4623	D	2-27-81 R02

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	A. WILLIAMS	DES/DFT	2-7-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

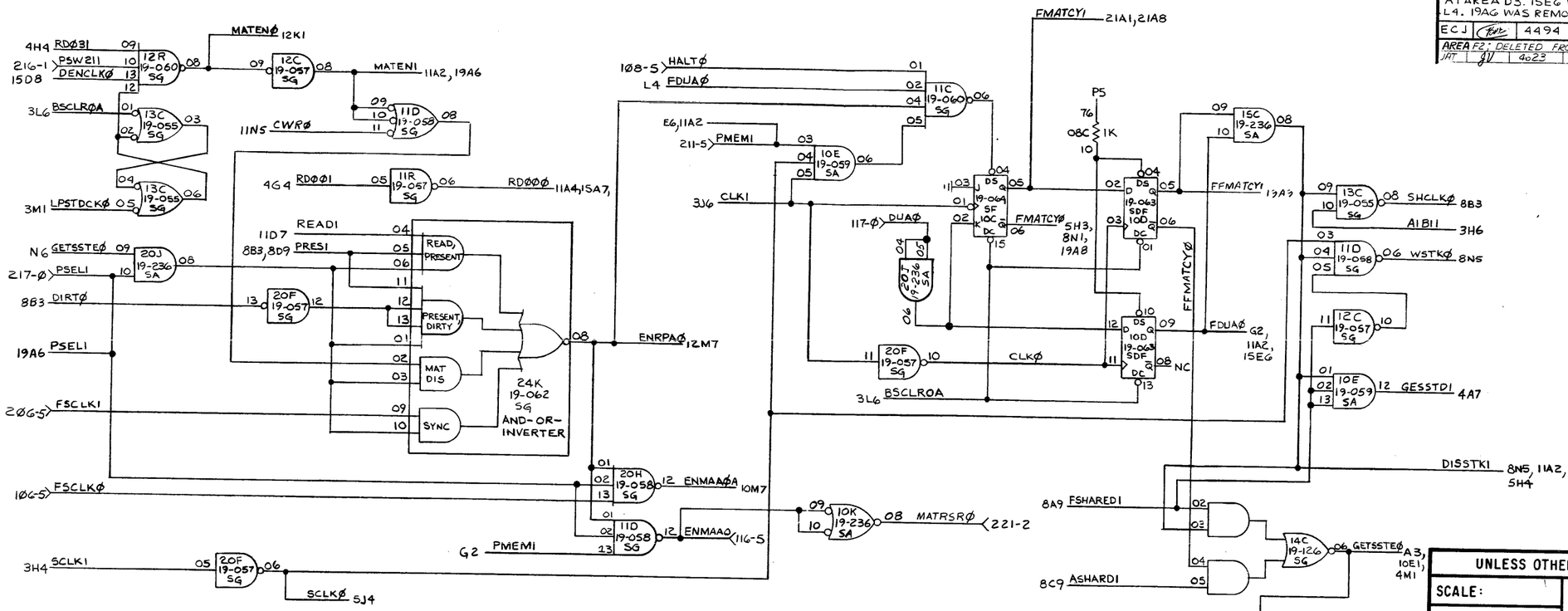
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC CPU-C
SEGMENT TABLE REGISTER STACKS AND STACK LOAD BUFFER

TASK 03976 SHT 8 - 25
DWG 35-769 R02 D08

NOTES

REVISIONS				
NMEMONIC "READ1" WAS ADDED TO PIN 29K09 AT AREA D3. PIN 29K09 WAS CONN. TO 11R05 AT AREA D3. 15E6 WAS ADDED TO "FDUAØ" AT L4. 19AG WAS REMOVED FROM "RD000" AT E3.				
ECJ	[illegible]	4494	M	10-23-80 R01
AREA F2: DELETED FROM PMEM1 REF 15E6.				
JAT	JV	4023	D	2-27-81 R02



NOTES

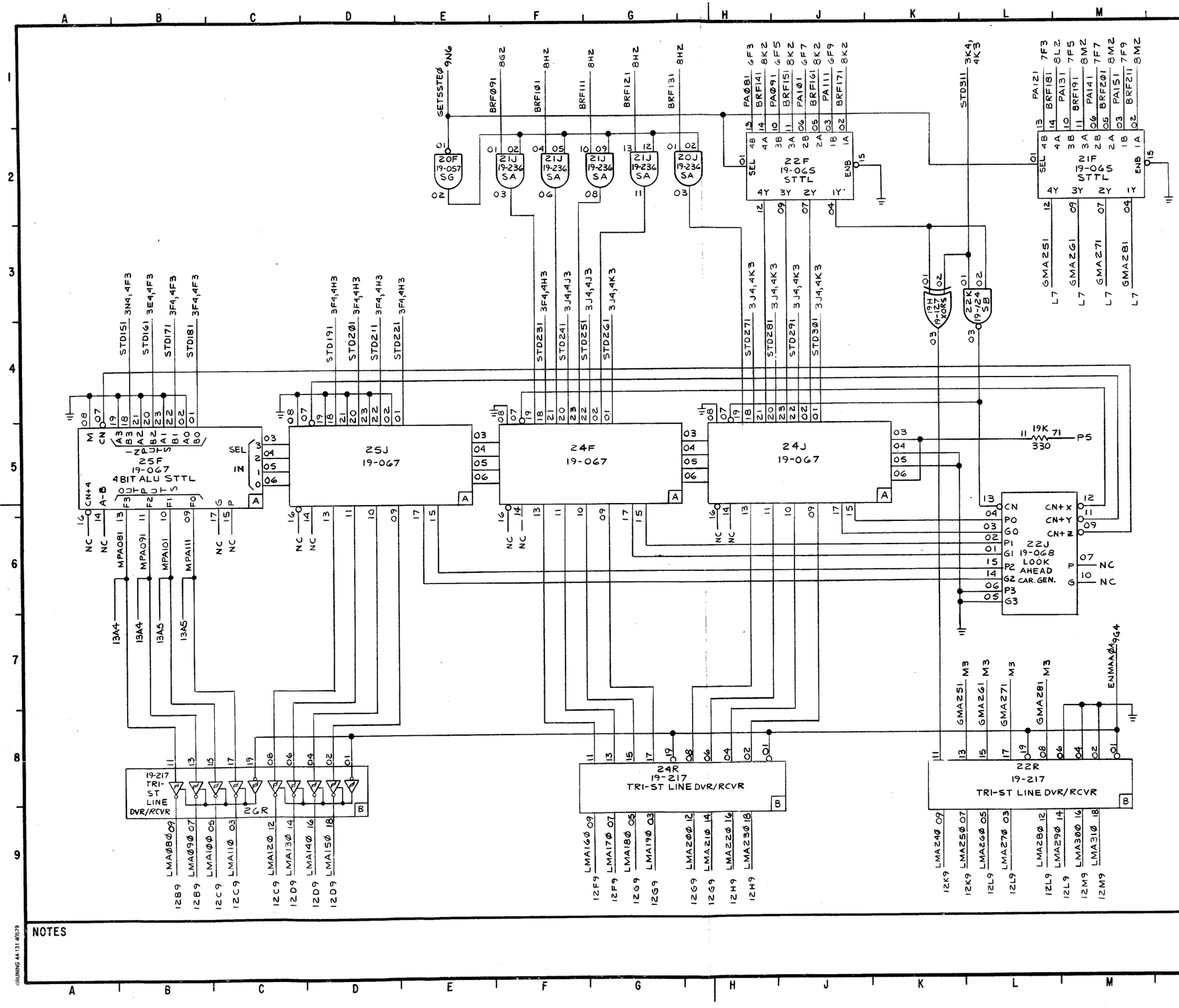
UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
A. WILLIAMS	DES/DFT	2-11-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
MAT CONTROL

TASK 03976
DWG 35-769 R02 D08
SHT 9 -25



NOTES

REVISIONS				
AREA FAB 16 24H PIN 14 WAS PIN 13				
JAT	GV	4623	D	2-27-81 KCH

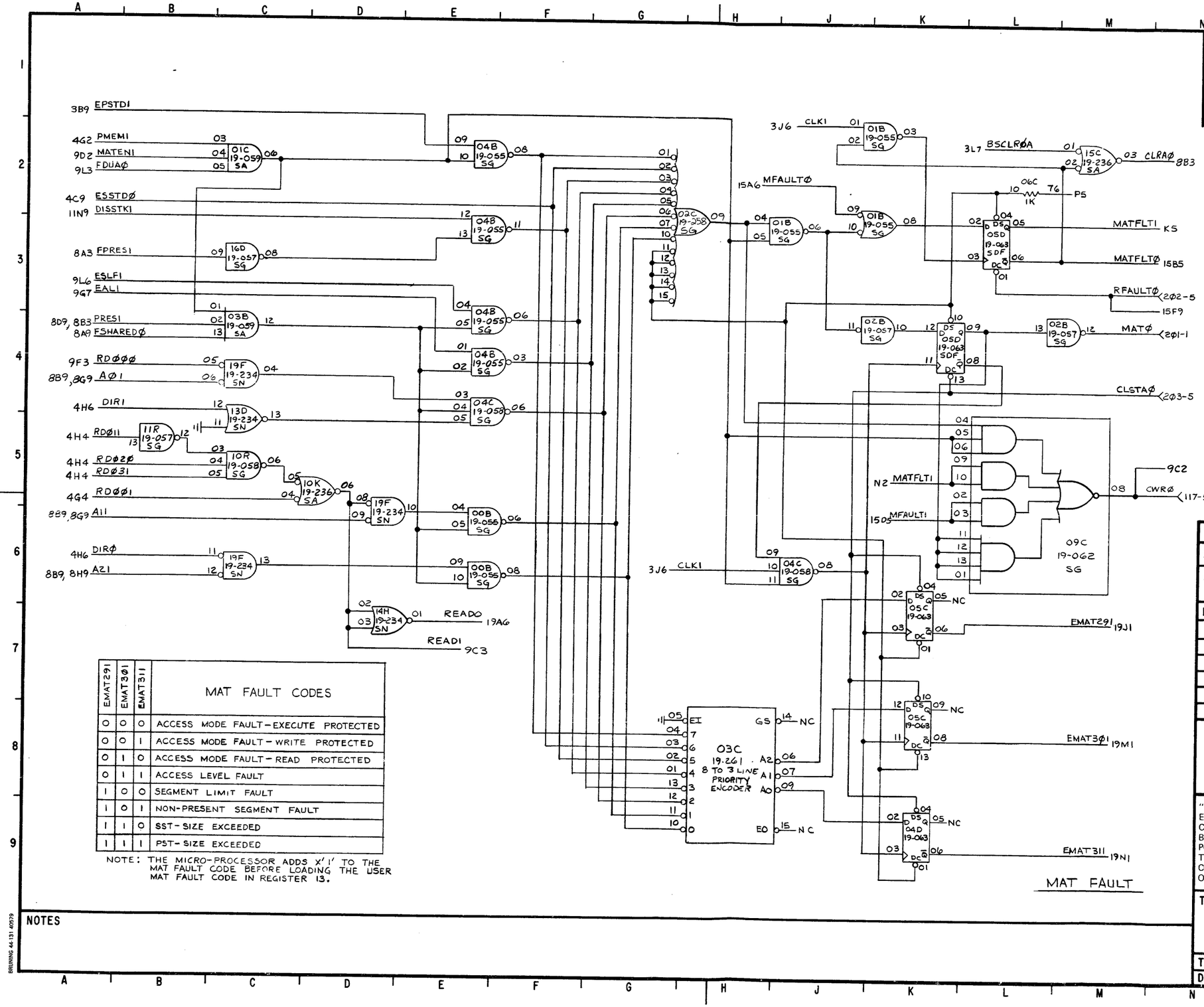
UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
A. WILLIAMS	DES/DFT	2-7-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
MAT RELOCATION SUMMER AND LMA DRIVERS

TASK 03976 SHT 10 -25
DWG 35-769 R01 D08



EMAT29I	EMAT3ØI	EMAT31I	MAT FAULT CODES
0	0	0	ACCESS MODE FAULT – EXECUTE PROTECTED
0	0	1	ACCESS MODE FAULT – WRITE PROTECTED
0	1	0	ACCESS MODE FAULT – READ PROTECTED
0	1	1	ACCESS LEVEL FAULT
1	0	0	SEGMENT LIMIT FAULT
1	0	1	NON-PRESENT SEGMENT FAULT
1	1	0	SST – SIZE EXCEEDED
1	1	1	PST – SIZE EXCEEDED

NOTE: THE MICRO-PROCESSOR ADDS X'1' TO THE MAT FAULT CODE BEFORE LOADING THE USER MAT FAULT CODE IN REGISTER 13.

REVISIONS

I.C. 14H 19-234 SN AT D7 WAS ADDED.					
ECJ	[illegible]	4494	M	10-23-80	R01

NOTES

UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

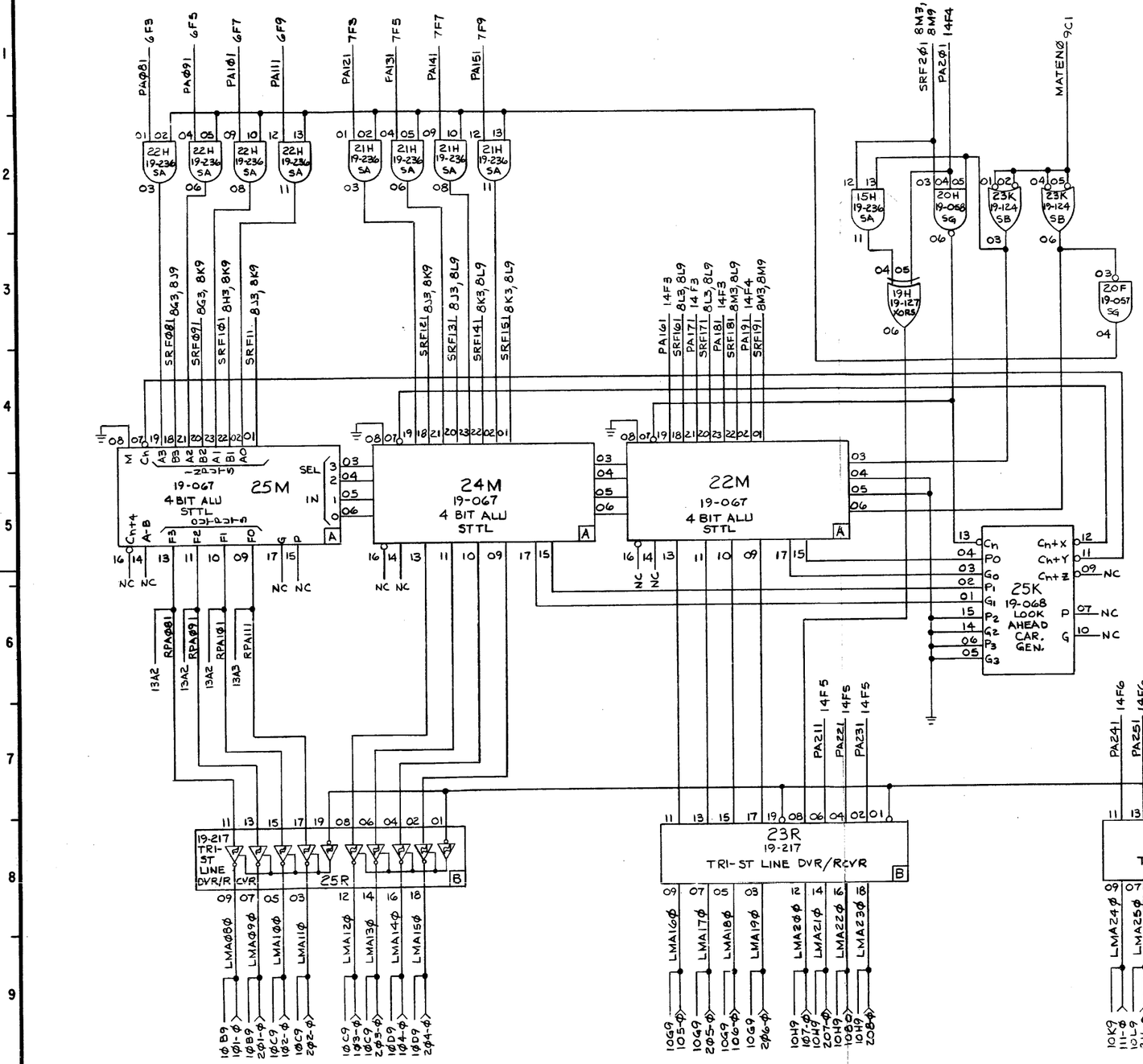
NAME		TITLE	DATE
	A.WILLIAMS	DES/DFT	2-7-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
MAT FAULT DECODE

TASK 03976
DWG 35-769 R01 D08
SHT 11 – 25



NOTES

REVISIONS

UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

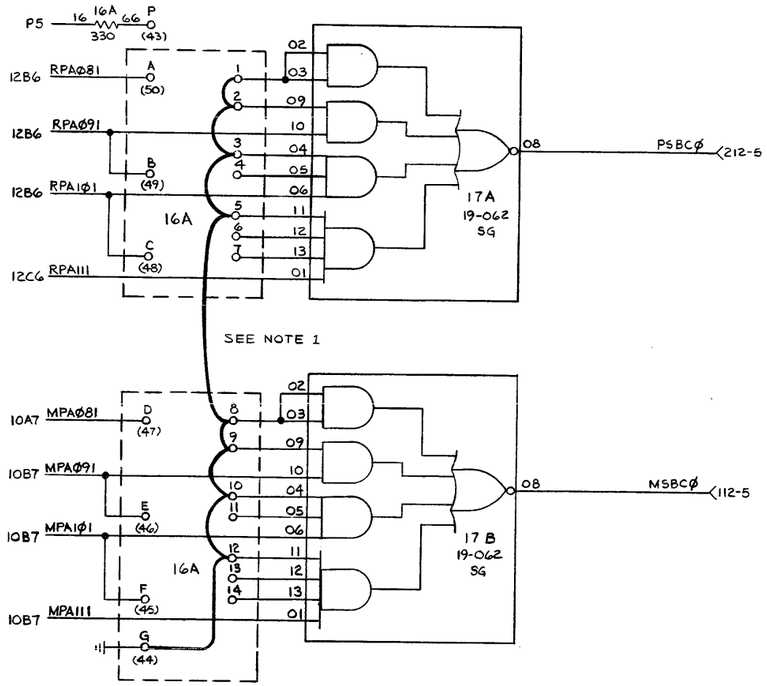
NAME	TITLE	DATE
A.WILLIAMS	DES/DFT	1-30-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
PROGRAM ADDRESS RELOCATION
SUMMER LMA DRIVERS

TASK 03976
DWG 35-769 D08
SHT 12 -25



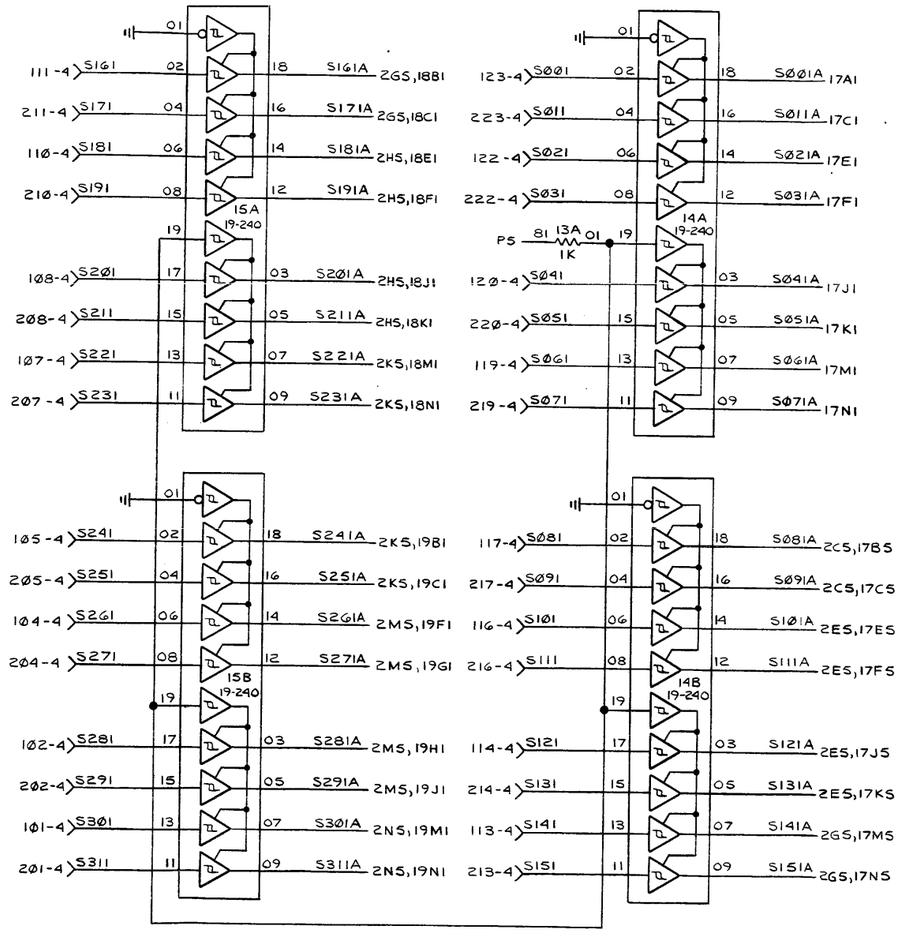


TABLE 1 SHARED/MEMORY STRAPPING																
TEST POINTS	MEGA BYTES OF SHARED MEMORY															
	Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	G	G	G	G	G	G	G	G	A	A	A	A	A	A	A	A	P
2	G	G	G	G	A	A	A	A	G	G	G	G	P	P	P	P	G
3	G	G	A	A	G	G	A	A	G	G	P	P	G	G	P	P	G
4	NC	NC	B	B	NC	NC	P	P	NC	NC	B	B	NC	NC	P	P	NC
5	G	A	G	A	G	A	G	A	G	P	G	P	G	P	G	P	G
6	NC	B	NC	B	NC	P	NC	P	NC	B	NC	B	NC	P	NC	P	NC
7	NC	C	NC	P	NC	C	NC	P	NC	C	NC	P	NC	C	NC	P	NC
8	G	G	G	G	G	G	G	G	D	D	D	D	D	D	D	D	P
9	G	G	G	G	D	D	D	D	G	G	G	G	P	P	P	P	G
10	G	G	D	D	G	G	D	D	G	G	P	P	G	G	P	P	G
11	NC	NC	E	E	NC	NC	P	P	NC	NC	E	E	NC	NC	P	P	NC
12	G	D	G	D	G	D	G	D	G	P	G	P	G	P	G	P	G
13	NC	E	NC	E	NC	P	NC	P	NC	E	NC	E	NC	P	NC	P	NC
14	NC	F	NC	P	NC	F	NC	P	NC	F	NC	P	NC	F	NC	P	NC

NOTE: NC=NO CONNECTION

NOTES 1. STRAPPING IS SHOWN FOR AN ALL LOCAL MEMORY SYSTEM, NO SHARED MEMORY. SEE TABLE 1 FOR LOCAL/SHARED MEMORY STRAPPING.

REVISIONS

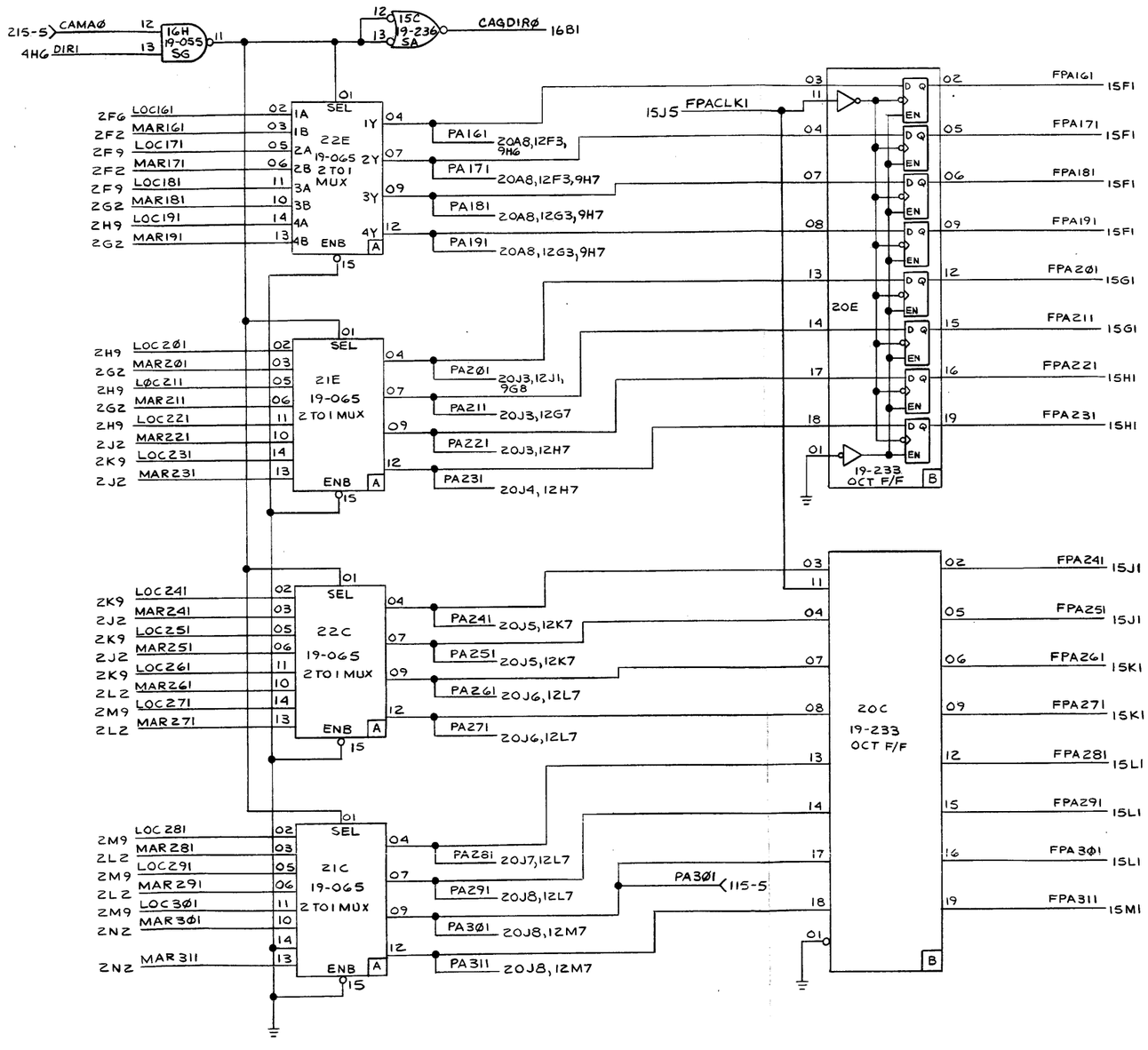
ADDED STRAP FROM PIN 9 (16A) TO 16A08 & 16A10 (GND)					
JLV	JV	4907	MS	12-28-81	R01 X

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	E. JOHNSON	DES/DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
LOCAL/SHARED MEMORY DETECTION

TASK 03976 | SHT 13 -25
DWG 35-769 R01 D08



REVISIONS

NOTES

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
E. JOHNSON	DES / DFT	1-28-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
PROGRAM ADDRESS MULTIPLEXOR AND LATCH

TASK 03976 SHT 14-25
DWG 35-769 D08

REVISIONS					
PIN 10E10 AT FG WAS PMEM1, 9G2					
ECJ	[illegible]	4494	M	10-23-80	R01

EIMARI

EIMARØ

FPACLKI 19G2

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	E. JOHNSON	DES/DFT	1-28-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

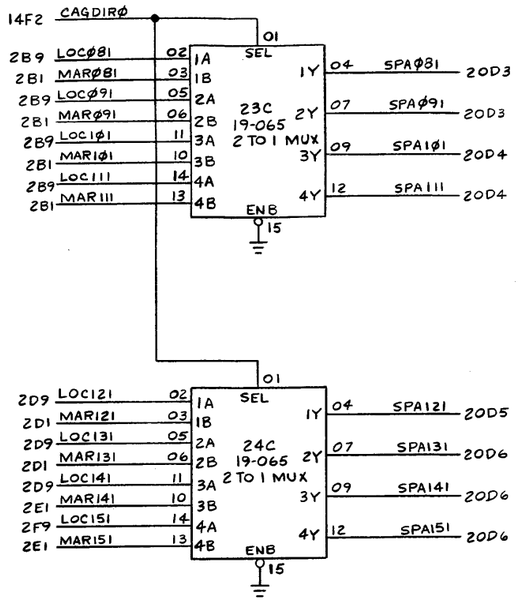
Computer Systems Division
Oceanport, N.J. 07757

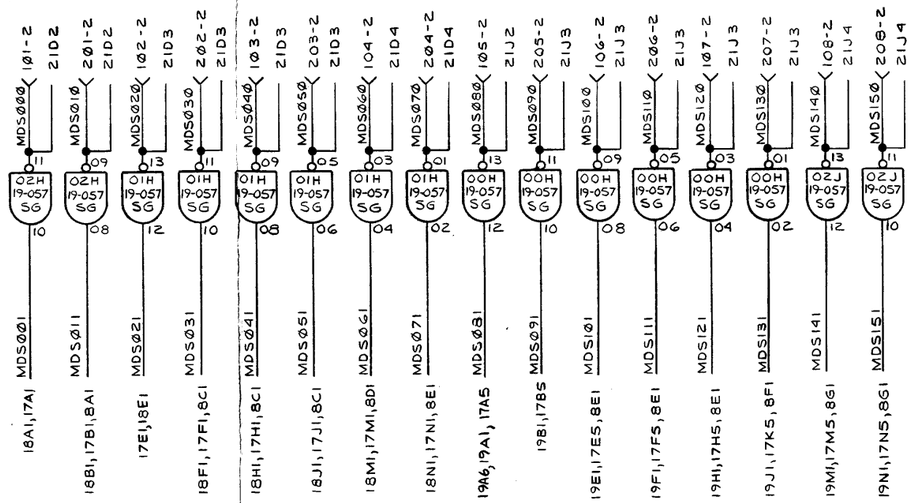
TITLE SCHEMATIC
CPU-C ZMAR

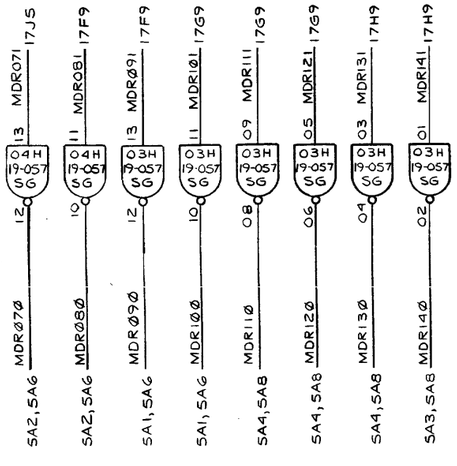
TASK 03976 | SHT 15 -25

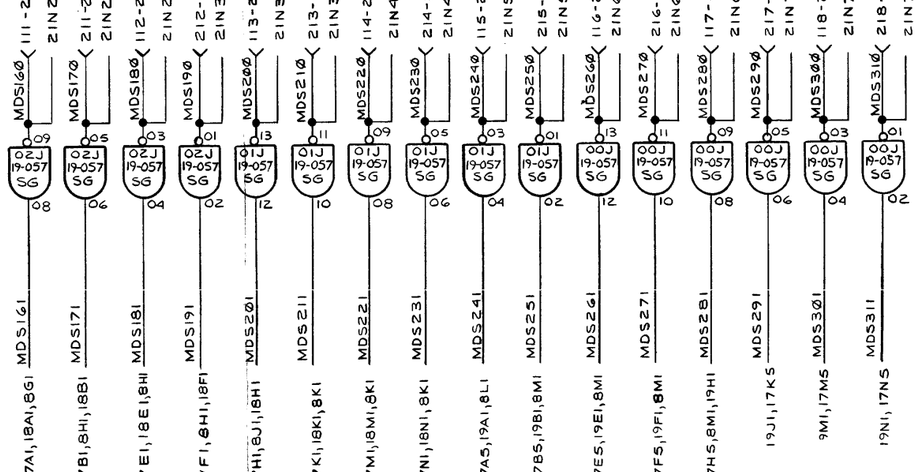
DWG 35-769 R01 D08

NOTES









NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
		DES/DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
MDS BUFFERS

TASK 03976	SHT 16-25
DWG 35-769 D08	

REVISIONS

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Oceanport, N.J. 07757

REVISIONS

B	A	MDR 0/15 MUX
0	0	EMD
0	1	OMS
1	0	MAT FAULT
1	1	S BUS

SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	2-11-80
		CHK	
		ENGR	

TITLE SCHEMATIC
CPU-C
PROCESSOR MDR
BITS 0-15

TASK NO. 03976 SHEET OF

DWG NO. 35-769 D08 17 – 25

PERKIN ELMER

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

B	A	MDR 16-23 DATA MUX
0	0	EMD
0	1	OMS
1	0	MAT FAULT
1	1	SBUS

SCALE—	NAME	TITLE	DATE	TITLE CPU-C PROCESSOR MDR BITS 16-23
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	2-11-80	
		CHK		
		ENGR		

TASK NO. 03976 | SHEET OF 18 — 25

DWG NO. 35-769 D08

PERKIN ELMER
Computer Systems Division
Oceanport N J 07757

REVISIONS				
PIN 11M03 AT A6 WAS RD000,11E6.				
LTR	ECO	4494	M	10-23-80	R01

MDS081 16K4
MDS241 16K9
S241A 13J6
MDL5A1 18B1
MDS818 18B1
MDS041 16K4
MDS251 16K9
S251A 13J6
19-116 04M STTL
INPUT 1 INPUT 2 1Y 2Y

MDS101 16K4
MDS261 16K9
S261A 13J6
MDS111 16L4
MDS271 16L9
S271A 13J6
19-116 03M STTL

MDS121 16L4
MDS281 16L9
S281A 13J7
MDS131 16M4
MDS291 16M9
EMAT291 11M7
S291A 13J7
19-116 02M STTL

MDS141 16M4
MDS301 16M9
EMAT301 11M8
S301A 13J7
MDS151 16M4
MDS311 16M9
EMAT311 11M9
S311A 13J8
19-116 01M STTL

18R1 MDLCKØ 09
R6 DISB1 10
09J 19-235 SOR 08

8A5 ASHRDØ
16K4 MDS ØB1
10K 19-236 SA 03
JAMSHRD1 8B1
09J 19-235 SOR
JAMDIRTØ 8B1

9A4 PSEL1 01
9D2 MATEN1 02
11E6 READØ 13
11M 19-059 SA 12
8B3 DIRTØ
8A9 FSHAREDØ
8B3 PRES1
10M 19-062 SG
MATRSDØ 222-2

15B6 XRPD
09D 19-063 SDF
9K3 FMATCYØ 11
08 NC
9M3 FFMATCY1

19-233 OOM
OCT F/F RMD3
MDR241 23H1 20J5, 4J1, 3J1, 21K5
MDR251 23H2 20J6, 4J1, 3J1, 21K6
MDR261 23H3 20J6, 4K1, 3J1, 21K4
MDR271 23H4 20J6, 4K1, 3J1, 21K6
MDR281 23H5 20J8, 4K1, 3J1, 21K7
MDR291 23H6 20J8, 4K1, 3J1, 21K7
MDR301 23H7 20J8, 4K1, 3K1, 21K7
MDR311 23H8 20J9, 4K1, 3K1, 21K7

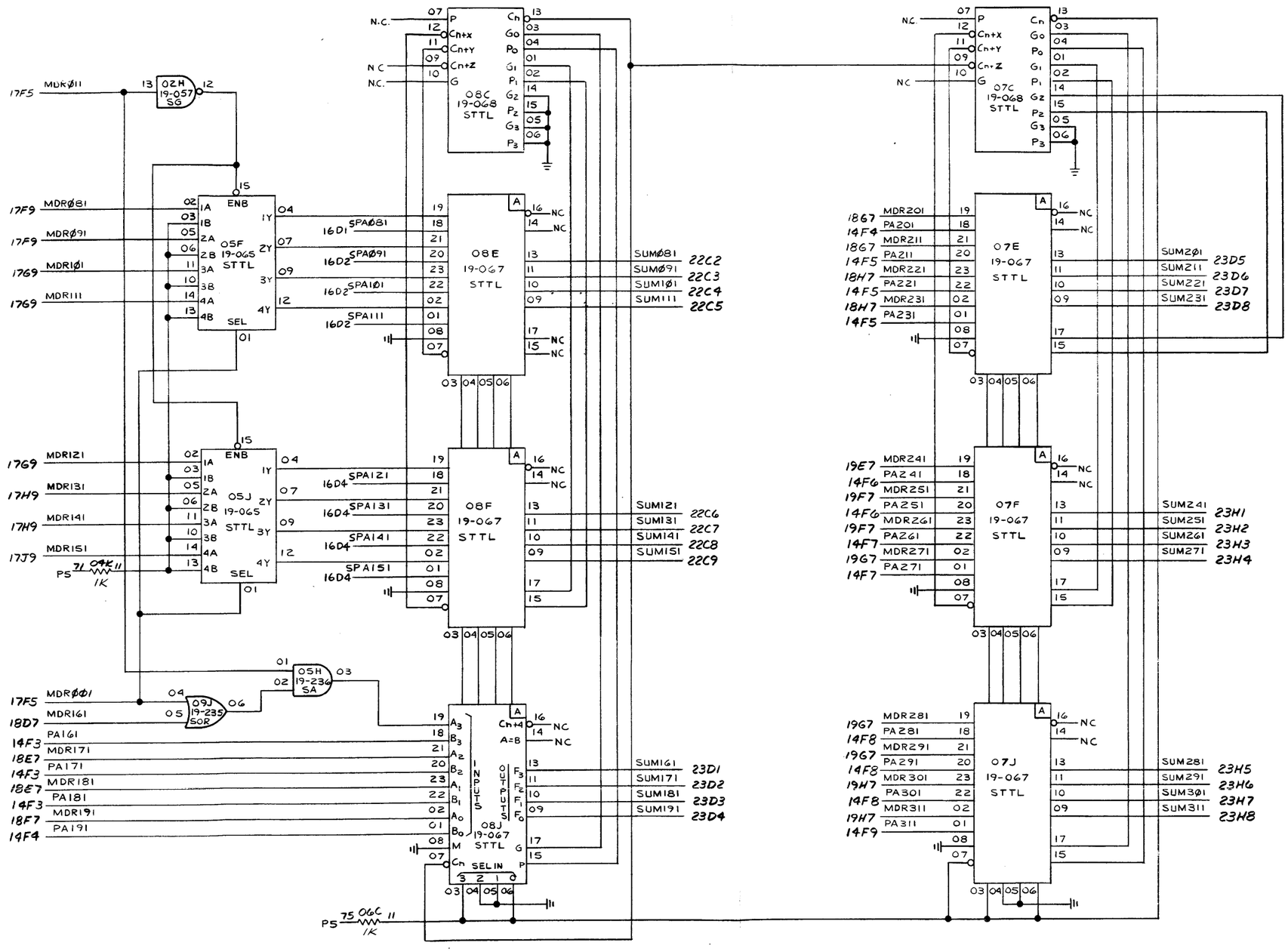
202-1 DEXBØ
2N1 MAR 311
LMDRØ 23C7
UMDRØ 22G2
11R 19-057 SG
11M 19-059 SA
18A 19-057 SG
14R 19-057 SG
11H 19-055 SG
DISA1 18R3
DISB1 D5
EXBØ 102-1

B	A	MDR24/31 DATA MUX
0	0	EMD
0	1	OMS
1	0	MAT FAULT
1	1	SBUS

SCALE—
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
A. WILLIAMS	DRAFT	2-7-80
	CHK	
	ENGR	

TITLE CPU-C PROCESSOR MDR BITS 24-31
TASK NO. 03976
DWG NO. 35-769 R01
SHEET OF 19—25



REVISIONS

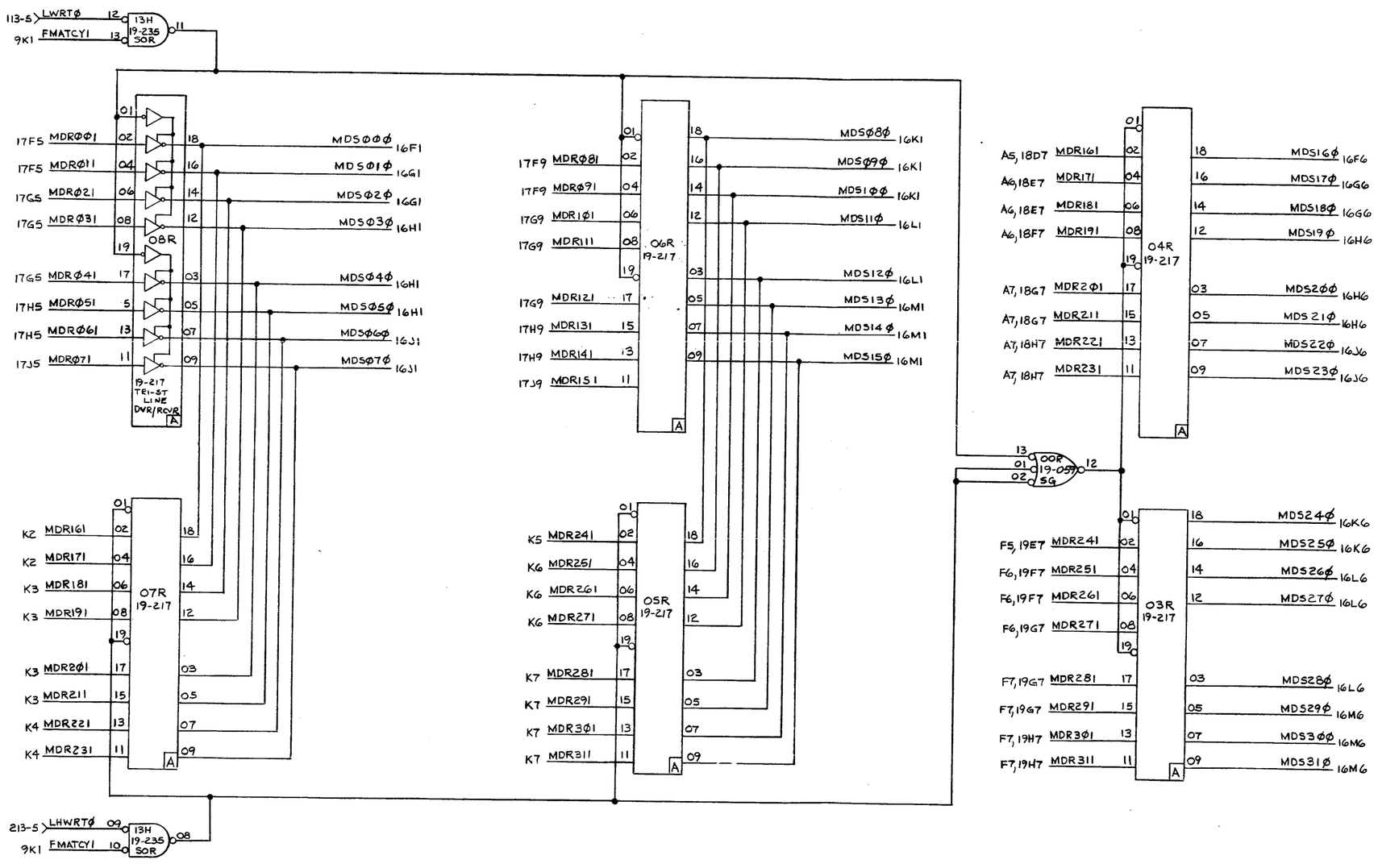
NOTES

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
E. JOHNSON	DES / DFT	1-3-79
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
MDR SUMMER AND EXTEND SIGN LOGIC

TASK 03976 SHT 20-25
DWG 35-769 D08



REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	A. WILLIAMS	DES / DFT	2-19-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

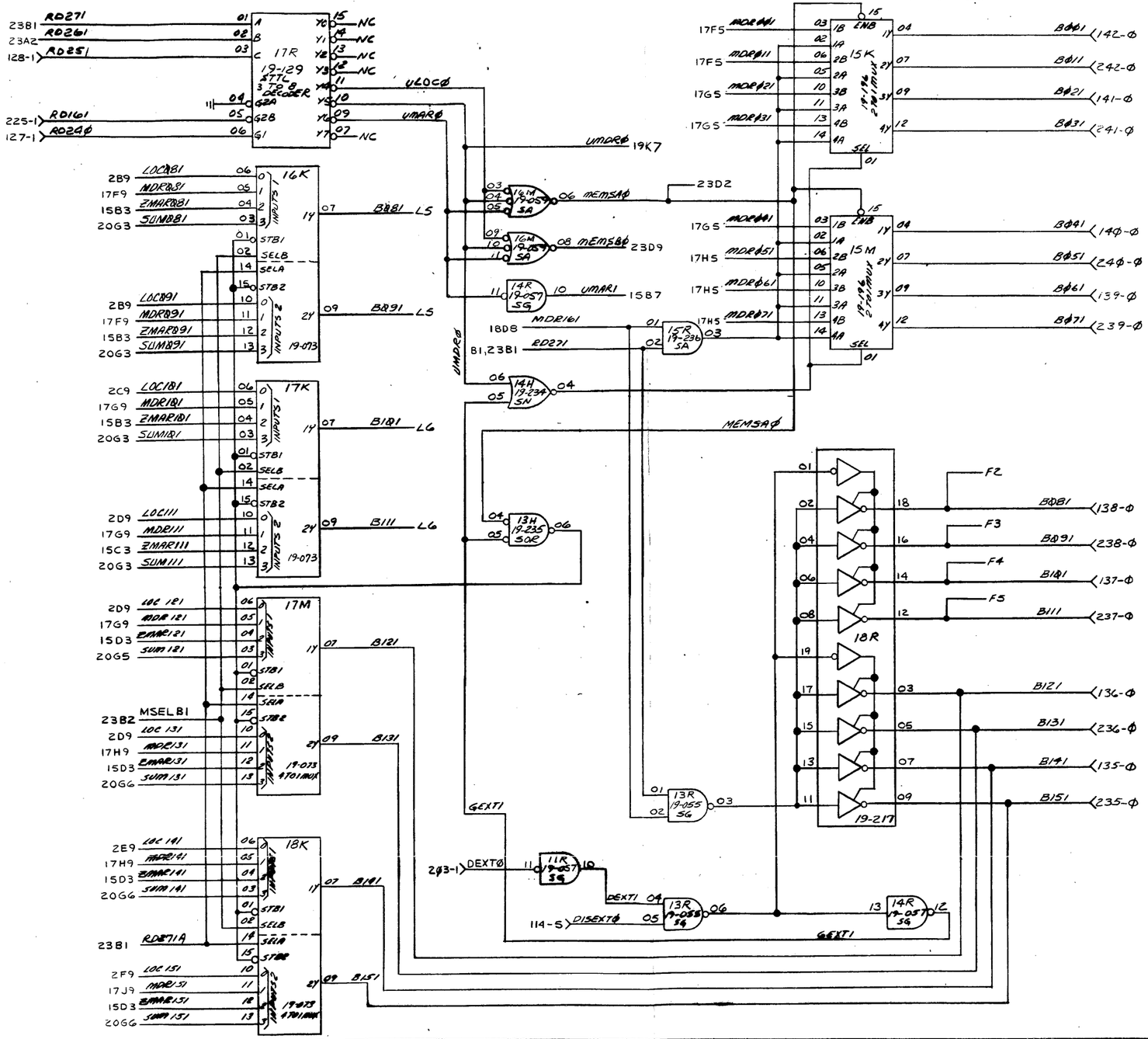
PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
MDS DRIVERS

TASK 03976 SHT 21 - 25
DWG 35-769 D08

NOTES



NOTES

REVISIONS

UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	A. WILLIAMS	DES / DFT	2-7-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
B-BUS DRIVERS
BITS ØØ-15

TASK 03976	SHT 22-25
DWG 35-769 D08	

PERKIN ELMER

Oceanport, N.J. 07757

REVISIONS

STB	B	A	"B" MUX
0	0	0	LOC
0	0	1	MDR
0	1	0	MAR
0	1	1	SUM
1	X	X	HI Z

22C9 RD271A
22G4, 22B1
229-1 > RD271
228-1 > KW261
22B1
Z14-5 > MDRE0
22C7 M5ELB1
14R 19-057 SG
14R 19-055 SG
01R 19-055 SG

2F9 LOC161
18D7 MDR161
15F3 ZMAR161
20G8 SUM161
22H2 MEMSA0
RD271A
18M 19-073 4 TO 1 MUX
B161 (132-0
2F9 LOC171
18E7 MDR171
15F3 ZMAR171
20G8 SUM171
B171 (232-0

2F9 LOC181
18E7 MDR181
15F3 ZMAR181
20G8 SUM181
B181 (131-0
2H9 LOC191
18F7 MDR191
15F3 ZMAR191
20G8 SUM191
19R 19-073 4TO1MUX
B191 (231-0

2H9 LOC201
18G7 MDR201
15G3 ZMAR201
20M3 SUM201
B201 (130-0
2H9 LOC211
18G7 MDR211
15H3 ZMAR211
20M3 SUM211
19K 19-073 4TO1MUX
B211 (230-0

2H9 LOC221
18H7 MDR221
15H3 ZMAR221
20M3 SUM221
2263 MEMSB0
B221 (129-0
2K9 LOC231
18H7 MDR231
15H3 ZMAR231
20M3 SUM231
19M 19-073 4TO1MUX
B231 (229-0

2K9 LOC241
19E7 MDR241
15J3 ZMAR241
20M5 SUM241
B241 (128-0
2K9 LOC251
19F7 MDR251
15J3 ZMAR251
20M6 SUM251
20R 19-073 4TO1MUX
B251 (228-0

2K9 LOC261
19F7 MDR261
15K3 ZMAR261
20M6 SUM261
B261 (127-0
2M9 LOC271
19G7 MDR271
15K3 ZMAR271
20M6 SUM271
20K 19-073 4TO1MUX
B271 (227-0

2M9 LOC281
19G7 MDR281
15L3 ZMAR281
20M8 SUM281
B281 (126-0
2M9 LOC291
19G7 MDR291
15L3 ZMAR291
20M8 SUM291
20M 19-073 4TO1MUX
B291 (226-0

2M9 LOC301
19H7 MDR301
15L3 ZMAR301
20M8 SUM301
B301 (125-0
19H7 MDR311
15M3 ZMAR311
20M8 SUM311
21K 19-073 4TO1MUX
B311 (225-0

125-1 > RD150 05 14R 19-057 SG 06
126-1 > RD191 02
226-1 > RD131 03
227-1 > RD121 04
19-168 LTTL 3 TO 8 DECODER 16R
01 A, 02 B, 03 C, 04 G2A, 05 G2B, 06 G1
Y0 15 NC, Y1 14 NC, Y2 13 NC, Y3 12 NC, Y4 11, Y5 10 LMDR0 19K7, Y6 09 LMAR0 2A1, Y7 07 NC
11, 20K, 1K, 7I, P5
LLOC0
14R 19-057 SG 01, 02 LLOC1 2A6

SCALE—
TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 10°
UNLESS OTHERWISE SPECIFIED

NAME | TITLE | DATE
DRAFT
CHK
ENGR

TITLE CPU-C
B-BUS DRIVER
BITS 16-31

TAB NO. 03976
DWG NO. 35-769 DOB
SHEET OF 23—25

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0001	ACTR08Ø	5	0063	BCTR12Ø	5	0125	ESLF1	9	0187	LMA11Ø	12	0249	MAR141	15	0311	MDSØ4Ø	16	0373	MPA1Ø1	10	0435	PSBCO	13	0497	SØ31A	13	0559	STD3Ø1	4	0621	2ØA15	2	0683	12D66	5
0002	ACTR09Ø	5	0064	BCTR13Ø	5	0126	EMAT291	19	0188	LMA12Ø	12	0250	MAR151	15	0312	MDSØ5Ø	16	0374	MPA111	10	0436	PRES1	8	0498	SØ41A	13	0560	STD311	4	0622	19B03	2	0684	Ø1C12	5
0003	ACTR1ØØ	5	0065	BCTR14Ø	5	0127	EMAT3Ø1	19	0189	LMA13Ø	12	0251	MAR161	15	0313	MDSØ6Ø	16	0375	MSTOPØ	3	0437	RFAULTØ	11	0499	SØ51A	13	0561	SUMØ81	20	0623	25B1Ø	2	0685	ØØCØ6	5
0004	ACTR11Ø	5	0066	BCTR15Ø	5	0128	EMAT311	19	0190	LMA14Ø	12	0252	MAR171	15	0314	MDSØ7Ø	16	0376	MARSTPØ	2	0438	RPAØ31	12	0500	SØ61A	13	0562	SUMØ91	20	0624	24A1Ø	2	0686	ØØA06	5
0005	ACTR12Ø	7	0067	BPAØ81	6	0129	EIMARO	15	0191	LMA15Ø	12	0253	MAR181	15	0315	MDSØ8Ø	16	0377	MCLKIA	3	0439	RPAØ41	12	0501	SØ71A	13	0563	SUM1Ø1	20	0625	23A1Ø	2	0687	ØØDØ3	5
0006	ACTR13Ø	7	0068	BPAØ91	6	0130	EIMARI	15	0192	LMA16Ø	12	0254	MAR191	15	0316	MDSØ9Ø	16	0378	MATSTOPØ	5	0440	RPA1Ø1	12	0502	SØ31A	13	0564	SUM111	20	0626	22A1Ø	2	0688	Ø1D12	5
0007	ACTR14Ø	7	0069	BPA1Ø1	6	0131	EXBO	19	0193	LMA17Ø	12	0255	MAR2Ø1	15	0317	MDS1ØØ	16	0379	MATEN0	9	0441	RPA111	12	0503	SØ91A	13	0565	SUM131	20	0627	18A1Ø	2	0689	13DØ1	5
0008	ACTR15Ø	7	0070	BPA111	6	0132	ENMAAO	9	0194	LMA18Ø	12	0256	MAR211	15	0318	MDS11Ø	16	0380	MATEN1	9	0442	RDØØØ	9	0504	S1Ø1A	13	0566	SUM151	20	0628	18AØ4	2	0690	Ø3E15	5
0009	APAØ81	6	0071	BPA121	7	0133	FPAØ81	15	0195	LMA19Ø	12	0257	MAR221	15	0319	MDS12Ø	16	0381	MFAULTØ	15	0443	RDØ01	4	0505	S111A	13	0567	SUM161	20	0629	19B03	2	0691	ØØA03	5
0010	APAØ91	6	0072	BPA131	7	0134	FPAØ91	15	0196	LMA2ØØ	12	0258	MAR231	15	0320	MDS13Ø	16	0382	MATFLTØ	11	0444	RDØ11	4	0506	S121A	13	0568	SUM171	20	0630	25BØ7	2	0692	15FØ7	8
0011	APA1Ø1	6	0073	BPA141	7	0135	FPA1Ø1	15	0197	LMA21Ø	12	0259	MAR241	15	0321	MDS14Ø	16	0383	MATO	11	0445	RDØ2Ø	4	0507	S131A	13	0569	SUM181	20	0631	22B1Ø	2	0693	15F1Ø	8
0012	APA111	6	0074	BPA151	7	0136	FPA111	15	0198	LMA22Ø	12	0260	MAR251	15	0322	MDS15Ø	16	0384	MSBCO	13	0446	RDØ31	4	0508	S141A	13	0570	SUM191	20	0632	23B1Ø	2	0694	15F15	8
0013	APA121	7	0075	BRFØ81	4	0137	FPA121	15	0199	LMA23Ø	12	0261	MAR261	15	0323	MDS16Ø	16	0385	MDHSAI	17	0447	RD121	23	0509	S151A	13	0571	SUM2Ø1	20	0633	24B1Ø	2	0695	15HØ8	8
0014	APA131	7	0076	BRFØ91	4	0138	FPA131	15	0200	LMA24Ø	12	0262	MAR271	15	0324	MDS17Ø	16	0386	MDSBIA	18	0448	RD131	23	0510	S161A	13	0572	SUM211	20	0634	19B11	2	0696	15HØ6	8
0015	APA141	7	0077	BRF1Ø1	4	0139	FPA141	15	0201	LMA25Ø	12	0263	MAR281	15	0325	MDS18Ø	16	0387	MDHCKO	17	0449	RD141	23	0511	S171A	13	0573	SUM221	20	0635	18AØ6	2	0697	15HØ3	8
0016	APA151	7	0078	BRF111	4	0140	FPA151	15	0202	LMA26Ø	12	0264	MAR291	15	0326	MDS19Ø	16	0388	MDLCKO	18	0450	RD161	22	0512	S181A	13	0574	SUM231	20	0636	14MØ2	3	0698	16HØ3	8
0017	ACSO	5	0079	BRF121	4	0141	FPA161	14	0203	LMA27Ø	12	0265	MAR3Ø1	15	0327	MDS2ØØ	16	0389	MATFLT1	11	0451	RD251	22	0513	S191A	13	0575	SUM241	20	0637	14MØ5	3	0699	16HØ6	8
0018	AWEO	5	0080	BRF131	4	0142	FPA171	14	0204	LMA28Ø	12	0266	MAR311	15	0328	MDS21Ø	16	0390	MFAULT1	15	0452	RD261	23	0514	S2Ø1A	13	0576	SUM251	20	0638	14MØ6	3	0700	13CØ6	9
0019	AØ1	8	0081	BRF141	4	0143	FPA181	14	0205	LMA29Ø	12	0267	MDRØ7Ø	16	0329	MDS22Ø	16	0391	MDLSA1	18	0453	RD271	23	0515	S211A	13	0577	SUM261	20	0639	14M09	3	0701	2ØJØ8	9
0020	A11	8	0082	BRF151	4	0144	FPA191	14	0206	LMA3ØØ	12	0268	MDRØ8Ø	16	0330	MDS23Ø	16	0392	MDSBIB	18	0454	RD271A	23	0516	S221A	13	0578	SUM271	20	0640	14M12	3	0702	2ØF12	9
0021	A21	8	0083	BRF161	4	0145	FPA2Ø1	14	0207	LMA31Ø	12	0269	MDRØ9Ø	16	0331	MDS24Ø	16	0393	MDSBO	18	0455	RD15Ø	23	0517	S231A	13	0579	SUM281	20	0641	14M15	3	0703	11RØ2	9
0022	A1B11	3	0084	BRF171	4	0146	FPA211	14	0208	LOCØ81	2	0270	MDR1ØØ	16	0332	MDS25Ø	16	0394	MSELB1	23	0456	RD24Ø	22	0518	S241A	13	0580	SUM291	20	0642	14M16	3	0704	11RØ4	9
0023	ALGN0	15	0085	BRF181	4	0147	FPA221	14	0209	LOCØ91	2	0271	MDR11Ø	16	0333	MDS26Ø	16	0395	MEMSAØ	22	0457	SØØ1	13	0519	S251A	13	0581	SUM3Ø1	20	0643	14M19	3	0705	11CØ6	9
0024	ACP1	5	0086	BRF191	4	0148	FPA231	14	0210	LOC1Ø1	2	0272	MDR12Ø	16	0334	MDS27Ø	16	0396	MEMSBØ	22	0458	SØ11	13	0520	S261A	13	0582	SUM311	20	0644	1ØJØ7	3	0706	13CØ3	9
0025	APE1	5	0087	BRF2Ø1	4	0149	FPA241	14	0211	LOC111	2	0273	MDR13Ø	16	0335	MDS28Ø	16	0397	MDREO	23	0459	SØ21	13	0521	S271A	13	0583	UMARI	22	0645	17J06	3	0707	08C1Ø	9
0026	ASHRD1	8	0088	BRF211	10	0150	FPA251	14	0212	LOC121	2	0274	MDR14Ø	16	0336	MDS29Ø	16	0398	PAØ86	6	0460	SØ31	13	0522	S281A	13	0584	UMARO	22	0646	1ØJØ5	3	0708	12C1Ø	9
0027	BØØ1	22	0089	BPEO	5	0151	FPA261	14	0213	LOC131	2	0275	MDRØØ1	17	0337	MDS3ØØ	16	0399	PAØ96	6	0461	SØ41	13	0523	S291A	13	0585	UMDRO	22	0647	12H08	3	0709	1ØD06	9
0028	BØ11	22	0090	BWEO	5	0152	FPA271	14	0214	LOC141	2	0276	MDRØ11	17	0338	MDS31Ø	16	0400	PA1ØØ	6	0462	SØ51	13	0524	S3Ø1A	13	0586	WSTKO	9	0648	14K02	4	0710	1ØD05	9
0029	BØ21	22	0091	BCSO	5	0153	FPA281	14	0215	LOC151	2	0277	MDRØ21	17	0339	MDSØØ1	16	0401	PA11Ø	6	0463	SØ61	13	0525	S311A	13	0587	XRPA	3	0649	14K05	4	0711	22DØ8	9
0030	BØ31	22	0092	BCP1	5	0154	FPA291	14	0216	LOC161	2	0278	MDRØ31	17	0340	MDSØ11	16	0402	PA12Ø	7	0464	SØ71	13	0526	SCLK1	3	0588	XRPØØA	5	0650	14K06	4	0712	16C08	9
0031	BØ41	22	0093	BSCLRØ	3	0155	FPA3Ø1	14	0217	LOC171	2	0279	MDRØ41	17	0341	MDSØ21	16	0403	PA13Ø	7	0465	SØ81	13	0527	SCLRØC	3	0589	XRPB	4	0651	14K09	4	0713	1ØE06	9
0032	BØ51	22	0094	BSCLRØA	3	0156	FPA311	14	0218	LOC181	2	0280	MDRØ51	17	0342	MDSØ31	16	0404	PA14Ø	7	0466	SØ91	13	0528	SCLKØ	9	0590	XRPD	15	0652	14K12	4	0714	21JØ3	10
0033	BØ61	22	0095	BAØ1	8	0157	FAINCRØA	5	0219	LOC191	2	0281	MDRØ61	17	0343	MDSØ41	16	0405	PA15Ø	7	0467	SØ81	13	0529	SHCLKØ	8	0591	ULOCO	22	0653	14K15	4	0715	21JØ6	10
0034	BØ71	22	0096	BA11	8	0158	FAINCR1	5	0220	LOC2Ø1	2	0282	MDRØ71	17	0344	MDSØ51	16	0406	PAØ81	6	0468	S111	13	0530	SHARED1	8	0592	ZMARØ81	15	0654	14K16	4	0716	21JØ8	10
0035	BØ81	22	0097	BA21	8	0159	FAINCRØ	5	0221	LOC211	2	0283	MDRØB1	17	0345	MDSØ61	16	0407	PAØ91	6	0469	S121	13	0531	SRFØ81	8	0593	ZMARØ91	15	0655	14K19	4	0717	2ØF02	10
0036	BØ91	22	0098			0160	FAINCRIA	5	0222	LOC221	2	0284	MDRØ91	17	0346	MDSØ71	16	0408	PA1Ø1	6	0470	S131	13	0532	SRFØ91	8	0594	ZMAR1Ø1	15	0656	13K02	4	0718	2ØJØ3	10
0037	B1Ø1	22	0099	CAMAO	14	0161	FBINCRØ	5	0223	LOC231	2	0285	MDR1Ø1	17	0347	MDSØ81	16	0409	PA 111	6	0471	S141	13	0533	SRF1Ø1	8	0595	ZMAR111	15	0657	13K05	4	0719	22F12	10
0038	B111	22	0100	CLK1	3	0162	FBINCR1	5	0224	LOC241	2	0286	MDR 111	17	0348	MDSØ91	16	0410	PA 121	7	0472	S151	13	0534	SRF 111	8	0596	ZMAR121	15	0658	13K06	4	0720	22FØ9	10
0039	B121	22	0101	CLSTAO	11	0163	FBINCRØN	5	0225	LOC251	2	0287	MDR121	17	0349	MDS1Ø1	16	0411	PA 131	7	0473	S161	13	0535	SRF 121	8	0597	ZMAR131	15	0659	13K09	4	0721	22FØ7	10
0040	B131	22	0102	CLK1C	3	0164	FBINCRIA	5	0226	LOC261	2	0288	MDR131	17	0350	MDS 111	16	0412	PA141	7	0474	S171	13	0536	SRF131	8	0598	ZMAR141	15	0660	13K12	4	0722	22FØ4	10
0041	B141	22	0103	CLKØ	9	0165	FSHAREDI	8	0227	LOC271	2	0289	MDR141	17	0351	MDS 121	16	0413	PA151	7	0475	S181	13	0537	SRF141	8	0599	ZMAR151	15	0661	02HB2	4	0723	22J12	10
0042	B151	22	0104	CWRO	11	0166	FSHAREDØ	8	0228	LOC281	2	0290	MDR151	17	0352	MDS131	16	0414	PA161	14	0476	S191	13	0538	SRF151	8	0600	ZMAR161	15	0662	12C02	4	0724	22J11	10
0043	B161	23	0105	DSTOPØ	3	0167	FPRES1	8	0229	LOC291	2	0291	MDR161	18	0353	MDS 141	16	0415	PA171	14	0477	S2Ø1	13	0539	SRF161	8	0601	ZMAR171	15	0663	11F06	4	0725	22J09	10
0044	B171	23	0106	DIRØ	4	0168	FMATCY1	9	0230	LOC3Ø1	2	0292	MDR171	18	0354	MDS151	16	0416	PA181	14	0478	S211	13	0540	SRF171	8	0602	ZMAR181	15	0664	11F07	4	0726	25J13	10
0045	B181	23	0107	DCLK1	3	0169	FSCLK1	9	0231	LPSTDCKØ	3	0293	MDR181	18	0355	MDS161	16	0417	PA191	14	0479	S221	13	0541	SRF181	8	0603	ZMAR191	15	0665	19F07	4	0727	25J11	10
0046	B191	23	0108	DIR1	4	0170	FSCLKØ	9	0232	LPSTD1	3	0294	MDR191	18	0356	MDS171	16	0418	PA2Ø1	14	0480	S231	13	0542	SRF191	8	0604	ZMAR2Ø1	15	0666	18F06	4	0728	25J1Ø	10
0047	B2Ø1	23	0109	DISSTK1	8	0171	FDUAØ	9	0233	LPSTDØ	3	0295	MDR2Ø1	18	0357	MDS181	16	0419	PA211	14	0481	S241	13	0543	SRF2Ø1	8	0605	ZMAR211	15	0667	Ø9F07	4	0729	25JØ9	10
0048	B211	23	0110	DISSTKØ	8	0172	FNCEO	15	0234	LLOC1	23	0296	MDR211	18	0358	MDS191	16	0420	PA221	14	0482	S251	13	0544	STD151	4	0606	ZMAR221	15	0668	Ø1EØ5	5	0730	24F13	10
0049	B221	23	0111	DUAO	9	0173	FPACLK1	15	0235	LMARO	23	0297	MDR221	18	0359	MDS2Ø1	16	0421	PA231	14	0483	S261	13	0545	STD161	4	0607	ZMAR231	15	0669	13DØ4	5	0731	24F11	10
0050	B231	23	0112	DIRTO	8	0174	GMA 251	10	0236	LMDRO	23	0298	MDR231	18	0360	MDS211	16	0422	PA241	14	0484	S271	13	0546	STD171	4	0608	ZMAR241	15	0670	Ø4E15	5	0732	24F1Ø	10
0051	B241	23	0113	DEXBO	19	0175	GMA 261	10	0237	LSSTDO	4	0299	MDR241	19	0361	MDS221	16	0423	PA251	14	0485	S281	13	0547	STD181	4	0609	ZMAR251	15	0671	ØSE15	5	0733	24FØ9	10
0052	B251	23	0114	DISA1	19	0176	GMA 271	10	0238	LSSTDCKØ	4	0300	MDR251	19	0362	MDS231	16	0424	PA261	14	0486	S291	13	0548	STD191	4	0610	ZMAR261	15	0672	Ø1DØ2	5	0734	19K11	10
0053	B261	23	0115	DISBI	19	0177	GMA 281	10	0239	LØ1	8	0301	MDR261	19	0363	MDS241	16	0425	PA271	14	0487	S3Ø1	13	0549	STD2Ø1	4	0611	ZMAR271	15	0673	Ø1DØ8	5	0735	22K03	10
0054	B271	23	0116	DISEXTØ	22	0178	GETSSTE1	3	0240	L11	8	0302	MDR271	19	0364	MDS251	16	0426	PA281	14	0488	S311	13	0550	STD211	4	0612	ZMAR281	15	0674	Ø2E15	5	0736	25J17	10
0055	B281	23	0117	DEXTØ	22	0179	GETSSTEØ	9	0241	LHWRTO	21	0303	MDR281	19	0365	MDS261	16	0427	PA291	14	0489	SLFØ1	8	0551	STD221	4	0613	ZMAR291	15	0675	ØØE06	5	0737	25J15	10
0056	B291	23	0118	DEXT1	22	0180	GEXT1	22	0242	LWRTO	21	0304	MDR291	19	0366	MDS271	16	0428	PA3Ø1	14	0490	SLF11	8	0552	STD231	4	0614	ZMAR3Ø1	15	0676	ØØD11	5	0738	24F17	10
0057	B3Ø1	23	0119	DRD1	15	0181	HALTO	9	0243	MARØ81	15	0305	MDR3Ø1	19	0367	MDS281	16	0429	PA 311	14	0491	SLF21	8	0553	STD241	4	0615	ZMAR311	15	0677	ØØC03	5	0739	24F15	10
0058	B311	23	0120	EPSTD1	3	0182	ILOCO	2	0244	MARØ91	15	0306	MDR311	19	0368	MDS291	16	0430	PSEL1	9	0492	SLF31	8	0554	STD251	4	0616	18BØ6	2	0678	ØØC11	5	0740	24J17	10
0059	BCTRØ8Ø	5	0121	ESSTDØ	4	0183	IMARO	2	0245	MAR1Ø1	15	0307	MDSØØØ	16	0369	MDS3Ø1	16	0431	PSW1Ø1	9	0493	SLF41	8	0555	STD261	4	0617	18B03	2	0679	ØØE05	5	0741	24J15	10
0060	BCTRØ9Ø	5	0122	ENMAAØA	9	0184	LMAØ8Ø	12	0246	MAR 111	15	0308	MDSØ1Ø	16	0370	MDS 311	16	0432	PSW111	9	0494	SØØ1A	13	0556	STD271	4	0618	25AN0	2	0680	Ø5H08	5	0742	19H03	10
0061	BCTR1ØØ	5	0123	EALI	9	0185	LMAØ9Ø	12	0247	MAR121	15	0309	MDSØ2Ø	16	0371	MPAØ81	10	0433	PMEM1	9	0495	SØ11A	13	0557	STD281	4	0619	18A12	2	0681	12DØ3	5	0743	24J13	10
0062	BCTR11Ø	5	0124	ENRPAO	9	0186	LMA1ØØ	12	0248	MAR131	15	0310	MDSØ3Ø	16	0372	MPAØ91	10	0434	PSW211	9	0496	SØ21A	13	0558	STD291	4	0620	19BØ6	2	0682	Ø1E06	5	0744	24J11	10

NOTES

BRUNING 44-131-405-5

REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
J.BIELSKIE		DES/DFT	5-16-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C

TASK 03976 SHT 24-25
DWG 35-769 D08

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0745	24J10	10	0807	16A06	13	0869	05F07	20	0931	GND		0993	CLRAO	11	1055			1117			1179			1241			1303			1365			1427		
0746	24J09	10	0808	16A07	13	0870	05F09	20	0932	GND		0994	MATRSRO	9	1056			1118			1180			1242			1304			1366			1428		
0747			0809	16A08	13	0871	05F12	20	0933	GND		0995	11D08	9	1057			1119			1181			1243			1305			1367			1429		
0748	16D08	11	0810	16A09	13	0872	05J04	20	0934	GND		0996	DENCLK0	15	1058			1120			1182			1244			1306			1368			1430		
0749	03B12	11	0811	16A10	13	0873	05J07	20	0935	GND		0997	21J11	10	1059			1121			1183			1245			1307			1369			1431		
0750	19F04	11	0812	16A11	13	0874	05J09	20	0936	GND		0998	13D13	11	1060			1122			1184			1246			1308			1370			1432		
0751	19F10	11	0813	16A12	13	0875	05J12	20	0937	GND		0999	CAGDIRO	14	1061			1123			1185			1247			1309			1371			1433		
0752	19F13	11	0814	16A13	13	0876	08C12	20	0938	GND		1000	SPA081	16	1062			1124			1186			1248			1310			1372			1434		
0753	04B08	11	0815	16A14	13	0877	03C11	20	0939	GND		1001	SPA091	16	1063			1125			1187			1249			1311			1373			1435		
0754			0816	16A66	13	0878	09J06	20	0940	GND		1002	SPA101	16	1064			1126			1188			1250			1312			1374			1436		
0755	04B11	11	0817	06B08	15	0879	05H03	20	0941	GND		1003	SPA111	16	1065			1127			1189			1251			1313			1375			1437		
0756	04B06	11	0818	06C11	15	0880	08F17	20	0942	GND		1004	SPA121	16	1066			1128			1190			1252			1314			1376			1438		
0757	04B03	11	0819	06B12	15	0881	08F15	20	0943	GND		1005	SPA131	16	1067			1129			1191			1253			1315			1377			1439		
0758	00B03	11	0820	09E06	15	0882	08J17	20	0944	GND		1006	SPA141	16	1068			1130			1192			1254			1316			1378			1440		
0759	00B06	11	0821	13D10	15	0883	08J15	20	0945	GND		1007	SPA151	16	1069			1131			1193			1255			1317			1379			1441		
0760	00B08	11	0822	13C11	15	0884	08C13	20	0946	GND		1008	GND		1070			1132			1194			1256			1318			1380			1442		
0761	06C10	11	0823	09D06	15	0885	06C11	20	0947	GND		1009	GND		1071			1133			1195			1257			1319			1381			1443		
0762	02C09	11	0824	05H06	15	0886	07C11	20	0948	GND		1010	07E17	20	1072			1134			1196			1258			1320			1382			1444		
0763	01B06	11	0825	02B06	15	0887	07C12	20	0949	GND		1011	07E15	20	1073			1135			1197			1259			1321			1383			1445		
0764	01B08	11	0826	09M07	17	0888	07F17	20	0950	GND		1012	00R12	21	1074			1136			1198			1260			1322			1384			1446		
0765	01B03	11	0827	09M09	17	0889	07F15	20	0951	GND		1013	MATRSD0	19	1075			1137			1199			1261			1323			1385			1447		
0766	02B10	11	0828	08M07	17	0890	07J17	20	0952	GND		1014	09D09	19	1076			1138			1200			1262			1324			1386			1448		
0767	04C08	11	0829	08M09	17	0891	07J15	20	0953	GND		1015	11M12	19	1077			1139			1201			1263			1325			1387			1449		
0768	03C06	11	0830	07M07	17	0892	13H11	21	0954	GND		1016	GND		1078			1140			1202			1264			1326			1388			1450		
0769	03C07	11	0831	07M09	17	0893	13H08	21	0955	GND		1017	10K06	11	1079			1141			1203			1265			1327			1389			1451		
0770	03C09	11	0832	06M07	17	0894	13H06	22	0956	GND		1018	10R06	11	1080			1142			1204			1266			1328			1390			1452		
0771	05D08	11	0833	06M09	17	0895	15R03	22	0957	GND		1019	11R12	11	1081			1143			1205			1267			1329			1391			1453		
0772	05D09	11	0834	09K07	17	0896	14H04	22	0958	GND		1020	01C06	11	1082			1144			1206			1268			1330			1392			1454		
0773	22H03	12	0835	09K09	17	0897	13R06	22	0959	GND		1021	MCLK1	3	1083			1145			1207			1269			1331			1393			1455		
0774	22H06	12	0836	08K07	17	0898	13R03	22	0960	GND		1022	ASHRD0	8	1084			1146			1208			1270			1332			1394			1456		
0775	22H08	12	0837	08K09	17	0899	14R08	23	0961	GND		1023	20J06	9	1085			1147			1209			1271			1333			1395			1457		
0776	22H11	12	0838	07K07	17	0900	14R06	23	0962	GND		1024	READ0	11	1086			1148			1210			1272			1334			1396			1458		
0777	21H03	12	0839	07K09	17	0901	LLOCO	23	0963	GND		1025			1087			1149			1211			1273			1335			1397			1459		
0778	21H06	12	0840	06K07	17	0902	20K11	23	0964	GND		1026			1088			1150			1212			1274			1336			1398			1460		
0779	21H08	12	0841	06K09	17	0903	16H11	14	0965	GND		1027			1089			1151			1213			1275			1337			1399			1461		
0780	21H11	12	0842	13H03	15	0904	GND		0966	GND		1028			1090			1152			1214			1276			1338			1400			1462		
0781	24M13	12	0843	04K07	18	0905	GND		0967	GND		1029			1091			1153			1215			1277			1339			1401			1463		
0782	24M11	12	0844	04K09	18	0906	GND		0968	GND		1030			1092			1154			1216			1278			1340			1402			1464		
0783	24M10	12	0845	03K07	18	0907	GND		0969	GND		1031			1093			1155			1217			1279			1341			1403			1465		
0784	24M09	12	0846	03K09	18	0908	GND		0970	GND		1032			1094			1156			1218			1280			1342			1404			1466		
0785	24M17	12	0847	02K07	18	0909	GND		0971	GND		1033			1095			1157			1219			1281			1343			1405			1467		
0786	24M15	12	0848	02K09	18	0910	GND		0972	GND		1034			1096			1158			1220			1282			1344			1406			1468		
0787	19H06	12	0849	01K07	18	0911	GND		0973	GND		1035			1097			1159			1221			1283			1345			1407			1469		
0788	22M17	12	0850	01K09	18	0912	GND		0974	GND		1036			1098			1160			1222			1284			1346			1408			1470		
0789	22M15	12	0851	09J11	18	0913	GND		0975	GND		1037			1099			1161			1223			1285			1347			1409			1471		
0790	22M13	12	0852	04M07	19	0914	GND		0976	GND		1038			1100			1162			1224			1286			1348			1410			1472		
0791	22M11	12	0853	04M09	19	0915	GND		0977	GND		1039			1101			1163			1225			1287			1349			1411			1473		
0792	22M10	12	0854	03M07	19	0916	GND		0978	GND		1040			1102			1164			1226			1288			1350			1412			1474		
0793	22M09	12	0855	03M09	19	0917	GND		0979			1041			1103			1165			1227			1289			1351			1413			1475		
0794	20H06	12	0856	02M07	19	0918	GND		0980	GND		1042			1104			1166			1228			1290			1352			1414			1476		
0795	25K12	12	0857	02M09	19	0919	GND		0981	GND		1043			1105			1167			1229			1291			1353			1415			1477		
0796	25K11	12	0858	01M07	19	0920	GND		0982	GND		1044			1106			1168			1230			1292			1354			1416			1478		
0797	23K03	12	0859	01M09	19	0921	GND		0983	GND		1045			1107			1169			1231			1293			1355			1417			1479		
0798	23K06	12	0860	09J08	19	0922	GND		0984	GND		1046			1108			1170			1232			1294			1356			1418			1480		
0799	20F04	12	0861	14R04	19	0923	GND		0985	SUM121	20	1047			1109			1171			1233			1295			1357			1419			1481		
0800	15H11	12	0862	18A08	19	0924	GND		0986	SUM141	20	1048			1110			1172			1234			1296			1358			1420			1482		
0801	16A01	13	0863	11R08	19	0925	GND		0987	18B08	2	1049			1111			1173			1235			1297			1359			1421			1483		
0802	16A02	13	0864	11H06	19	0926	GND		0988	GESSTD1	9	1050			1112			1174			1236			1298			1360			1422			1484		
0803	16A03	13	0865	11H03	19	0927	GND		0989	01B11	5	1051			1113			1175			1237			1299			1361			1423			1485		
0804	16A04	13	0866	02H12	20	0928	GND		0990	FMATCY0	9	1052			1114			1176			1238			1300			1362			1424			1486		
0805	16A05	13	0867	04K11	20	0929	GND		0991	JAMSHRD1	19	1053			1115			1177			1239			1301			1363			1425			1487		
0806	13A01	13	0868	05F04	20	0930	GND		0992	JAMDIRT0	19	1054			1116			1178			1240			1302			1364			1426			1488		

NOTES

REVISIONS					
READ0 WAS ADDED TO NET 1024.					
ECJ		4494	M	10-23-80	R01

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .XX ±.02	.X ±.03 ANGLES ±1°
NAME	TITLE	DATE
J. BIELSKIE	DES/DFT	5-17-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C

TASK 03976
DWG 35-769 R01 D08
SHT 25-25

TEST POINTS

T. P.	MNEMONIC	SHT.
TPA	FDA1A (115-6)	5
TPB	BRST1 (114-6)	5
TPC	(113-6)	6
TPD	GND (112-6)	6
TPE	(111-6)	6
TPF	(110-6)	6
TPG	GND (116-6)	5
TPH	(109-6)	6
TPJ	EXOSCØ (108-6)	9
TPK	INHFSØ (107-6)	13
TPM	CLK1D (106-6)	9
TPN	ENEXOØ (105-6)	9

STRAPPING INFO.

FROM	TO	SHT
00A-72	00A-10	5
02A-73	02A-09	6

CABLE CONNECTOR MAP

CONN	TERM. NO.	ROW 2	ROW 1
6	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		
5	24	GND	GND
	23		
	22		
	21		
	20		
	19		
	18		
	17		CWRØ
	16	MDH5AI	ENMAAØ
	15	CAMAØ	PA301
	14	MDREØ	DISEXTØ
	13	LHWRTØ	LWRTØ
	12	PSBCØ	MSBCØ
	11	PMEMI	MFAULTØ
	10	MDLCKØ	MDHCKØ
	09	MDSBØ	MDL5AI
	08		HALTØ
	07	GND	GND
	06	FSCLK1	FSCLKØ
	05	GND	GND
	04	LPSTDØ	LSSTDØ
	03	CLSTAØ	MATSTOPØ
	02	RFAULTØ	MARSTPØ
	01	ILOCØ	IMARØ
	00	GND	GND
4	24	GND	GND
	23		
	22		
	21	GND	GND
	20		
	19		
	18	GND	GND
	17		
	16		
	15	GND	GND
	14		
	13		
	12	GND	GND
	11	S171	S161
	10	S191	S181
	09	GND	GND
	08	S211	S201
	07	S231	S221
	06	GND	GND
	05	S251	S241
	04	S271	S261
	03	GND	GND
	02	S291	S281
	01	S311	S300
	00	GND	GND
3	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		

FOR SPARE GATES LISTING SEE SHEET 8

PART NO.	~~REF DESIGNATION~~	~~SPARE OUTPUT NO.~~

BACK PANEL MAP

CONN	TERM. NO.	ROW 1	ROW 2
2	43	GND	GND
	42	DMA19Ø	DMA15Ø
	41	DMA12Ø	DMA13Ø
	40	DMA1ØØ	DMA11Ø
	39	DMA Ø8Ø	DMA Ø9Ø
	38	DMA Ø6Ø	DMA Ø7Ø
	37	DMA Ø4Ø	DMA Ø5Ø
	36	DMA Ø2Ø	DMA Ø3Ø
	35	DMA ØØØ	DMA Ø1Ø
	34	GND	GND
	33	GND	GND
	32	DMA17Ø	DMX15Ø
	31	DMA16Ø	DMX14Ø
	30	LOADØ	DMX13Ø
	29	ANSØ	DMX12Ø
	28	SOTØ	DMX11Ø
	27	EOTØ	DMX1ØØ
	26	XREQØ	DMX Ø9Ø
	25	QUEØ	DMX Ø8Ø
	24	GND	GND
	23	GND	GND
	22	FAULTØ	TPCØ
	21	DMARSØ	
	20	GND	GND
	19	GND	GND
	18	MDS3ØØ	MDS31Ø
	17	MDS28Ø	MDS29Ø
	16	MDS26Ø	MDS27Ø
	15	MDS24Ø	MDS25Ø
	14	MDS22Ø	MDS23Ø
	13	MDS2ØØ	MDS21Ø
	12	MDS18Ø	MDS19Ø
	11	MDS16Ø	MDS17Ø
	10	GND	GND
	09	GND	GND
	08	MDS14Ø	MDS15Ø
	07	MDS12Ø	MDS13Ø
	06	MDS1ØØ	MDS11Ø
	05	MDS Ø8Ø	MDS Ø9Ø
	04	MDS Ø6Ø	MDS Ø7Ø
	03	MDS Ø4Ø	MDS Ø5Ø
	02	MDS Ø2Ø	MDS Ø3Ø
	01	MDS ØØØ	MDS Ø1Ø
	00	GND	GND

BACK PANEL MAP

ROW 1	ROW 2	TERM. NO.	CONN.
GND	GND	43	
YS21	YS31	42	
YS01	YS11	41	
YD101	YD111	40	
YD081	YD091	39	
IRØ6Ø	IRØ7Ø	38	
IRØ4Ø	IRØ5Ø	37	
IRØ2Ø	IRØ3Ø	36	
IRØØØ	IRØ1Ø	35	
GND	GND	34	
GND	GND	33	
FPPFLTØ	LMRQØ	32	
SERØ	SMBSYØ	31	
DISBØ	DISAØ	30	
GDIRØ	RD271	29	
RD251	RD261	28	
RD24Ø	RD121	27	
RD141	RD131	26	
RD15Ø	RD161	25	
GND	GND	24	
GND	GND	23	
RDØØ1	RD011	22	
RD021	RD031	21	
GND	GND	20	
GND	GND	19	
RD041	RD051	18	
RD301	RD311	17	
RD281	RD291	16	
PSW101	PSW111	15	
PSW261	PSW271	14	
PSW181	MSTOPØ	13	
OPSTOPØ	DSTOPØ	12	
FPPFØ	RSTOPØ	11	
GND	GND	10	
GND	GND	09	
BWRTØ	TRAPØ	08	
SCLRØ	CLFLRØ	07	
SVØ	BCNTØ	06	
TACKØ2Ø	TACKØ3Ø	05	
TACKØØØ	TACKØ1Ø	04	
SYNØ	DAØ	03	
DRØ	CMDØ	02	
SRØ	ADRSØ	01	
GND	GND	00	
GND	GND	43	
D14Ø	D15Ø	42	
D12Ø	D13Ø	41	
D1ØØ	D11Ø	40	
D Ø8Ø	D Ø9Ø	39	
D Ø6Ø	D Ø7Ø	38	
D Ø4Ø	D Ø5Ø	37	
D Ø2Ø	D Ø3Ø	36	
D ØØØ	D Ø1Ø	35	
GND	GND	34	
GND	GND	33	
B1G1	B171	32	
B181	B191	31	
B201	B211	30	
B221	B231	29	
B241	B251	28	
B261	B271	27	
B281	B291	26	
B301	B311	25	
GND	GND	24	
GND	GND	23	
CLK1B	CLK1A	22	
CLK1C	SCLK1	21	
GND	GND	20	
GND	GND	19	
NCEØ	FNCEØ	18	
DUAØ	PSELI	17	
DMAHWØ	LMBSYØ	16	
LERØ	WRTØ	15	
LMA3ØØ	LMA31Ø	14	
LMA28Ø	LMA29Ø	13	
LMA26Ø	LMA27Ø	12	
LMA24Ø	LMA25Ø	11	
GND	GND	10	
GND	GND	09	
LMA22Ø	LMA23Ø	08	
LMA2ØØ	LMA21Ø	07	
LMA18Ø	LMA19Ø	06	
LMA16Ø	LMA17Ø	05	
LMA14Ø	LMA15Ø	04	
LMA12Ø	LMA13Ø	03	
LMA1ØØ	LMA11Ø	02	
LMA Ø8Ø	LMA Ø9Ø	01	
GND	GND	00	

35 770 R08
BOARD REV LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

REVISION	06	02		01	03	01	01	03	04	02	04	02		02	02	01	01	01	01	03
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

USED IN MANUAL; 47-004

BRUNING 44-131 40579

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV VC	6/2/80

CONNL. TOPOL. 15-1 & 221-2 WERE SPEC AS MATRIXD Ø, & MATRSRØ. SHEETS 2,5, 9, 11, 12, 14, 17 & 18 WERE ROØ. IN AREA 69 35-770 WAS SPEC AS ROØ.

D.B.P.	JV	4527	M	10-29-80	R01

RELEASED FOR PRODUCTION

ENG. _____ DATE 11-19-80

AREA N9 35-770 WAS R01. REVISED SHTS 4,5,6 & 20.

JLV	JV	4650	MS	3-26-81	R02

REVISED SHTS 15, 16

HN		4717	R	07-12-81	R03

AREA N9: 35-770 WAS R02. REVISED SHTS 1, 8, 11, 20, 9 & 10

JLV	JV	4772	M	10-1-81	R04

AREA N9, 35-770 WAS R03 REVISED SHTS 1, 8, 9, 10, 11, 19 & 20 SHT 1 ADD TO BACK Panel MAP FPPFLTØ AT CONN 1, ROW 1, PIN 32 & BWRTØ AT CONN 1, ROW 1, PIN 08.

KR	JV	4908	M	12-15-81	R05	X

REV'D SHTS: 1, 2, 4, 5, 7, 8, 9, 11, 12, 14 & 15

JAH	JV	5090	MS	8-23-82	R06	X

UNLESS OTHERWISE SPECIFIED

SCALE:

TOLERANCE:

DIMENSIONS ARE IN INCHES

.XXX ±.005 .X ±.03
.XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
V. PERRI	E JOHNSON	DES/DFT	7-6-80
R. CERO		SUPV	11-19-80
E. GREENSTEIN		SYS. TEST	11-19-80
P BALAS		ENG	11-19-80
D. FRANKENBERGER		MGR	11-19-80
R. BARKER		QC	11-19-80

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE

CPU-D

TASK 03976

DWG 35-770 R06 D08

SHT 1 -20

PERKIN-ELMER

REVISIONS				
IN AREA R4 EFWRT1 WAS CROSS REFERENCED AS 7J7 ONLY				
0889	GU	4527	10/29/80	R01
AREA G-5, 07C 10 DID GO TO GND. ADDED CROSS REF. IN AREA G8				
MH	GU	5070	MS 8-25-82	R02

886 SCLR1 → 24K 19-124 SB → DCLRØ 6A3, 7B2, 7A8

24K 19-124 SB → ACLRØ B7, 9A3, 5B2, 9F7, 8J8

24K 19-124 SB → BCLRØ 9C1, 11J7, 12E5, 13K1

107-1 SCLRØB → 23K 19-057 SG → 24K 19-124 SB → CCLRØ M7, 5F5, 6A7, 10D6, 11L1, 12J6, 5J7

6A6 XREQØ → 14M 19-236 SA → XREQØA 8H4

P5 7I 14K 270

232-1 LMRQØ

DS D 14K Q 19-063 SDF — NC

DS D 14K Q 19-063 SDF — NC

7D2 CLSØ

FMREQ1

6N6 SOTØA

DS J 05C Q 19-064 SF K — FSOT1 7K3, 7E1

5M5 FBRTRDØ → 06B 19-055 SG

FSOTØ 10

7J4, 5J5, 5A3, 5J7

8M5 LOAD1

7G1 CLADAØ

DS D 05E Q 19-063 SDF — FLADR1 5B2, 5B6

FLADRØ 7K4, 8H3

12 06B 19-055 SG 11 — 09 05B 19-236 SA 06

FERDØ 5G6

BRWRTØ 8H2

DS D 05E Q 19-063 SDF

12 05B 19-236 SA 11 — 09 DS D 06D Q 19-063 SDF

XRPØSB F9

12 05A 70 1K P5

FLDARB1 NC

FLDARBØ A8, 7K7

EFWRT1 7J7, 5M7

FEFW1 5G8

FLDARA1 A8

FLDARAØ 7K5, 8H3

FLADR1

4M3 LMBSY1 04

N6 DMASEL1 08

5N8 BRSTI 09

G8 SMBSY1 10

07C 19-241 SN 06

11 08D 19-057 SG 10 HALTI 9B5

HALTØ 4G6, 6H3, 9F7

108-5

13 08D 19-057 SG 12 PSELIA → 217-Ø

DMASEL1 G5, 4J2, 8H4, 10A7, 7J8, 9F8, 5E9

9N6 SCLK1A

DS J 05C Q 19-064 SF K — 07 DMASELØ 1SK2, 4J1, 7K9

14 CCLRØ H2

DS D 06E Q 19-131 SDF CLR

DS D 06C Q 19-131 SDF CLR

NC NC NC NC NC NC NC NC

9L4 AIB11A

9L4 AIB1Ø

G1 ACLRØ

5G7 ERD1

08C 19-126 STTL

FQEOT1 5B4

FQEOTØ 5B7, 7A1

09 05B 19-236 SA 08

4E2 FDUAØ

DMBZY1 9F8

N4 FLDARBØ

M5 FLDARA1

5G6 FERDØ

5G8 FEFWØ

07E 19-058 SG 12

01 06B 19-055 SG 03

02

5L6 FBRTRD1

8H8 EOT1

06B 19-055 SG 06

FDEOT1

DS D 06D Q 19-063 SDF 05

5M8 BRSTI

4M3 LMBSY1 → 07D 19-241 SN 05 → DMALM1 4J7

4E2 FDUA1

FLMRQØ 1SF2

05D 19-235 SDR 03

9N5 FBØ

9F6 FSCLK1

07E 19-058 SG 08 CLSTØ 7A2

DMASM1 4J9

G5, 4J9 SMBSY1

6N8 SOTIA

DS D 09D Q 19-063 SDF 06

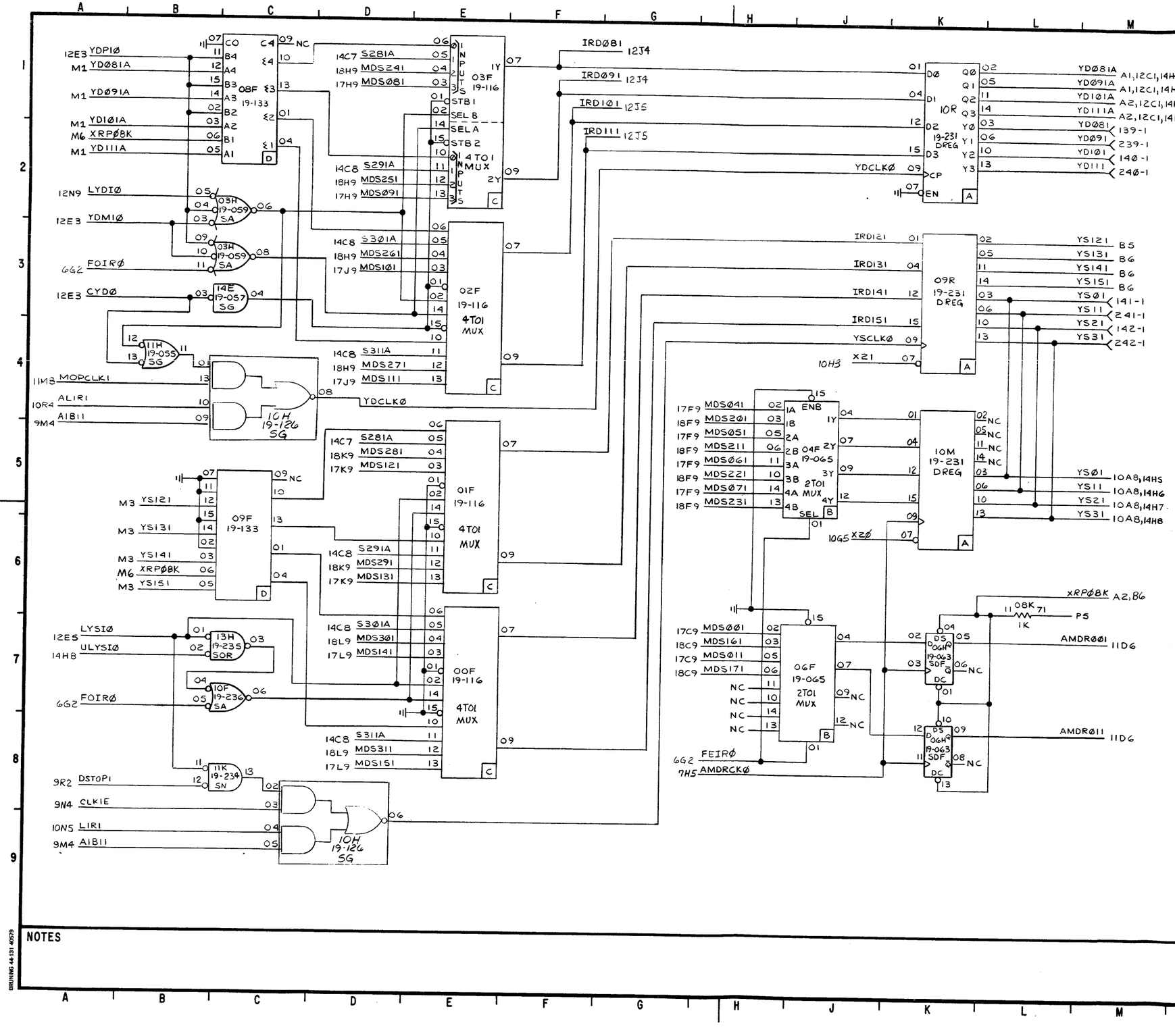
XRPØ5B N4

SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	D STINE	DRAFT	3-29-78
		CHK	
		ENGR	

TITLE CPU-D REFRESH CONTENTION EDMA CONTENTION

TASK NO. 03976 — SHEET OF 2

DWG. NO. 35-770R02D09



REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	E. JOHNSON	DES/DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

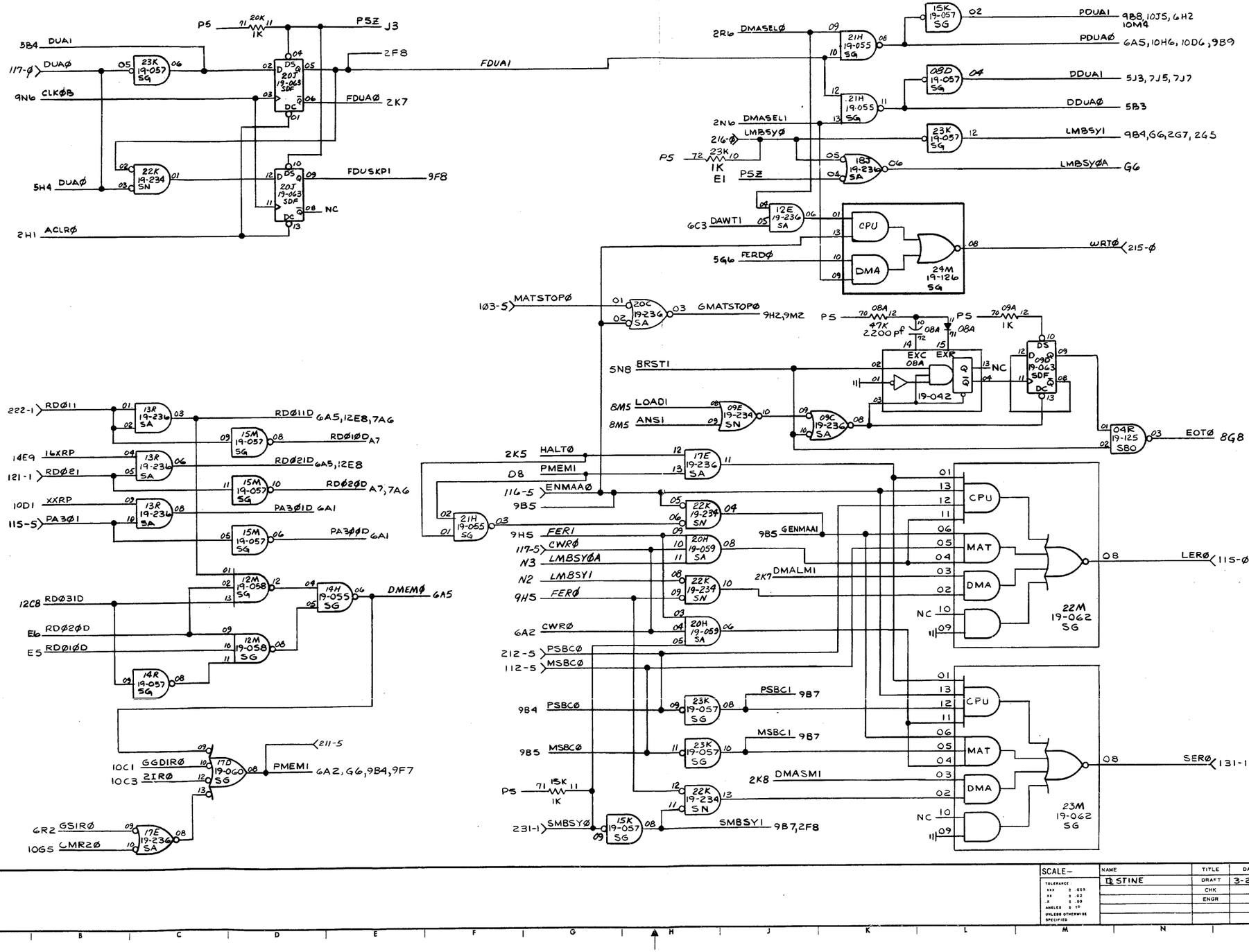
TITLE CPU-D
INSTRUCTION REGISTER YD & YS FIELDS

TASK 03976
DWG 35-770 D08
SHT 3 - 20

NOTES

PERKIN-ELMER

REVISIONS					
AREA J2, ADDED 1K RES. IN LOC. 23K. APLA 81, ADDED 7819					
AH	AJ	5090	MS	8-23-82	R01



SCALE–	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	D STINE	DRAFT	3-29-78
		CHK	
		ENGR	

TITLE CPU-D LOCAL MEMORY TIMING & CONTROL

TASK NO. 03976 SHEET 4 OF 20

DWG. NO. 35-770R01D08

PERKIN ELMER

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA M7 0ED09 WAS DISCONNECTED TO 03D10.				
DJF	AU	4527	10-29-80	R01
AREA D1 ADDED CONN 00A73 TO 00B03.				
JWJ	AU	4650	MS	3-25-81 R02
ADD A J-7, ADDED CROSS REF. CRS TO ERWRT1. ADDED 1.5K 09				
AH	AU	5070	MS	8-23-82 R03

H3 ENAOSCØ

68 PF 73 00A

7S 00A 07 2.2K

P5 74 00A 08 1K

06 00A 76 1K

05 00A 77 4.7uH

80 00A 02 9-35 pf

M6 FBRTRDI 03
M4 FDRDY1 04
EJ4 FLADR1 05

7F2 STI 09

2F5 FSOTØ 12
G6 FERDI 13

R8 BRST1 04
4N2 DDUAØ 09
2G7 FQEOT1 10
4A2 DUAI 11

J7 BRWRT1 01

H2 FDA1 02
H3 FDAØ 01
G7 ERDI 02
K2 FDB1 04
G8 FEFW1 05
G8 FEFWØ 01

9N5 CLK1

P5 71 01A 11 1K 5XRP

F1 DOSCØ 01

ZH2 CCLRØ 10

E4 DOSCØ

FDAAØ 7B1

TPG 116-6
FDA1A TPA 115-6

FDA1 B4, 8B1, 7B1
FDAØ B4, 8B4
FDB1 B4, 8B3
FDC1 8B3
FDCØ 8B2

NC

ENAOSCØ B1, 8H3

MEMORY TO EDMA - CONTROL

4R2 DDUA1 01
9N5 CLKIF 02
L6 FBRTRDI 03
4A1 DUAØ 04
05

XRPØ5 7L2
12 01A 70 1K P5
FDRDY1 B2
FDRDYO
7D1 CLRDYØ

15	16	17	
1	0	0	RD HW
0	1	0	WRT HW
1	1	0	RD FW
1	0	1	WRT FW
0	1	1	BRST RD
1	1	1	BRST WRT

XRPØ5

16J4 RDATIS1

2J4 FLADR1
2G1 ACLRØ

FERD1 8B1, 8H4, A3, 17M1, 7K6

FERDØ 4K4, 7K5, 8H4 2K5, 2A8

2F5 FSOTØ

BRTRD1 8H2, 7B1

BRTRDØ 7E1

FBRTRDØ 2G4, 8H2
FBRTRDI B2, H4, 2B8

2F7 FQEOTØ

P5 70 00K 12 1K

ENB
NC 02 I0 02M I0 03 Z0
NC 05 I1 19-118 Z1 06
NC 11 I2 Z2 10 NC
NC 14 I3 Z3 13 NC
QUAD BUS TRANSCEIVER
B0 B1 B2 B3
01 04 12 15 NC NC

P5 72 01K 10 180
131-2 DMA16Ø
71 01K 11 180
132-2 DMA17Ø
72 02K 10 390
71 02K 11 390

2F4 FSOTØ

BRWRT1 B3, 8H2, 8B4, 8B8

2H2 CCLRØ

15K 04 BWRTØ 108-1

2R5 EFWRT1
8G8 EOT1
FBRWRT1 NC
FBRWRTØ 8H3

BRSTØ 0114-6 TPB
04 BRST1 B3, 2G6, 2B9, 4H5

FEFW1 B5, 2M5, 8B3

FEFWØ B5, 2A8, 7K6, 8A1

EDMA TO MEMORY OPERATION - DECODE

DMAHWØ 116-Ø

08 DMARSØ 121-2

2N6 DMASEL1

SCALE —
TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 10'
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
A. WILLIAMS	DRAFT	2-14-80
	CHK	
	ENGR	

TITLE SCHEMATIC CPU-D EDMA TO LOC. MEM CONTROL

TASK NO. 03976
DWG NO. 35-770R03D0B
SHEET 5 OF 20

PERKIN ELMER

Data Systems Division
Westbury, L.I., N.Y. 11590

REVISIONS					
ADDED CAP 02A CONNECTED TO 03A6E. ADDED CAP 04A CONNECTED TO GND.					
JLV	90	4650	MS	3-26-81	R01

MEMORY OPERATION DECODE

EDMA PROTOCOL LOGIC

NOTES:
1. NORMALLY STRAPPED TO GND.

SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	2-15-80
		CHK	
		ENGR	

TITLE CPU-D
PROC. MEM. OP. DECODE
EDMA PROTOCOL LOGIC

TASK NO. 03976
DWG NO. 35-770.R01 D08
SHEET 6 OF 20

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
AREA B:2: 11A05 DID GO TO LMDR1 (10C, 12N9):
AH 11 5090 mis 8-23-82 R01

5K6 BRTRD∅
5H2 FDA1
5J1 FDAA∅
5J6 BRTRD1
2F7 FQEOT∅
2H1 DCLR∅
2M8 CLST∅
11B 19-058 SG
06E 19-059 SA
12A 19-236 SA
2E4 FSOT1
11A 19-057 SG
CLRDY∅ 5J5
CLS∅ 2A5
CLADA∅ 2G5
ST1 5B3

C6 RMSR1
9C9 STMDR1
09E 19-234 SN
11A 19-057 SG
12B 19-055 SG
MDSB∅ 209-5
MDHSA1 216-5
6G2 FBIR∅
6H9 EVDAT1
6L2 GRD1
6G2 FEIR∅
14B 19-059 SA
MDLSA1 109-5
9L2 DSTOP∅A
6L3 RDFW∅
9L4 AIB11
10A 19-126
MDHCLK∅ 110-5
AMDRCK∅ 3H8
09A 19-058 SG
MDLCK∅ 216-5
6L3 GRD∅
6G2 FEIR∅
12B 19-055 SG

6A2 RD∅∅∅D
4E5 RD∅11D
4E6 RD∅2∅D
12D7 RD∅31D
12E5 DRFALT∅
07C 19-241 SN
RMSR1 A2
READ MAT STATUS REGISTER
(PR2, RFAULT)

XXRP 10D1
10D 19-063 SDF
9R8 MCLK∅
9N6 SCLK1A
2H1 DCLR∅
09C 19-236 SA
CLSTA∅ 203-5
NC

SM3 XRP05
10D7 ENCE1
FENCE1 1SE2
R5 EEDCLK∅
R7 OEDCLK∅
09C 19-236 SA
01H 19-063 SDF
NC

2G4 FSOT1
02B 19-057 SG
LDMAL∅ 16K7,15JG
2F5 FSOT∅
DDUA1
2J5 FLADR∅
05H 19-126 SG
ILDMA∅ 16K7,15JG

5G6 FERD∅
2M5 FLDARA∅
9N4 CLK1D
4R2 DDUA1
5G5 FERD1
05B 19-236 SA
EEDCLK∅ 17M1,K2
07H 19-062 SG
HW WRT
READ
FW WT
5G8 FEFW∅
1589 DL3∅1
4R2 DDUA1
2R5 EFWRT1
2R4 FLDARB∅
OEDCLK∅ 18M1,K2
NC
2R6 DMASEL1
08 19-055 SG
DMAWRT∅ 17M6, 18M6
09A 19-058 SG
LWRT∅ 113-5
10B 19-057 SG
6D4 EDAT1
6D3 DAWT1
2R6 DMASEL∅
LHWRT∅ 213-5

SCALE—	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	
		CHK	
		ENGR	

TITLE CPU-D MEMORY CONTROL LOGIC
TASK NO. 03976
DWG NO. 35-770R01 D08
SHEET OF 7—20

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
DELETED 19-060 19J 06 FROM SPARES TABLE				
JLW	4772	M	10-1-81	R01
DELETED 19-055 19H08 FROM SPARE TABLE.				
KRW	4908	M	12-15-81	R02
AREA B-D 7&8), ADDED 18J & 19H. IN SPARES TABLE DELETED FOLLOWING: 19-055(19H-11), 19-235(21C-6), 19-226(18J-3), 19-057(15K-4), 19-236(14M-6), ADDED B7 CROSS REF. (AREA H-2) TO ENXCVRØ:				
JAH	5090	MS	8-23-82	R03

19-126	24M	6
19-063	23J	5/6
19-241	22H	5
19-165	22A	5/6
19-235	21K	3,6
19-235	21C	8,11
19-063	20E	5/6
19-059	19B	6
19-064	19E	5/6
19-057	18B	,12
19-236	17A	6
19-036	16R	6,8,11
19-022	16K	12
19-064	16B	7/9
19-126	16A	6
19-057	15K	6,12
19-055	15F	6
19-063	15B	5/6
19-063	14F	5/6
19-057	14E	2,6
19-057	14D	12
19-055	13A	8
19-057	12H	4
19-236	12E	3
19-055	12A	3
19-057	11A	2,
19-057	10B	4,6
19-234	09E	13
19-236	09C	11
19-236	09B	11
19-057	08D	2
19-055	05D	8,11
19-125	04E	6
19-069	04C	5/6
19-057	03B	6
19-241	01E	5
19-235	01B	3,6
19-057	01A	10,12
PART NO.	REF DESIGNATION	SPARE OUTPUT NO.

SCALE– | TOLERANCE: XXX ±.005, XX ±.02, X ±.03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
A. WILLIAMS	DRAFT	2-27-80
	CHK	
	ENGR	

TITLE SCHEMATIC CPU-D

TASK NO. 03976 | SHEET OF 8–20

SYS NO. 35-770103D08

P/O DMA PROTOCOL LOGIC

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA N5 MSTOPØA WAS NOT CROSS REFERENCED TO 12B2				
KAW	4527		10/29/80	R01
ADDED 11K1 TO "CLKIE" & "FBØ" AREAS N4 & N5.				
JLM	4772	M	10-15-81	R02
AREA J4 RES 19A WAS 330Ω.				
KAW	4908	M	12-15-81	R03
AREA B,C,D-8 & 9, 16D,10 DID GO TO UMDRI. ADDED 21C & 19M.				
JLM	5090	M	8-23-82	R04

CLOCKSINGLE STEP CONTROL

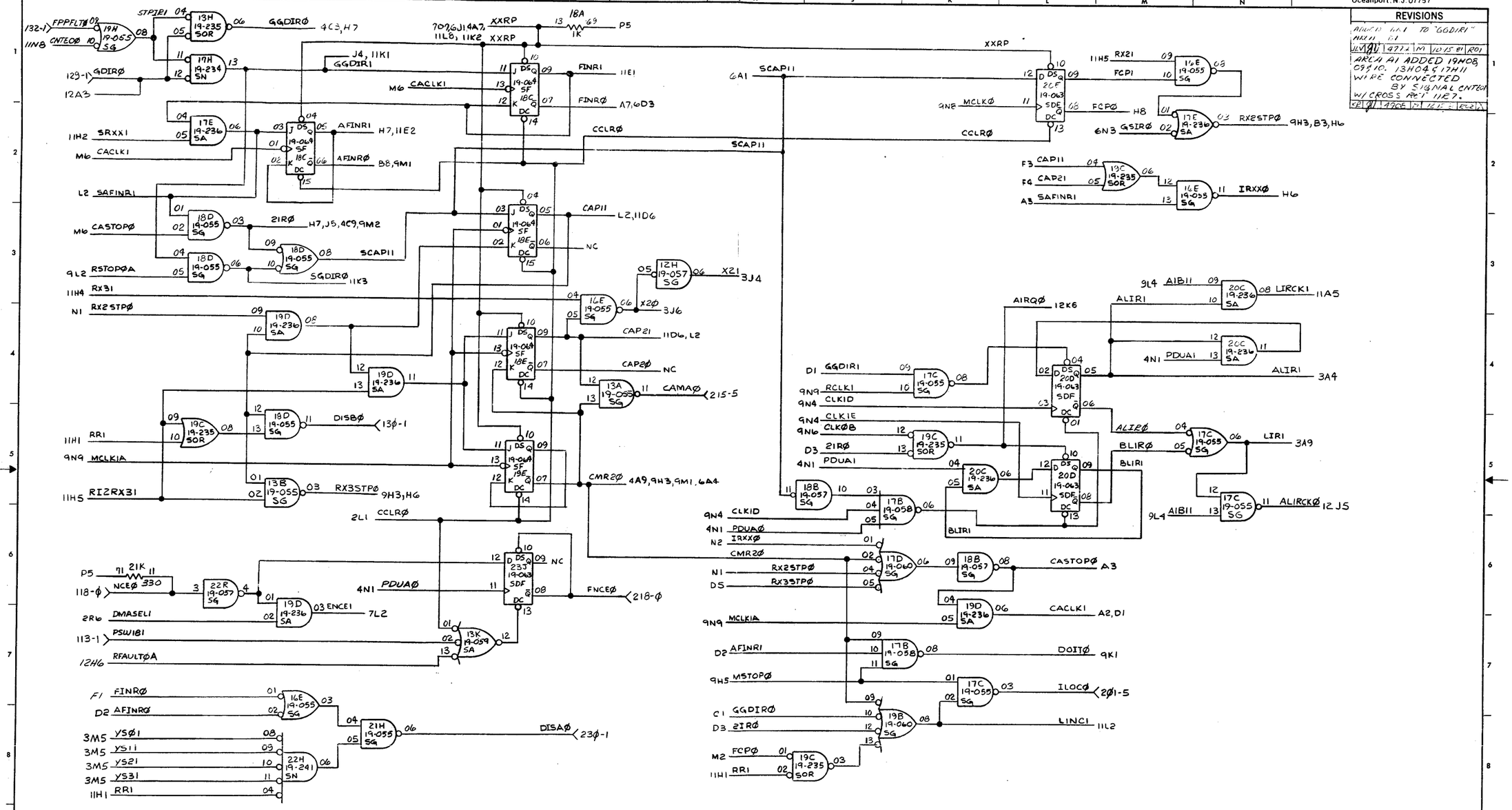
SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	D STINE	DRAFT	
		CHK	
		ENGR	

TITLE CPU-D
CLOCKS & STOPS

TASK NO. 03976 SHEET OF 9-2C
DWG NO. 35-770 REV D08

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS						
ADDED 11A1 TO "GGDIR1" PRINT 11A1						
LTR	DWG	REV	BY	DATE	APPD	
K	4772	M		10/15/81	R01	
ADDED A1 TO 19N08 09 & 10. 13H04 & 17H11 WIRE CONNECTED BY SIGNAL CNTL01 W/ CROSS REF WIE7.						
K	4926	M		12/2/82	R02	



SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	2-15-80
		CHK	
		ENGR	

TITLE CPU-D
CALCULATE ADDRESS LOGIC

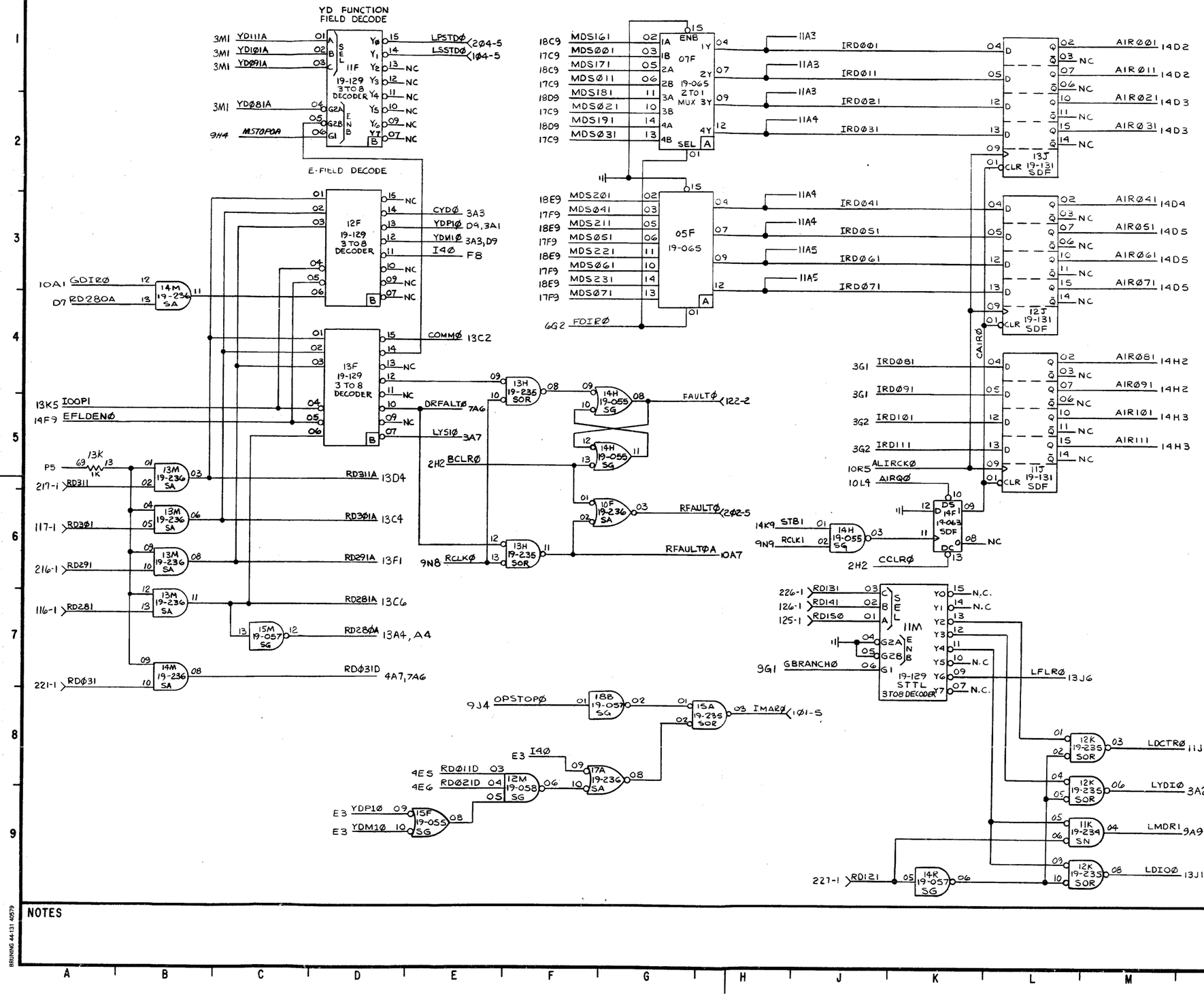
TASK NO. 03976
DWG NO. 35-770 R02D08
SHEET 10 OF 20

PERKIN ELMER

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS						
IN AREA N7 & N5 08S & 08T WERE NOT SPEC.						
NW	9/1	4525			10 23 80	R01
IN AREA K2: 19J01 WAS CCLRD DESTINATION 2LI. ADDED 14J						
NW	9/1	4772	M	10-1-81		R02
AREA N8 18B06 WAS CONNECTED TO 17N11 BY SIGNAL CNTE01 W/ CROSS REF 10A1. AREA N7 ADDED 10A1 TO CNTE0Ø						
KE	9/1	4908	M	12-15-81	E03	X
AREA B7-E3, ICs 08S & 08T WERE 21-099 F02. ICs:						
NW	9/1	5089	VMS	8-20-82	R04	X

SCALE—	NAME	TITLE	DATE	TITLE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	A.WILLIAMS	DRAFT		CPU-D
		CHK		
		ENGR		
				TASK NO. 03976
				DWG. NO. 35-770 RC4D08
				SHEET 11 OF 20



REVISIONS

IN AREA B2 11F06 WAS SPEC AS CONNECTED TO 13M01 AREA A5.				
HAP	GJ	4527	10-29-80	R01
AREA N-9, CROSS REF. ON 'LMDRI' WAS 7A2.				
JAH	GJ	5090	MS	8-23-82 R02 X

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	A. WILLIAMS	DES / DFT	3-4-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC CPU-D
INSTRUCTION REG
DEST. DECODE
SOURCE DECODE

TASK 03976 SHT 12 -20

DWG 35-770 R02 D08

NOTES

PERKIN ELMER

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

I/O CONTROL

I/O DATA

SKIP F/F

CONTROL IN F/F

CONTROL OUT F/F

DATA F/F

SYNC F/F

18M 19-118 QUAD BUS TRANSCEIVER

18R 19-118 QUAD BUS TRANSCEIVER

19M 19-118 QUAD BUS TRANSCEIVER

19R 19-118 QUAD BUS TRANSCEIVER

NOTES:
1. INSTALL JUMPER FROM A TO B IN ORDER TO INSURE A 350 ns MINIMUM WIDTH ON THE ADDRESS CONTROL LINE (ADRS0)

SCALE —	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	E. JOHNSON	DRAFT	
		CHK	
		ENGR	

TITLE CPU-D
I/O CONTROL AND DATA

TASK NO. 03976
DWG NO. 35-770 D08
SHEET OF 13 — 2

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA R5 & R8 055 & 05T WERE NOT SPEC.				
338	9527		10/29/80	R01
A.K.A.: N-L LN-B. IC'S 055 & 05T WERE 21-099 F02 10K.				
411	5090	MS	8-23-82	R02

RD "B" SOURCE DECODE

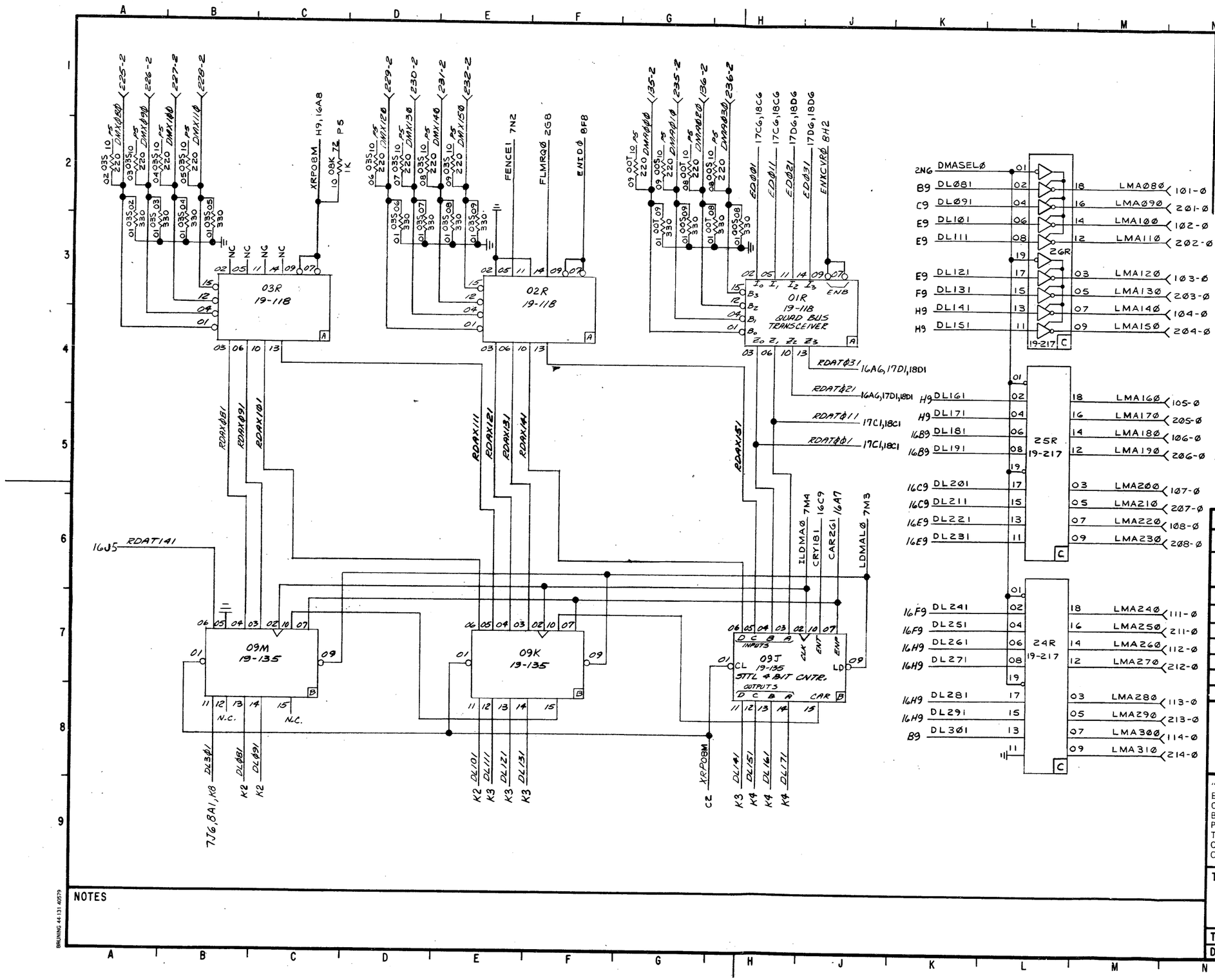
"B" BUS MULTIPLEXORS

STB	B	A	"B" MUX
0	0	0	IO
0	0	1	YDI
0	1	0	LENGTH
0	1	1	YSI
1	X	X	HIZ

SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	E JOHNSON	DRAFT	
		CHK	
		ENGR	

TITLE CPU-D
"S" BUS BUFFERS
"B" BUS DRIVERS
"B" SOURCE DECODE

TASK NO. 03976
DWG NO. 35-770R02D08
SHEET 14 OF 20



REVISIONS

RELABELED RESISTORS AS FOLLOWS: 005, 035, & 007 WERE 007, 037, & 005 RESP					
HN		4717	R	07-13-81	R01
01R07 & 09 AND 02R07 & 09 WERE CONNECTED TO ENXCVR0.					
JAH		5090	MS	8-23-82	R02

NOTES

UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

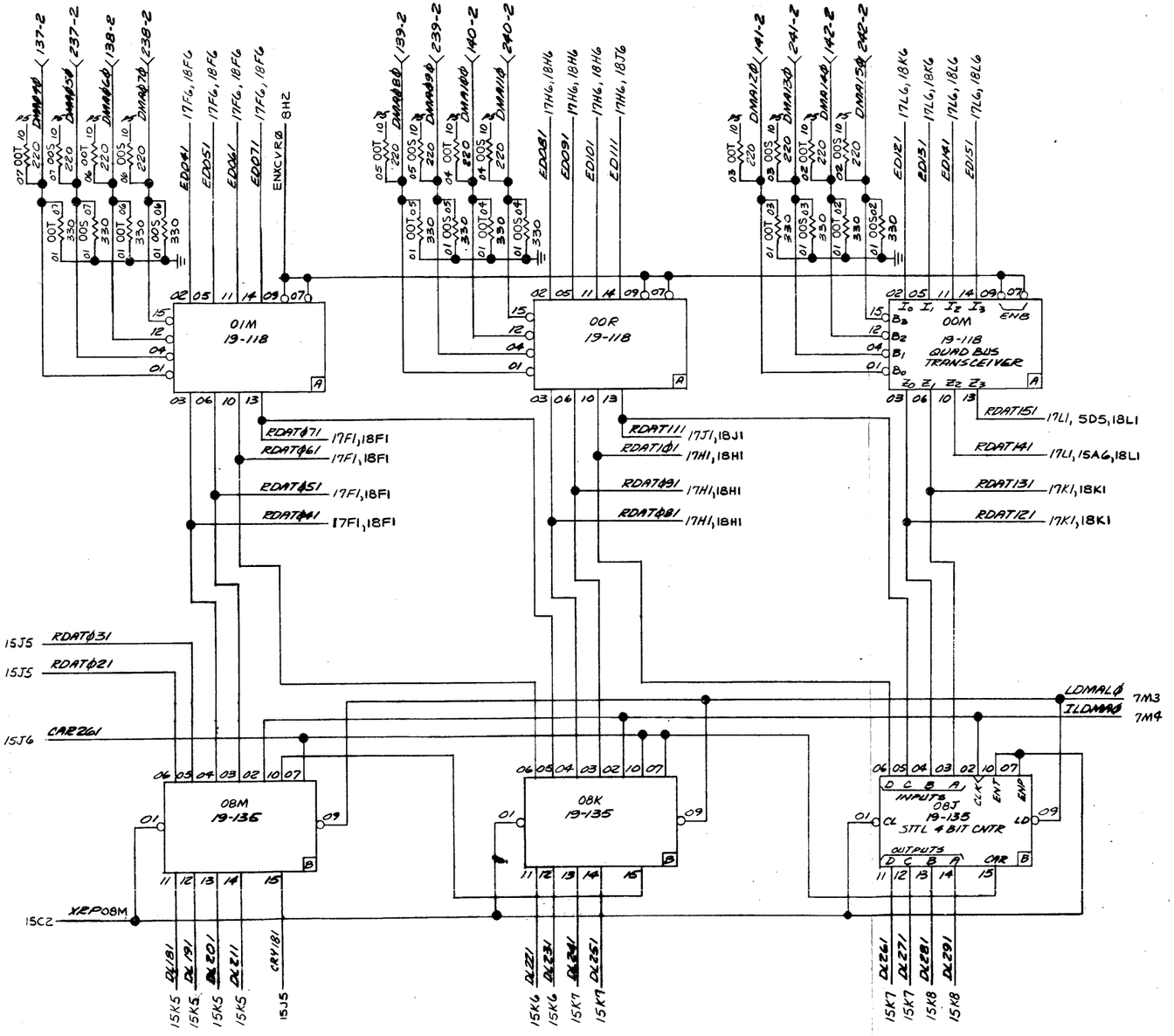
NAME		TITLE	DATE
	E. JOHNSON	DES / DFT	1-14-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
CPU-D
EDMAS DATA XCVRS
EDMAR ADDRESS 08-17

TASK 03976	SHT
DWG 35-770 R02 DO8	15-20

REVISIONS					
RELABELED RESISTORS AS FOLLOWS : 005, 035, 007 WERE 007, 037 & 005 RESP					
HN	MH	4717	R	07-13-81	R01



UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	E. JOHNSON	DES / DFT	1-14-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

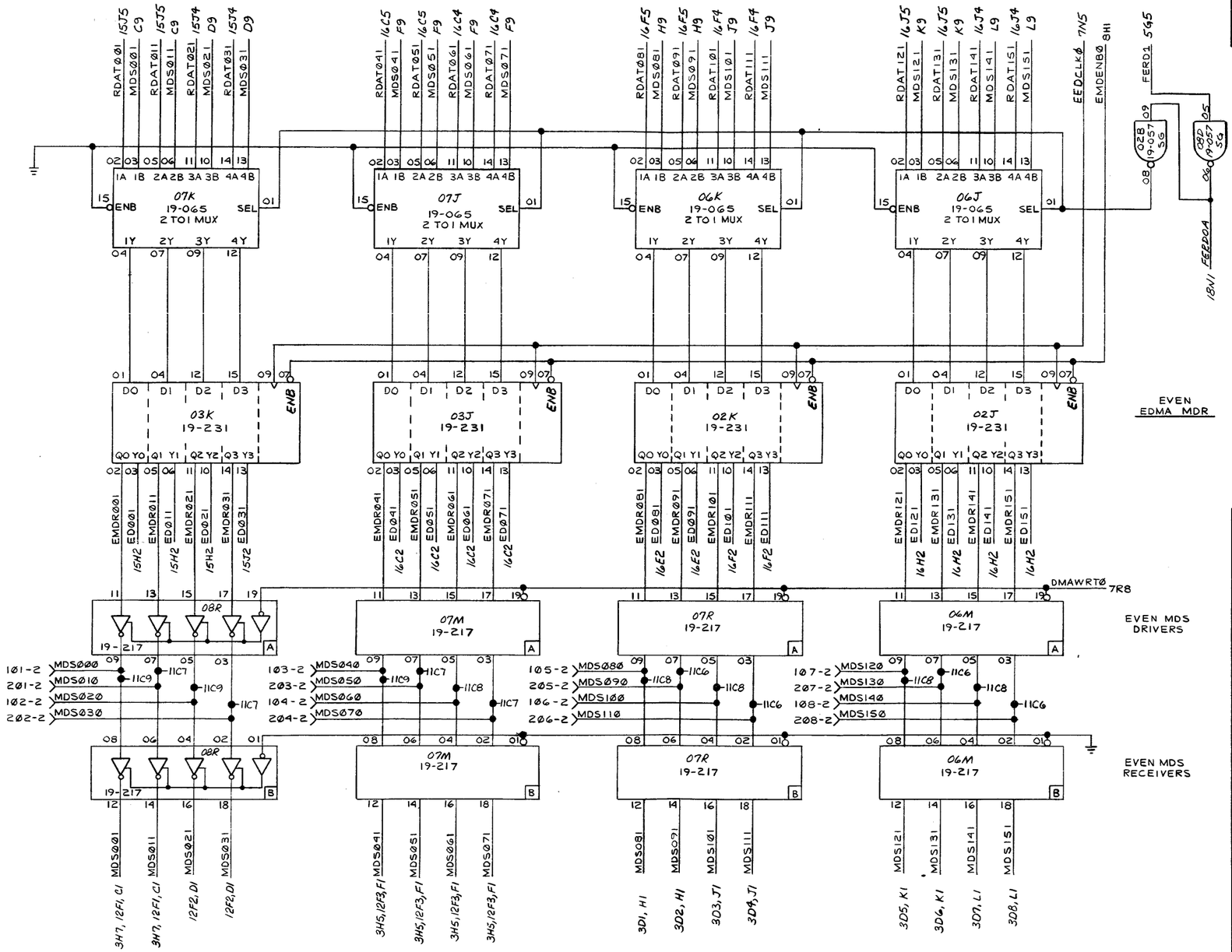
TITLE CPU-D

EDMAS DATA XCVRS
EDMA ADDRESS 18-29

TASK 03976	SHT
DWG 35-770 R01 D08	16-20

NOTES

REVISIONS					
IN AREAS C7, F7, H7 & L7 "MDS" LINES WERE NOT CROSS REFERENCED TO ANY OTHER SHEET.					
LTR	BY	4527		10-29-80	R01



NOTES

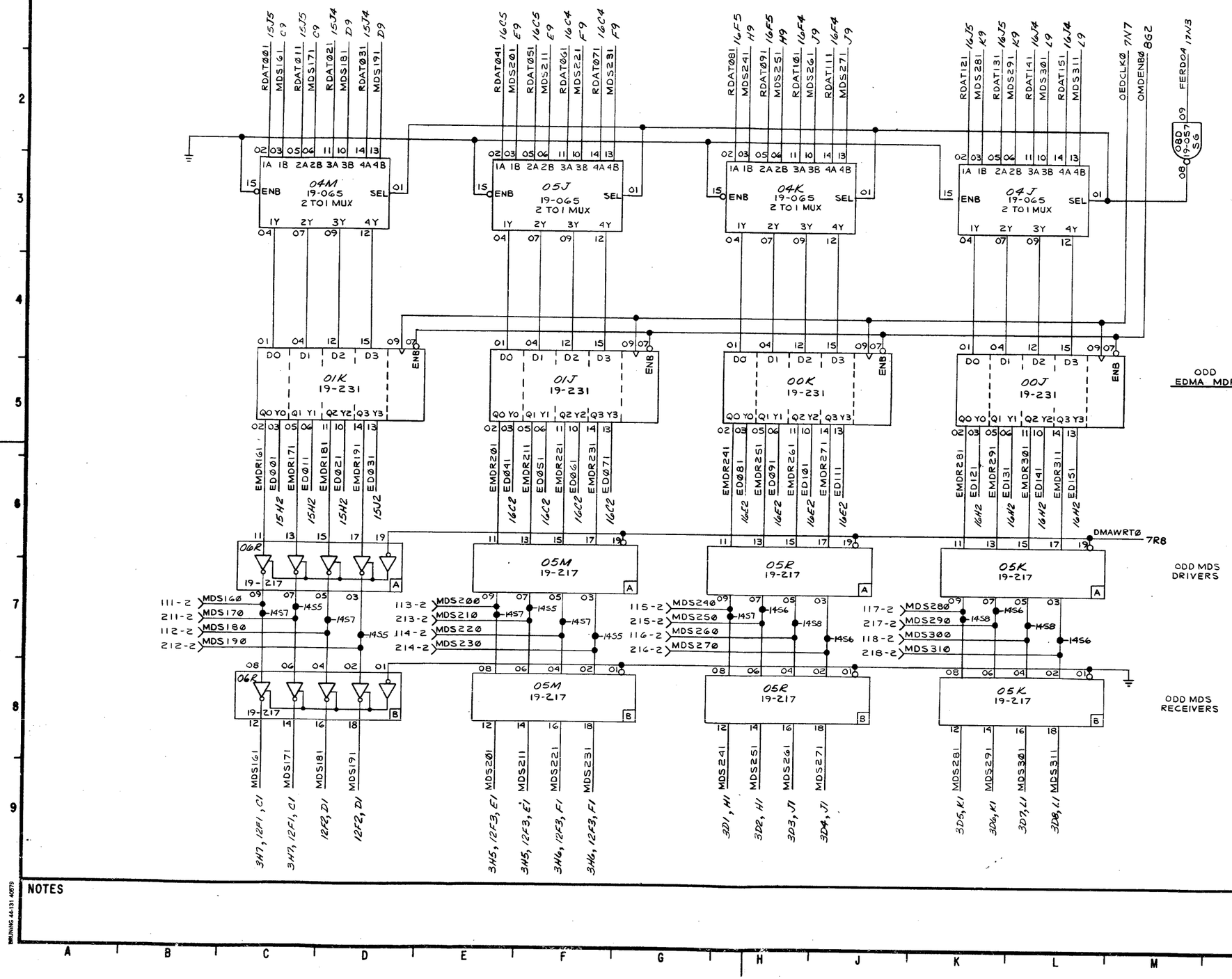
UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	E. JOHNSON	DES / DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-D
EDMA MDR 0/15

TASK 03976 | SHT 17 -20
DWG 35-770 R01 D08



REVISIONS

IN AREAS C7 F7 H7 & L7 "MDS" LINES WERE NOT CROSS REFERENCED TO ANY OTHER SHEET.					
42-P	JJ	4527		10-29-80	R01

NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	E. JOHNSON	DES/DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-D
EDMA MDR 16-31

TASK 03976	SHT
DWG 35-770 R01 D08	18-20

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0001	AIRØØ1	12	0063	CLKIC	9	0125	DL2Ø1	16	0187	EDØ11	15	0249	ENCE1	10	0311	FQEOTØ	2	0373	IOL71	13	0435	MDSØ2Ø	17	0497	MCLKØ	9	0559	RCLK1	9	0621	5311	14	0683	XREQØ	6
0002	AIRØ11	12	0064	CLKID	9	0126	DL211	16	0188	EDØ21	15	0250	FADV1	9	0312	FLADR1	2	0374	IO2Ø1	13	0436	MDSØ3Ø	17	0498	MCLK1A	9	0560	RESCO	8	0622	5161A	14	0684	XREQØA	2
0003	AIRØ21	12	0065	CLKIE	9	0127	DL221	16	0189	EDØ31	15	0251			0313	FLADRØ	2	0375	IO291	13	0437	MDSØ4Ø	17	0499	MSTOPØ	9	0561	RDFWO	6	0623	5171A	14	0685	ZIRØ	10
0004	AIRØ31	12	0066	CLKIF	9	0128	DL231	16	0190	EDØ41	16	0252	FCPØ	10	0314	FDUAØ	4	0376	IO3Ø1	13	0438	MDSØ5Ø	17	0500	MSTOPØA	9	0562	RRØ	6	0624	5181A	14	0686	YDØØ1	3
0005	AIRØ41	12	0067	CLKØ	9	0129	DL241	16	0191	EDØ51	16	0253	FCP1	10	0315	FDUA1	4	0377			0439	MDSØ6Ø	17	0501	MARSTPØ	9	0563	RSTOPØA	9	0625	5191A	14	0687	YDØ91	3
0006	AIRØ51	12	0068	CLKØA	9	0130	DL251	16	0192	EDØ61	16	0254	FDUSKT1	4	0316	FEFWØ	5	0378	ILDMAØ	7	0440	MDSØ7Ø	17	0502	MFAULTØ	9	0564	RX2STPØ	10	0626	5201A	14	0688	YD101	3
0007	AIRØ61	12	0069	CLKØB	9	0131	DL261	16	0193	EDØ71	16	0255	FENCE1	7	0317	FEFWI	5	0379	ILOCØ		0441	MDSØ8Ø	17	0503	MSBC1	4	0565	RX3STPØ	10	0627	5211A	14	0689	YD111	3
0008	AIRØ71	12	0070	CACLK1	10	0132	DL271	16	0194	EDØ81	16	0256			0318	FBØ	9	0380	IRXXØ	10	0442	MDSØ9Ø	17	0504	MSBCØ	4	0566	RSTOPØ	9	0628	5221A	14	0690	YDØØ1A	3
0009	AIR081	12	0071	CASTOPØ	10	0133	DL281	16	0195	EDØ91	16	0257	ST1	5	0319	FSCLK1	9	0381			0443	MDS1ØØ	17	0505	MATSTOPØ	4	0567	RXXSTPØ	11	0629	5231A	14	0691	YDØ91A	3
0010	AIR091	12	0072	CHP11	10	0134	DL291	16	0196	EDI01	16	0258	FTITI		0320	FSCLKØ	9	0382	IOSTOPØ	13	0444	MDS11Ø	17	0506	MDSBØ	7	0568	RR1	11	0630	5241A	14	0692	YD1ØIA	3
0011	AIR1Ø1	12	0073	CAP21	10	0135	DL3Ø1	16	0197	EDI11	16	0259	FWI	6	0321	FOIRØ	6	0383	IMAREØ	12	0445	MDS12Ø	17	0507	MDMSA1	7	0569	RIZO	11	0631	5251A	14	0693	YD111A	3
0012	AIR111	12	0074	CAMAØ	10	0136	DMAØØØ	15	0198	EDI21	16	0260	FERD	9	0322	GBRANCHØ	9	0384	I4O	12	0446	MDS13Ø	17	0508	MDLSA1	7	0570	RX21	11	0632	5261A	14	0694	YSØ1	3
0013	ALIRCKØ	10	0075	CAR2G1	16	0137	DMAØ1Ø	15	0199	EDI31	16	0261	FSIRI	9	0323	GDIRØ	10	0385	LMAØBØ	15	0447	MDS14Ø	17	0509	MREADI	6	0571	RX31	11	0633	5271A	14	0695	YS11	3
0014	ALIQØ	10	0076	CCLRO	2	0138	DMAØ2Ø	15	0200	EDI41	16	0262	FPDI	6	0324	GEOTI	8	0386	LMAØ9Ø	15	0448	MDS15Ø	17	0510	MDHCLKØ	7	0572	RIZRX31	11	0634	5281A	14	0696	YS21	3
0015	ALIRI	10	0077	CLADAØ	7	0139	DMAØ3Ø	15	0201	EDI51	16	0263	FPEI	6	0325	GGDIRØ	10	0387	LMAIØØ	15	0449	MDS16Ø	18	0511	MDLCLKØ	7	0573	RFAULTØA	12	0635	5291A	14	0697	YS31	3
0016	ALIRØ	10	0078	CLSØ	7	0140	DMAØ4Ø	16	0202	EEDCLKØ	7	0264	FPFI	6	0326	GGDIR1	10	0388	LMAI1Ø	15	0450	MDS17Ø	18	0512	MDRBØ	11	0574	RDØØ1	6	0636	53Ø1A	14	0698	YS121	3
0017	AIBIØ	9	0079			0141	DMA05Ø	16	0203	EMDENBØ	8	0265	FPCI	6	0327	GMATSTOPØ	4	0389	LMA12Ø	15	0451	MDS18Ø	18	0513	OEDCLKØ	7	0575	RDØØØD	6	0637	5311A	14	0699	YS131	3
0018	AIBI1A	9	0080	CLRDYO	7	0142	DMAØ6Ø	16	0204	ENXCVRØ	8	0266	FPFØ	6	0328	GRDØ	6	0390	LMAI3Ø	15	0452	MDS19Ø	18	0514	OMDENBØ	8	0576	RDØ11	4	0638	5B291	13	0700	YS141	3
0019	AIBI1	9	0081	CLSTØ	2	0143	DMAØ7Ø	16	0205	EMDEØØ1	17	0267	FPG1	6	0329	GRDI	6	0391	LMAI4Ø	15	0453	MDS2ØØ	18	0515	OSCØ	9	0577	RDØ21	4	0639	5BØ	13	0701	YS151	3
0020	ACLRØ	2	0082	CMRZØ	10	0144	DMAØBØ	16	0206	EMDR011	17	0268	FPGØ	6	0330	GSIRØ	6	0392	LMAI5Ø	15	0454	MDS21Ø	18	0516	OPSTOPØ	9	0578	RDØ1ØD	4	0640	SDFF1	13	0702	YDCLKØ	3
0021	AMDREØ1	3	0083	CNTEØØ	11	0145	DMAØ9Ø	16	0207	EMDR021	17	0269	FBIRI	2	0331	GDATØ	13	0393	LMAI6Ø	15	0455	MDS22Ø	18	0517	NOCNTØ	11	0579	RDØ11D	4	0641	SYNØ	13	0703	YSCLKØ	3
0022	AMDR011	3	0084	STPIR1	10	0146	DMA1ØØ	16	0208	EMDR031	17	0270	FBIRØ	7	0332	HALTØ	2	0394	LMAI7Ø	15	0456	MDS23Ø	18	0518	NCEØ	10	0580	RDØ2ØD	4	0642	SMBSYØ	4	0704	YDTIØ	12
0023	AMDRCKØ	7	0085	COMMØ	12	0147	DMA11Ø	16	0209	EMDR041	17	0271	FDIR1	6	0333	HALTI	2	0395	LMAIBØ	15	0457	MDS24Ø	18	0519	PA3Ø1	4	0581	RDØ21D	4	0643	SMBSY1	4	0705	YDMIØ	12
0024	ANSI	8	0086	COMSTPØ	13	0148	DMA12Ø	16	0210	EMDR051	17	0272	FRD1	6	0334	HOST1	8	0396	LMAI9Ø	15	0458	MDS25Ø	18	0520	PA3ØØD	4	0582	RDØ31D	12	0644	SCLRØB	2	0706	14KØ6	2
0025	ANSØ	8	0087	CRY1B1	15	0149	DMA13Ø	16	0211	EMDREØ6	17	0273	Ø4BØ2	6	0335	IRØØØ	11	0397	LMA2ØØ	15	0459	MDS26Ø	18	0521	PA3Ø1	4	0583	RDØ31	12	0645	SCLR1	2	0707	Ø7E12	2
0026	AFINRØ	10	0088	CYDØ	12	0150	DMA14Ø	16	0212	EMDR071	17	0274			0336	IRØ1Ø	11	0398	LMA21Ø	15	0460	MDS27Ø	18	0522	PSBCØ	4	0584	RDØ41	9	0646	SCLKIA	9	0708	Ø78ØB	2
0027	AFINR1	10	0089	CWRØ	6	0151	DMA15Ø	16	0213	EMDR0B1	17	0275	FMREQ1	2	0337	IRØ2Ø	11	0399	LMA22Ø	15	0461	MDS28Ø	18	0523	PSPC1	4	0585	RDØ51	9	0647	SCLK1	9	0709	Ø6B83	2
0028	AMSTOPØ	9	0090	CMDØ	13	0152	DMX0BØ	15	0214	EMDR091	17	0276	Ø9DØ6	2	0338	IRØ3Ø	11	0400	LMA23Ø	15	0462	MDS29Ø	18	0524	PDUAØ	4	0586	RD121	12	0648	SCAPI1	10	0710	Ø6EØ2	2
0029	ADVØ	9	0091	CAIRØ	12	0153	DMX09Ø	15	0215	EMDR101	17	0277	FLMRQØ	2	0339	IRØ4Ø	11	0401	LMA24Ø	15	0463	MDS3ØØ	18	0525	PDUA1	4	0587	RD131	12	0649	SERØ	4	0711	Ø6E15	2
0030	ASEL1	14	0092	CLFLRØ	13	0154	DMX1ØØ	15	0216	EMDR111	17	0278	FDEOT1	2	0340	IRØ5Ø	11	0402	LMA25Ø	15	0464	MDS31Ø	18	0526	PMEM1	4	0588	RD141	12	0650	SOTØ	6	0712	Ø6C02	2
0031	ADESØ	13	0093	DØØØ	13	0155	DMX11Ø	15	0217	EMDR121	17	0279	FLDARA1	2	0341	IRØ6Ø	11	0403	LMA26Ø	15	0465	MDSØ41	17	0527	PROSC1	6	0589	RD15Ø	12	0651	SOTØA	6	0713	Ø6GØ7	2
0032	B161	14	0094	DØ1Ø	13	0156	DMX12Ø	15	0218	EMDR131	17	0280	FLDARAØ	2	0342	IRØ7Ø	11	0404	LMA27Ø	15	0466	MDSØ11	17	0528	PSELIA	2	0590	RD161	14	0652	SOTIA	6	0714	Ø6G1Ø	2
0033	B171	14	0095	DØ2Ø	13	0157	DMX13Ø	15	0219	EMDR141	17	0281	FEIRØ	6	0343	IRDØØ1	12	0405	LMA28Ø	15	0467	MDSØ21	17	0529	PSZ	4	0591	RD24Ø	14	0653	STDØ	14	0715	Ø6B8Ø	2
0034	B181	14	0096	DØ3Ø	13	0158	DMX14Ø	15	0220	EMDR151	17	0282	FLDARBØ	2	0344	IRDØ11	12	0406	LMA29Ø	15	0468	MDSØ31	17	0530	PSW181	10	0592	RD251	14	0654	STB1	14	0716	Ø6B11	2
0035	B191	14	0097	DØ4Ø	13	0159	DMX15Ø	15	0221	EMDR161	18	0283	FAULTØ	12	0345	IRD021	12	0407	LMA3ØØ	15	0469	MDSØ41	17	0531	PSW271	13	0593	RD261	14	0655	SAFINR1	10	0717	Ø5B06	2
0036	B2Ø1	14	0098	DØ5Ø	13	0160	DMASELØ	2	0222	EMDR171	18	0284	FPTFØ	13	0346	IRDØ31	12	0408	LMA31Ø	15	0470	MDSØ51	17	0532	PSW2G1	13	0594	RD271	14	0656	SGDIRØ	10	0718	Ø8CØB	2
0037	B211	14	0099	DØ6Ø	13	0161	DMASEL1	2	0223	EMDR181	18	0285	FCOMMØ	13	0347	IRD041	12	0409	LOADØ	8	0471	MDSØ61	17	0533	QUEØ	6	0595	RD281	12	0657	SRXX1	11	0719	Ø5B0B	2
0038	B221	14	0100	DØ7Ø	13	0162	DMASM1	2	0224	EMDR191	18	0286	FCOUTØ	13	0348	IRDØ51	12	0410	LOAD1	8	0472	MDSØ71	17	0534	RDATØØ1	15	0596	RD291	12	0658	SBØ	13	0720	Ø6F07	3
0039	B231	14	0101	DØBØ	13	0163	DMALM1	2	0225	EMDR2Ø1	18	0287	FDATØ	13	0349	IRD061	12	0411	LERØ	4	0473	MDSØB1	17	0535	RDAT011	15	0597	RD3Ø1	12	0659	TPCØ	6	0721	Ø6F04	3
0040	B241	14	0102	DØ9Ø	13	0164	DMBEY1	2	0226	EMDR211	18	0288	FSYNØA	13	0350	IRD071	12	0412	LMBSYØA	4	0474	MDSØ91	17	0536	RDATØ21	15	0598	RD311	12	0660	TRAPØ	9	0722	Ø4F04	3
0041	B251	14	0103	DIØØ	13	0165	DSTOP1	9	0227	EMDR221	18	0289	FSYN1	13	0351	IRD0B1	3	0413	LMBSYØ	4	0475	MDS1Ø1	17	0537	RDAT031	15	0599	RD28ØA	12	0661	TACKØØØ	13	0723	Ø4F07	3
0042	B261	14	0104	DI1Ø	13	0166	DSTOPØ	9	0228	EMDR231	18	0290	FNEEØ	10	0352	IRD091	3	0414	LMBSY1	4	0476	MDS111	17	0538	RDATØ41	16	0600	RD281A	12	0662	TACKØ1Ø	13	0724	Ø4F09	3
0043	B271	14	0105	DI2Ø	13	0167	DSTOPØA	9	0229	EMDR241	18	0291	FINRØ	10	0353	IRD1Ø1	3	0415	LMRQØ	2	0477	MDS121	17	0539	RDATØ51	16	0601	RD291	12	0663	TACKØ2Ø	13	0725	Ø4F12	3
0044	B281	14	0106	DI3Ø	13	0168	DOITØ	10	0230	EMDR251	18	0292	FINR1	10	0354	IRD111	3	0416	LYDIØ	12	0478	MDS131	17	0540	RDATØ61	16	0602	RD3Ø1A	12	0664	TACKØ3Ø	13	0726	11K13	3
0045	B291	14	0107	DI4Ø	13	0169	DCLKØ	9	0231			0293	FCINI	13	0355	IRD121	3	0417	LYSIØ	12	0479	MDS141	17	0541	RDATØ71	16	0603	RD311A	12	0665	TPC	6	0727	1ØFØ4	3
0046	B301	14	0108	DI5Ø	13	0170	DAWTI	6	0232			0294	FDAAØ	5	0356	IRD131	3	0418	LIRI	10	0480	MDS151	17	0542	RDATØB1	16	0604	EFAULTØ	12	0666	TPE	6	0728	11H11	3
0047	B311	14	0109	DAØ	13	0171	DMEMØ	4	0233	EMDR261	18	0295	FDAØ	5	0357	IRD141	3	0419	LINC1	10	0481	MDS161	18	0543	RDATØ91	16	0605	RMSR1	7	0667	TPF	6	0729	Ø9FØ4	3
0048	BRWRTØ	8	0110	DRØ	13	0172	DMAWRTØ	7	0234	EMDR271	18	0296	FDA1	5	0358	IRD151	3	0420	LEN2B1	11	0482	MDS171	18	0544	RDAT1Ø1	16	0606	S1G1	14	0668	TPH	6	0730	Ø9FØ1	3
0049	BRWRT1	5	0111	DISAØ	10	0173	DCLRØ	2	0235	EMDR281	18	0297	FDB1	5	0359	INHFSØ	13	0421	LEN291	11	0483	MDS181	18	0545	RDAT111	16	0607	S171	14	0669	ULIØØ	14	0731	Ø9F13	3
0050	BRTRDØ	5	0112	DISBØ	10	0174	DDUAØ	4	0236	EMDR291	18	0298	FDC1	5	0360	IOOP1	13	0422	LEN3Ø1	11	0484	MDS191	18	0546	RDAT121	16	0608	S181	14	0670	ULS1Ø	14	0732	Ø9F1Ø	3
0051	BRTRD1	5	0113	DLØB1	15	0175	DDUA1	4	0237	EMDR3Ø1	18	0299	FDCØ	5	0361			0423	LPSTOØ	12	0485	MDS2Ø1	18	0547	RDAT131	16	0609	S191	14	0671	UMDR1	14	0733	14EØ4	3
0052	BCLRØ	2	0114	DLØ91	15	0176	DUAØ	4	0238	EMDR311	18	0300	FBRTRDØ	5	0362	IO161	13	0424	LSSTOØ	12	0486	MDS211	18	0548	RDAT141	16	0610	S2Ø1	14	0672	WETØ	7	0734	Ø3HØB	3
0053	BCNTØ	13	0115	DL1Ø1	15	0177	DUA1	6	0239			0301	FBRTRD1	5	0363	IO171	13	0425	LDWALØ	7	0487	MDS221	18	0549	RDAT151	16	0611	S211	14	0673	SXRP	5	0735	Ø3HØ6	3
0054	BMSTOPØ	9	0116	DL111	15	0178	DOSCØ	5	0240			0302	FDRDYØ	5	0364	IO181	13	0426	LHWETØ	7	0488	MDS231	18	0550	RDAXØB1	15	0612	S221	14	0674	16XRP	14	0736	ØBF1Ø	3
0055	BRANCHØ	9	0117	DL121	15	0179	DMAHWØ	5	0241			0303	FDRDY1	5	0365	IO191	13	0427	LWRTØ	7	0489	MDS241	18	0551	RDAXØ91	15	0613	S231	14	0675	XRPØ5	5	0737	ØBF13	3
0056	BRSTØ	5	0118	DL131	15	0180	DMARSØ	5	0242			0304	FDAIA	5	0366	IO2Ø1	13	0428	LMDRI	12	0490	MDS251	18	0552	RDAX1Ø1	15	0614	S241	14	0676	XRPØBK	6	0738	ØBF91	3
0057	BRST1	5	0119	DL141	15	0181	DMA16Ø	5	0243			0305	FBRWRTØ	5	0367	IO211	13	0429	LDCTRD	12	0491	MDS261	18	0553	RDAX111	15	0615	S251	14	0677	XRPØBM	16	0739	ØBFØ4	3
0058	BLIRI	10	0120	DL151	15	0182	DMA17Ø	5	0244			0306	FERDØ	5	0368	IO221	13	0430	LFLRE	12	0492	MDS271	18	0554	RDAX121	15	0616	S261	14	0678	XRPSB	2	0740	1ØFØ6	3
0059	BLIRØ	10	0121	DL161	15	0183	DANSI	8	0245	EVDAT1	6	0307	FERD1	5	0369	IO231	13	0431	LIRCK1	10	0493	MDS281	18	0555	RDAX131	15	0617	S271	14	0679	XRP13	13	0741	2ØJ12	4
0060	CLK1	9	0122	DL171	15	0184	DISEXTØ	11	0246			0308	FSOTØ	2	0370	IO241	13	0432	LDIØØ	12	0494	MDS291	18	0556	RDAX141	15	0618	S281	14	0680	X20	3	0742	12M12	4
0061	CLKIA	9	0123	DL181	15	0185	DEFALTØ	12	0247	EXOSC	9	0309	FSOT1	5	0371	IO251	13	0433	MDSØØØ	17	0495	MDS3Ø1	15	0557	RDAX151	15	0619	S291	14	0681	X21	10	0743	12M08	4
0062	CLKIB	9	0124	DL191	16	0186	EDØØ1	15	0248	EDAT1	6	0310	FQEOT1	2	0372	IO261	13	0434	MDSØ1Ø	17	0496	MDS311	15	0558	RCLKØ	9	0620	S3Ø1	14	0682	XXRP	10	0744	12M11	4

NOTES

BRUNING 44-13 "X" "Y"

REVISIONS

NET 84 WAS CMTFØ1, SHT 11.

KR	411	4908	M	12 15:31	R01

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
V. PERRI	BLUSK	DES/DFT	6-10-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-D

EDMA MDR 0/15

TASK 03976	SHT
DWG 35-770 R01 D08	19 - 20

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0745	17EØ8	4	0807	ØZDØ9	6	0869	13EØ8	9	0931	16MØ3	13	0993	ØSJØ9	18	1055	GND	18	1117			1179			1241			1303			1365			1427		
0746	21JØ6	4	0808	ØADØ5	6	0870	16B15	9	0932	16MØ6	13	0994	ØSJ12	18	1056		18	1118			1180			1242			1304			1366			1428		
0747	Ø9E1Ø	4	0809	ØSAØ3	6	0871	13CØ6	9	0933	16M83	13	0995	ØAKØ4	18	1057		18	1119			1181			1243			1305			1367			1429		
0748	17E11	4	0810	ØADØ4	6	0872	19CØ3	10	0934	16M11	13	0996	ØAKØ7	18	1058		18	1120			1182			1244			1306			1368			1430		
0749	2BHØ8	4	0811	ØSAØ8	6	0873	19CØ6	10	0935	13KØ6	13	0997	ØAKØ9	18	1059		4	1121			1183			1245			1307			1369			1431		
0750	22K10	4	0812	ØSH11	6	0874	16EØ8	10	0936	15JØ5	13	0998	ØAK12	18	1060		13	1122			1184			1246			1308			1370			1432		
0751	2BHØ6	4	0813	Ø1DØ6	6	0875	20C11	10	0937	15J02	13	0999	ØAJØ4	18	1061		13	1123			1185			1247			1309			1371			1433		
0752	22K13	4	0814	Ø3BØ9	6	0876	17KØ8	10	0938	18H12	13	1000	ØAJØ7	18	1062		13	1124			1186			1248			1310			1372			1434		
0753	Ø9CØ8	4	0815	Ø3A11	6	0877	17BØ6	10	0939	16HØ6	13	1001	ØAJØ9	18	1063		13	1125			1187			1249			1311			1373			1435		
0754	ØBA04	4	0816	Ø2A77	6	0878			0940	18J11	13	1002	ØAJ12	18	1064		13	1126			1188			1250			1312			1374			1436		
0755	Ø9DØ8	4	0817	Ø3AØ8	6	0879	2BCØ6	10	0941	18HØ6	13	1003	ØAJØ1	18	1065		13	1127			1189			1251			1313			1375			1437		
0756	Ø9DØ9	4	0818	Ø3A1Ø	6	0880	17DØ6	10	0942	17HØ4	13	1004			1066		2	1128			1190			1252			1314			1376			1438		
0757	Ø9D1Ø	4	0819	Ø4HØ8	6	0881	17BØ3	10	0943	17KØ6	13	1005			1067		2	1129			1191			1253			1315			1377			1439		
0758	ØBA14	4	0820	Ø4H12	6	0882	16EØ3	10	0944	16K13	13	1006			1068		2	1130			1192			1254			1316			1378			1440		
0759	ØBA15	4	0821	11C15	6	0883	22HØ6	10	0945	16H12	13	1007			1069		7	1131			1193			1255			1317			1379			1441		
0760	ØBA1Ø	4	0822	Ø3AØ6	6	0884	22RØ4	10	0946	15J09	13	1008			1070		3	1132			1194			1256			1318			1380			1442		
0761	Ø2M09	5	0823	Ø4BØ8	6	0885	19E12	10	0947	17K11	13	1009			1071		3	1133			1195			1257			1319			1381			1443		
0762	Ø1A4B	5	0824	Ø3AØ3	6	0886	19D11	10	0948	17KØ3	13	1010	Ø9CØ6	7	1072		3	1134			1196			1258			1320			1382			1444		
0763	ØØBØ2	5	0825	Ø4AØ5	6	0887	19CØ8	10	0949	17JØ5	13	1011	11FØ6	12	1073		3	1135			1197			1259			1321			1383			1445		
0764	ØØBØ3	5	0826	Ø3AØ5	6	0888	19DØ8	10	0950	16K15	13	1012	13K12	10	1074		3	1136			1198			1260			1322			1384			1446		
0765	ØØB12	5	0827	12B11	7	0889	16KØ2	11	0951	16K14	13	1013	13AØ5	9	1075		3	1137			1199			1261			1323			1385			1447		
0766	Ø1B13	5	0828	11B12	7	0890	16KØ5	11	0952	15H04	13	1014	13AØ1	9	1076		4	1138			1200			1262			1324			1386			1448		
0767	ØØA77	5	0829	11B04	7	0891	16KØ6	11	0953	18H03	13	1015	11A12	7	1077	GND	4	1139			1201			1263			1325			1387			1449		
0768	ØØB11	5	0830			0892	16KØ9	11	0954	16JØ6	13	1016	15FØ8	12	1078			1140			1202			1264			1326			1388			1450		
0769	ØØD06	5	0831	11B06	7	0893	16K12	11	0955	14R04	13	1017	15K1Ø	13	1079	GND	5	1141			1203			1265			1327			1389			1451		
0770	Ø2DØ8	5	0832	11A06	7	0894	16K15	11	0956	14R02	13	1018	12K11	13	1080	GND	5	1142			1204			1266			1328			1390			1452		
0771	Ø1D11	5	0833	12B08	7	0895	16K16	11	0957	18MØ6	13	1019	GND	6	1081	GND	5	1143			1205			1267			1329			1391			1453		
0772	Ø1E06	5	0834	12A06	7	0896	16K19	11	0958			1020		7	1082	EFWRTI		1144			1206			1268			1330			1392			1454		
0773	Ø2D03	5	0835	11B08	7	0897	Ø9E04	11	0959			1021		8	1083	ERDI		1145			1207			1269			1331			1393			1455		
0774	ØØH06	5	0836	Ø5B03	7	0898	Ø9H06	11	0960	16JØ9	13	1022		8	1084	EOTI		1146			1208			1270			1332			1394			1456		
0775	ØØD12	5	0837	10B02	7	0899	16KJØ9	11	0961	19A19	14	1023	GND	8	1085			1147			1209			1271			1333			1395			1457		
0776	ØØDØ8	5	0838	Ø7A06	8	0900	12H08	11	0962	11K1Ø	14	1024		8	1086			1148			1210			1272			1334			1396			1458		
0777	Ø1A04	5	0839	Ø7A11	8	0901	Ø7E06	11	0963	13KØ8	14	1025		9	1087	GENMAAI		1149			1211			1273			1335			1397			1459		
0778	Ø1C06	5	0840	Ø7A03	8	0902	12N12	11	0964	14J09	14	1026		9	1088			1150			1212			1274			1336			1398			1460		
0779	Ø1C05	5	0841	Ø7AØ8	8	0903	2BAØ2	11	0965	14J12	14	1027	GND	11	1089	EOTØ		1151			1213			1275			1337			1399			1461		
0780	Ø1D0B	5	0842	Ø2B02	8	0904	2BA04	11	0966	19H03	14	1028		11	1090	ENMAAØ		1152			1214			1276			1338			1400			1462		
0781	ØØ5Ø6	5	0843	06A14	8	0905	2BAØ6	11	0967	Ø9J15	15	1029		11	1091	ENAOSCØ		1153			1215			1277			1339			1401			1463		
0782	Ø1AØ2	5	0844	Ø2CØ5	8	0906	2BAØB	11	0968	Ø9K15	15	1030		11	1092	FERI		1154			1216			1278			1340			1402			1464		
0783	Ø3DØ6	5	0845	ØBBØB	8	0907	2BA1Ø	11	0969	ØBN1Ø	16	1031		11	1093	14H11		1155			1217			1279			1341			1403			1465		
0784	Ø1D03	5	0846	10F10	8	0908	2BA12	11	0970	Ø7KØ4	17	1032		12	1094	EFLDENØ		1156			1218			1280			1342			1404			1466		
0785	Ø3C06	5	0847	10FØB	8	0909	22A09	11	0971	Ø7KØ7	17	1033		12	1095	21H03		1157			1219			1281			1343			1405			1467		
0786	Ø3DØ8	5	0848	Ø9HØ8	8	0910	22A09	11	0972	Ø7KØ9	17	1034		12	1096	FRCØ		1158			1220			1282			1344			1406			1468		
0787	Ø2D06	5	0849	10F11	8	0911	2BBØB	11	0973	Ø7K12	17	1035		12	1097	Ø9BØ8		1159			1221			1283			1345			1407			1469		
0788	Ø3D03	5	0850	10E04	8	0912	2BB12	11	0974	Ø7J04	17	1036		13	1098	12B06		1160			1222			1284			1346			1408			1470		
0789	Ø2MØ3	5	0851	Ø4EØB	8	0913	21B14	11	0975	Ø7JØ7	17	1037		14	1099	CLSTAØ		1161			1223			1285			1347			1409			1471		
0790	Ø2MØ6	5	0852	13A06	9	0914	21B13	11	0976	Ø7JØ9	17	1038		14	1100	10D06		1162			1224			1286			1348			1410			1472		
0791	Ø2D11	5	0853	15B12	9	0915	21B10	11	0977	Ø7J12	17	1039		14	1101	FERDØA		1163			1225			1287			1349			1411			1473		
0792	Ø3H12	5	0854	15BØ7	9	0916	21A14	11	0978	Ø6KØ4	17	1040		14	1102			1164			1226			1288			1350			1412			1474		
0793	Ø2HØB	5	0855	17A11	9	0917	21A13	11	0979	Ø6KØ7	17	1041		14	1103			1165			1227			1289			1351			1413			1475		
0794	Ø2H09	5	0856	13CØ9	9	0918	21A12	11	0980	Ø6K09	17	1042		14	1104			1166			1228			1290			1352			1414			1476		
0795	ØØC07	5	0857	13C10	9	0919	21A11	11	0981	Ø6K12	17	1043		17	1105			1167			1229			1291			1353			1415			1477		
0796	11D06	6	0858	15FØ3	9	0920	13HØB	12	0982	Ø6JØ4	17	1044		17	1106			1168			1230			1292			1354			1416			1478		
0797	11DØB	6	0859	13CØ5	9	0921	14F11	12	0983	Ø6JØ7	17	1045		17	1107			1169			1231			1293			1355			1417			1479		
0798	11E12	6	0860	17A12	9	0922	11M13	12	0984	Ø6J09	17	1046		17	1108			1170			1232			1294			1356			1418			1480		
0799	11D12	6	0861	14A09	9	0923	11M12	12	0985	Ø6J12	17	1047		17	1109			1171			1233			1295			1357			1419			1481		
0800	16B12	6	0862	14A10	9	0924	11M11	12	0986	Ø2BØB	17	1048		17	1110			1172			1234			1296			1358			1420			1482		
0801	16CØ3	6	0863	13B12	9	0925	14RØ6	12	0987	Ø4MØ4	18	1049		17	1111			1173			1235			1297			1359			1421			1483		
0802	16B10	6	0864	15C01	9	0926	11FØ5	12	0988	Ø4MØ7	18	1050		17	1112	GND	5	1174			1236			1298			1360			1422			1484		
0803	Ø9B03	6	0865	15A06	9	0927	13F12	12	0989	Ø4MØ9	18	1051		18	1113	GND	6	1175			1237			1299			1361			1423			1485		
0804	Ø9B06	6	0866	12C08	9	0928	12M06	12	0990	Ø4MI7	18	1052		18	1114	GND	6	1176			1238			1300			1362			1424			1486		
0805	Ø3BØ8	6	0867	16B05	9	0929	21K11	13	0991	Ø5J04	18	1053		18	1115	14J06	11	1177			1239			1301			1363			1425			1487		
0806	Ø4DØB	6	0868	12D05	9	0930	21K12	13	0992	Ø5J07	18	1054		18	1116	FPPFLTØ	10	1178			1240			1302			1364			1426			1488		

NOTES

BRUNING 44-1131 4/5/79

REVISIONS					
ADDED MNEMONICS FOR NEW NETS 1112 THRU 1114.					
JLV	JV	4650	MS	4-21-81	R01
ADDED MNEMONICS FOR NEW NET 1115.					
JLV	JV	4772	M	10-1-81	R02
ADDED NET 1116.					
KR	JV	4908	M	12-15-81	R03

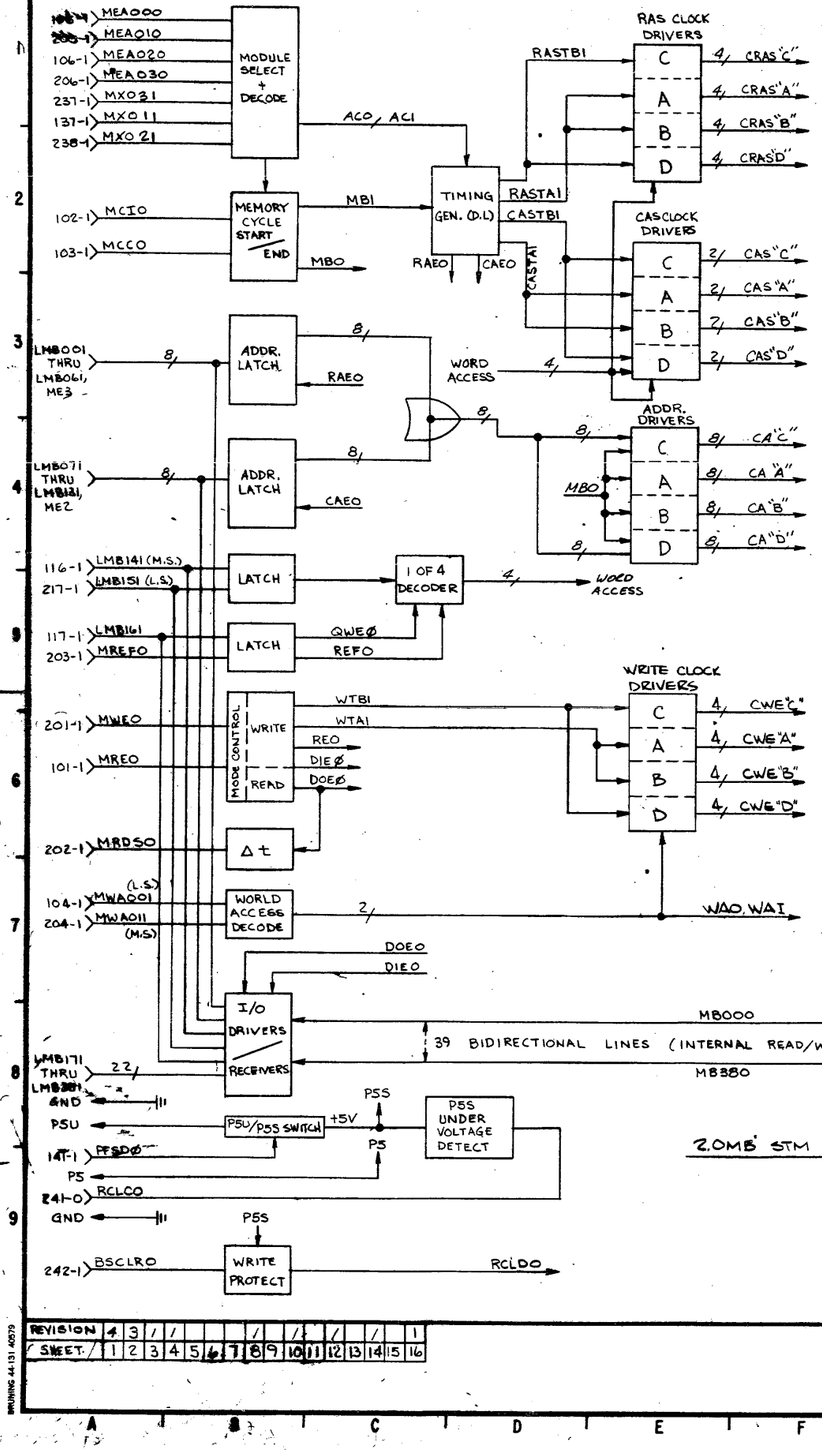
UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
V. PERRI	BLUSK	DES/DFT	6-10-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-D
EDMA MDR 0/15

TASK 03976 SHT
DWG 35-770 R03 D08 20-20



2.0MB STM BLOCK DIAGRAM

TEST POINT		
E4	P5U	SHT 16
E5	P5S	SHT 16

STRAPPING INFORMATION					
STAKE	MNEMONIC	SHT	STAKE	MNEMONIC	SHT
E	—	2	B	—	2
E1	—	2	B1	CCO	2
E2	—	2	B2	GND	2
E3	—	2	C	—	2
			C1	BZERO	2

BACK PANEL MAP		TERM. NO.	CONN.
ROW 1	ROW 2		
GND	GND	43	
PFSDO	BSCLRO	42	
	RCLCO	41	
		40	
		39	
	MX021	38	
MX011	MX031	37	
LMB381	LMB371	36	
LMB361	LMB351	35	
GND	GND	34	
GND	GND	33	
LMB341	LMB331	32	
LMB321	LMB311	31	
LMB301	LMB291	30	
LMB281	LMB271	29	
LMB261	LMB251	28	
LMB241	LMB231	27	
LMB221	LMB211	26	
LMB201	LMB191	25	
GND	GND	24	
		23	
		22	
		21	
		20	
GND	GND	19	
LMB181	LMB171	18	
LMB161	LMB151	17	
LMB141	LMB131	16	
LMB121	LMB111	15	
LMB101	LMB091	14	
LMB081	LMB071	13	
LMB061	LMB051	12	
LMB041	LMB031	11	
GND	GND	10	
GND	GND	09	
LMB021	LMB011	08	
LMB001		07	
MEA020	MEA030	06	
MEA000	MEA010	05	
MWA001	MWA011	04	
MCCO	MREFO	03	
MCIO	MRDSØ	02	
MREO	MWEO	01	
GND	GND	00	

A37			
A25			
A61	19-190	01, 02	
A66	19-240	03	
A48	19-125	08, 11	
A46	19-058	12	
REF.	PT. NO:	SPARE OUTPUT	

USED IN MANUAL 47-004

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

BOARD	REV. LEVEL
35-764 F01	R04
35-764 F02	R04
35-764 F03	R02
35-764-F04	R02

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

REVISION	4	3	1	1											
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

PT. NO.	VARIATION
F01	AS SHOWN, SHTS 1-16, FOR VARIATIONS SEE SHTS. 2,3,8,10 THRU 15
F02	AS SHOWN, SHTS 1-16, 2,3,8,10 THRU 15
F03	AS SHOWN, SHTS 1-16, FOR VARIATIONS SEE SHTS. 2,3,8 THRU 15
F04	AS SHOWN, SHTS 1-16.

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV [illegible]	7/31/81

SEE SHEET 16 FOR REVISION

AREA A9, UPDATED REVISION RECORD AREA K9, F01 & F02 WERE R00

GPS	[illegible]	4499	M	10-8-80	R01

REVISED SHTS 2,3. AREA L,M-364.: DELETED STRAPPING TABLES 2,3.

JAT	[illegible]	4707	E	6-9-81	R02

ADDED A25 & A37 TO TABLE OF SPARES. AREA K9: REVISED REV LEVEL OF PARTS LIST. REVISED SHTS 2,4,8,10,12 & 14.

JAT	[illegible]	4733	M5	6-10-81	R03

RELEASED FOR PRODUCTION

ENG. [illegible] DATE 1-13-82

REVISED SHTS 1&2.

KR	[illegible]	4900	E	12-3-81	R04

UNLESS OTHERWISE SPECIFIED

SCALE: NONE

TOLERANCE: DIMENSIONS ARE IN INCHES .XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
G. SHINN	S. TRIMARCHI	DES/DFT	11-9-79
Z. CERO		SUPV	10-16-81
E. GREENSTEIN		TEST	10-16-81
P. OBRDA		ENG	10-16-81
L. PEZZI/D. FRANK		MGR	10-16-81
R. A. BARKER		QC	10-16-81

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC

STM 2.0MB

TASK 03979	SHT
DWG 35-764 R04D08	1 - 16

BRUNING 44-151 A3579

REVISIONS					
ADDED NOTE 8. AREAS F/M9: REMOVED TABLES 1 & 2. AREA M4 & F5: REMOVED REFS TO TABLES 1 & 2.	JAT	411	4707	E	6-9-81	201
AREA D4: STRAP WAS BETWEEN B1 & B2. ADDED CONN. BETWEEN TP-C & A78-12.	JAT	411	4733	MS	6-10-81	202
AREA G3, M6 E J9, IC'S A62, A47 & A77 WERE 19-249 FXX. ADDED NOTE 9.	KP	411	4900	E	12-3-81	203

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S. TRIMARCHI	DES / DFT	9-21-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

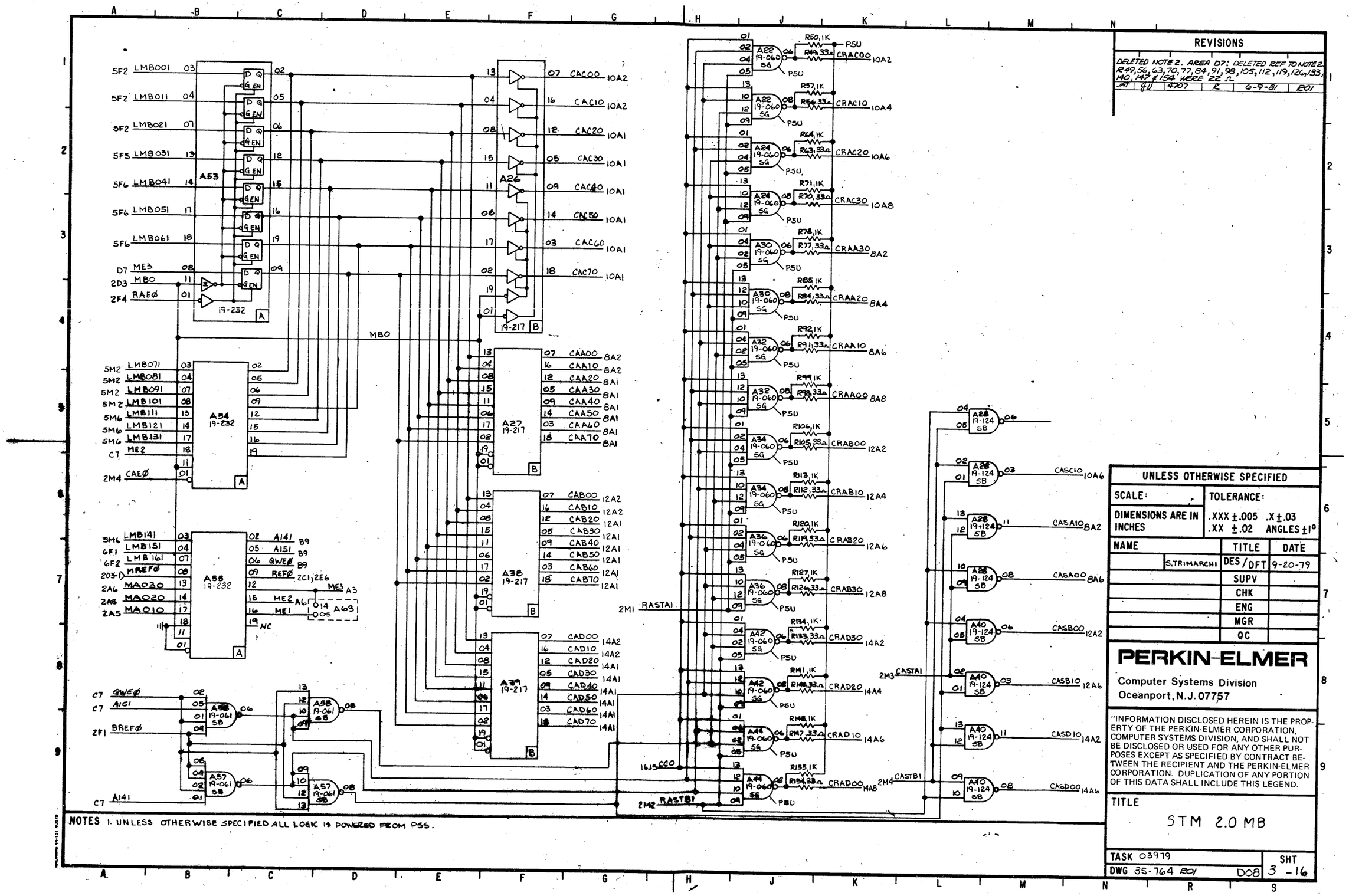
TITLE

STM 2.0 MB

TASK 03979	SHT
DWG 35-764 E03 D08	2 - 16

NOTES,
1. INTERNAL REFRESH OPTION IS AVAILABLE ON F03 AND F04, AND IS ENABLED IN A SPECIAL APPLICATIONS ONLY
   TO ENABLE, CONNECT C-C1, DISCONNECT B-B2 AND CONNECT B-B1
2.
3. SWITCHES ARE SHOWN IN POSITION 0.
4. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED FROM P5S
5.
6. ◉ DENOTES INTERNAL CONNECTION ON IC'S.
7. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE ¼W, 5%
8. FOR STRAPPING INFORMATION AT LOCATION A56 & A63 REFER TO APPROPRIATE MAINTENANCE MANUAL.
9. IC LOCATIONS SHOWN IN PARENTHESIS REPRESENT ALTERNATE USE OF 19-249 FXX.

DRAWING 44-131 40079



NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED FROM P5S.

REVISIONS

DELETED NOTE 2. AREA D7: DELETED REF TO NOTE 2. R49,56,63,70,77,84,91,98,105,112,119,126,133, M0,147 & 154 WERE 22 Ω.					
JAT	911	4707	R	6-9-81	B01

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	9-20-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

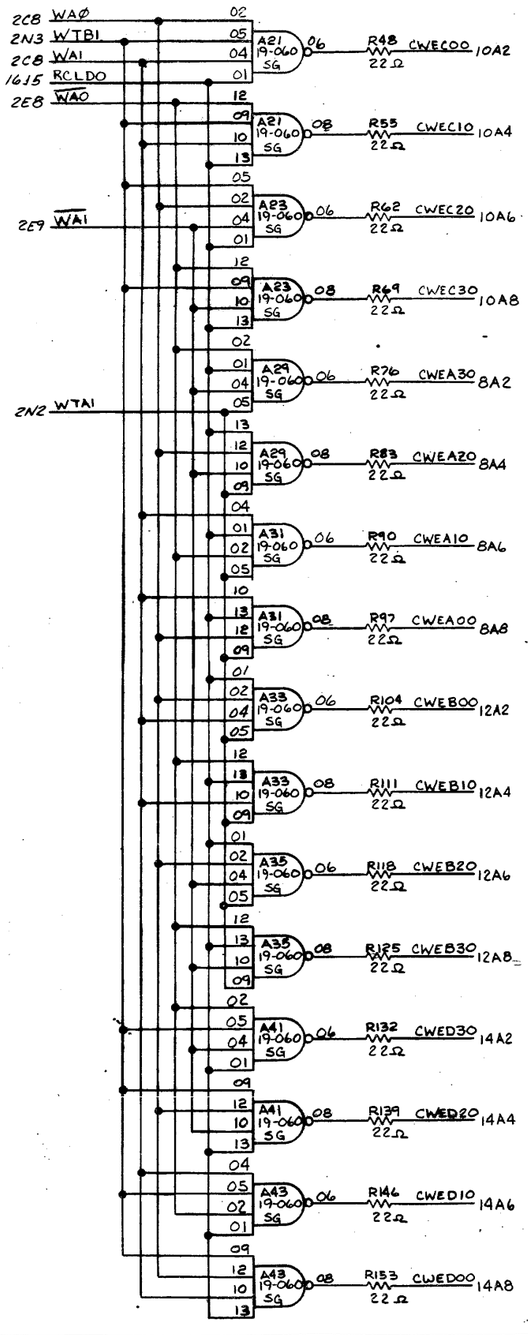
TITLE

STM 2.0 MB

TASK 03979

DWG 35-764 B01 D08

SHT 3 -16



NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED FROM PSS
2.

REVISIONS

APEA G-A: REMOVED A25 & A37.				
JAT	4733	MS	6-10-81	R01

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	9-21-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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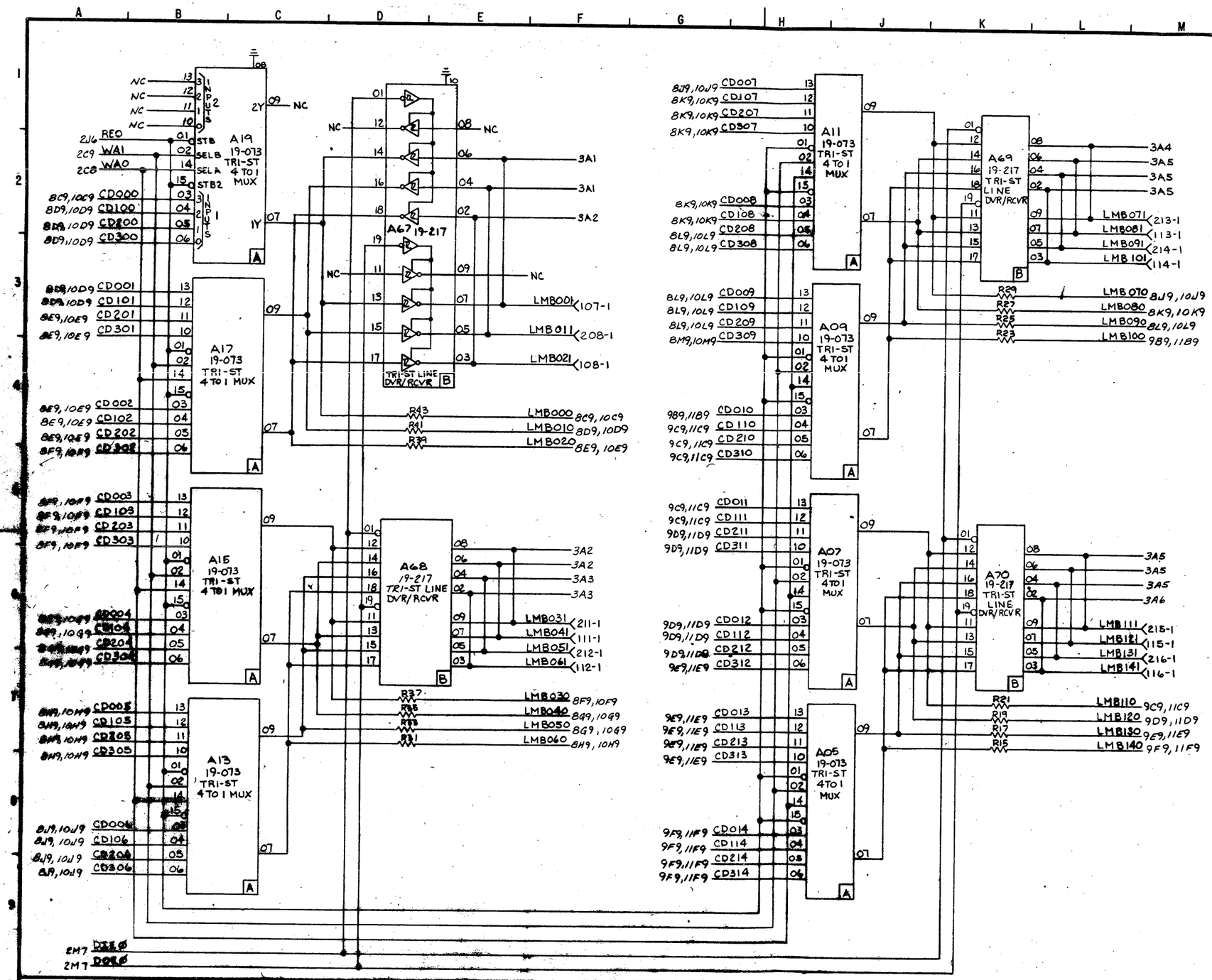
Oceanport, N.J. 07757

TITLE
STM 2.0 MB

TASK 03979	SHT
DWG 35-764 R01 D08	4 - 16



NOTES 1. UNLESS OTHERWISE SPECIFIED:

A) ALL LOGIC POWERED FROM P5
B) ALL RES. ARE 822 1/8 W ±5%

REVISIONS

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
S.TRIMARCHI	DES/DFT	8-17-79
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

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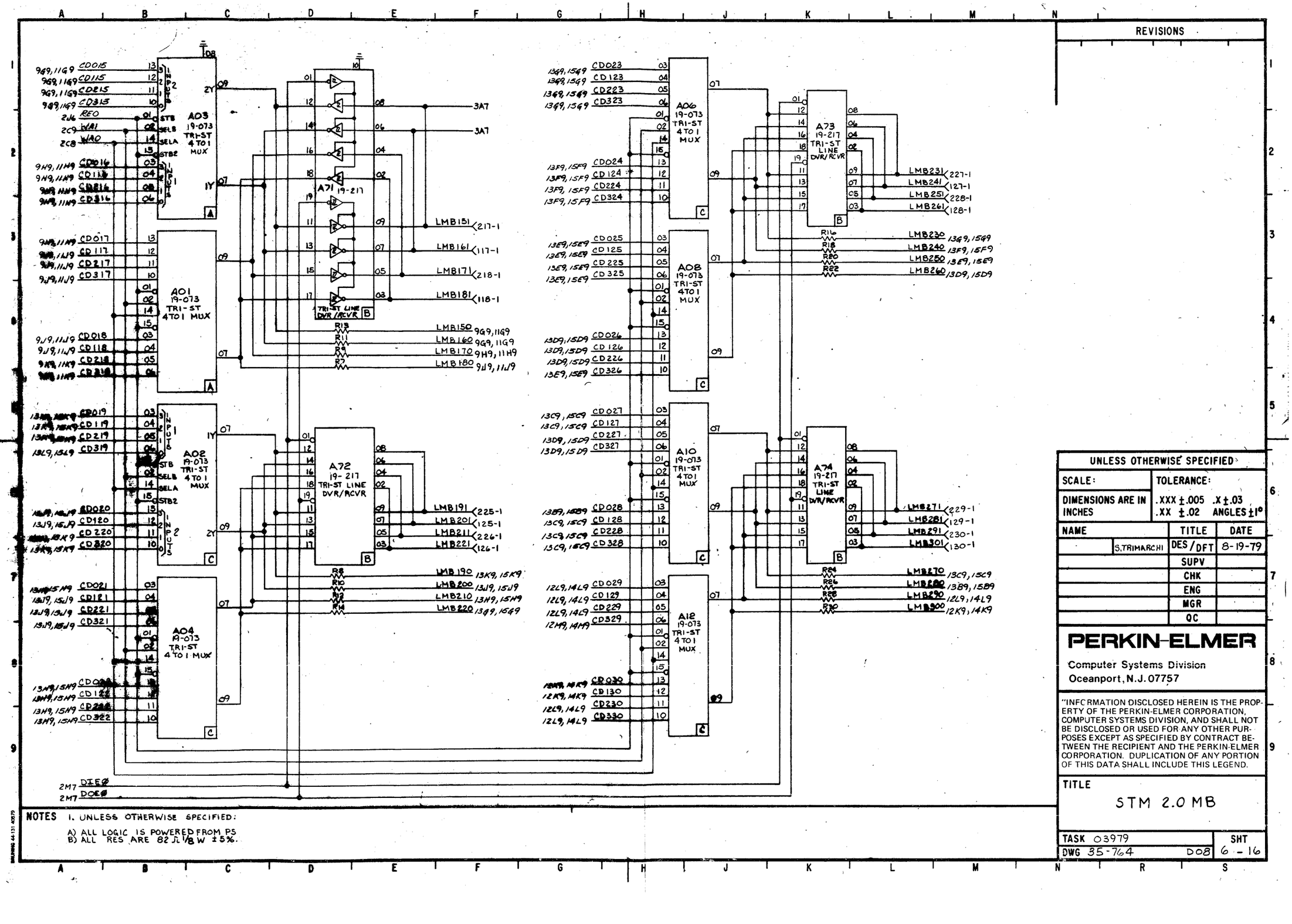
TITLE

STM 2.0MB

TASK 03979 SHT 5 - 16
DWG 35-764 D08



REVISIONS

NOTES 1. UNLESS OTHERWISE SPECIFIED:

A) ALL LOGIC IS POWERED FROM PS
B) ALL RES ARE 82 Ω 1/8 W ±5%.

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	8-19-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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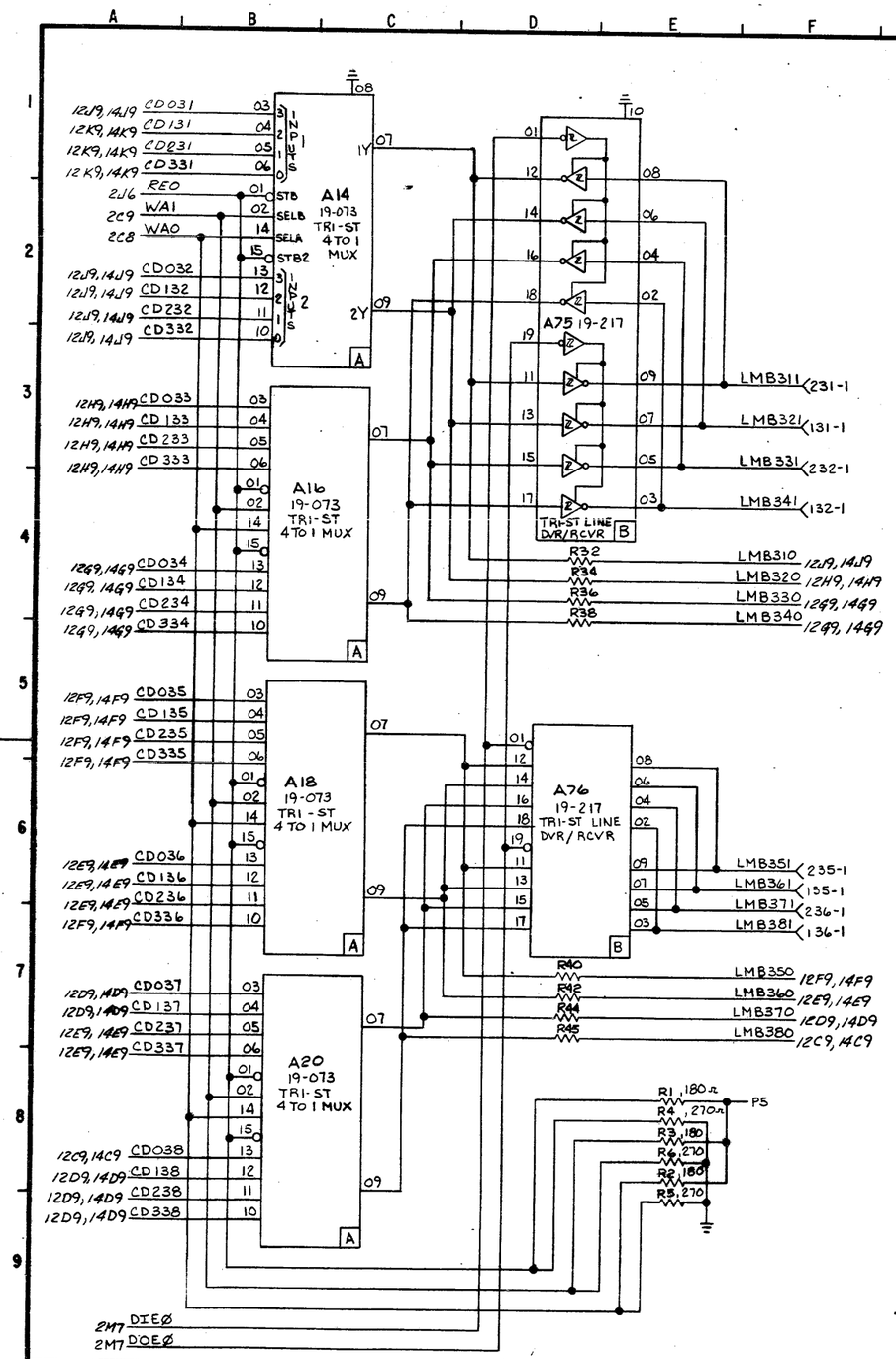
TITLE
STM 2.0 MB

TASK 03979	SHT
DWG 35-764 D08	6 - 16



NOTES 1. UNLESS OTHERWISE SPECIFIED:

A) ALL LOGIC IS POWERED BY P5
B) ALL RES ARE 82Ω, 1/8 W ± 5%.

REVISIONS

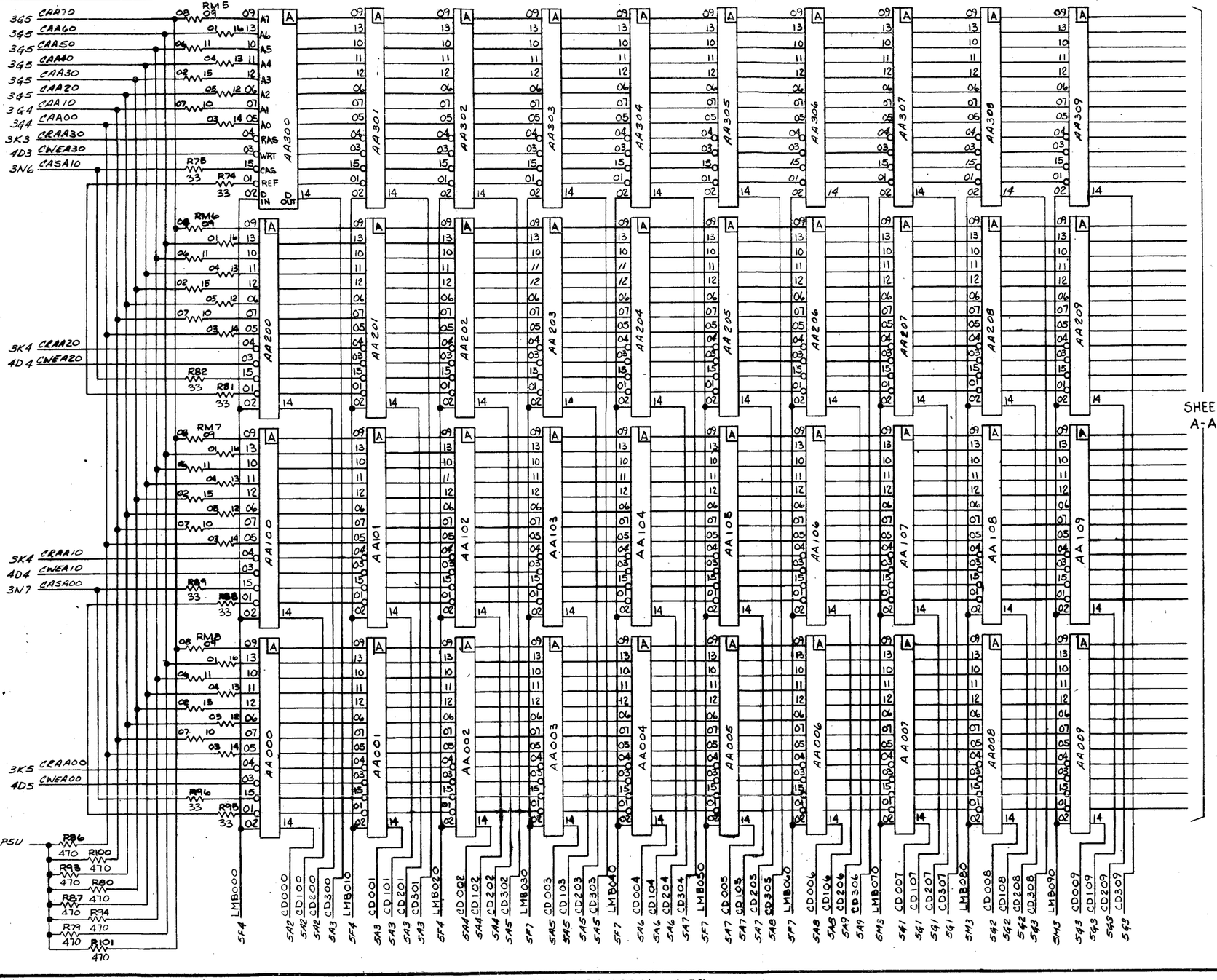
UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES / DFT	8-19-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE

STM 2.0 MB

TASK 03979 | SHT 7 - 16
DWG 35-764 D08



SHEET 9
A-A

REVISIONS					
AREAS A2 & A6. REMOVED CROSS-REF'S TO A2S (PG 4)					
JAT	GJ	4733	MS	6-10-81	R01

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES / DFT	8-13-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

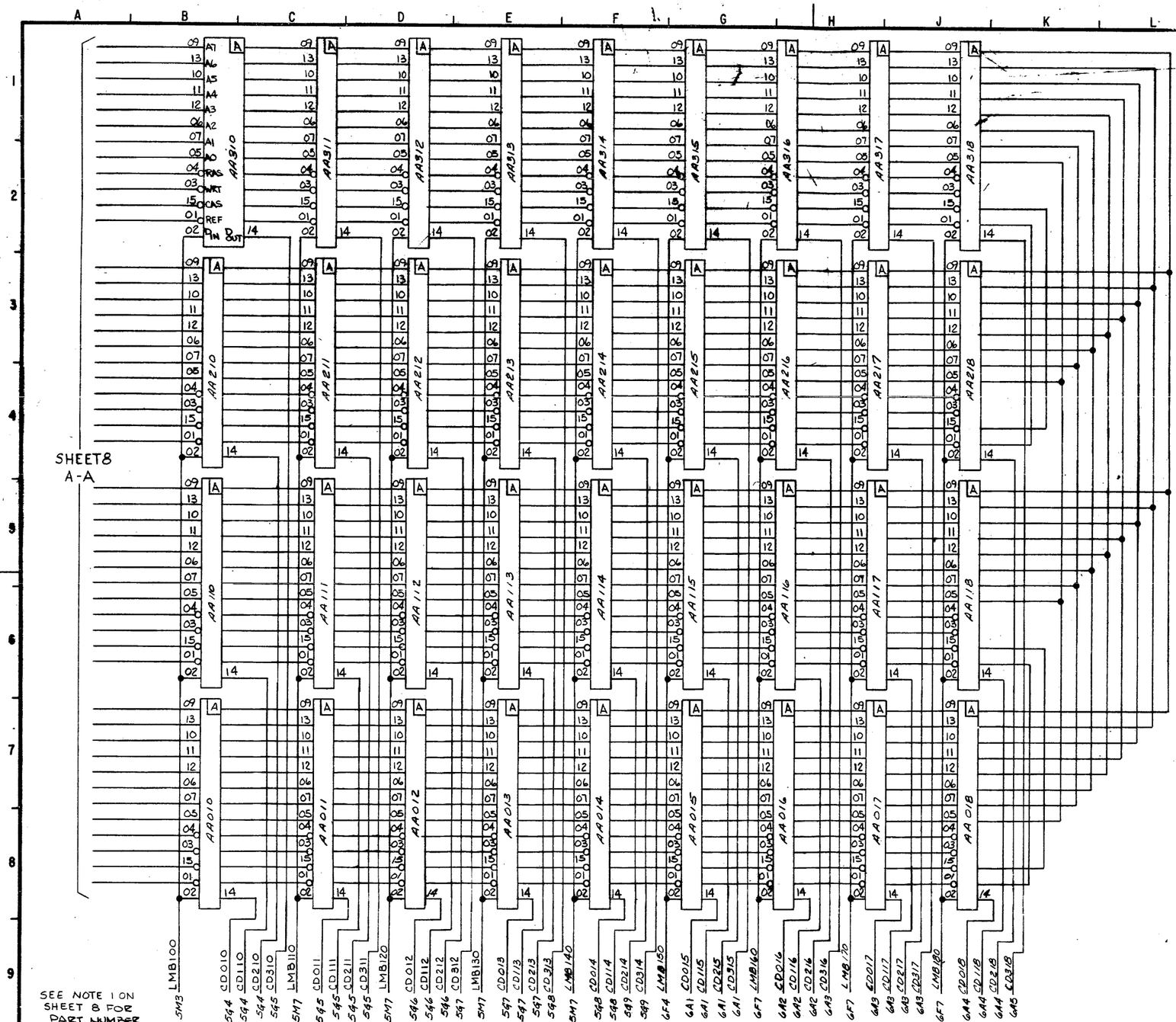
Computer Systems Division
Oceanport, N.J. 07757

TITLE

STM 2.0 MB

TASK 03979	SHT
DWG 35-764 R01 D08	8 - 16

NOTES
1. PER F01 VARIATION : AA000 THRU AB338 ARE 19-274 (16K RAM)
   PER F02 " AA000 " AD338 ARE 19-274 (16K RAM)
   PER F03 " AA000 " AB338 ARE 19-281 (64K RAM)
   PER F04 VARIATION : AA000 THRU AD338 ARE 19-281 (64K RAM)
2. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU
3. ALL RESISTORS ARE ⅛W, ± 5%
4. RESISTORS MODULES ARE 21-073, 33Ω.



REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE: -	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	8-13-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE

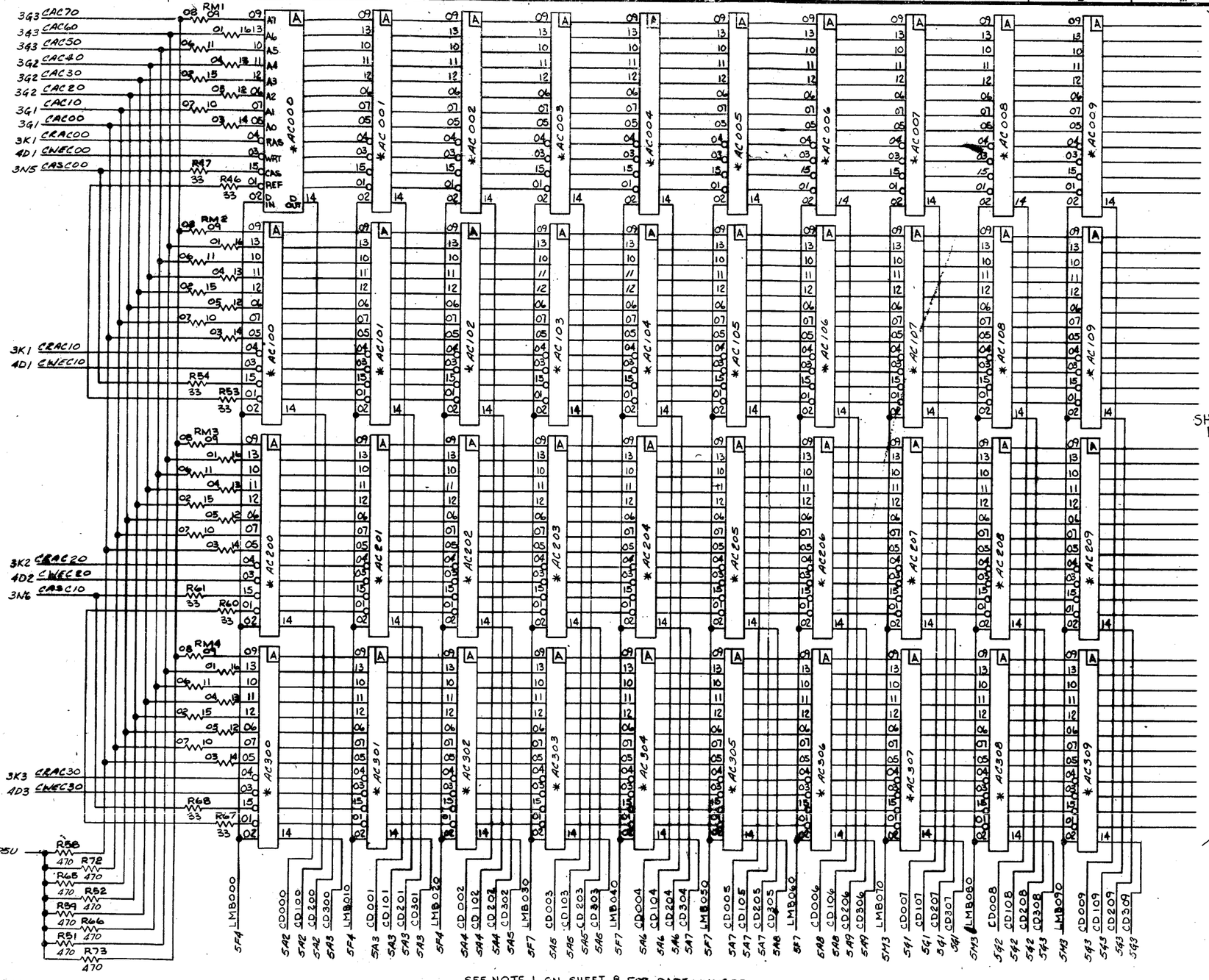
STM 2.0 MB

TASK 03979

DWG 35-764 D08

SHT 9 -16

NOTES 1. UNLESS OTHERWISE SPECIFIED: ALL LOGIC IS POWERED BY PSU



SEE NOTE 1 ON SHEET 8 FOR PART NUMBER

NOTES

1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY P5U
2. ALL RESISTORS ARE V8 W ±5%
3. RESISTOR MODULES ARE 21-073, 33 Ω

PT. NO.	VARIATION
F02 & F04	AS SHOWN
F01 & F03	AS SHOWN LESS PARTS MARKED WITH AN ASTERISK (*)

REVISIONS

AREA A2 / AG.: REMOVED REF'S TO A25 (Pg 4)					
JAT	AU	4733	MS	6-10-81	201

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .XX ±.02	X ±.03 ANGLES ±1°
NAME		TITLE	DATE
	S.TRIMARCHI	DES / DFT	8-13-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

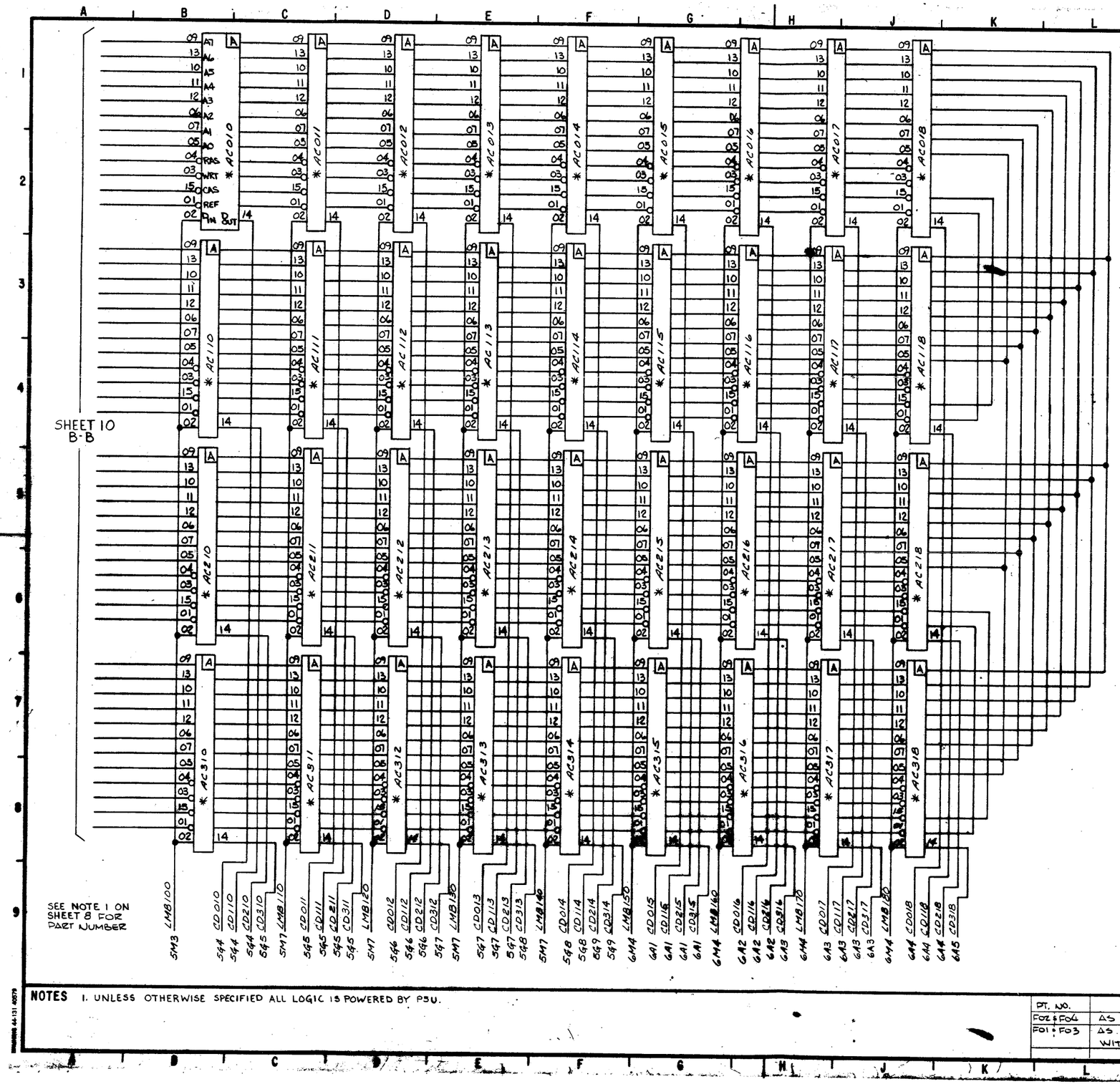
PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE

STM 2.0 MB

TASK 03979	SHT
DWG 35-764 R01 D08	10 - 16



NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU.

PT. NO.	VARIATION
F02 ÷ F04	AS SHOWN
F01 ÷ F03	AS SHOWN LESS PARTS MARKED WITH AN ASTERISK (*)

REVISIONS

UNLESS OTHERWISE SPECIFIED

SCALE:

TOLERANCE:

DIMENSIONS ARE IN INCHES

.XXX ±.005 .X ±.03
.XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	8-18-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

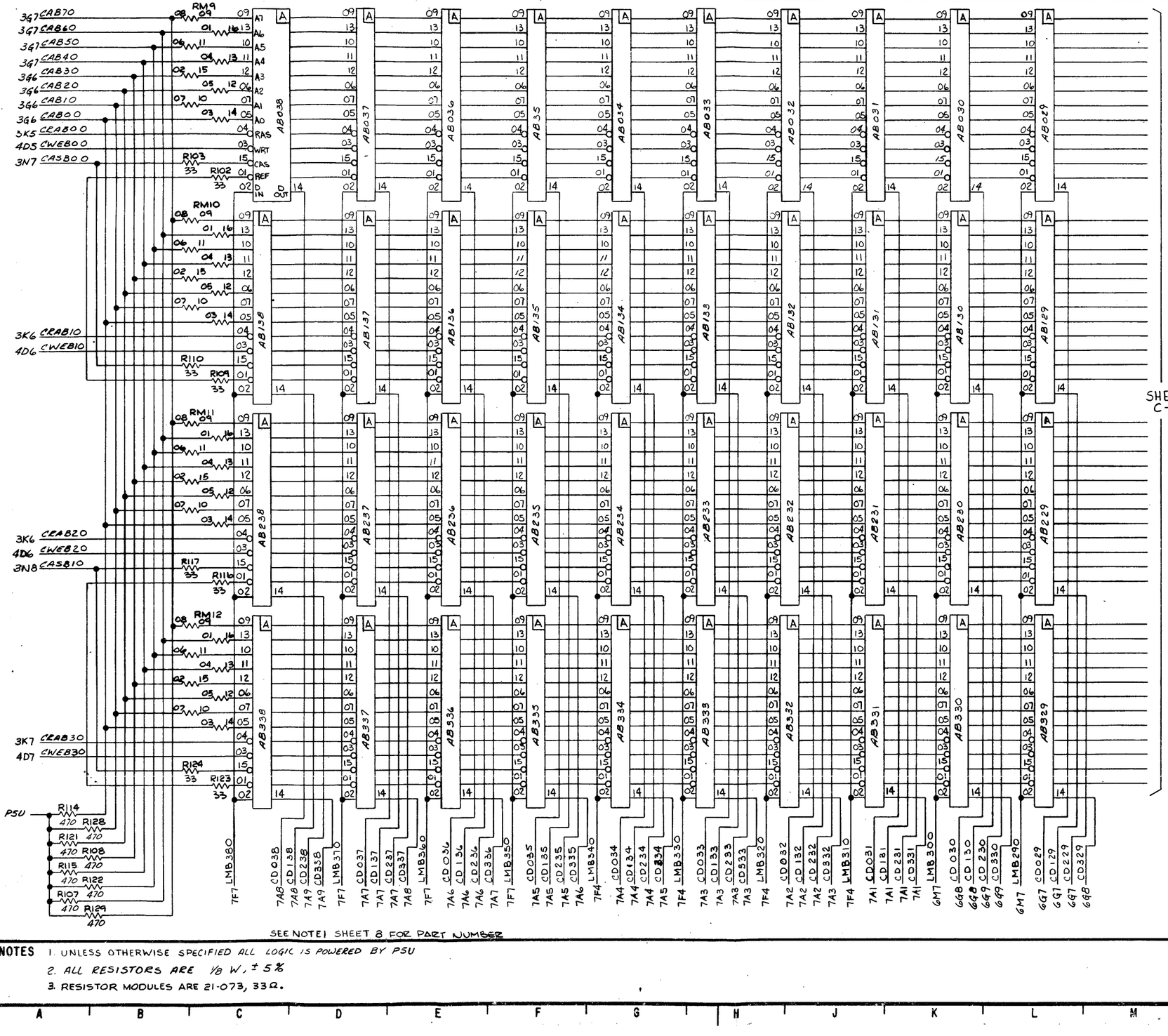
TITLE

STM 2.0 MB

TASK 03979

SHT 11 - 16

DWG 35-764 D08



NOTES

1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU
2. ALL RESISTORS ARE 1/8 W, ± 5%
3. RESISTOR MODULES ARE 21-073, 33Ω.

REVISIONS				
AREAS A2 & A6: REMOVED CROSS-REFS TO A37. (Pg 4)				
JAT	AV	4733	MS	6-10-81	R01

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ± .005 .XX ± .02	.X ± .03 ANGLES ± 1°
NAME		TITLE	DATE
	S. TRIMARCHI	DES / DFT	8-13-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

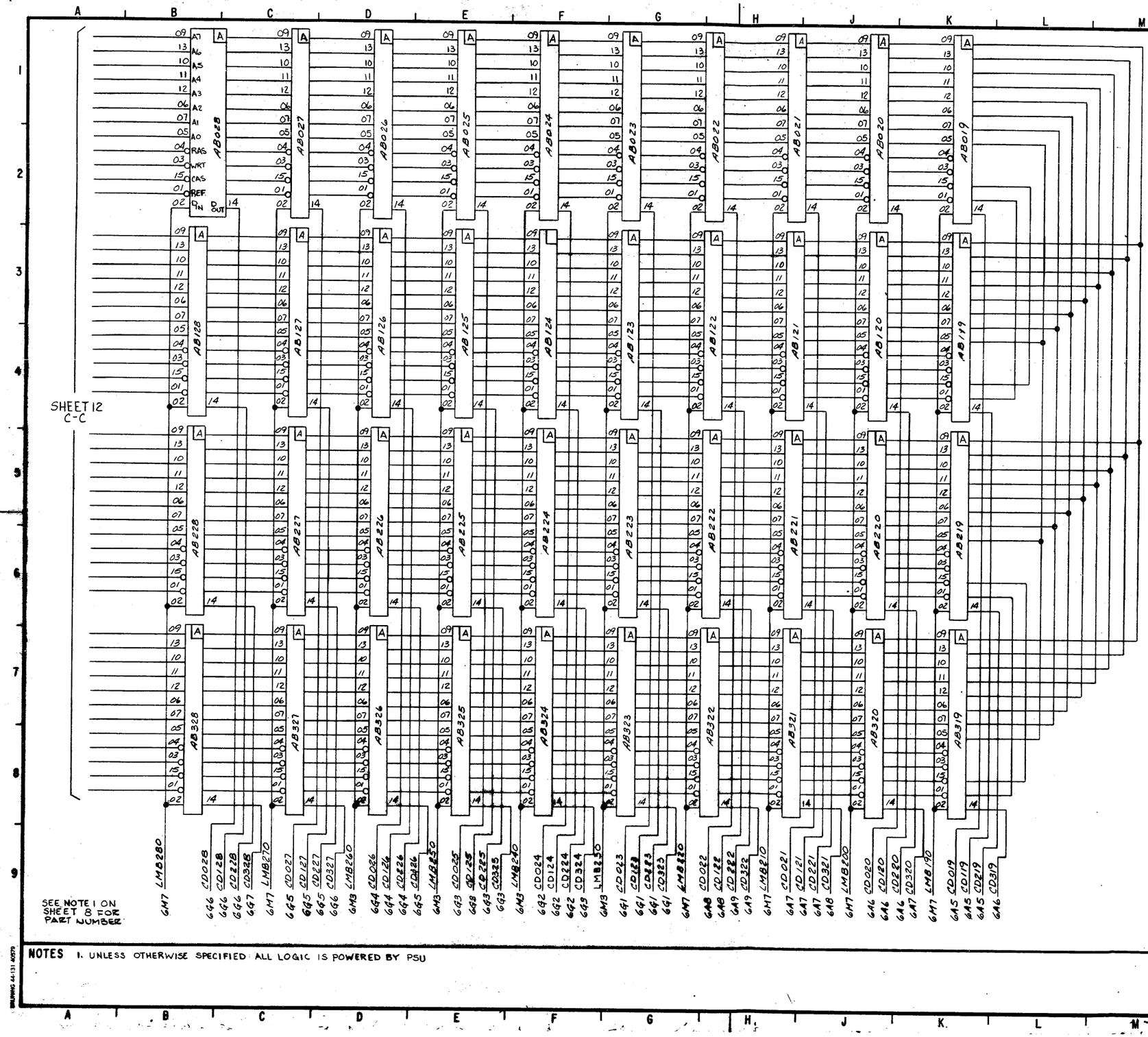
PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE

STM 2.0 MB

TASK 03979	SHT
DWG 35-764 R01 D08	12 - 16



REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	S. TRIMARCHI	DES / DFT	8-14-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

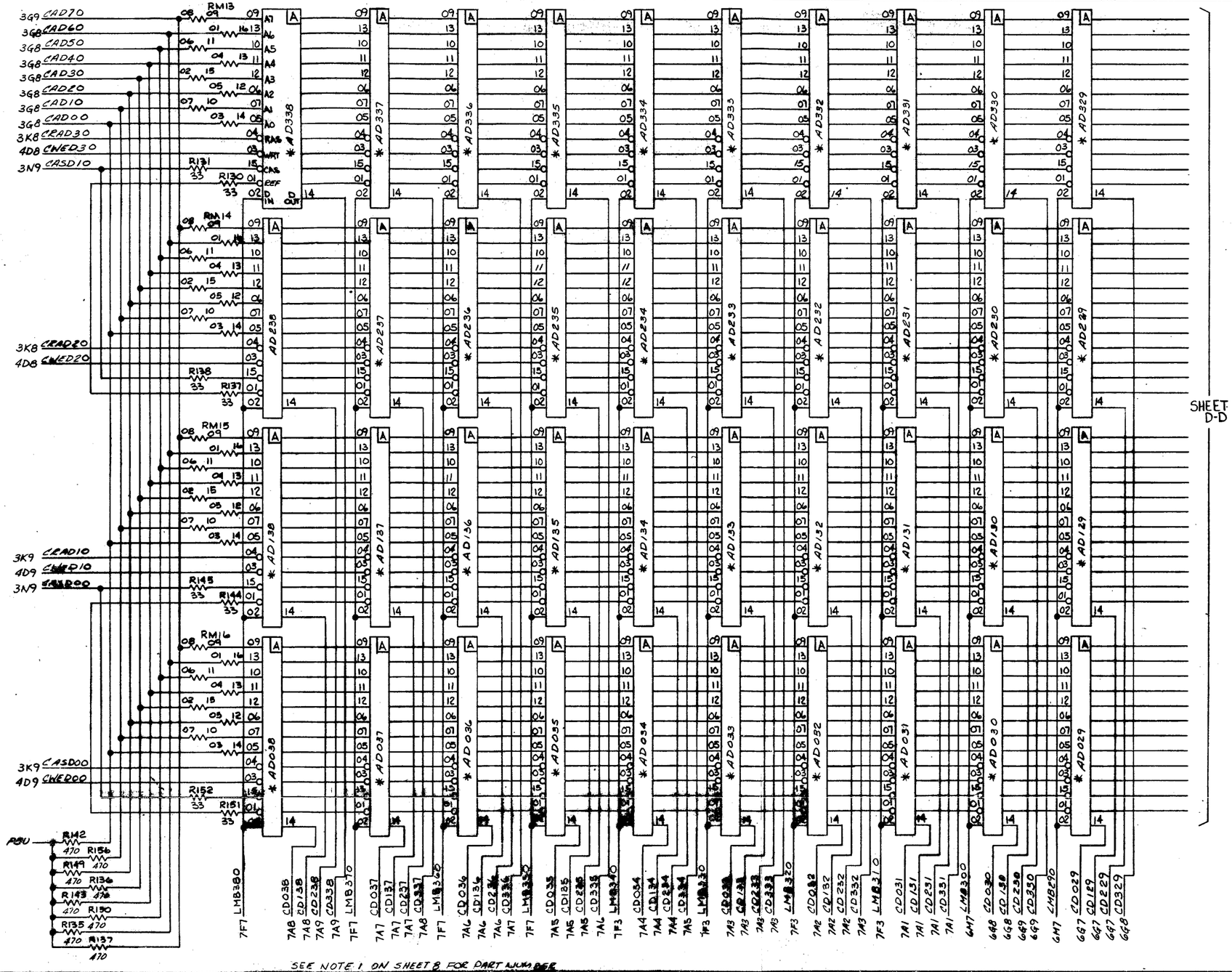
Computer Systems Division
Oceanport, N.J. 07757

TITLE

STM 2.0MB

TASK 03979	SHT
DWG 35-764 D08	13 - 16

NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU



SHEET 15
D-D

SEE NOTE 1 ON SHEET 8 FOR PART NUMBER

NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU
2. ALL RESISTORS ARE 1/8 W, ±5%
3. RESISTOR MODULES ARE 21-073, 33Ω.

PART NO	VARIATION
F02 + F04	AS SHOWN
F01 + F03	AS SHOWN LESS PARTS MARKED WITH AN ASTERISK (*)

REVISIONS

ADDED A2 & A6. REMOVED CROSS REFS TO A37 (3,4)				
JAT	GJ	4733	MS	6-10-81	R01

UNLESS OTHERWISE SPECIFIED

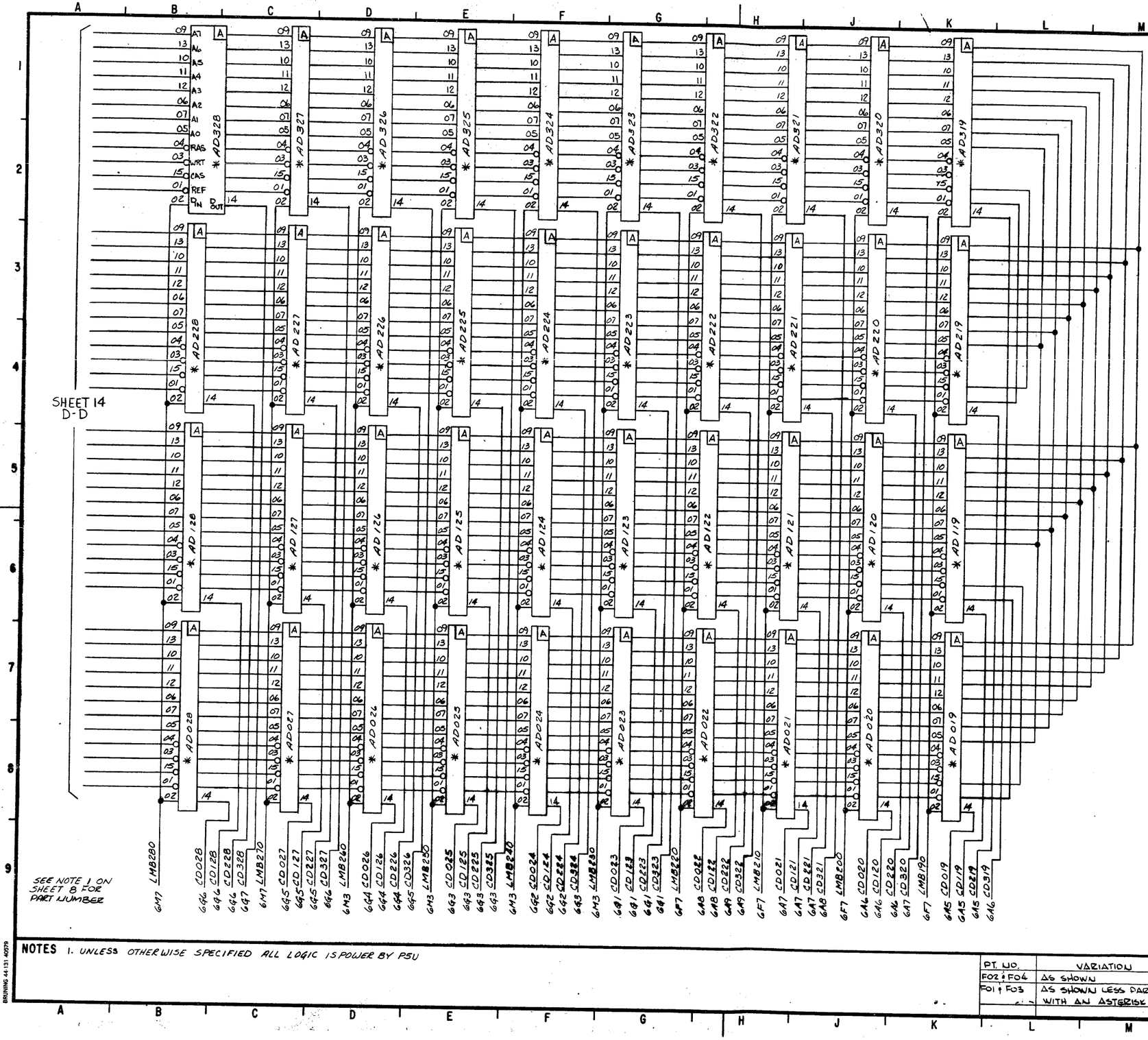
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	S.TRIMARCHI	DES / DFT	8-13-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
STM 2.0 MB

TASK 03979 | SHT 14 - 16
DWG 35-764 R01 D08



NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWER BY PSU

PT. NO.	VARIATION
F02 ↑ F04	AS SHOWN
F01 ↑ F03	AS SHOWN LESS PARTS MARKED WITH AN ASTERISK (*)

REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	8-14-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

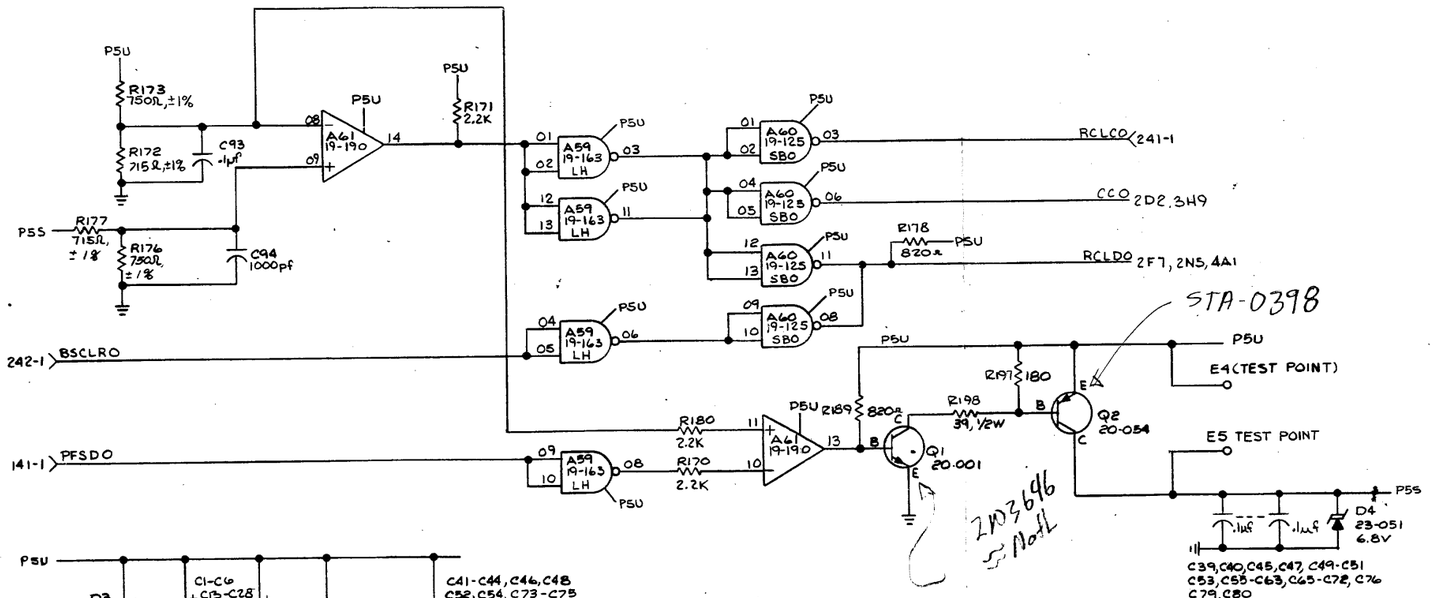
Computer Systems Division
Oceanport, N.J. 07757

TITLE

STM 2.0 MB

TASK 03979	SHT
DWG 35-764 D08	15 - 16

REVISIONS					
ADDED R178 AT G5					
GPS		4499	M	10-8-80	R01



NOTES 1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/4 W, ± 5%

UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	S. TRIMARCHI	DES / DFT	9-28-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

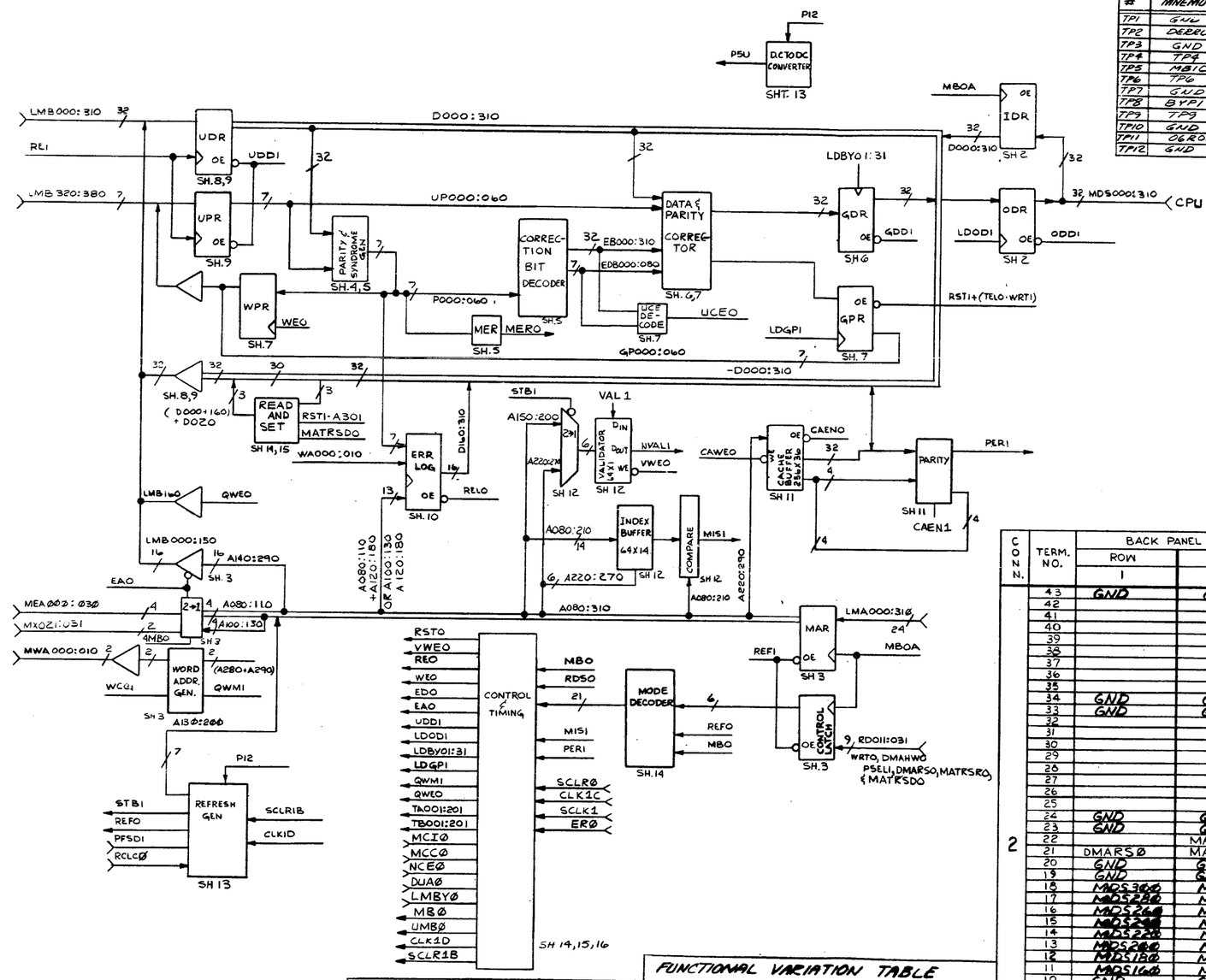
TITLE

STM 2.0MB

TASK 03979	SHT
DWG 35-764 R01 D08	16 - 16

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J 07757



TEST POINTS		
#	MNEMONIC	SHT.
TP1	GND	5
TP2	DERRO	5
TP3	GND	12
TP4	TP3	13
TP5	MBIC	13
TP6	TP6	13
TP7	GND	16
TP8	BYP1	16
TP9	TP9	5
TP10	GND	3
TP11	06R08	7
TP12	GND	7

BACK PANEL MAP		TERM. NO.	CONN.
ROW 1	ROW 2		
GND	GND	43	
	BSCLR0	42	
PFSD0	RCLC0	41	
		40	
		39	
	MX021	38	
MX011	MX031	37	
LMB381	LMB371	36	
LMB361	LMB351	35	
GND	GND	34	
GND	GND	33	
LMB341	LMB331	32	
LMB321	LMB311	31	
LMB301	LMB291	30	
LMB281	LMB271	29	
LMB261	LMB251	28	
LMB241	LMB231	27	
LMB221	LMB211	26	
LMB201	LMB191	25	
GND	GND	24	
GND	GND	23	
RD001	RD011	22	
RD021	RD031	21	
GND	GND	20	
GND	GND	19	
LMB181	LMB171	18	
LMB161	LMB151	17	
LMB141	LMB131	16	
LMB121	LMB111	15	
LMB101	LMB091	14	
LMB081	LMB071	13	
LMB061	LMB051	12	
LMB041	LMB031	11	
GND	GND	10	
GND	GND	09	
LMB021	LMB011	08	
LMB001		07	
MEA020	MEA030	06	
MEA000	MEA010	05	
MWA001	MWA011	04	
MCC0	MREF0	03	
MCI0	MRDS0	02	
MREQ	MWE0	01	
GND	GND	00	

BACK PANEL MAP		TERM. NO.	CONN.
ROW 1	ROW 2		
		43	
		42	
		41	
		40	
		39	
		38	
		37	
		36	
		35	
GND	GND	34	
GND	GND	33	
		32	
		31	
		30	
		29	
		28	
		27	
		26	
		25	
GND	GND	24	
GND	GND	23	
	MATRSD0	22	
DMARS0	MATRSR0	21	
GND	GND	20	
GND	GND	19	
MDS300	MDS310	18	
MDS280	MDS290	17	
MDS260	MDS270	16	
MDS240	MDS250	15	
MDS220	MDS230	14	
MDS200	MDS210	13	
MDS180	MDS190	12	
MDS160	MDS170	11	
GND	GND	10	
GND	GND	09	
MDS140	MDS150	08	
MDS120	MDS130	07	
MDS100	MDS110	06	
MDS080	MDS090	05	
MDS060	MDS070	04	
MDS040	MDS050	03	
MDS020	MDS030	02	
MDS000	MDS010	01	
GND	GND	00	

BACK PANEL MAP		TERM. NO.	CONN.
ROW 1	ROW 2		
GND	GND	43	
	SCLR0	42	
		41	
		40	
		39	
		38	
		37	
GND	GND	36	
		35	
GND	GND	34	
GND	GND	33	
		32	
		31	
		30	
		29	
		28	
		27	
		26	
		25	
GND	GND	24	
GND	GND	23	
NVM0		22	
CLK1C	SCLK1	21	
GND	GND	20	
GND	GND	19	
NCE0	GMWE0	18	
DUA0	PSEL1	17	
DMAHW0	LMBY0	16	
ER0	WRT0	15	
LMA300	LMA310	14	
LMA280	LMA290	13	
LMA260	LMA270	12	
LMA240	LMA250	11	
GND	GND	10	
GND	GND	09	
LMA220	LMA230	08	
LMA200	LMA210	07	
LMAI80	LMAI90	06	
LMAI60	LMAI70	05	
LMAI40	LMAI50	04	
LMAI20	LMAI30	03	
LMAI00	LMAI10	02	
LMA080	LMA090	01	
GND	GND	00	

REVISIONS																		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
	08	05	02		01	01	02	01	05	03	02	04	05	04	03	05	03	05

NOTE - SEE SHT 2 FOR TABLE OF SPARES.

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REV LEVEL.

	F04	35-771 R09	F04	W/O CACHE & W/O D.C. TO D.C. CONVERTER; AS SHOWN ON SHTS 11, 12 AND 13
OBSOLETE	F03	35-771 R06	F03	W/CACHE & DC TO DC CONVERTER; AS SHOWN ON SHT'S 11, 12 AND 13
OBSOLETE	F02	35-771 R07	F02	W/O CACHE & W/DC TO DC CONVERTER; AS SHOWN ON SHT'S 11, 12 AND 13
	F01	35-771 R09	F01	W/CACHE & W/O DC TO DC CONVERTER; AS SHOWN ON SHT'S 11, 12 AND 13

FUNCTIONAL VARIATION TABLE

USED IN MANUAL 47-011 & 47-004

REVISIONS					
PRE PRODUCTION APPROVAL	DEV PROD	INIT	DATE		

III VARIATION TABLE FOR NAS MDT SPEC. 35-771 WAS SPEC AS R00. SHEETS 2, 7, 8, 9, 10, 11, 12, 13, 14, 16, 17 & 18 WERE R00.
VT 4592 M 11-5-80 R01

RELEASED FOR PRODUCTION
ENG. S. [illegible] DATE 11/ [illegible]

REVISED SHTS 1, & 12
VT 4597 MS 2-5-81 R02

REVISED SHTS 2, 3, 7, 10, 11, 13, 14
JAM 4635 MS 6-8-81 R03

REVISED SHTS 1, 9, 13 & 18:
4743 MS 7-21-81 R04

REV'D SHTS 1-3, 9, 13, 15-18: REV TABLE, 35-771 F01, F03 & F04 WAS R03: 35-771 F02 WAS R04;
4764 MS 10-13-81 R05

REV TABLE 35-771 F01, F03 & F04 WAS R05. 35-771 F02 WAS R06. F02 & F03 HAVE BEEN MADE OBSOLETE. REVISED SHTS 1, 2, 9, 12 & 14-18
4891 MS 11-6-81 R06

REVISE SHTS 1, 16 & 18. 35-771 F01 & F04 WERE R06.
4900 R 11-20-81 R07

REV'D SHTS 1, 2, 5, 6, 9, 10, 12, 13-16; 35-771 F01 & F04 WERE R07.
5089 MS 8-13-82 R08

SCALE -

TOLERANCE
XXX ± .005
XX ± .02
X ± .09
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

E. GREENSTEIN	TEST	11-14-80
B. GRAY	DRAFT	11-14-80
R. OERO	CHK	11-14-80
S. AGRAWAL	ENGR	11-14-80
R. BARKER	QC	11-14-80
D. FRANKENBERGER	MGR	11-14-80

TITLE SCHEMATIC
LOCAL BANK CONTROLLER

TASK NO. 03976
SIZE NO. D
SYM NO. 35-771 R08
SHEET OF 1 — 18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J 07757

REVISIONS				
IN TABLE OF SPARES DELETED OGR11 AND 20H-03. ADDED 17A, 19-236, 08 & 11, 22D-12 & 19M10.				
DSF	AV	4542	11-5-80	R01
SPARE GATE CHART REMOVED U.M13 & ADDED 22D03, 12B04				
JAT	AV	4625	MS	4-9-81	R02
IN SPARE GATE CHART, ADDED 19D1: DELETED 18A, 19-234; SPARE 13:				
JAM	AV	4749	MS	10-13-81	R03
ADDED OGM TO SPARE GATE TABLE				
JLV	AV	4891	MS	11-6-81	R04
DELETED 05A, 19-063, OUTPUT 09 FROM SPARES TABLE.				
[illegible]	AV	5089	MS	8-19-82	R05

PROCESSOR DATA BUS

01K 19-232 (ODR)
00K 19-232
03K 19-232
04K 19-232

OUTPUT DATA REGISTER

ODD1 16N4
LDOD1 16K9

MDS000 101-2
MDS010 201-2
MDS020 102-2
MDS030 202-2
MDS040 103-2
MDS050 203-2
MDS060 104-2
MDS070 204-2
MDS080 105-2
MDS090 205-2
MDS100 106-2
MDS110 206-2
MDS120 107-2
MDS130 207-2
MDS140 108-2
MDS150 208-2
MDS160 111-2
MDS170 211-2
MDS180 112-2
MDS190 212-2
MDS200 113-2
MDS210 213-2
MDS220 114-2
MDS230 214-2
MDS240 115-2
MDS250 215-2
MDS260 116-2
MDS270 216-2
MDS280 117-2
MDS290 217-2
MDS300 118-2
MDS310 218-2
MB0A 13N7

01R 19-232
00R 19-232
07R 19-232
08R 19-232

INPUT DATA REGISTER

INPUT OUTPUT DATA REGISTER

13C 19-126 SG
03J 19-236 SA

TA061 16D5
SFW1 14H4
TA101 16D5
WDENO 14M9
MDS160 10R3

REF. DES.	PART NUMBER	SPARE OUTPUTS
23M	19-055	06
05M	19-234	04, 10, 13
20H	19-055	06

TABLE OF SPARES

REF. DESIGN	PART NUMBER	SPARE OUTPUTS
19H	19-058	12
17E	19-126	08
16E	19-055	11
15C	19-131	07, 06, 10, 11, 14, 15
01F	19-241	06
19M	19-234	10
07C	19-236	08,
06C	19-235	03, 08, 11
05H	19-234	04, 10, 13
05F	19-234	13
12E	19-163	06, 08 & 11
10A	19-163	03, 08
23D	19-154	08, 10, 12
05E	19-127	11
13H	19-126	06
13C	19-126	08
14D	19-234	04, 10, 13
25F	19-124	03, 06
09R	19-125	08, 11
09B	19-057	04
25H	19-059	12
19A	19-059	12
22F	19-058	06, 12
22D	19-057	08, 06, 10, 12
20B	19-057	06, 10, 12
20A	19-057	06
12B	19-057	04
03F	19-057	04, 10 & 12
17A	19-236	08, 11
06M	19-235	08, 11
10A	19-163	11
09A	19-160	11

TABLE OF SPARES

SCALE—
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
B. GRAY	DRAFT	
	CHK	
	ENGR	

TITLE SCHEMATIC
LBC
TASK NO. 03976
DWG NO. 35-771R05D08
SHEET OF 2—18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA K9: REMOVED CROSS REF TO/FROM 12B02				
JAT	4935	MS	6-8-81	R01
AREA H-7, ADDED NEW IC 19D: 23F05 DID GO TO DEI: 15L2				
JAH	4769	MS	10-13-81	R02

PROCESSOR ADDRESS BUS

4MB/16MB MODULE ID

QUAD WORD COUNTER

NOTES:
1. STRAP 215-5 (TP10) TO 216-5(TP9) FOR 4MB SYSTEM. FOR SYSTEMS LARGER THAN 4MB, REMOVE THE STRAP.

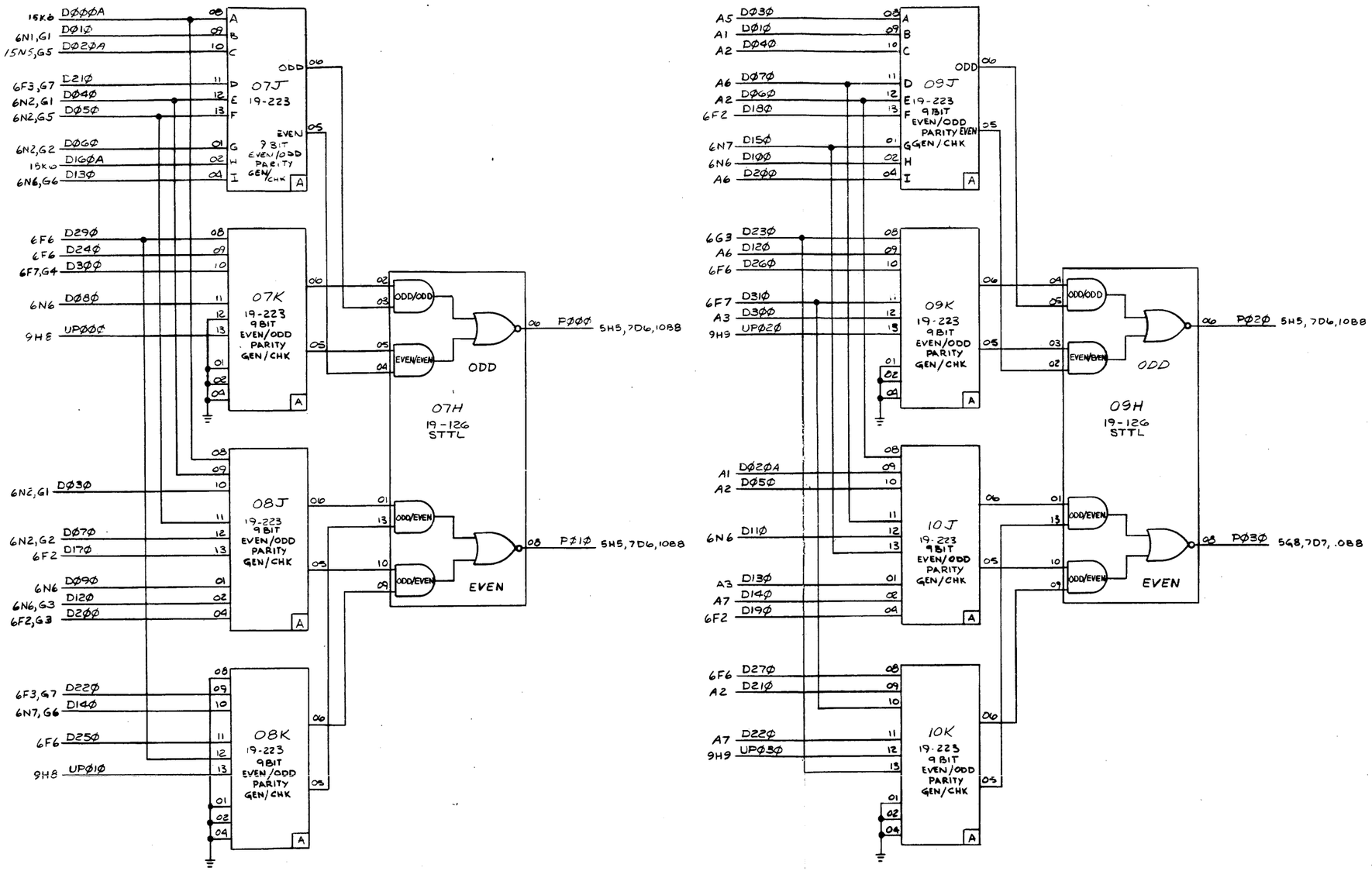
SCALE–	NAME	TITLE	DATE
TOLERANCE .XX ± .005, .X ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	B. GRAY	DRAFT	1-11-80
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC

TASK NO. 03976
DWG NO. 35-771 R02008
SHEET OF 3 — 18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



PARITY GENERATOR

SCALE –	NAME	TITLE	DATE
UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE : SCHEMATIC
LBC

PART NO 03976
DWG NO 35-771 D08
SHEET OF 4 - 18

DRAWING 44-231 24539

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS					
AREA L-3, 06J10 WAS 06J01 IN ERROR. CHG'D PER M102.					
HH	AV	5089	MS	8-18-82	R01

6N2 D03Ø
6N6 DØ8Ø
15K6 DØØØA
6N6 DØ9Ø
6N6 D10Ø
6N1 DØ1Ø
15N5 DØ2ØA
6F2,G1 D18Ø
6F1,G1 D17Ø
11J 19-223 9 BIT EVEN/ODD PARITY GEN/CHK
ODD
EVEN
A

15K6,G1 DKØØA
6N6 D11Ø
6F2,G2 D19Ø
6F7 D31Ø
9H8 UPØ4Ø
6F6,G3 D28Ø
11K 19-223 9 BIT EVEN/ODD PARITY GEN/CHK

6F6,G2 D24Ø
6F6,G2 D25Ø
12J 19-223 9 BIT EVEN/ODD PARITY GEN/CHK

6N6 D12Ø
6N6 D13Ø
6N6 D14Ø

6N7 D15Ø
6F6,G3 D26Ø
6F6,G3 D27Ø
6F6 D29Ø
9H8 UPØ5Ø
6F7 D30Ø
12K 19-223 9 BIT EVEN/ODD PARITY GEN/CHK

ODD/ODD
EVEN/EVEN
11H 19-126 STTL

ODD/EVEN
EVEN

PØ4Ø 48, 7D7, 10B8
PØ5Ø 48, 7D7, 10B8

A3 DIGØA
A3 D17Ø
A2 D18Ø
A3 D19Ø
6F3 D22Ø
6F4 D23Ø
A5 D24Ø
A5 D25Ø
A7 D26Ø
13J 19-223 9 BIT EVEN/ODD PARITY GEN/CHK

ODD/EVEN
ODD/EVEN
13H 19-126 STTL

A7 D27Ø
A4 D28Ø
6F3 D20Ø
6F3 D21Ø
9H9 UPØ6Ø
13K 19-223 9 BIT EVEN/ODD PARITY GEN/CHK

4F4 PØØØ
4F6 PØ1Ø
4M4 PØ2Ø
15L2 MEØ
DERRO
08H 19-129 3 TO 8 DECODER
G2A SEL
G2B DNB
G1

P5 75 03F 11 01 03F 19-057 SG 02
1K
TP1 224-5
TP2 223-5
SEE NOTE 1

7D7, 10B8 PØ6Ø

10H 19-129 3 TO 8 DECODER

4M6 PØ3Ø
F4 PØ4Ø
F5 PØ5Ø
12H 19-129 3 TO 8 DECODER

DBØØ 6H7, 7A3
DB1Ø 6H2, 7A1
DB2Ø 6H6, 7A2
DB3Ø 6A8
DB4Ø 6A9, 7A3
DB5Ø 6A9
DB6Ø 6H2
DB7Ø 6H3

DAØØ 6A2, 7A5
DA1Ø 6A2
DA2Ø 6A1
DA3Ø 6A3
DA4Ø 6A1
DA5Ø NC
DA6Ø NC
DA7Ø NC

DCØØ 6A3, 7A2
DC1Ø 6A4, 7A3
DC2Ø 6A1, 7A4
DC3Ø 6A3
DC4Ø 6A5, 7A5
DC5Ø 6A7
DC6Ø 6A8
DC7Ø 6H7

PØØØ
PØ1Ø
PØ2Ø
PØ3Ø
PØ4Ø
PØ5Ø
PØ6Ø
PØ7Ø
06J 19-082 SGO

PØ3Ø
PØ2Ø
PØ1Ø
PØØØ
06H 19-082 SGO

08 MERO 15N2
10 03F 76 470 P5
05 03F 19-057 SG 06 MERI 15E8, 7N6

NOTES;
1. TO DISABLE ERROR CORRECTION CONNECT 224-5 TO 223-5.

MEMORY ERROR AND PARITY GENERATOR

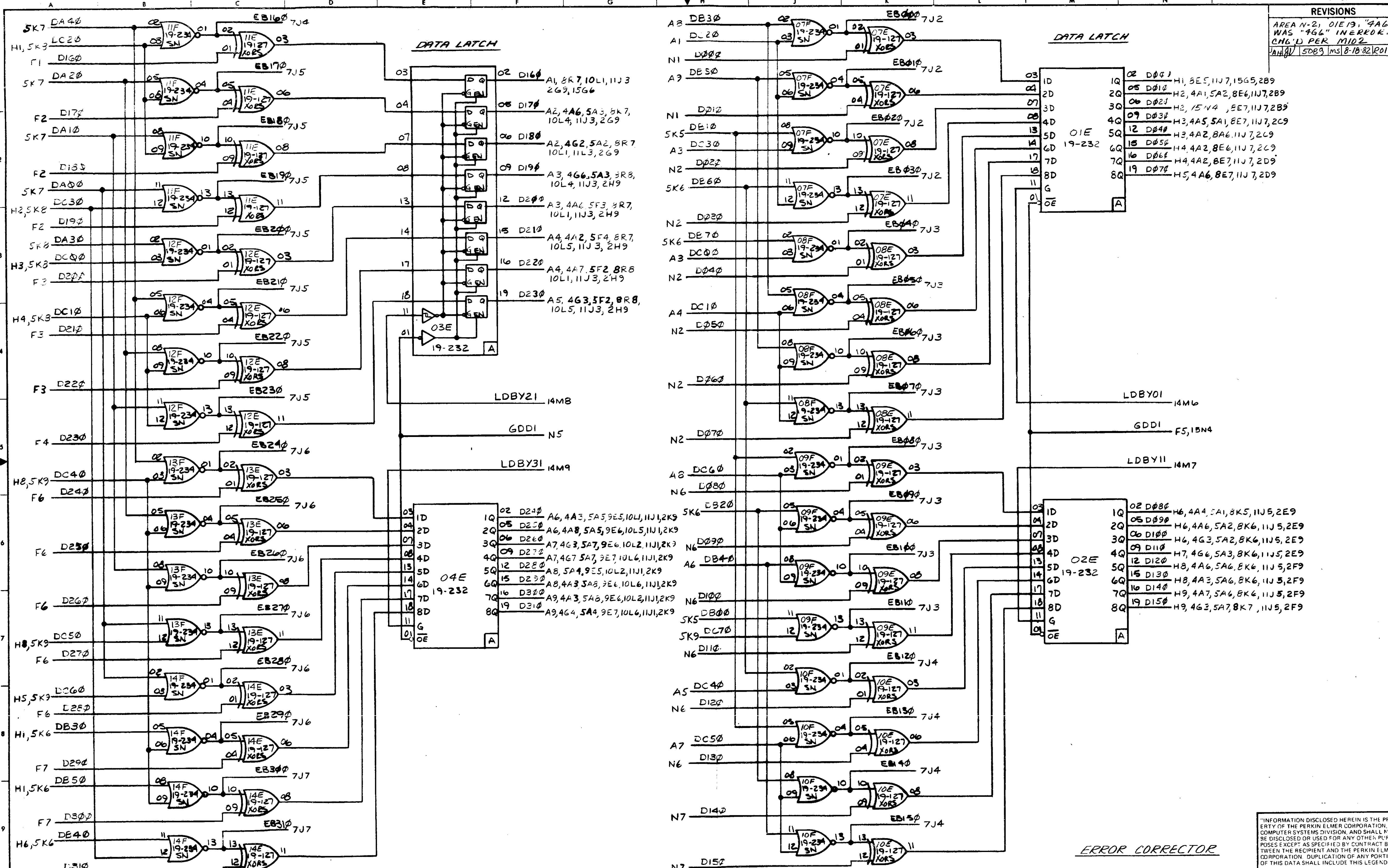
SCALE –
DRAWN
CHK
ENGR
DATE
TITLE: SCHEMATIC
LBC
TASK NO 03976
DWG NO 35-771R01D08
SHEET 5 OF 18

BRUNING 44-231 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

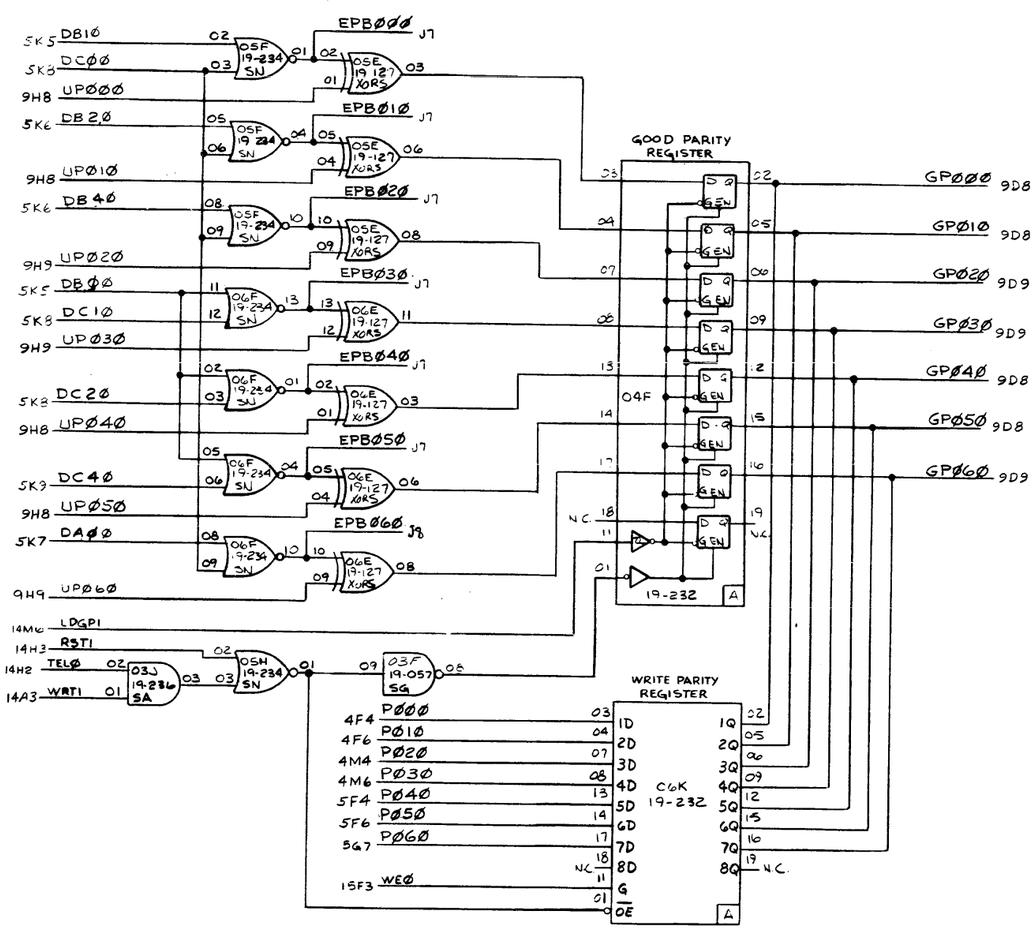
AREA N-2, 01E19, "4A6" WAS "4G6" IN ERROR. CHG'D PER M102
AH | 5089 | MS | 8-18-82 | R01



SCALE –	NAME	TITLE	DATE	TITLE : SCHEMATIC LBC
TOLERANCE .XXX ± .005 .XX ± .02 .X ± .03 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT		
		CHK		
		ENGR		TASK NO. 03976
				DWG NO. 35-771R01D08 SHEET 6 OF 18

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA R3 UCEO WAS SPEC AS CROSS REFERENCED TO 9N3, 12A1, 15A2. IN AREA R4 GATE 06R & RESISTOR 00K WERE NOT SPEC.				
JAT	1342		11-4-80	BCV
IC 06R AREA K8: PIN 9 WAS TO 3K9, A191. PIN 10 WAS TO 14H5 RELI.				
JAT	1635	MS	6-8-81	BDZ



NOTES:
1. FOR CUSTOMER SERVICE ONLY:
TO TURN OFF UCE/NPM AND MODULE I.D. LAMPS;
CONNECT TP11 TO TP12 MOMENTARILY. DO NOT STRAP.
MAKE SURE TO REMOVE THE JUMPER.

PARITY CORRECTOR & UNCORRECTABLE ERROR

SCALE -	NAME	TITLE	DATE
UNLESS OTHERWISE SPECIFIED	B. GRAY	DRAFT	
		CHK	
		ENGR	

TITLE : SCHEMATIC
LBC
DWG NO 03976
REV NO 35-771 R02 D08
SHEET OF 7 – 18

DRAWING 44-231 24538

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
12S, 12T, 14S, 14T, 17S & 17T WERE 21-090F03, 330 & 470Ω.				
4592	M	11-4-80	R01	

LMB001 107-1 08 220 330 10 P5U
LMB021 108-1 09 220 330 P/O 17T 21-090 F01 01
LMB001 3G5
LMB021 3G5

LMB011 208-1 09 220 330 10 P5U P/O 17S 21-090 F01 01
LMB011 3G5

LMB041 111-1 09 220 330 10 P5U
LMB061 112-1 08 220 330 P/O 14T 21-090 F01 01
LMB041 3G5
LMB061 3G6

LMB031 211-1 09 220 330 10 P5U
LMB051 212-1 08 220 330
LMB071 213-1 07 220 330 P/O 14S 21-090 F01 01
LMB031 3G5
LMB051 3G5
LMB071 3G6

LMB081 113-1 07 220 330 10 P5U
LMB101 114-1 06 220 330
LMB121 115-1 05 220 330
LMB141 116-1 04 220 330 P/O 14T 21-090 F01 01
LMB081 3M1
LMB101 3M2
LMB121 3M2
LMB141 3M3

LMB091 214-1 06 220 330 10 P5U
LMB111 215-1 05 220 330
LMB131 216-1 04 220 330
LMB151 217-1 03 220 330 P/O 14S 21-090 F01 01
LMB091 3M2
LMB111 3M2
LMB131 3M2
LMB151 3M3

LMB161 117-1 03 220 330 10 P5U
LMB181 118-1 02 220 330 P/O 14T 21-090 F01 01
LMB171 218-1 02 220 330 10 P5U P/O 14S 21-090 F01 01

LMB201 125-1 02 220 330 10 P5
LMB221 126-1 03 220 330 P/O 12T 21-090 F01 01

LMB191 225-1 02 220 330 10 P5
LMB211 226-1 03 220 330
LMB231 227-1 04 220 330 P/O 12S 21-090 F01 01

K5 D080 02 K5 D120 17 K5 D090 04 K6 D130 15 K6 D100 06 K6 D140 13 K6 D110 08 K6 D150 11
A_1 B_4 A_2 B_3 A_3 B_2 A_4 B_1 BOE AOE
AY_1 BY_4 AY_2 BY_3 AY_3 BY_2 AY_4 BY_1
13M 19-240 A
18 03 16 05 14 07 12 09
01
1D 5D 2D 6D 3D 7D 4D 8D G OE
1Q 5Q 2Q 6Q 3Q 7Q 4Q 8Q
14R 19-232 B
02 12 04 15 07 17 08 18 11 01
D080 F5,6N6
D120 F5,6N6
D090 F6,6N6
D130 F6,6N6
D100 F6,6N6
D140 F6,6N7
D110 F6,6N6
D150 F6,6N7

15K6 D160A 02 N7 D200 17 N7 D170 04 N7 D210 15 N8 D180 06 N8 D220 13 N8 D190 08 N8 D230 11
A_1 B_4 A_2 B_3 A_3 B_2 A_4 B_1 BOE AOE
AY_1 BY_4 AY_2 BY_3 AY_3 BY_2 AY_4 BY_1
12M 19-240 A
18 03 16 05 14 07 12 09
01
1D 5D 2D 6D 3D 7D 4D 8D G OE
1Q 5Q 2Q 6Q 3Q 7Q 4Q 8Q
13R 19-232 B
02 12 04 15 07 17 08 18 11 01
D160 6F1
D200 J7,6F3
D170 J7,6F2
D210 J7,6F3
D180 J8,6F2
D220 J8,6F3
D190 J8,6F2
D230 J8,6F3

15K6 D000A 02 E6 D040 17 E6 D010 04 E6 D050 15 15K5 D020A 06 E7 D060 13 E7 D030 08 E7 D070 11 15E8 EDI 19 15G1 EDO 01
19-240 14M A
20 10 P5U
18 03 13 04 14 07 17 08 18 11 01
15R 19-232 B
D Q GEN
02 D000 6N1
12 D040 A6,6N2
05 D010 A6,6N1
15 D050 A6,6N2
06 D020 6N2
16 D060 A7,6N2
09 D030 A7,6N2
19 D070 A7,6N2

15K3 RE1
15L5 UDD1

LMB161 9M8

LMB BUS
DRIVERS AND RECEIVERS

SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	P MARCUS	DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC
TASK NO. 03976
DWG. NO. 35-7717R01D08
SHEET OF 8 — 18

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

12T 12S 9T 9S 17T & 17S WERE 21-090 F03, 330 & 470Ω, 21R03 WAS GMVFØ TO CONN 218-D.
IN AREA RB 21R11 WAS SPEC AS MNEMONIC "LCEO"; 21R19 WAS SPEC AS "LCEO" TO CONN 118-D. 21R17 WAS SPEC AS GDWG. TO 19M10. 19M & 22D GATES WERE DELETED. 20H & 06R 300K WERE NOT SPEC.
JW | JH | 4542 | | 11-4-80 | R01

AREA 5B. CROSS REF. FOR BMVFØ WAS N7, L7:
JW | JH | 4793 | MS | 7-21-81 | R02

AREA NB; RES: 00K WAS 09M, 1K TO P5; ADDED 13E8
JW | JH | 4769 | MS | 10-13-81 | R03

AREA K7-K9: 15M17 WAS NC; 15M04 WAS MNEM. GWEØ, DEST. 16S7; 15M19 WAS NC; 15M01 WAS MNEM. EAØ, DEST. 16S4; 15M03 WAS NC; 15M16 WAS MNEM. LMB161, DEST. 8R6. ADDED 18K RESISTOR TO 15M16
JW | JH | 4891 | MS | 11-5-81 | R04

AREA R-B: DELETED 13E9 FROM BMVFØ. GND PER M102
JW | JH | 5089 | MS | 12-28-81 | R05

LMB BUS
DRIVERS AND RECEIVERS

SCALE—
NAME
TITLE
DRAFT
CHK
ENGR
DATE

TITLE: SCHEMATIC
LBC

FSCM NO. 03976
DWG NO. 35-7718-05008
SHEET OF 9—18

PERKIN-ELMER

Ocean, N.J.

WRITE/READ ERROR LOGGER
ADDRESS MUX

ERROR LOGGER
SHIFT REGISTER

REVISIONS					
IN AREA AB 07M11 WAS TO LDGP1 LOC. 14M6. ADDED 17A					
VJ	GV	7542		11-4-80	R01
AREA R4: ADDED 7J8 TO 1K 21M PIN 06					
JAT	GV	7635	MS	6-8-81	R02
AREA N3, DELETED 09M 11K RES.), BETWEEN 06R03 & P5,					
JAH	GV	5089	MS	8-18-82	R03

ERROR LOGGER

SCALE—	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC

TASK NO. 03976
DWG NO. 35-771 R3 D08
SHEET OF 10 — 18

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN NOTE 1 FOA VARIATION WAS NOT SPEC.				
JAT	9542	11-5-80	E01	
AREAS K1-K8: ADDED 4 (02R/4SR) RESISTOR PACKAGES. ADDED NOTE 2.				
JAT	9635	WS	2-9-81	E02

CACHE 256 x 36

CACHE PARITY CHECK

16H7 TAA121 — FW WRITE
14G4 SFW1 — PW WRITE
1257 HIT1 — QW ERR
16D1 TB661 — QW NO ERR
14H3 SPW1
15L2 MEI — 03J 19-236 SA
1657 QWM1 — 03J 19-236 SA
16B4 TB661
16H2 TB121
16E4 TB080
20C 19-062 — 08 CAWEO

3E8 A22Ø
3E8 A23Ø
3E8 A24Ø
3E8 A25Ø
3E8 A26Ø
3E9 A27Ø
3K3 A28Ø
3K3 A29Ø
1656 CAENO

21K 19-254 256X9 RAM — WE, CE, OD — DB — A
22K 19-254 256X9 RAM — A
24K 19-254 256X9 RAM — A
25K 19-254 256X9 RAM — A

D31Ø 6F7 D30Ø 6F7 D29Ø 6F7 D28Ø 6F7 D27Ø 6F7 D26Ø 6F6 D25Ø 6F6 D24Ø 6F6
D23Ø 6F4 D22Ø 6F3 D21Ø 6F3 D20Ø 6F3 D19Ø 6F2 D18Ø 6F2 D17Ø 6F2 D16Ø 6F1
D15Ø 6N7 D14Ø 6N7 D13Ø 6N6 D12Ø 6N6 D11Ø 6N6 D10Ø 6N6 D09Ø 6N6 D08Ø 6N6
D07Ø 6N2 D06Ø 6N2 D05Ø 6N2 D04Ø 6N2 D03Ø 6N2 D02Ø 6N1 D01Ø 6N1 D00Ø 6N1

SEE NOTE 2 — 65.20K 1K — 21-025 F01 — P5
SEE NOTE 1 — 21-025 F04

23K 470 70 P5
23K 470 71 P5
23K 470 72 P5
23K 470 73 P5

23J 19-055 SQ
23K 19-056 SGO

9BIT EVEN/ODD PARITY GEN/CHK — A — B
21J 19-223 — EVEN OUT 05 NC — ODD OUT 06
22J 19-223 — 05 NC — 06
24J 19-223 — 05 NC — 06
25J 19-223 — 05 NC — 06

21H 19-060 SG — 06 PERI 16L8, 15A8

XRP2 14J3
1256 CHITI — 12A 19-064 SF DC — DS1 09 NC — DC 07
16R9 CPERI
13A4 SCLROC
218-4
219-4
330 16A* 76 P5
06 CACHE PARITY ERROR

1657 CAENI

NOTE 1. DEPOPULATE COMPONENTS MARKED WITH AN ASTERISK FOR F02 & F04 VARIATION.
2 DEPOPULATE COMPONENTS MARKED WITH A TRIANGLE (Δ) FOR F01 & F03 VARIATIONS.

CACHE & CACHE PARITY

SCALE—
TOLERANCE
XXX ± .005
XX ± .02
X ± .09
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
B. GRAY / D. STINE	DRAFT	
	CHK	
	ENGR	

TITLE SCHEMATIC
LBC

TAB NO. 03976
DWG NO. 35-771 R02D08
SHEET 11 OF 18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN NOTE 2 FOR VARIATION WAS NOT SPEC.				
WF/WJ	4542	11-5-80	R01	
AREA D2, REMOVED ASTERISK FROM 21D				
VT/WJ	4597	MS	2-5-81	P02
AREA N6; ADDED "MISB1" AND REF 15A8 TO 18F09 ADDED "MISA1" & REF 15A6 TO 18F10; ADDED "MISS1" & REF 15A7 TO 18F8!				
JCH/WJ	4891	MS	11-5-81	R03
CACHE VALIDATOR PER M102 AREA R-6, DELETED "15A9" FROM MIS1.				
WH/WJ	5089	MS	8-18-82	R04

NOTES:
1. REMOVE JUMPER 221-5 TO 222-5 TO FORCE CACHE MISSES.
2. DEPOPULATE IC'S MARKED WITH AN ASTERISK FOR F02 / F04 VARIATION.

SCALE—

	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC

SIZE 03976 | SHEET 12 OF 18
771 R04

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS					
IN AREA C2 REMOVED P5 CONNECTION FROM 19A. IN NOTE 2 FD4 VARIATION WAS NOT SPEC.					
JAT	AV	4542		11-5-80	RD1
AREA A5: REMOVED 12B 03L04 AREA G8: CROSS REF B5 WAS A5.					
JAT	AV	4635	MS	6-9-81	RD2
AREA F6-9, ADDED 05M & 06M: AREA H-3, ADDED CROSS REF C9 TO SCLR0B: AREA H9, 15B02503 WAS TO DPR1 K2					
JAH	AV	4743	MS	7-21-81	RD3
AREA F-3, CHGD MNEM. ON 05M02 FROM BMVFO TO NVM0; AREA R5, ADDED CROSS REF. 3M3 TO 11A11;					
JAH	AV	4764	MS	10-13-81	RD4
ADDED CROSS REF.: AREA R-8, TO MB1B (16G3).					
JAH	AV	5089	MS	8-19-82	RD5

16 MICRO SEC. OSC.

BURST REFRESH

1.8 MS OSC.

REFRESH COUNTERS

12V TO 5V CONVERTER

SEE NOTE 2

REFRESH & CONTROL

NOTE;
1. ALL IC ON THIS SHEET ARE P5U UNLESS NOTED OTHERWISE
2. DEPOPULATE COMPONENTS IN THE DOTTED BOX FOR FO1 & FO4 VARIATION.

SCALE—
TOLERANCE: XXX ± .005; XX ± .02; X ± .03; ANGLES ± 1°; UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
B. GRAY	DRAFT	
	CHK	
	ENGR	

TITLE SCHEMATIC LBC

TASK NO. 03976 SHEET OF

DWG NO. 35-7718205008 13—18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
IN AREA M6 "LDGP1" WAS SPEC AS GOING TO 10B8. IN AREA M5 "FNPMO" WAS SPEC AS GOING TO 7M4 ONLY
JAT 4342 11-4-80 R01
AREA J4: FROM 25H06 DEL 7J8 AREA D1: TO 19F06 ADDED DRST1 AREA C8: IC 19M WAS 22D.
JAT 4635 MS 6-9-81 R02
AREA M3: 08C04 WAS CONN. TO 18K13
JLV 9891 MS 11-5-81 R03
AREA R-5, 25R09 (FNPM1) DID GO TO 9M7 IN ERROR. CHG'D PER M102.
JAT 5089 MS 8-18-82 R04

COMMAND DECODE AND CONTROL

SCALE– | NAME | TITLE | DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED
DRAFT
CHK
ENGR

TITLE SCHEMATIC
LBC
TASK NO. 03976
DWG NO. 35-771R04-D08
SHEET OF 14—18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

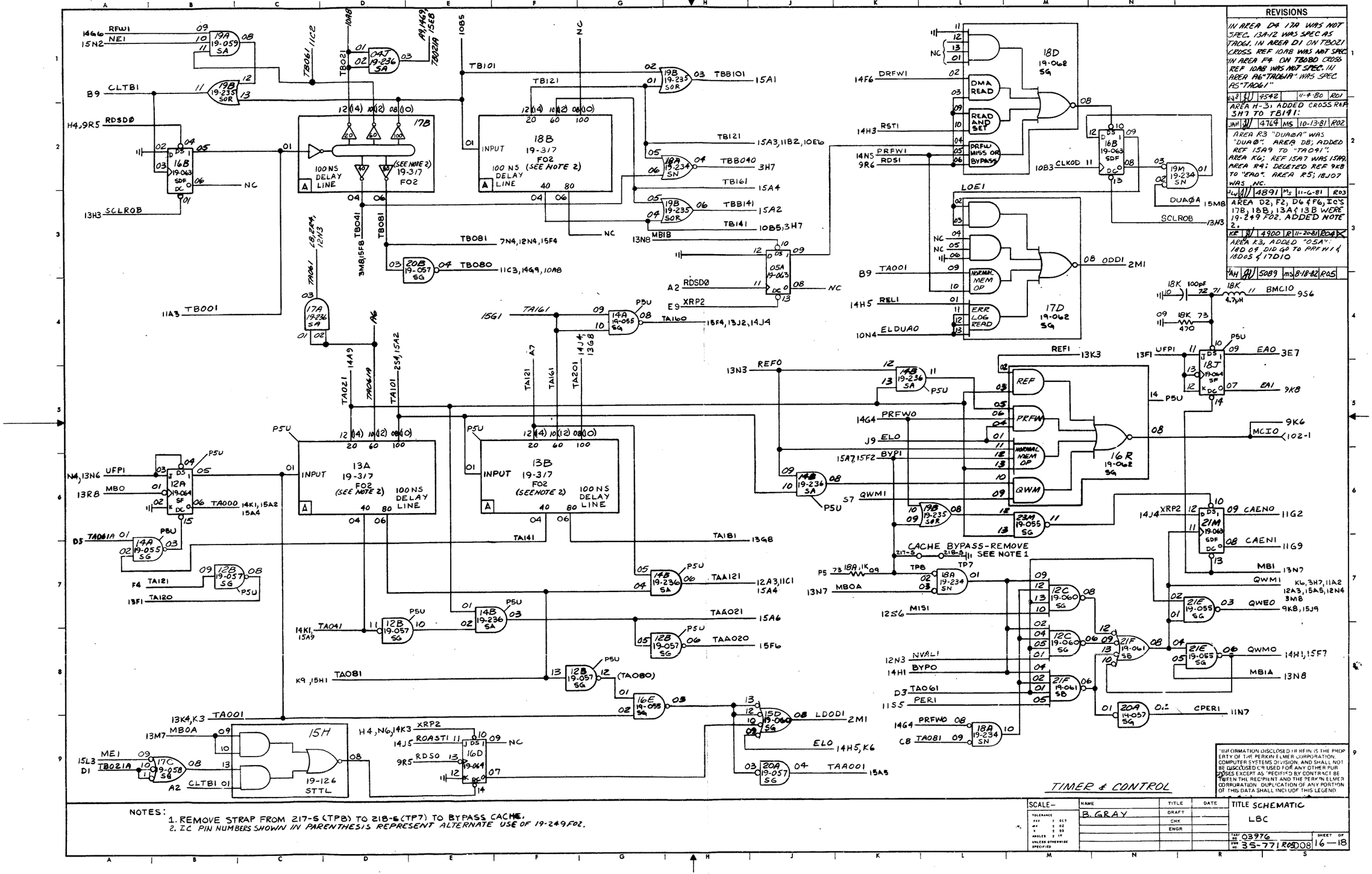
REVISIONS				
AREA L-2: DELETED 3H7 FROM ME1; ADDED 3H7 TO ME0: AREA F-3, 19C/3 DID GO TO 20D05:				
JH	GJ	4764	MS	10-13-81	R01
AREA A7-A9: ADDED GATE 06M; 18F02 WAS "MISI" REF 12N5; PIN 12 WAS "BYPI" REF 16K6; PIN 13 WAS CONN. TO PIN 12; 14J02 WAS "TA06I" REF 16D1. AREA N7: "DUA0A" WAS "DUA0", DELETED REF 11T-0 & ADDED 9K8. AREA H8; IC 18M WAS A 19-082, & DELETED RESISTER (470) 18K63-67 WHERE 18K63 WAS CONN. TO 18M08.				
JH	WW	4891	MS	11-6-81	R02
AREA J-7, DELETED "19N4" FROM "SCLKIA":				
JH	WW	5089	MS	8-18-82	R03

CONTROL

SCALE–	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	B. GRAY	DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC
TASK NO. 03976
DWG NO. 35-771R03D08
SHEET OF 15–18

PERKIN-ELMER
Computer Systems Division
Oceanport N.J. 07757



TIMER & CONTROL

REVISIONS					
IN AREA D4 17A WAS NOT SPEC. 13A-12 WAS SPEC AS TA06I. IN AREA D1 ON TB021 CROSS REF 10A8 WAS NOT SPEC. IN AREA F4 ON TB080 CROSS REF 10A8 WAS NOT SPEC. IN AREA A6 "TA061A" WAS SPEC AS "TA061"					
WJP	JJ	4542		11-4-80	R01
AREA H-3, ADDED CROSS REF 3H7 TO TB141:					
JAH	JJ	4764	MS	10-13-81	R02
AREA R3 "DUA0A" WAS "DUA0". AREA D8; ADDED REF 15A9 TO "TA041". AREA K6; REF 15A7 WAS 15A9. AREA R4: DELETED REF 9K8 TO "EA0". AREA R5; 18J07 WAS NC.					
JLV	JJ	4891	MS	11-6-81	R03
AREA D2, F2, D6 & F6, IC'S 17B, 18B, 13A & 13B WERE 19-249 F02. ADDED NOTE 2.					
KE	JJ	4900	R	11-20-81	R04
AREA K3, ADDED "05A": 18D 04 DID GO TO PRFW1 & 18D05 & 17D10					
JAH	JJ	5089	MS	8-18-82	R05

NOTES:
1. REMOVE STRAP FROM 217-5 (TP8) TO 218-5 (TP7) TO BYPASS CACHE.
2. IC PIN NUMBERS SHOWN IN PARENTHESIS REPRESENT ALTERNATE USE OF 19-249 F02.

SCALE-	NAME	TITLE	DATE
TOLERANCE XXX ± .005 XX ± .02 X ± .03 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	B. GRAY	DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC

TAS/NO 03976
DWG NO. 35-771 R05 D08
SHEET 16 OF 18

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0001	A080	3	0063	D090	11	0125			0187	ELMA31	3	0249	LMB111	8	0311	MDS150	2	0373	RD021	3	0435	TA161	16	0497	07J05	4	0559	05E06	7	0621	22E02	12	0683	20M08	14
0002	A090	3	0064	D100	11	0126	EB000	6	0188	FNPMO	14	0250	LMB121	8	0312	MDS160	2	0374	RD031	3	0436	TA181	16	0498	07K06	4	0560	05E08	7	0622	25A05	12	0684	22H06	14
0003	A100	3	0065	D110	11	0127	EB010	6	0189			0251	LMB131	8	0313	MDS170	2	0375	RDS0	9	0437	TA201	16	0499	07K05	4	0561	05E11	7	0623	25A07	12	0685	20J14	14
0004	A110	3	0066	D120	11	0128	EB020	6	0190	TP9	3	0252	LMB141	8	0314	MDS180	2	0376	RDS1	9	0438	TB001	16	0500	08J06	4	0562	06E03	7	0624	25A09	12	0686	17H10	14
0005	A120	3	0067	D130	11	0129	EB030	6	0191	LDO1	10	0253	LMB151	8	0315	MDS190	2	0377	REO	15	0439	TB021	16	0501	08J05	4	0563	06E06	7	0625	25A11	12	0687	21D04	14
0006	A130	3	0068	D140	11	0130	EB040	6	0192	LDO2	10	0254	LMB161	8	0316	MDS200	2	0378	RE1	15	0440	TB041	16	0502	08K06	4	0564	06E08	7	0626	24A05	12	0688	21D05	14
0007	A140	3	0069	D150	11	0131	EB050	6	0193	LDBY01	14	0255	LMB171	8	0317	MDS210	2	0379	REFO	13	0441	TB061	16	0503	08K05	4	0565	08D05	7	0627	24A07	12	0689	21D06	14
0008	A150	3	0070	D160	11	0132	EB060	6	0194	LDBY11	14	0256	LMB181	8	0318	MDS220	2	0380	REFOA	13	0442	TB081	16	0504	09J06	4	0566	08D06	7	0628	24A09	12	0690	21D07	14
0009	A160	3	0071	D170	11	0133	EB070	6	0195	LDBY21	14	0257	LMB191	8	0319	MDS230	2	0381	REF1	13	0443	TB101	16	0505	09J05	4	0567	10D05	7	0629	24A11	12	0691	16D05	14
0010	A170	3	0072	D180	11	0134	EB080	6	0196	LDBY31	14	0258	LMB201	8	0320	MDS240	2	0382	REL1	14	0444	TB121	16	0506	09K06	4	0568	10D06	7	0630	23A05	12	0692	22F08	14
0011	A180	3	0073	D190	11	0135	EB090	6	0197	LDGPI	14	0259	LMB211	8	0321	MDS250	2	0383	REQI	13	0445	TB141	16	0507	09K05	4	0569	12D05	7	0631	23A07	12	0693	02F06	14
0012	A190	3	0074	D200	11	0136	EB100	6	0198	LDOD1	16	0260	LMB221	8	0322	MDS260	2	0384	RFA01	13	0446	TB161	16	0508	10J06	4	0570	12D06	7	0632	23A09	12	0694	01C06	14
0013	A200	3	0075	D210	11	0137	EB110	6	0199	LMBY0	15	0261	LMB231	8	0323	MDS270	2	0385	RFA11	13	0447	TB080	16	0509	10J05	4	0571	06D05	7	0633	23A11	12	0695	03C06	14
0014	A210	3	0076	D220	11	0138			0200	LMBY1	15	0262	LMB241	9	0324	MDS280	2	0386	RFA21	13	0448	TAA020	16	0510	10K06	4	0572	06D06	7	0634	22A05	12	0696	02C06	14
0015	A220	3	0077	D230	11	0139	EB120	6	0201	LOE1	16	0263	LMB251	9	0325	MDS290	2	0387	RFA31	13	0449	TAA001	16	0511	10K05	4	0573	05H01	7	0635	22A07	12	0697	04C06	14
0016	A230	3	0078	D240	11	0140	EB130	6	0202	GP000	7	0264	LMB261	9	0326	MDS300	2	0388	RFA41	13	0450	TAA121	16	0512	11J06	5	0574	03J03	7	0636	25M04	12	0698	03C08	14
0017	A240	3	0079	D250	11	0141	EB140	6	0203	GP010	7	0265	LMB271	9	0327	MDS310	2	0389	RFA51	13	0451	TBB040	16	0513	11J05	5	0575	03F08	7	0637	25M07	12	0699	19C06	15
0018	A250	3	0080	D260	11	0142	EB150	6	0204	GP020	7	0266	LMB281	9	0328	MREO	9	0390	RFA61	13	0452	TBB101	16	0514	11K06	5	0576	13D09	7	0638	24M04	12	0700	18C06	15
0019	A260	3	0081	D270	11	0143	EB160	6	0205	GP030	7	0267	LMB291	9	0329	MREFO	9	0391	RFA71	13	0453	TBB141	16	0515	11K05	5	0577	16C02	7	0639	24M07	12	0701	15J11	15
0020	A270	3	0082	D280	11	0144	EB170	6	0206	GP040	7	0268	LMB301	9	0330	MWA001	9	0392	RFQ1	15	0454	TAA021	16	0516	12J06	5	0578	42X10	7	0640	24M09	12	0702	19C11	15
0021	A280	3	0083	D290	11	0145	EB180	6	0207	GP050	7	0269	LMB311	9	0331	MWA011	9	0393	RFWI	14	0455	TELO	14	0517	12J05	5	0579	16C07	7	0641	24M12	12	0703	17C12	15
0022	A290	3	0084	D300	11	0146	EB190	6	0208	GP060	7	0270	LMB321	9	0332	MWEO	9	0394	RDSTI	14	0456	TEL1	14	0518	12K06	5	0580	42X07	7	0642	21C08	12	0704	15E03	15
0023	A300	3	0085	D310	11	0147	EB200	6	0209	GDD1	15	0271	LMB331	9	0333	MX021	3	0395	RSELO	13	0457	UP000	9	0519	12K05	5	0581	16C10	7	0643	18F06	12	0705	18C08	15
0024	A310	3	0086	D000A	15	0148	EB210	6	0210	GMERI	15	0272	LMB341	9	0334	MX031	3	0396	RSTO	14	0458	UP010	9	0520	13J06	5	0582	42X04	7	0644	MISS1	12	0706	15A10	15
0025	A161	10	0087	D020A	15	0149	EB220	6	0211	GMVF0	9	0273	LMB351	9	0335	NCEO	9	0397	RST1	14	0459	UP020	9	0521	13J05	5	0583	42X00	7	0645	25D02	12	0707	14J06	15
0026	A171	10	0088	D160A	15	0150	EB230	6	0212	HIT1	12	0274	LMB361	9	0336	NCLR1	14	0398	RURE1	14	0460	UP030	9	0522	13K06	5	0584	42X01	7	0646	25D04	12	0708	14J08	15
0027	A181	10	0089	DA00	5	0151	EB240	6	0213	LMA080	3	0275	LMB371	9	0337	NEO	15	0399	SO01	10	0461	UP040	9	0523	13K05	5	0585	15C03	7	0647	25D06	12	0709	05K08	15
0028	A191	3	0090	DA10	5	0152	EB250	6	0214	LMA090	3	0276	LMB381	9	0338	NE1	15	0400	SO11	10	0462	UP050	9	0524	03F02	5	0586	42X16	7	0648	25D08	12	0710	18J06	15
0029	A301	14	0091	DA20	5	0153	EB260	6	0215	LMA100	3	0277	MBO	13	0339	NPMO	14	0401	SO21	10	0463	UP060	9	0525			0587	09M14	7	0649	MISB1	12	0711	23M08	15
0030	AD01	10	0092	DA30	5	0154	EB270	6	0216	LMA110	3	0278	MBOA	13	0340	NBALI	12	0402	SO31	10	0464	UCEO	7	0526	11E03	6	0588	09K10	9	0650	MISA1	12	0712	18H06	15
0031	AD11	10	0093	DA40	5	0155	EB280	6	0217	LMA120	3	0279	MB1	13	0341	NVMO	9	0403	SO41	10	0465	UCE1	7	0527	11E06	6	0589	PSU		0651	25D10	12	0713	18K05	15
0032	AD21	10	0094	DB00	5	0156	EB290	6	0218	LMA130	3	0280	MB1A	13	0342	ODD1	16	0404	SO51	10	0466	UDD0	15	0528	11E08	6	0590	19M10	9	0652	25D12	12	0714	04J08	15
0033	AD31	10	0095	DB10	5	0157	EB300	6	0219	LMA140	3	0281	MB1B	13	0343	MATE0	14	0405	SO61	10	0467	UDD1	15	0529	11E11	6	0591	17H02	10	0653	24D02	12	0715	04J06	15
0034	BMC10	9	0096	DB20	5	0158	EB310	6	0220	LMA150	3	0282	MB1C	13	0344	MATDO	14	0406	SDYI	14	0468	UFP1	16	0530	12E03	6	0592	15H06	10	0654	24D04	12	0716	17J08	15
0035	BMVF0	9	0097	DB30	5	0159	EPB000	7	0221	LMA160	3	0283	MC10	16	0345	PSFWO	14	0407	SCLK1	9	0469	VALO	12	0531	12E06	6	0593	05K05	10	0655	24D06	12	0717	23D06	15
0036	BSCLR0	9	0098	DB40	5	0160	EPB010	7	0222			0284	MCC0	9	0346	PSHWO	14	0408	SCLK1A	9	0470	VAL1	12	0532	12E08	6	0594	15E06	10	0656	24D08	12	0718	16E08	15
0037	BYP0	16	0099	DB50	5	0161	EPB020	7	0223	LMA170	3	0285	MEO	10	0347	P000	4	0409	SCLK0A	10	0471	WA000	3	0533	12E11	6	0595	23M06	10	0657	24D10	12	0719	05C06	14
0038	BYP1	16	0100	DB60	5	0162	EPB030	7	0224	LMA180	3	0286	ME1	15	0348	P010	4	0410	SCLR1B	13	0472	WA001	3	0534	13E03	6	0596	16H06	10	0658	24D12	12	0720	15E11	14
0039	CAEN0	16	0101	DB70	5	0163	EPB040	7	0225	LMA190	3	0287	MEA000	9	0349	P020	4	0411	SCLR0	13	0473	WA010	3	0535	13E06	6	0597	19M04	10	0659	23D02	12	0721	19E13	14
0040	CAEN1	16	0102	DC00	5	0164	EPB050	7	0226	LMA200	3	0288	MEA010	9	0350	P030	4	0412	SCLR0B	13	0474	WA011	3	0536	13E08	6	0598	16H08	10	0660	23D04	12	0722	15J08	14
0041	CAR1	13	0103	DC10	5	0165	EPB060	7	0227	LMA210	3	0289	MEA020	9	0351	P040	5	0413	SCLR0C	13	0475	WC0	3	0537	13E11	6	0599	17H04	10	0661	05A67	13	0723	15D06	14
0042	CAWE0	11	0104	DC20	5	0166	EA0	16	0228	LMA220	3	0290	MEA030	9	0352	P050	5	0414	SFWO	14	0476	WCC0	3	0538	14E03	6	0600	18K12	10	0662	05A63	13	0724	15E08	14
0043	CB011	3	0105	DC30	5	0167	EDO	15	0229	LMA230	3	0291	MERO	5	0353	P060	5	0415	SFW1	14	0477	WCC1	3	0539	14E06	6	0601	23K03	11	0663	06A02	13	0725	16D06	14
0044	CB021	3	0106	DC40	5	0168	EDI	15	0230	LMA240	3	0292	MER1	5	0354	PER1	11	0416	SHIFT1	10	0478	WDENO	3	0540	14E08	6	0602	23K06	11	0664	09A06	13	0726	18E08	14
0045	CB031	3	0107	DC50	5	0169	ELO	14	0231	LMA250	3	0293	MIS1	12	0355	PFSDO	9	0417	SHW1	14	0479	WE0	15	0541	14E11	6	0603	23K08	11	0665	07A09	13	0727	17F06	14
0046	CH121	12	0108	DC60	5	0170	ELDUA0	10	0232	LMA260	3	0294	MRDS0	9	0356	PFSD1	13	0418	SPW0	14	0480	WE1	15	0542	07E03	6	0604	23K11	11	0666	09B08	13	0728	17E05	14
0047	CLKOD	10	0109	DC70	5	0171	ELDUA1	10	0233	LMA270	3	0295	MDS000	2	0357	PRFW0	14	0419	SPW1	14	0481	WRT0	3	0543	07E06	6	0605	23J03	11	0667	09A71	13	0729	22H05	14
0048	CLKIC	9	0110	DERR0	5	0172	ELST1	14	0234	LMA280	3	0296	MDS010	2	0358	PRFW1	14	0420	STB0	13	0482	WRT0A	3	0544	07E08	6	0606	23J06	11	0668	10A06	13	0730	18F05	15
0049	CLKID	9	0111	DHW0	3	0173	END1	13	0235	LMA290	3	0297	MDS020	2	0359	PSBY0	14	0421	STB1	13	0483	WRT1	14	0545	07E11	6	0607	23J08	11	0669	09A08	13	0731	14J03	15
0050	CLR0	13	0112	DMHW0	3	0174	ER0	13	0236	LMA300	3	0298	MDS030	2	0360	PSEL1	14	0422	TA000	16	0484	XRP1	15	0546	08E03	6	0608	23J11	11	0670	08B12	13	0732	19J08	15
0051	CLROB	15	0113	DPR1	13	0175			0237	LMA310	8	0299	MDS040	2	0361	PSELIA	3	0423	TA080	16	0485	XRP2	16	0547	08E06	6	0609	23K01	11	0671	06A14	13	0733	16J06	15
0052	CLTB1	16	0114	DREL1	14	0176	ELA040	10	0238	LMB001	8	0300	MDS050	2	0362	QWE0	16	0424	TA120	16	0486	21R19	9	0548	08E08	6	0610	22J06	11	0672	06A01	13	0734	20K08	15
0053	CPER1	16	0115	DRFW0	14	0177	ELA050	10	0239	LMB011	8	0301	MDS060	2	0363	QWM0	16	0425			0487	03J06	2	0549	08E11	6	0611	24J06	11	0673	06A14	13	0735	16J07	15
0054	D000	11	0116	DRFW1	14	0178	ELA060	10	0240	LMB021	8	0302	MDS070	2	0364	QWM1	16	0426	TA160	16	0488	18R03	3	0550	09E03	6	0612	25J06	11	0674	11B15	13	0736	16J09	15
0055	D010	11	0117	DDSFW0	14	0179	ELA070	10	0241	LMB031	8	0303			0365	RCARO	10	0427	TA001	16	0489	18R06	3	0551	09E06	6	0613	12A07	11	0675	09A03	13	0737	19C03	15
0056	D020	11	0118	DDSHW0	14	0180	ELA080	10	0242	LMB041	8	0304	MDS080	2	0366	RCLC0	9	0428	TA021	16	0490	23F08	3	0552	09E08	6	0614	42X19	11	0676	22M06	13	0738	15A13	15
0057	D030	11	0119	DUA0	15	0181	ELA090	10	0243	LMB051	8	0305	MDS090	2	0367	RCLC1	9	0429	TA041	16	0491	22H03	3	0553	09E11	6	0615	03J11	11	0677			0739	19A08	16
0058	D040	11	0120	DUA1	15	0182	ELA100	10	0244	LMB061	8	0306	MDS100	2	0368	RCLR0	13	0430	TA061	16	0492	18R11	3	0554	10E03	6	0616	03J08	11	0678	15B08	13	0740	14A03	16
0059	D050	11	0121	DSHW0	14	0183	ELA110	10	0245	LMB071	8	0307	MDS110	2	0369	RCLR1	13	0431	TA081	16	0493	24F05	3	0555	10E06	6	0617	14A06	12	0679	08B06	13	0741	17C08	16
0060	D060	11	0122	DSFW0	14	0184	ELMA01	3	0246	LMB081	8	0308	MDS120	2	0370	RCT0	13	0432	TA101	16	0494	25H08	3	0556	10E08	6	0618	22A02	12	0680	20M06	14	0742	15H08	16
0061	D070	11	0123	20J14	14	0185	ELMA11	3	0247	LMB091	8	0309	MDS130	2	0371	RCT1	13	0433	TA121	16	0495	21E11	3	0557	10E11	6	0619	22B02	12	0681	19E01	14	0743	12B10	16
0062	D080	11	0124	MARSTO	14	0186	ELMA21	3	0248	LMB101	8	0310	MDS140	2	0372	RD011	3	0434	TA141	16	0496	07J06	4	0558	05E03	7	0620	22C02	12	0682	22D08	14	0744	16D07	16

NOTES

REVISIONS

NET #189 WAS SPEC AS FNPMI SHT 14.

NET #589 WAS SPEC AS 22D12 SHT 9.

V.P.	AV	4592		11-5-80	R01

DLL'ED EWE1 (NET 175) SHT. 15.

JAH	AV	4767	MS	10-13-81	R02

NET 119 WAS DAO. NET 644 WAS 52X21. NET 649 WAS 21A19. NET 650 WAS 21B19.

JLV	AV	4891	MS	11-6-81	R03

UNLESS OTHERWISE SPECIFIED

SCALE:

TOLERANCE:

DIMENSIONS ARE IN INCHES

.XXX ±.005 .X ±.03
.XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
V. PERRI	E. JOHNSON	DES/DFT	4-24-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division,
Oceanport, N.J. 07757

TITLE

LBC

TASK 03976

SHT 17-18

DWG 35-771 R03 D08

BRUNING 44-13"-X-2"-S

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0745	16E03	16	0807	GND16J		0869			0931			0993			1055			1117			1179			1241			1303			1365			1427		
0746	14B11	16	0808	GND20D		0870			0932			0994			1056			1118			1180			1242			1304			1366			1428		
0747	14B08	16	0809	GND08A		0871			0933			0995			1057			1119			1181			1243			1305			1367			1429		
0748	19B08	16	0810	13C06	2	0872			0934			0996			1058			1120			1182			1244			1306			1368			1430		
0749	18A10	16	0811	GND10C		0873			0935			0997			1059			1121			1183			1245			1307			1369			1431		
0750	12C08	16	0812	06R08	7	0874			0936			0998			1060			1122			1184			1246			1308			1370			1432		
0751	12C06	16	0813	04J11	7	0875			0937			0999			1061			1123			1185			1247			1309			1371			1433		
0752	21F06	16	0814	TB02IA	15	0876			0938			1000			1062			1124			1186			1248			1310			1372			1434		
0753	23M11	16	0815	42X13	13	0877			0939			1001			1063			1125			1187			1249			1311			1373			1435		
0754	18K71	16	0816	52X19	13	0878			0940			1002			1064			1126			1188			1250			1312			1374			1436		
0755	16B08	16	0817			0879			0941			1003			1065			1127			1189			1251			1313			1375			1437		
0756	19M01	16	0818	MATRSR0	3	0880			0942			1004			1066			1128			1190			1252			1314			1376			1438		
0757	18D08	16	0819	MATRSD0	3	0881			0943			1005			1067			1129			1191			1253			1315			1377			1439		
0758	P5U09A		0820	DMARS0	3	0882			0944			1006			1068			1130			1192			1254			1316			1378			1440		
0759	P5U07A		0821	RDSD0	9	0883			0945			1007			1069			1131			1193			1255			1317			1379			1441		
0760	P5U07B		0822	CLK0E	9	0884			0946			1008			1070			1132			1194			1256			1318			1380			1442		
0761	P5U09B		0823	07C11	12	0885			0947			1009			1071			1133			1195			1257			1319			1381			1443		
0762			0824	UCECLR0	14	0886			0948			1010			1072			1134			1196			1258			1320			1382			1444		
0763	GND20R		0825	NCAR1	13	0887			0949			1011			1073			1135			1197			1259			1321			1383			1445		
0764	GND19R		0826	07C06	13	0888			0950			1012			1074			1136			1198			1260			1322			1384			1446		
0765	GND23F		0827	08C01	13	0889			0951			1013			1075			1137			1199			1261			1323			1385			1447		
0766	GND07K		0828	08A08	13	0890			0952			1014			1076			1138			1200			1262			1324			1386			1448		
0767	GND08K		0829	RFANT1	13	0891			0953			1015			1077			1139			1201			1263			1325			1387			1449		
0768	GND09K		0830	09R08	13	0892			0954			1016			1078			1140			1202			1264			1326			1388			1450		
0769	GND10K		0831	19F06	14	0893			0955			1017			1079			1141			1203			1265			1327			1389			1451		
0770	GND11K		0832	CCAR1	13	0894			0956			1018			1080			1142			1204			1266			1328			1390			1452		
0771	GND12K		0833	TADEIA	14	0895			0957			1019			1081			1143			1205			1267			1329			1391			1453		
0772	GND13K		0834	07M11	10	0896			0958			1020			1082			1144			1206			1268			1330			1392			1454		
0773	GND04D		0835	05M01	13	0897			0959			1021			1083			1145			1207			1269			1331			1393			1455		
0774	GND21R		0836	06M03	13	0898			0960			1022			1084			1146			1208			1270			1332			1394			1456		
0775	GND07M		0837	MERR1	3	0899			0961			1023			1085			1147			1209			1271			1333			1395			1457		
0776	GND15F		0838	EWE0	15	0900			0962			1024			1086			1148			1210			1272			1334			1396			1458		
0777	GND16F		0839	14CP5	3	0901			0963			1025			1087			1149			1211			1273			1335			1397			1459		
0778	GND05K		0840	14CGND	3	0902			0964			1026			1088			1150			1212			1274			1336			1398			1460		
0779	GND21K		0841	18A13	15	0903			0965			1027			1089			1151			1213			1275			1337			1399			1461		
0780	GND22K		0842	DUA0A	9	0904			0966			1028			1090			1152			1214			1276			1338			1400			1462		
0781	GND24K		0843	BPMS1	15	0905			0967			1029			1091			1153			1215			1277			1339			1401			1463		
0782	GND06J		0844	EA1	9	0906			0968			1030			1092			1154			1216			1278			1340			1402			1464		
0783	GND17J		0845	17BGND	16	0907			0969			1031			1093			1155			1217			1279			1341			1403			1465		
0784	GND18J		0846	18BGND	16	0908			0970			1032			1094			1156			1218			1280			1342			1404			1466		
0785	GND01H		0847	13AGND	16	0909			0971			1033			1095			1157			1219			1281			1343			1405			1467		
0786	GND12H		0848	13BGND	16	0910			0972			1034			1096			1158			1220			1282			1344			1406			1468		
0787	GND18D		0849			0911			0973			1035			1097			1159			1221			1283			1345			1407			1469		
0788	GND17D		0850			0912			0974			1036			1098			1160			1222			1284			1346			1408			1470		
0789	GND16B		0851			0913			0975			1037			1099			1161			1223			1285			1347			1409			1471		
0790	GND12A		0852			0914			0976			1038			1100			1162			1224			1286			1348			1410			1472		
0791	GND16D		0853			0915			0977			1039			1101			1163			1225			1287			1349			1411			1473		
0792	GND13D		0854			0916			0978			1040			1102			1164			1226			1288			1350			1412			1474		
0793	GND22A		0855			0917			0979			1041			1103			1165			1227			1289			1351			1413			1475		
0794	GND22B		0856			0918			0980			1042			1104			1166			1228			1290			1352			1414			1476		
0795	GND22C		0857			0919			0981			1043			1105			1167			1229			1291			1353			1415			1477		
0796	GND22E		0858			0920			0982			1044			1106			1168			1230			1292			1354			1416			1478		
0797	GND25K		0859			0921			0983			1045			1107			1169			1231			1293			1355			1417			1479		
0798	GND25R		0860			0922			0984			1046			1108			1170			1232			1294			1356			1418			1480		
0799	GND17E		0861			0923			0985			1047			1109			1171			1233			1295			1357			1419			1481		
0800	GND21D		0862			0924			0986			1048			1110			1172			1234			1296			1358			1420			1482		
0801	GND21A		0863			0925			0987			1049			1111			1173			1235			1297			1359			1421			1483		
0802	GND21B		0864			0926			0988			1050			1112			1174			1236			1298			1360			1422			1484		
0803			0865			0927			0989			1051			1113			1175			1237			1299			1361			1423			1485		
0804	GND24M		0866			0928			0990			1052			1114			1176			1238			1300			1362			1424			1486		
0805	GND25M		0867			0929			0991			1053			1115			1177			1239			1301			1363			1425			1487		
0806	GND26R		0868			0930			0992			1054			1116			1178			1240			1302			1364			1426			1488		

NOTES

BRUNING 44-131 4C579

REVISIONS

NETS #833 & 834 WERE NOT SPEC.					
J&P	JV	4542		11-5-80	R01
ADDED NETS 835 & 836:					
JAH	JV	4743	MS	7-21-81	R02
ADDED NEW NETS 836-841					
JAH	JV	4764	MS	10-13-81	R03
ADDED NEW NETS 842-844.					
JLV	JV	4891	MS	11-6-81	R04
ADDED NEW NETS 845-848.					
KR	JV	4900	R	11-20-81	R05 X

UNLESS OTHERWISE SPECIFIED

SCALE: NONE	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME DES/DFT		TITLE	DATE
V. PERRI	B. LUSK	DES/DFT	4-22-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

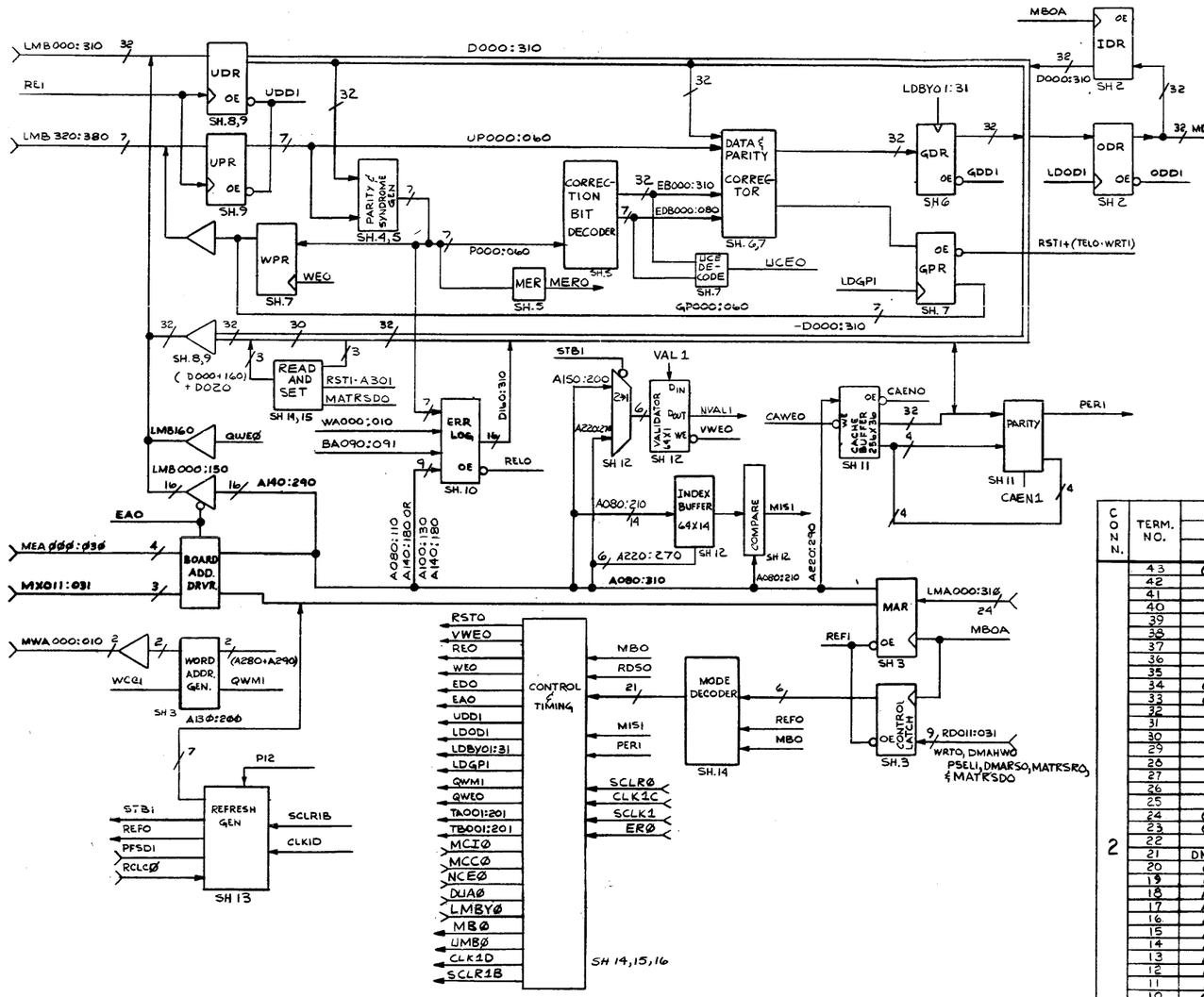
Computer Systems Division
Oceanport, N.J. 07757

TITLE

LBC

TASK 03976	SHT
DWG 35-771 R05 D08	18-18

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757



TEST POINTS

#	MNEMONIC	SHT.
TP1	GND	5
TP2	DERRO	5
TP3	GND	12
TP4	TP4	12
TP5	MBIC	13
TP6	TP6	13
TP7	GND	16
TP8	BYP1	16
TP9	TP9	3
TP10	GND	3
TP11	OER08	7
TP12	GND	7

TEST POINTS (CONT)

#	MNEMONIC	SHT
TP13	CSTRIN00	13
TP14	CSTRIN10	13
TP15	RFCTLD0	13
TP16	TAST0	16
TPA	PFSD1	13
TPB	PFSD1A	13
TPC	TGA211	12
TPD	TGA201	12
TPE	TGA191	12
TPF	TGA181	12
TPG	TGA171	12
TPH	TGA161	12
TPI	TGA151	12
TPJ	TGA141	12
TPK	TGA131	12
TPL	TGA121	12
TPM	TGA111	12
TPN	TGA101	12
TPO	TGA091	12
TPP	TGA081	12

BACK PANEL MAP

CONN.	TERM. NO.	ROW 1	ROW 2	ROW 1	ROW 2	TERM. NO.
2	43	GND	GND	GND	GND	43
	42				SCLR0	42
	41					41
	40					40
	39					39
	38					38
	37					37
	36			GND	GND	36
	35					35
	34	GND	GND	GND	GND	34
	33	GND	GND	GND	GND	33
	32					32
	31					31
	30					30
	29					29
	28					28
	27					27
	26					26
	25					25
	24	GND	GND	GND	GND	24
	23	GND	GND	GND	GND	23
	22		MATRSDØ	NVMØ		22
	21	DMARSØ	MATRSRØ	CLK1C	SCLK1	21
	20	GND	GND	GND	GND	20
	19	GND	GND	GND	GND	19
	18	MDS30Ø	MDS31Ø	NCEØ	GMVFØ	18
	17	MDS28Ø	MDS29Ø	DUAØ	PSEL1	17
	16	MDS26Ø	MDS27Ø	DMAHWØ	LMBYØ	16
	15	MDS24Ø	MDS25Ø	ERØ	WRTØ	15
	14	MDS22Ø	MDS23Ø	LMA30Ø	LMA31Ø	14
	13	MDS20Ø	MDS21Ø	LMA28Ø	LMA29Ø	13
	12	MDS18Ø	MDS19Ø	LMA26Ø	LMA27Ø	12
	11	MDS16Ø	MDS17Ø	LMA24Ø	LMA25Ø	11
	10	GND	GND	GND	GND	10
	09	GND	GND	GND	GND	09
	08	MDS14Ø	MDS15Ø	LMA22Ø	LMA23Ø	08
	07	MDS12Ø	MDS13Ø	LMA20Ø	LMA21Ø	07
	06	MDS10Ø	MDS11Ø	LMA18Ø	LMA19Ø	06
	05	MDS08Ø	MDS09Ø	LMA16Ø	LMA17Ø	05
	04	MDS06Ø	MDS07Ø	LMA14Ø	LMA15Ø	04
	03	MDS04Ø	MDS05Ø	LMA12Ø	LMA13Ø	03
	02	MDS02Ø	MDS03Ø	LMA10Ø	LMA11Ø	02
	01	MDS00Ø	MDS01Ø	LMA08Ø	LMA09Ø	01
	00	GND	GND	GND	GND	00

FUNCTIONAL VARIATION TABLE

F02	35-806 R05	F02	W/O CACHE	AS SHOWN ON SHT'S 2, 11&12
F01	35-806 R05	F01	W/CACHE	AS SHOWN ON SHT'S 2, 11&12

REVISIONS

PRE PRODUCTION APPROVAL	DEV	INIT	DATE

SHT 2,3,9,13,15,17,&18 WERE SPEC. AS REV R00. REV LEVEL OF BOARDS IN VARIATION TABLE WERE R00.

R3	VV	4963		8-18-81	R01

RELEASED FOR PRODUCTION
ENG. _____ DATE _____

REVISED SHTS 1,2 & 18

4th	W	4855	R	11-11-81	R02	X

REVISED SHTS 1, 16, 18.

KR	VV	4900	Z	12-2-81	R03	X

AREA K9 47-022 WAS 47-004. AREA E9 35-806 F01 & F02 WERE R02. REVISED SHTS 1,2,9,12,14,15, 16, 17 & 18

KR	VV	4909	R	1-19-82	R04	X

REV'D SHTS 1, 2, 10, 13, 16 & 18 · 35-806 F01 & F02 WERE R03.

4th	W	5089	ms	8-20-82	R05	

(207-6) A	(206-6) B	13
(216-5) TP9	(215-5) TP10	3
FROM	TO	SHT LOC.
STRAPPING INFO		

REVISIONS	5	4	1	0	0	0	0	0	2	1	0	1	2	1	2	3	2	5
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

NOTE - SEE SHT 2 FOR TABLE OF SPARES.

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REV LEVEL.

USED IN MANUAL 47-022

SCALE – | TOLERANCE: XXX ±.005, XX ±.02, X ±.03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

E.GREENSTEIN	TEST	
R. CERO	DRAFT	12-10-80
M. MANGIONE	CHK	9-11-81
P. BARKER	ENGR	9-11-81
P. OBROCK	QC	9-11-81
	MGR	9-11-81

TITLE SCHEMATIC
LOCAL BANK CONTROLLER (8MB CAPABILITY)
SIZE 03183
DWG NO. 35-806 R05 D08
SHEET OF 1 — 18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J 07757

REVISIONS				
TABLE OF SPARES; CIM WAS NOT SPEC., 18Q-13, A 19-236 WAS DELETED, 17F-08 A 19-126 WAS DELETED, 06C SPARE OUTPUT 03 FOR WIRE DELETED.	RS	VJP	4763	8-18-81 R01
DELETED 10A, 08 & 11 FROM SPARE GATES TABLE	JW	JV	4855	R 11-11-81 R02
DELETED 06C11, 19-235 FROM SPARE GATE LIST.	KR	JV	4909	MS 1-19-82 R03
DELETED 05A 8/9, 19-063 FROM SPARE LIST.	JW	JV	5089	MS 8-20-82 R04

PROCESSOR DATA BUS

MDS000 101-2
MDS010 201-2
MDS020 102-2
MDS030 202-2
MDS040 103-2
MDS050 203-2
MDS060 104-2
MDS070 204-2
MDS080 105-2
MDS090 205-2
MDS100 106-2
MDS110 206-2
MDS120 107-2
MDS130 207-2
MDS140 108-2
MDS150 208-2
MDS160 111-2
MDS170 211-2
MDS180 112-2
MDS190 212-2
MDS200 113-2
MDS210 213-2
MDS220 114-2
MDS230 214-2
MDS240 115-2
MDS250 215-2
MDS260 116-2
MDS270 216-2
MDS280 117-2
MDS290 217-2
MDS300 118-2
MDS310 218-2
MB0A 13N7

01K 19-232 ODR
00K 19-232 OCT F/F
03K 19-232 OCT F/F
04K 19-232 OCT F/F
01R 19-232 OCT F/F
00R 19-232 OCT F/F
07R 19-232 OCT F/F
08R 19-232 OCT F/F

ODD1 16N4
LDOD1 16K9

OUTPUT DATA REGISTER

02R 21-025 F01 15 PIN DIP 1K TO COM.
D9 D070 01 — 16 P5
B9 D000 02 — 15 D080 E9
D9 D060 03 — 14 D140 F9
B9 D010 04 — 13 D090 E9
C9 D050 05 — 12 D130 F9
B9 D020 06 — 11 D100 E9
C9 D040 07 — 10 D120 F9
C9 D030 08 — 09 D110 F9

13C 19-126 SG
02 TA061 16D5
03
04 SFW1 14H4
05 TA101 16D5
06
03J 19-236 5A 04 05
WDENO 14M9
MDS160 10N5

05R 21-025 F01 15 PIN DIP 1K TO COM.
J9 D240 01 — 16 P5
L9 D310 02 — 15 D160 G9
K9 D280 03 — 14 D220 H9
K9 D300 04 — 13 D170 G9
K9 D260 05 — 12 D210 H9
K9 D290 06 — 11 D180 G9
K9 D270 07 — 10 D200 H9
K9 D280 08 — 09 D190 H9

F9 D150 17 — 00K 1K — 65 P5
J9 D230 16 — 00K 1K — 66 P5

INPUT DATA REGISTER

25F	19-124	03,06
23M	19-055	06
23D	19-154	08,10,12
22D	19-057	06,08,10,12
20H	19-055	06
20B	19-057	06,10,12
20A	19-057	06
19M	19-234	10,
19H	19-058	12
19A	19-059	12
17A	19-236	11
01M	19-234	04,10,13
15C	19-131	7/6, 10/11, 15/14
12R	19-163	06,08,11
10A	19-163	03
09R	19-055	08,11
12B	19-057	04
09A	19-160	11
06A	19-190	13
05H	19-234	04,10,13
05F	19-234	13
05E	19-127	11
03F	19-057	04,10,12
02A	19-063	8/9
17A	19-057	04
01F	19-241	06
REF. DESIGN.	PART NUMBER	SPARE OUTPUTS

TABLE OF SPARES

INPUT OUTPUT DATA REGISTER

NOTES 1. DEPOPULATE IC'S & DISCRETES MARKED WITH AN ASTERISK (*) FOR F01 VARIATION.

SCALE— | TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
RSTINE	DRAFT	12-10-80
	CHK	
	ENGR	

TITLE SCHEMATIC
LBC
8MB CAPABILITY
TASK NO. 03183 SHEET OF 2—18
DWG NO 35-806 R04 Dash

PROCESSOR ADDRESS BUS

REVISIONS					
AREA M4, IC 17F08 WAS NOT SPECIFIED. IN AREA H9 MNEMONIC OF 23F-05 WAS ME1					
DS	WJP	4763		8-18-81	R01

NOTES 1. STRAP 215-5 (TP10) TO 8MB SYSTEM. FOR SYSTEMS LARGER THAN 8MB, REMOVE THE STRAP.

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
LBC (8MB CAPABILITY)

DRAFTER	
Q STINE	
DATE	TASK 03183 / SHT
12-13-80	DWG 35-806 R01 D08 / 3 - 18

PERKIN-ELMER
Computer Systems Division
Oceanport N J 07757

REVISIONS

15KΩ D∅∅∅A
6N1,G1 D∅1∅
15N5,G5 D∅2∅A
6F3,G7 D21∅
6N2,G1 D∅4∅
6N2,G5 D∅5∅
6N2,G2 D∅G∅
15KΩ D1G∅A
6N6,G6 D13∅

07J
19-223
9 BIT EVEN/ODD PARITY GEN/CHK
A

ODD
EVEN

6F6 D29∅
6F6 D24∅
6F7,G4 D3∅∅
6N6 D∅8∅
9H8 UP∅∅∅

07K
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

ODD/ODD
EVEN/EVEN
ODD

07H
19-126
STTL

P∅∅∅ 5H5,7D6,10A7

6N2,G1 D∅3∅
6N2,G2 D∅7∅
6F2 D17∅
6N6 D∅9∅
6N6,G3 D12∅
6F2,G3 D2∅∅

08J
19-223
9 BIT EVEN/ODD PARITY GEN/CHK
A

6F3,G7 D22∅
6N7,G6 D14∅
6F6 D25∅
9H8 UP1∅

08K
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

ODD/EVEN
EVEN/ODD
EVEN

P∅1∅ 5H5,7D6,10A7

A5 D∅3∅
A1 D∅1∅
A2 D∅4∅
A6 D∅7∅
A2 D∅G∅
6F2 D18∅
6N7 D15∅
6N6 D1∅∅
A6 D2∅∅

09J
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

ODD
EVEN

6G3 D23∅
A6 D12∅
6F6 D26∅
6F7 D31∅
A3 D3∅∅
9H9 UP∅2∅

09K
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

ODD/ODD
EVEN/EVEN
ODD

09H
19-126
STTL

P∅2∅ 5H5,7D6,10A7

A1 D∅2∅A
A2 D∅5∅
6N6 D11∅
A3 D13∅
A7 D14∅
6F2 D19∅

10J
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

ODD/EVEN
EVEN/ODD
EVEN

6F6 D27∅
A2 D21∅
A7 D22∅
9H9 UP∅3∅

10K
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

P∅3∅ 5G8,7D7,10A8

PARITY GENERATOR

SCALE –
NAME RSTINE
CHK
ENGR
TITLE : SCHEMATIC
LBC (BME CAPABILITY)
SIZE 03183
DWG NO 30-806 D08
SHEET 4 OF 18

BRUNING 44-231 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

11J 19-223 9 BIT EVEN/ODD PARITY GEN/CHK
11K 19-223 9 BIT EVEN/ODD PARITY GEN/CHK
12J 19-223 9 BIT EVEN/ODD PARITY GEN/CHK
12K 19-223 9 BIT EVEN/ODD PARITY GEN/CHK
11H 19-126 STTL
EVEN
13J 19-223 9 BIT EVEN/ODD PARITY GEN/CHK
13K 19-223 9 BIT EVEN/ODD PARITY GEN/CHK
13H 19-126 STTL
08H 19-129 3 TO 8 DECODER
10H 19-129 3 TO 8 DECODER
12H 19-129 3 TO 8 DECODER
06J 19-082 SGO
06H 19-082 SGO
03F 19-057 SG

NOTES;
1. TO DISABLE ERROR CORRECTION CONNECT 224-5 TO 223-5.

MEMORY ERROR AND PARITY GENERATOR

SCALE
DRAWN
CHK
ENGR
DATE
TITLE: SCHEMATIC
LEC (8MB CAPABILITY)
TAB NO 03183
DWG NO 35 806 D08
SHEET OF 5 — 18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

DATA LATCH

03E 19-232 A

03	D16Ø	A1, 8R7, 10H1, 11J3 2G9, 15G6	
04	D17Ø	A2, 4A6, 5A3, 8R7, 10L1, 11J3, 2G9	
07	D18Ø	A2, 4G2, 5A2, 8R7 10H1, 11L3, 2G9	
08	D19Ø	A3, 4G6, 5A3, 8R8, 10L1, 11J3, 2H9	
13	D2ØØ	A3, 4A4, 5F3, 8R7, 10H2, 11J3, 2H9	
14	D21Ø	A4, 4A2, 5F4, 8R7, 10L1, 11J3, 2H9	
17	D22Ø	A4, 4A7, 5F2, 8R8 10H2, 11J3, 2H9	
18	D23Ø	A5, 4G3, 5F2, 8R6, 10L2, 11J3, 2H9	

LDBY21 14M8
GDD1 N5
LDBY31 14M9

04E 19-232

02	D24Ø	A6, 4A3, 5A5, 9E5, 10H2, 11J1, 2K9
05	D25Ø	A6, 4A8, 5A5, 9E6, 10L2, 11J1, 2K9
06	D26Ø	A7, 4G3, 5A7, 9E6, 10H2 11J1, 2K9
09	D27Ø	A7, 4G7, 5A7, 9E7, 10L2 11J1, 2K9
12	D28Ø	A8, 5A4, 9E5, 10H2, 11J1, 2K9
15	D29Ø	A8, 4A3, 5A8, 9E6, 10L3, 11J1, 2K9
16	D3ØØ	A9, 4A3, 5A8, 9E6, 10H2, 11J1, 2K9
19	D31Ø	A9, 4G4, 5A4, 9E7, 10L3, 11J1, 2K9

DATA LATCH

01E 19-232 A

02	DØØØ	H1, 8E5, 11J7, 15G5, 2B9
05	DØ1Ø	H2, 4A1, 5A2, 8E6, 11J7, 2B9
06	DØ21	H2, 15N4, 8E7, 11J7, 2B9
09	DØ3Ø	H3, 4A5, 5A1, 8E7, 11J7, 2C9
12	DØ4Ø	H3, 4A2, 8A6, 11J7, 2C9
15	DØ5Ø	H4, 4A2, 8E6, 11J7, 2C9
16	DØ61	H4, 4A2, 8E7, 11J7, 2D9
19	DØ7Ø	H5, 4G6, 8E7, 11J7, 2D9

LDBY01 14M6
GDD1 F5, 15N4
LDBY11 14M7

02E 19-232

02	DØ8Ø	H6, 4A4, 5A1, 8K5, 11J5, 2E9
05	DØ9Ø	H6, 4A6, 5A2, 8K6, 11J5, 2E9
06	DlØØ	H6, 4G3, 5A2, 8K6, 11J5, 2E9
09	Dl1Ø	H7, 4G6, 5A3, 8K6, 11J5, 2E9
12	Dl2Ø	H8, 4A6, 5A6, 8K6, 11J5, 2F9
15	Dl3Ø	H8, 4A3, 5A6, 8K6, 11J5, 2F9
16	Dl4Ø	H9, 4A7, 5A6, 8K6, 11J5, 2F9
19	Dl5Ø	H9, 4G3, 5A7, 8K7, 11J5, 2F9

ERROR CORRECTOR

SCALE—
TOLERANCE: XXX ± .005; XX ± .02; X ± .05; ANGLES ± 1°; UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	CRAFT	
	CHK	
	ENGR	

TITLE : SCHEMATIC
LBC (8MB CAPABILITY)

TASK NO 03183
DWG NO 35-806 D08
SHEET OF 6 — 18

DRAWING 44-231 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

GOOD PARITY REGISTER

WRITE PARITY REGISTER

PARITY CORRECTOR & UNCORRECTABLE ERROR

UNCORRECTED ERROR LEDS

NON PRESENT MEMORY - LAMP-OFF
INCORRECTABLE ERROR - LAMP-ON

SEE NOTES

NOTES:
1. FOR CUSTOMER SERVICE ONLY:
TO TURN OFF UCE/NPM AND MODULE I.D. LAMPS;
CONNECT TP11 TO TP12 MOMENTARILY. DO NOT STRAP.
MAKE SURE TO REMOVE THE JUMPER.

BRUNING 44-231 24538

SCALE -

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE: SCHEMATIC
LBC (8MB CAPABILITY)

TASK NO 03183
SYM NO 35-8016 B08
SHEET OF 7 - 18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

LMB BUS
DRIVERS AND RECEIVERS

SCALE—	NAME	TITLE	DATE	TITLE SCHEMATIC
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT		LBC (8MB CAPABILITY)
		CHK		
		ENGR		
				TASK NO. 03183
				SMC NO. 35-806 D08
				SHEET OF 8 — 18

REVISIONS					
AREA L9 RES. 00K WAS 09M W/ PIN 16 TO P5 & PIN 09 TO NVMØ VALUE 1K					
RDS	UJP	4763		8-18-81	R01
AREA K9, EXTENSIVE CHANGES MADE TO IC 15M, FOR PREVIOUS REV LEVEL SEE R01 MICRO-FILM COPY.					
KR		4909	MS	1-15-82	R02

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC

LBC (8MB CAPABILITY)

NOTES

DRAFTER	DSTINE
DATE	12-11-80
TASK	03183
DWG	35-806 R02 D08
SHT	9 - 18

WRITE/READ ERROR LOGGER ADDRESS MUX

ERROR LOGGER SHIFT REGISTER

REVISIONS						
ADD A N-5, DELETED 1K RESISTOR C9M BETWEEN GATES 5 & P5.						
JAH	JV	5089	NIS	A 19-82	K01	

NOTES

DRAFTER	QSTINE
DATE	12-15-80

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
LBC (8MB CAPABILITY)

TASK 03183	SHT
DWG 35 806 R01 D08	10 - 18

ERROR LOGGER

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

CACHE 256 x 36

CACHE PARITY CHECK

16H7 TAA121 11 — FW WRITE
14G4 SFW1 13
1257 HIT1 01
04
16D1 TB061 05 — PW WRITE
14H3 SPW1 06
15L2 ME1 12 — 03J 19-236 SA — 11 — 02
16S7 QWM1 13
16H2 TB121 03 — QW ERR
10 — 03J 19-236 SA — 08 — 09
16B4 TB061 09
16E4 TB080 10 — QW NO ERR
ZOC 19-062
08 CAWEO

3C8 A22Ø
3C8 A23Ø
3C8 A24Ø
3C8 A25Ø
3C8 A26Ø
3C9 A27Ø
3K7 A28Ø
3J3 A29Ø
1656 CAENO

21K 19-254 256X9 RAM — A
22K 19-254 256X9 RAM — A
24K 19-254 256X9 RAM — A
25K 19-254 256X9 RAM — A

D31Ø 6F7 D30Ø 6F7 D29Ø 6F7 D28Ø 6F7 D27Ø 6F7 D26Ø 6F6 D25Ø 6F6 D24Ø 6F6
D23Ø 6F4 D22Ø 6F3 D21Ø 6F3 D20Ø 6F3 D19Ø 6F2 D18Ø 6F2 D17Ø 6F2 D16Ø 6F1
D15Ø 6N7 D14Ø 6N7 D13Ø 6N6 D12Ø 6N6 D11Ø 6N6 D10Ø 6N6 D09Ø 6N6 D08Ø 6N6
D07Ø 6N2 D06Ø 6N2 D05Ø 6N2 D04Ø 6N2 D03Ø 6N2 D02Ø 6N1 D01Ø 6N1 D00Ø 6N1

21J 19-223 9BIT EVEN/ODD PARITY GEN/CHK — EVEN OUT 05 NC; ODD OUT 06
22J 19-223 9BIT EVEN/ODD PARITY GEN/CHK — 05 NC
24J 19-223 9BIT EVEN/ODD PARITY GEN/CHK — 05 NC
25J 19-223 9BIT EVEN/ODD PARITY GEN/CHK — 05 NC — SEE NOTE 1

23K 470 70 P5
23K 470 71 P5
23K 470 72 P5
23K 470 73 P5

23J 19-055 SG
23K 19-056 SGO

21H 19-060 SG — 06 PER1 16L8, 15A8

XRPE 14K3
1256 CHIT1 — 12A 19-064 SF — 09 NC; 07
16R9 CPER1
13E4 SCLROC
219-4 — 330 — 16A 76 P5 — CACHE PARITY ERROR

1657 CAENI

CACHE & CACHE PARITY

NOTE 1. DEPOPULATE COMPONENTS MARKED WITH AN ASTERISK FOR F02 VARIATION.

SCALE—
TOLERANCE XXX ± .005; XX ± .02; X ± .03; ANGLES ± 1° UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE SCHEMATIC
LBC (8MB CAPABILITY)

CAGE NO. 03183 — SIZE D — DWG NO. 35-806 D08 — SHEET 11—18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
AREA M6, ADDED MISBI & MISAI W/CROSS REF 15AB TO 18F09 & 18F10. AREA N6, ADDED MISSI W/CROSS REF 15A7 TO 18F81.
KP 4909 MS 1-15-82 E01

STB0
13H2 TEL0
14H2 RST0
7S4 UCE0

21H* 19-060 SG

VALØ

21E 19-055 SG

VALI N1

N3

3C8 A220
3C8 A230

21D
19-259 P/O
2-TO-4
LINE DECODER/DEMULTIPLEXER

2Y3 2Y1 2Y2 2Y0

16S7 QWM1
16H7 TRA121

19A 19-055 SG

3C1 A0B0
3C2 A090
3C2 A100
3C2 A110

A0B0:A210 TAG FIELD

TPP 203-3 TGA081
TPN 204-3 TGA091
TPM 205-3 TGA101
TPM 206-3 TGA111

25A* 19-075 16x4 REG STK
25B* 19-075 16x4 REG STK
25C* 19-075 16x4 REG STK
25E* 19-075 16x4 REG STK

3C3 A120
3C3 A130
3C3 A140
3C4 A150

TPL 207-3 TGA121
TPK 208-3 TGA131
TPJ 209-3 TGA141
TPJ 210-3 TGA151

24A* 19-075 16x4 REG STK
24B* 19-075 16x4 REG STK
24C* 19-075 16x4 REG STK
24E* 19-075 16x4 REG STK

3C5 A160
3C5 A170
3C5 A180
3C5 A190

TPH 211-3 TGA161
TPG 212-3 TGA171
TPF 213-3 TGA181
TPE 214-3 TGA191

23A* 19-075 16x4 REG STK
23B* 19-075 16x4 REG STK
23C* 19-075 16x4 REG STK
23E* 19-075 16x4 REG STK

ADRS A B C D

DATA IN OUT PUTS S1 S2 S3 S4

3C6 A200
3C7 A210

TPD 215-3 TGA201
TPC 216-3 TGA211

22A* 19-075 16x4 REG STK
22B* 19-075 16x4 REG STK
22C* 19-075 16x4 REG STK
22E* 19-075 16x4 REG STK

A220:A270 INDEX ADDRESS

3C8 A240
3C8 A250
3C8 A260
3C9 A270

SEE NOTE 2

3C8 A260
3C5 A190
3C9 A270
3C6 A200
NC
NC
NC
NC

23M* 19-065 2TO1 MUX

13H2 STB1

3C8 A220
3C4 A150
3C8 A230
3C5 A160
3C8 A240
3C8 A170
3C8 A250
3C8 A180

24M* 19-065 2TO1 MUX

SEL

25D* 19-154
25D* 19-154
25D* 19-154
25D* 19-154
24D* 19-154
24D* 19-154
24D* 19-154
24D* 19-154
23D 19-154
23D 19-154

21A* 19-279 EOUT

TAG COMPARE

21B* 19-279 EOUT

EIN

26R* 19-237 256X1 RAM

DATA IN
DATA OUT
WE
ME1
ME2
ME3

CACHE VALIDATOR

VALI H1

NVALI 16L9, N7, 15A8

F1 VALØ
16D5 TA061
57 HITI

HIT
UCE NORM MEM OP
UCE (QWM)
QWM

21C* 19-062 SG

16E3 TB0B1
1443 SPW1
7R4 UCE1

07C 19-236 SA

16S7 QWM1

REFI 13J3
UCECLRØ 14S4

15A8
MISBI
MISAI
18F 19-241 SN
22D 19-057 SG
MISI 16L8, 15A9

221-5 TP4
TP3 81 18F 1K 85
222-5 P5
15A7 MISSI

NVALI N3
PSU
15A 19-234 SN
CHITI 11N6

STBD 13H2
DS 14C 19-063 SF DC
HITI N9, 11C2
N.C.

16D8 TA0B1
13N8 MB1A

CACHE HIT DETECTOR

NOTES:
1. REMOVE JUMPER 221-5 TO 222-5 TO FORCE CACHE MISSES.
2. DEPOPULATE IC'S MARKED WITH AN ASTERISK FOR F02 VARIATION.

SCALE—

	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC (8MB CAPABILITY)

TOM 03183
PEC 35-806201 D08
SHEET 12 OF 18

PERKIN-ELMER

REVISIONS				
IN AREA F9, G9 IC'S DIM01 LOCOR WERE NOT SPECIFIED				
RS	UNP.	4763	8.18.81	R01
ADDED CROSS REF. 16H9 TO MB1B (AREA R-8).				
AH	AV	5089	MS	8-20-82	R02

16 MICRO SEC. OSC.

1.8 MS OSC.

BURST REFRESH

REFRESH COUNTERS

REFRESH & CONTROL

NOTE: 1 ALL IC ON THIS SHEET ARE P5U UNLESS NOTED OTHERWISE.

2 THIS STRAP MUST BE IN PLACE. IT IS REMOVED FOR TESTING PURPOSES ONLY.

SCALE –	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC (8MB CAPABILITY

TAB NO. 03183 SHEET OF 13–18

DWG NO. 35-806R02 D08

PERKIN-ELMER

Spacecraft Systems Division
Oceanport N.J.U.S.A.

REVISIONS				
AREA M3 WAS SHOWN AS FOLLOWS: REMOVED 18K RES & RE-LOCATED IT ON SHT 16.				
NP	JU	4909	MS	1-15-82	R01

3F8 MATRØ
3F8 MATDØ
3F9 DMAESTØ
15F5 MATDØ
13N8 MB1B
RSTDCD1 B8
RSTI 7A6, 15A6, 16K2, 15D5
16L8 BYPO
16S8 QWMO
G6 RFWI
3F8 CBØ31
3F8 CBØ21
3F8 CBØ11
MB0A
7A6 WRTI
3C6 WRTØA
20H W/W ONLY
20F 19-129 STTL
ENP
3 TO 8 DECODER
WRITE COMMANDS
20J 19-129 STTL
READ COMMANDS
PSBYO
PSHWO
DSHWO
DDSHWO
PSFWO
DSFWO
DDSFWO
PRFWO
ELO
DRELI
RCTO 05
ELSTI
RSTO
DRFWØ
DRFWI 16K1
A301
A300
A310
A191
BAØ8Ø
TELØ 7A6, 15F2, 12A1
SBYI G9
TELI 15A1, J5
RSTO 12A1
SPWI 15A6, 11C2, 12N4
SHWI G9
SFWO A8
SFWI 2R4, 11C2, 15A2
PRFWØ 16K5, 16K9
PRFWI J1, 15A8, 15F2, 16K2
SPWO 15F2
ELSTI J1, 10H5, 10L5, 15A8
RELI 16K4, 10A4, 15G8
ROASTI 16E9
RFWI H1, 15A1, 16A1
TB0080
TB021
SBYI
WDENO 2S4
16B6 TAØØØ
16D8 TAØ41
H4 PRFWI
H5 ELSTI
15N2 NEI
10E6 AD31
10A4 CLKØD
3M7 WCCI
15F3 WEI
15N3 REO
QWMO
16G5 TA201
16H4 TA160
15K3 REI
N2 MBIA
A7 REFO
H2 TELI
H4 SHWI
16E4
16D1
H2
MBIA J4, 13N8
DUAI 15N7
10D4 SCLKØA
NCLRI 13G9
WCECLRØ 12S5
NPMO 15F5, 7M8
FNPMI NC
FNPMO 7M4, 9L7
13G7 ERO
13E4 SCLROC
LDGPI 7A6
LDBY01 6N5
LDBY11 6N5
LDBY21 6F5
LDBY3i 6F5
RUREI 15J4
13K3 REFI
J4, 13N3 REFO
3C6 PSELIA
3C6 DHWO
13N7 MBIA
H4 SFWO
16D5 TA021
D1 RSTDCD1

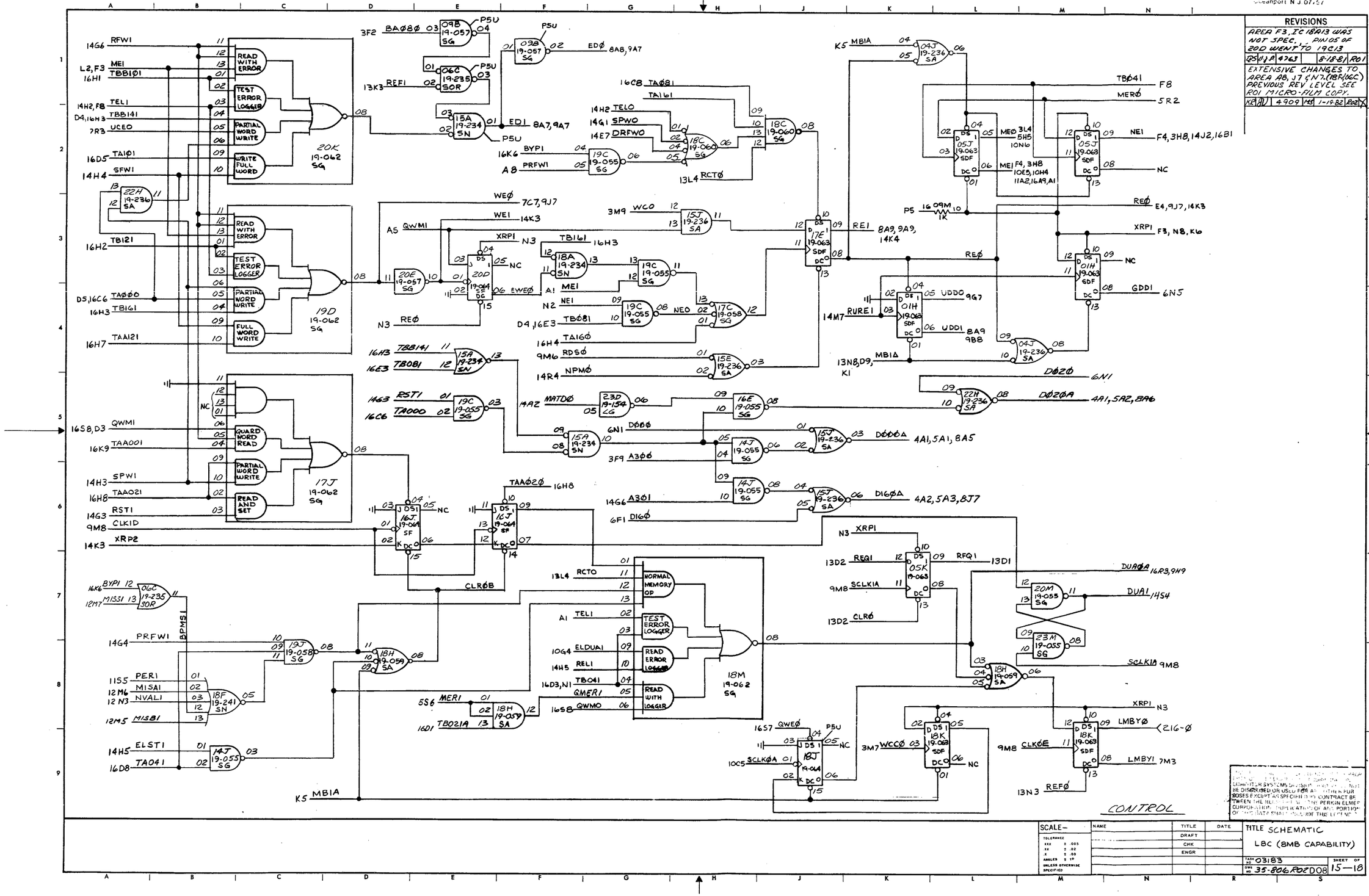
COMMAND DECODE AND CONTROL

SCALE–	NAME	TITLE	DATE
TOLERANCE XX ± .005, X ± .02, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC (8MB CAPABILITY)
TASK NO. 03183
DWG NO. 35-806 R01 D08
SHEET OF 14—18

PERKIN-ELMER
Computer Systems Division
Clearport N.J. 07757

REVISIONS				
AREA F3, IC 18A13 WAS NOT SPEC. PINOS OF 20D WENT TO 19C13				
DS	MJA	4763	8-18-81	R01
EXTENSIVE CHANGES TO AREA A8, J7 & N7. (18A10GC) PREVIOUS REV LEVEL SEE R01 MICRO-FILM COPY.				
KE	MJA	4909	MS	1-19-82	R02



CONTROL

SCALE–	NAME	TITLE	DATE
TOLERANCE		DRAFT	
XXX ± .005		CHK	
XX ± .02		ENGR	
X ± .03			
ANGLES ± 1°			
UNLESS OTHERWISE SPECIFIED			

TITLE SCHEMATIC
LBC (8MB CAPABILITY)

TASK NO 03183 SHEET OF
DWG NO 35-806A02D08 15—18

PERKIN-ELMER
Computer Systems Division
Oceanport N.J. 07757

REVISIONS			
AREA D1, F1, D4 & F4 IC'S 17B, 18B, 13A & 13B WERE 19-249 F02. ADDED NOTE 2.	KB	4900	A 12-2-81 RDI
AREA C8 ADDED 15A9 TO TA041. AREA R3 DUA0A WAS DUA0. AREA S5 18J PIN 07 WAS NC. 18J PIN 09 WAS ALSO CROSS REF TO 9J9. AREA E9 ADDED RES 18K TO 16D PIN 10.	KB	4909	MS 1-19-82 P02
AREA K-2, 18D04 DID GO TO PRFW1, LOC. 14H5. 18D05 DID GO TO 18D04. AREA J-3 & 4, ADDED 05A, IC.	JH	5089	MS 8-19-82 P03

TIMER & CONTROL

NOTES:
1. REMOVE STRAP FROM 217-S (TP8) TO 218-S (TP7) TO BYPASS CACHE.
2. IC LOCATIONS SHOW IN PARENTHESIS REPRESENT ALTERNATE USE OF 19-249 F02.

SCALE—
TOLERANCE: XXX ± .005; XX ± .02; X ± .03; ANGLES ± 1/2°; UNLESS OTHERWISE SPECIFIED

	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC

TASK NO 03183
DWG NO 35-806 R03 D08
SHEET OF 16—18

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0001	A080	3	0063	D090	11	0125			0187	ELMA31	3	0249	LMB111	8	0311	MDSI50	2	0373	RD021	3	0435	TA161	16	0497	07J05	4	0559	05E06	7	0621	22E02	12	0683	20M08	14
0002	A090	3	0064	D100	11	0126	EB000	6	0188	FNPMO	14	0250	LMB121	8	0312	MDS160	2	0374	RD031	3	0436	TA181	16	0498	07K06	4	0560	05E08	7	0622	TGA081	12	0684	22H06	14
0003	A100	3	0065	D110	11	0127	EB010	6	0189			0251	LMB131	8	0313	MDS170	2	0375	RDSO	9	0437	TA201	16	0499	07K05	4	0561	05E11	7	0623	TGA091	12	0685	20J14	14
0004	A110	3	0066	D120	11	0128	EB020	6	0190	TP9	3	0252	LMB141	8	0314	MDS180	2	0376	RDSI	9	0438	TB001	16	0500	08J06	4	0562	06E03	7	0624	TGA101	12	0686	17H10	14
0005	A120	3	0067	D130	11	0129	EB030	6	0191	LD01	10	0253	LMB151	8	0315	MDS190	2	0377	REO	15	0439	TB021	16	0501	08J05	4	0563	06E06	7	0625	TGA111	12	0687	21D04	14
0006	A130	3	0068	D140	11	0130	EB040	6	0192	LD02	10	0254	LMB161	8	0316	MDS200	2	0378	REI	15	0440	TB041	16	0502	08K06	4	0564	06E08	7	0626	TGA121	12	0688	21D05	14
0007	A140	3	0069	D150	11	0131	EB050	6	0193	LDBY01	14	0255	LMB171	8	0317	MDS210	2	0379	REFO	13	0441	TB061	16	0503	08K05	4	0565	08D05	7	0627	TGA131	12	0689	21D06	14
0008	A150	3	0070	D160	11	0132	EB060	6	0194	LDBY11	14	0256	LMB181	8	0318	MDS220	2	0380	REFOA	13	0442	TB081	16	0504	09J06	4	0566	08D06	7	0628	TGA141	12	0690	21D07	14
0009	A160	3	0071	D170	11	0133	EB070	6	0195	LDBY21	14	0257	LMB191	8	0319	MDS230	2	0381	REFI	13	0443	TB101	16	0505	09J05	4	0567	10D05	7	0629	TGA151	12	0691	16D05	14
0010	A170	3	0072	D180	11	0134	EB080	6	0196	LDBY31	14	0258	LMB201	8	0320	MDS240	2	0382	RELI	14	0444	TB121	16	0506	09K06	4	0568	10D06	7	0630	TGA161	12	0692	22F08	14
0011	A180	3	0073	D190	11	0135	EB090	6	0197	LDGPI	14	0259	LMB211	8	0321	MDS250	2	0383	REQI	13	0445	TB141	16	0507	09K05	4	0569	12D05	7	0631	TGA171	12	0693	02F06	14
0012	A190	3	0074	D200	11	0136	EB100	6	0198	LDOD1	16	0260	LMB221	8	0322	MDS260	2	0384	RFA01	13	0446	TB161	16	0508	10J06	4	0570	12D06	7	0632	TGA181	12	0694	01C06	14
0013	A200	3	0075	D210	11	0137	EB110	6	0199	LMBY0	15	0261	LMB231	8	0323	MDS270	2	0385	RFA11	13	0447	TB080	16	0509	10J05	4	0571	06D05	7	0633	TGA191	12	0695	03C06	14
0014	A210	3	0076	D220	11	0138			0200	LMBY1	15	0262	LMB241	9	0324	MDS280	2	0386	RFA21	13	0448	TAA020	16	0510	10K06	4	0572	06D06	7	0634	TGA201	12	0696	02C06	14
0015	A220	3	0077	D230	11	0139	EB120	6	0201	LOE1	16	0263	LMB251	9	0325	MDS290	2	0387	RFA31	13	0449	TAA001	16	0511	10K05	4	0573	05H01	7	0635	TGA211	12	0697	04C06	14
0016	A230	3	0078	D240	11	0140	EB130	6	0202	GP000	7	0264	LMB261	9	0326	MDS300	2	0388	RFA41	13	0450	TAA121	16	0512	11J06	5	0574	03J03	7	0636	25M04	12	0698	03C08	14
0017	A240	3	0079	D250	11	0141	EB140	6	0203	GP010	7	0265	LMB271	9	0327	MDS310	2	0389	RFA51	13	0451	TBB040	16	0513	11J05	5	0575	03F08	7	0637	25M07	12	0699	19C06	15
0018	A250	3	0080	D260	11	0142	EB150	6	0204	GP020	7	0266	LMB281	9	0328	MREO	9	0390	RFA61	13	0452	TBB101	16	0514	11K06	5	0576	13D09	7	0638	24M04	12	0700	18C06	15
0019	A260	3	0081	D270	11	0143	EB160	6	0205	GP030	7	0267	LMB291	9	0329	MREFO	9	0391	RFA71	13	0453	TBB141	16	0515	11K05	5	0577	16C02	7	0639	24M07	12	0701	15J11	15
0020	A270	3	0082	D280	11	0144	EB170	6	0206	GP040	7	0268	LMB301	9	0330	MWA001	9	0392	RFQ1	15	0454	TAA021	16	0516	12J06	5	0578	42X10	7	0640	24M09	12	0702	19C11	15
0021	A280	3	0083	D290	11	0145	EB180	6	0207	GP050	7	0269	LMB311	9	0331	MWA011	9	0393	RFWI	14	0455	TELO	14	0517	12J05	5	0579	16C07	7	0641	24M12	12	0703	17C12	15
0022	A290	3	0084	D300	11	0146	EB190	6	0208	GP060	7	0270	LMB321	9	0332	MWEO	9	0394	RDSTI	14	0456	TELI	14	0518	12K06	5	0580	42X07	7	0642	21C08	12	0704	15E03	15
0023	A300	3	0085	D310	11	0147	EB200	6	0209	GDD1	15	0271	LMB331	9	0333	MX021	3	0395	RSELO	13	0457	UP000	9	0519	12K05	5	0581	16C10	7	0643	18F06	12	0705	18C08	15
0024	A310	3	0086	D000A	15	0148	EB210	6	0210	GMERI	15	0272	LMB341	9	0334	MX031	3	0396	RSTO	14	0458	UP010	9	0520	13J06	5	0582	42X04	7	0644	MISSI	12	0706	15A10	15
0025	A161	10	0087	D020A	15	0149	EB220	6	0211	GMVFO	9	0273	LMB351	9	0335	NCEO	9	0397	RSTI	14	0459	UP020	9	0521	13J05	5	0583	42X00	7	0645	25D02	12	0707	14J06	15
0026	A171	10	0088	D160A	15	0150	EB230	6	0212	HITI	12	0274	LMB361	9	0336	NCLRI	14	0398	RUREI	14	0460	UP030	9	0522	13K06	5	0584	42X01	7	0646	25D04	12	0708	14J08	15
0027	A181	10	0089	DA00	5	0151	EB240	6	0213	LMA080	3	0275	LMB371	9	0337	NEO	15	0399	SO01	10	0461	UP040	9	0523	13K05	5	0585	15C03	7	0647	25D06	12	0709	05K08	15
0028	A191	3	0090	DA10	5	0152	EB250	6	0214	LMA090	3	0276	LMB381	9	0338	NEI	15	0400	SO11	10	0462	UP050	9	0524	03F02	5	0586	42X16	7	0648	25D08	12	0710	18J06	15
0029	A301	14	0091	DA20	5	0153	EB260	6	0215	LMA100	3	0277	MBO	13	0339	NPMO	14	0401	SO21	10	0463	UP060	9	0525			0587	09M14	7	0649	MISBI	12	0711	23M08	15
0030	ADO1	10	0092	DA30	5	0154	EB270	6	0216	LMA110	3	0278	MBOA	13	0340	NBALI	12	0402	SO31	10	0464	UCEO	7	0526	11E03	6	0588	09K10	9	0650	MISAI	12	0712	18H06	15
0031	AD11	10	0093	DA40	5	0155	EB280	6	0217	LMA120	3	0279	MBI	13	0341	NVMO	9	0403	SO41	10	0465	UCEI	7	0527	11E06	6	0589	P500K		0651	25D10	12	0713	18K05	15
0032	AD21	10	0094	DB00	5	0156	EB290	6	0218	LMA130	3	0280	MBIA	13	0342	ODDI	16	0404	SO51	10	0466	UDDO	15	0528	11E08	6	0590	19M10	9	0652	25D12	12	0714	04J08	15
0033	AD31	10	0095	DB10	5	0157	EB300	6	0219	LMA140	3	0281	MBIB	13	0343	MATFO	14	0405	SO61	10	0467	UDD1	15	0529	11E11	6	0591	17H02	10	0653	24D02	12	0715	04J06	15
0034	BMC10	9	0096	DB20	5	0158	EB310	6	0220	LMA150	3	0282	MBIC	13	0344	MATDO	14	0406	SDYI	14	0468	UFPI	16	0530	12E03	6	0592	15H06	10	0654	24D04	12	0716	17J08	15
0035	BMVFO	9	0097	DB30	5	0159	EPB000	7	0221	LMA160	3	0283	MC10	16	0345	PSFWO	14	0407	SCLKI	9	0469	VALO	12	0531	12E06	6	0593	05K05	10	0655	24D06	12	0717	23D06	15
0036	BSCLRO	9	0098	DB40	5	0160	EPB010	7	0222			0284	MCCO	9	0346	PSHWO	14	0408	SCLKIA	9	0470	VALI	12	0532	12E08	6	0594	15E06	10	0656	24D08	12	0718	16E08	15
0037	BYPO	16	0099	DB50	5	0161	EPB020	7	0223	LMA170	3	0285	MEO	10	0347	POOO	4	0409	SCLKOA	10	0471	WA000	3	0533	12E11	6	0595	22M08	10	0657	24D10	12	0719	05C06	14
0038	BYPI	16	0100	DB60	5	0162	EPB030	7	0224	LMA180	3	0286	MEI	15	0348	PO10	4	0410	SCLRIB	13	0472	WA001	3	0534	13E03	6	0596	16H06	10	0658	24D12	12	0720	15E11	14
0039	CAENO	16	0101	DB70	5	0163	EPB040	7	0225	LMA190	3	0287	MEA000	9	0349	PO20	4	0411	SCLRO	13	0473	WA010	3	0535	13E06	6	0597	19M04	10	0659	23D02	12	0721	19E13	14
0040	CAENI	16	0102	DC00	5	0164	EPB050	7	0226	LMA200	3	0288	MEA010	9	0350	PO30	4	0412	SCLROB	13	0474	WA011	3	0536	13E08	6	0598	16H08	10	0660	23D04	12	0722	15J08	14
0041	CARI	13	0103	DC10	5	0165	EPB060	7	0227	LMA210	3	0289	MEA020	9	0351	PO40	5	0413	SCLROC	13	0475	WCO	3	0537	13E11	6	0599		10	0661	05A67	13	0723	15D06	14
0042	CAWEO	11	0104	DC20	5	0166	EAO	16	0228	LMA220	3	0290	MEA030	9	0352	PO50	5	0414	SFWO	14	0476	WCCO	3	0538	14E03	6	0600	18K12	10	0662	05A63	13	0724	15E08	14
0043	CBO11	3	0105	DC30	5	0167	EDO	15	0229	LMA230	3	0291	MERO	5	0353	PO60	5	0415	SFWI	14	0477	WCCI	3	0539	14E06	6	0601	23K03	11	0663	06A02	13	0725	16D06	14
0044	CBO21	3	0106	DC40	5	0168	EDI	15	0230	LMA240	3	0292	MERI	5	0354	PERI	11	0416	SHIFTI	10	0478	WDENO	3	0540	14E08	6	0602	23K06	11	0664	09A06	13	0726	18E08	14
0045	CBO31	3	0107	DC50	5	0169	ELO	14	0231	LMA250	3	0293	MISI	12	0355	PFSDO	9	0417	SHWI	14	0479	WEO	15	0541	14E11	6	0603	23K08	11	0665	07A09	13	0727	17F06	14
0046	CHI21	12	0108	DC60	5	0170	ELDUAO	10	0232	LMA260	3	0294	MRDSO	9	0356	PFSDI	13	0418	SPWO	14	0480	WEI	15	0542	07E03	6	0604	23K11	11	0666	09B08	13	0728	17E05	14
0047	CLKOD	10	0109	DC70	5	0171	ELDUAI	10	0233	LMA270	3	0295	MDS000	2	0357	PRFWO	14	0419	SPWI	14	0481	WRTO	3	0543	07E06	6	0605	23J03	11	0667	09A71	13	0729	22H05	14
0048	CLKIC	9	0110	DERRO	5	0172	ELSTI	14	0234	LMA280	3	0296	MDS010	2	0358	PRFWI	14	0420	STBO	13	0482	WRTOA	3	0544	07E08	6	0606	23J06	11	0668	10A06	13	0730	18F05	15
0049	CLKID	9	0111	DHWO	3	0173	END1	13	0235	LMA290	3	0297	MDS020	2	0359	PSBYO	14	0421	STBI	13	0483	WRTI	14	0545	07E11	6	0607	23J08	11	0669	09A08	13	0731	14J03	15
0050	CLRO	13	0112	DMHWO	3	0174	ERO	13	0236	LMA300	3	0298	MDS030	2	0360	PSELI	14	0422	TA000	16	0484	XRPI	15	0546	08E03	6	0608	23J11	11	0670	08B12	13	0732	19J08	15
0051	CLROB	15	0113	DPRI	13	0175			0237	LMA310	8	0299	MDS040	2	0361	PSELIA	3	0423	TA080	16	0485	XRP2	16	0547	08E06	6	0609	23K01	11	0671	06A14	13	0733	16J06	15
0052	CLTBI	16	0114	DRELI	14	0176	ELA040	10	0238	LMB001	8	0300	MDS050	2	0362	QWEO	16	0424	TA120	16	0486	21R19	9	0548	08E08	6	0610	22J06	11	0672	06A01	13	0734	20K08	15
0053	CPERI	16	0115	DRFWO	14	0177	ELA050	10	0239	LMB011	8	0301	MDS060	2	0363	QWMO	16	0425			0487	03J06	2	0549	08E11	6	0611	24J06	11	0673	06A14	13	0735	16J07	15
0054	DOOO	11	0116	DRFWI	14	0178	ELA060	10	0240	LMB021	8	0302	MDS070	2	0364	QWMI	16	0426	TA160	16	0488	18R03	3	0550	09E03	6	0612	25J06	11	0674	11B15	13	0736	16J09	15
0055	DO10	11	0117	DDSFWO	14	0179	ELA070	10	0241	LMB031	8	0303			0365	RCARO	10	0427	TA001	16	0489	18R06	3	0551	09E06	6	0613	12A07	11	0675	09A03	13	0737	19C03	15
0056	DO20	11	0118	DDSHWO	14	0180	ELA080	10	0242	LMB041	8	0304	MDS080	2	0366	RCLCO	9	0428	TA021	16	0490	23F08	3	0552	09E08	6	0614	42X19	11	0676	22M06	13	0738	15A13	15
0057	DO30	11	0119	DUA0	15	0181	ELA090	10	0243	LMB051	8	0305	MDS090	2	0367	RCLCI	9	0429	TA041	16	0491	22H03	3	0553	09E11	6	0615	03J11	11	0677			0739	19A08	16
0058	DO40	11	0120	DUAI	15	0182	ELA100	10	0244	LMB061	8	0306	MDS100	2	0368	RCLRO	13	0430	TA061	16	0492	18R11	3	0554	10E03	6	0616	03J08	11	0678	15B08	13	0740	14A03	16
0059	DO50	11	0121	DSHWO	14	0183	ELA110	10	0245	LMB071	8	0307	MDS110	2	0369	RCLRI	13	0431	TA081	16	0493	24F05	3	0555	10E06	6	0617	14A06	12	0679	08B06	13	0741	17C08	16
0060	DO60	11	0122	DSFWO	14	0184	ELMA01	3	0246	LMB081	8	0308	MDS120	2	0370	RCTO	13	0432	TA101	16	0494	25H08	3	0556	10E08	6	0618	22A02	12	0680	20M06	14	0742	13C08	16
0061	DO70	11	0123	20J14	14	0185	ELMA11	3	0247	LMB091	8	0309	MDS130	2	0371	RCTI	13	0433	TA121	16	0495	21E11	3	0557	10E11	6	0619	22B02	12	0681	19E01	14	0743	12b10	16
0062	DO80	11	0124	MARSTO	14	0186	ELMA21	3	0248	LMB101	8	0310	MDS140	2	0372	RDO11	3	0434	TA141	16	0496	07J06	4	0558	05E03	7	0620	22L02	12	0682	22D08	14	0744	16D07	16

NOTES

REVISIONS				
DELETED NET 175 SIG. TWEI.				
BS	JL	9763		E 12-81 R01
NET 114 WAS D20. NET 644 WAS 52A21. NET 699 WAS 11419 NET 650 WAS 21B19.				
KR	JL	4907	M81 1-19-82	2021X

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
	DES/DFT	
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE

LBC
(8MB CAPABILITY)

TASK 03183	SHT
DWG 35-806 R02 D08	17-18

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0745	16E03	16	0807	GND16J		0869	09B04	15	0931			0993			1055			1117			1179			1241			1303			1365			1427		
0746	14B11	16	0808	GND20D		0870	06C03	15	0932			0994			1056			1118			1180			1242			1304			1366			1428		
0747	14B08	16	0809	GND08A		0871	07D03	7	0933			0995			1057			1119			1181			1243			1305			1367			1429		
0748	19B08	16	0810	13C06	2	0872	07D06	7	0934			0996			1058			1120			1182			1244			1306			1368			1430		
0749	18A10	16	0811	GND10C		0873	07D08	7	0935			0997			1059			1121			1183			1245			1307			1369			1431		
0750	12C08	16	0812	06R08	7	0874	07D11	7	0936			0998			1060			1122			1184			1246			1308			1370			1432		
0751	12C06	16	0813	04J11	7	0875			0937			0999			1061			1123			1185			1247			1309			1371			1433		
0752	21F06	16	0814	TB02IA	15	0876	MERRI	3	0938			1000			1062			1124			1186			1248			1310			1372			1434		
0753	23M11	16	0815	42X13	13	0877	01M01	13	0939			1001			1063			1125			1187			1249			1311			1373			1435		
0754	18K71	16	0816	52X19	13	0878	06C08	13	0940			1002			1064			1126			1188			1250			1312			1374			1436		
0755	16B08	16	0817			0879	EWE0	15	0941			1003			1065			1127			1189			1251			1313			1375			1437		
0756	19M01	16	0818	MATRSR0	3	0880	18A13	15	0942			1004			1066			1128			1190			1252			1314			1376			1438		
0757	18D08	16	0819	MATRSD0	3	0881	PSU06C	9	0943			1005			1067			1129			1191			1253			1315			1377			1439		
0758	P5U09A		0820	DMARS0	3	0882	13A4ND	16	0944			1006			1068			1130			1192			1254			1316			1378			1440		
0759			0821	RDSD0	9	0883	13B6ND	16	0945			1007			1069			1131			1193			1255			1317			1379			1441		
0760	P5U07B		0822	CLK0E	9	0884	17B4ND	16	0946			1008			1070			1132			1194			1256			1318			1380			1442		
0761	P5U05A		0823	07C11	12	0885	18B6ND	16	0947			1009			1071			1133			1195			1257			1319			1381			1443		
0762			0824	UCECLR0	14	0886	DUA0A	15	0948			1010			1072			1134			1196			1258			1320			1382			1444		
0763	GND20R		0825	NCAR1	13	0887	BPMS1	15	0949			1011			1073			1135			1197			1259			1321			1383			1445		
0764	GND19R		0826	07C06	13	0888	EA1	9	0950			1012			1074			1136			1198			1260			1322			1384			1446		
0765	GND23F		0827	08C01	13	0889	GND05A	16	0951			1013			1075			1137			1199			1261			1323			1385			1447		
0766	GND07K		0828	08A08	13	0890	05A09	16	0952			1014			1076			1138			1200			1262			1324			1386			1448		
0767	GND08K		0829			0891			0953			1015			1077			1139			1201			1263			1325			1387			1449		
0768	GND09K		0830	19F06	13	0892			0954			1016			1078			1140			1202			1264			1326			1388			1450		
0769	GND10K		0831		14	0893			0955			1017			1079			1141			1203			1265			1327			1389			1451		
0770	GND11K		0832	CCAR1	13	0894			0956			1018			1080			1142			1204			1266			1328			1390			1452		
0771	GND12K		0833	TA06IA	14	0895			0957			1019			1081			1143			1205			1267			1329			1391			1453		
0772	GND13K		0834	07M11	10	0896			0958			1020			1082			1144			1206			1268			1330			1392			1454		
0773	GND04D		0835			0897			0959			1021			1083			1145			1207			1269			1331			1393			1455		
0774	GND21R		0836	GND09C	3	0898			0960			1022			1084			1146			1208			1270			1332			1394			1456		
0775	GND07M		0837	ERLA01	3	0899			0961			1023			1085			1147			1209			1271			1333			1395			1457		
0776	GND15F		0838	BA090	3	0900			0962			1024			1086			1148			1210			1272			1334			1396			1458		
0777	GND16F		0839	BA091	3	0901			0963			1025			1087			1149			1211			1273			1335			1397			1459		
0778	GND05K		0840	GND14D	3	0902			0964			1026			1088			1150			1212			1274			1336			1398			1460		
0779	GND21K		0841	09C07	3	0903			0965			1027			1089			1151			1213			1275			1337			1399			1461		
0780	GND22K		0842	MX011	3	0904			0966			1028			1090			1152			1214			1276			1338			1400			1462		
0781	GND24K		0843	15H08	10	0905			0967			1029			1091			1153			1215			1277			1339			1401			1463		
0782	GND06J		0844	13H06	10	0906			0968			1030			1092			1154			1216			1278			1340			1402			1464		
0783	GND17J		0845	RELA1	10	0907			0969			1031			1093			1155			1217			1279			1341			1403			1465		
0784	GND18T		0846	02K06	10	0908			0970			1032			1094			1156			1218			1280			1342			1404			1466		
0785	GND01H		0847	06M01	10	0909			0971			1033			1095			1157			1219			1281			1343			1405			1467		
0786	GND12H		0848	06M13	10	0910			0972			1034			1096			1158			1220			1282			1344			1406			1468		
0787	GND18D		0849	06M04	10	0911			0973			1035			1097			1159			1221			1283			1345			1407			1469		
0788	GND17D		0850	06M10	10	0912			0974			1036			1098			1160			1222			1284			1346			1408			1470		
0789	GND16B		0851	GND05M	10	0913			0975			1037			1099			1161			1223			1285			1347			1409			1471		
0790	GND12A		0852	05M09	10	0914			0976			1038			1100			1162			1224			1286			1348			1410			1472		
0791	GND16D		0853	02K12	10	0915			0977			1039			1101			1163			1225			1287			1349			1411			1473		
0792	GND13D		0854	02K08	10	0916			0978			1040			1102			1164			1226			1288			1350			1412			1474		
0793	GND22A		0855	GND02M	10	0917			0979			1041			1103			1165			1227			1289			1351			1413			1475		
0794	GND22B		0856	02M05	10	0918			0980			1042			1104			1166			1228			1290			1352			1414			1476		
0795	GND22C		0857	22M06	10	0919			0981			1043			1105			1167			1229			1291			1353			1415			1477		
0796	GND22E		0858			0920			0982			1044			1106			1168			1230			1292			1354			1416			1478		
0797	GND25K		0859	10A11	13	0921			0983			1045			1107			1169			1231			1293			1355			1417			1479		
0798	GND25R		0860	10A08	13	0922			0984			1046			1108			1170			1232			1294			1356			1418			1480		
0799	GND17E		0861	CSTRIN10	13	0923			0985			1047			1109			1171			1233			1295			1357			1419			1481		
0800	GND21D		0862	CSTRIN00	13	0924			0986			1048			1110			1172			1234			1296			1358			1420			1482		
0801	GND21A		0863	RFCTLD0	13	0925			0987			1049			1111			1173			1235			1297			1359			1421			1483		
0802	GND21B		0864	PFSD1A	13	0926			0988			1050			1112			1174			1236			1298			1360			1422			1484		
0803			0865	TAST0	16	0927			0989			1051			1113			1175			1237			1299			1361			1423			1485		
0804	GND24M		0866	BA080	3	0928			0990			1052			1114			1176			1238			1300			1362			1424			1486		
0805	GND25M		0867	17A08	14	0929			0991			1053			1115			1177			1239			1301			1363			1425			1487		
0806	GND26R		0868	16E11	14	0930			0992			1054			1116			1178			1240			1302			1364			1426			1488		

NOTES

REVISIONS

NETS 826 THRU 851 WERE NOT SPECIFIED				
RJS		4763	8-18-81	R01
16.1 E16 WAS MNEMONIC "06L03"				
JLV	GJ	4835	R	11-11-81	R02
ADDED NETS E16, F16.				
KR	GJ	4900	R	12-2-81	R03
ADDED NETS 886-888				
KR	GJ	4909	M	1/26/82	R04
ADDED NETS 889 & 890				
JAH	GJ	5089	MS	8/31/82	R05

UNLESS OTHERWISE SPECIFIED

SCALE: NONE

TOLERANCE:

DIMENSIONS ARE IN INCHES

.XXX ±.005 .X ±.03
.XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
		DES/DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE

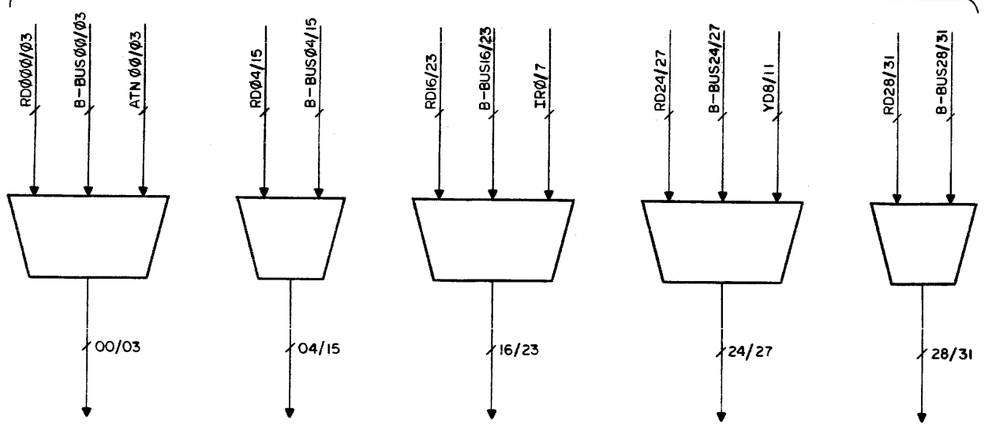
LBC
(8 MB CAPABILITY)

TASK 03183 | SHT

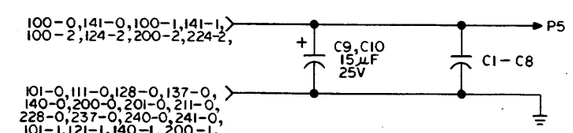
DWG 35-806 R05 D08 | 18-18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

BACKPANEL
CPU-A



TEST AID
DISPLAY



CONN	TERM. NO.	CABLE CONNECTOR MAP ROW 2	CABLE CONNECTOR MAP ROW 1	BACK PANEL MAP ROW 1	BACK PANEL MAP ROW 2	TERM. NO.	CONN
2	16			P5		41	1
	15			GND	GND	40	
	14					39	
	13					38	
	12					37	
	11					36	
	10					35	
	09			RD22I	RD23I	34	
	08			RD2ØI	RD2II	33	
	07				RDI9I	32	
	06			RDI7Ø	RDI8I	31	
	05				RD27I	30	
	04			RD25I	RD26I	29	
	03			RD24Ø	RDI2I	28	
	02			RDI4I	RDI3I	27	
	01			RDI5Ø	RDI6I	26	
	00			RDØØI	RDØII	25	
				RDØ2I	RDØ3I	24	
				RDØ4I	RDØ5I	23	
	24			RD3ØI	RD3II	22	
	23			GND	GND	21	
	22			RDØ9Ø	RDIØØ	20	
	21			RDIIØ		19	
	20			RD28I	RD29I	18	
	19					17	
	18					16	
	17					15	
	16					14	
	15					13	
	14			IRØ7Ø	IRØ6Ø	12	
	13			IRØ5Ø	IRØ4Ø	11	
	12			IRØ3Ø	IRØ2Ø	10	
	11			IRØIØ	IRØØØ	09	
	10			YDØ8I	YDØ9I	08	
	09			YDIØI	YDIII	07	
	08			FLR28I	FLR29I	06	
	07			FLR3ØI	FLR3II	05	
	06					04	
	05					03	
	04					02	
	03			GND	GND	01	
	02			P5	GND	00	
	01						
	00			P5	GND	41	
				GND	GND	40	
						39	
						38	
				GND	GND	37	
	24	P5	P5			36	
	23	GND	GND			35	
	22					34	
	21	FLR29Ø	FLR28Ø			33	
	20	FLR3IØ	FLR3ØØ			32	
	19	MXDØ11	MXDØØ1	SFTENØ	DFTENØ	31	
	18	MXDØ31	MXDØ21	ATNØØØ	ATNØIØ	30	
	17	MXDØ51	MXDØ41	ATNØ2Ø	ATNØ3Ø	29	
	16	MXDØ71	MXDØ61	GND	GND	28	
	15	MXDØ91	MXDØ81	BØØI	BØII	27	
	14	MXDIII	MXDIØI	BØ2I	BØ3I	26	
	13	MXDI3I	MXDI2I	BØ4I	BØ5I	25	
	12	MXDI5I	MXDI4I	BØ6I	BØ7I	24	
	11	MXDI7I	MXDI6I	BØ8I	BØ9I	23	
	10	MXDI9I	MXDI8I	BIØI	BIIII	22	
	09	MXD2II	MXD20I	BI2I	BI3I	21	0
	08	MXD23I	MXD22I	BI4I	BI5I	20	
	07	MXD25I	MXD24I	BI6I	BI7I	19	
	06	MXD27I	MXD26I	BI8I	BI9I	18	
	05	MXD29I	MXD28I	B2ØI	B2II	17	
	04	MXD3II	MXD3ØI	B22I	B23I	16	
	03	IRØ	RDØ	B24I	B25I	15	
	02			B26I	B27I	14	
	01	GND	GND	B28I	B29I	13	
	00	P5	P5	B3ØI	B3II	12	
				GND	GND	11	
						10	
	16					09	
	15					08	
	14					07	
	13					06	
	12					05	
	11					04	
	10					03	
	09					02	
	08			GND	GND	01	
	07			P5	GND	00	
	06						
	05						
	04						
	03						
	02						
	01						
	00						

REF. DESIG.	PART NUMBER	SPARE OUTPUT
AØ6	19-154	02,04,12
AØ5	19-057	08
AØ2	19-154	06

SPARE I.C.'S

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

REVISIONS
RELEASED FOR PRODUCTION
ENG. [signature] DATE 1-4-80

USED IN MANUAL :
29-695

35-734MOI	R00
BOARD	REV.

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

REVISION	○	○
SHEET	1	2

NOTES:
1. UNLESS OTHERWISE SPECIFIED :
   A. ALL RESISTORS ARE ±5%, 1/4W
   B. ALL CAPACITORS ARE .1μF, 30V

SCALE —

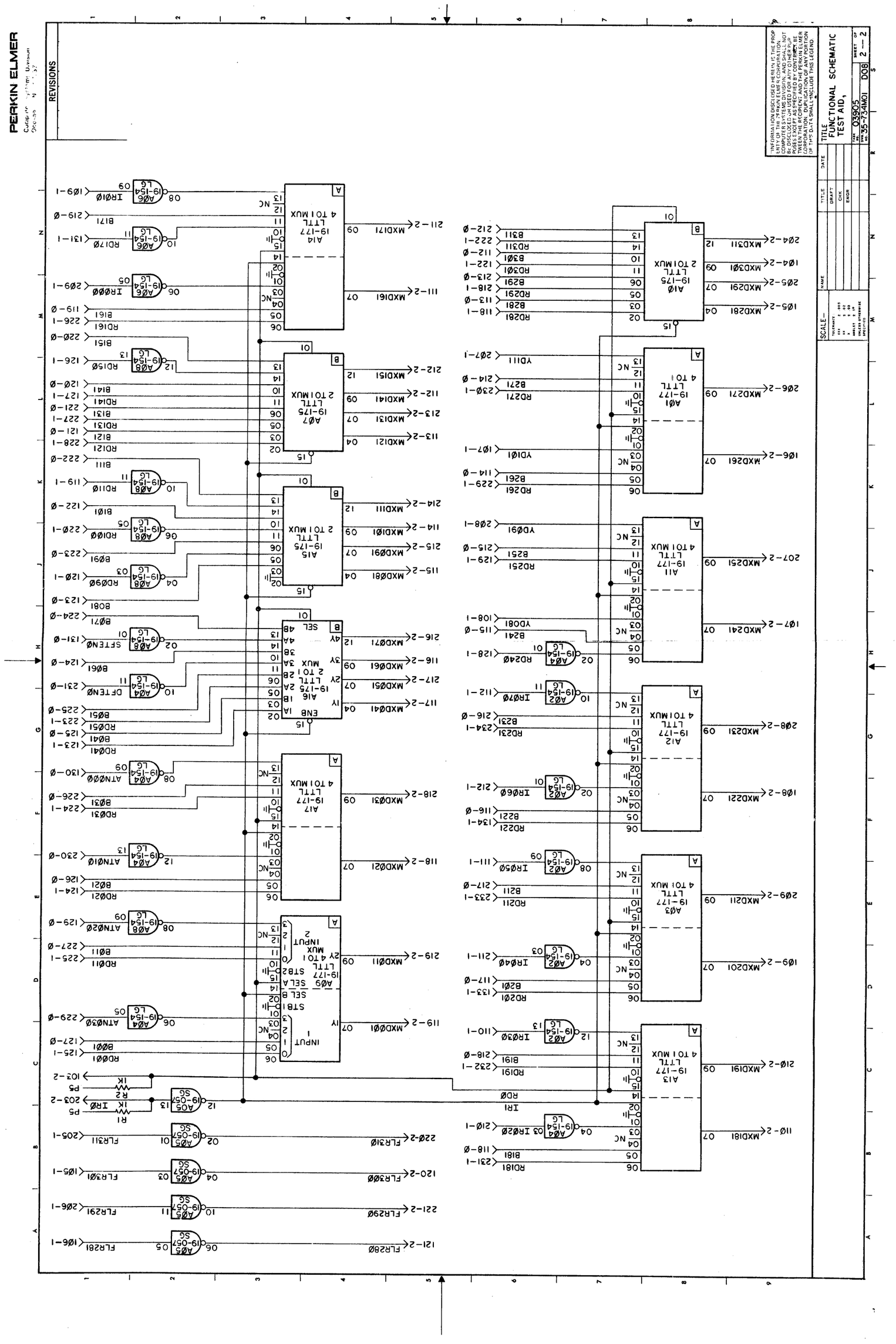
TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	11-1-79
E. GREENSTEIN	SYS.TEST	5-13-80
E. MARCH	ENGR	5-13-80
R. BARKER	Q.C.	5-8-80
D. FRANKENBERGER	MGR.	5-13-80

TITLE
FUNCTIONAL SCHEMATIC
TEST AID

TAB NO. 03976
DWG NO 35-734MOI D08
SHEET OF 1 — 2

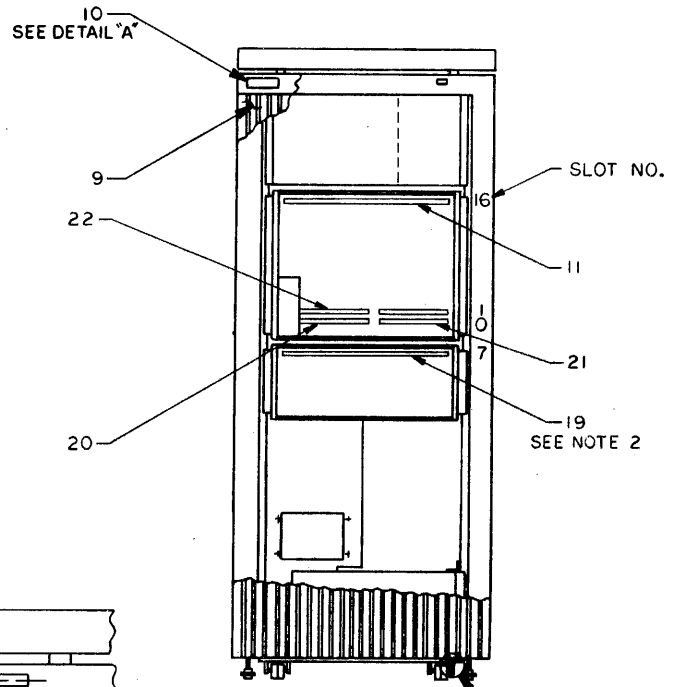
BRUNING 44-231 24538


PERKIN ELMER
REVISIONS
TITLE
FUNCTIONAL SCHEMATIC
TEST AID,
SCALE—
DRAFT
CHK
ENGR
DATE
NAME
CAGE 03505
SIZE D08
SHEET 2 OF 2
35-734M01
A07 19-175 LTTL 2 TO 1 MUX
A14 19-177 LTTL 4 TO 1 MUX
A10 19-175 2 TO 1 MUX
A01 19-177 4 TO 1
A15 19-175 2 TO 1 MUX
A11 19-177 4 TO 1 MUX
A16 19-175 2 TO 1 MUX
A12 19-177 4 TO 1 MUX
A17 19-177 4 TO 1 MUX
A03 19-177 4 TO 1 MUX
A09 19-177 2 TO 4 MUX
A13 19-177 4 TO 1 MUX
A05 19-057 SG
A06 19-154 LG
A08 19-154 LG
A04 19-154 LG
A02 19-154 LG

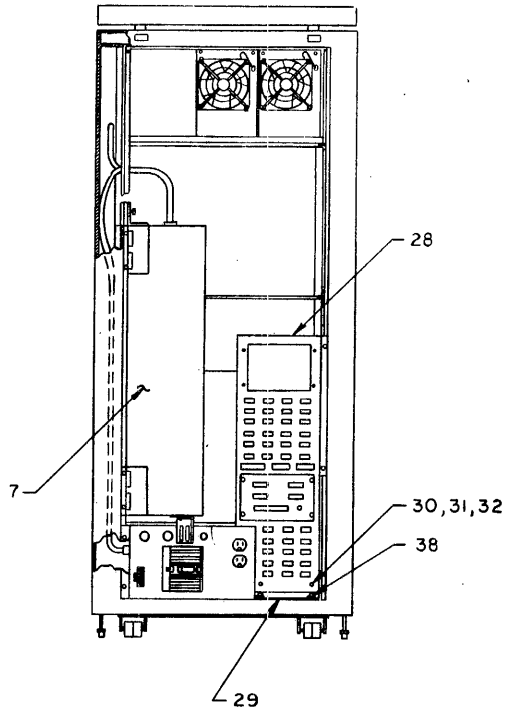
MILLIMETERS	INCHES
25.4	1.0

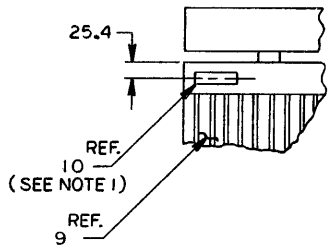
REVISIONS				
PRE PRODUCTION APPROVAL	INIT	DATE		
	DEV	7-25-80		
	PROD	7-25-80		
ADDED "SEE NOTE 2" TO ITEM 19, AREA E4. CHG'D NOTE 2.				
E.J.	4526	R	10-28-80	RQ1
AREA E3, DELETED ITEM 18, USED IN MANUAL WAS 47-010 TITLE WAS BASIC 3225 CABINET				
FM	4526	R	3-5-81	R02

RELEASED FOR PRODUCTION
MFG. ENG. [signature] DATE 10/16/81

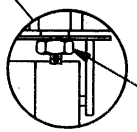


FRONT VIEW





DETAIL "A"
SCALE — NONE



ADJUST DOOR HEIGHT LEVEL WITH TOP OF CABINET. SECURE WITH #10-32 HEX. NUTS.

USED IN MANUAL
47-004

METRIC

TOL. IN MILLIMETERS
X ±.8
.X ±.5
.XX ±.13
UNLESS OTHERWISE SPECIFIED

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

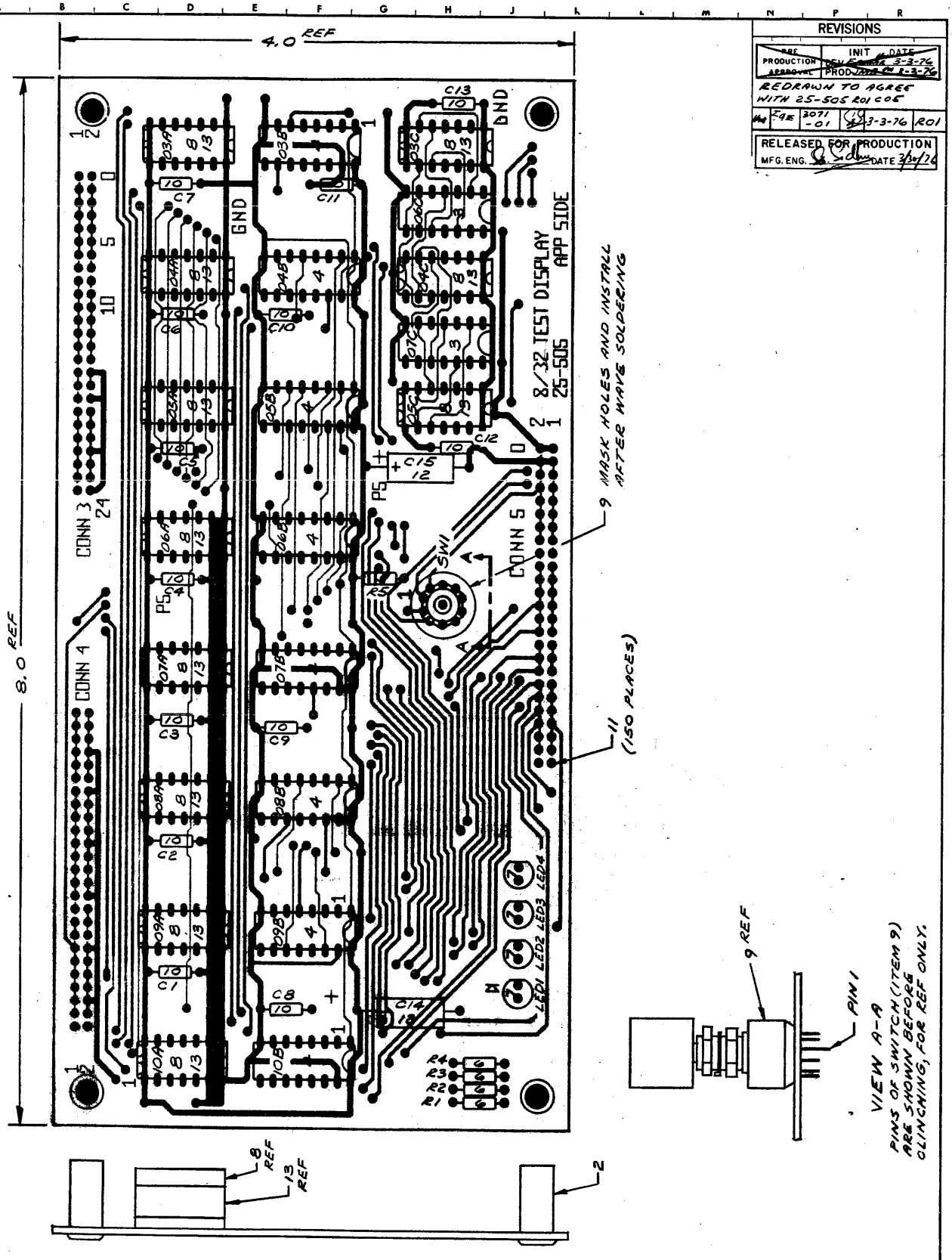
NOTES:
1. ALIGN LOGO ON FIRST RIB OF DOOR & CENTER AS SHOWN.
2. BASIC I/O, MEMORY CONFIGURATION AND BOARD LOCATION (ITEM 19). MAY BE RECONFIGURED PER CUSTOMER ORDER.
3. ITEM 24 NOT SHOWN

UNLESS OTHERWISE SPECIFIED			
SCALE: 1:8	TOLERANCE IN INCHES: .XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
DIMENSIONS ARE IN MILLIMETERS			
NAME		TITLE	DATE
R. MARCUS		DES/DFT	6-2-80
R. CERO		SUPV	10-16-81
		CHK	
R. DENGEL		ENG	10-16-81
P. ABITANTE		MGR	10-16-81
R. BARKER		QC	10-16-81

TITLE ASSEMBLY
BASIC 3230 CABINET
512KB MOS

TASK 03977 SHT
DWG 01-142R02.C03 1-1

BRUNING 44-131 40579



REVISIONS			
PRODUCTION APPROVAL	INIT	DATE	
	PROD	3-3-76	
REDRAWN TO AGREE WITH 25-505 R01 CO5			
MN	3071 -01	3-3-76	R01

RELEASED FOR PRODUCTION
MFG. ENG. DATE 3/30/76

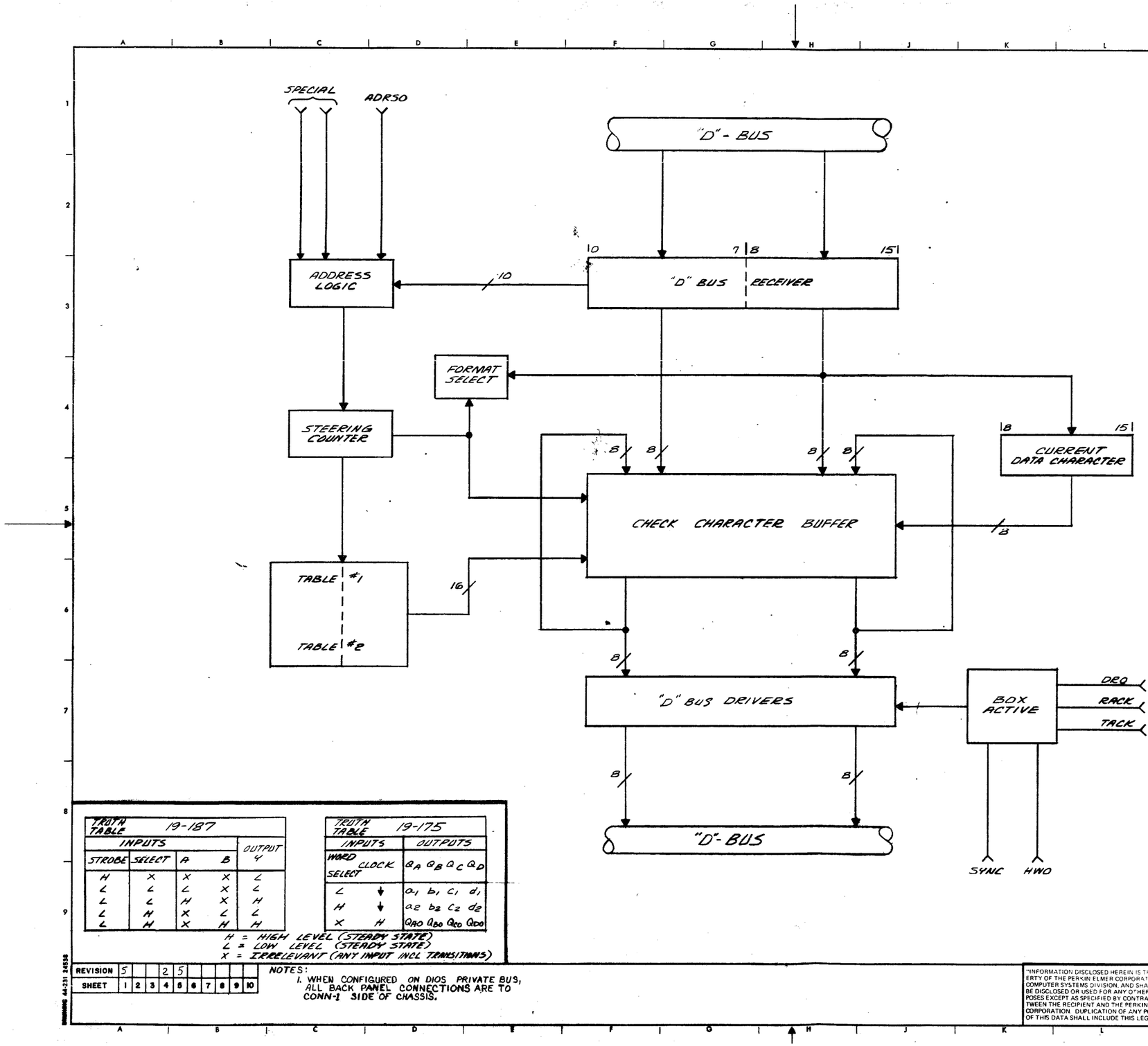
DIMENSIONS ARE IN INCHES

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

SCALE—2:1	NAME	TITLE	DATE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .09, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	H. MATTER	DRAFT	3-3-76
		CHK	3-30-76
	T. FYFE	ENGR	3-30-76
	R.A. BARKER	QC	3-30-76
	S. MESSINA	MGR	3-30-76

TITLE: ASSEMBLY 8/32 TEST DISPLAY

TASK NO. 03071 | DWG. NO. 35-612 R01 C03 | SHEET OF 1—1



TRUTH TABLE 19-187				
INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

TRUTH TABLE 19-175		
INPUTS		OUTPUTS
WORD SELECT	CLOCK	Q_A Q_B Q_C Q_D
L	↓	a_1 b_1 c_1 d_1
H	↓	a_2 b_2 c_2 d_2
X	H	Q_{A0} Q_{B0} Q_{C0} Q_{D0}

H = HIGH LEVEL (STEADY STATE)
L = LOW LEVEL (STEADY STATE)
X = IRRELEVANT (ANY INPUT INCL TRANSITIONS)

REVISION	5			2	5					
SHEET	1	2	3	4	5	6	7	8	9	10

NOTES:
1. WHEN CONFIGURED ON DIOS PRIVATE BUS, ALL BACK PANEL CONNECTIONS ARE TO CONN-1 SIDE OF CHASSIS.

DRAWING 44-231 24558

BACK PANEL MAP ROW 1	BACK PANEL MAP ROW 2	TERM. NO.	CONN
		41	
		40	
		39	
		38	
		37	
		36	
		35	
		34	
		33	
		32	
		31	
		30	
		29	
		28	
		27	
		26	
		25	
		24	
		23	
		22	
		21	1
		20	
		19	
		18	
		17	
		16	
		15	
		14	
		13	
		12	
		11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
		01	
		00	
PS GND	GND GND	41	
		40	
		39	
		38	
		37	
		36	
		35	
BCNT0 (F00 ONLY)	BADR0 (F00 ONLY)	34	
		33	
		32	
		31	
		30	
		29	
		28	
	DCRQ (F00 ONLY)	27	
SCLRQ	HWO	26	
PRACK0 (F01 ONLY)		25	
DBCNT0 (F01 ONLY)	CBIN0 (F01 ONLY)	24	
SYNQ		23	
ACKQ	TACK0 (F00 ONLY)	22	
		21	0
DRQ	CMD0	20	
	ADR50	19	
D140	D150	18	
D120	D130	17	
D100	D110	16	
D080	D090	15	
D060	D070	14	
D040	D050	13	
D020	D030	12	
D000	D010	11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
GND	GND	01	
PS	GND	00	

SEE NOTE 1

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

PRE PRODUCTION APPROVAL	DEV	INIT	DATE 4-20-76	
REVISED SHT 5. 35-622 (BELOW) WAS R00				
PE 03073-		4-5-76	R01	
REVISED SHTS 1, 4, & 5. 35-622 (BELOW) WAS R01.				
PE 03073-		4-20-76	R02	
RELEASED FOR PRODUCTION DATE 4/27				
REVISED SHT 5. BOARD REV LEVEL WAS R02				
KW 3883	M	2-14-79	R03	
ADDED NOTE 1 & USED IN MANUAL. BOARD REV WAS R03. REVISE SHTS 4&5. ADDED F00 & F01 ONLY TO BACK PANEL MAP. ALSO ON SHT 5 ADDED F00 & F01 VARIATIONS.				
KR 3938	M	9-13-79	R04	
AREA 59: DELETED 29-683 & ADDED 47-009 & 47-009 TO "USED IN MANUAL" AREA 58: 35-622 F01 WAS R01 & 35-622 WAS R05. REVISED SHTS. 1 & 5.				
MV 4683	MS	5-27-81	R05	

USED IN MANUALS
29-519, 29-724, 29-695, 29-520, 47-004, 47-009

BOARD	REV LEVEL
35-622 F01	R01
35-622	R06

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

SCALE —

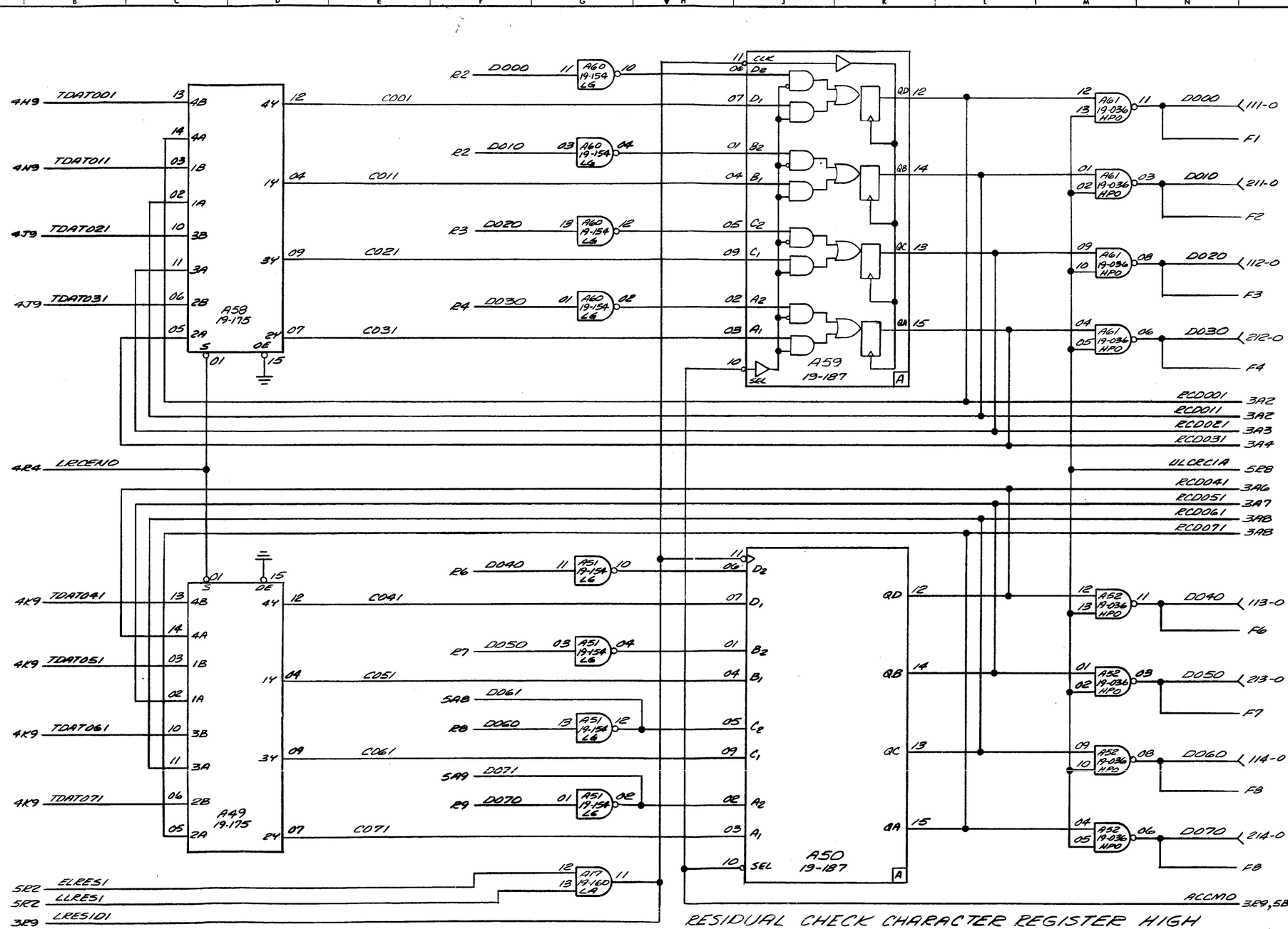
NAME	TITLE	DATE
V. PERRI	DRAFT	1-30-76
R. REDO	CHK	1-30-76
G. JOYCE	ENGR	4-28-76
E.A. BARLEE		4-28-76
S. MESSINA	MGR.	4-28-76

TITLE FUNCTIONAL SCHEMATIC COMM. HDW. ASSIST BD

TASK NO. 03073 SYS NO. 02-428/05008 SHEET OF 1-5

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



SCALE—

TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
V. PERRI	DRAFT	1-21-76
	CHK	
	ENGR	

TITLE

TASK NO. 03073 SHEET OF

DWG NO. 02-428 D08 2-5

BRUNING 44-231 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

RESIDUAL CHECK CHARACTER REGISTER LOW

A91 19-175 (A32 19-175)

4B9	LRCD0B1	13	4B
2R4	RCDD01	12	A40 19-172 LXE
4L9	TDAT0B1	13	A40 19-172 LXE
		11	4A
4B9	LRCD091	10	3B
2R4	RCDD11	09	A40 19-172 LXE
4M9	TDAT091	10	A40 19-172 LXE
		08	3A
4C9	LRCD101	03	1B
2R5	RCDD21	02	A40 19-172 LXE
4M9	TDAT101	01	A40 19-172 LXE
		03	02 1A
4C9	LRCD111	06	2B
2R5	RCDD31	05	A40 19-172 LXE
4M9	TDAT111	04	A40 19-172 LXE
		06	05 2A
		S	01
		OE	15
4R5	LRCEN1		
4E9	LRCD121	13	4B
2R5	RCDD41	12	A31 19-172 LXE
4N9	TDAT121	13	A31 19-172 LXE
		11	4A
4F9	LRCD131	10	3B
2R5	RCDD51	09	A31 19-172 LXE
4N9	TDAT131	10	A31 19-172 LXE
		08	3A
4F9	LRCD141	03	1B
2R6	RCDD61	02	A31 19-172 LXE
4N9	TDAT141	01	A31 19-172 LXE
		03	02 1A
4G9	LRCD151	06	2B
2R6	RCDD71	05	A31 19-172 LXE
4P9	TDAT151	04	A31 19-172 LXE
		06	05 2A
		S	01
		OE	15

A42 19-187 (A33 19-187)

R2	D0B1	11	C2
		09	C1
			QC 13
R3	D091	06	D2
		07	D1
			QD 12
R3	D101	01	B2
		04	B1
			QB 14
R4	D111	02	A2
		03	A1
			QA 15
		10	SEL
			A
R6	D121	11	C2
		09	C1
			QC 13
R7	D131	06	D2
		07	D1
			QD 12
R8	D141	01	B2
		04	B1
			QB 14
R9	D151	02	A2
		03	A1
			QA 15
		10	SEL
			A

C0B1	12	4Y	
C091	09	3Y	
C101	04	1Y	
C111	07	2Y	
C121	12	4Y	
C131	09	3Y	
C141	04	1Y	
C151	07	2Y	

04	A44 19-036 HPD	06	D0B0 <115-0
03	A43 19-154 LG	04	D0B1 H1, 4M1, 5B7
01	A44 19-036 HPD	03	D090 <215-0
01	A43 19-154 LG	02	D091 H2, 4M1, 5B6
12	A44 19-036 HPD	11	D100 <116-0
13	A43 19-154 LG	12	D101 H3, 4L1, 5B6
09	A44 19-036 HPD	08	D110 <216-0
10	A43 19-154 LG	10	D111 H3, 4L1, 5B5
04	A35 19-036 HPD	06	D120 <117-0
03	A34 19-154 LG	04	D121 H6, 4L1, 5B5
01	A35 19-036 HPD	03	D130 <217-0
01	A34 19-154 LG	02	D131 H7, 4L1, 5B7
12	A35 19-036 HPD	11	D140 <118-0
13	A34 19-154 LG	12	D141 H7, 4L1, 5B7
09	A35 19-036 HPD	08	D150 <218-0
10	A34 19-154 LG	10	D151 H8, 4L1, 5B8

RCD0B1 4D9
RCD091 4D9
RCD101 4D9
RCD111 4D9
RCD121 4D9
RCD131 4D9
RCD141 4E9
RCD151 4E9

LLCRC1 5R7
ACCM0 2P9
LRESID1 2A9

SCALE —	NAME	TITLE	DATE
TOLERANCE XXX ± .005, FX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	V. PERRI	DRAFT	1-21-76
		CHK	
		ENGR	

TITLE

TASK NO. 03073 SHEET 3 OF 5
DWG NO. 02-428 DOB

BRUNING 44-231 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
AREA M4: ADDED K, L, M STRAP OPTION AND NOTE 1			
PA	03078	4-20-76	R01
ADDED 3220 & 3240 PROCESSOR TO NOTE 1.			
KR	3938	M 9-4-79	R02

LDATA1 5R3 · LFMT1 5R1 · D15I 3R9 · D14I 3R8 · D13I 3R7 · D12I 3R6 · D11I 3R4 · D10I 3R3 · D09I 3R3 · D08I 3R2 · ADES1 5D4 · LLCRC1 5R7 · CLRNTD 5B1

19-167 A37 HDFF

19-167 A28 HDFF

P9 1K · P5

P10 1K · P5

A48D 19-165 DS LSDF

00 = BISYNC (CRC-16)
10 = LRC
01 = SDLC

SEE NOTE 1

P5 · E1 6.8K · P5 · E4 1K

EXC EXR · A6 19-042 · POS · N.C.

A57 19-153 LSG

LRCENO 2A5

LRCENI 3A5

A38 19-172 LSX

A29 19-172 LSX

CURRENT CHARACTER REGISTER
CRC TABLES FORMAT REGISTER

A56 19-195 F01 · A47 19-195 F02 · A39 19-195 F03 · A30 19-195 F04

LRCD00I 3A1 · LRCD01I 3A2 · LRCD10I 3A3 · LRCD11I 3A3 · ECD08I 3A4 · ECD09I 3A5 · ECD10I 3A5 · ECD11I 3A5 · ECD12I 3A5 · ECD13I 3A5 · ECD14I 3A5 · ECD15I 3A5 · LRCD12I 3A6 · LRCD13I 3A7 · LRCD14I 3A7 · LRCD15I 3A8

TDAT00I 2A1 · TDAT01I 2A2 · TDAT02I 2A3 · TDAT03I 2A3 · TDAT04I 2A6 · TDAT05I 2A7 · TDAT06I 2A7 · TDAT07I 2A8 · TDAT08I 3A2 · TDAT09I 3A2 · TDAT10I 3A3 · TDAT11I 3A4 · TDAT12I 3A6 · TDAT13I 3A7 · TDAT14I 3A8 · TDAT15I 3A8

1. AS SHOWN IS STRAPPED FOR 7/32C PROCESSOR, 3220 PROCESSOR OR DIOS OPERATIONS (K TO L).
FOR 8/32 PROCESSOR OR 3240 PROCESSOR OPERATIONS REMOVE STRAPS FROM K TO L AND ADD STRAP FROM K TO M.

SCALE —	NAME	TITLE	DATE	TITLE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT		
		CHK		
		ENGR		
				TASK NO. 03073
				DWG NO. 02-428 FORDOB
				SHEET 4-5

BRUNING 44-231 24536

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
AREA B3: ADDED R11, R12, C50 & C51. AREA E8: DELETED R6 & C1. AREA D1 & E9: REMOVED 16 DECOUPLING CAPS. ADDED NOTES 1 & 2. A2C-12 WAS SCLRO. A17-01 WAS CLRNTO. A17-02 WAS ACCMO. A17-03 WAS CLRNTO
REV A/J 03073 S 4-5-76 R01
AREA D4: ADDED ADRSI CROSS REF. AREA F6: CONNECTED A19-04 TO A19-01. A19-04 WAS TO A19-18.
REV A/J 03073 T 4-20-76 R02
AREA F-5. ADDED SPARE GATE A21 PINS 8 & 9. A20 PIN 1 WAS TO A19 PIN 10.
REV A/J 3883 M 3-19-79 R03
EXTENSIVE CHANGES IN AREAS B3-4, ADDED FOO & FOI VARIATIONS. SEE MICRO FILM REV R03 FOR PREVIOUS CHANGES.
REV KR/J 3938 M 9-13-79 R04
AREA F6 ADDED A11, A20-02 WAS TO A19-03
REV A/J 4683 MS 5-27-81 R05

TIMING & CONTROL

DECOUPLING CAPACITORS

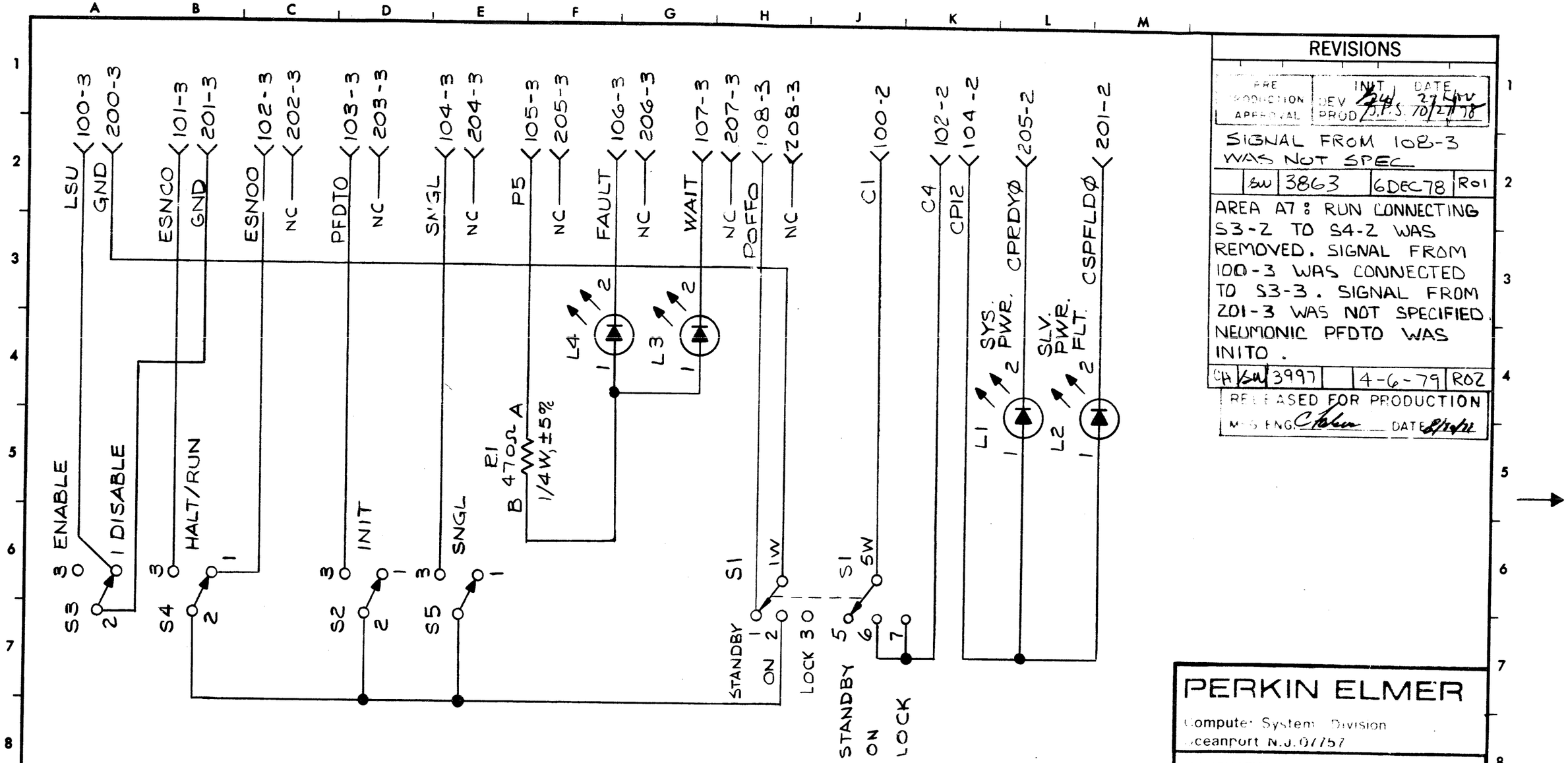
NOTES:
1. WHEN USED ON A 7/32C PROCESSOR 3220 PROCESSOR/DIOS 'TP4' MUST BE STRAPPED TO GROUND. WHEN USED ON AN 8/32 PROCESSOR OR 3240 PROCESSOR 'TP6' MUST BE STRAPPED TO GROUND.
2. WHEN USED ON A 7/32C PROCESSOR OR 3220 PROCESSOR 'G' MUST BE STRAPPED TO 'J' AS SHOWN. WHEN USED ON AN 8/32 PROCESSOR OR DIOS 'G' MUST BE STRAPPED TO 'H'.

SCALE—	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE

TASK NO. 03073
DWG NO. 02-428905 DOB
SHEET OF 5—5

BRUNING 44-231 24538



REVISIONS			
PRE PRODUCTION APPROVAL	INIT	DATE	
	DEV	27 Nov 78	
	PROD	D.P.S. 10/27/78	

SIGNAL FROM 108-3 WAS NOT SPEC

SW	3863	6DEC78	R01

AREA A7: RUN CONNECTING S3-2 TO S4-2 WAS REMOVED. SIGNAL FROM 100-3 WAS CONNECTED TO S3-3. SIGNAL FROM 201-3 WAS NOT SPECIFIED. NEUMONIC PFDTO WAS INITO.

CH	SW	3997	4-6-79	R02

RELEASED FOR PRODUCTION
MFG ENG. C Tobin DATE 8/28/79

PERKIN ELMER
Computer System Division
Oceanport N.J. 07757

NOTES

SCALE—

TOLERANCE:
.XXX ± .005
.XX ± .02
.X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

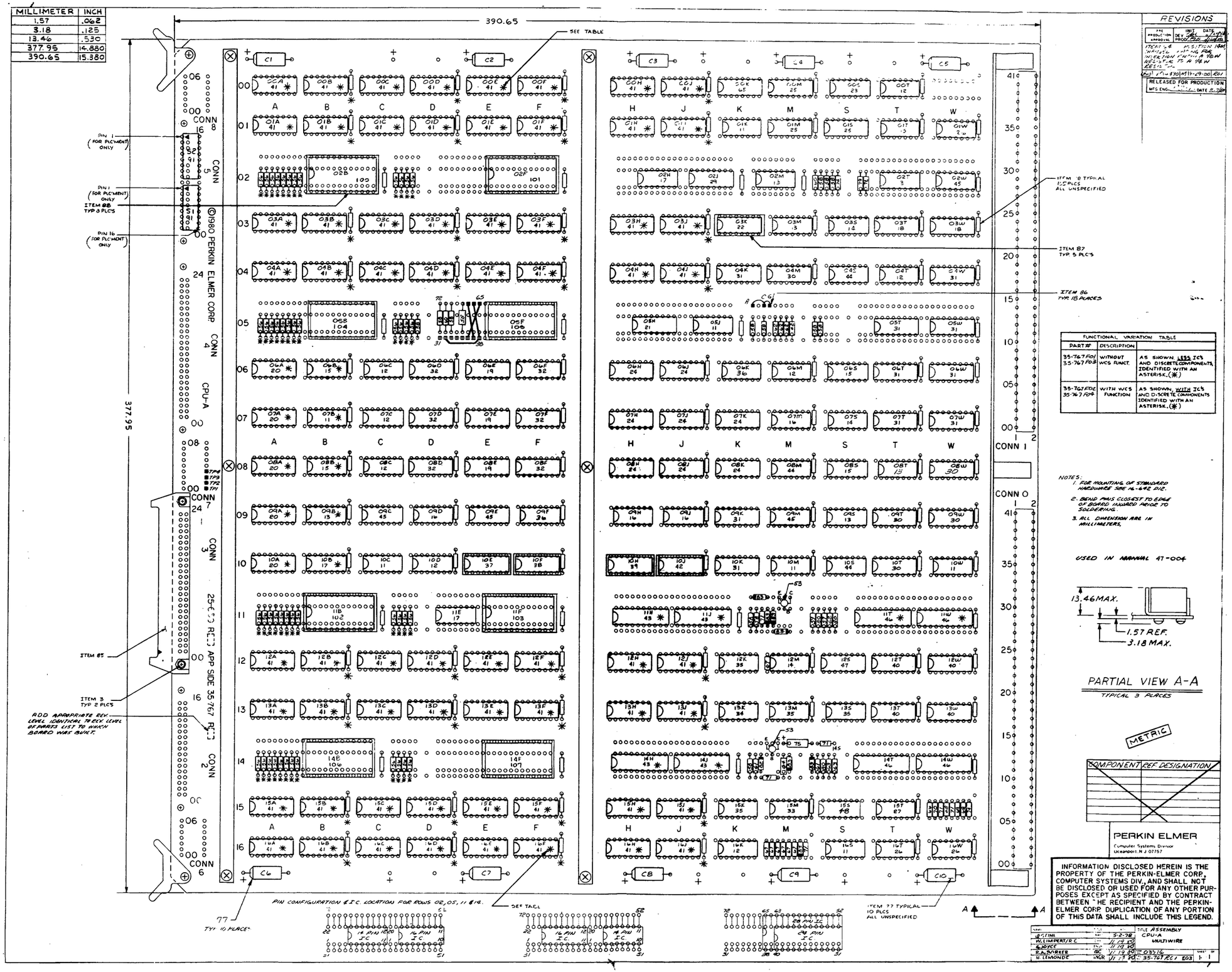
NAME		DRAFT	7-24-78
P.CARD			
R. BARKER		Q.C	8.28.79
R. CERO		CHK	8.28.79
G. WELLY		ENGR	8.28.79
E. GREENSTEIN		SYS. TEST	8.28.79
P. ABITANTE		MGR.	8.28.79

TITLE SCHEMATIC
SYSTEM CONTROL

TASK NO. 03916
DWG. NO. 09-108 R02B08
SHEET OF 1—1

OGILVIE PRESS

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530
377.95	14.880
390.65	15.380



REVISIONS

THE PRODUCTION APPROVAL	INIT. DEV	DATE 11/19/79
	PROD	DATE 11/19/79

ITEM 18 POSITION 18A1, INITIAL +.22 PER PLC, INSERTION LENGTH A .700 MAX. INSERT. TO A 1/8 W RESIS.

Part 7 Rev 890419-9-00 Rel

RELEASED FOR PRODUCTION

MFG ENG. DATE 5-2-78

FUNCTIONAL VARIATION TABLE		
PART #	DESCRIPTION	
35-767 F01 35-767 F03	WITHOUT WCS RANGT.	AS SHOWN WITH IC'S AND DISCRETE COMPONENTS, IDENTIFIED WITH AN ASTERISK.(*)
35-767 F02 35-767 F04	WITH WCS FUNCTION	AS SHOWN, WITH IC'S AND DISCRETE COMPONENTS IDENTIFIED WITH AN ASTERISK.(*)

NOTES:
1. FOR MOUNTING OF STANDARD HARDWARE SEE 16-642 DI2.
2. BEND PINS CLOSEST TO EDGE OF BOARD, INWARD PRIOR TO SOLDERING.
3. ALL DIMENSION ARE IN MILLIMETERS.

USED IN MANUAL 47-004

PARTIAL VIEW A-A
TYPICAL 3 PLACES

METRIC

COMPONENT REF. DESIGNATION

PERKIN ELMER
Computer Systems Division
Ukiah, Calif. 95482

R. STINE	ENG	5-2-78	TITLE ASSEMBLY CPU-A MULTIWIRE
W. LIMPERT/R.C.	ENG	11-12-79	
A. JOYCE	PROD	11-12-79	
R.A. BARKER	QC	11-19-80	DWG 03316
M. LEMONDE	MGR	11-19-80	35-767 REV E03

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530
377.95	14.880
390.65	15.380

390.65

377.95

CONN 8 CONN 5 CONN 4 CPU-B CONN 2 CONN 3 CONN 7 CONN 6

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25 660 R... APP SIDE 35-768 R...

CONN 1 CONN 0

TYP. 119 PLCS ITEM 46

TYP. 10 PLCS ITEM 45

ITEM 50 (TYP. 2 PLCS)

ITEM 3 (TYP. 4 PLCS)

ADD APPROPRIATE REV. LEVEL IDENTICAL TO REV LEVEL OF PARTS LIST TO WHICH BOARD WAS BUILT.

PIN CONFIGURATION & IC LOCATION FOR ROWS 02, 05, 11, & 14

16 PIN IC

16 PIN IC

24 PIN IC

TYP. 10 PLCS ITEM 45

NOTES:
1. FOR MOUNTING OF STANDARD HARDWARE SEE ML-648 SHT.
2. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING.
3. ALL DIMENSIONS ARE IN MILLIMETERS.

USED IN MANUAL 47-004

13.46 MAX.

1.57 REF.

3.18 MAX.

PARTIAL VIEW A-A

TYPICAL 3 PLACES

METRIC

COMPONENT REF DESIGNATION

PERKIN ELMER
Computer Systems Division
Oceanport N J 07757

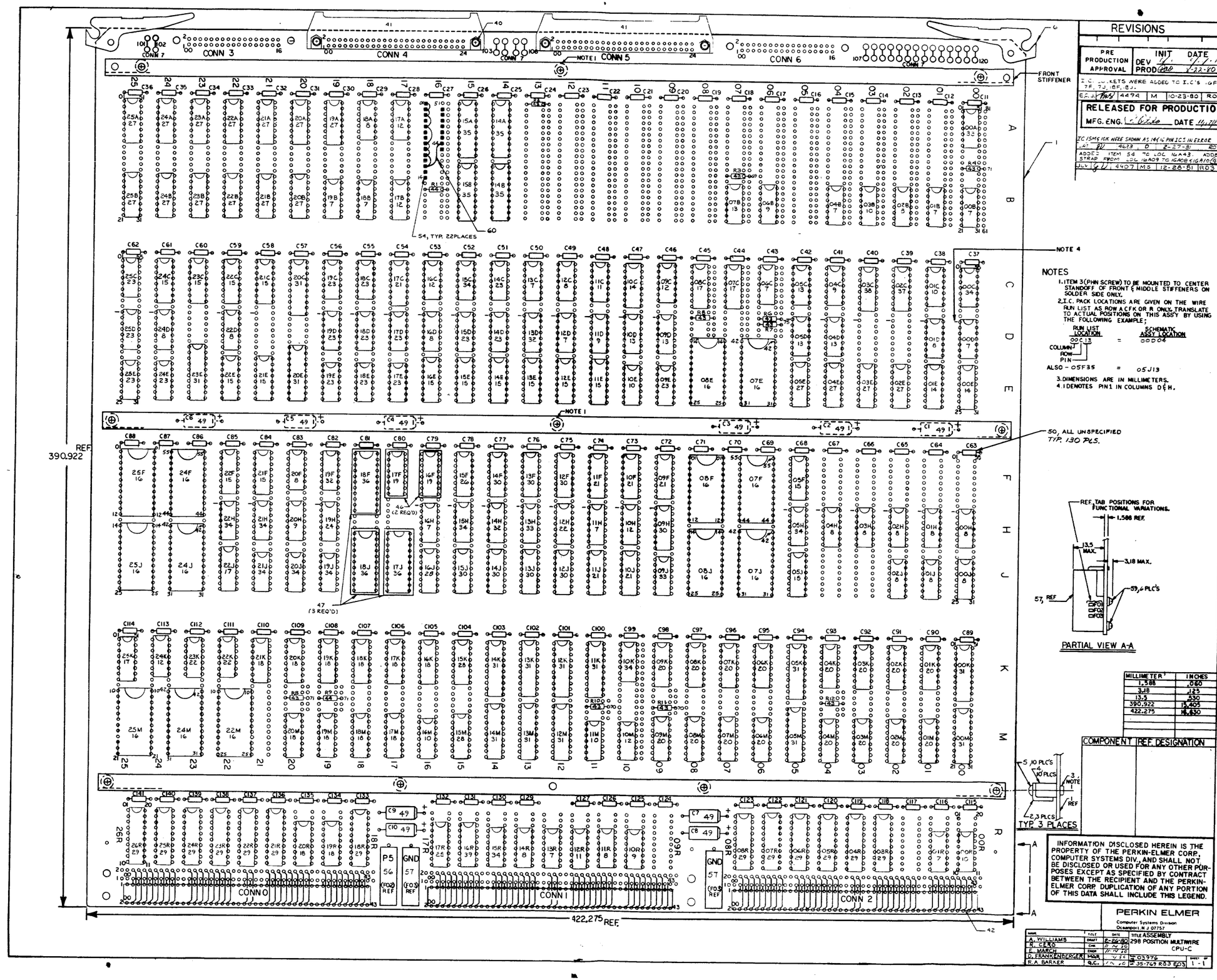
REVISIONS

REL PRODUCTION APPROVAL	DATE	BY

RELEASED FOR PRODUCTION
MFG ENG. CHAR DATE 7-27-78
RES. AT LOC 11 NOB - 11 MIS
WAS ITEM 46 D.
NO W/ 1 4660 E 11=38 R01

NAME	INIT.	DATE	TITLE
[illegible]	[illegible]		CPU-E
[illegible]	[illegible]		ASSEMBLY
R.D. BARKLE	RC	MAY	SIZE 039
[illegible]	[illegible]		35-768016 03

SHEET OF 1-1



REVISIONS

	PRE PRODUCTION APPROVAL	INIT	DATE
		DEV	4/1..
		PROD	4-22-80

I.C. SOCKETS WERE ADDED TO I.C.'S 10F, 7F, 7J, 16F, 8J.

E.J.		4494	M	10-23-80	R01

RELEASED FOR PRODUCTION

MFG. ENG. _____ DATE 11/7/80

IC 15M5 16K WERE SHOWN AS 14/16 PIN ICS IN ERROR

JAT		4623	D	2-27-81	R02

ADDED ITEM 54 TO LOC 16A43. ADDED STRAP FROM LOC 16A09 TO 16A08 & 16A10/GND

JLV		4907	MS	12-28-81	R03

NOTES

1. ITEM 3(PHN SCREW) TO BE MOUNTED TO CENTER STANDOFF OF FRONT & MIDDLE STIFFENERS ON SOLDER SIDE ONLY.
2. I.C. PACK LOCATIONS ARE GIVEN ON THE WIRE RUN LIST AS ROW A,C,F,K OR R ONLY. TRANSLATE TO ACTUAL POSITIONS ON THIS ASSY BY USING THE FOLLOWING EXAMPLE;

RUN LIST LOCATION		SCHEMATIC ASSY LOCATION
05J13	=	00D04

COLUMN / ROW / PIN

ALSO - 05F35 = 05J13

3. DIMENSIONS ARE IN MILLIMETERS.
4. 1 DENOTES PIN1 IN COLUMNS D & H.

PARTIAL VIEW A-A

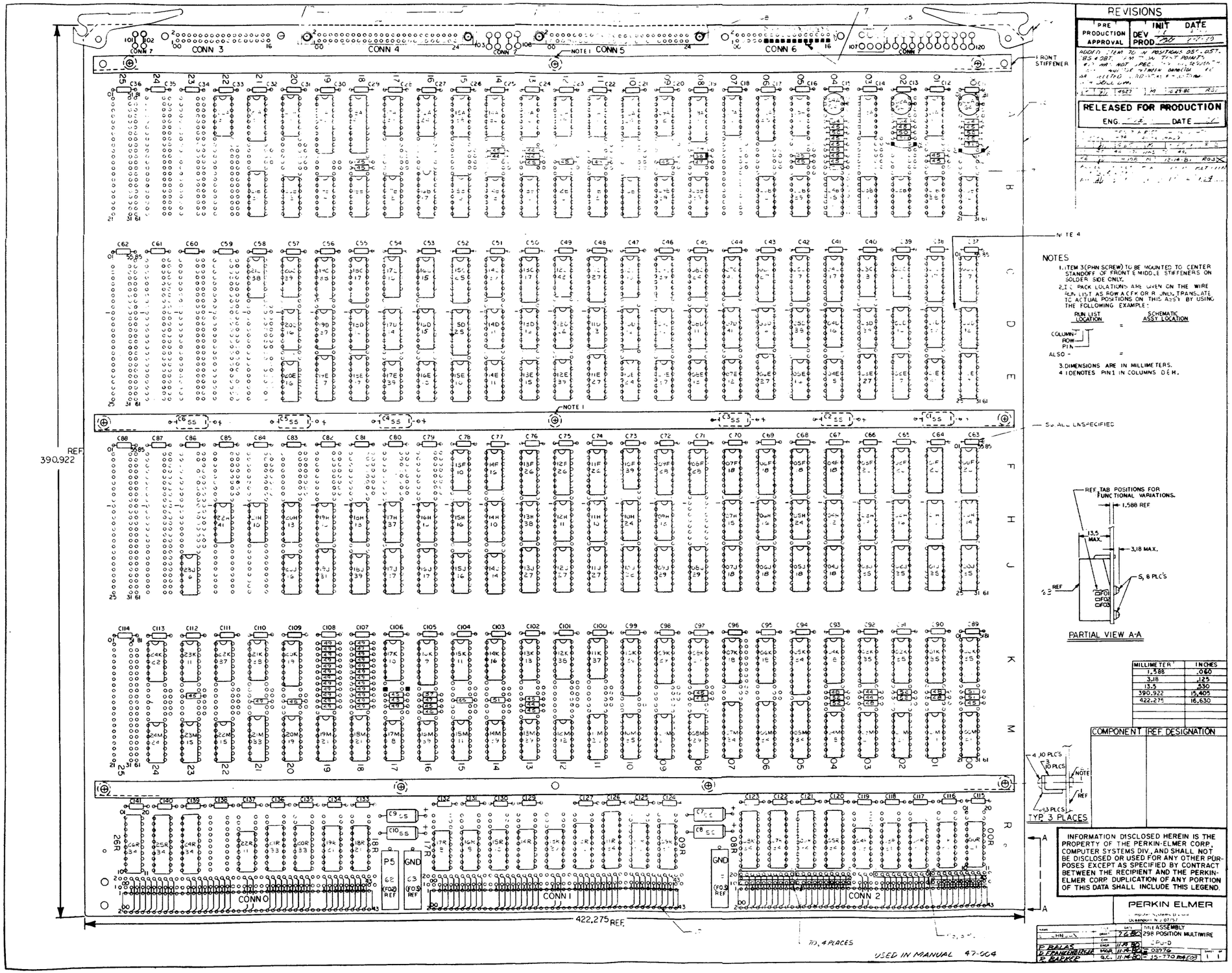
MILLIMETER	INCHES
1.588	.060
3.18	.125
13.5	.530
390.922	15.405
422.275	16.630

COMPONENT	REF. DESIGNATION

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

NAME	TITLE	DATE	TITLE ASSEMBLY
A. WILLIAMS	DRAFT	2-26-80	298 POSITION MULTIWIRE
R. CERO	CHK	3/14/80	CPU-C
E. MARCIN	ENGR	3/14/80	
D. FRANKENBERGER	MGR	4/1/80	03976
R.A. BARKER	Q.C.	4/14/80	35-769 R3 603

SHEET 1 OF 1 - 1



REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	C	7-7-80
PROD	JBC	11-19-80

ADDED ITEM 20 IN ASSEMBLY DES. LIST. ADDED DIM. AT TWO POINTS. REVISED NOTE 1. REMOVED NOTE 2. REVISED NOTE 3. REVISED NOTE 4. ADDED DIM. — JBC 11-19-80 RST

RELEASED FOR PRODUCTION
ENG. _____ DATE _____

12 AH 4115 M 12-16-81 ROS

NOTES

1. ITEM 3 (PHN SCREW) TO BE MOUNTED TO CENTER STANDOFF OF FRONT & MIDDLE STIFFENERS ON SOLDER SIDE ONLY.
2. I.C. PACK LOCATIONS ARE GIVEN ON THE WIRE RUN LIST AS ROW A,C,E,K OR R AND TRANSLATE TO ACTUAL POSITIONS ON THIS ASSY BY USING THE FOLLOWING EXAMPLE:

RUN LIST LOCATION	=	SCHEMATIC ASSY LOCATION
COLUMN-ROW-PIN	=	
ALSO -	=	

3. DIMENSIONS ARE IN MILLIMETERS.
4. ! DENOTES PIN 1 IN COLUMNS D & H.

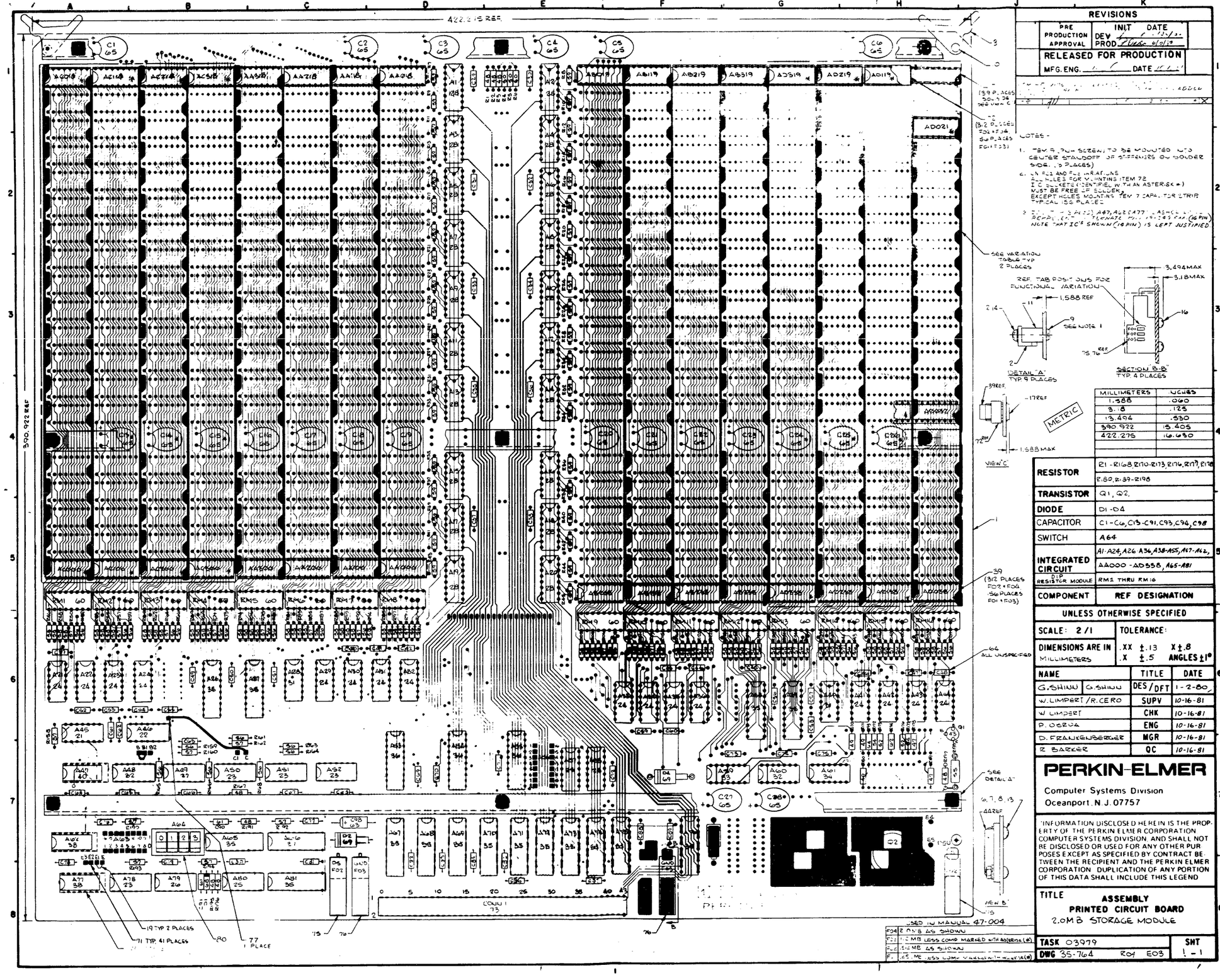
MILLIMETER	INCHES
1.588	.060
3.18	.125
13.5	.530
390.922	15.405
422.275	16.630

COMPONENT	REF. DESIGNATION

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

J. HINDS	DRAFT	7.6.82	TITLE ASSEMBLY 298 POSITION MULTIWIRE
P. BALAS	ENGR	11.19.80	SIZE D
D. FRANKENBERGER	ENGR	11.19.80	03976
R. BARKER	Q.C.	11.19.80	25-770 REV FOR

SHEET 1 OF 1



REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	12-1-80
	PROD	6/8/81

RELEASED FOR PRODUCTION

MFG. ENG. _____ DATE _____

199 PLACES SOLDER SIDE SEE VIEW C

70 (3.2 DIA) PLACES FOR F04 & F03 5 PLACES FOR F02 & F01

NOTES -

1. TSV 9 PIN SCREW TO BE MOUNTED WITH CENTER STANDOFF OF FASTENERS ON SOLDER SIDE. (5 PLACES)
2. CONFIGURATIONS ALL HOLES FOR MOUNTING ITEM 72. IC SOCKETS IDENTIFIED WITH AN ASTERISK (*) MUST BE FREE OF SOLDER. EXCEPT HOLES MOUNTING ITEM 7 CAP. FOR STRIP TYPICAL 158 PLACES
3. [illegible] A87, A22 [illegible] REPRESENTATIVE [illegible] 16 PIN) NOTE "NAT IC'S SHOWN (14 PIN) IS LEFT JUSTIFIED

SEE VARIATION TABLE TYP 2 PLACES

REF. TAB POSITIONS FOR FUNCTIONAL VARIATION

1.588 REF

2.14

SEE NOTE 1

DETAIL 'A' TYP 8 PLACES

3.494 MAX

3.18 MAX

16

FOR FUNCTIONAL VARIATION

15.76 REF

SECTION B-B TYP 4 PLACES

.39 REF.

.17 REF

.72 REF

1.588 MAX

VIEW 'C'

METRIC

MILLIMETERS	INCHES
1.588	.060
3.18	.125
13.494	.530
390.922	15.405
422.275	16.630

39 (3/2 PLACES FOR F04 & F03, 136 PLACES FOR F01 & F02)

64 ALL UNSPECIFIED

SEE DETAIL 'A'

6, 7, 8, 13

.44 REF

VIEW 'B'

RESISTOR	R1-R168, R170-R173, R176, R177, R178
	R180, R189-R198
TRANSISTOR	Q1, Q2,
DIODE	D1-D4
CAPACITOR	C1-C6, C13-C91, C93, C94, C98
SWITCH	A64
INTEGRATED CIRCUIT	A1-A24, A26-A36, A38-A55, A67-A82,
	AA000-AD558, A65-A81
DIP RESISTOR MODULE	RM1 THRU RM16
COMPONENT	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED

SCALE: 2/1

TOLERANCE: .XX ±.13 X ±.8 .X ±.5 ANGLES ±1°

DIMENSIONS ARE IN MILLIMETERS

NAME		TITLE	DATE
G. SHINU	G. SHINU	DES/DFT	1-2-80
W. LIMPERT/R. CERO		SUPV	10-16-81
W. LIMPERT		CHK	10-16-81
P. CERUA		ENG	10-16-81
D. FRANKENBERGER		MGR	10-16-81
R. BARKER		QC	10-16-81

PERKIN-ELMER

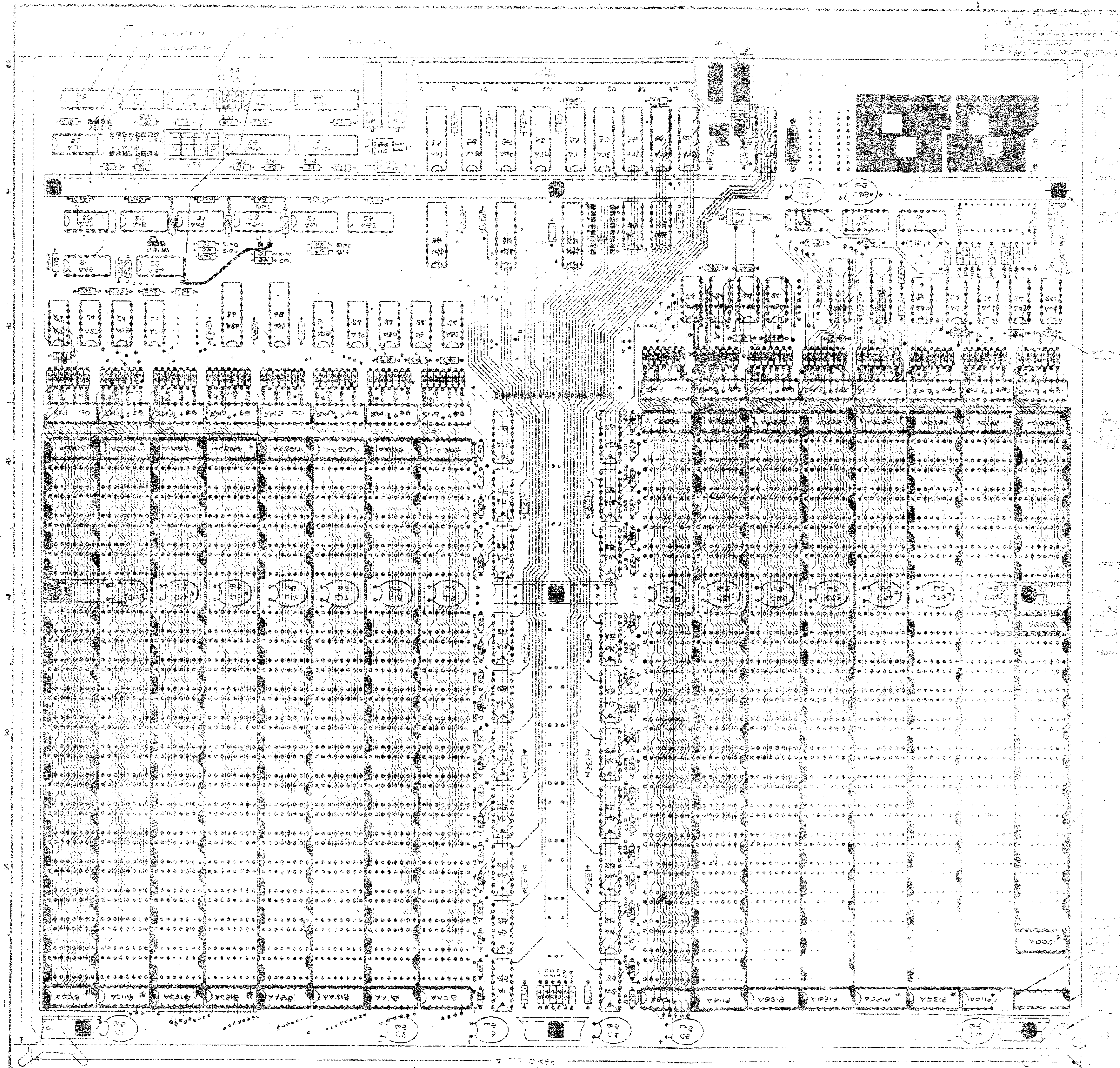
Computer Systems Division
Oceanport, N.J. 07757

TITLE **ASSEMBLY PRINTED CIRCUIT BOARD 2.0MB STORAGE MODULE**

TASK 03979

DWG 35-764 R01 E03

SMT 1-1



DWG. NO.	SHT
TITLE	STORAGE MODULE PRINTED CIRCUIT BOARD ASSEMBLY

Computer Systems Division
Oceanport N.J. 07757

PERKIN-ELMER

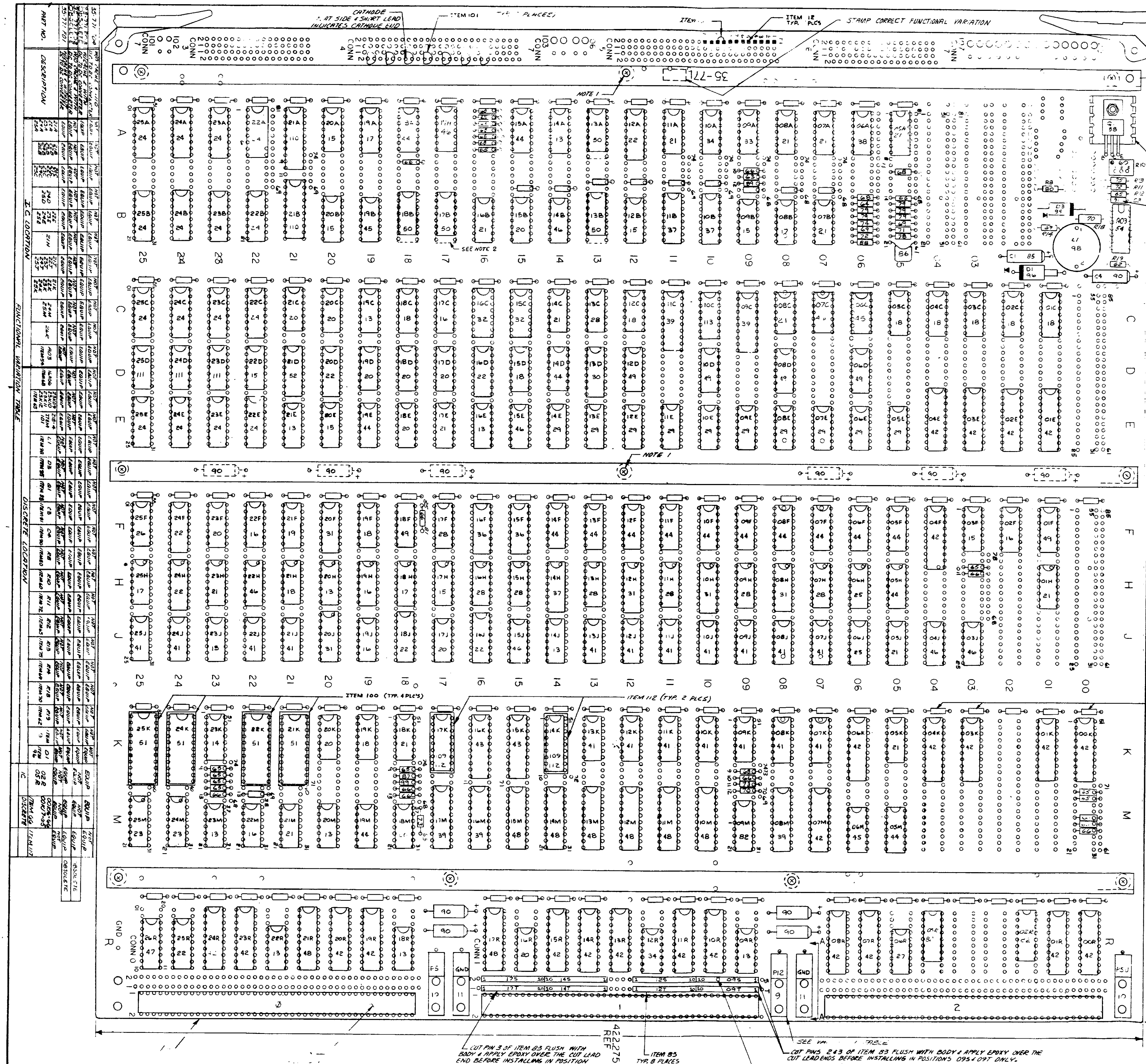
	OC	10-19-81
	MGH	10-19-81
	EMG	10-19-81
	CHK	10-19-81
	SUPV	10-19-81
	DES/DFT	
NAME	TITLE	DATE

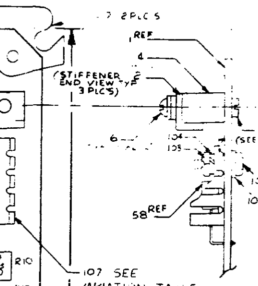
DIMENSIONS ARE IN	ANGLES
SCALE 2/1	TOLERANCE
UNLESS OTHERWISE SPECIFIED	

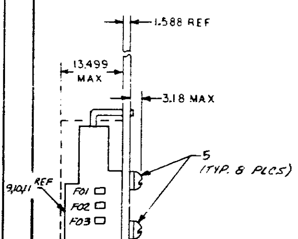
COMPONENT	REF DESIGNATION
INTEGRATED CIRCUIT	
SWITCH	
CAPACITOR	
DIODE	
TRANSISTOR	
RESISTOR	

MFG ENG	DATE
RELEASED FOR PRODUCTION	
PRE PRODUCTION APPROVAL	PROD DEV
	INIT DATE

REVISIONS







PARTIAL VIEW A-A

REVISIONS

RELEASED FOR PRODUCTION

REMOVED 21D FROM FUNCTIONAL VARIATION TABLE — 4597 MS 2-5-81 R02

IC 18M WAS ITEM 25 (19-082) RESISTOR 18K AT PIN 63 WAS LABELED 33; THIS RESISTOR WAS ITEM 65. MADE F02 & F03 VERSION OBSOLETE — 4891 MS 11-9-81 R06

IC LOCATIONS 13A, 13B, 17B & 18B WERE 19 249 FXX. NOTE 3 WAS NOTE 2. ADDED NEW NOTE 2. — 4900 11-24-81 R07

NOTES:

1. ITEM 3 (PHN SCREW) TO BE MOUNTED INTO CENTER STANDOFFS OF FRONT & MIDDLE STIFFENERS ON SOLDER SIDE ONLY.
2. IC LOCATIONS (4 PLACES) 13A, 13B, 17B & 18B DASHED LINES REPRESENT ALTERNATE USE OF 19 249FXX.
3. I.C PACK LOCATION ARE GIVEN IN THIS LIST AS ROW A,C,F,K, OR R ONLY. TO FIND ACTUAL LOCATION ON ASS'Y DWG 35-771 F03 SCHEMATIC, USE THE FOLLOWING EXAMPLES;

RUN LIST LOCATION		SCHEMATIC & ASS'Y LOCATION
00F13	=	00H04
AL50		
03K32	=	03M10

(00H04: COLUMN, ROW, PIN NUMBER)

MILLIMETERS	INCHES
1.588	.060
3.18	.125
13.499	.530
390.922	15.390
422.275	16.630

METRIC

USED IN MANUAL 47-011

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J 07757

NAME	TITLE	DATE
V. PEER	DES DFT	11-14-80
R CERO	SUPV	11-14-80
[illegible]	CHK	11-19-80
S. AGGARWAL	ENG	11-19-80
D FRAUENBERGER	MGR	11-14-80
R.A BARKER	QC	11-14-80

ASSEMBLY
LOCAL BANK
CONTROLLER

TASK 33276
DWG 35-771 R07 F03
SHT 1-1

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS		
LTR	DESCRIPTION	DATE
	AT LOC DIM TEM 5 WAS NOT TYP. IN MFG SPEC. AT LOC 12H&J ITEM 69 WAS SHOWN AT 90° FROM ITS TRUE POS. AN IDENTIFYING TABLE FOR PCB IDENTIFICATION WAS DELETED FROM MFG EQUIPPED COLUMN.	
P1	1.4743	8-20-84 RPW
	RELEASED FOR PRODUCTION	

PART NO.	DESCRIPTION
35-806-102	4400 CACHE
35-806-101	4417 CACHE

I.C. LOCATION FUNCTIONAL VARIATION TABLE

I.C. LOCATION	4400 CACHE	4417 CACHE
2114	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2124	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2134	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2144	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2154	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2164	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2174	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2184	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2194	16KX4 150ns EQUIV	16KX4 150ns EQUIV
21H	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2254	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2264	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2274	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2284	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2294	16KX4 150ns EQUIV	16KX4 150ns EQUIV
22H	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2344	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2354	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2364	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2374	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2384	16KX4 150ns EQUIV	16KX4 150ns EQUIV
2394	16KX4 150ns EQUIV	16KX4 150ns EQUIV
23H	4KX4 200ns EQUIV	4KX4 200ns EQUIV
24H	4KX4 200ns EQUIV	4KX4 200ns EQUIV
25H	4KX4 200ns EQUIV	4KX4 200ns EQUIV
26H	4KX4 200ns EQUIV	4KX4 200ns EQUIV
27H	4KX4 200ns EQUIV	4KX4 200ns EQUIV
28H	4KX4 200ns EQUIV	4KX4 200ns EQUIV
29H	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2AH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2BH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2CH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2DH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2EH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2FH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2GH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2HH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2JH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2KH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2LH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2MH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2NH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2PH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2RH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2SH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2TH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2UH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2VH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2WH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2XH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2YH	4KX4 200ns EQUIV	4KX4 200ns EQUIV
2ZH	4KX4 200ns EQUIV	4KX4 200ns EQUIV

DISC LOCATION

DISC LOCATION	4400 CACHE	4417 CACHE
1751	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1752	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1753	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1754	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1755	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1756	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1757	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1758	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1759	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1760	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1761	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1762	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1763	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1764	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1765	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1766	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1767	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1768	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1769	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1770	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1771	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1772	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1773	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1774	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1775	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1776	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV
1777	1MB 4 MEGA DISC EQUIV	1MB 4 MEGA DISC EQUIV

CATHODE - FLAT SIDE & SHORT LEAD INDICATES CATHODE END

ITEM 101 (TYP 7 PLACES)

ITEM 11 (2 PLCS)

ITEM 1 TYP ALL PCBS

STAMP CORRECT FUNCTIONAL VARIATION

35-806-

NOTE 1

SEE NOTE 3.

ITEM 18 (TYP. 4 PLCS)

ITEM 17 (TYP. 4 PLCS)

ITEM 93 (ALL UNSPECIFIED) TYP 134

CUT PIN 3 OF ITEM 83 FLUSH WITH BODY & APPLY EPOXY OVER THE CUT LEAD END BEFORE INSTALLING IN POSITION 111 ONLY.

ITEM 85 TYP. 8 PLACES

CUT PINS 2 & 3 OF ITEM 83 FLUSH WITH BODY & APPLY EPOXY OVER THE CUT LEAD ENDS BEFORE INSTALLING IN POSITIONS 095 & 097 ONLY.

CUT PIN 7 OF ITEM 83 (095 ONLY) FLUSH WITH B DY ANE APPLY EPOXY OVER THE CUT LEAD BEFORE INSTALLING IN P SITION 095.

422.275 REF

390.922 REF

(STIFFENER END VIEW TYP 3 PLCS)

6 TYP 4 PLCS

4 (SEE NOTE)

NOTES:
1. ITEM 4 (PHN SCREW) TO BE MOUNTED INTO CENTER STANDOFFS OF FRONT & MIDDLE STIFFENERS ON SOLDER SIDE ONLY.

- I.C. PACK LOCATION ARE GIVEN IN THIS LIST AS ROW A, C, E, H, OR R ONLY. TO FIND ACTUAL LOCATION ON ASS'Y DWG 35-806 (03) SCHEMATIC, USE THE FOLLOWING EXAMPLES;

RUN LIST LOCATION		ASSY LOCATION
00F13	=	00H04 (PIN NUMBER, ROW, COLUMN)
ALSO		
03K32	=	03M10

2. I.C. (TYP 4 PLCS) 2A, 3B, 12B & 8H DASHED LINE REPRESENTS ALTERNATE USE OF P/N 1.249 FCI.

1.588 REF
13.499 MAX
3.18 MAX
14.15 REF
P01 P02 P03
8 (TYP. 6 PLCS)

PARTIAL VIEW A-A

MILLIMETERS	INCHES
1.588	.060
3.18	.125
13.499	.530
390.922	15.390
422.275	16.630

DIMENSIONS IN MILLIMETERS
X ± .8
XX ± .25
UNLESS OTHERWISE SPECIFIED

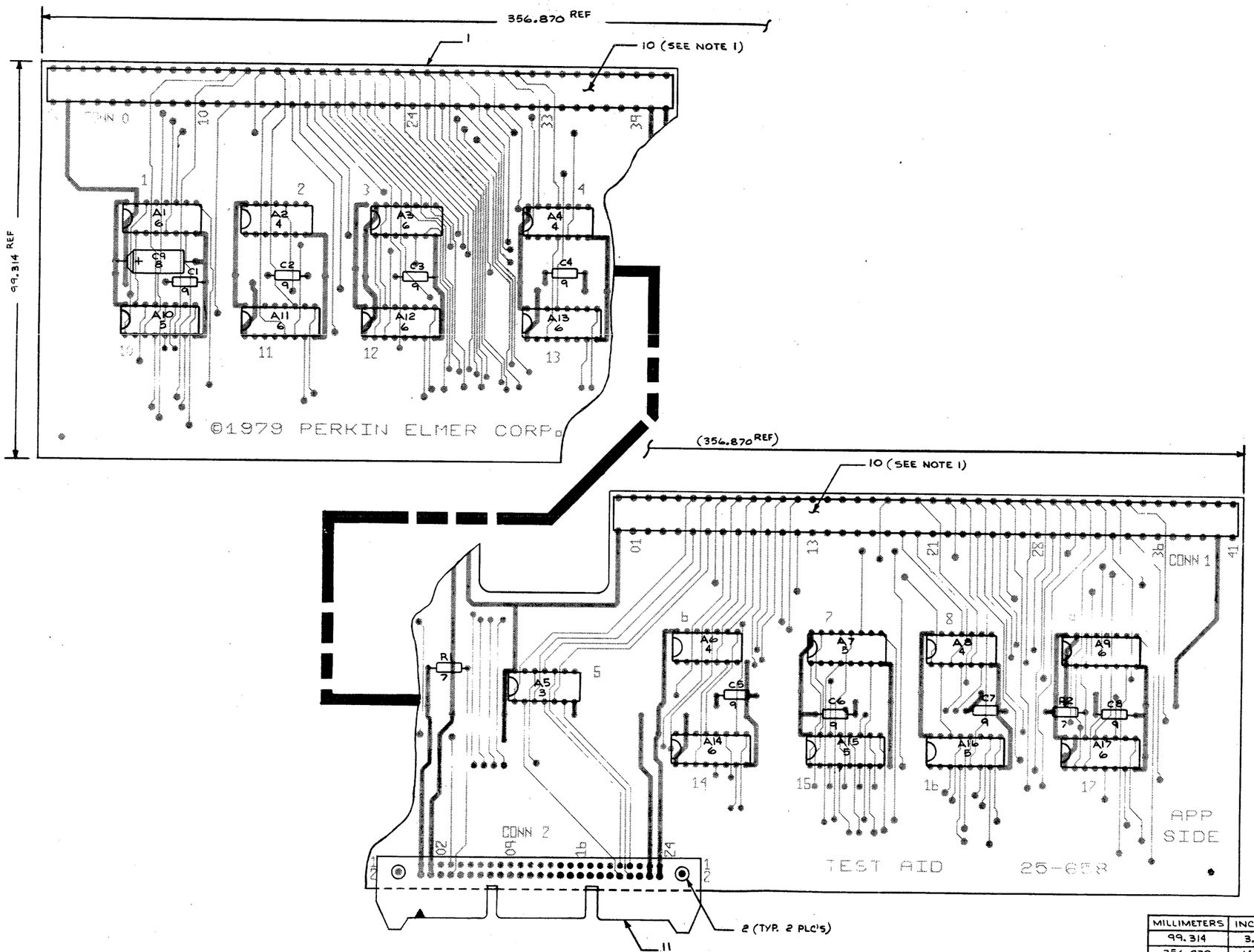
METRIC

USED IN MANUAL 47-022

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

NAME	TITLE	DATE
QSTINE QSTINE	DES	1-29-81
R CERO	SUPV	2-11-81
	CHK	
M MANIGIONE	ENG	3-11-81
R GARCIA	MGR	3-11-81
N. BLAZEVICH	QC	3-11-81

ASSEMBLY
LOCAL CHANNEL CONTROLLER (LCMB)
TASK 03183 SHT 1
DWG 35-806-03E03 REV —



MILLIMETERS	INCHES
99.314	3.91
356.870	14.05

NOTES 1. CONNECTOR PINS CLOSET TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

BRUNING 44-131 40579

REVISIONS

RELEASED FOR PRODUCTION
MFG. ENG. D Osso DATE 6/24/80

METRIC

USED ON MANUAL 29-695

UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

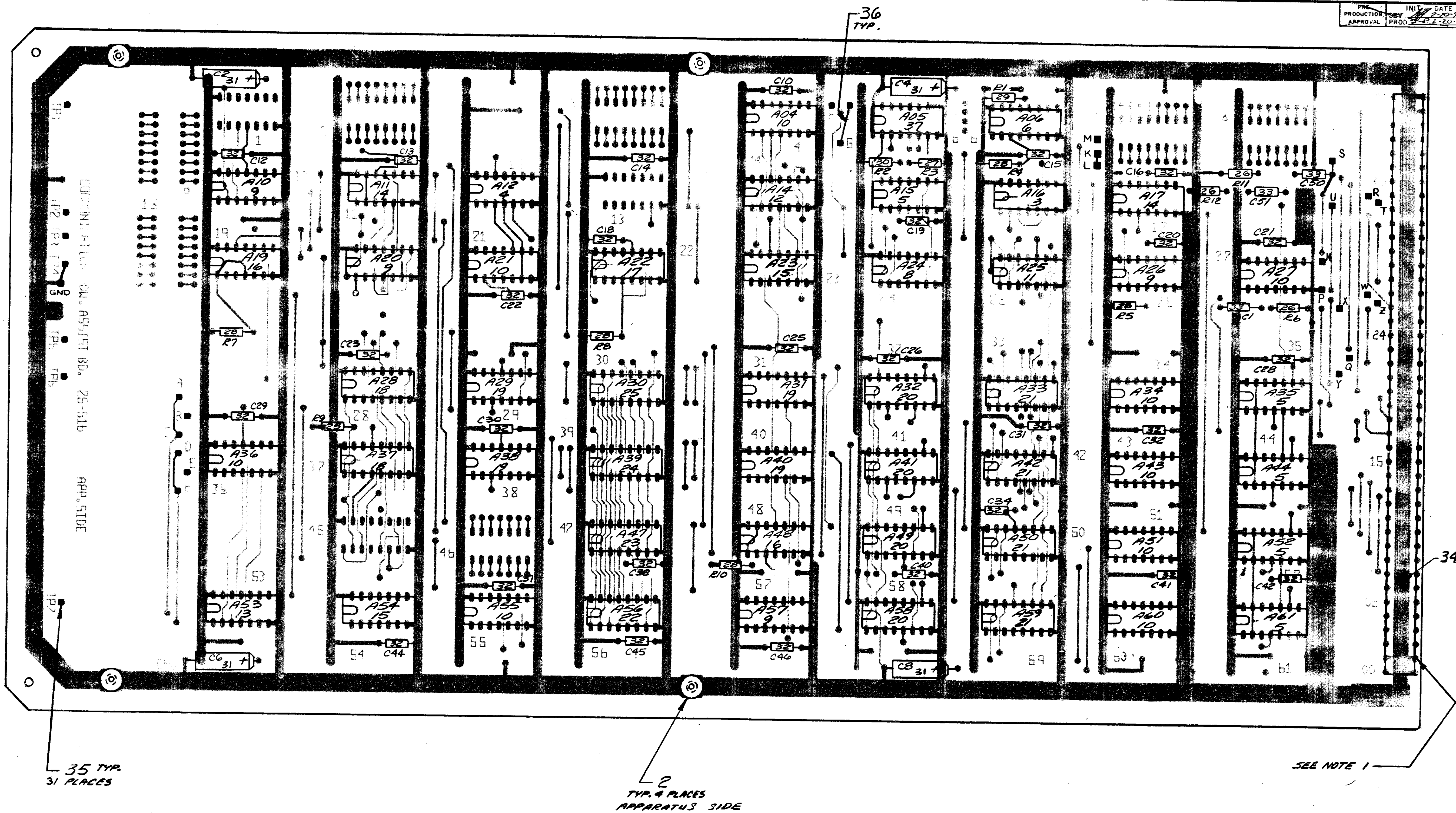
NAME		TITLE	DATE
J. BIELSKIE	DESTINE	DES/DFT	12-19-79
R. CERO		SUPV	5-13-80
R. CERO		CHK	5-13-80
E. MARCH		ENG	5-13-80
D. FRANKENBERGER		MGR	5-13-80
R. BARKER		QC	5-8-80

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE ASSEMBLY
TEST AID

TASK 03976 SHT 1 - 1
DWG 35-734 M01 D03



PRE PRODUCTION APPROVAL	INIT.	DATE
DEV		2-20-76
PROD		2-20-76

VARIATION TABLE

	RESISTORS		CAP.		STRAPS									
	R12	R11	C50	C51	G-J	G-H	N-P	P-Q	R-S	S-U	T-U	U-W	X-Y	X-Z
35-622 F00	YES	YES	YES	YES	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO
35-622 F01	NO	NO	NO	NO	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES

NOTES:
1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO WAVE SOLDERING.

REVISED PER R05 COPPER — JLV 4683 MS 5-27-81 R06

EXTENSIVE CHANGE MADE FOR R04 SEE PREVIOUS MIRCO FILM COPY. ADDED VARIATIONS & TABLE — KR 3938 M 9-13-79 R05

A48 WAS SPEC'D AS ITEM 2. — 2923 — 9-3-76 R03

REVISED PER R03 COPPER — 3883 M 3-19-79 R04

ADDED STAKES K, L, & M. REVISED PER R02 COPPER — 03073-4 EP 4-20-76 R02

RELEASED FOR PRODUCTION — MFG. ENG. E Porgio DATE 4-28-76

REVISIONS
REVISED PER R01 COPPER. ADDED R11, R12, C50 & C51. DELETED C3, C5, C7, C9, C11, C17, C24, C27, C33, C35, C36, C39, C43, C47, C48, C49. REVERSED C15 & C26. ADDED W/W STAKE. FOR ... REV. 3&E R00 — 5-5-76 R01

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Oceanport, N.J. 07757

CAPACITORS	C34, -C38, C40-C42, C44-46, C50, C51
CAPACITORS	C1, C2, C4, C6, C8, C10, C12-16, C18-C23 C25, C26, C28-C32
RESISTORS	R1-R12
I.C.'s	A04-A06, A10-A12, A14-A17, A19-A44, A47-A61

NAME	TITLE	DATE	
V. PERRI	DRAFT	2-5-76	ASSEMBLY COMMUNICATION HDW. ASSIST BOARD
E. CERO	CHECK	2-5-76	
G. JOYCE	ENGR	4-28-76	
R.A. BARKER	Q.C.	4-28-76	03073
S. MESSINA	MGR.	4-28-76	35-622R06 D03 — SHT 1 OF 1

PERKIN ELMER
Computer Systems Division
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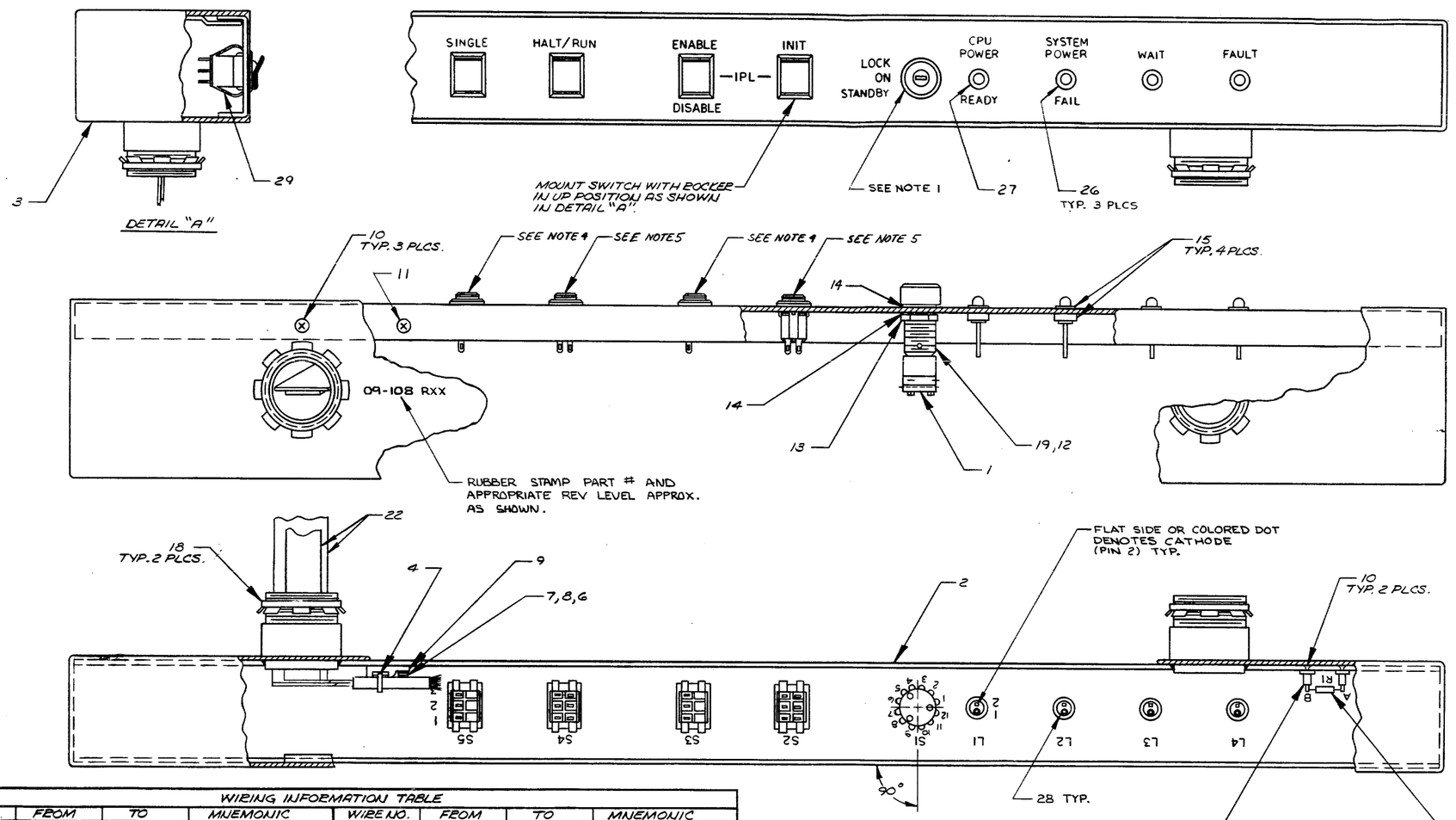
REVISIONS			
PRE PRODUCTION APPROVAL	INIT	DATE	
	DEV	2-24-78	
	PROD	4-11-78	
WIRE #2 WAS: 202-2/ L3-2/CSNVMO. WIRE #15 WAS: 200-3 THRU 207-3.	LW	38603	6 DEC 78 R01
EXTENSIVE CHANGES FOR PREVIOUS REV LEVEL SEE R01 D03 MICROFILM COPY			
	KR	3997	4-6-79 R02
RELEASED FOR PRODUCTION MFG ENG		DATE	8/10/79
AREA H3 ADDED SEC LOCK WASHER (ITEM 14) TO ITEM 1			
	KR	LI-9002-03 R	9-12-79 R03
AREA C2 29 WAS 24 REF. AREA F&H3, F&H6 REFLECTED S2&S4 TO SHOW 6 TERMINALS NOT 3. ADDED NOTES 4&5. AREA E3 THRU H3 SEE NOTE 4 (2 PLCS) & SEE NOTE 5 (2 PLCS) WERE 23&24.			
	KR	4656 R	5-7-81 R04



WIRING INFORMATION TABLE

WIRE NO.	FROM	TO	MNEMONIC	WIRE NO.	FROM	TO	MNEMONIC
1	100-2	S1-5W	C1	19	P1-B	L4-1	
2	102-2	S1-7	C4	20	L4-1	L3-1	
3	104-2	L1-1	CP12	21			
4	205-2	L1-2	CPEDYØ	22	S4-2	S2-2	
5	201-2	L2-2	CSPFLDØ	23	S2-2	S1-2	
6	108-3	S1-1	POFFO	24	S5-2	S4-2	
7	100-3	S3-1	LSU				
8	101-3	S4-3	ESNCO				
9	102-3	S4-1	ESNOO				
10	103-3	S2-3	PFDTO				
11	104-3	S5-3	SUGL				
12	105-3	P1-A	P5				
13	106-3	L4-2	FAULT				
14	107-3	L3-2	WAIT				
15	200-3	S1-1W	GND				
16	201-3	S3-2	GND				
17	L1-1	L2-1					
18	S1-6	S1-7					

NOTES:
1. TURN SWITCH (S1) TO CENTER POSITION & ORIENT AS SHOWN.
2. WIRES 1 THRU 16 ARE PART OF 17-471 ITEM 22.
3. WIRES 17 THRU 24 ARE #24 GA. WHT. ITEM 21.
4. 3 TERMINAL SWITCH FROM ITEM 29.
5. 6 TERMINAL SWITCH FROM ITEM 29.

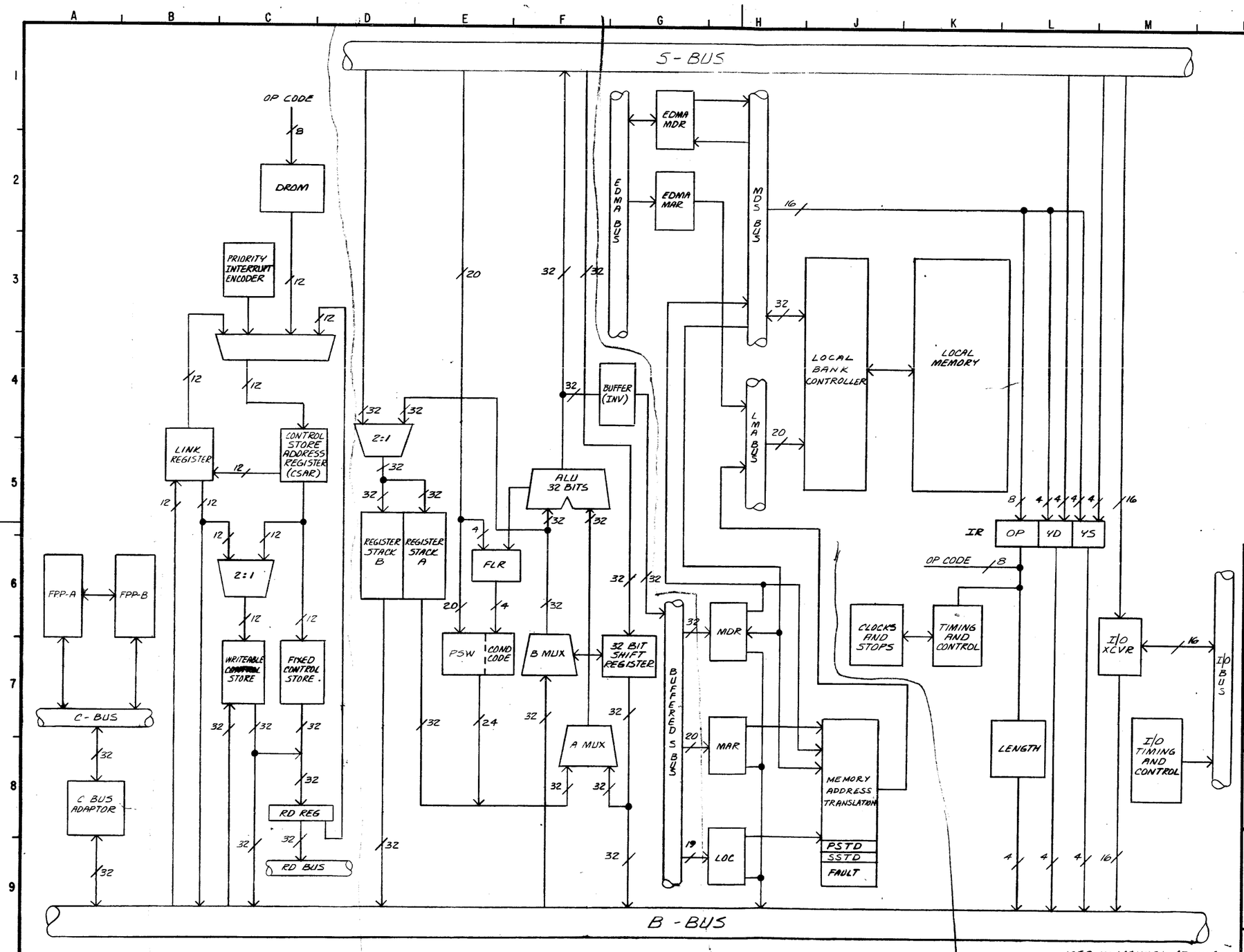
SCALE – 1 : 1	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	P. CARD	DRAFT	8-1-78
	E. CERO	CHK	8.28.79
	G. WELLY	ENGR	8.28.79
	E. BARKER	Q.C.	8.28.79
	P. ABITANTE	MGR.	8.28.79

TITLE ASSEMBLY SYSTEM CONTROL

PART NO. 03916

DWG NO. 09-108R04D03

SHEET OF 1 — 1



USED IN MANUAL 47-004

REVISIONS	01		01	
SHEETS	1	2	3	4

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

BRUNING 44-131 40579

REVISIONS

RELEASED FOR PRODUCTION
ENG. [illegible] DATE 10/1/21

REVISED SHTS 1&3.

KR	91	4916	M	12-21-81	201

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
B. GRAY	DES / DFT	10-8-81
R. CERO	SUPV	10-8-81
E. GRLENSTEIN	SYS TEST	10-8-81
S. BASTIAN	ENG	10-8-81
P. ORBDA	MGR	10-8-81
R. BARKER	QC	10-8-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
BACKPANEL

TASK 03976 | SHT 1-4
DWG 01-142 M01R01 D08

REVISIONS

SEE NOTE 1

J1

ROW 2	PIN NO	ROW 1
GND	00	GND
PRDY1	01	NVMØ
2XLFI	02	SCLRSI
SCLRØ	03	SCLRØ
NVRSØ	04	PTSDI
P5	05	* KEY
	06	

J3

ROW 1	PIN NO	ROW 2
LSUI	00	GND
SCATNØ	01	GND
RCATNØ	02	GND
PFDTØ	03	GND
SINGLØ	04	GND
P5	05	GND
FAULTØ	06	GND
WAITØ	07	GND
PØFFØ	08	GND
	09	GND
	10	* KEY
	11	GND
	12	GND

CONN	STM 15		STM 16		TITLE BOARD ACC TERM NO
	ROW 2	ROW 1	ROW 2	ROW 1	
1	GND	GND	GND	GND	00
	MWE0	MRE0	MWE0	MRE0	01
	MRDS0	MCI0	MRDS0	MCI0	02
	MREF0	MCC0	MREF0	MCC0	03
	MWA011	MWA001	MWA011	MWA001	04
	MEA010	MEA000	MEA010	MEA000	05
	MEA030	MEA020	MEA030	MEA020	06
		LMB001		LMB001	07
	LMB011	LMB021	LMB011	LMB021	08
	GND	GND	GND	GND	09
	GND	GND	GND	GND	10
	LMB031	LMB041	LMB031	LMB041	11
	LMB051	LMB061	LMB051	LMB061	12
	LMB071	LMB081	LMB071	LMB081	13
	LMB091	LMB101	LMB091	LMB101	14
	LMB111	LMB121	LMB111	LMB121	15
	LMB131	LMB141	LMB131	LMB141	16
	LMB151	LMB161	LMB151	LMB161	17
	LMB171	LMB181	LMB171	LMB181	18
	GND	GND	GND	GND	19
					20
					21
					22
					23
	GND	GND	GND	GND	24
	LMB191	LMB201	LMB191	LMB201	25
	LMB211	LMB221	LMB211	LMB221	26
	LMB231	LMB241	LMB231	LMB241	27
	LMB251	LMB261	LMB251	LMB261	28
	LMB271	LMB281	LMB271	LMB281	29
	LMB291	LMB301	LMB291	LMB301	30
	LMB311	LMB321	LMB311	LMB321	31
	LMB331	LMB341	LMB331	LMB341	32
	GND	GND	GND	GND	33
	GND	GND	GND	GND	34
	LMB351	LMB361	LMB351	LMB361	35
	LMB371	LMB381	LMB371	LMB381	36
	MX030	MX010	MX030	MX010	37
	MX020		MX020		38
					39
					40
	RCLC0	PFSD0	RCLC0	PFSD0	41
	BSCLR0	PTSD1	BSCLR0	PTSD1	42
	GND	GND	GND	GND	43

CONN	STM 12		STM 13		TITLE BOARD ACC TERM NO
	ROW 2	ROW 1	ROW 2	ROW 1	
1	GND	GND	GND	GND	00
	MWE0	MRE0	MWE0	MRE0	01
	MRDS0	MCI0	MRDS0	MCI0	02
	MREF0	MCC0	MREF0	MCC0	03
	MWA011	MWA001	MWA011	MWA001	04
	MEA010	MEA000	MEA010	MEA000	05
	MEA030	MEA020	MEA030	MEA020	06
		LMB001		LMB001	07
	LMB011	LMB021	LMB011	LMB021	08
	GND	GND	GND	GND	09
	GND	GND	GND	GND	10
	LMB031	LMB041	LMB031	LMB041	11
	LMB051	LMB061	LMB051	LMB061	12
	LMB071	LMB081	LMB071	LMB081	13
	LMB091	LMB101	LMB091	LMB101	14
	LMB111	LMB121	LMB111	LMB121	15
	LMB131	LMB141	LMB131	LMB141	16
	LMB151	LMB161	LMB151	LMB161	17
	LMB171	LMB181	LMB171	LMB181	18
	GND	GND	GND	GND	19
					20
					21
					22
					23
	GND	GND	GND	GND	24
	LMB191	LMB201	LMB191	LMB201	25
	LMB211	LMB221	LMB211	LMB221	26
	LMB231	LMB241	LMB231	LMB241	27
	LMB251	LMB261	LMB251	LMB261	28
	LMB271	LMB281	LMB271	LMB281	29
	LMB291	LMB301	LMB291	LMB301	30
	LMB311	LMB321	LMB311	LMB321	31
	LMB331	LMB341	LMB331	LMB341	32
	GND	GND	GND	GND	33
	GND	GND	GND	GND	34
	LMB351	LMB361	LMB351	LMB361	35
	LMB371	LMB381	LMB371	LMB381	36
	MX030	MX010	MX030	MX010	37
	MX020		MX020		38
					39
					40
	RCLC0	PFSD0	RCLC0	PFSD0	41
	BSCLR0	PTSD1	BSCLR0	PTSD1	42
	GND	GND	GND	GND	43

NOTES 1. * INDICATES KEY LOCATION IN J1 & J3

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
BACKPANEL

TASK 03976 | SHT 2 - 4
DWG 01-142 M01 D08

REVISIONS					
ADDED MNEMONICS AT 17AX26, 17AX08, 19KV; 12A22.					
A2	JW	4416	M	12.21.81	R01

O	CONN	TITLE	BOARD LOC	TERM NO
LBC 08 ROW2 GND	00			
LMA090	01			
LMA110	02			
LMA130	03			
LMA150	04			
LMA170	05			
LMA190	06			
LMA210	07			
LMA230	08			
GND	09			
GND	10			
LMA250	11			
LMA270	12			
LMA290	13			
LMA310	14			
WRT0	15			
LER0	16			
LMBSY0	17			
PSELI	18			
FNCE0	19			
GND	20			
SCLK1	21			
CLK1C	22			
CLK1B	23			
GND	24			
GND	25			
B331	26			
B271	27			
B241	28			
B231	29			
B221	30			
B211	31			
B181	32			
B171	33			
GND	34			
GND	35			
B151	36			
B141	37			
B131	38			
B121	39			
B081	40			
B071	41			
B061	42			
B021	43			

O	CONN	TITLE	BOARD LOC	TERM NO
CPU-C 06 ROW2 GND	00			
MAT0	01			
DEXB0	02			
DEXT0	03			
	04			
	05			
	06			
SCLR0	07			
GND	08			
GND	09			
GND	10			
	11			
DSTOP0	12			
MSTOP0	13			
	14			
PSW11	15			
PSW21	16			
	17			
RD020	18			
GND	19			
GND	20			
RD031	21			
RD011	22			
GND	23			
GND	24			
RD150	25			
RD141	26			
RD121	27			
RD240	28			
RD251	29			
	30			
	31			
GND	32			
GND	33			
	34			
	35			
	36			
	37			
	38			
	39			
	40			
	41			
GND	42			
GND	43			

O	CONN	TITLE	BOARD LOC	TERM NO
CPU-D 07 ROW2 GND	00			
MA090	01			
MA110	02			
MA130	03			
MA150	04			
MA170	05			
MA190	06			
MA210	07			
MA230	08			
GND	09			
GND	10			
MA250	11			
MA270	12			
MA290	13			
MA310	14			
WRT0	15			
LER0	16			
MBSY0	17			
PSELI	18			
FNCE0	19			
GND	20			
SCLK1	21			
CLK1A	22			
CLK1B	23			
GND	24			
GND	25			
B301	26			
B291	27			
B281	28			
B271	29			
B261	30			
B251	31			
B241	32			
B231	33			
B221	34			
B211	35			
B201	36			
B191	37			
B181	38			
B171	39			
B161	40			
B151	41			
B141	42			
B131	43			

O	CONN	TITLE	BOARD LOC	TERM NO
CPU-C 06 ROW2 GND	00			
MAT0	01			
DEXB0	02			
DEXT0	03			
	04			
	05			
	06			
SCLR0	07			
GND	08			
GND	09			
GND	10			
	11			
DSTOP0	12			
MSTOP0	13			
	14			
PSW11	15			
PSW21	16			
	17			
RD020	18			
GND	19			
GND	20			
RD031	21			
RD011	22			
GND	23			
GND	24			
RD150	25			
RD141	26			
RD121	27			
RD240	28			
RD251	29			
	30			
	31			
GND	32			
GND	33			
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	35			
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	39			
	40			
	41			
GND	42			
GND	43			

O	CONN	TITLE	BOARD LOC	TERM NO
CPU-D 07 ROW2 GND	00			
ADRS0	01			
CMD0	02			
DA0	03			
TACK020	04			
TACK030	05			
BCNT0	06			
CLFLR0	07			
TRAP0	08			
	09			
	10			
RSTOP0	11			
OPSTOP0	12			
PSW171	13			
PSW271	14			
PSW161	15			
PSW261	16			
RD251	17			
RD231	18			
RD061	19			
RD071	20			
RD150	21			
RD131	22			
RD240	23			
RD261	24			
RD271	25			
GDIR0	26			
DISB0	27			
DISA0	28			
SMBSY0	29			
SERR0	30			
LMRQ0	31			
IPPRT0	32			
	33			
	34			
IR010	35			
IR030	36			
IR050	37			
IR070	38			
IR090	39			
YD071	40			
YS11	41			
YS31	42			
YS51	43			

O	CONN	TITLE	BOARD LOC	TERM NO
CPU-C 06 ROW2 GND	00			
ALGN0	01			
EXB0	02			
	03			
	04			
	05			
	06			
	07			
GND	08			
GND	09			
GND	10			
	11			
	12			
	13			
	14			
PSW10	15			
	16			
	17			
	18			
GND	19			
GND	20			
	21			
	22			
GND	23			
GND	24			
	25			
	26			
	27			
	28			
	29			
	30			
	31			
GND	32			
GND	33			
	34			
	35			
	36			
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	38			
	39			
	40			
	41			
GND	42			
GND	43			

O	CONN	TITLE	BOARD LOC	TERM NO
CPU-D 07 ROW2 GND	00			
ADRS0	01			
CMD0	02			
DA0	03			
TACK010	04			
TACK020	05			
BCNT0	06			
CLFLR0	07			
TRAP0	08			
	09			
	10			
RSTOP0	11			
OPSTOP0	12			
PSW171	13			
PSW271	14			
PSW161	15			
PSW261	16			
RD251	17			
RD231	18			
RD061	19			
RD071	20			
RD150	21			
RD131	22			
RD240	23			
RD261	24			
RD271	25			
GDIR0	26			
DISB0	27			
DISA0	28			
SMBSY0	29			
SERR0	30			
LMRQ0	31			
IPPRT0	32			
	33			
	34			
IR010	35			
IR030	36			
IR050	37			
IR070	38			
IR090	39			
YD071	40			
YS11	41			
YS31	42			
YS51	43			

1	CONN	TITLE	BOARD LOC	TERM NO
LBC 08 ROW2 GND	00			
MA090	01			
MA110	02			
MA130	03			
MA150	04			
MA170	05			
MA190	06			
MA210	07			
MA230	08			
GND	09			
GND	10			
MA250	11			
MA270	12			
MA290	13			
MA310	14			
WRT0	15			
LER0	16			
MBSY0	17			
PSELI	18			
FNCE0	19			
GND	20			
SCLK1	21			
CLK1A	22			
CLK1B	23			
GND	24			
GND	25			
B301	26			
B291	27			
B281	28			
B271	29			
B261	30			
B251	31			
B241	32			
B231	33			
B221	34			
B211	35			
B201	36			
B191	37			
B181	38			
B171	39			
B161	40			
B151	41			
B141	42			
B131	43			

1	CONN	TITLE	BOARD LOC	TERM NO
LBC 08 ROW2 GND	00			
MDS010	01			
MDS030	02			
MDS050	03			
MDS070	04			
MDS090	05			
MDS110	06			
MDS130	07			
MDS150	08			
GND	09			
GND	10			
MDS170	11			
MDS190	12			
MDS210	13			
MDS230	14			
MDS250	15			
MDS270	16			
MDS290	17			
MDS310	18			
GND	19			
GND	20			
MDS011	21			
MDS031	22			
MDS051	23			
MDS071	24			
MDS091	25			
MDS111	26			
MDS131	27			
MDS151	28			
MDS171	29			
MDS191	30			
MDS211	31			
MDS231	32			
MDS251	33			
MDS271	34			
MDS291	35			
MDS311	36			
MDS331	37			
GND	38			
GND	39			
RCLC0	40	PFSD0		
RSCLR0	41	PTSD1		
GND	42			
GND	43			

1	CONN	TITLE	BOARD LOC	TERM NO
CPU-C 06 ROW2 GND	00			
MDS010	01			
MDS030	02			
MDS050	03			
MDS070	04			
MDS090	05			
MDS110	06			
MDS130	07			
MDS150	08			
GND	09			
GND	10			
MDS170	11			
MDS190	12			
MDS210	13			
MDS230	14			
MDS250	15			
MDS270	16			
MDS290	17			
MDS310	18			
GND	19			
GND	20			
MDS011	21			
MDS031	22			
MDS051	23			
MDS071	24			
MDS091	25			
MDS111	26			
MDS131	27			
MDS151	28			
MDS171	29			
MDS191	30			
MDS211	31			
MDS231	32			
MDS251	33			
MDS271	34			
MDS291	35			
MDS311	36			
MDS331	37			
GND	38			
GND	39			
RCLC0	40	PFSD0		
RSCLR0	41	PTSD1		
GND	42			
GND	43			

1	CONN	TITLE	BOARD LOC	TERM NO
CPU-D 07 ROW2 GND	00			
MDS010	01			
MDS030	02			
MDS050	03			
MDS070	04			
MDS090	05			
MDS110	06			
MDS130	07			
MDS150	08			
GND	09			
GND	10			
MDS170	11			
MDS190	12			
MDS210	13			
MDS230	14			
MDS250	15			
MDS270	16			
MDS290	17			
MDS310	18			
GND	19			
GND	20			
MATRS0	21			
MATRS0	22			
GND	23			
GND	24			
	25			
	26			
	27			
	28			
	29			
	30			
	31			
GND	32			
GND	33			
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GND	42			
GND	43			

1	CONN	TITLE	BOARD LOC	TERM NO
CPU-C 06 ROW2 GND	00			
MDS010	01			
MDS030	02			
MDS050	03			
MDS070	04			
MDS090	05			
MDS110	06			
MDS130	07			
MDS150	08			
GND	09			
GND	10			
MDS170	11			
MDS190	12			
MDS210	13			
MDS230	14			
MDS250	15			
MDS270	16			
MDS290	17			
MDS310	18			
GND	19			
GND	20			
MATRS0	21			
MATRS0	22			
GND	23			
GND	24			
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	26			
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GND	32			
GND	33			
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GND	42			
GND	43			

1	CONN	TITLE	BOARD LOC	TERM NO
CPU-D 07 ROW2 GND	00			
MDS010	01			
MDS030	02			
MDS050	03			
MDS070	04			
MDS090	05			
MDS110	06			
MDS130	07			
MDS150	08			
GND	09			
GND	10			
MDS170	11			
MDS190	12			
MDS210	13			
MDS230	14			
MDS250	15			
MDS270	16			
MDS290	17			
MDS310	18			
GND	19			
GND	20			
TPC0	21	DMARS0		
FAULT0	22	MATRS0		
GND	23			
GND	24			
	25			
	26			
	27			
	28			
	29			
	30			
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GND	32			
GND	33			
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GND	42			
GND	43			

2	CONN	TITLE	BOARD LOC	TERM NO
LBC 08 ROW2 GND	00			
MDS010	01			
MDS030	02			
MDS050	03			
MDS070	04			
MDS090	05			
MDS110	06			
MDS130	07			
MDS150	08			
GND	09			
GND	10			
MDS170	11			
MDS190	12			
MDS210	13			
MDS230	14			
MDS250	15			
MDS270	16			
MDS290	17			
MDS310	18			
GND	19			
GND	20			
MDS011	21			
MDS031	22			
MDS051	23			
MDS071	24			
MDS091	25			
MDS111	26			
MDS131	27			
MDS151	28			
MDS171	29			
MDS191	30			
MDS211	31			
MDS231	32			
MDS251	33			
MDS271	34			
MDS291	35			
MDS311	36			
MDS331	37			
GND	38			
GND	39			
RCLC0	40	PFSD0		
RSCLR0	41	PTSD1		
GND	42			
GND	43			

2	CONN	TITLE	BOARD LOC	TERM NO
CPU-C 06 ROW2 GND	00			
MDS010	01			
MDS030	02			
MDS050	03			
MDS070	04			
MDS090	05			
MDS110	06			
MDS130	07			
MDS150	08			
GND	09			
GND	10			
MDS170	11			
MDS190	12			
MDS210	13			
MDS230	14			
MDS250	15			
MDS270	16			
MDS290	17			
MDS310	18			
GND	19			
GND	20			
MATRS0	21	DMARS0		
MATRS0	22			
GND	23			
GND	24			
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GND	32			
GND	33			
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GND	42			
GND	43			

2	CONN	TITLE	BOARD LOC	TERM NO
CPU-D 07 ROW2 GND	00			
MDS010	01			
MDS030	02			
MDS050	03			
MDS070	04			
MDS090	05			
MDS110	06			
MDS130	07			
MDS150	08			
GND	09			
GND	10			
MDS170	11			
MDS190	12			
MDS210	13			
MDS230	14			
MDS250	15			
MDS270	16			
MDS290	17			
MDS310	18			
GND	19			
GND	20			
DMARS0	21			
GND	22			
GND	23			
GND	24			
	25			
	26			
	27			
	28			
	29			
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GND	32			
GND	33			
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	40			
	41			
GND	42			
GND	43			

2	CONN	TITLE	BOARD LOC	TERM NO
CPU-C 06 ROW2 GND	00			
MDS010	01			
MDS030	02			
MDS050	03			
MDS070	04			
MDS090	05			
MDS110	06			
MDS130	07			
MDS150	08			
GND	09			
GND	10			
MDS170	11			
MDS190	12			
MDS210	13			
MDS230	14			
MDS250	15			
MDS270	16			
MDS290	17			
MDS310	18			
GND	19			
GND	20			
MATRS0	21	DMARS0		
MATRS0	22			
GND	23			
GND	24			
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GND	32			
GND	33			
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	41			
GND	42			
GND	43			

2	CONN	TITLE	BOARD LOC	TERM NO
CPU-D 07 ROW2 GND	00			
MDS010	01			
MDS030	02			
MDS050	03			
MDS070	04			
MDS090	05			
MDS110	06			
MDS130	07			
MDS150	08			
GND	09			
GND	10			
MDS170	11			
MDS190	12			
MDS210	13			
MDS230	14			
MDS250	15			
MDS270	16			
MDS290	17			
MDS310	18			
GND	19			
GND	20			
TPC0	21	DMARS0		
FAULT0	22	MATRS0		
GND	23			
GND	24			
	25			
	26			
	27			
	28			
	29			
	30			
	31			
GND	32			
GND	33			
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GND	42			
GND	43			

NOTES

BRUNING 44-131 40579

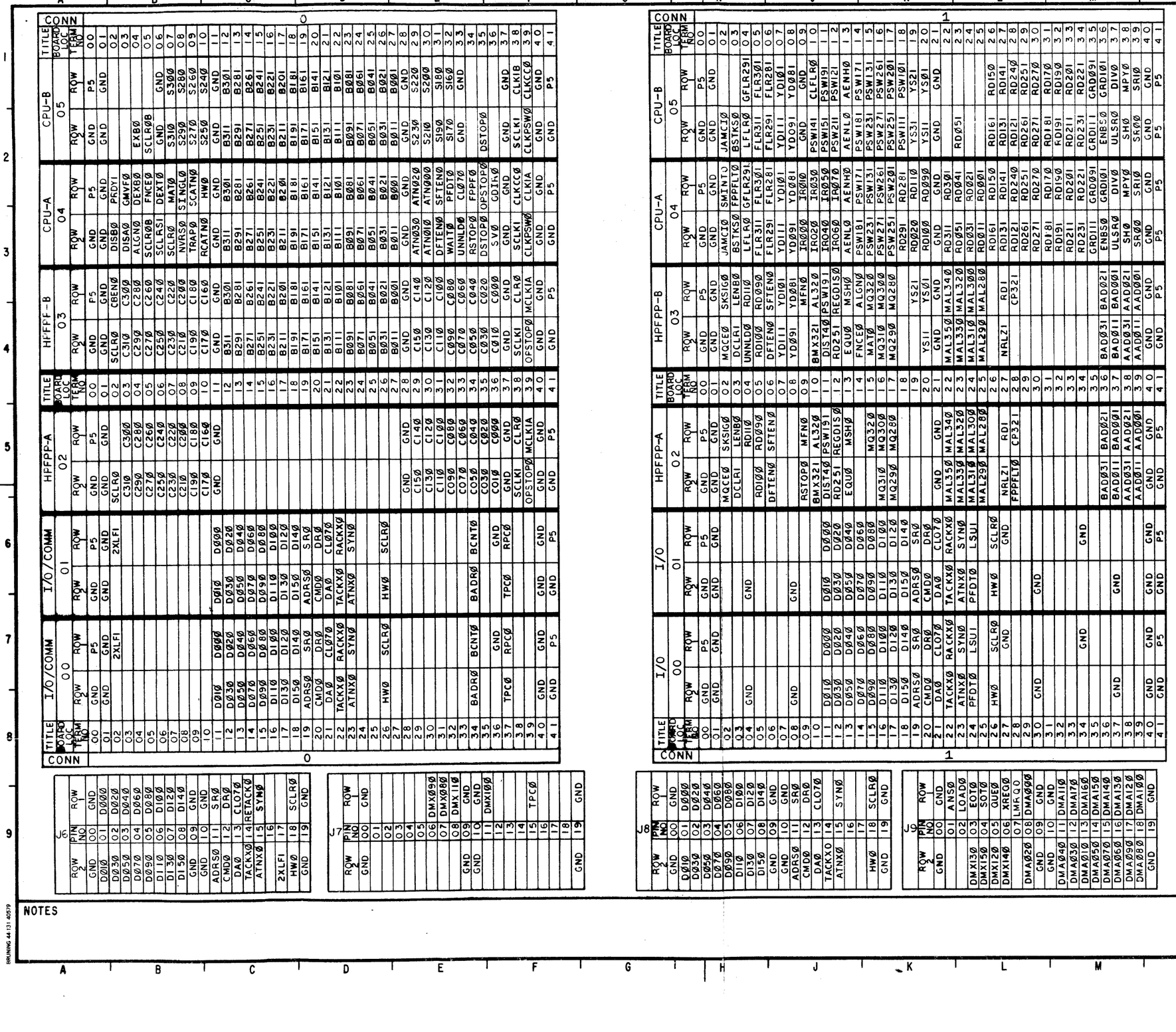
PERKIN-ELMER

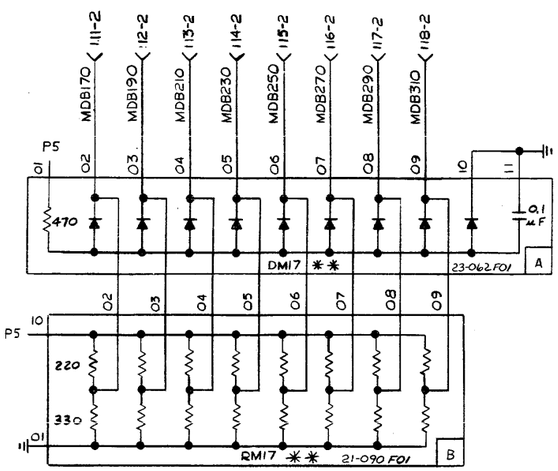
Computer Systems Division
Oceanport, N.J. 07757

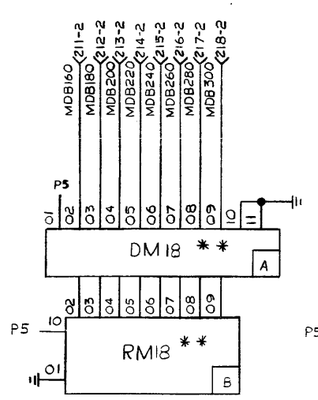
TITLE
BACKPANEL

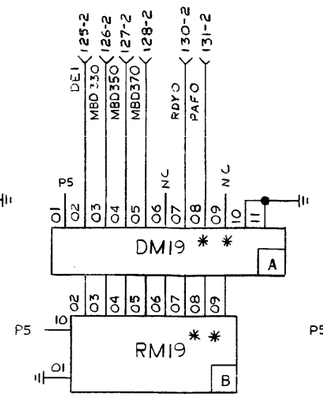
TASK 03976 | SHT 3 - 4

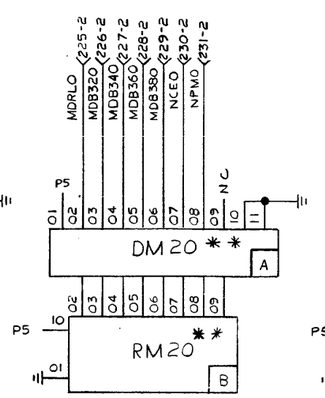
DWG 01-142 M01 R01 D08

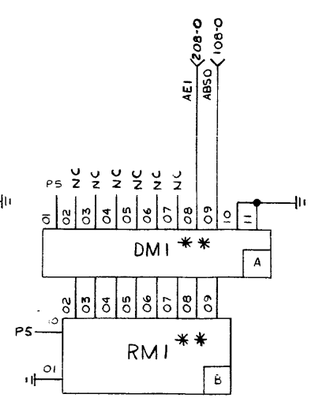

CONN 0
TITLE I/O/COMM
BOARD LOC
TERM NO
00 ROW 1 ROW 2 GND GND P5
01 ROW 1 ROW 2 GND GND P5
02 ROW 1 ROW 2 2XLF1 2XLF1
03 ROW 1 ROW 2 D000 D000
04 ROW 1 ROW 2 D010 D020
05 ROW 1 ROW 2 D030 D040
06 ROW 1 ROW 2 D050 D060
07 ROW 1 ROW 2 D070 D080
08 ROW 1 ROW 2 D090 D100
09 ROW 1 ROW 2 D110 D120
10 ROW 1 ROW 2 D130 D140
11 ROW 1 ROW 2 D150 D160
12 ROW 1 ROW 2 ADRS0 SR0
13 ROW 1 ROW 2 CMD0 DR0
14 ROW 1 ROW 2 DA0 CL070
15 ROW 1 ROW 2 TACKX0 RACKX0
16 ROW 1 ROW 2 ATNX0 SYN0
17 ROW 1 ROW 2
18 ROW 1 ROW 2
19 ROW 1 ROW 2 GND GND P5
CONN 1
TITLE I/O
BOARD LOC
TERM NO
00 ROW 1 ROW 2 GND GND P5
01 ROW 1 ROW 2 GND GND P5
02 ROW 1 ROW 2 GND GND
03 ROW 1 ROW 2 GND
04 ROW 1 ROW 2 GND
05 ROW 1 ROW 2 GND
06 ROW 1 ROW 2 GND
07 ROW 1 ROW 2 GND
08 ROW 1 ROW 2 GND
09 ROW 1 ROW 2 GND
10 ROW 1 ROW 2 D010 D000
11 ROW 1 ROW 2 D030 D020
12 ROW 1 ROW 2 D050 D040
13 ROW 1 ROW 2 D070 D060
14 ROW 1 ROW 2 D090 D080
15 ROW 1 ROW 2 D110 D100
16 ROW 1 ROW 2 D130 D120
17 ROW 1 ROW 2 D150 D140
18 ROW 1 ROW 2 ADRS0 SR0
19 ROW 1 ROW 2 CMD0 DR0
20 ROW 1 ROW 2 DA0 CL070
21 ROW 1 ROW 2 TACKX0 RACKX0
22 ROW 1 ROW 2 ATNX0 SYN0
23 ROW 1 ROW 2 PFDT0 LSUI
24 ROW 1 ROW 2 HW0 SCLR0
25 ROW 1 ROW 2 GND
26 ROW 1 ROW 2
27 ROW 1 ROW 2
28 ROW 1 ROW 2
29 ROW 1 ROW 2
30 ROW 1 ROW 2 GND
31 ROW 1 ROW 2
32 ROW 1 ROW 2
33 ROW 1 ROW 2
34 ROW 1 ROW 2 GND
35 ROW 1 ROW 2
36 ROW 1 ROW 2
37 ROW 1 ROW 2
38 ROW 1 ROW 2
39 ROW 1 ROW 2
40 ROW 1 ROW 2 GND GND P5
41 ROW 1 ROW 2 GND GND P5
HPFPP-A
02
ROW 1 ROW 2 GND GND
GND GND
MQCE0 SKSIG0
DCLA1 LENB0
RDI0 RD0B0
DFTEN0 SFTEN0
MQ320
MQ310 MQ300
MQ290 MQ280
RSTOP0 MFN0
BMX321 AL320
DIST40 PSW191
RD251 REGDIS0
EQU0 MSH0
MAL350 MAL340
MAL330 MAL320
MAL310 MAL300
MAL290 MAL280
NRLZ1 RDI
FPPFLT0 CP321
BAD031 BAD021
BAD011 BAD001
AAD031 AAD021
AAD011 AAD001
HPFPP-B
03
ROW 1 ROW 2 GND GND
GND GND
MQCE0 SKSIG0
DCLA1 LENB0
UNNLD0 RD110
C000 C0B0
C010 C0A0
C020 C090
C030 C080
C040 C070
C050 C060
C060 C050
C070 C040
C080 C030
C090 C020
C0A0 C010
C0B0 C000
SCLK1 CLR0
OPSTOP0 MCLKIA
GND GND P5
GND GND P5
CPU-A
04
ROW 1 ROW 2 GND GND
GND GND
JAMCI0 SMINT0
BSTKS0 FPPFLT0
LFLR0 GFLR291
FLR311 FLR301
FLR291 FLR281
YDI11 YDI01
YD091 YD081
IR000 IR010
IR020 IR030
IRO40 IRO50
IRO60 IRO70
AENH0 AENL0
PSW181 PSW171
PSW231 PSW131
PSW271 PSW261
PSW251 PSW201
RD291 RD281
RD0B0 RD110
RD0D0 RD0C0
RD0F0 RD0E0
RD101 RD0A1
RD121 RD111
RD141 RD131
RD161 RD151
RD181 RD171
RD1A1 RD191
RD1C1 RD1B1
RD1E1 RD1D1
RD201 RD1F1
RD221 RD211
RD241 RD231
ENBS0 GRD101
ULSR0 DIV0
SH0 MPY0
SR00 SRI0
GND GND P5
GND GND P5
CPU-B
05
ROW 1 ROW 2 GND GND P5
GND GND
EXB0 GMVF0
SCLR0B FNCE0
GND GND
S310 S300
S290 S280
S270 S260
S250 S240
GND GND
B311 B301
B291 B281
B271 B261
B251 B241
B231 B221
B211 B201
B191 B181
B171 B161
B151 B141
B131 B121
B111 B101
B091 B081
B071 B061
B051 B041
B031 B021
B011 B001
GND GND
S230 S220
S210 S200
SI90 SI80
SI70 SI60
GND GND
DSTOP0
SCLK1 CLK1B
CLKPSW0 CLKCC0
GND GND
GND GND P5
CPU-B
05
ROW 1 ROW 2 GND GND P5
GND GND
JAMCI0
BSTKS0 LFLR0 GFLR291
FLR311 FLR301
FLR291 FLR281
YDI11 YDI01
YD091 YD081
GND GND
PSW141 CLFLR0
PSW151 PSW191
PSW211 PSW121
AENL0 AENH0
PSW181 PSW171
PSW231 PSW131
PSW251 PSW201
PSW111 PSW101
YS31 YS21
YS11 YS01
GND GND
RD051
RD161 RD150
RD131 RD141
RD121 RD240
RD261 RD251
RD271 RD270
RD181 RD170
RD191 RD190
RD211 RD201
RD231 RD221
GRD111 GRD091
ENBS0 GRD101
ULSR0 DIV0
SH0 MPY0
SR00 SRI0
GND GND P5
GND GND P5
J6
ROW 2 PIN NO ROW 1
GND 00 GND
D010 01 D000
D030 02 D020
D050 03 D040
D070 04 D060
D090 05 D080
D110 06 D100
D130 07 D120
D150 08 D140
GND 09 GND
GND 10 GND
ADRS0 11 SR0
CMD0 12 DR0
DA0 13 CL070
TACKX0 14 RETACK0
ATNX0 15 SYN0
16
2XLF1 17
HW0 18 SCLR0
GND 19 GND
J7
ROW 2 PIN NO ROW 1
GND 00 GND
01
02
03
04
05 DMX0900
06 DMX0800
07 DMX0700
08 DMX0600
GND 09 GND
GND 10 GND
11 DMX0100
12
13
14
15 TPC0
16
17
18
GND 19 GND
J8
ROW 2 PIN NO ROW 1
GND 00 GND
D010 01 D000
D030 02 D020
D050 03 D040
D070 04 D060
D090 05 D080
D110 06 D100
D130 07 D120
D150 08 D140
GND 09 GND
GND 10 GND
ADRS0 11 SR0
CMD0 12 DR0
DA0 13 CL070
TACKX0 14
ATNX0 15 SYN0
16
17
HW0 18 SCLR0
GND 19 GND
J9
ROW 2 PIN NO ROW 1
GND 00 GND
01 ANS0
02 LOAD0
DMX130 03 EOT0
DMX150 04 SOT0
DMX120 05 QUE0
DMX140 06 XREQ0
07 LMRQ0
DMA020 08 DMA0900
GND 09 GND
GND 10 GND
DMA040 11 DMA110
DMA030 12 DMA170
DMA010 13 DMA160
DMA050 14 DMA150
DMA070 15 DMA140
DMA060 16 DMA130
DMA090 17 DMA120
DMA080 18 DMA100
GND 19 GND
NOTES
REVISIONS
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757
"INFORMATION DISCLOSED HEREIN IS THE PROPERTY OF THE PERKIN-ELMER CORPORATION, COMPUTER SYSTEMS DIVISION, AND SHALL NOT BE DISCLOSED OR USED FOR ANY OTHER PURPOSES EXCEPT AS SPECIFIED BY CONTRACT BETWEEN THE RECIPIENT AND THE PERKIN-ELMER CORPORATION. DUPLICATION OF ANY PORTION OF THIS DATA SHALL INCLUDE THIS LEGEND.
TITLE
BACKPANEL
TASK 03976
SHT 4 - 4
DWG 01-142 M01 D08
8RUNNING 44-131 40579

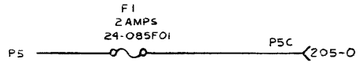


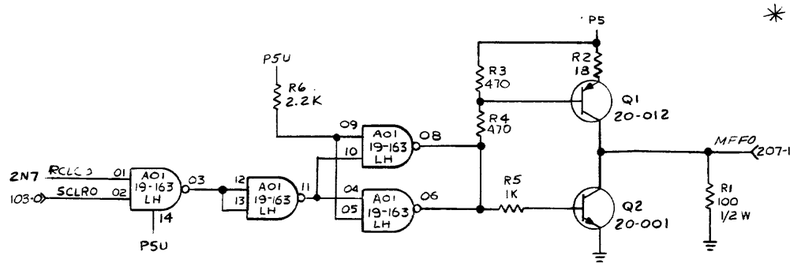












PIN NO	35-772 F00, F01 & F02 CONNECTOR 0 ROW 2	ROW 1	35-772 F00 & F01 CONNECTOR 1 ROW 2	ROW 1	35-772 F00 & F02 CONNECTOR 2 ROW 2	ROW 1
43	GND	GND	GND	GND	GND	GND
42	MAB320	MAB330	BSCLRO			
41	MAB300	MAB310	RCLCO			
40	MAB280	MAB290	GND			
39	MAB260	MAB270	GND			
38	MAB240	MAB250	MXO21			
37	MAB220	MAB230	MXO31	MXO11		
36	MAB200	MAB210	LMB371	LMB381		
35	MAB180	MAB190	LMB351	LMB361		
34	GND	GND	GND	GND	GND	GND
33	GND	GND	GND	GND	GND	GND
32	MAB160	MAB170	LMB331	LMB341		
31	MAB140	MAB150	LMB311	LMB321	NPMO	PAFO
30	MAB120	MAB130	LMB291	LMB301	NCEO	RDYO
29	MAB100	MAB110	LMB271	LMB281	MDB 380	
28	MAB080	MAB090	LMB251	LMB261	MDB360	MDB370
27	MAB060	MAB070	LMB231	LMB241	MDB340	MDB350
26	MAB040	MAB050	LMB211	LMB221	MDB320	MDB330
25	MAB020	MAB030	LMB191	LMB201	MDRLO	DEI
24	GND	GND	GND	GND	GND	GND
23						
22						
21						
20						
19	GND	GND	GND	GND	GND	GND
18	MAB000	MAB010	LMB171	LMB181	MDB300	MDB310
17	MAR030	MAG030	LMB151	LMB161	MDB280	MDB290
16	MAR020	MAG020	LMB131	LMB141	MDB260	MDB270
15	MAR010	MAG010	LMB111	LMB121	MDB240	MDB250
14	MAR000	MAG000	LMB091	LMB101	MDB220	MDB230
13	ARO	ARYO	LMB061	LMB081	MDB200	MDB210
12	ABYO	WDRYO	LMB051	LMB061	MDB180	MDB190
11	ARQO	AHRPO	LMB031	LMB041	MDB160	MDB170
10	GND	GND	GND	GND	GND	GND
09	GND	GND	GND	GND	GND	GND
08	AEI	ABSO	LMB01	LMB021	MDB140	MDB150
07			MPFO	LMB001	MDB120	MDB130
06			MEA030	MEA020	MDB100	MDB110
05	P5C (NOTE 3)		MEA010	MEA000	MDB080	MDB090
04			MWA010	MWA000	MDB060	MDB070
03		SCLRO (NOTE 3)	MREFO	MCCO	MDB040	MDB050
02			MRDSO	MCIO	MDB020	MDB030
01			MWEO	MREO	MDB000	MDB010
00	GND	GND	GND	GND	GND	GND

NOTES:
1. UNLESS OTHERWISE SPECIFIED,
   ALL DIODES ARE 23-034
   ALL RESISTORS ARE 1/4 W, ± 5%
   ALL RESISTORS MODULES ARE 21-090 F01
   ALL DIODE MODULES ARE 23-062 F01
2. ALL COMPONENTS SHOWN ARE ON 35-772 F00
   COMPONENTS MARKED WITH AN ASTERISK (*) ARE ON 35-772 F00 & F01 VERSIONS ONLY
   COMPONENTS MARKED WITH A DOUBLE ASTERISK (**) ARE 35-772 F00 & F02 VERSIONS ONLY.

NOTE 3: THESE SIGNALS ALSO INCLUDED ON F01 TERMINATOR

USED IN MANUAL 47-004
PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-772 F00	R01
35-772 F01	R01
35-772 F02	R01

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

VARIATION TABLE

F02	DOUBLE ASTERISK (FIELDS 0 & 2)
F01	ONE ASTERISK (FIELDS 0 & 1)
F00	AS SHOWN (FIELDS 0, 1, & 2)

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

PRE PRODUCTION APPROVAL	DEV	INIT	DATE

NOTE 3 ADDED. CONN 1, ROW 2, PIN NO.'S 37-40 WERE ADDED. CONN 1, ROW 1, PIN NO. 37 ADDED. AREA L5 WAS 35-772 F00, F01, F02. TITLE WAS M3250 BUS TERM. BD. (PSU). SHT. 1&2

ECI	EE	4934	7-22-80	R01

RELEASED FOR PRODUCTION
ENG. [illegible] DATE 7-24-80

SCALE – NONE

TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

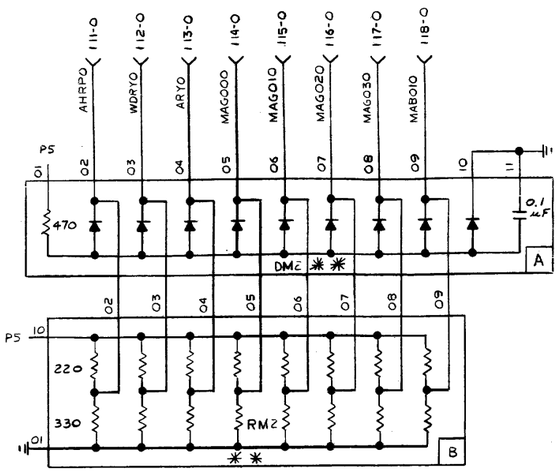
NAME	TITLE	DATE
B. GRAY	DRAFT	7-24-80
R. CERO	CHK	7-24-80
ROBROA	ENGR	7-24-80
R. BARKER	QC	7-24-80
E. GREENSTEIN	SYS. TEST	7-24-80

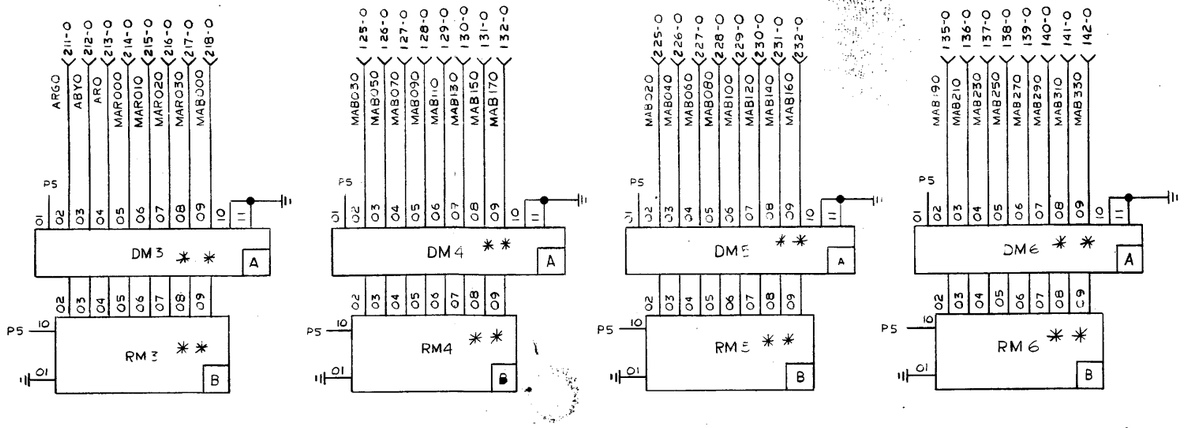
TITLE 3200 SERIES BUS TERM (PSU)

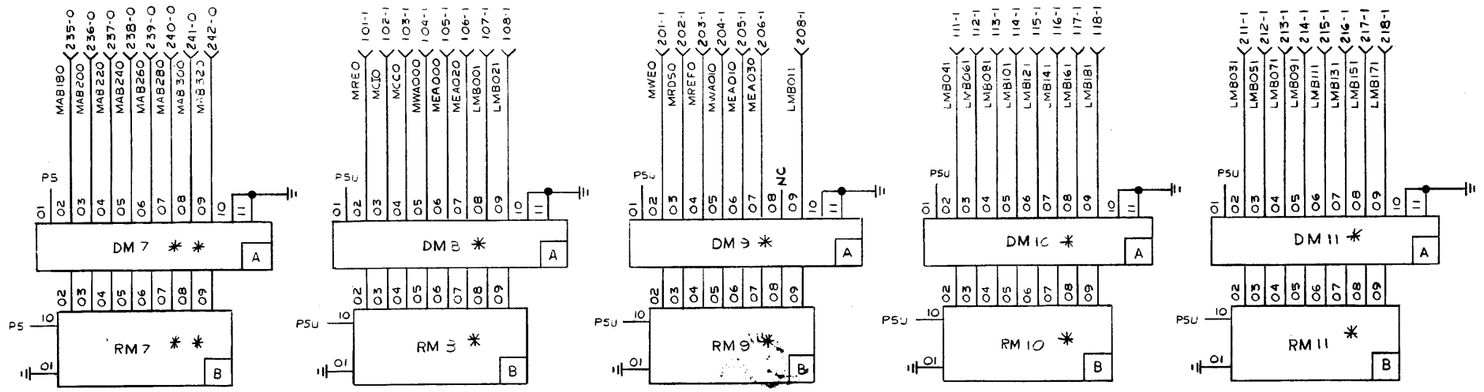
TAPE NO. 03979 SHEET OF 1 — 2
DWG NO. 35-772 R01 DOB

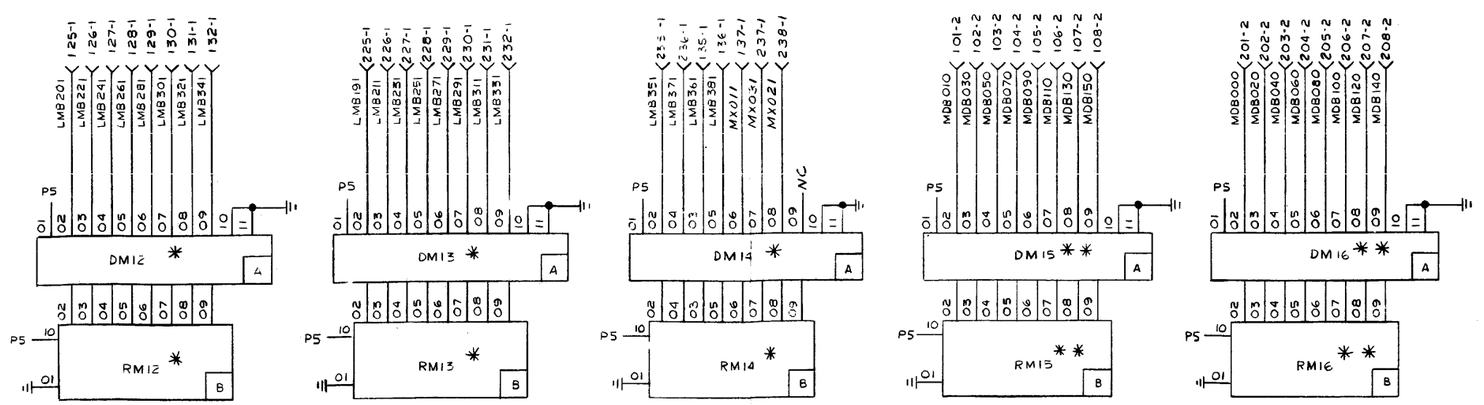
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

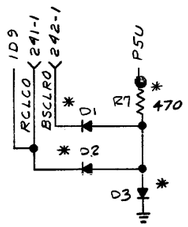
REVISIONS









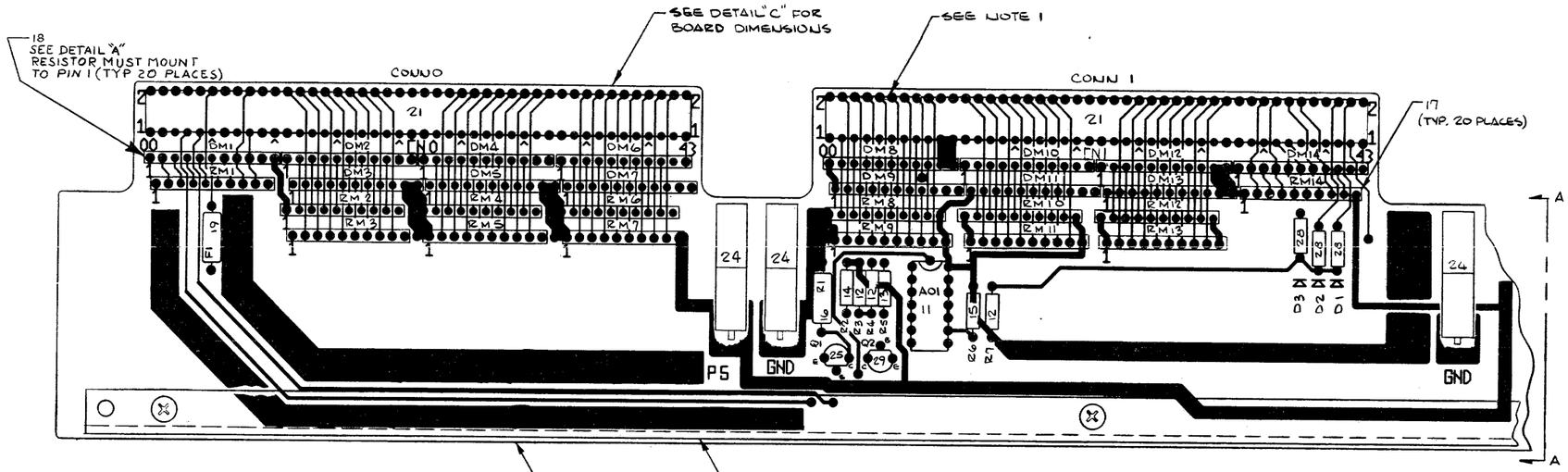


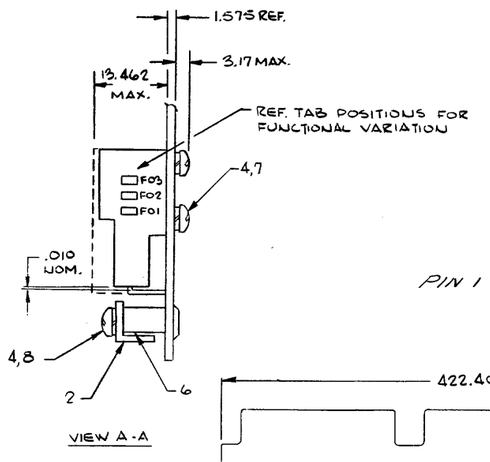
SCALE – ~	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	B. GRAY	DRAFT	
	R. CERO	CHK	
	P. OBRDA	ENGR	
	R. BARKER	Q.C.	
	E. GREENSTEIN		

TITLE
3200 SERIES
BUS TERM (PSU)

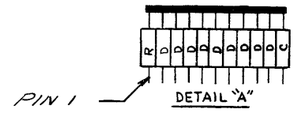
TASK NO. 03979
DWG NO. 35-772R01 D08
SHEET OF 2 – 2

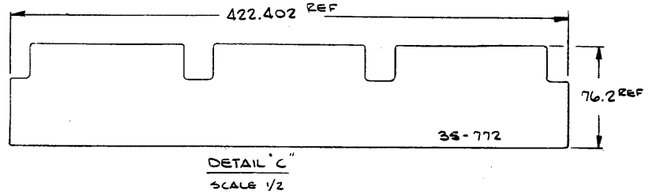
MILLIMETERS	INCHES
422.402	16.630
76.2	3.00
13.462	.530
3.175	.125
1.575	.062



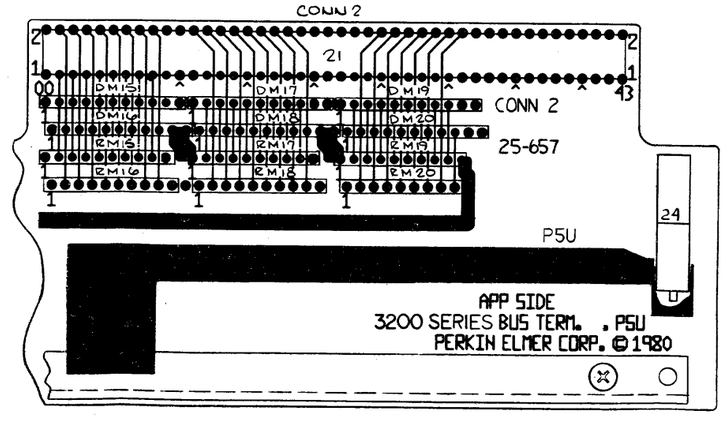


VIEW A-A





DETAIL "C"
SCALE 1/2



36-772 F00

METRIC

USED IN MANUAL 47-004

NOTES 1. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING.

BRUNING 44-131 40579

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	
	PROD	7-24-80

TITLE WAS ASSY BUS TERM., M3250, P5U (FIELDS 0,1&2) SHTS. 1-3

ECJ	RC	9939		7-23-80	R01

RELEASED FOR PRODUCTION
MFG. ENG. P Ubdo DATE 7-24-80

REVISED CIRCUITRY ON F00-F02. REVISED SHTS 1-3.

KR	GJ	5046	R	9-20-82	R02

F02	SEE SHT. 3
F01	SEE SHT. 2
F00	SEE SHT. 1
VARIATIONS	

UNLESS OTHERWISE SPECIFIED

SCALE: 2/1

TOLERANCE: .XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

DIMENSIONS ARE IN MILLIMETERS

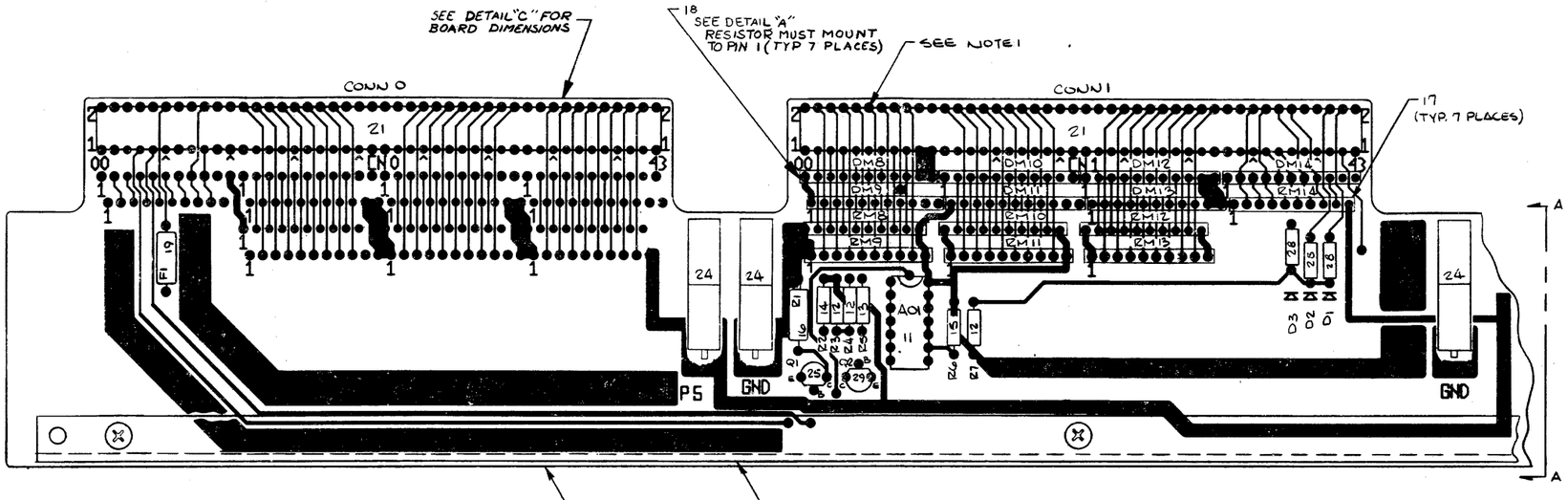
NAME		TITLE	DATE
B. GRAY	G. SHINN	DES/DFT	2-18-80
R. CERO		SUPV	7-24-80
R. CERO		CHK	7-24-80
P. OBRDA		ENG	7-24-80
D. FRANKENBERGER		MGR	7-24-80
R. BARKER		QC	7-24-80

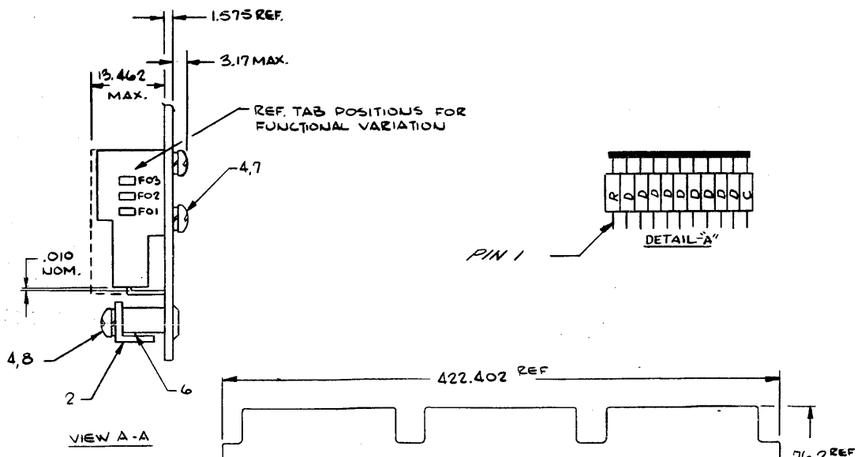
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

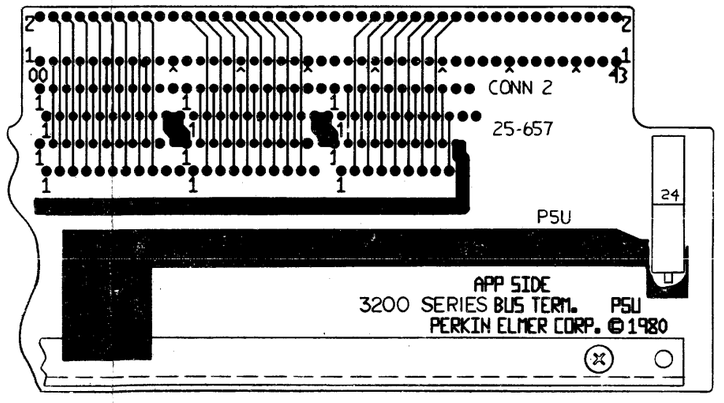
TITLE
3200 SERIES
BUS TERM P5U
(FIELDS 0,1 & 2)

TASK 03979	SHT
DWG 36-772 R02 D03	1 - 3

MILLIMETERS	INCHES
422.402	16.630
76.2	3.00
13.462	.530
3.175	.125
1.575	.062







35-772 F01

METRIC

NOTES 1. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING.

BRUNING 44-131 40579

REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE: 2/1		TOLERANCE:	
DIMENSIONS ARE IN MILLIMETERS		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
B. GRAY	G. SHINN	DES/DFT	2-18-80
R. CERO		SUPV	
R. CERO		CHK	
P. OBRDA		ENG	
D. FRANKENBERGER		MGR	
R. BARKER		QC	

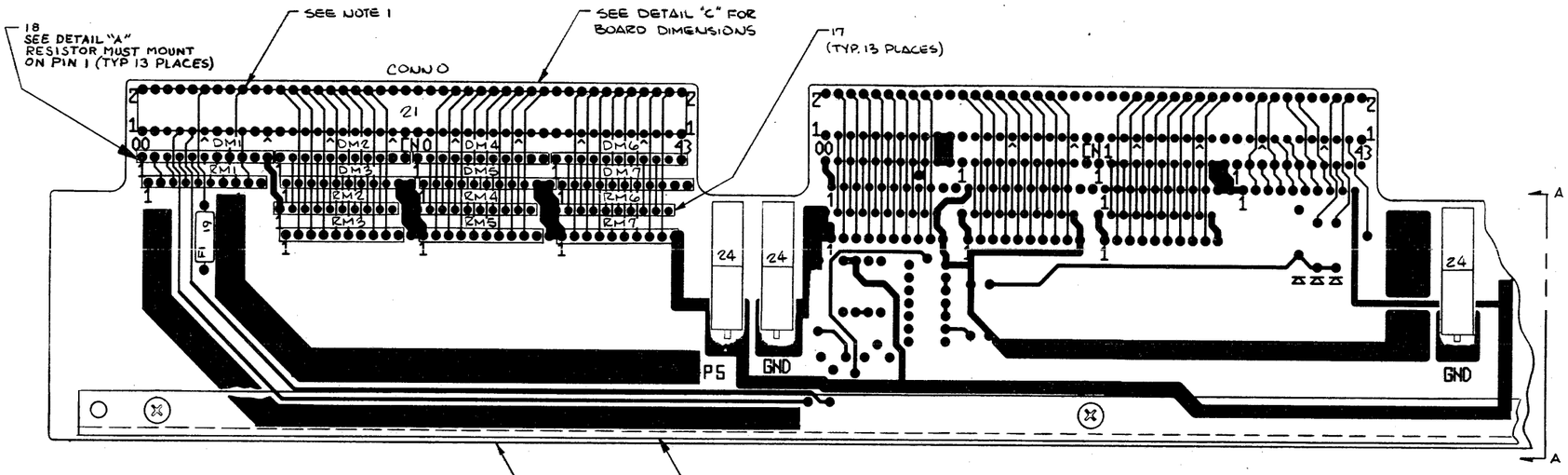
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

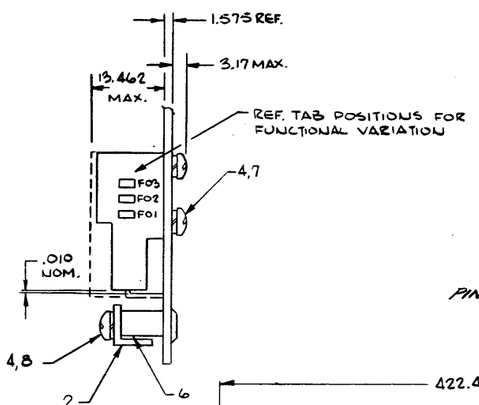
TITLE
3200 SERIES
BUS TERM P5U
(FIELDS 0 & 1)

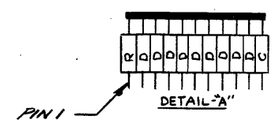
TASK 03979	SHT
DWG 35-772 R02 D03	2 - 3

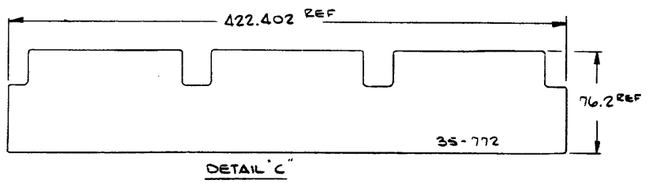
MILLIMETERS	INCHES
422.402	16.630
76.2	3.00
13.462	.530
3.175	.125
1.575	.062

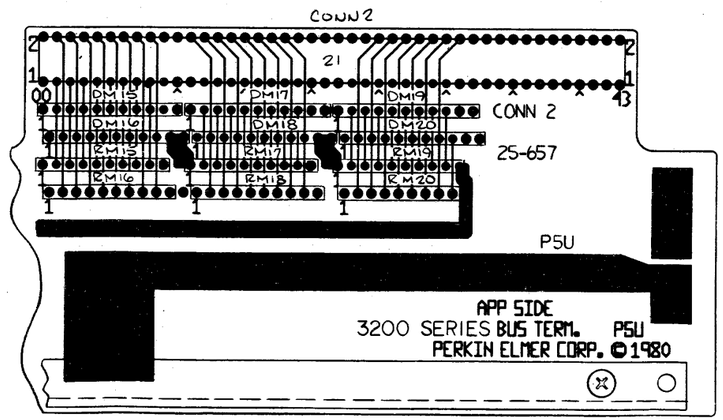
REVISIONS











35-772 F02

METRIC

NOTES 1. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING.

BRUNING 44-131 40679

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN MILLIMETERS	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
B. GRAY	G. SHINN	DES/DFT	2-18-80
R. CERO		SUPV	
R. CERO		CHK	
P. OBRDA		ENG	
D. FRANKENBERGER		MGR	
R. BARKER		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE
3200 SERIES
BUS TERM P5U
(FIELDS 0 & 2)

TASK 03979

DWG 35-772 R02 D03

SHT 3 - 3

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