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81-010 HOW TO USE MAIN STORAGE PROCESSOR ERROR INFORMATION

Main storage processor error information is used to determine the cause of failures of the main storage processor. These failures may be either intermittent failures or failures that the MAPs do not find.

Run the error recording analysis procedure for the main storage processor, and look at the error information that was recorded. If status byte 2 contains a repeating pattern of hexadecimal values, suspect an intermittent failure. Go to MAP 8101 to determine the failing FRU (field replaceable unit).

If there is not a repeating pattern in status byte 2 of the error history information, go to paragraph 81-200 for a general description of what the recorded information means and where to look for more detail.

81-200 MAIN STORAGE PROCESSOR ERROR HISTORY INFORMATION

An example of the main storage processor error history information that is recorded is shown in the following sample printout.

```
ERROR HISTORY TABLE FOR MAIN STORAGE PROCESSOR
                                        ATRS          PROG   STATUS   FAIL.

IAR  ARR  XR1  XR2  OP1  OP2  IR O1 O2 OP Q  MR SR  0  2  3  ADDR.  DATE   TIME
.......................... HEX ..................................... YYMMDD HHMMSS
096E 0952 1E58 BD00 BD01 BD00 01 17 17 AF 01 00 01 2B 61 00 00BD01 770413 000009
096E 0952 1E58 BD00 BD02 BD01 01 17 17 AF 02 00 01 2B 61 00 00BD02 770413 000009
096E 0952 1E58 BD00 BD01 BD00 01 17 17 AF 01 00 01 2B 61 00 00BD01 770413 000009
096E 0952 1E28 BD00 BD02 BD01 01 17 17 AF 02 00 01 2B 61 00 00BD02 770413 000303
```

81-310 Instruction Address Register Contents
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81-300 MAIN STORAGE PROCESSOR SENSE BYTES–GENERAL INFORMATION

The information recorded is that which was present when the error occurred. The amount of information recorded relies on the programs that were running in the system at that time. If the main storage error recovery routine senses a parity check in any of the registers (IAR, ARR, XR1, XR2, Op1, or Op2), the routine fills the register with 7777 to indicate that the register contents are not known.

81-310 INSTRUCTION ADDRESS REGISTER (IAR)

The instruction address register value (also an address translation register if address translation is used) determines where in main storage the next byte of the system instruction is located.

81-320 ADDRESS RECALL REGISTER (ARR)

The ARR (address recall register) contains a main storage address which is used as a pointer. The ARR points to the byte *after* the last Branch instruction that completed a correct branch. Decimal operations (ZAZ, AZ, and SZ) and the ITC (Insert and Test Character) also change the contents of the ARR.

81-330 INDEX REGISTER 1 (XR1)

The XR1 (index register 1) contents are used if the operand addresses are to be determined by indexing using index register 1. The value of the operand address is calculated by adding 1 byte in the instruction being fetched to the index register value.

81-340 INDEX REGISTER 2 (XR2)

The XR2 (index register 2) contents are used if the operand addresses are to be determined by indexing using index register 2. The value of the operand address is calculated by adding 1 byte in the instruction being fetched to the index register value.

81-350 OPERAND 1 (OP1)

The Op1 (operand 1) value (also an address translation register value if address translation is used) determines where in main storage the next byte of operand 1 is located.

81-360 OPERAND 2 (OP2)

The Op2 (operand 2) value (also an address translation register value if address translation is used) determines where in main storage the next byte of operand 2 is located.

81-370 ADDRESS TRANSLATION REGISTERS (ATRs)

If address translation is being used when the error occurred, the log out includes the ATRs (address translation registers) which are necessary to determine the real location in main storage that was being addressed at the time of the error.

81-371 Instruction Translation Register

If address translation is being used during I-FETCH, the instruction translation register (ATRs IR) value is the value of the address translation register that is used with the instruction address register to determine the real location in main storage that was addressed while fetching the instruction.

81-372 Operand 1 Translation Register

If address translation is being used during operand 1 fetch cycles (EB time), ATR 01 register value is the value of the address translation register that is used with the operand 1 address register (Op1) value to determine the real location in main storage that was addressed for operand 1.

81-373 Operand 2 Translation Register

If address translation is being used during operand 2 fetch cycles (EA time), the ATR 02 register contains the value of the address translation register that is used with the operand 2 address register (Op2) value to determine the real location in main storage that was addressed for operand 2.

81-380 OPERATION CODE

This field in the printout contains the operation code of the instruction that was being executed when the error occurred that caused the log out.

81-390 Q CODE

This field in the printout contains the Q code of the instruction that was being executed when the error occurred that caused the log out.

81-400 PROGRAM MODE REGISTER (PMR)

This register contains information that is used to determine if address translation was being used when the error occurred that caused the log out.

Program Mode Register

Bit 0–off = enable, on = disable task switching
Bits 1, 2, 3–not used
Bit 4–translated main storage processor addressing during instruction fetch (I) cycles
Bit 5–translated main storage processor addressing during operand 2 fetch (EA) cycles
Bit 6–translated main storage processor addressing during operand 1 fetch (EB) cycles
Bit 7–privileged mode

81-410 PROGRAM STATUS REGISTER (PSR)

The PSR (program status register) contains information about the status of the last operation (of the type that affects the PSR) performed in the main storage processor.

Program Status Register

Bits 0, 1–not used
Bit 2–binary overflow
Bit 3–test false
Bit 4–decimal overflow
Bit 5–high
Bit 6–low
Bit 7–equal

81-420 STATUS BYTES

The status bytes contain information about the current state of the system when the error occurred that caused the log out. (See paragraphs 81-421, 81-422, and 81-423.)

81-421 Status Byte 0

Status byte 0 contains information about where in the instruction fetch or execution cycles the main storage processor was when the error occurred.

Status byte 0

Bit 0–not used
Bit 1–complement latch set
Bits 2, 3, 4, 5–encoded next major cycle times
0000 = Op time
0001 = Q time
0010 = IH1/IX1 time
0011 = IL1 time
0100 = IH2/IX2 time
0101 = IL2 time
1000 = EA time
1010 = EB time
1100 = EC time
Bits 6, 7–encoded last minor times
11 = MA
10 = MB
01 = MD
00 = MC

Note: Status byte 1 register cannot be sensed.

81-422 Status Byte 2

Status byte 2 contains information about main storage processor checks, and other states of the main storage processor when the error occurred.

Status byte 2

Bit 0–instruction cannot be executed
Bit 1–control gate check
Bit 2–local storage register gate check
Bit 3–main storage gate check
Bit 4–first cycle
Bit 5–recomplement cycle
Bit 6–main storage processor address checks
Bit 7–carry trigger

81-423 Status Byte 3

Status byte 3 contains information about main storage checks caused by the main storage processor when the error occurred.

Status byte 3

Bits 0 through 5 are not used

Bits 6	7	
0	1	Storage exception check
1	0	Main storage address check
1	1	MSAR parity check

81-430 FAILING ADDRESS

The failing address field indicates the real main storage location that was being addressed when the error occurred. When the failing address cannot be determined or when main storage is not being addressed, the failing address field is X'0000'.

Use the chart in MAP 8101 as a cross-reference between the failing address and the probable failing FRU.