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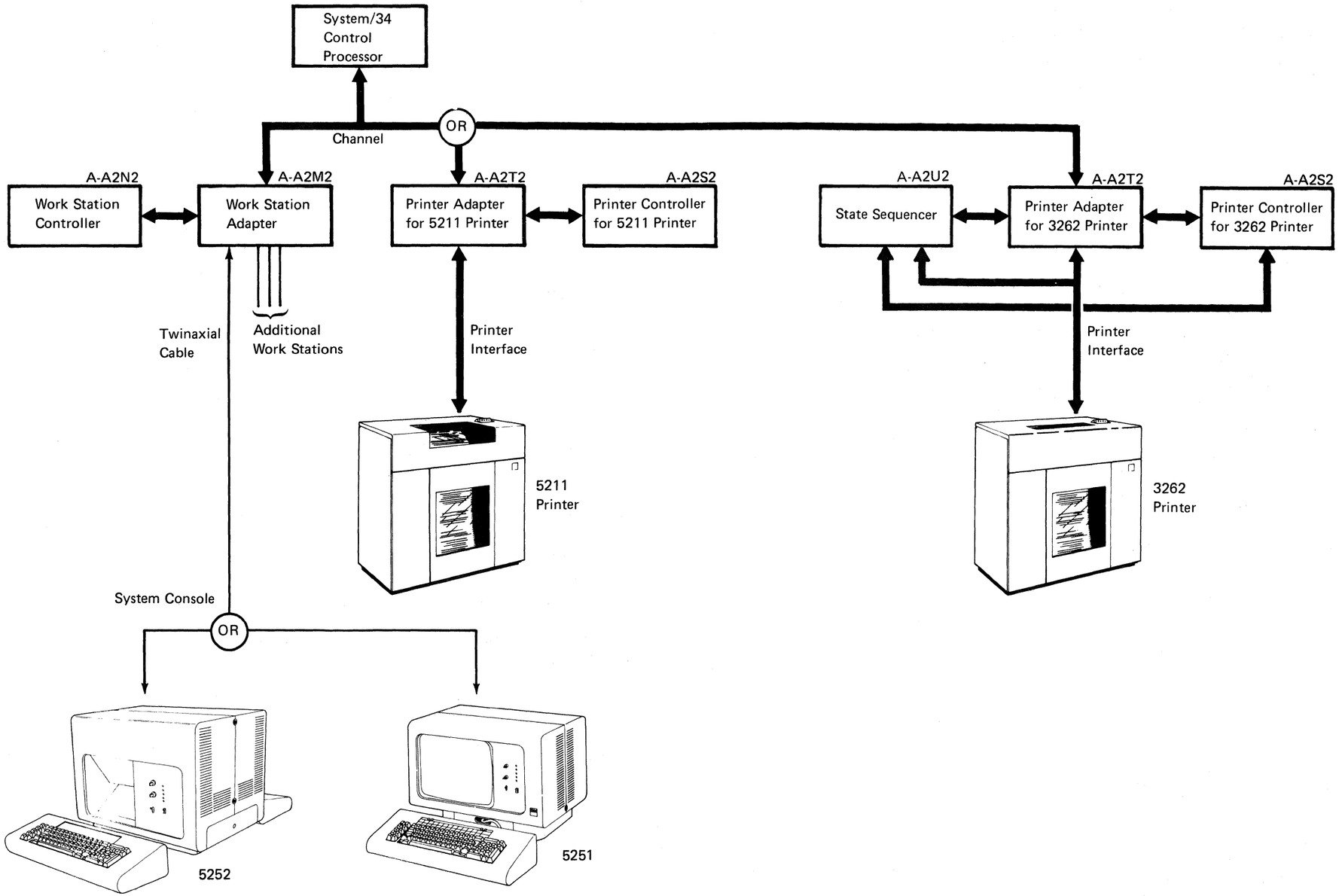
Attachment Controller 1

INTRODUCTION

The system console and all other work stations are attached to System/34 by the work station attachment; the 3262/5211 Printer is attached to System/34 by the printer attachment. Each attachment has an adapter card and a controller card. The controller card for the work station attachment is located in A-A2N2; the controller card for the 3262/5211 Printer attachment, if used, is in A-A2S2. The controller cards are of the same type and can be swapped.

The controller cards contain the following:

- Four-bit ALU and data flow.
- Eight bits of data in on controller DBI (CDBI).
- Eight bits of data out on controller DBO (CDBO).
- Parity checking on storage data, controller DBO, and controller DBI.
- Storage addressing lines for up to 64K bytes of storage using the storage address register (SAR). For the storage address, there are:
  - Sixteen bits of instruction out
  - Eight bits of data in
  - Eight bits of data out
- 2K bytes of random access memory (byte addresses from 0 to 2047).
- Forty-eight 4-bit, general-purpose registers (16 data address registers, 16 primary registers, and 16 auxiliary registers).
- Two levels of branch and link.
- Single-level interrupt.
- Operating speeds of:
  - 750 nanoseconds per instruction
  - 1.5 microseconds per storage instruction

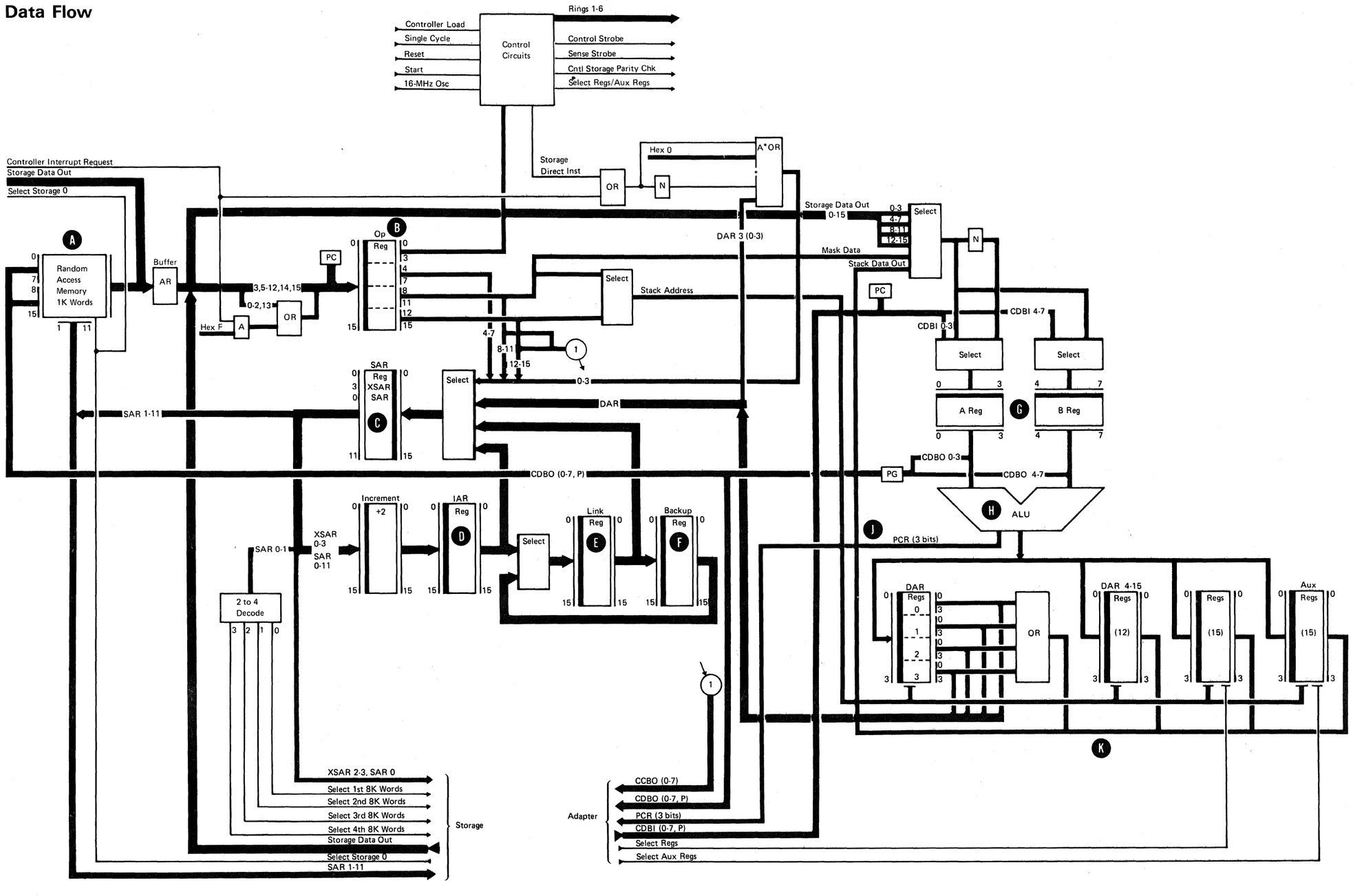


DATA FLOW AND FUNCTIONAL UNITS

The functional units and data flow figure, as described and shown in this section, are for the controller cards only. Because the controller cards are only a part of the work station and printer attachments, see the *Work Station Attachment* section for a description of the work station adapter card, the *3262 Printer Attachment* section for a description of the 3262 printer adapter cards, and the *5211 Printer Attachment* section for a description of the 5211 printer adapter card.

The data flow figure shows, in addition to the data flow, many of the control lines between the controllers and the adapter cards. For a description of these lines, see *Controller Lines* later in this section.

Data Flow



Functional Units

The functional units, as described here, are shown in the data flow figure on the preceding page.

Random Access Memory (A)

The controller card contains 2K bytes (1K words) of random access memory. Additional storage is on the sequencer card for the 3262 Printer or on the adapter card for the 5211 Printer and on the storage cards for the work stations.

Each word in storage has both the high byte (bits 0 through 7) and the low byte (bits 8 through 15). Storage output is 2 bytes wide; both bytes are selected when a word is taken from storage to be executed, and 1 byte is selected when data is read from storage. Storage input, on the other hand, is only 1 byte wide. It is loaded into either the high or low byte of storage when data is written to storage or during a controller load operation.

Operation Register (B)

The operation register (op reg) is a 16-bit register that is loaded with each instruction taken from storage. From this register, the instruction is analyzed to control the flow of data for ALU operations, storage addressing, or general-purpose register selection.

Storage Address Register (C)

The storage address register (SAR) is a 16-bit register that is used to address storage; it is loaded from four sources:

- From the instruction address register (IAR) if the next sequential instruction is to be executed
- From data address registers 0 through 3 if a data byte read or write to storage instruction is executed
- From the op reg on branch type instructions and storage direct instructions
- From the link register during a return instruction

The SAR bits are named XSAR 0 through 3 and SAR 0 through 11.

Instruction Address Register (D)

The instruction address register (IAR) is a 16-bit register that contains the address of the next sequential instruction to be executed. It is loaded with the current SAR value, increased by a value of 2, to point to the next word to be taken from storage.

This register is also used as the source for the SAR during a controller load operation. Because storage is loaded 1 byte at a time during a controller load operation, the IAR is increased by a value of 1 during the controller load operation.

Link Register (E)

The link register is a 16-bit register that keeps an address for the first-level branch and link instruction. This register is loaded from the IAR while a branch and link instruction is being executed; it is loaded from the backup register while a return instruction is being executed (after the link register has been gated to the SAR).

Backup Register (F)

The backup register is a 16-bit register that keeps an address for the second-level branch and link instruction. For example, it backs up or keeps the link address when two branch and link instructions are executed without an intervening return instruction.

A and B Registers (G)

The A and B registers are both 4 bits wide. They contain (1) the operands for ALU operations, (2) the controller DBO (CDBO) on I/O output instructions, or (3) the data byte sent to storage on storage write or controller load operations.

Arithmetic and Logic Unit (H)

The two operands sent to the arithmetic and logic unit (ALU) from the A and B registers are processed by the ALU when the controls are activated by the contents of the op reg. The ALU output is 4 bits wide and is loaded into a general-purpose register specified by the op reg.

Processor Condition Register (J)

The processor condition register (PCR) is a 3-bit register that contains information to be tested by conditional branch instructions. The three conditions tested (zero, nonzero, and carry) are results of ALU operations. Notice on the data flow figure that the PCR is shown as an output of the ALU.

General-Purpose Registers (K)

There are forty-eight 4-bit, general-purpose registers: 16 data address registers, 16 primary registers, and 16 auxiliary registers. The primary and auxiliary register stacks are exclusive in that an instruction selects only one stack of 16 registers at a time.

The 16 data address registers (DAR) are always selected. Data address registers 0 through 3 contain the implied address on storage reference instructions. Also, data address register 3 is always the page register that selects the 4K-byte page of storage on all branch instructions.

CONTROLLER LINES

Lines to the Controller

Except for the '16-MHz osc' signal, all of the following lines to the controller are generated on either the work station adapter card or printer adapter card and are sent to the respective controller card through a top card connector.

16-MHz Oscillator

The work station driver/receiver card in location A-A2R2 supplies this signal to both the work station controller card and the printer controller card. The '16-MHz osc' signal generates all controller timings.

Reset

When the 'reset' line is active, the IAR is reset to hexadecimal 0000. Also, the 'storage output parity check' latch is reset. When the 'reset' line is not active, the controller can execute code.

Controller Load

The 'controller load' signal causes the controller to go into a single-cycle mode. The first 'start' pulse after the 'controller load' signal goes active causes the data on controller DBI (CDBI) to be gated into the A and B registers, and increases the SAR by 1. The second 'start' pulse gates the A and B registers into storage at the address contained in the SAR (SAR loaded from IAR).

Start

The controller internal clock starts when this signal goes active. If the controller is stopped when the 'start' signal goes active, the 'start' signal causes the controller to start executing code.

An active 'start' signal during a controller load operation causes data to be loaded into storage.

Controller Interrupt Request

When this signal is active, the controller:

- Inhibits the IAR from being increased.
- Inhibits selection of storage outputs.
- Forces storage output bits 0-2 and bit 13 active. This forces a branch and link instruction to an address of hexadecimal 0004.

Select Regs and Select Aux Regs

These two signals are generated on the adapter cards in response to the 'select regs/aux regs' signal from the controller. The adapter card has a latch with outputs that select either the primary or auxiliary register stacks. The 'select regs/aux regs' signal is gated with this latch on the adapter card to generate either the 'select regs' or the 'select aux regs' signal.

Lines from the Controller

The following lines from the controller are sent to the work station adapter card and printer adapter card through top card connectors.

Control Strobe

This signal goes active on an I/O output instruction when controller DBO (CDBO) is active.

Sense Strobe

This signal goes active on an I/O input instruction when controller DBI (CDBI) is received by the controller.

Select Regs/Aux Regs

This signal is generated on the controller card when either the primary or auxiliary register stack is to be selected. The adapter card responds to this signal by activating the 'select regs' line or the 'select aux regs' line.

Data Bus Lines

The data bus lines are shown on the data flow figure as those lines going to, or coming from, the adapter.

Controller Command Bus Out (CCBO)

The CCBO bus supplies 8 bits of command information to the adapter during I/O instructions.

Controller Data Bus Out (CDBO)

The CDBO bus sends 1 byte of data from the controller to the adapter or into storage (as storage data in). It is valid during 'control strobe' time on an I/O output instruction.

Processor Condition Register

The processor condition register (PCR) bits are sent to the adapter where they are kept for controller interrupts. Then, during the interrupt PCR restore routine, the bits are sent to the controller on controller DBI (CDBI). The 3 PCR bits are zero, nonzero, and carry.

Controller Data Bus In (CDBI)

The CDBI bus is used by the adapter to present 1 byte of data to the controller during an I/O input command or during a controller load operation. To see the type of data that is sent to the controller, see the data flow figures in the *Work Station Attachment*, *3262 Printer Attachment*, and *5211 Printer Attachment* sections of this manual.

Storage Select Lines

Select Storage 0

This signal selects the random access memory on the controller card. The storage output is the word in random access memory that is selected by SAR bits 1-11.

Select 8K Words (1st, 2nd, 3rd, 4th)

By using XSAR bits 0 and 1, these four signals (select 1st, 2nd, 3rd, and 4th 8K words) are generated on the controller card to select one of four 8K-word sections of storage. The lines are mutually exclusive; that is, only one line can be active during a storage operation.

XSAR 2-3, SAR 0

These 3 bits select a 1K-word (2K-byte) section of storage in the 8K-word section of storage that is selected by one of the four lines described in *Select 8K Words*.

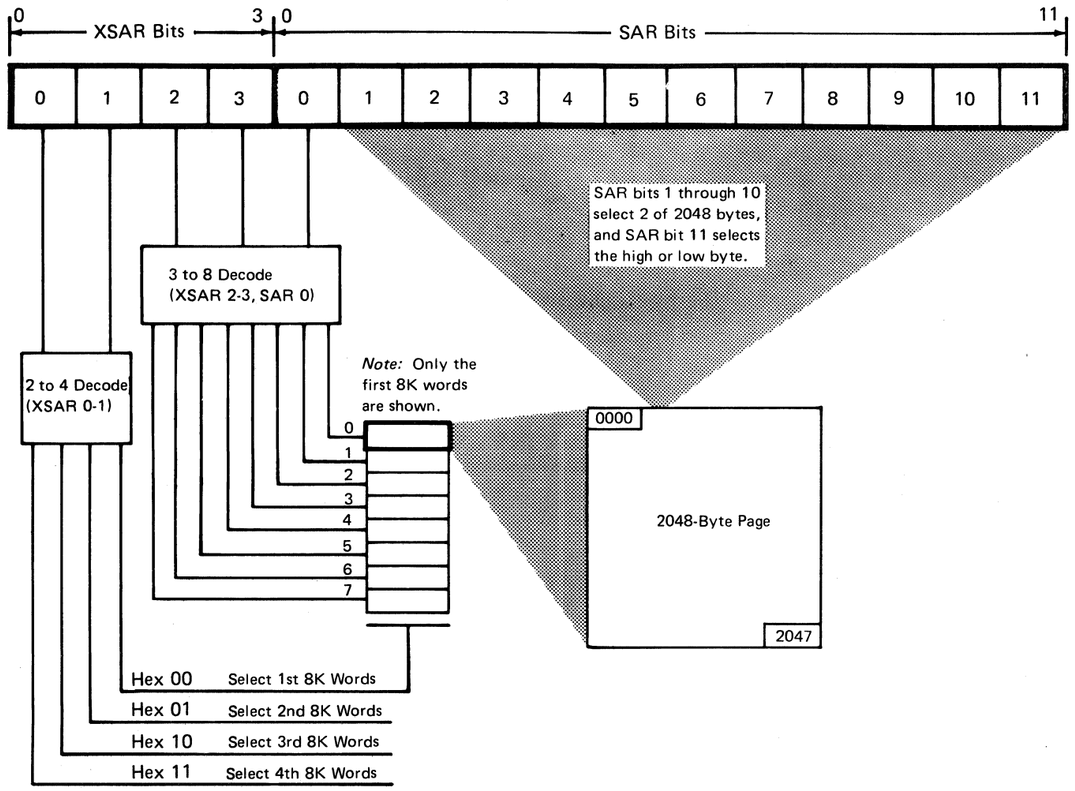
SAR 1-10

These 10 bits select one of 1,024 words in the 1K-word section of storage that is selected by the XSAR 2-3 and SAR 0 bits described in *XSAR 2-3, SAR 0*.

SAR 11

This bit selects the high or low byte of the word selected by the SAR bits 1 through 10, as described in *SAR 1-10*.

Storage Select Lines



Storage Data Lines

Storage Data In

Storage data in is shown on the data flow figure as CDBO (controller DBO). Controller DBO is the byte of data gated to storage data in on a storage write operation or during a controller load operation. Controller DBO is generated on the controller cards and sent to the storage cards (for the work station attachment) and to the adapter card (for the printer attachment) through top card connectors.

Storage Data Out

Storage data out is sent to the controller card in either of two ways:

- The work station storage cards supply a buffered storage data out. Therefore, these 'storage data out' lines are connected to the output of the buffer on the controller card.
- The printer adapter card supplies an unbuffered storage data out and is, therefore, connected to the input of the buffer on the controller card.

The 'storage data out' lines from the work station storage cards are sent to the controller card through board pins; from the printer adapter card, they are sent through top card connectors.

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