Contents

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62EH Disk Drive and Attachment

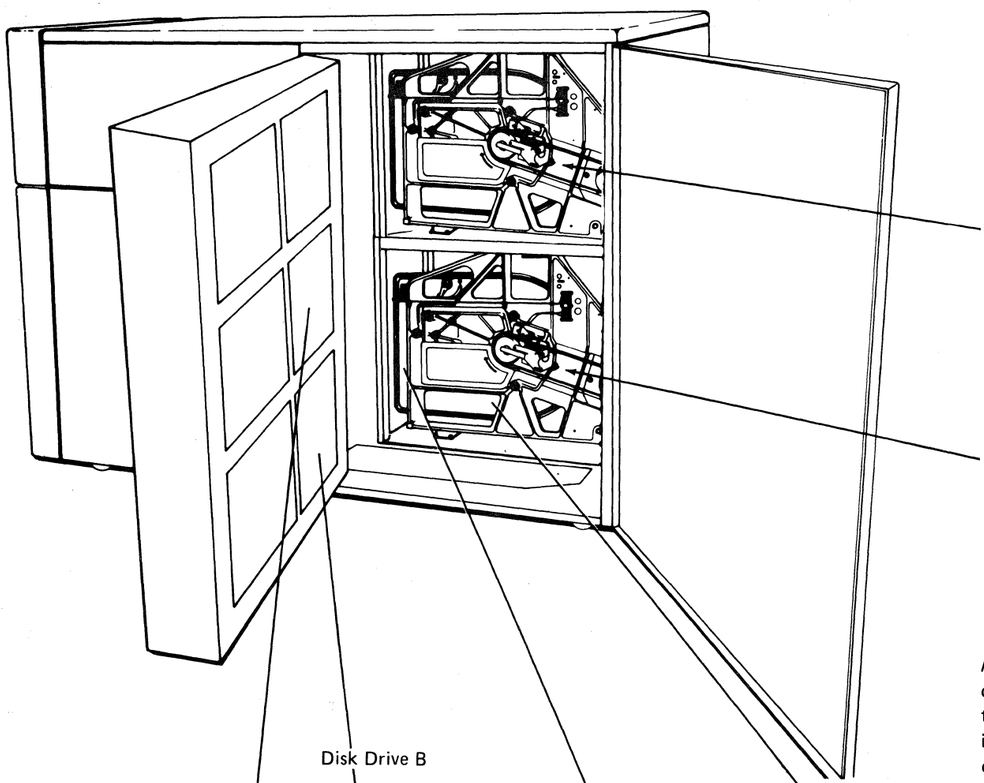
INTRODUCTION

The circuits for a disk drive are located in three separate areas: on the disk enclosure, inside the disk enclosure, and on the input/output boards.

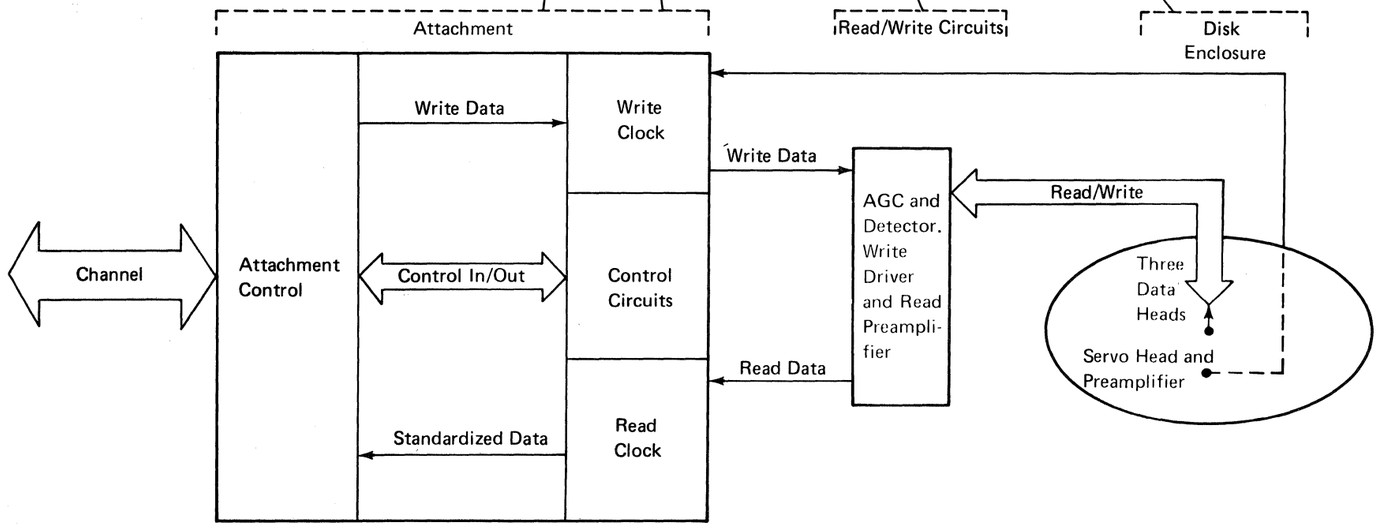
The attachment circuits on the A-A2 input/output board are for disk drive A, and the attachment circuits on the A-A3 input/output board are for disk drive B. The circuits on both input/output boards are the same. The disk drive A circuits are always located on A-A2 but, depending on your system, disk drive A could be installed in either the top or bottom frame.

62EH Disk Drive

The 62EH disk drive has one permanently installed magnetic disk. Data is written to and read from the disk by three data heads attached to an actuator. The disk drive has either 8.6 or 13.2 megabytes of customer storage. A second disk drive can be installed, which would increase total customer storage to 27.1 megabytes.



Note: When there is only one disk drive in the system, the disk drive could be installed in either the top or bottom frame.



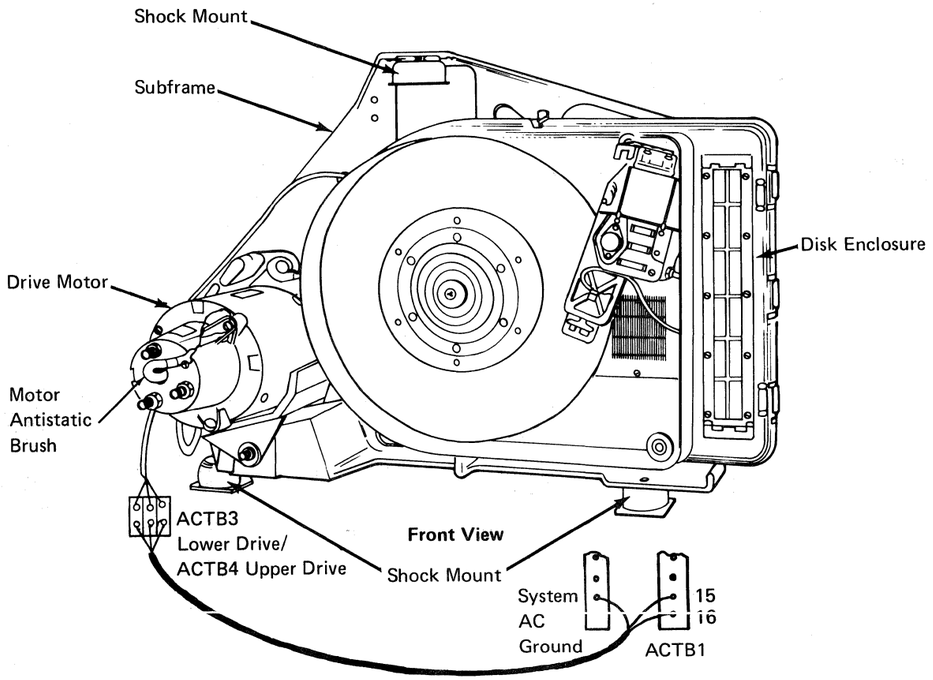
Subframe

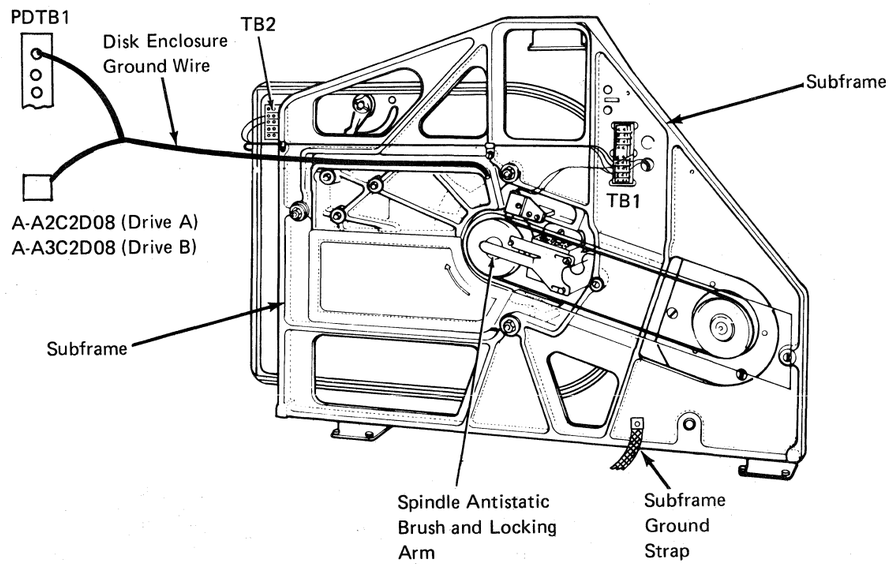
The subframe is installed vertically using three shock mounts. The shock mounts isolate the disk drive from the machine frame. The disk enclosure and the disk drive motor are installed on the subframe.

Grounding

The subframe is grounded by a ground strap connected to the machine frame. The drive motor is grounded by the system AC ground. The disk enclosure is grounded to the system DC ground. The spindle is grounded to the subframe by the spindle antistatic brush, which is part of the spindle locking arm. The motor armature is grounded by the motor antistatic brush, which is installed on the brake housing.

62EH Disk Drive





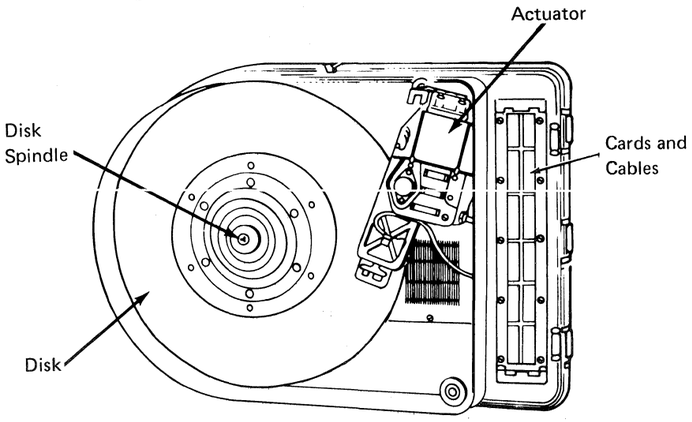
Back View

Disk Enclosure

The disk enclosure contains the disk, the disk spindle, and the actuator. These parts are visible through the clear plastic cover, but they are not accessible to the customer or the customer engineer.

Note: The disk enclosure is sealed at the factory and should not be opened in the field.

The disk enclosure has a closed-loop, air-moving system that uses blades on the spindle hub to continuously move air through the air filter. The filter lets the air pressure remain equal as the disk is getting up to speed and as the temperature inside the disk enclosure changes.

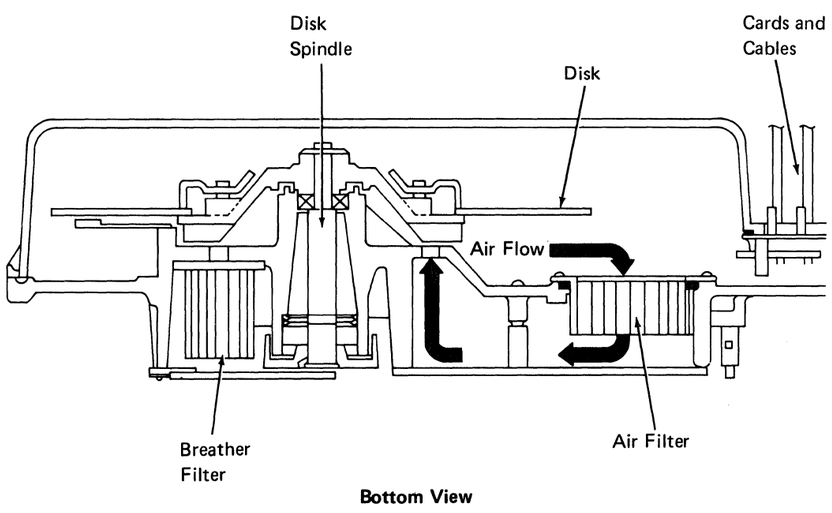


Front View

Disk Spindle

The disk spindle assembly is installed in a housing in the back of the disk enclosure. The housing is sealed to prevent dirt from getting inside the disk enclosure through the bearings.

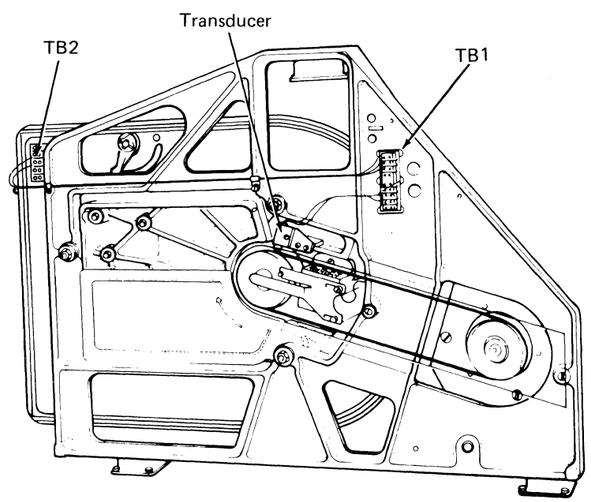
The disk is fastened to a hub on the disk spindle. A pulley is installed on the other end of the spindle and is driven by a drive motor installed on the subframe.



Bottom View

Transducer

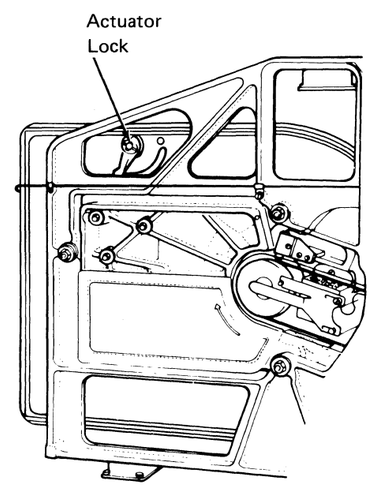
The transducer, which is installed on the disk enclosure, indicates the disk speed by sensing a slot in the spindle pulley.



Back View

Actuator Lock

The actuator lock in the On position locks the actuator in the landing zone position. The lock prevents the actuator from moving during shipment, installation, or removal of the disk enclosure.



Back View

Actuator

The actuator is inside the disk enclosure on a pivot beside the disk and carries the servo head and the data heads. The servo head and the data heads are attached to one end of the actuator, and a coil is on the other end. The coil, which is located in the field of a permanent magnet, moves when current passes through it. This causes the servo head and the data heads to move across the disk surface.

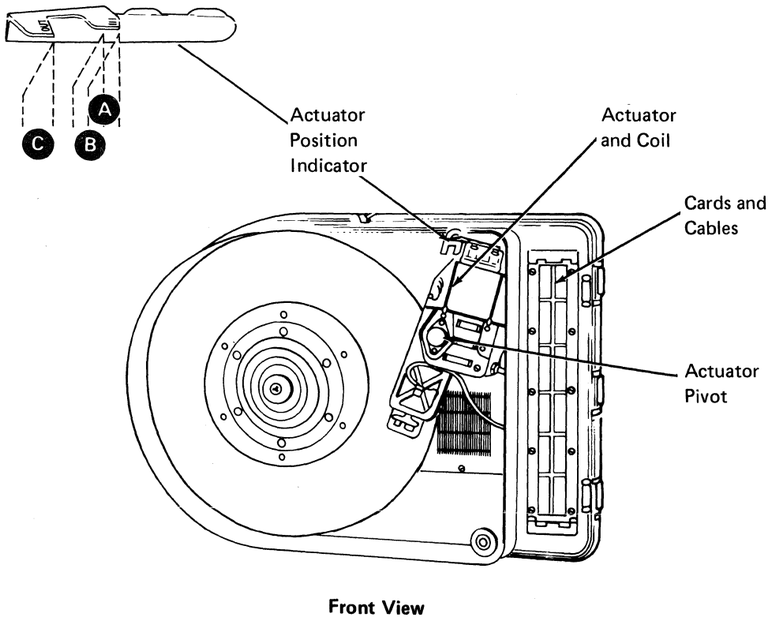
As the actuator moves across the disk surface, track-follow information is read from the servo tracks by the servo head to position the data heads over a desired data track. The servo head preamplifier is installed on the actuator close to the servo head. During any power-off condition, the actuator is retracted against the inner (spindle) stop and the magnetic catch holds the actuator in the retracted position.

Actuator Position Indicator

When the edge of the actuator coil is in line with the In edge of the indicator (A), the actuator is at the inner stop and behind home.

When the edge of the actuator coil is in line with the center of the In tab (B), the actuator is at home (cylinder 0).

When the edge of the actuator coil is in line with the Out edge of the indicator (C), the actuator is at the outer stop.



Front View

Circuit Locations

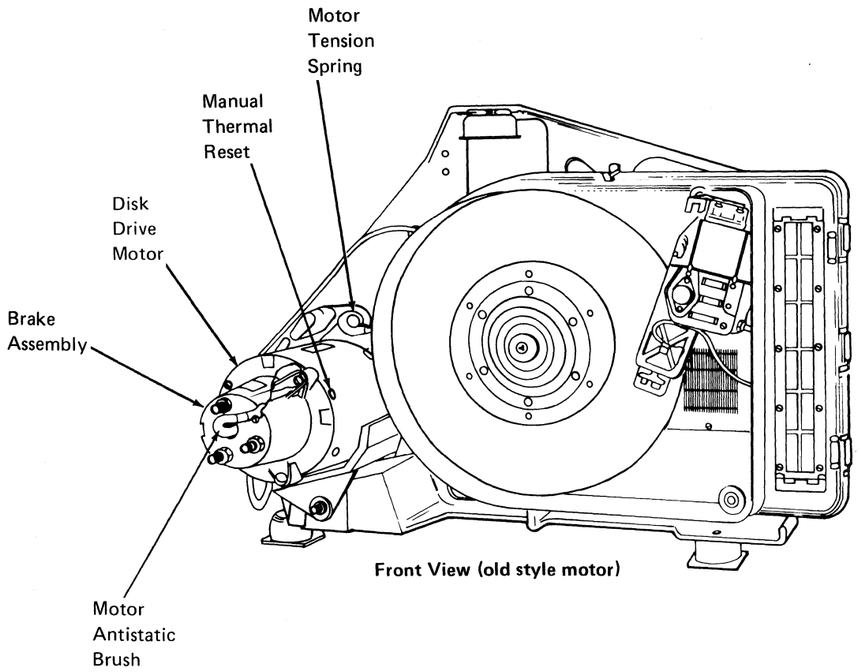
The circuits for a disk drive are installed in three separate locations. The cards and cables for the servo head output preamplifier, the write driver, and the read preamplifier are installed on the disk enclosure. The servo head preamplifier is installed on the actuator inside the disk enclosure. The remainder of the circuits are installed on either the A-A2 input/output board or the A-A3 input/output board.

Motor and Brake

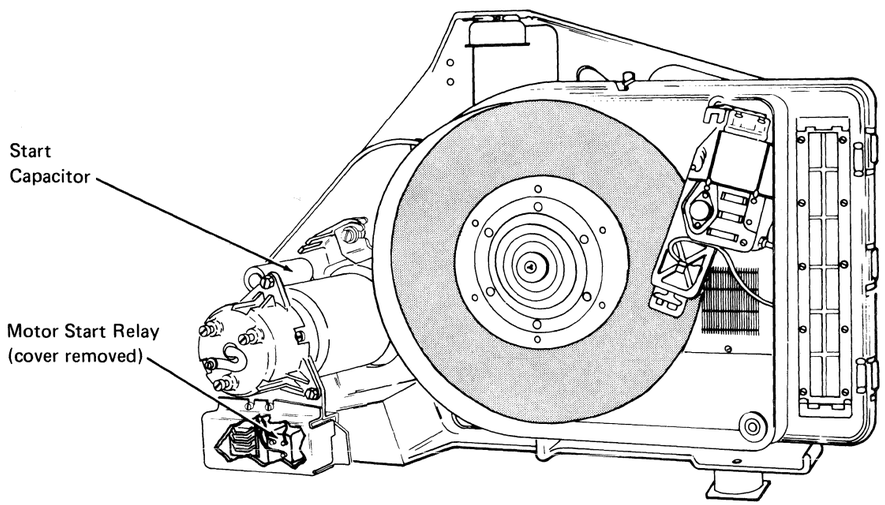
To limit the time that the servo head and the data heads touch the disk as it turns, the drive motor quickly starts the disk and the motor brake quickly stops the disk.

The brake is de-activated when 24 Vdc is present on the brake coil. The brake is activated by a spring when the machine power is off. There are two motor styles; the new style motor has a start capacitor on the top, a motor start relay on the bottom, and is smaller than the old style motor.

The motor has a manual thermal reset switch. A motor tension spring puts tension on the disk drive motor, which keeps tension on the drive belt. The motor antistatic brush is located on the brake assembly.



Front View (old style motor)



Front View (new style motor)

Write Safety

Data Unsafe Conditions

Circuits protect data from being destroyed during other than normal conditions. The data unsafe conditions that can occur are:

- Write selected and no write current.
- Write current source on but write not selected.
- Write selected and more than one head selected.
- Write selected and off track indicated.
- Write selected and disk not synchronized with attachment.
- Disk speed not correct.
- Card interlock circuit open, which indicates a loose or missing circuit card or cable.

When any of the data unsafe conditions occur, the 'write current' line is turned off and both the 'disk ready' and 'select head' lines are de-activated. The 'data unsafe' line signals the attachment of the condition. A reset line resets the 'data unsafe' line and a recalibrate-to-home operation sets the file 'ready' latch on.

File Ready

The disk drive becomes not ready for either of the following reasons:

- An electrical failure in the motor brake
- A data unsafe condition

Disk Speed

If the disk speed falls below 1,100 revolutions per minute, the disk drive becomes not ready and the actuator retracts.

Power On

During power on, the actuator is held against the inner stop until the disk is up to speed. This ensures that:

- The disk and control circuits can synchronize.
- The servo head and the data heads are off the disk before they move out of the landing zone.

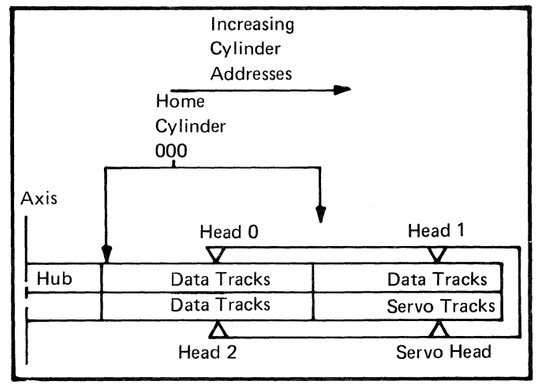
After a 32-second time-out, the actuator seeks to home (cylinder 0) and ready is indicated in the attachment.

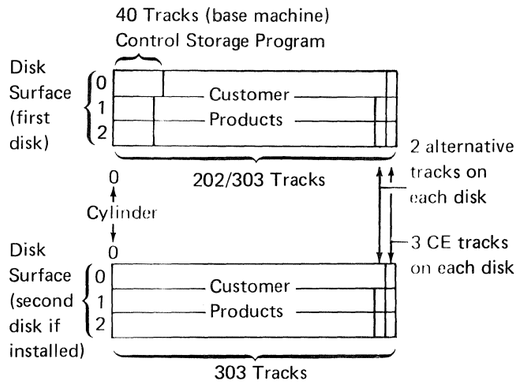
Disk Format

Data Tracks

The disk has cylinders, tracks, and sectors. A cylinder is the area that passes under the three data heads in one revolution, and a track is the area that passes under a single data head in one revolution. Each track is divided into 60 sectors. The data stored in one sector is a record. Each record contains 256 bytes. Therefore, there are 15,360 bytes per track and 46,080 bytes per cylinder. Information about the 62EH disk surface is shown in the following charts:

Number of disk drives installed	1		2
Disk capacity in megabytes	8.6	13.2	27.1
Number of tracks	606	909	1818
Number of cylinders	202	303	606
Data heads	3		6
Bytes per sector (record)	256		
Sectors (records) per track	60		

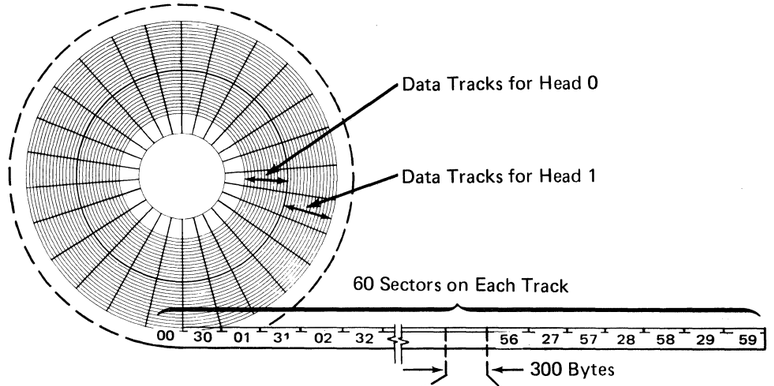




Sector Format

Each record on the disk has an identification address that contains cylinder, head, and sector numbers. This address (part of the identification field) is recorded at the actual physical location of the record on the disk. If the record area is damaged, the address area will contain the address of an alternative sector.

Sector 06		Sector 36		Sector 07		Sector 37	
ID	Data	ID	Data	ID	Data	ID	Data
Recovery Time		Rd	Write	Recovery Time		Rd	Write



Because the write operation may continue from one head to another, the sector numbers are moved by two from the preceding head.

Hd0	59	Index	0	30	01	31	02	32
Hd1	58	Index	29	59	0	30	01	31
Hd2	57	Index	28	58	29	59	0	30

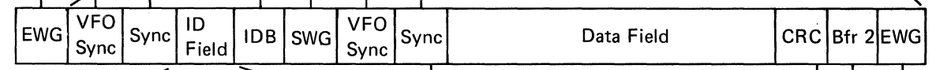
VFO sync is 12 bytes of hex FF that synchronize the read clock with data bits from the disk.

This 2-byte end write gap is written as part of the VFO sync area, giving a total of 14 bytes of hex FF.

Identification buffer is 1 byte (hex FF) of space after reading the ID field CRC before changing the circuits from read to write.

Start write gap is 2 bytes of hex FF that give time to change the circuits from read to write.

VFO sync is 12 bytes of hex FF.

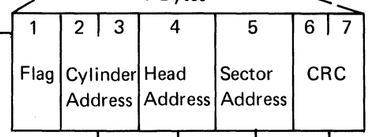


Sector or Index

256 bytes

Sector or Index

7 Bytes



Note: If a sector defect occurs within the ID region (VFO sync through the ID field CRC), this VFO sync is extended 64 bytes (14 plus 64 equals 78 bytes).

The ID field is 7 bytes as described below.

The flag is 1 byte:

Bits	Meaning	
0-4	Must compare to control field	
5	Data field may contain bad data. Used only in an alternative sector identification field. Must compare to the control field.	
6-7	00	Good primary sector
	01	Good alternative sector
	10	Defective primary sector
	11	Defective alternative sector

The cylinder address is 2 bytes.

Disk Capacity	Cylinder Address
8.6 megabytes	0 to 201
13.2 megabytes	0 to 302

The head address is 1 byte (hex 00 for head 0, hex 01 for head 1, or hex 10 for head 2).

The sector address is 1 byte (0 to 59).

Cyclic redundancy check is 2 bytes of check characters that verify that the data was read correctly from the ID field.

Sync is 1 byte (hex 0E) that synchronizes the bit ring. The bit ring gates the bits read from the disk into the serializer-deserializer to be formed into bytes.

Cyclic redundancy check is 2 bytes of check characters that verify that the data was read correctly from the data field.

Buffer 2 is 4 bytes (hex FF) of space after writing the data field CRC before changing the circuits back to read.

End write gap is 2 bytes of hex FF that give time to switch the circuits from write to read. End write gap is part of the VFO sync field for the next sector.

Disk Addressing

Sequential Sector Addressing

The type of addressing used by the main storage program to identify disk data areas is sequential sector addressing. The sequential sector number is a binary number, starting at hexadecimal 000001 (cylinder 0, head 0, sector 0), and is increased by 1 for each sector processed. Sequential sector addressing extends through the last data sector on the first disk and onto the second disk if two disks are installed. (See the *Data Areas Handbook* for more information on disk addressing.)

Actual Sector Addressing

This figure shows how the 62EH disk sectors are assigned. Although there are three separate read and write surfaces, this figure shows the three surfaces as they are to each other in sector address numbering from the index.

Each sector is 300 bytes long. The main fields of a sector are the identification field and the data field.

The time needed to change from a write operation to a read operation is too long to permit writing consecutive sectors because the read amplifiers need time to become operational. A data operation must be started before sensing the index pulse or sector pulse of the sector on which the operation is to be performed. The index pulse or sector pulse starts the operation. Because one data operation cannot be ended and the next one started before the next sector pulse, the sector addresses are alternated on the surface of the disk; that is, between sector 0 and sector 1 is sector 30 (hex 1E). Between sector 1 and sector 2 is sector 31 (hex 1F). This numbering sequence is continued around the surface until sector 59 (hex 3B).

With this numbering sequence, there is time to start a data operation on alternate physical sectors, so that every sector address on the surface can be read (or written) consecutively, in two revolutions of the disk, with the exception that the index pulse or a sector pulse must be skipped between the operation on sector 29 (hex 1D) and the operation on sector 30 (hex 1E). This occurs because sector 59 (hex 3B) and sector 0 are next to each other, and are also between sector 29 (hex 1D) and sector 30 (hex 1E).

Looking from the index in a clockwise direction, you can see that heads 1 and 2 are offset. On the surface for head 1, the sector addresses are offset two physical sectors from the sectors for head 0. On head 2, the sector addresses are offset by four physical sector addresses from the head 0 sector addresses. This means that the sector addresses for head 1 are as follows, starting at the index: sector 29 (hex 1D), sector 59 (hex 3B), sector 0 (hex 00), ... sector 57 (hex 39), sector 28 (hex 1C), sector 58 (hex 3A). The sector addresses on head 2 are as follows, starting at the index: sector 28 (hex 1C), sector 58 (hex 3A), sector 29 (hex 1D), ... sector 56 (hex 38), sector 27 (hex 1B), sector 57 (hex 39).

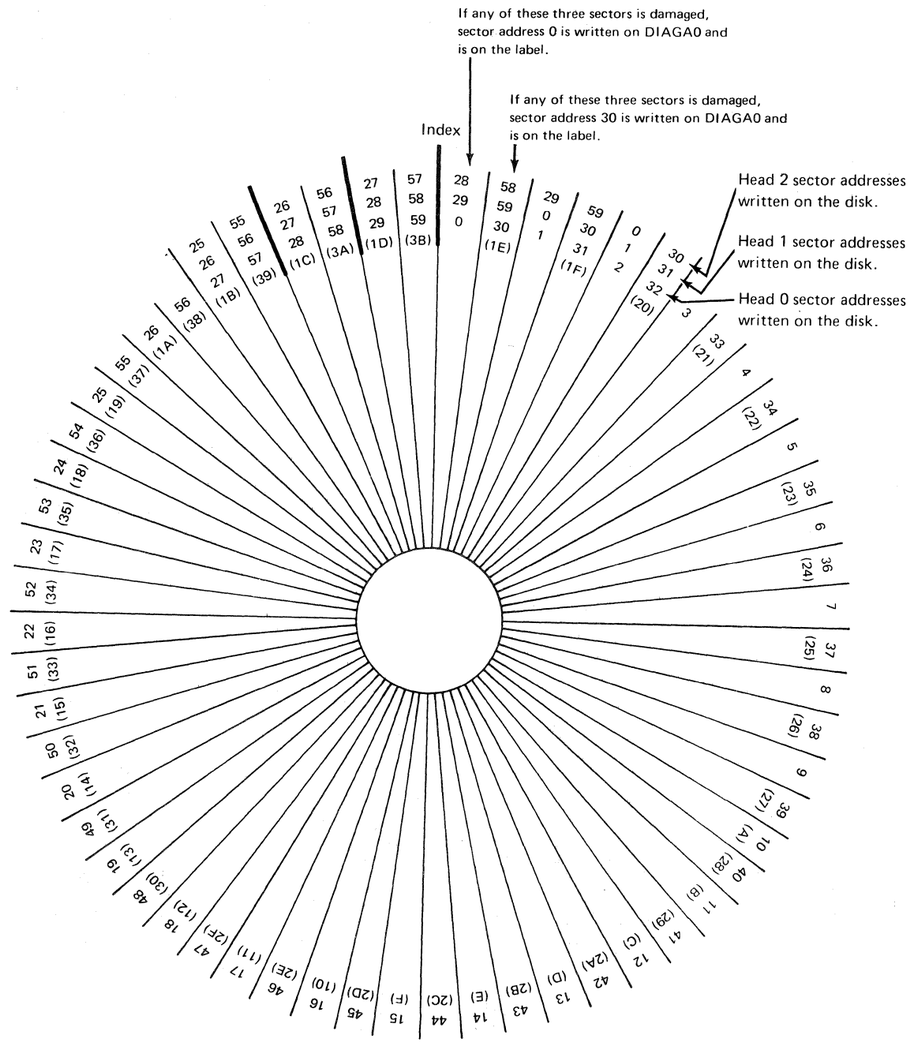
The disk file used in System/34 is the same type of disk file that is used in System/32. As the disk drives are assembled, they are initialized for use as System/32 files. That is, sector addresses on all heads are in the same position on the surface relative to the index (the same as head 0 sectors on System/34).

After the disk drives are assembled, they are tested for damaged sectors. The damaged sectors have flag bits set on in the identification field on the disk and are recorded on labels that are attached to the disk drive cover.

Because the disk is initialized for use on System/32, it must be initialized again by the System/34 initialization program. All sectors flagged as damaged must be assigned to alternative sectors, or be flagged as damaged alternative sectors so they will not be used for data.

The damaged sector identification fields and the disk drive sequence numbers are recorded on the DIAGA0 diskette for use by the program on later initializations. The same damaged sector identification fields appear on the label on the disk drive cover.

During the initialization process, a list of the sector identification fields on the alternative sector tracks is given to the operator. The sector identification fields of the damaged sectors replace the sector identification fields found in sectors on the alternative sector tracks. Any sector identification field recorded on the label on the disk drive cover is shown in this list. However, the damaged sectors for heads 1 and 2 have a different sector address than the one shown on the label(s) and written on the DIAGA0 diskette. Damaged sectors for tracks using head 1, other than sector 0 and sector 30 (hex 1E), are lowered by a count of 1. Sector 0 becomes sector 29 (hex 1E) and sector 30 (hex 1E) becomes sector 59 (hex 3B). Damaged sectors from tracks using head 2, other than sectors 0, 1, 30 (hex 1E), and 31 (hex 1F), are lowered by a count of 2. In this case, sector 0 becomes sector 28 (hex 1C), sector 1 becomes sector 29 (hex 1D), sector 30 (hex 1E) becomes sector 58 (hex 3A), and sector 31 (hex 1F) becomes sector 59 (hex 3B).



Servo Tracks

The servo tracks are electrical patterns that are written on the disk at the factory. The servo tracks include clock pulses, missing clock pulses, and position pulses in a specific sequence. The 2.2-microsecond clock pulses generate the 140-nanosecond write clock pulses in the attachment. The position pulses are used by the servo head to keep the data heads over a specified track.

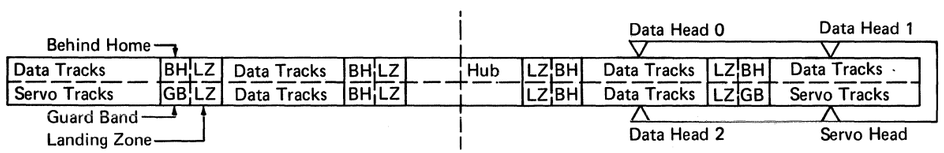
Specific combinations of clock pulses and missing clock pulses generate either the index pulses, the sector pulses, or the sector midpoint pulses. The sector midpoint pulses are used during seek operations to indicate that the actuator is not in the guard band area.

Landing Zone

The servo head and the data heads are retracted to the landing zone when the disk speed is less than 1,100 revolutions per minute. This prevents the heads from destroying data. The landing zone is indicated by missing sector pulses, index pulses, or sector midpoint pulses, and is about 40 tracks wide.

Guard Band

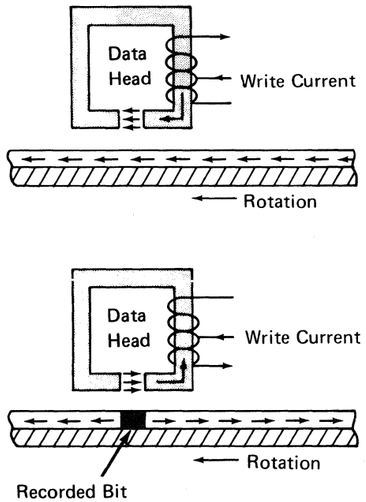
The guard band is a servo track area that contains clock pulses and position pulses but does not contain sector pulses, index pulses, or sector midpoint pulses. When the servo head is in the guard band position, the data heads are behind home.



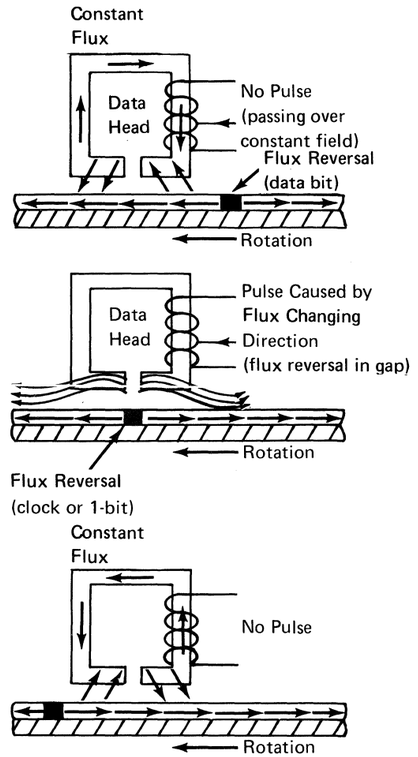
Data Recording

Read and Write Data

During a write operation, data is recorded by reversing the direction of the current in the coil, which reverses the direction of the magnetic flux in the data head gap. When the flux in the data head gap reverses, there is a magnetic change of direction on the disk surface. Each change of direction on the disk represents a recorded 0-bit or 1-bit.

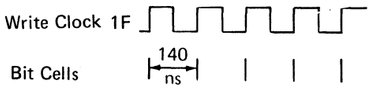


During a read operation, when the recorded disk surface is in one magnetic direction (no data bit), constant flux flows through the data head and no output pulse is generated. When a data bit, recorded on the disk surface, passes the data head, the magnetic change from the data bit causes a flux change in the data head and an output pulse is generated.



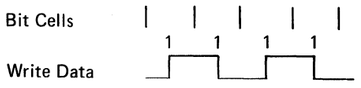
Only data bits are written on the disk drive data tracks. For write operations, the attachment uses clock pulses read from the servo tracks to generate the write clock. On read operations, the read clock is generated from the variable frequency oscillator sync fields and from the data being read.

The time during which a data bit may be written is known as a bit cell. A bit cell is 140 nanoseconds long and is generated by the 'write clock 1F' line.



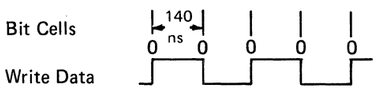
Writing 1-Bits

One-bits are always written in the center of a bit cell.

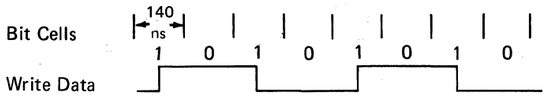


Writing 0-Bits

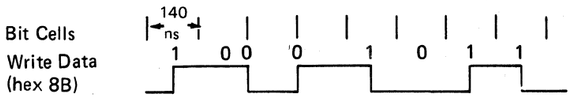
With one exception, 0-bits are always written at the start of a bit cell.



The exception is when a 0-bit immediately follows a 1-bit. In this case, no bit is written and the 0-bit is represented by no magnetic change of direction during its bit cell time.



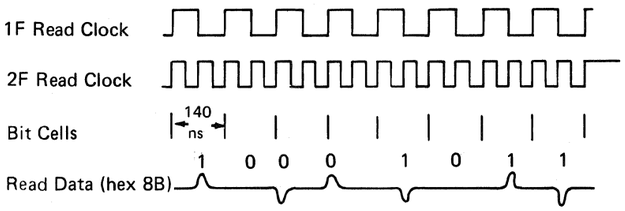
By writing hex 8B, both methods of writing 0-bits and the method of writing 1-bits can be shown.



The data written is transmitted on the data transmission line to the write circuits installed on the disk drive. For each change on the data transmission line, a 0-bit or a 1-bit is written on disk. These changes cause the current in the data head to be switched, which results in a polarity change on the disk track.

Reading Data Bits

When data is read from the disk drive, the read clock is generated by the variable frequency oscillator. This oscillator is synchronized to the read data by the variable frequency oscillator sync field as it is read from the disk. The phase lock loop then keeps the oscillator in sync with the read data (1's and 0's) so it can be decoded.



Actuator Movement

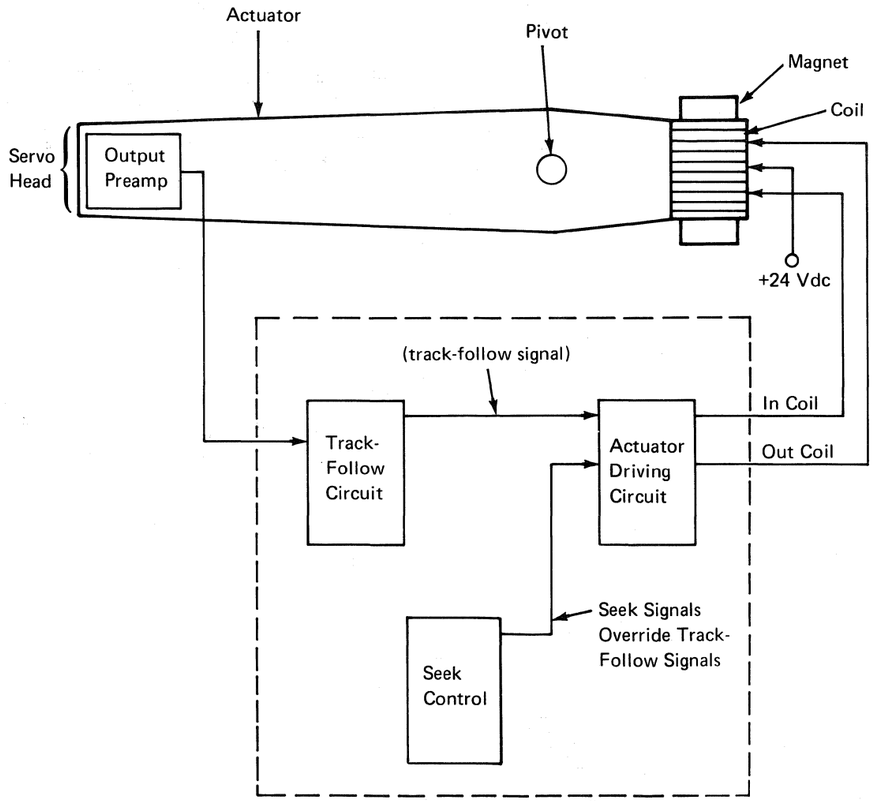
Seek

During the first part of a long seek operation, the seek controls cause the actuator to leave track-follow mode and increase the actuator speed until it reaches a maximum speed. During the last part of a long seek operation, the seek controls slow the actuator to a stop at the desired track. During short seeks, the actuator does not reach maximum speed. The actuator speed is increased for the first part of the seek and decreased for the last part of the seek. For more information, see *Seek Operation* later in this section.

Recalibrate

A recalibrate operation is executed by activating the actuator driving circuits. The actuator driving circuits move the heads across the tracks into the guard band area and then out to home (cylinder 0). The actuator moves at slow speed during the recalibrate operation.

A recalibrate operation is started during a normal power-on sequence and during error correction.



Circuits on A-A2 (I/O board) for disk drive A, on A-A3 for disk drive B.

Servo Track Follow

Servo Head Aligned Correctly

When the servo head is aligned correctly on the servo track, the servo head follows the area between position pulses P1 and P2. The C-patterns are common to all servo tracks and are used to generate the write clock pulses, sector pulses, and index pulses. Position pulses ensure correct alignment of the servo head over the servo track. When there is a seek to an even track, P1 is the inside pulse and P2 is the outside pulse. For a seek to an odd track, P1 is the outside pulse and P2 is the inside pulse. Note that the C-patterns are valid during seeks and are used during seeks.

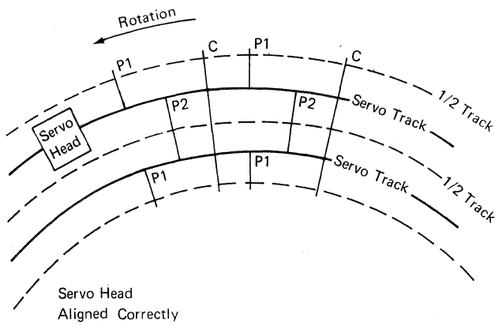
Servo Head Offset

The servo control follows the tracks by ensuring that the position pulses are received at equal amplitudes. This positions the servo head between two servo tracks.

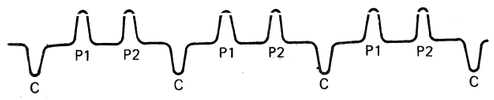
If the servo head moves off track, one position pulse is received at a low amplitude and the other position pulse is received at a high amplitude.

The servo control drives the servo head in the direction that increases the amplitude of the low amplitude position pulses (P1 and P2). The direction and degree of movement of the heads, to adjust for the error, is determined by the track being odd or even and the difference between the P1 and P2 pulses.

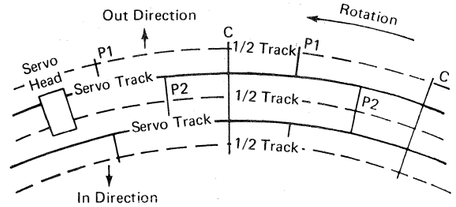
C = Clock Pulse
P1 = Position Pulse 1
P2 = Position Pulse 2



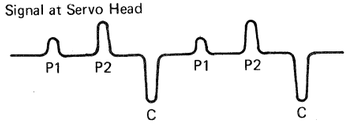
Signal at Servo Head When Aligned Correctly



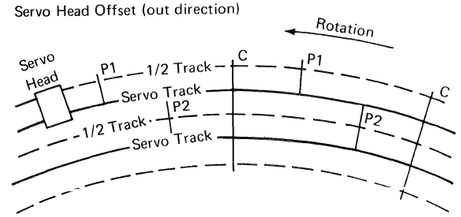
Servo Head Offset (in direction)



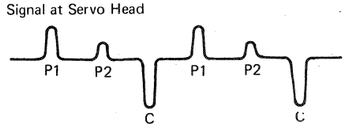
Signal at Servo Head

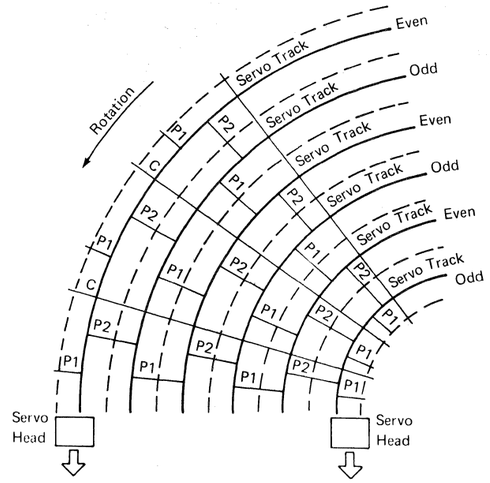


Servo Head Offset (out direction)

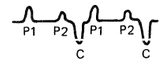


Signal at Servo Head



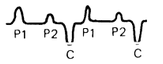


Even track, servo head offset. Servo head signal.



P1 ≠ P2 with an even track destination. If P2 > P1, the heads will move out. If P2 < P1, the heads will move in.

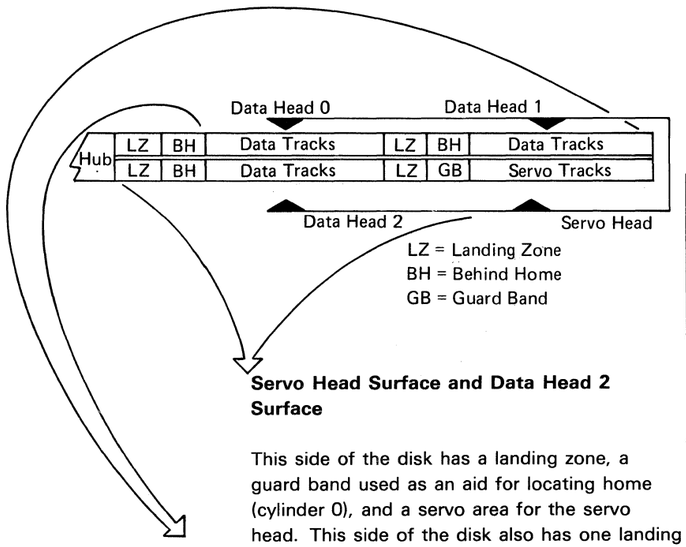
Odd track, servo head offset. Servo head signal.



P1 ≠ P2 with an odd track destination. If P2 > P1, the heads will move in. If P2 < P1, the heads will move out.

Head Alignment and Disk Description

One side of the disk is a data surface only (data heads 0 and 1). The other side is the servo surface (for the servo head) and the data surface for data head 2.

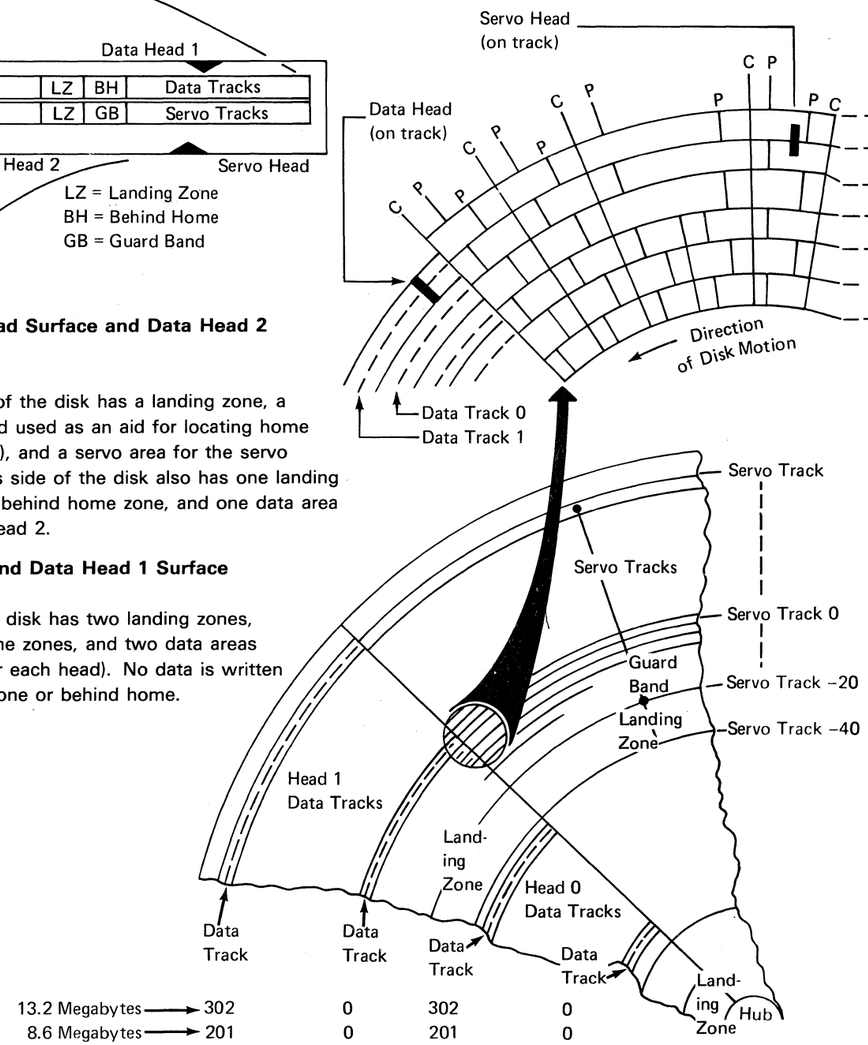


Servo Head Surface and Data Head 2 Surface

This side of the disk has a landing zone, a guard band used as an aid for locating home (cylinder 0), and a servo area for the servo head. This side of the disk also has one landing zone, one behind home zone, and one data area for data head 2.

Data Head 0 and Data Head 1 Surface

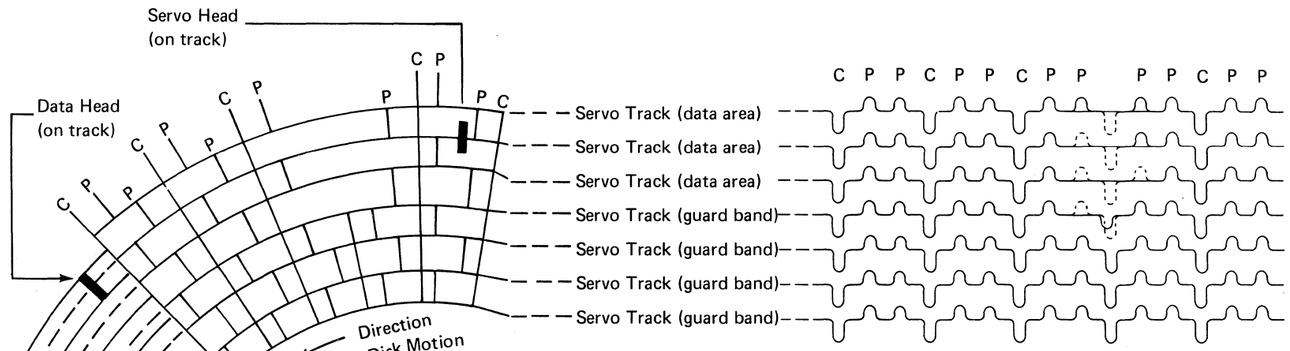
This side of the disk has two landing zones, two behind home zones, and two data areas (one of each for each head). No data is written in the landing zone or behind home.



Missing Clock Pulse and Position Pulses

Patterns of missing clock pulses decode into index pulses, sector pulses, or sector midpoint pulses, which activate the data area pulse.

P = Position Pulse
C = Clock Pulse



Guard Band

The guard band is a normal track area that has no index pulse, sector pulse, or sector midpoint pulse. The guard band is indicated at the servo track that has no missing clock pulses, which in turn indicates no data area pulses. Missing data area pulses let a 135-microsecond singleshot time-out, which indicates the guard band.

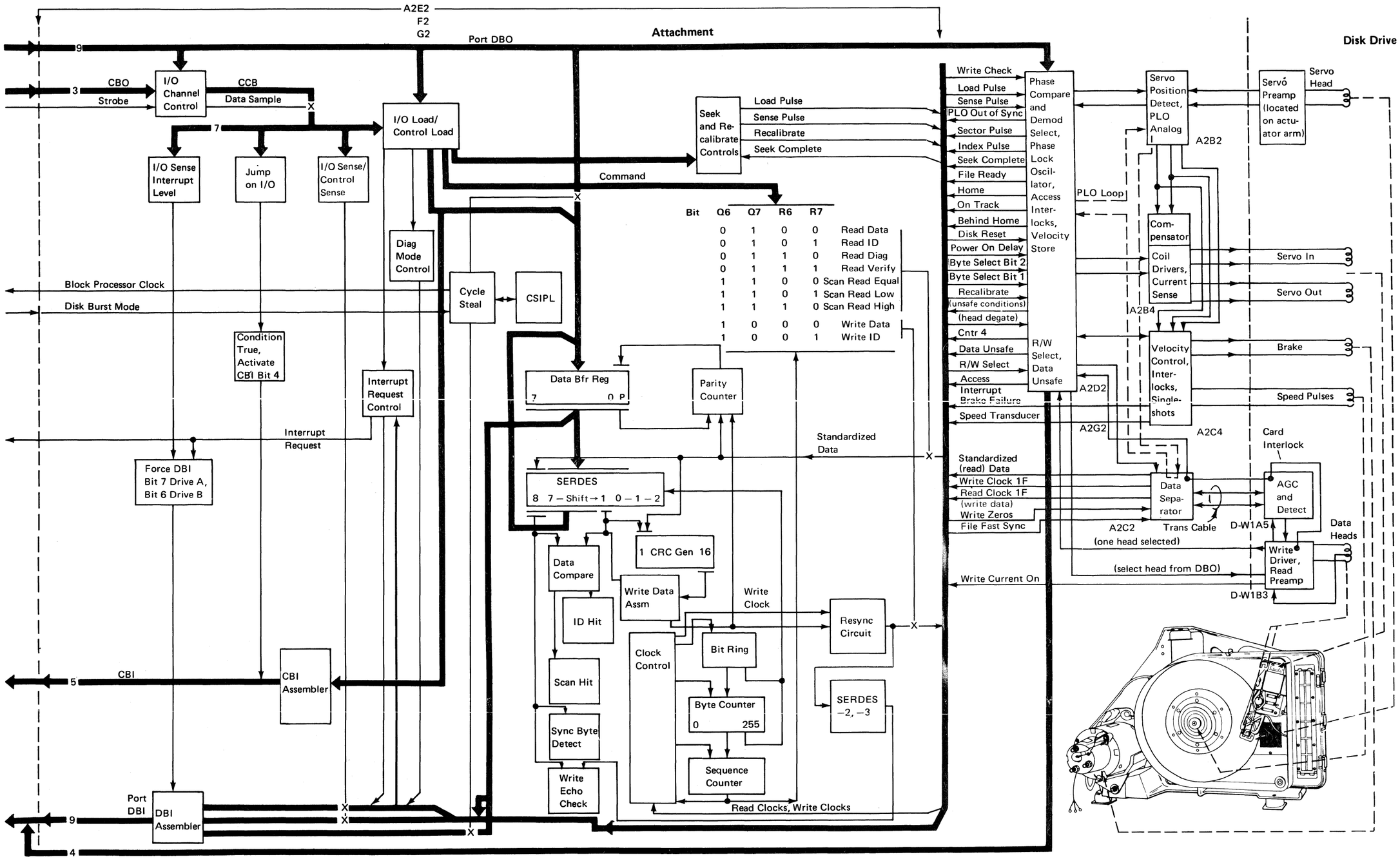
The guard band indicates that the data heads are behind home.

Behind Home

Behind home is the condition when the data heads are behind cylinder 0.

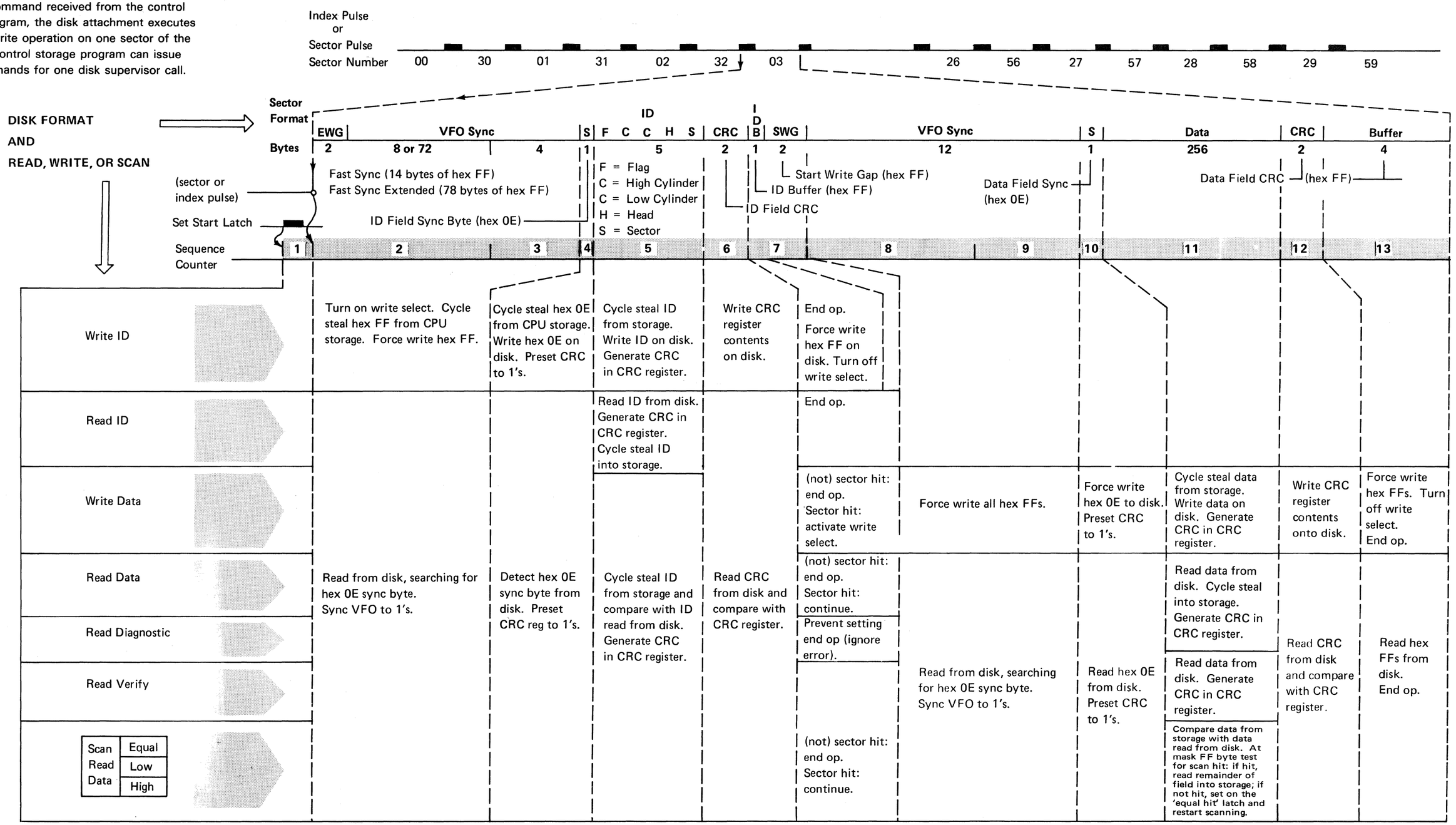
If the data heads attempt to seek to a cylinder that is farther in than cylinder 0, the seek operation is ended. When the heads stop, the actuator seeks to home (cylinder 0).

DATA FLOW


A2E2
F2
G2
Port DBO
Attachment
Disk Drive
9
3
CBO
Strobe
I/O Channel Control
CCB
Data Sample
X
7
I/O Load/ Control Load
I/O Sense Interrupt Level
Jump on I/O
I/O Sense/ Control Sense
Command
Seek and Re-calibrate Controls
Load Pulse
Sense Pulse
Recalibrate
Seek Complete
Bit Q6 Q7 R6 R7
0 1 0 0 Read Data
0 1 0 1 Read ID
0 1 1 0 Read Diag
0 1 1 1 Read Verify
1 1 0 0 Scan Read Equal
1 1 0 1 Scan Read Low
1 1 1 0 Scan Read High
1 0 0 0 Write Data
1 0 0 1 Write ID
Diag Mode Control
Block Processor Clock
Disk Burst Mode
Cycle Steal
CSIPL
Condition True, Activate CBI Bit 4
Interrupt Request Control
Data Bfr Reg
7 0 P
Parity Counter
Interrupt Request
Force DBI Bit 7 Drive A, Bit 6 Drive B
Standardized Data
SERDES
8 7 – Shift → 1 0 – 1 – 2
1 CRC Gen 16
Data Compare
ID Hit
Write Data Assm
Write Clock
Resync Circuit
Clock Control
Bit Ring
Scan Hit
Byte Counter
0 255
SERDES –2, –3
Sync Byte Detect
Sequence Counter
Write Echo Check
Read Clocks, Write Clocks
5
CBI
CBI Assembler
Port DBI
9
DBI Assembler
4
Write Check
Load Pulse
Sense Pulse
PLO Out of Sync
Sector Pulse
Index Pulse
Seek Complete
File Ready
Home
On Track
Behind Home
Disk Reset
Power On Delay
Byte Select Bit 2
Byte Select Bit 1
Recalibrate (unsafe conditions)
(head degate)
Cntr 4
Data Unsafe
R/W Select
Access Interrupt
Brake Failure
Speed Transducer
Phase Compare and Demod Select, Phase Lock Oscil-lator, Access Inter-locks, Velocity Store
R/W Select, Data Unsafe
A2D2
A2G2
Standardized (read) Data
Write Clock 1F
Read Clock 1F
(write data)
Write Zeros
File Fast Sync
Write Current On
Servo Position Detect, PLO Analog
A2B2
PLO Loop
Servo Preamp (located on actu-ator arm)
Servo Head
Com-pensator
Coil Drivers, Current Sense
A2B4
Servo In
Servo Out
Velocity Control, Inter-locks, Single-shots
Brake
Speed Pulses
A2C4
Card Interlock
Data Sepa-rator
A2C2
Trans Cable
AGC and Detect
D-W1A5
Data Heads
(one head selected)
(select head from DBO)
Write Driver, Read Preamp
D-W1B3

OPERATIONS

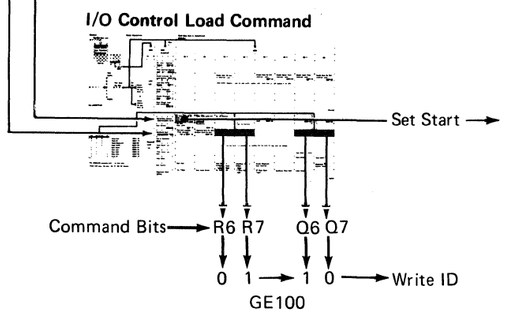
For each command received from the control storage program, the disk attachment executes a read or write operation on one sector of the disk. The control storage program can issue many commands for one disk supervisor call.

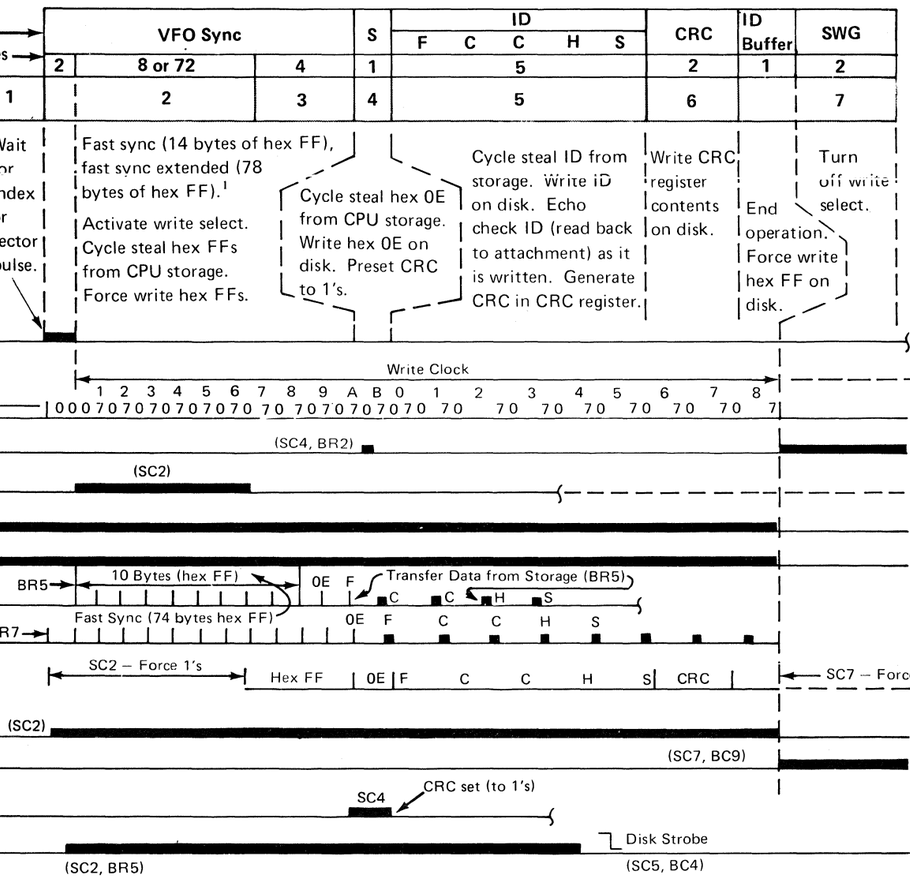


Write Identification

The primary use of the write identification operation is to write a new identification field when a damaged sector is found. When a permanent error is found in a sector, the sector's identification field must be written again to indicate which alternative track the data has been written on and to flag that sector as being damaged.

- A control load command issues write ID.
- A control load command issues set start, which gates the sequence counter and sets the block processor clock. The next sector or index pulse starts the sequence counter, and write ID is executed.
- The ID field is transferred from the control processor to the attachment by cycle steal. For more information, see *Cycle Steal* later in this section. Also see *Burst Cycle Steal Mode* under *Operations* in the *Channel* section of this manual.





[1] If a sector defect occurs within the ID region (VFO sync through CRC), the VFO fast sync is extended 64 bytes.

Read Identification

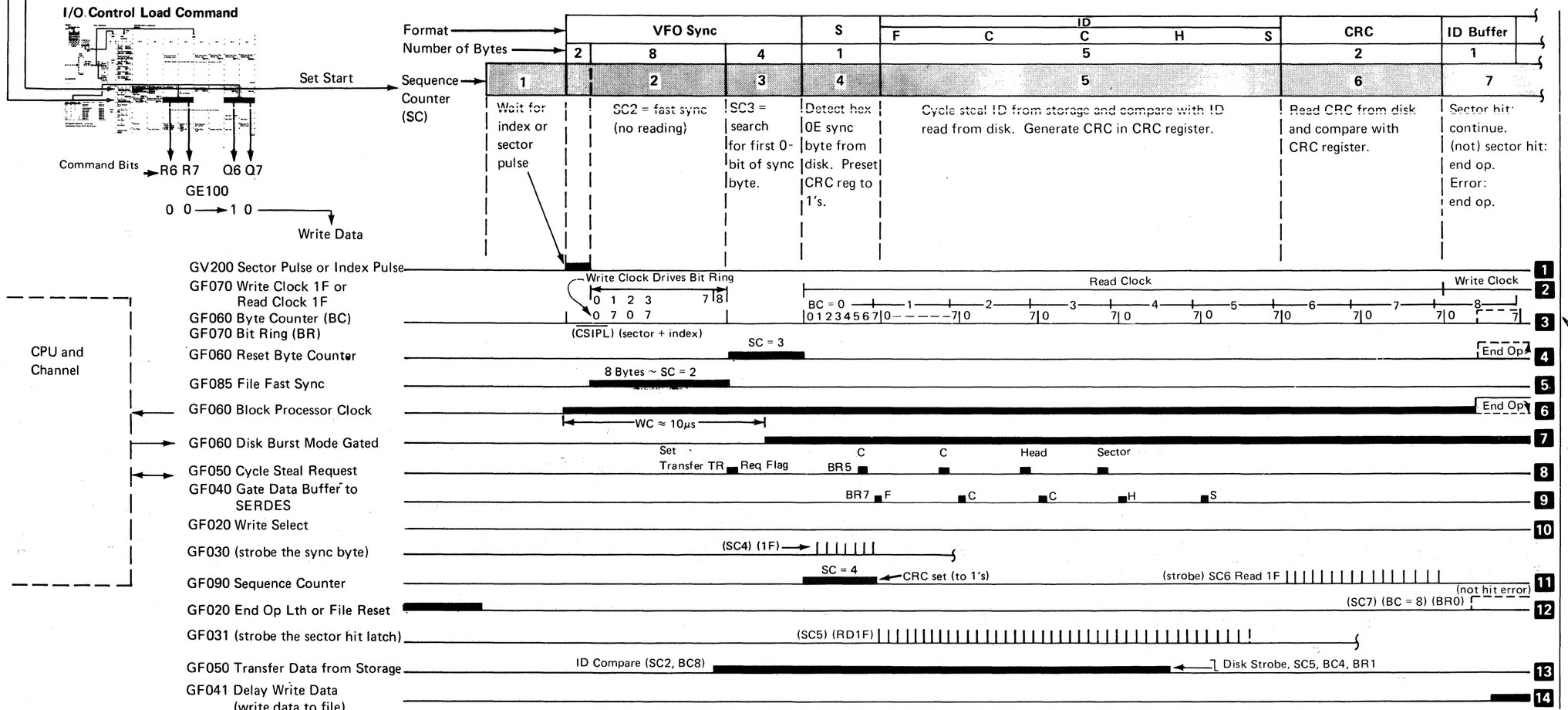
The read identification operation reads the identification field from a sector of the disk and sends the field to the control processor. There, the field is used during error correction to identify damaged sectors and to locate alternative sectors.

- A control load command issues read ID.
- A control load command issues set start, which gates the sequence counter. The next sector or index pulse starts the sequence counter, sets the 'block processor clock' latch, and executes read ID.
- The ID field is transferred from the attachment to the control processor by cycle steal. For more information, see *Cycle Steal* later in this section. Also see *Burst Cycle Steal Mode* under *Operations* in the *Channel* section of this manual.

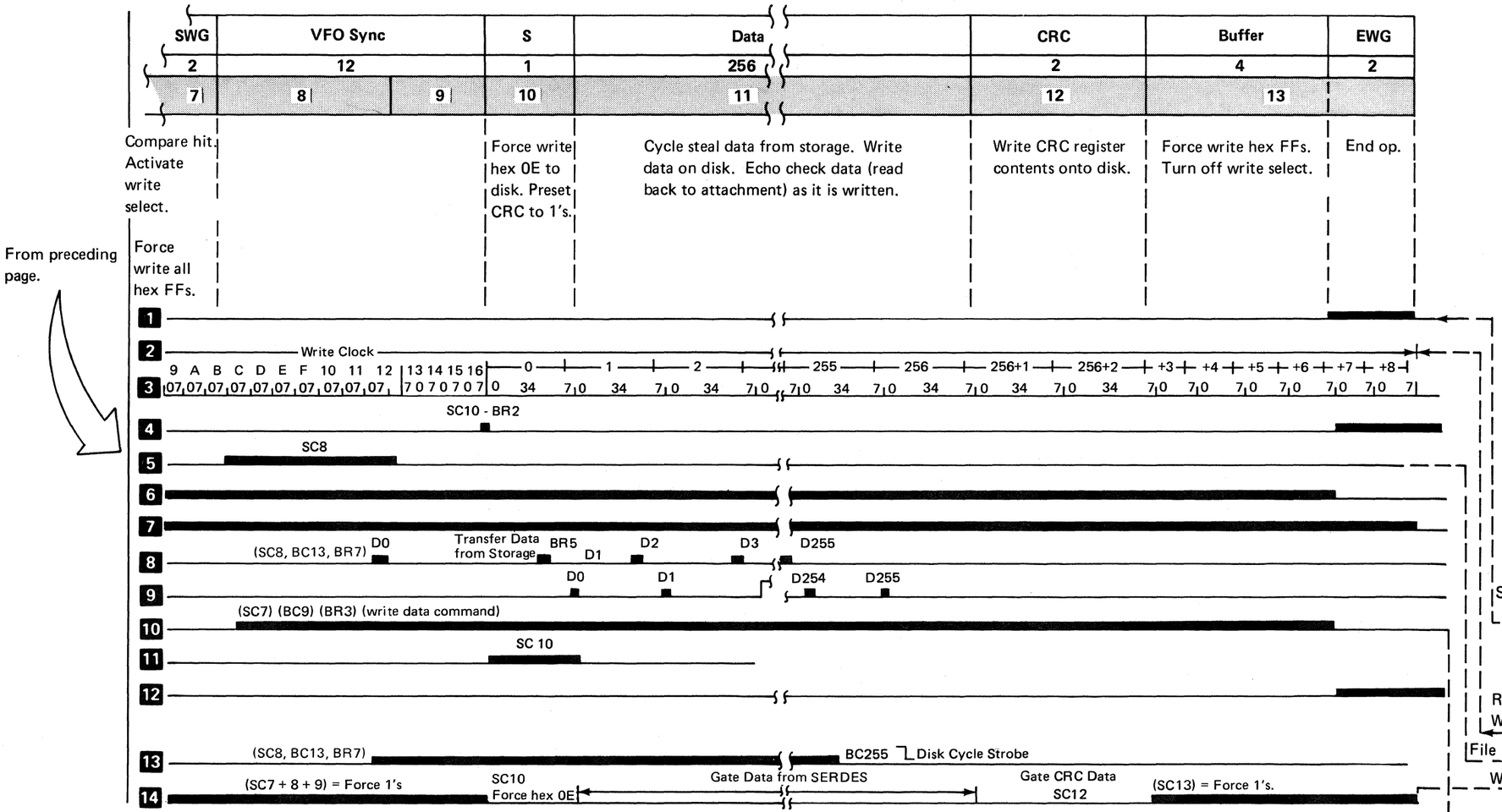
Write Data

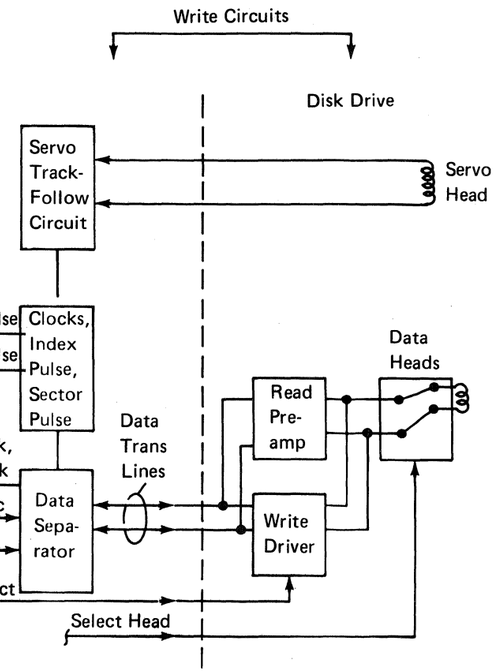
The write data operation sends 256 bytes of data from the control processor to the disk attachment, and the 256 bytes are written into the data field of a sector on the disk.

- A control load command issues write data.
- A control load command issues set start, which gates the sequence counter. The next sector or index pulse starts the sequence counter, sets the 'block processor clock' latch, and executes write data.
- The ID field and the data field are transferred from the control processor to the attachment by cycle steal. For more information, see *Cycle Steal* later in this section. Also see *Burst Cycle Steal Mode* under *Operations* in the *Channel* section of this manual.



Continued on next page

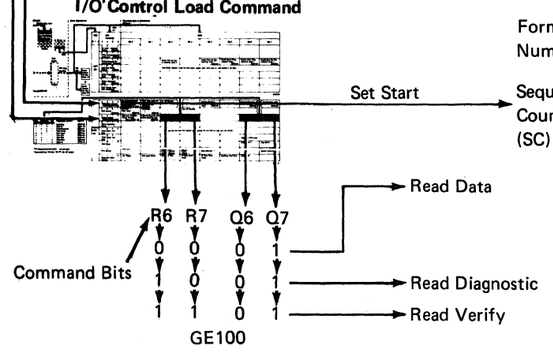

SWG
VFO Sync
S
Data
CRC
Buffer
EWG
2
12
1
256
2
4
2
7
8
9
10
11
12
13
Compare hit. Activate write select.
Force write hex 0E to disk. Preset CRC to 1's.
Cycle steal data from storage. Write data on disk. Echo check data (read back to attachment) as it is written.
Write CRC register contents onto disk.
Force write hex FFs. Turn off write select.
End op.
From preceding page.
Force write all hex FFs.
Write Clock
9 A B C D E F 10 11 12 13 14 15 16 0 1 2 255 256 256+1 256+2 +3 +4 +5 +6 +7 +8
SC10 - BR2
SC8
(SC8, BC13, BR7)
D0
Transfer Data from Storage
BR5
D1
D2
D3
D255
D254
(SC7) (BC9) (BR3) (write data command)
SC 10
BC255
Disk Cycle Strobe
(SC7 + 8 + 9) = Force 1's
SC10 Force hex 0E
Gate Data from SERDES
Gate CRC Data SC12
(SC13) = Force 1's.


Write Circuits
Disk Drive
Servo Track-Follow Circuit
Servo Head
Sector Pulse
Index Pulse
Clocks, Index Pulse, Sector Pulse
Data Heads
Read Pre-amp
Read Clock, Write Clock
Data Trans Lines
File Fast Sync
Write Data (zeros)
Data Sepa-rator
Write Driver
Read/Write Select
Select Head

Read Data

The read data operation reads 256 bytes of data from the data field of a sector on the disk and sends the 256 bytes of data through the attachment to the control processor.

- A control load command issues read data or read diagnostic or read verify.
- A control load command issues set start, which gates the sequence counter. The next sector or index pulse starts the sequence counter, sets the 'block processor clock' latch, and executes read data, read diagnostic, or read verify.
- The ID field and the data field are transferred from the attachment to the control processor by cycle steal. For more information, see *Cycle Steal* later in this section. Also see *Burst Cycle Steal Mode* under *Operations* in the *Channel* section of this manual.



Read Diagnostic

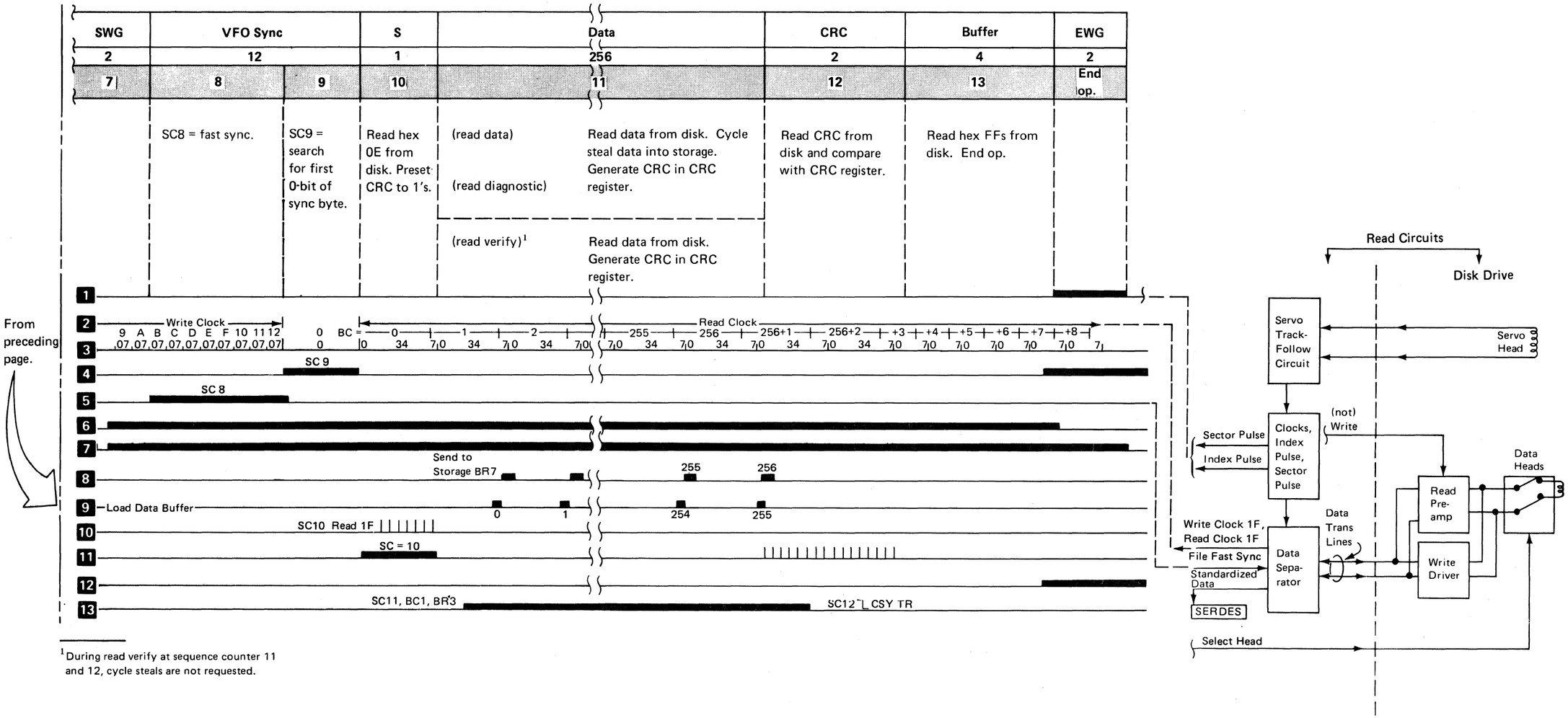
Normally, the data field of a record can be read only if a sector hit condition occurred during the identification search. The sector hit indicates that the desired record has been found.

However, if an identification field becomes damaged after the data has been written, it is possible that a sector hit may not occur during the identification search. If that is the case, the program can issue a read diagnostic operation. The read diagnostic operation is a normal read operation, but it does not end the operation if an error occurs during the identification compare. This lets the control processor recover data if the identification field becomes damaged. If an error occurs during the identification compare or if the identification does not compare, the 'sector hit' latch is not on at the end of the operation.

Read Verify

A read verify operation checks the contents of the data field after the field has been written. The read verify operation simulates read data in the attachment, but no data is sent to the control processor. As the record is read, the cyclic redundancy check character is generated to verify that the record can be read.

Continued on next page.



[1] During read verify at sequence counter 11 and 12, cycle steals are not requested.

Scan Read Data Equal

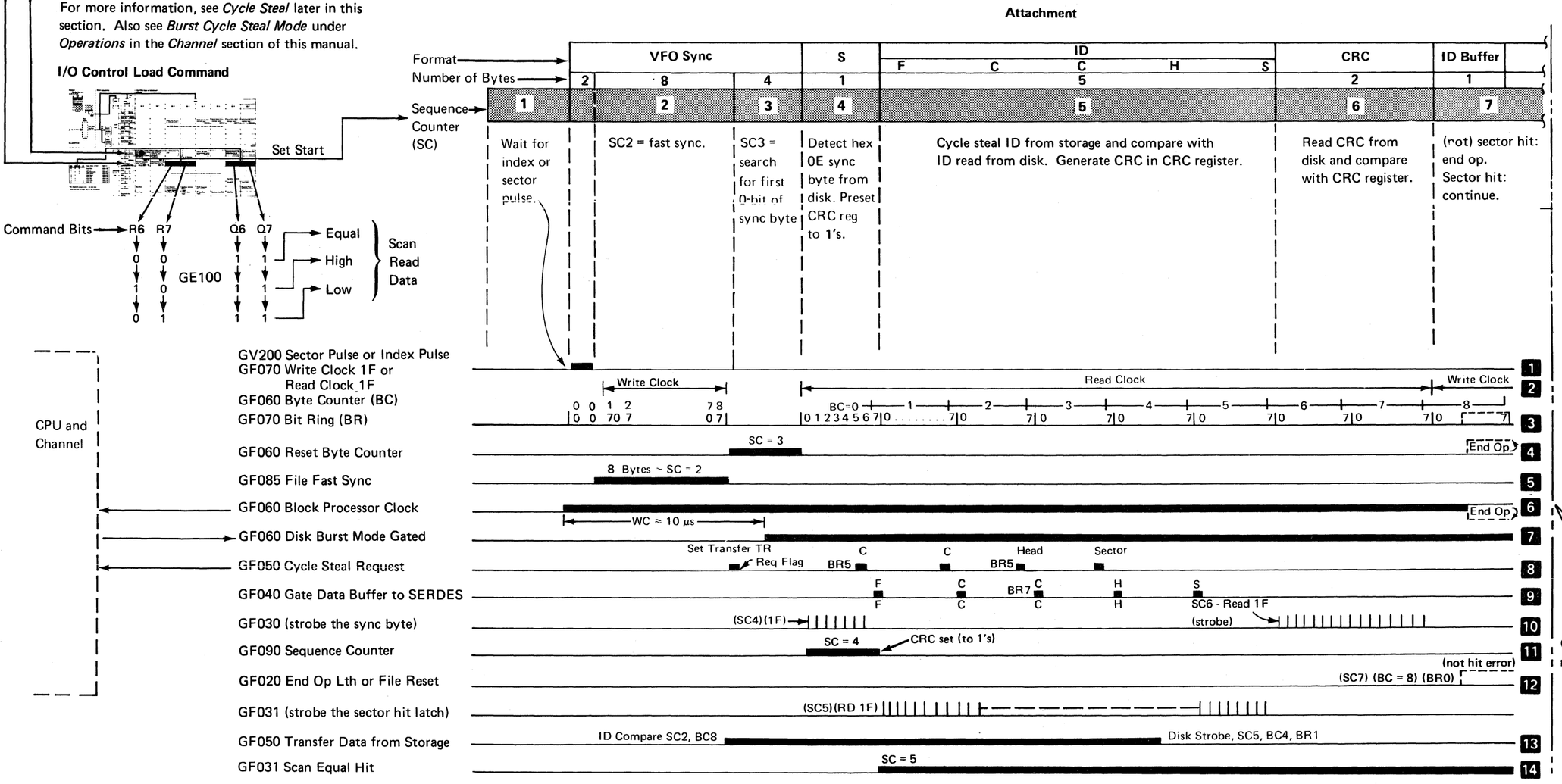
Scan Read Data Low or Equal

Scan Read Data High or Equal

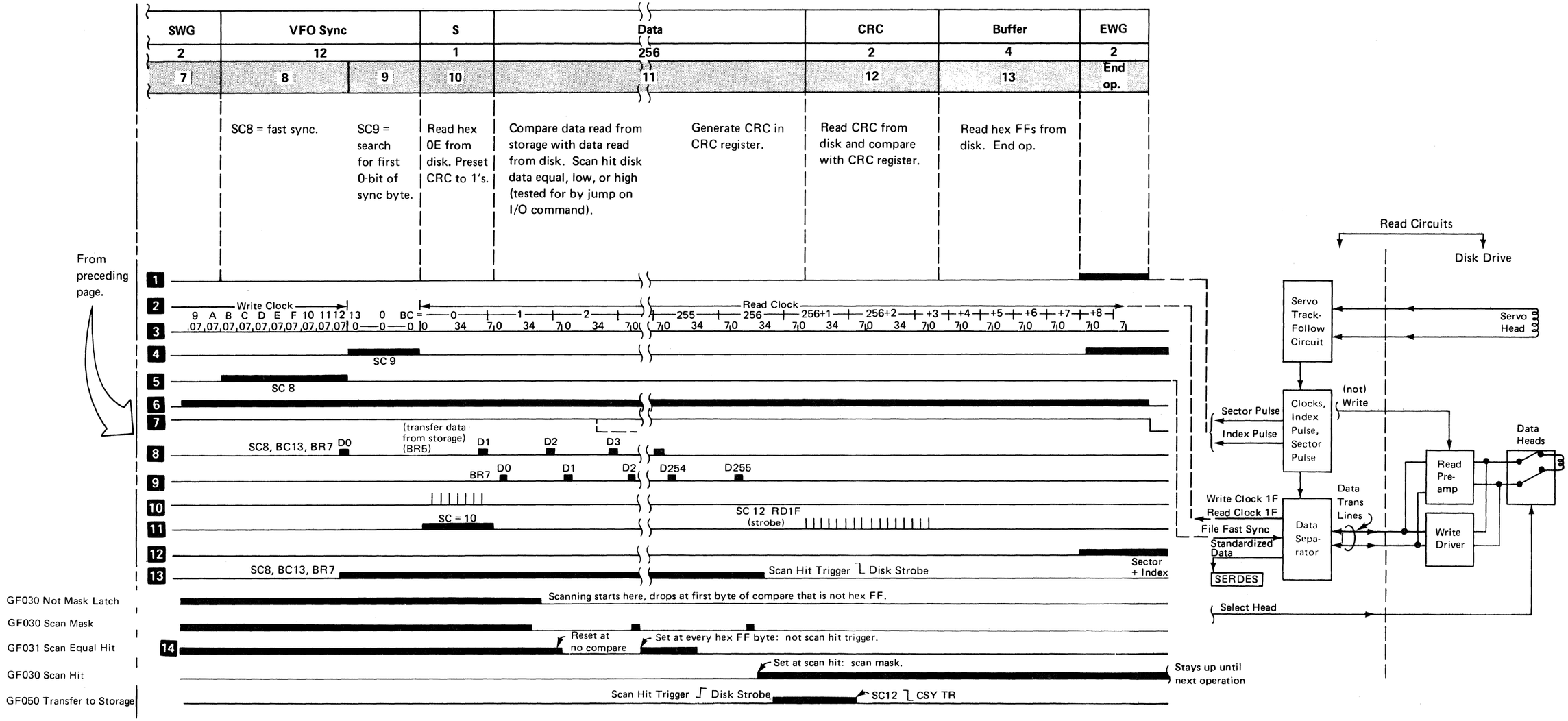
The control processor issues an I/O control load command specifying a scan read data equal, a scan read data low or equal, or a scan read data high or equal operation.

The control processor issues an I/O control load command specifying set start, which starts the sequence counter. Starting at the next sector pulse, the scan operation is executed. The contents of all or part of the data field on the disk are compared to a fixed field in the control processor. Following a hit decision, the data from the disk is read into main storage or control storage moved to the right by 2 bytes. The 2-byte delay is needed to change the direction of the data flow in the channel.

- CPU issues I/O control load, which specifies a scan data operation.
- CPU issues an I/O control load-set start. The next sector pulse starts the sequence counter, sets the 'block processor clock' latch, and executes the scan operation.
- The ID field and the data field are transferred from the control processor to the attachment by cycle steal. For more information, see *Cycle Steal* later in this section. Also see *Burst Cycle Steal Mode* under *Operations* in the *Channel* section of this manual.



Continued on next page.

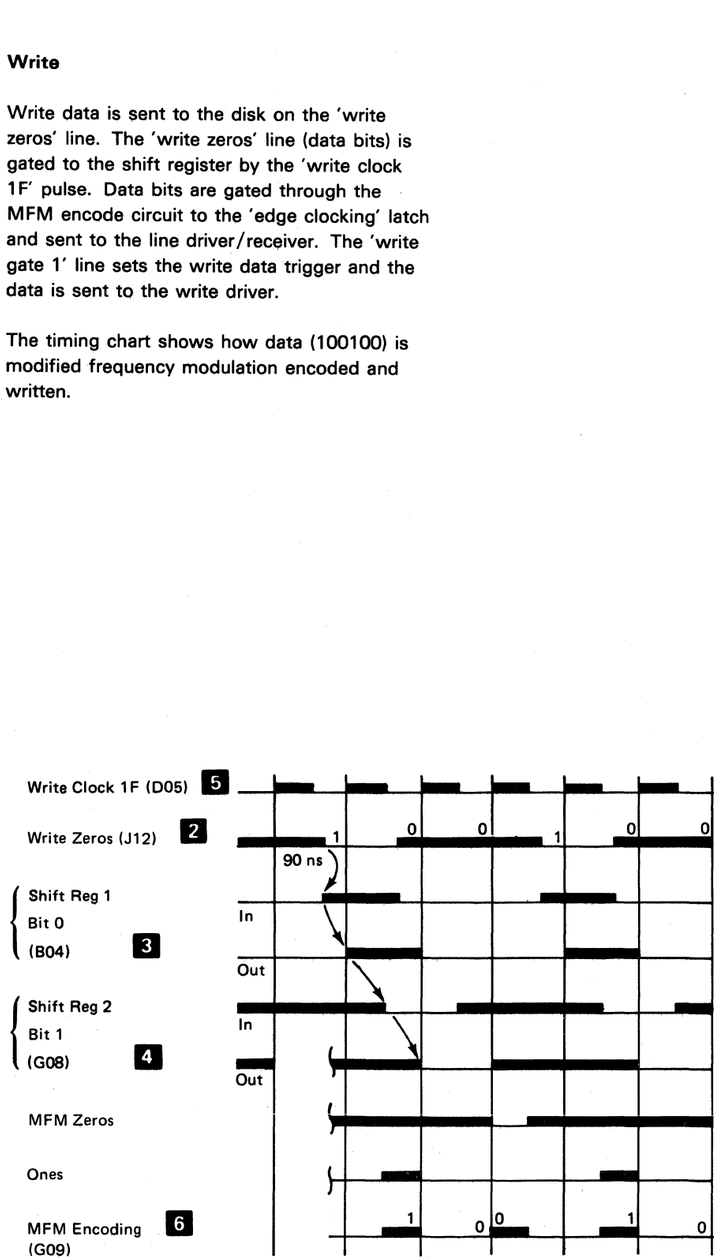

SWG
VFO Sync
S
Data
CRC
Buffer
EWG
2
12
1
256
2
4
2
7
8
9
10
11
12
13
End op.
SC8 = fast sync.
SC9 = search for first 0-bit of sync byte.
Read hex 0E from disk. Preset CRC to 1's.
Compare data read from storage with data read from disk. Scan hit disk data equal, low, or high (tested for by jump on I/O command).
Generate CRC in CRC register.
Read CRC from disk and compare with CRC register.
Read hex FFs from disk. End op.
From preceding page.
Write Clock
Read Clock
SC 9
SC 8
SC8, BC13, BR7
(transfer data from storage) (BR5)
BR7
SC = 10
SC 12 RD1F (strobe)
Sector + Index
Scan Hit Trigger
Disk Strobe
GF030 Not Mask Latch
Scanning starts here, drops at first byte of compare that is not hex FF.
GF030 Scan Mask
GF031 Scan Equal Hit
Reset at no compare
Set at every hex FF byte: not scan hit trigger.
GF030 Scan Hit
Set at scan hit: scan mask.
Stays up until next operation
GF050 Transfer to Storage
SC12 CSY TR
Read Circuits
Disk Drive
Servo Track-Follow Circuit
Servo Head
Clocks, Index Pulse, Sector Pulse
(not) Write
Sector Pulse
Index Pulse
Data Heads
Read Pre-amp
Write Driver
Write Clock 1F
Read Clock 1F
File Fast Sync
Standardized Data
Data Separator
Data Trans Lines
SERDES
Select Head

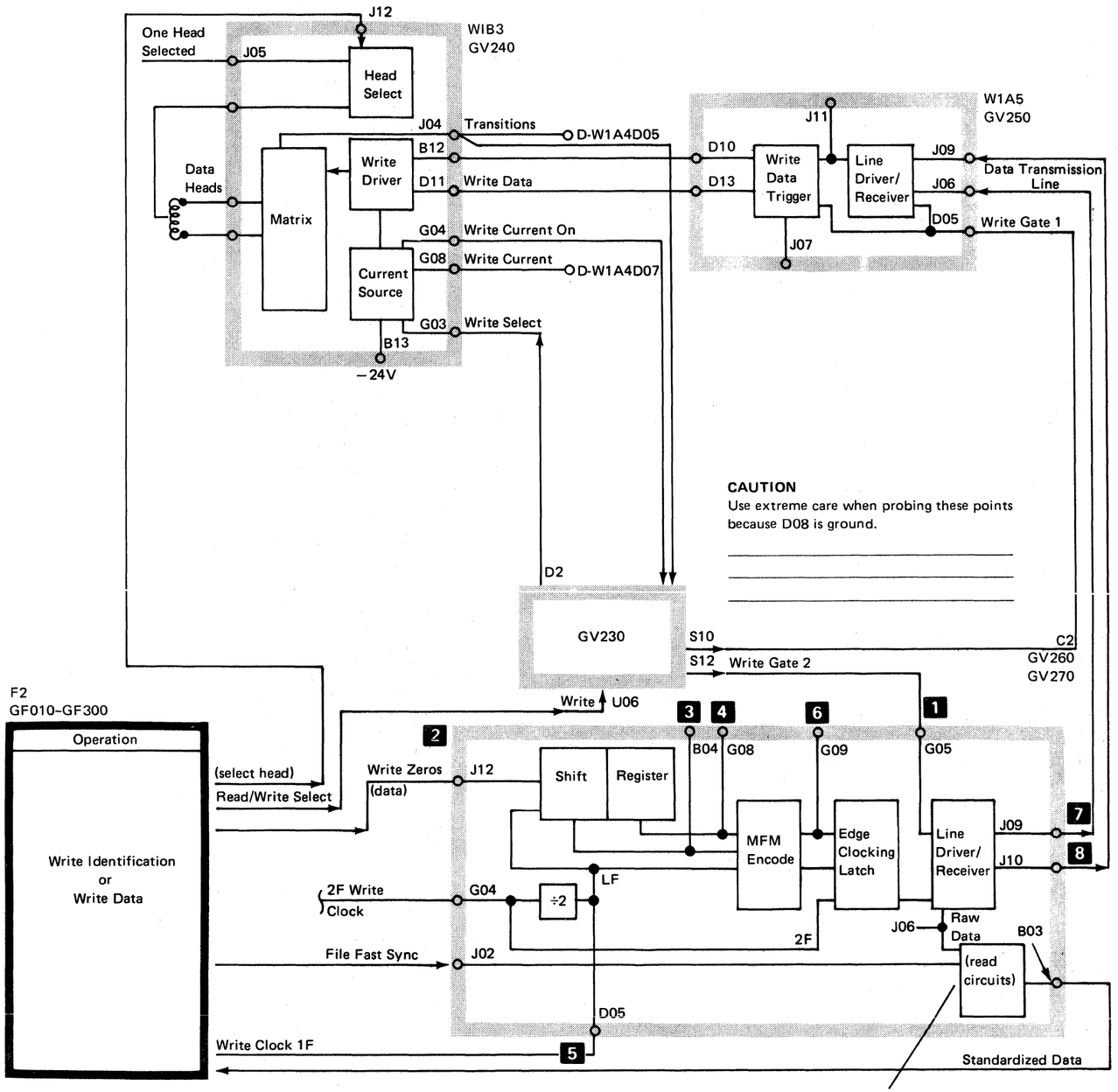
Write Circuits

Write

Write data is sent to the disk on the 'write zeros' line. The 'write zeros' line (data bits) is gated to the shift register by the 'write clock 1F' pulse. Data bits are gated through the MFM encode circuit to the 'edge clocking' latch and sent to the line driver/receiver. The 'write gate 1' line sets the write data trigger and the data is sent to the write driver.

The timing chart shows how data (100100) is modified frequency modulation encoded and written.





Note: The numbers on this figure (1 through 8) refer to the waveshapes on the following two pages.

Write Waveshapes

All of these waveshapes use the 'write gate 2' line as a sync point, with a times-10 grounded probe. There may be a small difference in amplitude of signals from one machine to another.

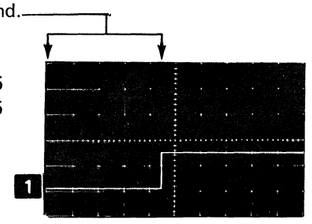
Write Identification

The following waveshapes can be seen on an oscilloscope when running the disk exerciser test using the following commands and options:

1. Seek to the CE cylinder:
   a. Recalibrate.
   b. Seek to the CE cylinder (these waveshapes were taken from a 13.2-megabyte disk). The CE cylinder is hex 00C9 on an 8.6-megabyte disk and hex 012E on a 13.2-megabyte disk.
   c. Select no options.
   d. Execute the command table.

2. Set up the command table for write identification:
   a. Write the identification.
   b. Select head 0.
   c. Select sector hex 1E.
   d. Select the option to restore the original control field.
   e. Select the scope loop option.
   f. Execute the command table.

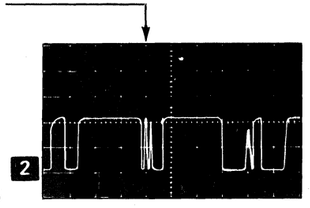
This waveshape shows write gate 2. Write gate 2 is active once during a write ID command.



Chan 1 Write Gate 2 C2G05
Sync Internal - Write Gate 2 C2G05

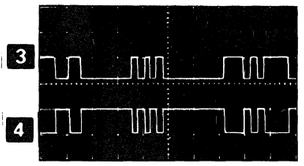
Voltage: 0.1 V/div
Time: 5 µs/div
DC Input

Turn the delay time multiplier to 0, then slowly advance the multiplier to get this figure. 12-µs delay. Keep the multiplier setting the same for the next waveshape.



Chan 1 Write Zeros C2J12
Sync External - Write Gate 2 C2G05

Voltage: 0.2 V/div
Time: Main Sweep 20 µs/div
Delayed Sweep 1 µs/div
DC Input



Chan 1 Shift Register Bit 0 C2B04

Chan 1 Shift Register Bit 1 C2G08
Sync External - Write Gate 2 C2G05

Voltage: 0.1 V/div
Time: Main Sweep 20 µs/div
Delayed Sweep 1 µs/div
DC Input

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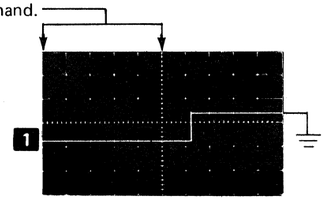
Write Data

The following waveshapes can be seen on an oscilloscope when running the disk exerciser test using the following commands and options:

1. Seek to the CE cylinder:
   a. Recalibrate.
   b. Seek to the CE cylinder (these waveshapes were taken from a 13.2-megabyte disk). The CE cylinder is hex 00C9 on an 8.6-megabyte disk and hex 012E on a 13.2-megabyte disk.
   c. Select no options.
   d. Execute the command table.

2. Set up the command table for write data:
   a. Select head 0.
   b. Select sector hex 1E.
   c. Select main storage data field 1.
   d. Set data field 1 to hex AAAA by pressing the A key.
   e. Select the scope loop option.
   f. Execute the command table.

This waveshape shows write gate 2. Write gate 2 is active once during a write data command.

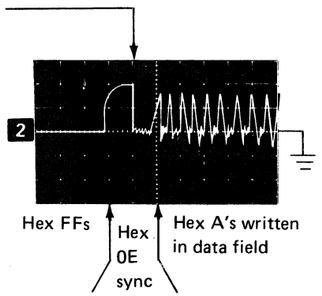


Chan 1 Write Gate 2 C2G05
Sync Internal - Write Gate 2 C2G05

Voltage: 0.1 V/div
Time: 50 μs/div
DC Input (about 35 μs)

Turn the delay time multiplier to 0, then slowly advance the multiplier to get this figure.

Keep the multiplier setting the same for the following waveshapes.



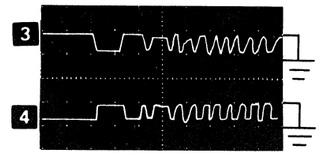
Chan 1 Write Zeros C2J12
Sync External - Write Gate 2 C2G05

Voltage: 0.2 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input

Chan 1 Shift Register Bit 0 C2B04

Chan 1 Shift Register Bit 1 C2G08

Sync External - Write Gate 2 C2G05

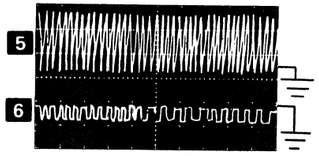


Voltage: 0.1 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input

Chan 1 Write Clock 1F C2D05

Chan 1 MFM Encoding C2G09

Sync External - Write Gate 2 C2G05

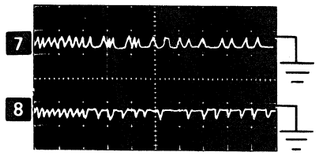


Voltage: 0.1 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input

Chan 1 Data Transmission Line C2J09

Chan 1 Data Transmission Line C2J10

Sync External - Write Gate 2 C2G05



Voltage: 0.1 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input

Read Circuits

Read

When the 'read select' and 'head select' lines from the attachment are activated, data is read from the disk and preamplified by a variable gain amplifier. Following the preamplifier is a circuit card that filters and shapes the data. This card also has a line driver/receiver that connects the read/write cable (data transmission line) to the logic gate.

Read Clock and Divide-by-2 Counter

The data separator card receives the data from the read/write cable and generates the read clock and standardized data. The read clock, which runs at 14.2 megahertz, is synchronized to the incoming data (see *File Fast Sync*).

Read Clock Synchronization Control

To lower the frequency of the clock (that is, delay the phase), the control voltage is lowered. To increase the clock frequency, the control voltage is increased. Therefore, to keep the clock locked to the data, the positive current source is turned on if the clock is behind phase with the data, and the negative current source is turned on if the clock runs in advance of the data.

Read Clock Sync

Current control is obtained from the 'data early' and 'data late' pulses that are generated from the data. The 'data early' and 'data late' pulses control the read clock as follows: each data bit sets the 'data SS' and 'phase' latches. The 'phase' latch output is compared with the 'data SS' latch output, which generates either the 'data early' or 'data late' pulse for use by the read clock '2F' pulse. If data is late, the frequency of the read clock is decreased; if data is early, the frequency of the read clock is increased.

Data Latch and Standardized Data Latch

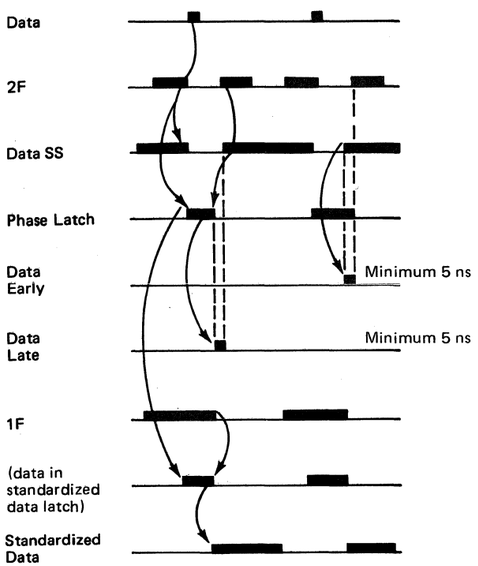
Input to the 'data' latch comes from the 2F clock, the 1F clock, and the 'phase' latch. The 'phase' latch activates the 'standardized data' latch. The 'standardized data' latch (read data) is then gated to the serializer/deserializer.

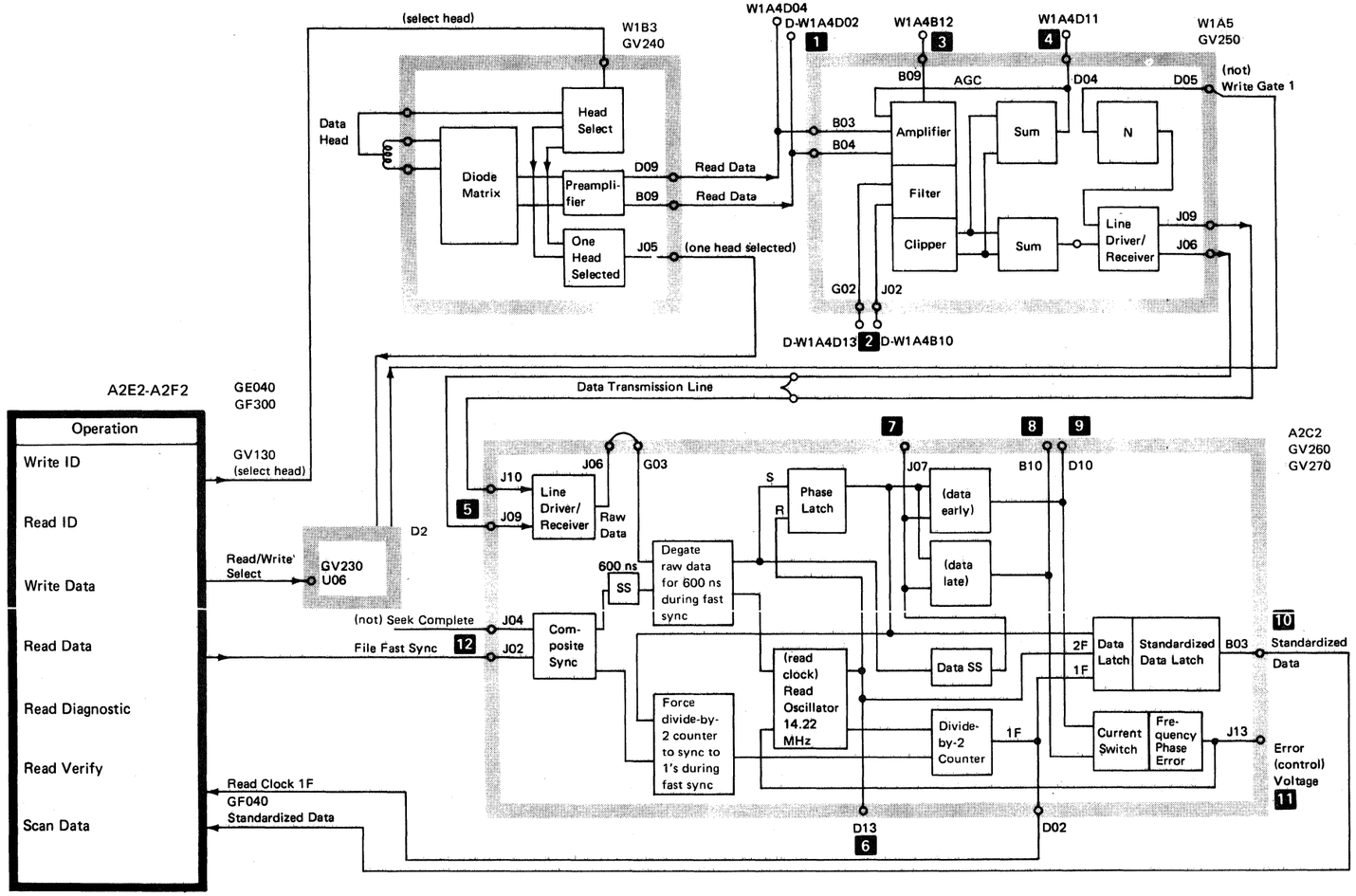
File Fast Sync

The 'file fast sync' line is activated for all read and write operations. For example, if a read identification operation is started, the variable frequency oscillator field is the first field read from the disk. The 'file fast sync' line is activated during the first 8 bytes of the field, which causes the read clock to sync to these 1's. This occurs because a field of 1's and a field of 0's have the same data pattern. Therefore, by forcing the read clock to synchronize to known 1's, the read clock senses 1's and 0's correctly for the remainder of the field.

Composite Sync

During a seek operation, the variable frequency oscillator is synchronized to the write clock. This keeps the oscillator near the correct frequency so it can sync to the read data after the seek.





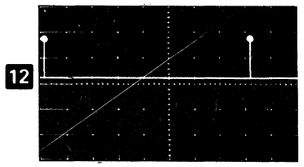
Note: The numbers on this figure (1 through 12) refer to the waveshapes on the following two pages.

Read Waveshapes

All of the read waveshapes were taken using a times-10 grounded probe. A scope hood should be used to view the signals. There may be a small difference in amplitude of signals from one machine to another.

Chan 1 File Fast Sync C2J02 12
Sync + Internal Chan 1

Voltage: 0.2 V/div
Time: 5 ms/div
AC Input



Read Identification

The following waveshapes can be seen on the oscilloscope when running the disk exerciser test using the following commands and options:

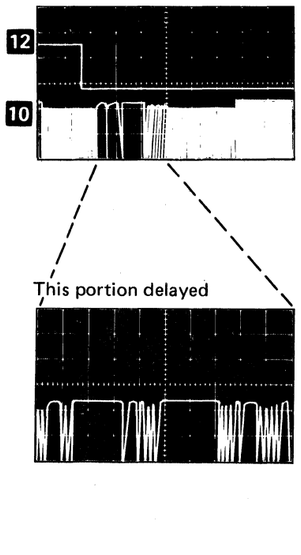
1. Seek to the CE cylinder:
   a. Recalibrate.
   b. Seek to the CE cylinder (these waveshapes were taken from a 13.2-megabyte disk). The CE cylinder is hex 00C9 on an 8.6-megabyte disk and hex 012E on a 13.2-megabyte disk.
   c. Select no options.
   d. Execute the command table.

2. Set up the command table for read identification:
   a. Select head 0.
   b. Select sector hex 1E.
   c. Select the scope loop option.
   d. Execute the command table.

Chan 1 File Fast Sync C2J02 12
Sync + Internal Chan 1

Chan 2 Standardized Data C2B03 10

Voltage: 0.2 V/div
Time: Main Sweep 5 μs/div
Delayed Sweep 1 μs/div



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Read Data

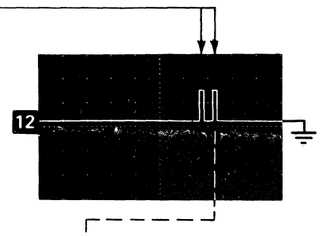
These waveshapes of hexadecimal A's were taken when the disk exerciser test was in a loop and reading from the CE track. Before these waveshapes are scoped, all hexadecimal A's must be written (on the CE track) by using the disk exerciser test.

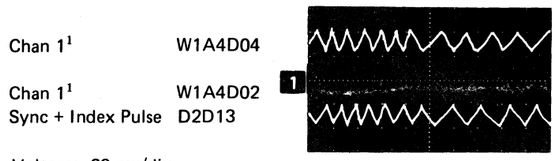
The following waveshapes can be seen on the oscilloscope when running the disk exerciser test using the following commands and options:

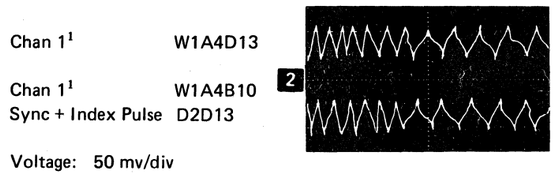
1. Seek to the CE cylinder:
   a. Recalibrate.
   b. Seek to the CE cylinder (these waveshapes were taken from a 13.2-megabyte disk). The CE cylinder is hex 00C9 on an 8.6-megabyte disk and hex 012E on a 13.2-megabyte disk.
   c. Select no options.
   d. Execute the command table.

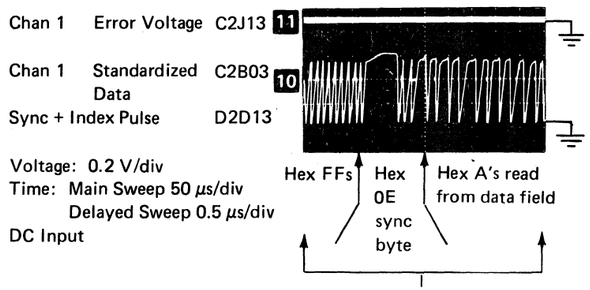
2. Set up the command table for read data:
   a. Select head 0.
   b. Select sector hex 1E.
   c. Select the scope loop option.
   d. Execute the command table.

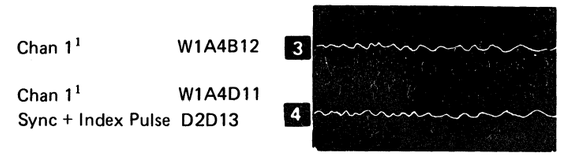
This waveshape shows file fast sync. File fast sync is active twice during a read data command.

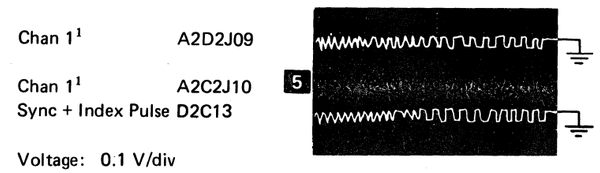


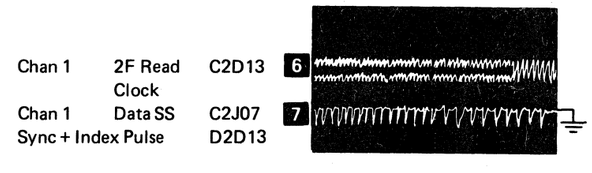


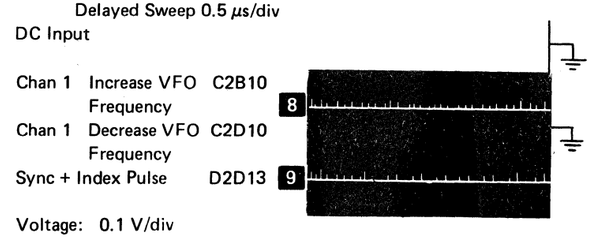












[1]May need a card extender

Track Follow Principles

The track follow circuits align the data heads on the track at the end of each seek operation and maintain head-to-track alignment during read and write operations.

The servo head reads a pattern that is aligned with each data track. The pattern is made up of position pulses (P1 and P2) and servo clock pulses (C) that repeat around each servo track.

Sequences of missing clock pulses identify the index pulses, sector pulses, and sector midpoint pulses. For more information, see *Servo Clock* later in this section.

Track Follow

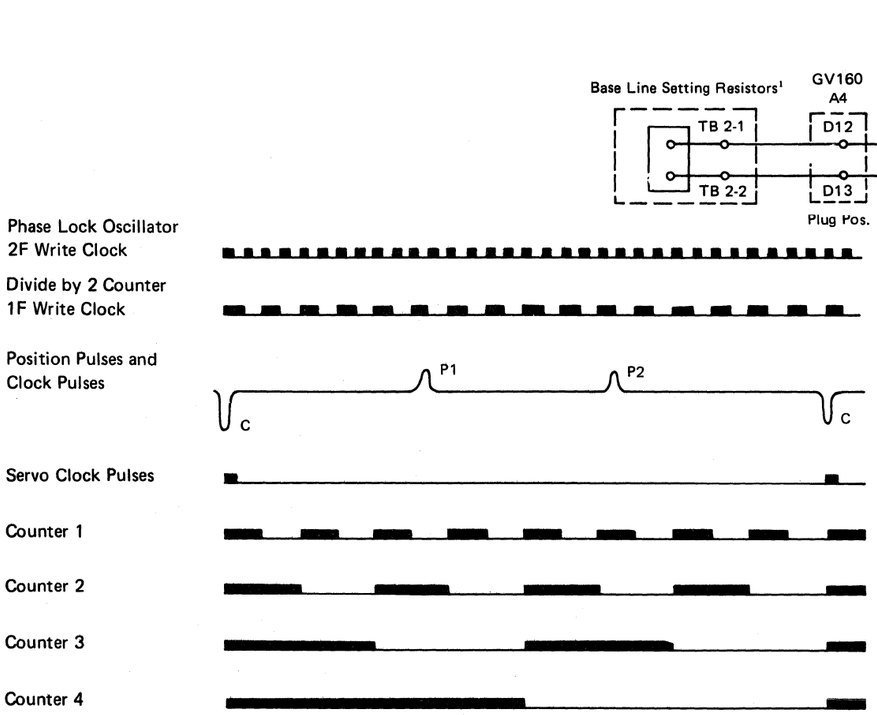
The servo track signal from the servo head is amplified, filtered, and separated into two signals: clock pulses and position pulses. These pulses are generated on the position detection and phase lock oscillator analog card (B2).

On the control and safety card (D2), each servo clock pulse fires a 600-nanosecond singleshot named the look-ahead singleshot. This singleshot permits a phase compare between the servo clock and the phase lock oscillator. If the servo clock occurs before the phase lock oscillator, a pulse is generated on the 'osc late' line. The width of the pulse is equal to the phase difference. If the servo clock is later than the phase lock oscillator, the pulse occurs on the 'osc early' line. The 'osc early' and 'osc late' signals are combined to form a control voltage to control the frequency of the phase lock oscillator. The phase lock oscillator runs at a frequency that is 32 times the frequency of the servo clock. A group of counters count the frequency down to the servo clock frequency.

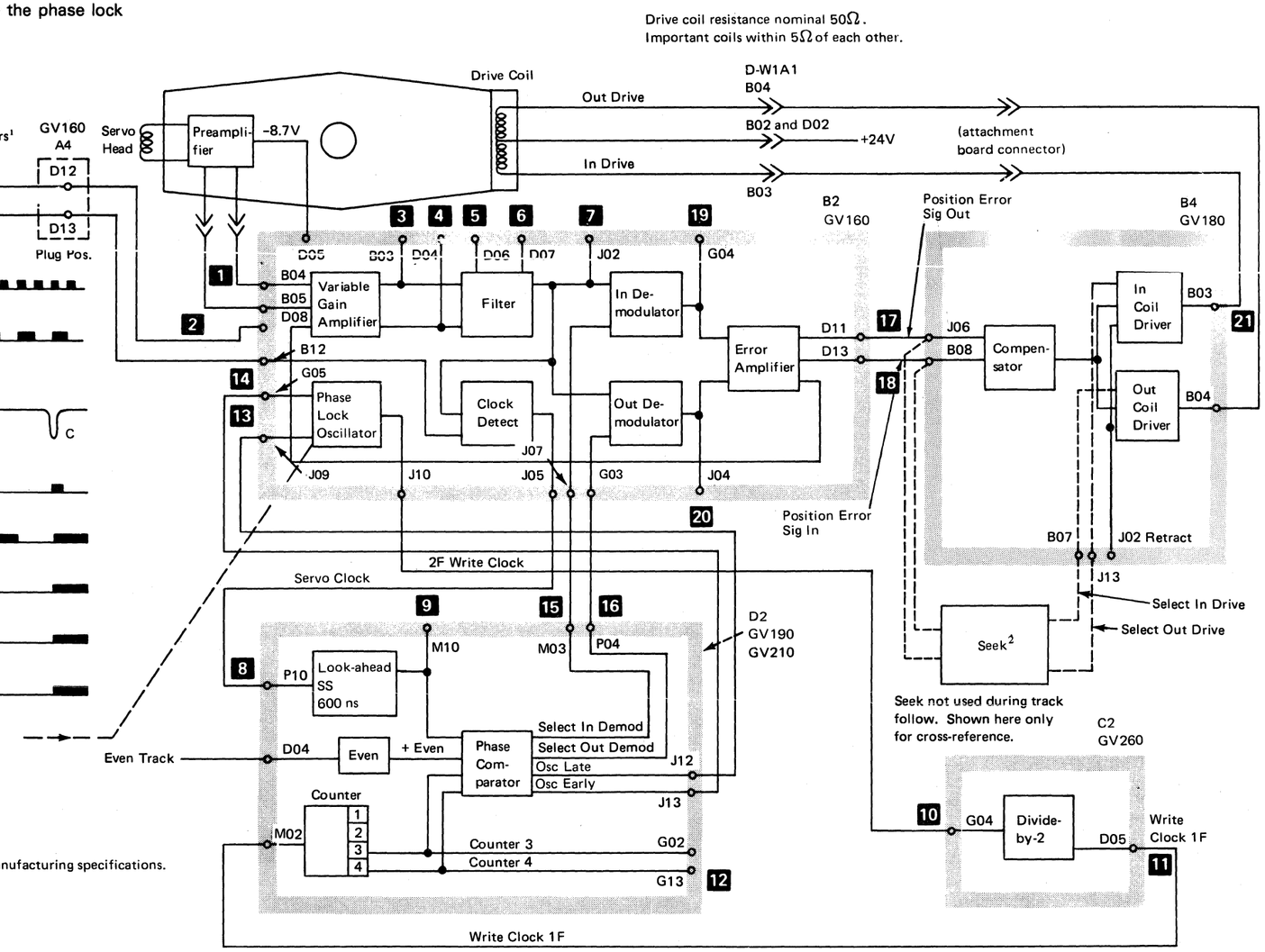
The 'select in demod' and 'select out demod' signals are synchronized with the servo pattern and switched so that one position pulse is gated to the in demodulator and the other position pulse is gated to the out demodulator. The polarity of even track (up for even and down for odd) indicates which position pulse is gated to which demodulator (select in or select out). This permits the position error signals to be used to keep the head on the desired track.

The position pulses, which generate the position error signals, are generated on the position detection card.

The position error signals are combined in the compensator to generate the drive signals for the coil drivers. The coil drivers move the actuator in the correct direction to position the servo head over the selected track. For more information, see *Servo Track Follow* later in this section.



The phase lock oscillator (PLO) operates at a frequency of 14.2 megahertz, and the output of the 'divide by 2 counter' has a frequency of 7.1 kilohertz. The 'servo clock' pulse (every 32 PLO pulses) is used as a reference to keep the 1F write clock in synchronization with the clock pulses.

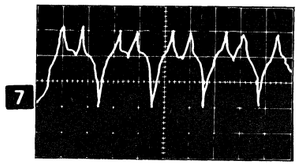


[1] Factory selection of the resistors is needed to match servo head and drive coil manufacturing specifications.

Track Follow Waveshapes

The following waveshapes can be seen on an oscilloscope if the servo operation is working correctly and the servo head is on a servo track. All waveshapes were taken with a times-10 grounded probe.

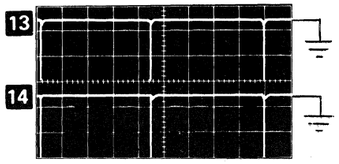
Chan 1 Servo Sig TP B2J02 **7**



Voltage: 0.1 V/div
Time: 1 μs/div
Trigger: External + D2P11, Chopped
AC Input

Chan 1 Osc Early B2G05 **13**

Chan 2 Osc Late B2J09 **14**



Voltage: 0.2 V/div
Time: 0.5 μs/div
Trigger: Internal + Chan 1, Chopped
AC Input

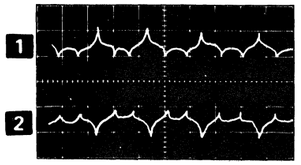
Chan 1 Out Demod B2G04 **19**

Chan 2 In Demod B2J04 **20**

Voltage: 10 mV/div
Time: 0.2 ms/div
Trigger: Internal + Chan 1
Vertical Mode: Add, Invert + Chan 2
Signal is inverted and therefore differential.

Chan 1 Pre-Amp Servo A B2B04 **1**

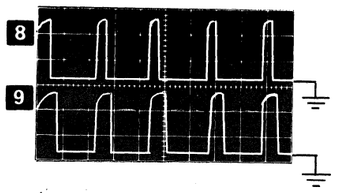
Chan 2 Pre-Amp Servo B B2B05 **2**



Voltage: 10 mV/div
Time: 1 μs/div
Trigger: External + D2P11 - Sector Pulse
AC Input

Chan 1 Servo Clock D2P10 **8**

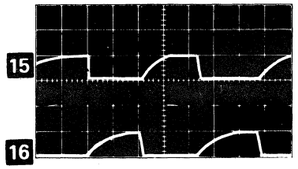
Chan 2 Look-ahead SS D2M10 **9**



Voltage: 0.2 V/div
Time: 1 μs/div
Trigger: External + D2P11, Chopped
DC Input

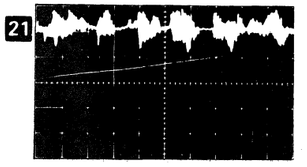
Chan 1 Select In Demod D2M03 **15**

Chan 2 Select Out Demod D2P04 **16**



Voltage: 0.5 V/div
Time: 0.5 μs/div
Trigger: Internal + Chan 1, Chopped
AC Input

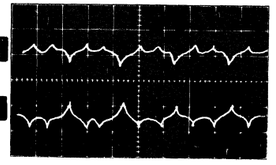
Chan 1 In Drive B4B03 **21**



Voltage: 1 V/div
Time: 1 ms/div
Trigger: External + C4J13 - Speed Transducer

Chan 1 B2B03 **3**

Chan 2 B2D04 **4**

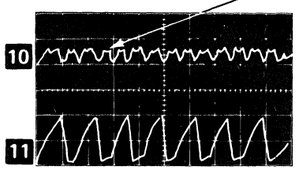


Voltage: 10 mV/div
Time: 1 μs/div
Trigger: External + D2P11, Chopped
AC Input

May be distorted at beginning because PLO is syncing in.

Chan 1 2F Write Clock C2G04 **10**

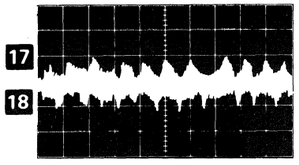
Chan 2 Write Clock 1F C2D05 **11**



Voltage: 0.2 V/div
Time: 0.1 μs/div
Trigger: External + D2P11, Chopped
AC Input

Chan 1 Position Error Sig Out B2D11 **17**

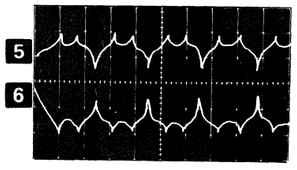
Chan 2 Position Error Sig In B2D13 **18**



Voltage: 5 mV/div
Time: 2 μs/div
Trigger: Internal + Chan 1
Vertical Mode: Add, Invert + Chan 2
Signal is inverted and therefore differential.

Chan 1 B2D06 **5**

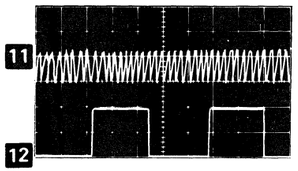
Chan 2 B2D07 **6**



Voltage: 20 mV/div
Time: 1 μs/div
Trigger: External + D2P11, Chopped
AC Input

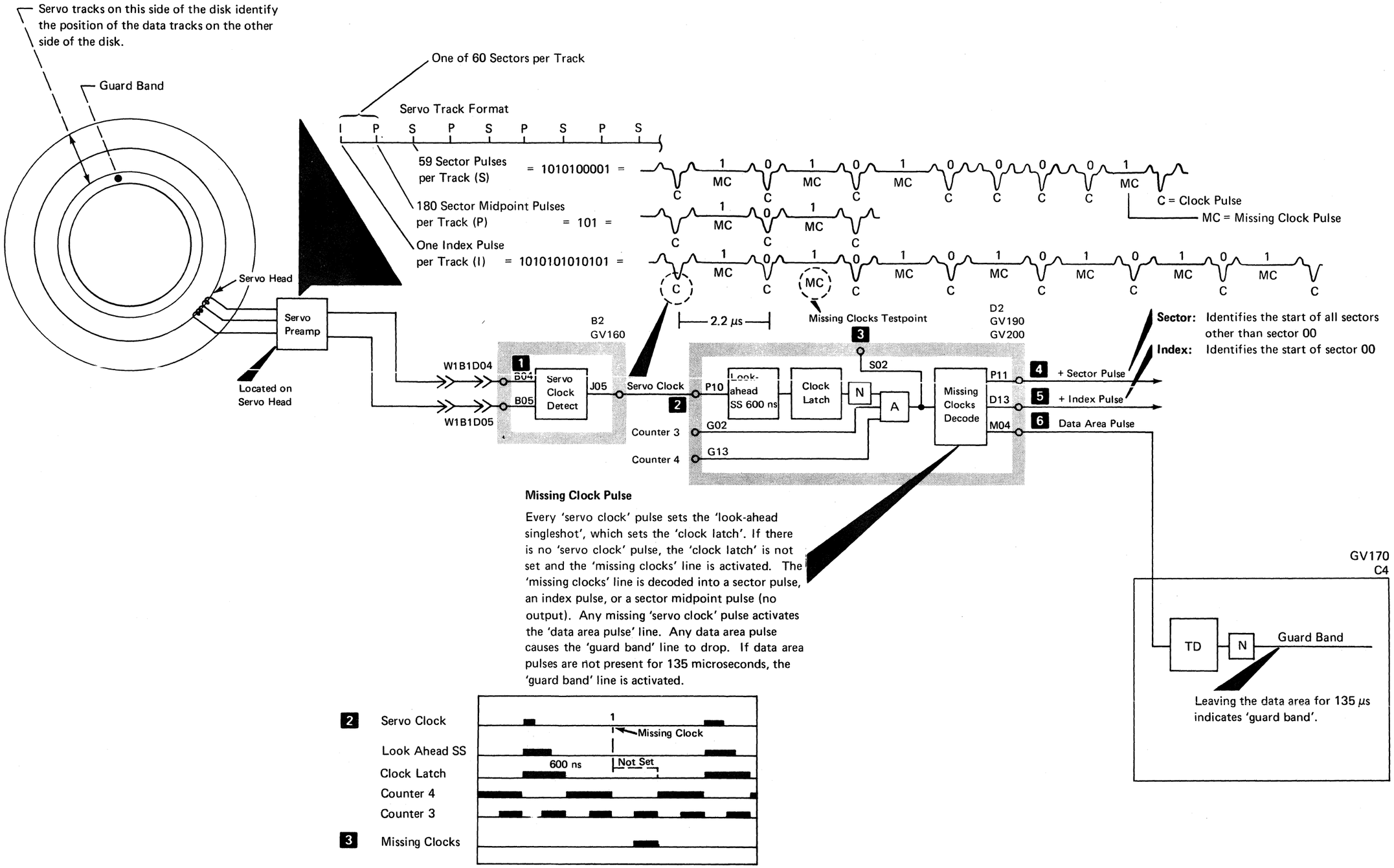
Chan 1 Write Clock 1F C2D05 **11**

Chan 2 Counter 4 D2G13 **12**



Voltage: 0.2 V/div
Time: 0.5 μs/div
Trigger: External + D2P11, Chopped
AC Input

Servo Clock



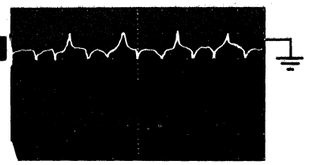
Missing Clock Pulse

Every 'servo clock' pulse sets the 'look-ahead singleshot', which sets the 'clock latch'. If there is no 'servo clock' pulse, the 'clock latch' is not set and the 'missing clocks' line is activated. The 'missing clocks' line is decoded into a sector pulse, an index pulse, or a sector midpoint pulse (no output). Any missing 'servo clock' pulse activates the 'data area pulse' line. Any data area pulse causes the 'guard band' line to drop. If data area pulses are not present for 135 microseconds, the 'guard band' line is activated.

Servo Clock Waveshapes

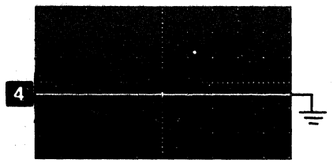
All waveshapes were taken with a times-10 probe.

Chan 1
Pre-Amp Servo A B2B04 1



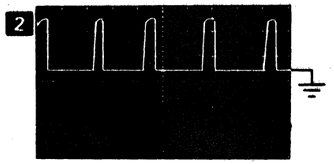
Voltage: 10 mV/div
Time: 1 μs/div
Trigger: External + D2P11 Sector Pulse
AC Input

Chan 1 Sector Pulse D2P11 4



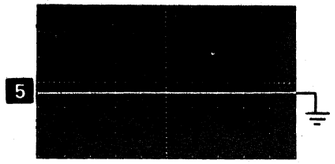
Voltage: 0.2 V/div
Time: 50 μs/div
Trigger: External + D2D13
DC Input

Chan 1 Servo Clock D2P10 2



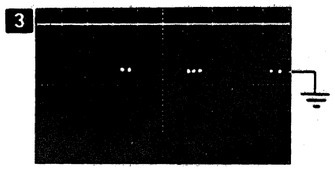
Voltage: 0.2 V/div
Time: 1 μs/div
Trigger: External + D2P11 Sector Pulse
DC Input

Chan 1 Index Pulse D2D13 5



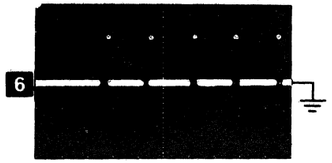
Voltage: 0.2 V/div
Time: 50 μs/div
Trigger: External + D2P11
DC Input

Chan 1 Missing Clocks D2S02 3



Voltage: 0.2 V/div
Time: 50 μs/div
Trigger: External + D2D13
DC Input

Chan 1 Data Area Pulse
D2M04 6

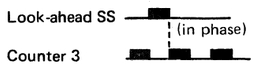


Voltage: 50 mV/div
Time: 50 μs/div
Trigger: External + D2D13
DC Input

Phase Lock Oscillator

Phase Lock Oscillator Synchronization

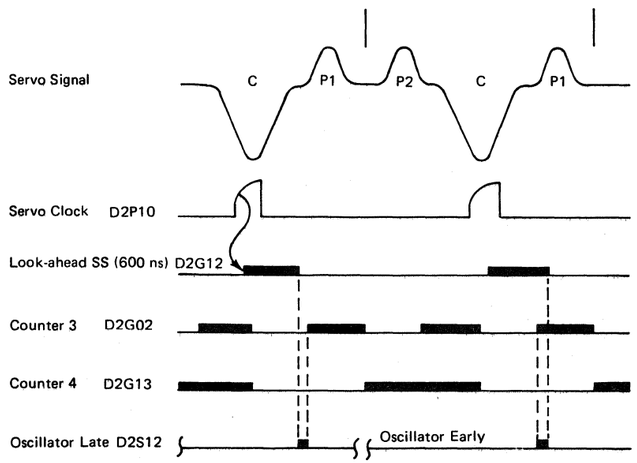
The phase lock oscillator is synchronized by comparing the phase of the servo clocks with the 'counter 3' signal. Correct synchronization occurs when the trailing edge of the 'look-ahead SS' is in phase with the leading edge of the 'counter 3' signal.



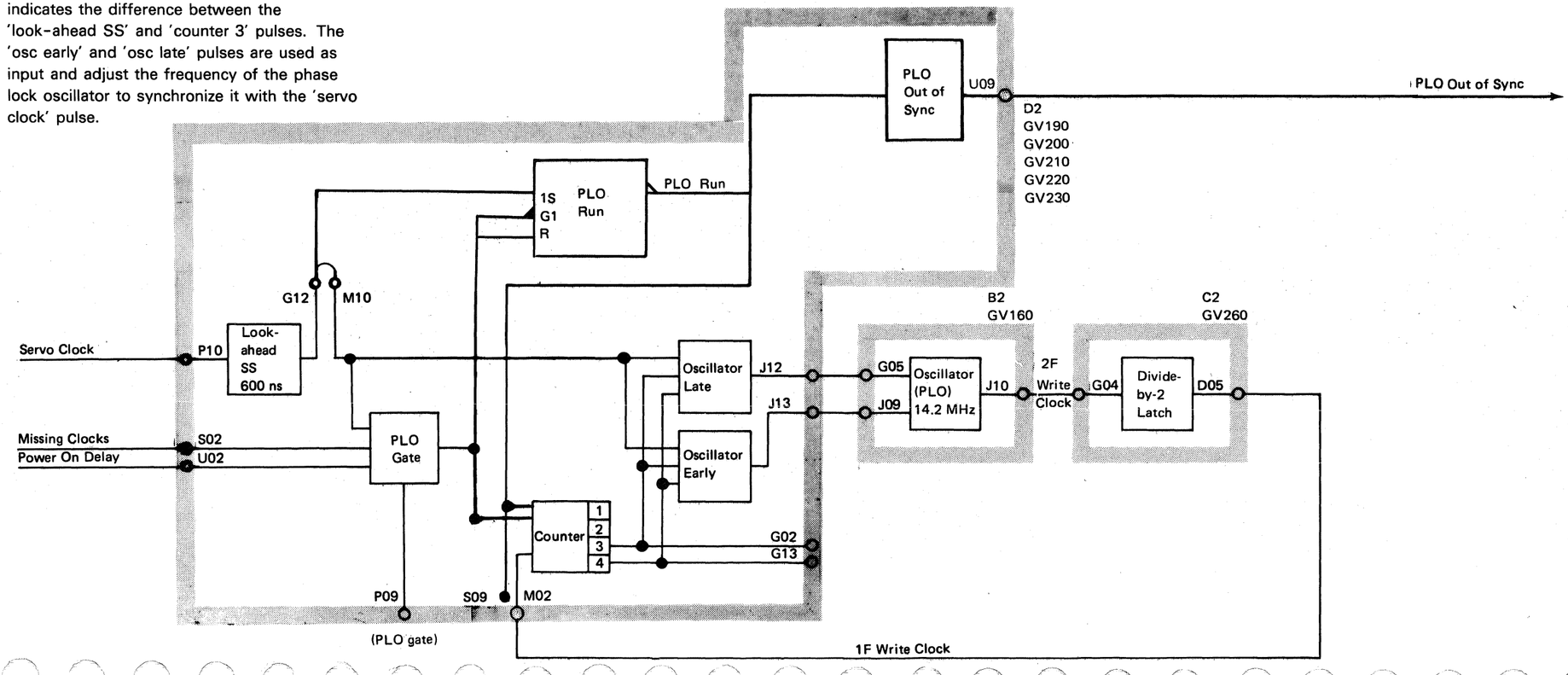
The 'counter 3' signal is generated from the phase lock oscillator by a divide-by-16 counter, and the 'look-ahead SS' is generated directly from the 'servo clock' pulse.

When the 'look-ahead SS' and 'counter 3' signals are out of phase, the difference between them generates an 'osc early' or 'osc late' pulse. The width of this oscillator pulse indicates the difference between the 'look-ahead SS' and 'counter 3' pulses. The 'osc early' and 'osc late' pulses are used as input and adjust the frequency of the phase lock oscillator to synchronize it with the 'servo clock' pulse.

Pulses in the Phase Lock Oscillator Circuits



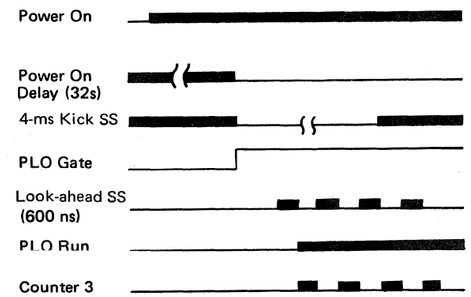
Note: This is a simplified timing diagram. The 'oscillator late' and 'oscillator early' pulses do not occur on consecutive 'servo clock' pulses.



Synchronization After Power On

When system power is set on, the 'power on delay' line is active for 32 seconds after all voltages come on. When the 'power on delay' line is de-activated, the '4-ms kick SS' causes the actuator control to start a recalibrate operation.

When the 'power on delay' line is active, the frequency dividing counters and the 'look-ahead SS' are held reset. To ensure that the counters and other circuits start operation in the correct status, the 'PLO run' latch sequences them into operation.



Phase Lock Oscillator Out of Synchronization

Two conditions cause the phase lock oscillator to be out of synchronization with the servo clock pulses:

- The loss of four or more servo clock pulses.
- A phase error of 90 degrees or more, between the 'look-ahead SS' and 'counter 3' pulses.

If the phase lock oscillator synchronization is lost during normal operation, both demodulator gates are selected. This forces a zero position error signal to prevent overdriving the actuator arm.

If the phase lock oscillator synchronization is lost during a write operation, a data unsafe condition occurs. See *Error Conditions* later in this section.

Recalibrate Operation

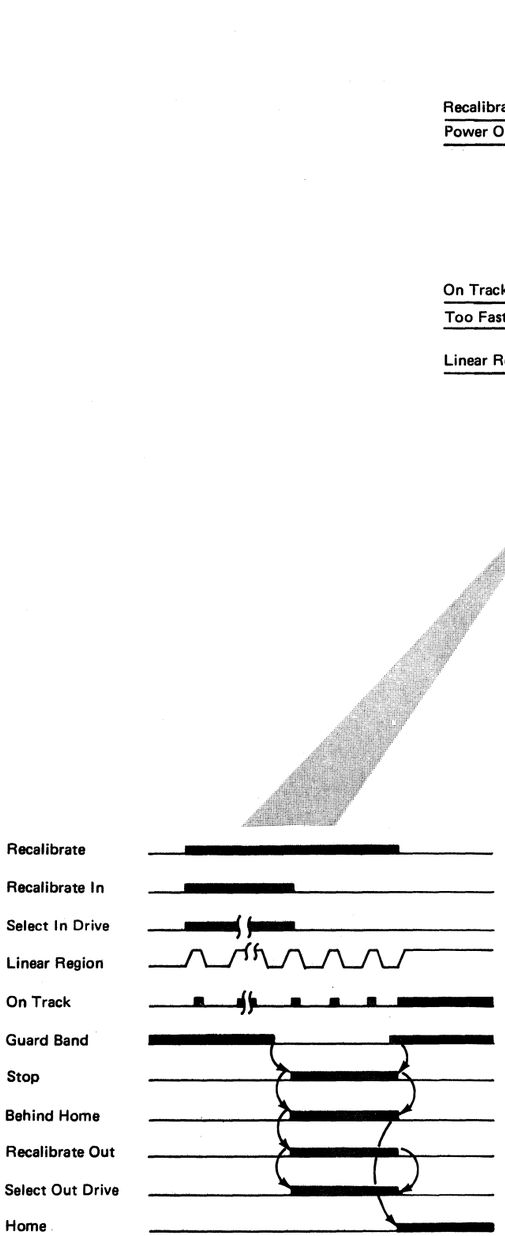
The recalibrate operation moves the heads across the cylinders to the guard band area (approximately cylinder -4), then out to stop at home (cylinder 0).

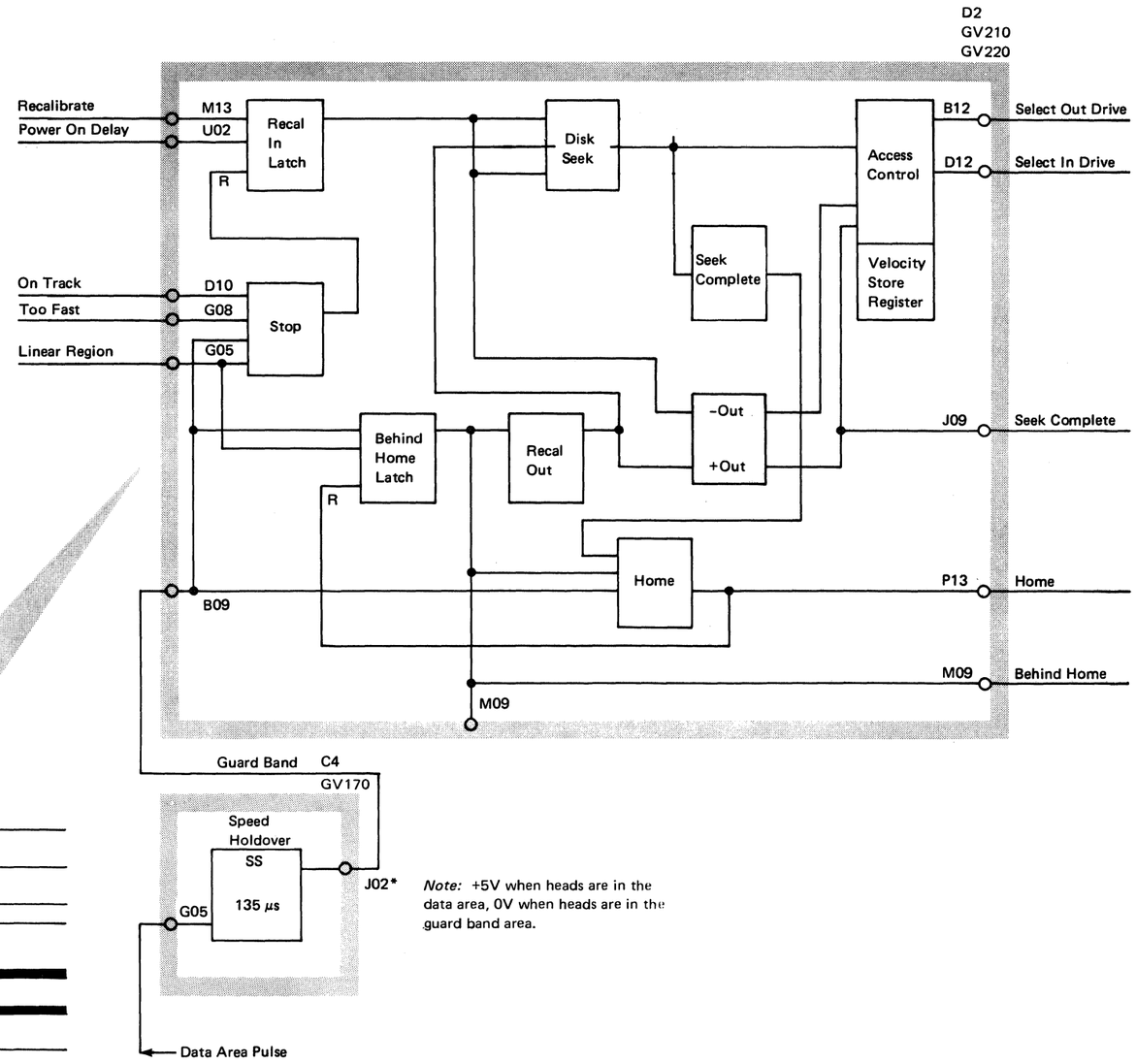
The disk exerciser can be used to seek out and recalibrate continuously. Select options 3 and 4 for recalibrate and seek out commands (a seek to the CE cylinder is a good example). Select E and enter Y or N for the next two screens, depending on the options desired. Select option 3 for the loop-on-command table.

During a recalibrate operation, the heads move at slow velocity.

When a recalibrate command is issued, it sets the 'recalibrate in' latch; the 'disk seek' and the 'select in drive' lines are activated. The servo head is driven into the guard band area. The 'guard band' line is active when the heads are behind home; the 'guard band' line sets the 'behind home' latch, which sets the 'recalibrate out' line, which activates the 'select out drive' line. When the 'select out drive' line is active, the servo head and the data heads are moved away from the spindle and out of the guard band area. As the heads move over cylinder 0, data area pulses are detected again. This drops the 'guard band' line, which sets the 'home' latch. The 'select out drive' line is de-activated and the heads settle on track over home (cylinder 0).

In a power-on sequence, the heads start from behind home. The recalibrate operation is started by the 'power on delay' and 'guard band' lines.





Note: +5V when heads are in the data area, 0V when heads are in the guard band area.

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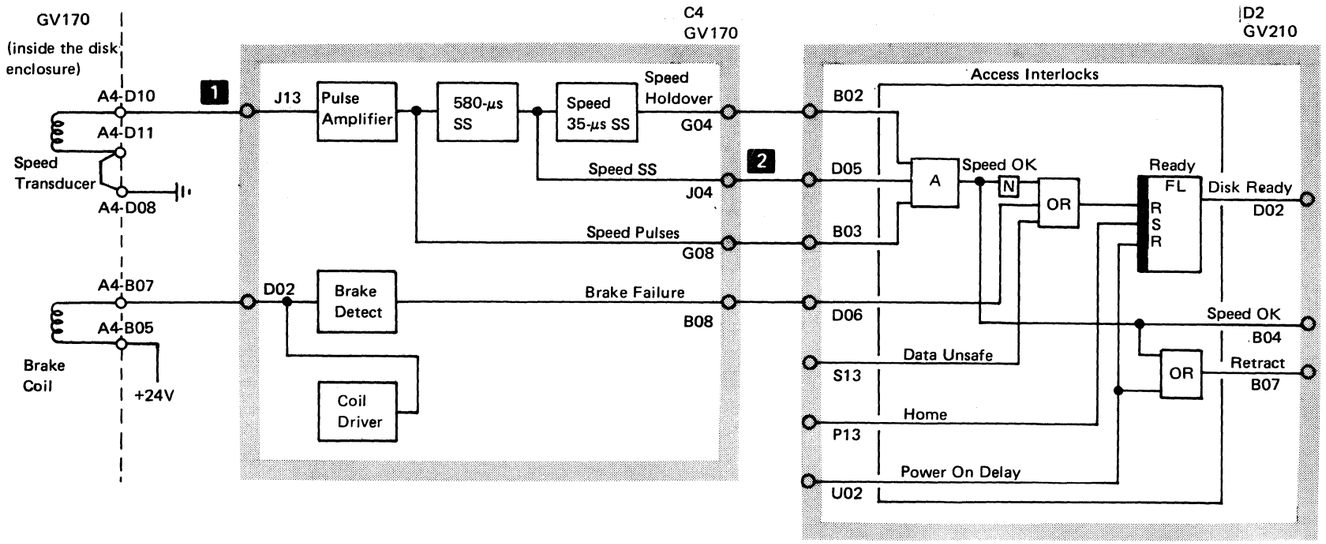
Disk Ready

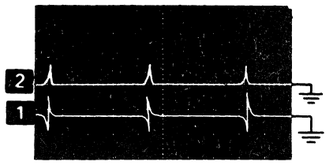
The 'disk ready' line is activated when the data heads are at home (cylinder 0) following power on or a recalibrate operation.

The disk may become not ready or fail to become ready after powering on for the following reasons:

- There is a data unsafe condition. The 'data unsafe' line indicates that one or more of the unsafe disk conditions in the attachment were set, or that a card is not plugged or seated correctly. For more information, see *Data Unsafe* later in this section.
- There is an electrical failure of the brake. A brake failure is indicated if there is a short circuit or an open circuit in the brake coil. The motor can override the brake, so the system removes AC power from the file motors when there is a brake failure.
- The disk is not turning at the correct speed. If the disk does not reach the correct speed, the actuator is kept at the inner stop. If there is a decrease in disk speed after power on, the 'ready' latch is reset.

Note: The actuator is retracted during power on delay or if the disk speed is too slow.

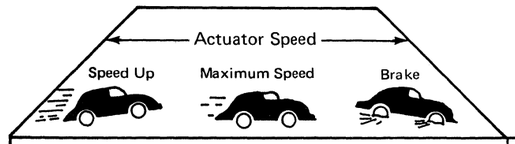




Voltage: 0.5 V/div
Time: 5 ms/div
Trigger: Internal + Channel, Chopped
DC Input

Seek Operation

The seek operation, which is started by an I/O control load command to the attachment, moves the heads to the desired cylinder. An I/O control load command controls the seek by specifying the number of tracks to seek. Another I/O control load command is needed to start the seek. After the seek is started, the attachment controls the direction to seek (in or out) and if an even or odd track is desired.



Seek Mode			
Start Moving the Actuator	Move the Actuator at Constant Speed	Stop the Actuator	Track Follow
When seek is activated, the actuator starts moving by energizing either the in or out actuator coil driver, depending upon the direction of the seek. The actuator continues to speed up until the 'hybrid velocity' line (the actual speed of the arm) is more than the 'compare velocity' line (the speed determined by the value in the down counter).	The 'compare velocity' line compared with the 'hybrid velocity' line (sensed speed) develops the 'too fast' line. The 'too fast' line and the 'velocity follow' latch control the 'select in drive' and 'select out drive' lines, which causes the actuator to move at a constant maximum speed.	The 'compare velocity' signal level begins to drop as the actuator nears the desired track. The 'hybrid velocity' signal is now greater than the 'compare velocity' signal. The 'too fast' line is active and causes continuous selection of the 'select out drive' line for an in move or the 'select in drive' line for an out move. The actuator therefore decelerates along a curve defined by the 'compare velocity' signal. One track before the seek ends, seek goes inactive to allow the 'velocity follow' latch to be reset by the next positive edge of the 'linear region' signal. When the 'velocity follow' latch is reset, the servo loop circuit controls the actuator and locks it on the track. The 'seek complete' line is activated when the 'on track' line has been active for 4 ms.	When the actuator enters the linear region of the desired track, track-follow mode begins. The actuator stays in this mode until the next seek.

Seek

Number of Tracks

The I/O control load command loads the track counter 2 with the number of tracks to seek. The track counter is stepped down with each 'on track' pulse as each track is passed. When the track counter reaches 0, the 'borrow' line resets the seek operation and the disk goes into track-follow mode.

The value set in the track counter at the start of a seek also determines how quickly the actuator moves to the desired track. The actuator speeds up until it either reaches maximum speed or meets the 'compare velocity' signal. When the 'hybrid velocity' signal (the speed of the actuator) is more than the 'compare velocity' signal (the desired speed generated by the track counter), the 'too fast' line becomes active and decreases the actuator speed until it follows the 'compare velocity' signal.

Seek Start

An I/O control load command activates:

- The 'seek' line 1, in the attachment.
- Either seek in or seek out. The 'seek in' line 17 sets up the circuits for the direction of the seek.
- The 'even track' line 18 if the seek is to an even track or de-activates the 'even track' line if the seek is to an odd track.

Note: The numbers on this page refer to the figures on the following three pages.

Actuator Feedback During Seek

Position Error

As the actuator moves across the tracks, the position error signals 3 and 4 from the servo heads change from maximum (between tracks) to minimum (on track) and back to maximum. Other signals generated from the position error signals are:

- The 'on track' signal 8 becomes active each time the head passes through a track alignment; the 'on track' signal steps the down counter.
- The 'linear region' signal 7 becomes active when the head-to-track alignment error is low enough to be corrected by track-follow mode; at the end of a seek operation, the leading edge of the 'linear region' pulse switches from seek mode to track-follow mode.
- The 'hybrid velocity' signal 6 follows the speed of the actuator; that is, it indicates the speed of the actuator.
- The 'too fast' signal 10 becomes active if the 'hybrid velocity' signal 6 is more than the 'compare velocity' signal 9. (The desired velocity is determined by the value in the track counter.) The 'velocity follow' latch permits the 'too fast' signal to control the actuator speed during a seek. When the 'too fast' signal is not active, the actuator speeds up; when the 'too fast' signal is active, the actuator slows down.

Note: The numbers on this page refer to the preceding page and the following two pages.

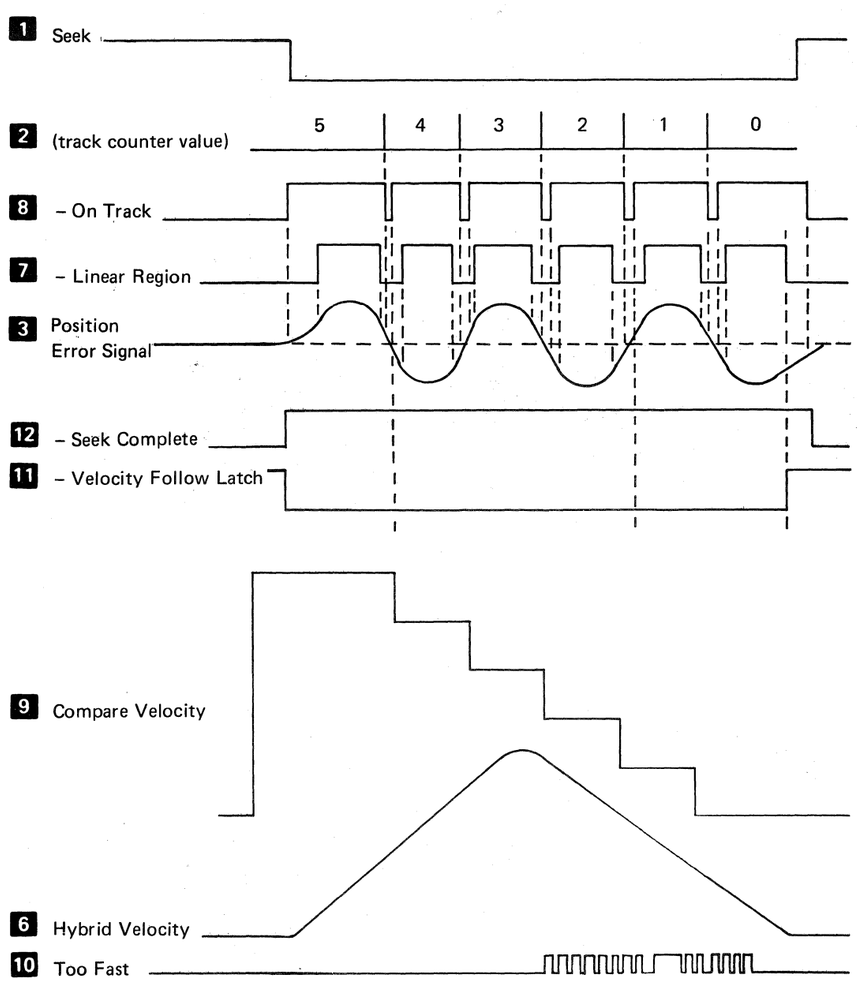
Compare Velocity

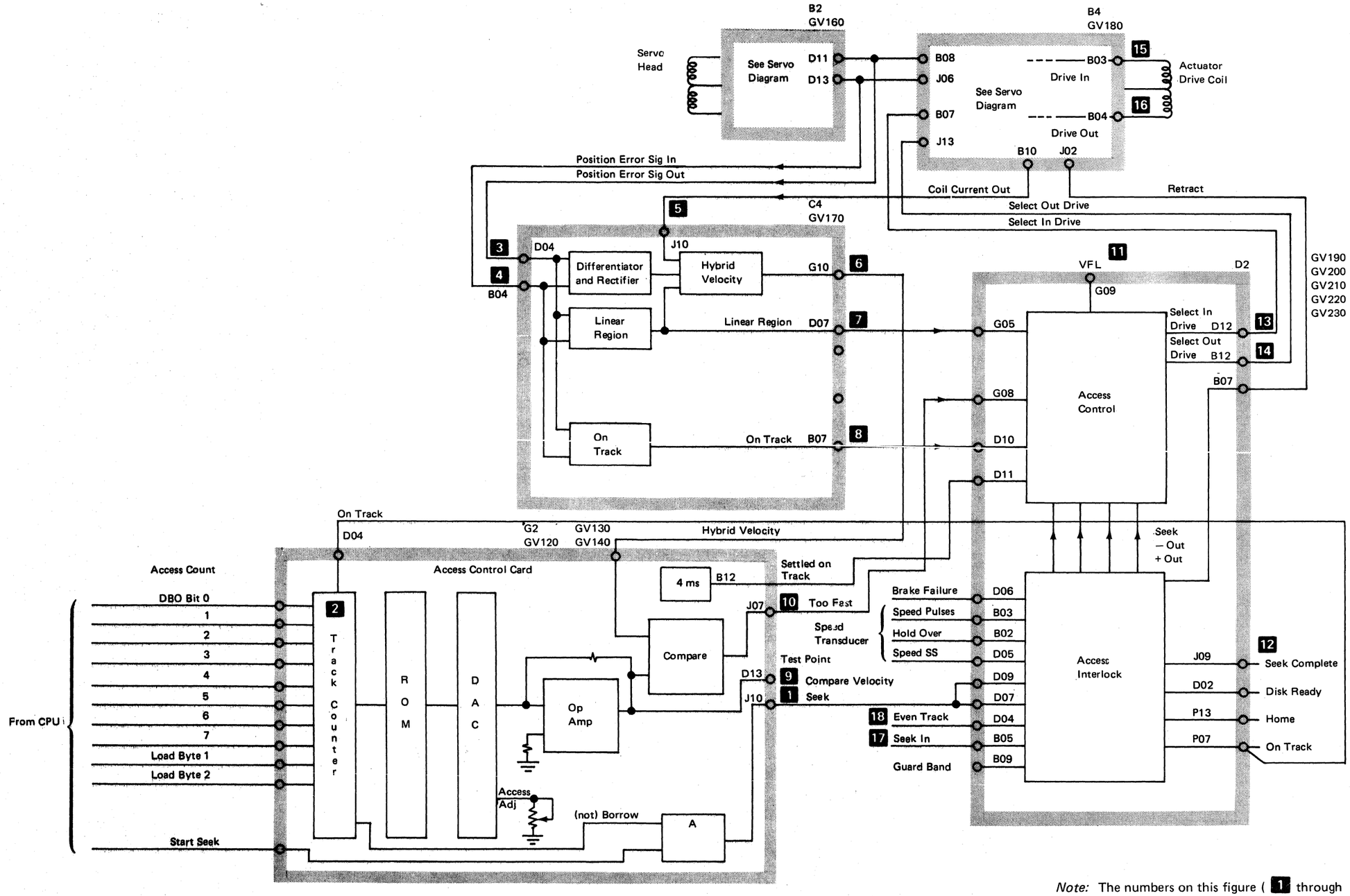
The 'compare velocity' line 9 is generated from the value set in the track counter at the start of the seek. The counter value feeds the read-only storage, which generates the 'compare velocity' signal level that feeds the digital-to-analog converter. A maximum 'compare velocity' signal level is reached on seeks of approximately 130 cylinders or greater. On a long seek, the actuator speeds up until it reaches maximum speed and then moves at maximum speed until 64 tracks before the desired track. Then, the 'compare velocity' signal steps down and the arm follows the down slope to the desired track.

Velocity Follow Latch

The 'velocity follow' latch 11 comes on at the start of a seek and gates the seek controls to the actuator. When the 'velocity follow' latch goes off, the actuator is under the control of track-follow mode.

Five-Track Seek Example





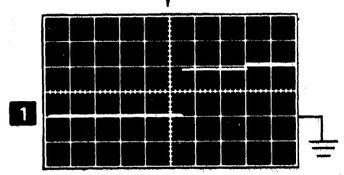
Note: The numbers on this figure (1 through 18) refer to the numbers on the preceding two pages and the next page.

Seek Waveshapes

Five-Track Seek (Tracks 0-5) Using the Disk Exerciser Test

All waveshapes were taken with a times-10 probe.

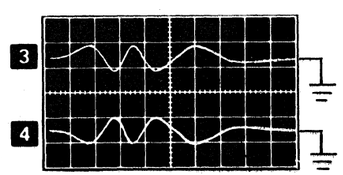
Seek G2J10



Voltage: 0.2 V/div
Time: 1 ms/div
Trigger: Internal

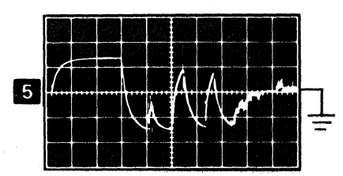
Position Error Sig Out B2D11

Position Error Sig In B2D13



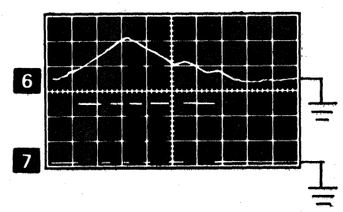
Voltage: 50 mv/div
Time: 1 ms/div
Trigger: External
Mode: Alternate

Coil Current Out C4J10



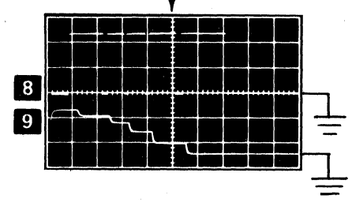
Voltage: 0.1 V/div
Time: 1 ms/div
Trigger: External G2J10

Hybrid Velocity C4G10



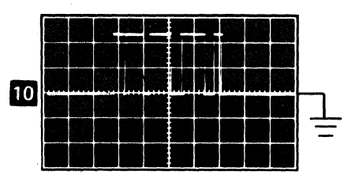
Voltage: 50 mv/div
Linear Region C4D07
Voltage: 0.2 V/div
Time: 1 ms/div
Trigger: External G2J10

On Track C4B07



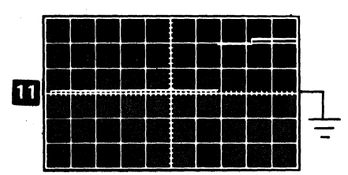
Voltage: 0.2 V/div
Compare Velocity G2D13
Voltage: 50 mv/div
Time: 1 ms/div
Trigger: External G2J10

Too Fast G2J07



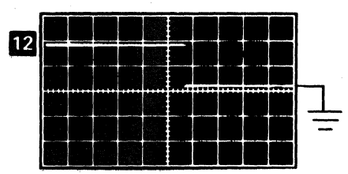
Voltage: 0.2 V/div
Time: 1 ms/div
Trigger: External G2J10

Velocity Follow Latch D2G09



Velocity: 0.2 V/div
Time: 1 ms/div
Trigger: External G2J10

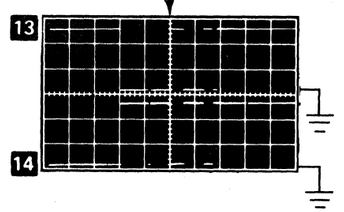
Seek Complete D2J09



Voltage: 0.2 V/div
Time: 2 ms/div
Trigger: External G2J10

Select In Drive D2D12

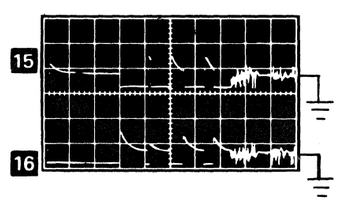
Select Out Drive D2B12



Voltage: 0.2 V/div
Time: 1 ms/div
Trigger: External G2J10

In Drive B4B03

Out Drive B4B04



Voltage: 5.0 V/div
Time: 1 ms/div
Trigger: External G2J10

Note: The numbers on this page (1 through 16) refer to the numbers on the preceding three pages.

Power On and Off

The Power switch (on the operator panel) and contactor K1 activate the DC power supplies (A).

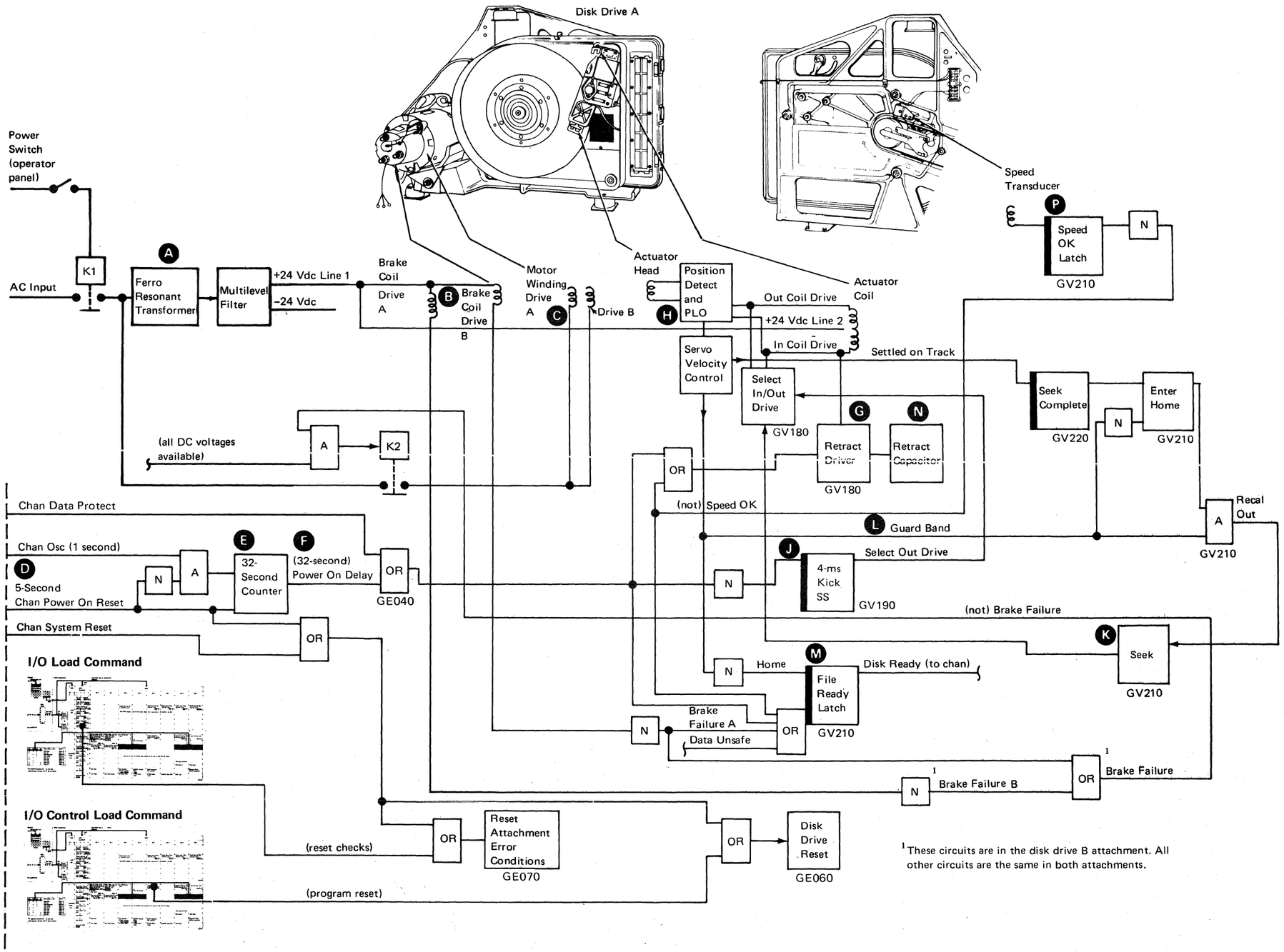
The brake coil circuit (B) lets contactor K2 pick and the disk drive motor (C) start. If the brake coil circuit indicates a brake failure on either disk drive A or disk drive B, K2 cannot pick. This prevents AC power to either motor.

The '5-second chan power on reset' line (D) holds the 32-second counter (E) reset. After 5 seconds, the 32-second counter starts to run. During this time, the 'power on delay' line (F) is active (see note). During power on delay, the retract driver (G) holds the actuator against the inner (spindle) stop. At the end of the 32-second delay, the 'power on delay' line goes off and the phase lock oscillator (H) synchronizes to the servo clock pulses.

At the end of the power on delay, the '4-ms kick SS' (J) starts the actuator outward movement; then, seek (K) continues the movement. Finding the data area de-activates the 'guard band' line (L). The outward seek is ended and the actuator stops the data heads over cylinder 0; the 'home' line activates the 'file ready' latch (M).

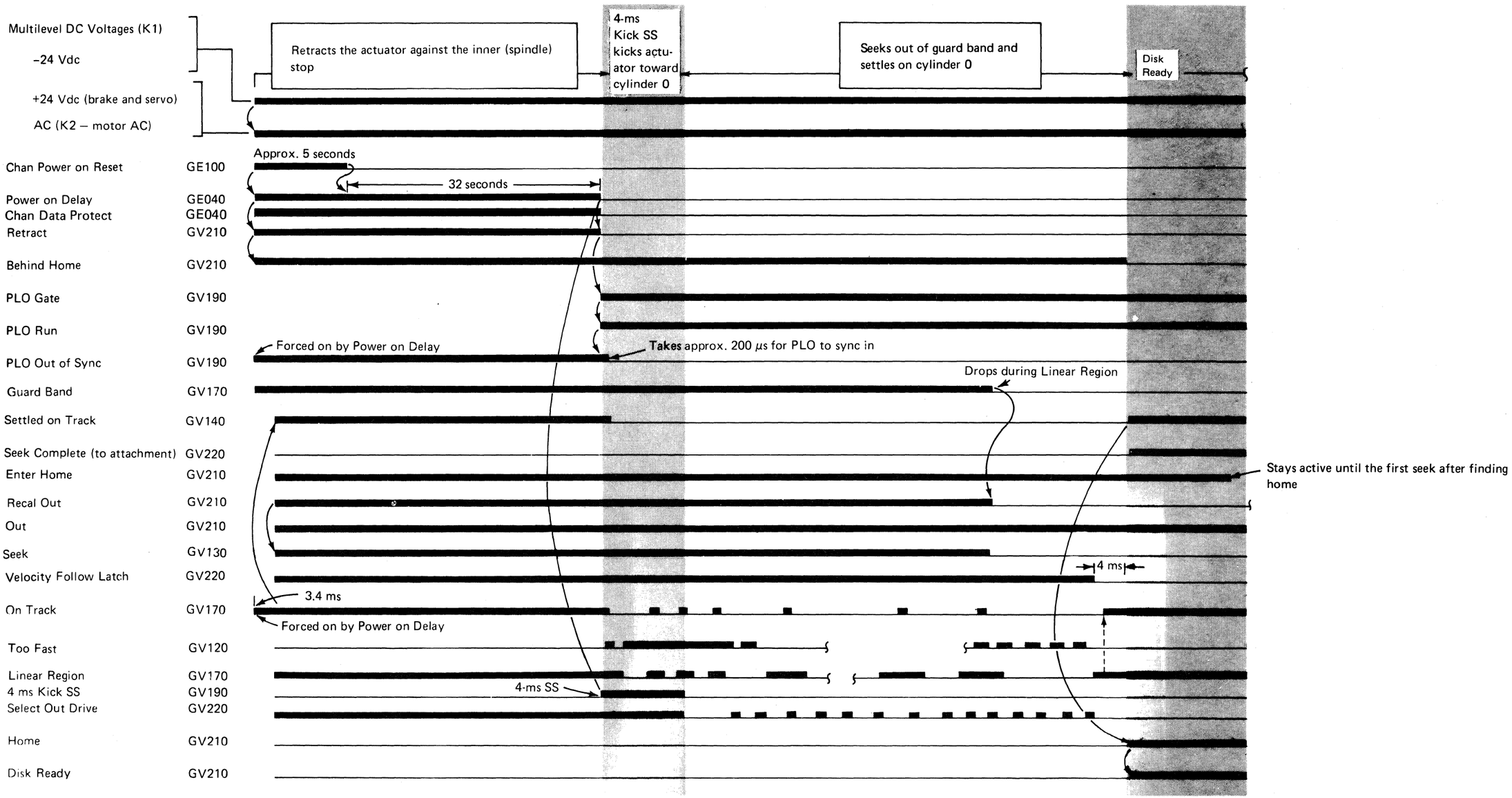
During all power-off conditions, the actuator arm is retracted against the inner (spindle) stop by the +24 Vdc power supply through the actuator coil or the retract capacitor (N). A magnetic catch holds the actuator in the retracted position. If the disk speed drops below 1,800 revolutions per minute, the 'speed OK' latch (P) is reset and the file goes not ready. The actuator is retracted so the heads will stop in contact in the landing zone.

Note: The 'power on delay' line is dot ORed with the 'chan data protect' line on 62EH I/O boards. Any device that requires channel data protect on 62EH systems will not operate until after the 32-second power on delay.



[1] These circuits are in the disk drive B attachment. All other circuits are the same in both attachments.

Power On and Seek Home

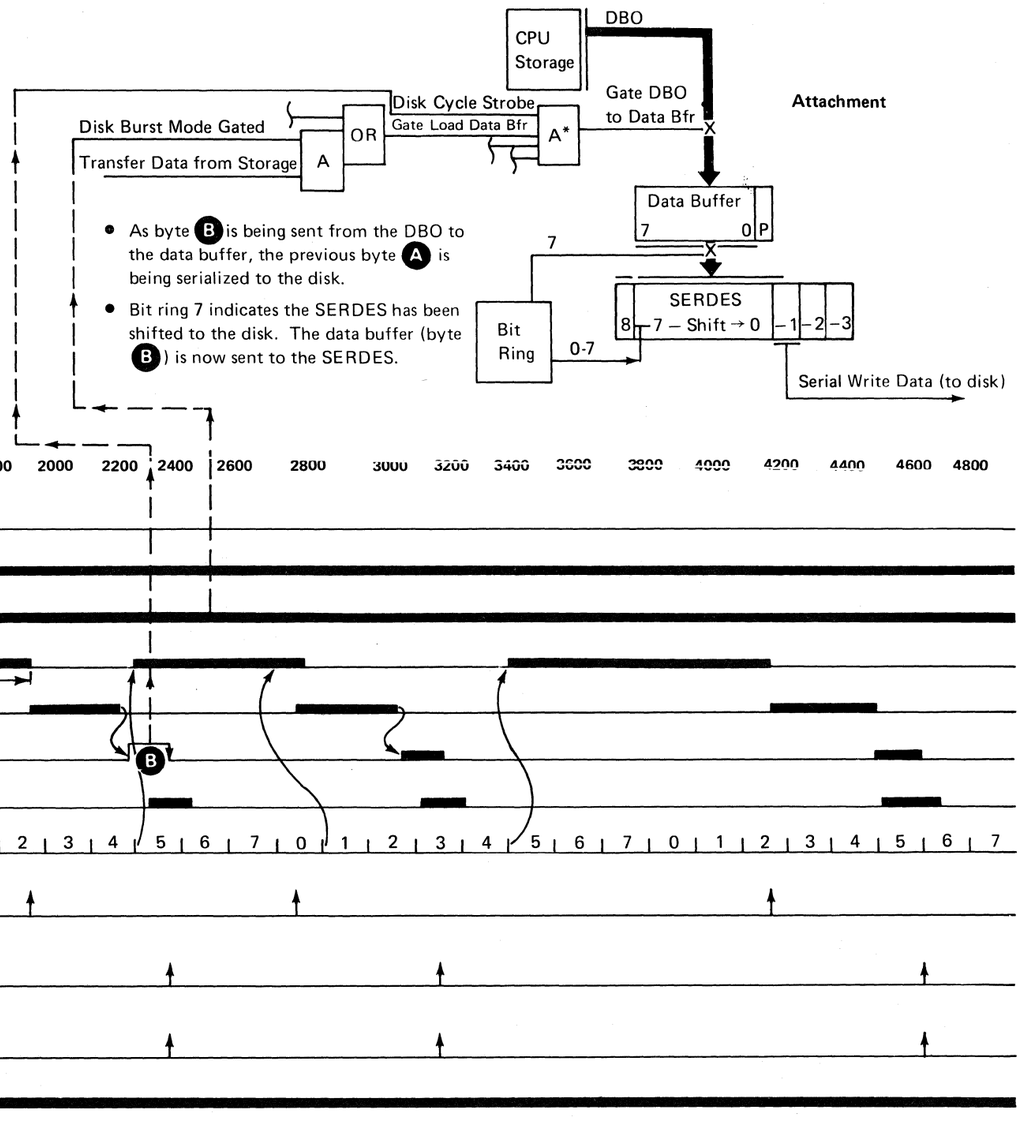


Cycle Steal

Cycle Steal from the Control Processor

During a disk read, disk write, or disk scan operation, data is sent from the control processor to the disk attachment. This data is sent in burst mode; that is, the 'disk drive A block proc clock' line from the disk attachment to the control processor prevents the control processor from starting any operations until the 'disk drive A block proc clock' line is de-activated. When the 'disk drive A block proc clock' line is active, cycle steals are not given to any other device.

For more information on cycle steal, see *Burst Cycle Steal Mode* under *Operations* in the *Channel* section of this manual.



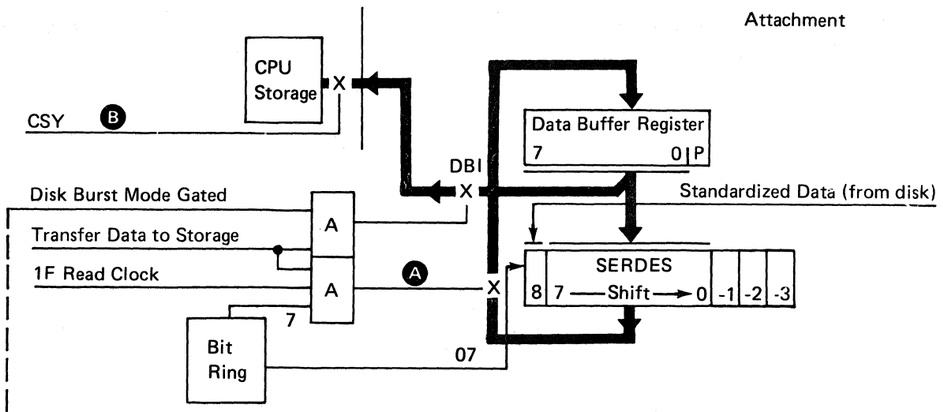
[1] For disk drive B, see GF400.

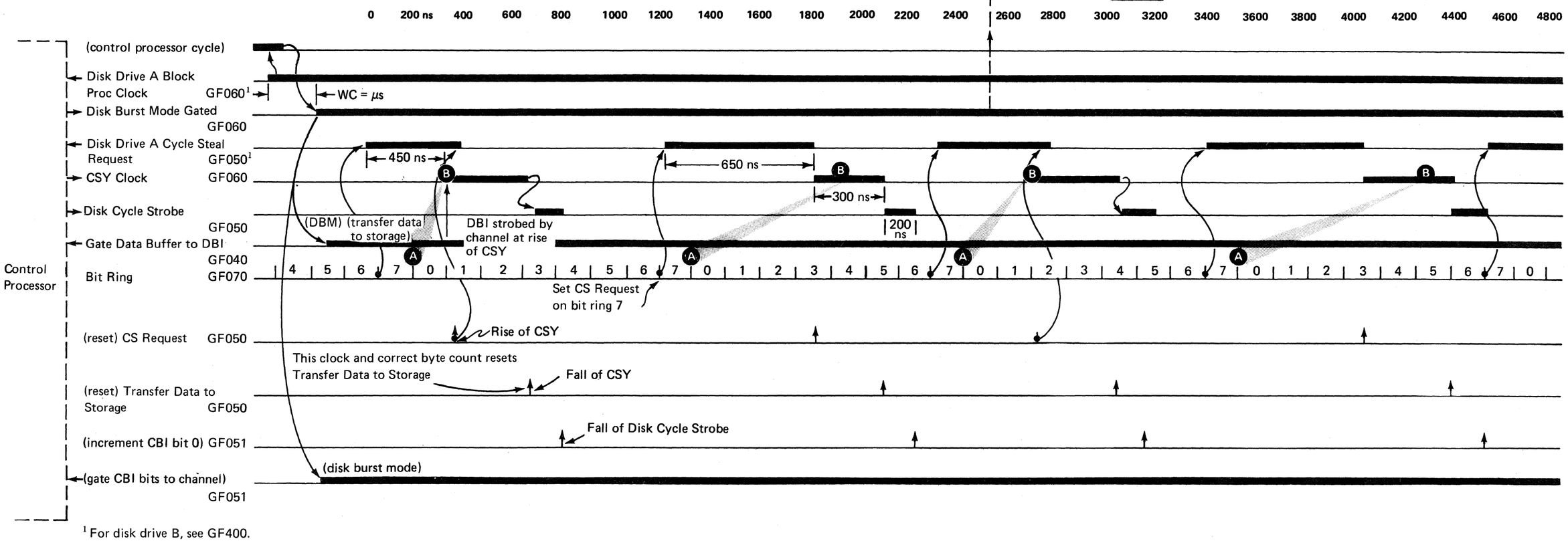
Cycle Steal to the Control Processor

During a disk read, disk write, or disk scan operation, data is sent to the control processor from the disk attachment. This data is sent in burst mode; that is, the 'disk drive A block proc clock' line from the disk attachment to the control processor prevents the control processor from starting any operations until the 'disk drive A block proc clock' line is de-activated. When the 'disk drive A block proc clock' line is active, cycle steals are not given to any other device.

A byte is gated serially to the serializer/deserializer, and then gated (A) to the data buffer register. The byte is then sent to the control processor (B).

For more information on cycle steal, see *Burst Cycle Steal Mode* under *Operations* in the *Channel* section of this manual.



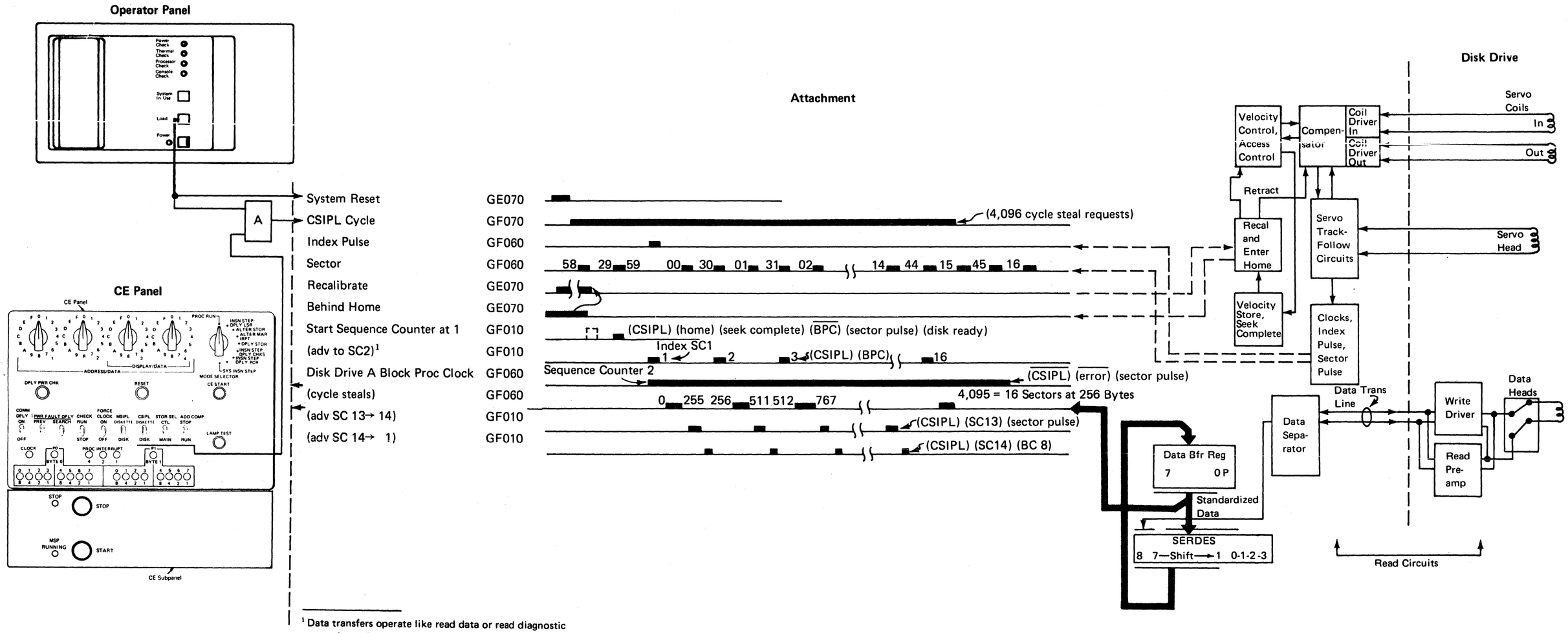


[1] For disk drive B, see GF400.

Control Storage Initial Program Load

Pressing the Load switch on the operator panel starts the CSIPL, which starts an immediate recalibrate to home (cylinder 0). This is followed by the loading of sectors 0 through F (2,048 words) from cylinder 0, head 0 into control storage addresses 0 through 400 (hexadecimal). This data transfer from disk operates in the same manner as the read data operation, except the sector ID fields are not cycle stealed from the control processor or compared in the disk attachment.

For more information on CSIPL, see the *Control Processor* section of this manual.



[1] Data transfers operate like read data or read diagnostic operations. Sector hit is forced.

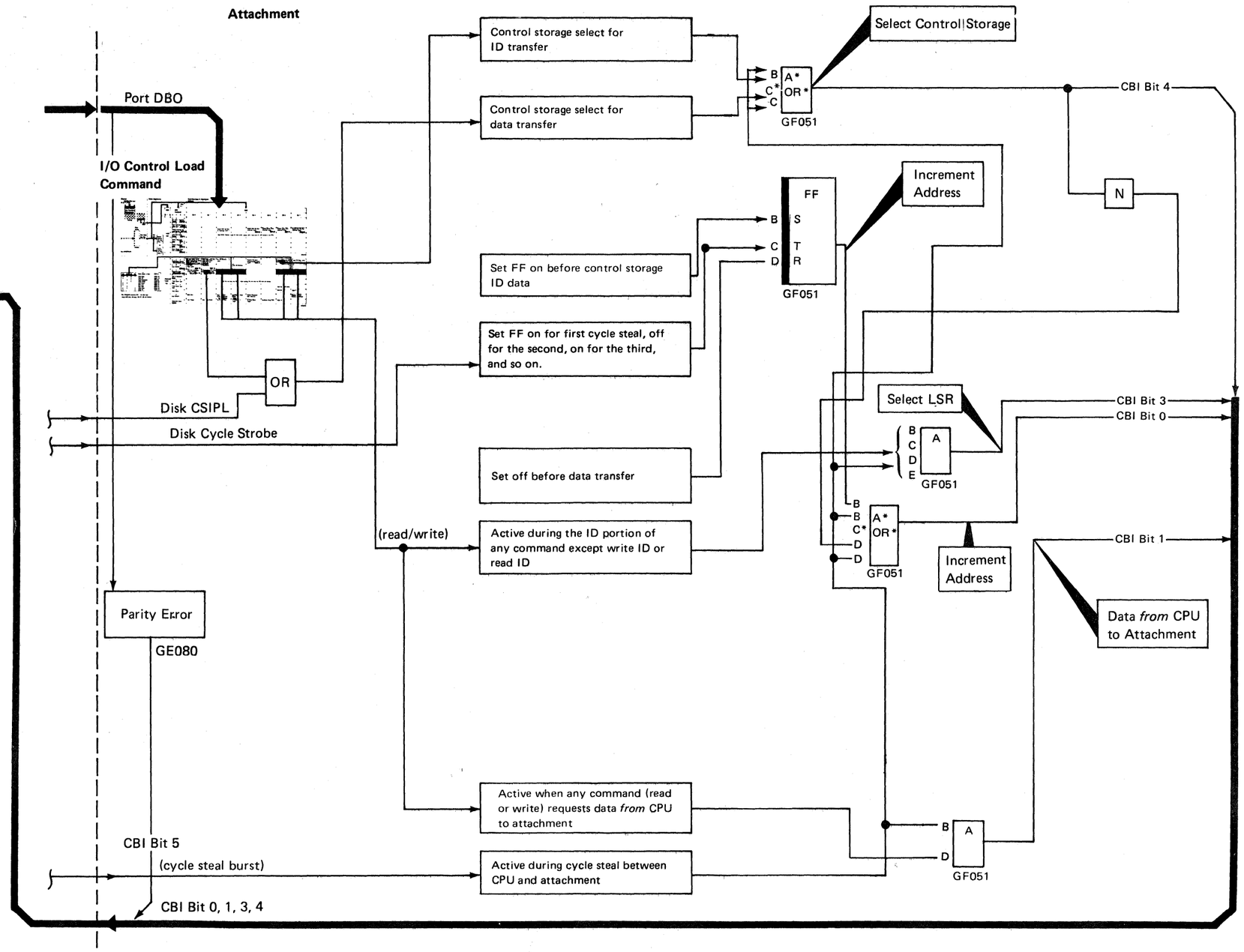
Command Bus In

Before a read or write operation between the control processor and the disk is executed, an I/O control load command sets the desired data bus in control circuits in the disk attachment. The control circuits select the desired command bus in configuration and send it back to the control processor, therefore controlling data and addressing between the control processor and attachment during the cycle steals that follow.

Command Bus In

Bits 0 1 3 4 5

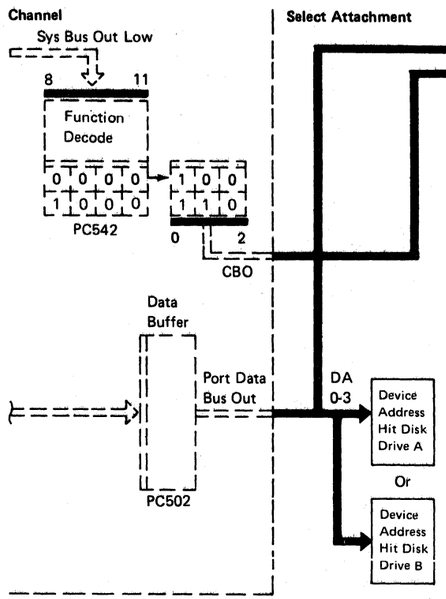
- 0 0 = Cycle steal data to CPU — no increment to MAR.
- 0 1 = Cycle steal data from CPU — no increment to MAR.
- 1 0 = Cycle steal data to CPU — increment MAR.
- 1 1 = Cycle steal data from CPU — increment MAR.
- 0 = Cycle steal LSR 14 (WR 4 interrupt level 1) select — data field address.
- 1 = Cycle steal LSR 15 (WR 5 interrupt level 1) select — ID field address.
- 1 = Select control storage during cycle steals. Indicates to the CPU not to check parity of DBI during a sense command/jump on I/O condition met.
- 1 = Data bus out parity check.



COMMANDS

I/O Load Command–I/O Control Load Command

These commands send 1 byte of diagnostic, interrupt, or operation control information from the control processor to the disk attachment. See *Commands* in the *Channel* section of this manual for a description of how these commands are executed.



CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
100 I/O Load	0 0 1 0 Set Interrupt Request Level 1								
	0 0 1 1 Reset Interrupt Request Level 1 or 4								
	0 1 1 0 Enable Interrupt Request Control			Enable seek op end on interrupt level 4 (see note 2)		Enable data op end interrupt level 1 (see note 2)	Enable sector pulse interrupt level 1 (see note 2)	Enable index pulse interrupt level 1 (see note 2)	Enable seek op end interrupt level 1 (see note 2)
	1 0 0 1 Load Data Buffer Register	Data buffer register (load the data buffer register with a byte from an LSR located in the CPU).							
	1 0 1 1 Enable Diagnostic Mode (see note 1)								
	1 1 0 0 Disable Diagnostic Mode (see note 1)								
	1 1 0 1 Diagnostic Control Byte 1 (see note 1)								Force file to landing zone
	1 1 1 1 Reset Checks (reset error conditions)								

R6	R7	Q6	Q7	Read, Write, or Scan
0	0	0	1	Read Data
0	1	0	1	Read ID
1	0	0	1	Read Diagnostic
1	1	0	1	Read Verify
0	0	1	1	Scan Equal
0	1	1	1	Scan Low
1	0	1	1	Scan High
0	0	1	0	Write Data
0	1	1	0	Write ID

110 I/O Control Load	0 0 0 0 Rd/Wr/Scan Control	Set start (initiated read, write, or scan operations)	Reset index pulse and sector pulse (reset latches for next command)	Set 'I/O working' latch					
	0 0 0 1 Seek Control	Set 'seek busy' latch		Recalibrate	Set 'I/O working' latch	Program DC reset (programmed system reset)		1=control storage for ID 0=main storage for ID	(set) 'disk busy' latch
	0 0 1 0 Command Byte	Fast sync extended (1=set, 0=reset)	1=control storage for data 0=main storage for data	R6	R7			Q6	Q7
	0 0 1 1 Reset Error								Set/reset not valid I/O buffer address error

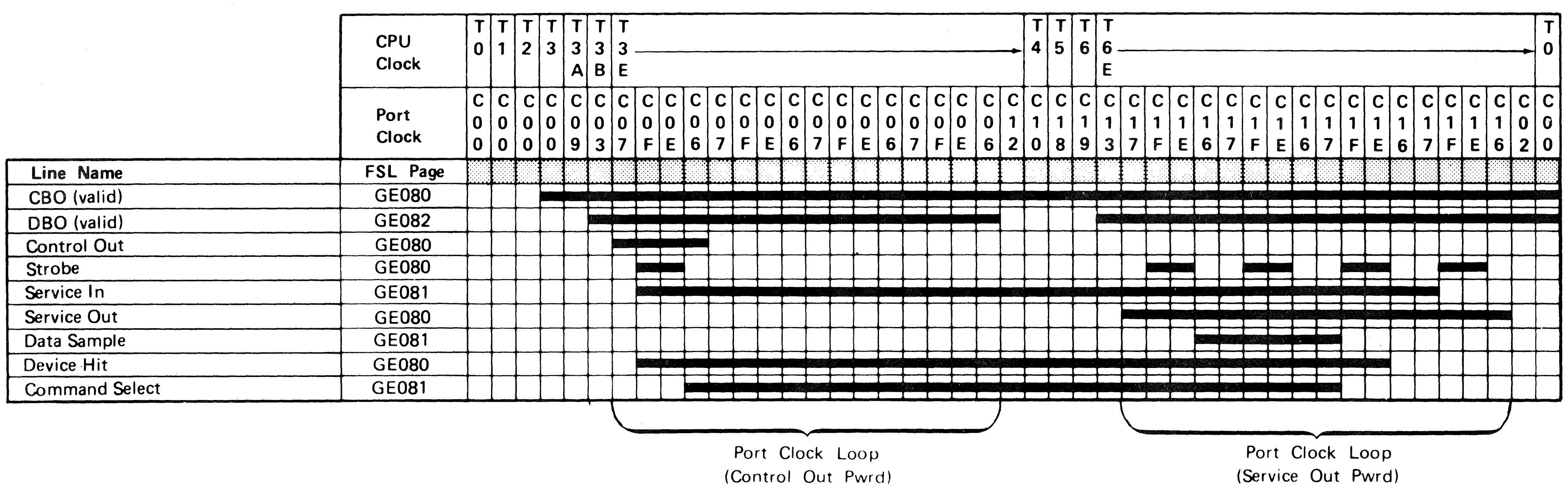
(continued on next page)

(from preceding page)

Notes:

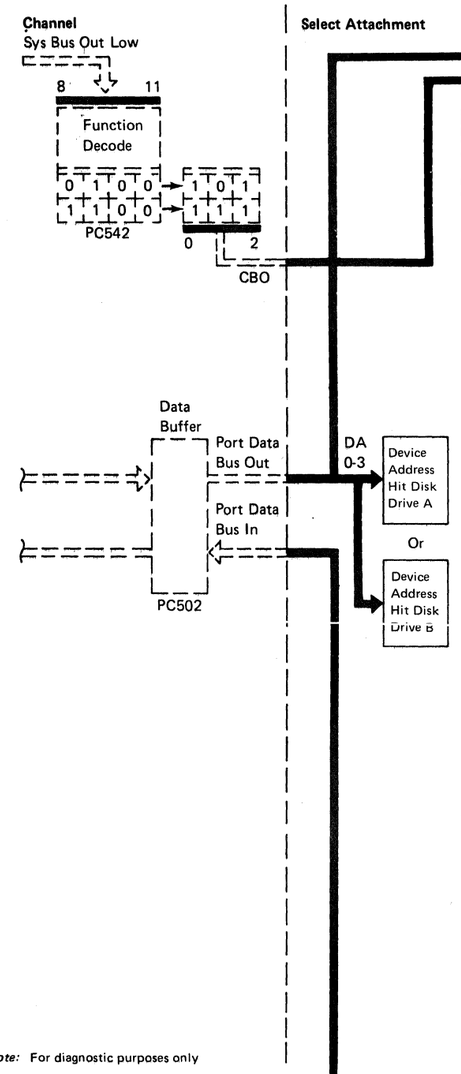
1. The enable diagnostic mode modifier of the I/O load command de-activates the main control lines between the channel and the attachment and between the attachment and the disk drive(s). Then, the diagnostic mode control modifier of the I/O control load command can simulate these main control lines, which permits diagnostic programs to simulate attachment operations.
2. Also enables interrupt time-out.
3. Reset the seek busy, file busy, R6, R7, Q6, and Q7 latches.

CCB	CCB	DBO							
0 1 2	3 4 5 6	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
	0 1 1 0 End of Operation Reset (see note 3)								
	1 0 0 0 Track Counter Low Byte	Load this low byte first because when loading this low byte the high byte can change.							
	1 0 0 1 Track Counter High Byte					High byte of track counter			
	1 0 1 0 Head Select							Head select bit 2	Head select bit 1
	1 0 1 1 Seek Control	Start seek		Seek direction: 0=higher cylinder 1=lower cylinder	Odd/even cylinder: 0=odd 1=even	Enable diagnostic seek interrupt			Diagnostic track counter decrement
	1 1 1 0 Diagnostic Mode Control (see note 1)	CSY trigger	Disk cycle strobe and advance byte counter 16	Set sector pulse	1F read clock toggle	1F read clock toggle	Set/reset read data	Index pulse	Diagnostic reset



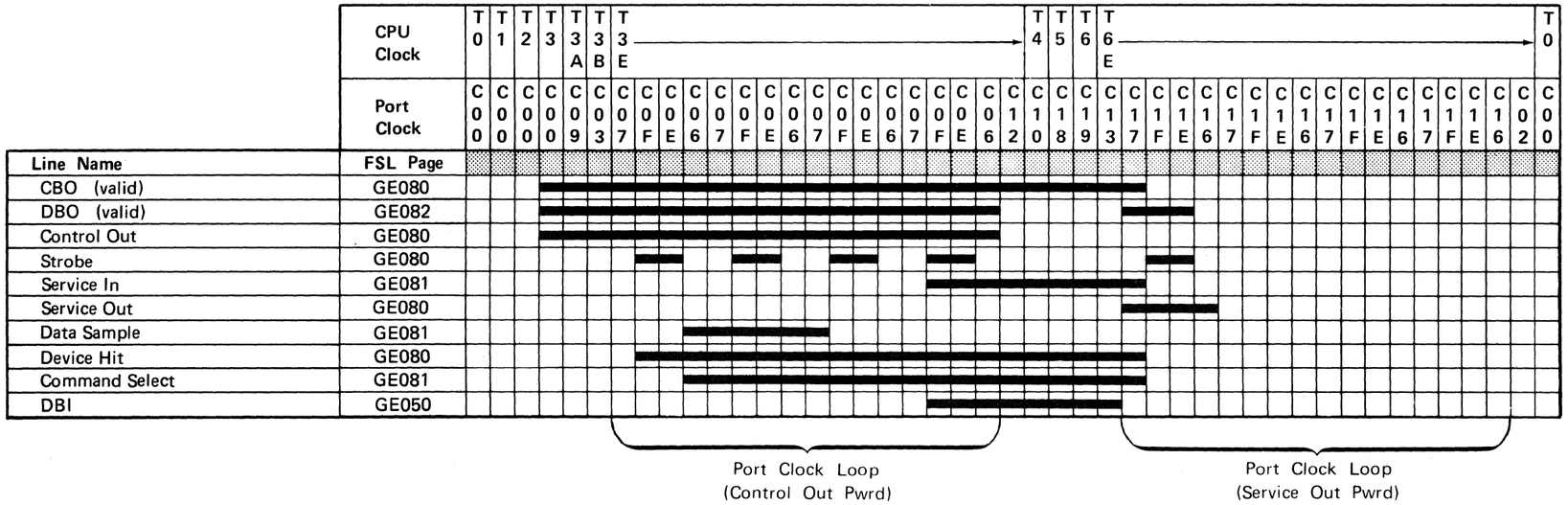
I/O Sense Command–I/O Control Sense Command

These commands send 1 byte of status, interrupt, or diagnostic information from the disk attachment to the control processor. See *Commands* in the *Channel* section of this manual for a description of how these commands are executed.



CCB 0 1 2	CCB 3 4 5 6	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
101 I/O Sense	0 0 0 0 Status Byte 0	Disk not ready		Sector sync check	Off-track check	CRC check	DBO parity check	Write data echo check	Cycle steal overrun
	0 0 0 1 Status Byte 1	No operation	Data unsafe	Not valid seek address	Attachment check	No record found	Scan equal hit	Scan not hit	Seek check
	0 0 1 0 Status Byte 2	SERDES check	Write check	Channel transfer check	PLO out of sync check	Interrupt time-out	Behind home		Sector check
	0 0 1 1 Diagnostic Byte (see note)	Position 9	CRC generate positions						Position 16
	0 1 1 0 Interrupt Condition			Seek op end on interrupt level 4	Interrupt time-out	Data op end enabled-op end latch	Sector enabled–sector pulse latch	Index enabled–index pulse latch	Seek op end on interrupt level 1
	1 0 0 1 Data Buffer	Data buffer register	(Send data buffer register contents to an LSR located in the CPU.)						
111 I/O Control Sense	0 0 0 0 Diagnostic Sense (see note)	Too fast	Home	Speed pulse	On track				
	0 0 1 0 Diagnostic Sense (see note)					Op end latch	Sector pulse latch	Power on reset latch	Index pulse latch
	0 1 0 0 Diagnostic Sense (see note)	SERDES bit 0	Byte counter 4	Byte counter 256	Sequence counter 3	Sequence counter 6	Bit ring 1	(not) cycle steal request trigger	(not) delay write data
	0 1 0 1 Diagnostic Sense (see note)	Scan hit latch	SERDES parity trigger	Sequence counter 4	Push mode	Pull mode	File fast sync	Bit ring 0	CRC counter 8
	0 1 1 0 Diagnostic Sense (see note)	Second drive installed	Head select unsafe	Write unsafe (write error)	Brake failure	Servo unsafe (servo error)			Disk capacity 0 = 8.6 megabytes 1 = 13.2 megabytes
	0 1 1 1 Diagnostic Sense (see note)	(not) file guard band	(not) VFL (velocity follow latch)	(not) select out drive (seek out)	(not) select in drive (seek in)	File fast sync (wrap)	(not) linear region	Read/write select (wrap)	
	1 0 0 0 Diagnostic Sense					Digital-to-Analog Converter Bits			
	1 0 0 1 Diagnostic Sense					Bit 1 Bit 5	Bit 2 Bit 6	Bit 3 Bit 7	Bit 4 Bit 8
	1 0 1 0 Head Select	Not valid I/O buffer address				Settled on track	On track	(not) head select latch Bit 2	Bit 1
	1 0 1 1 Diagnostic Sense					Even track	Seek in	Seek	PLO gate

Note: For diagnostic purposes only


CPU Clock
T0 T1 T2 T3 T3A T3B T3E T4 T5 T6 T6E T0
Port Clock
C00 C000 C000 C000 C009 C003 C007 C00F C00E C006 C007 C00F C00E C006 C007 C00F C00E C006 C007 C00F C00E C006 C012 C110 C118 C119 C113 C117 C11F C11E C116 C117 C11F C11E C116 C117 C11F C11E C116 C117 C11F C11E C116 C002 C000
Line Name
FSL Page
CBO (valid) GE080
DBO (valid) GE082
Control Out GE080
Strobe GE080
Service In GE081
Service Out GE080
Data Sample GE081
Device Hit GE080
Command Select GE081
DBI GE050
Port Clock Loop (Control Out Pwrd)
Port Clock Loop (Service Out Pwrd)

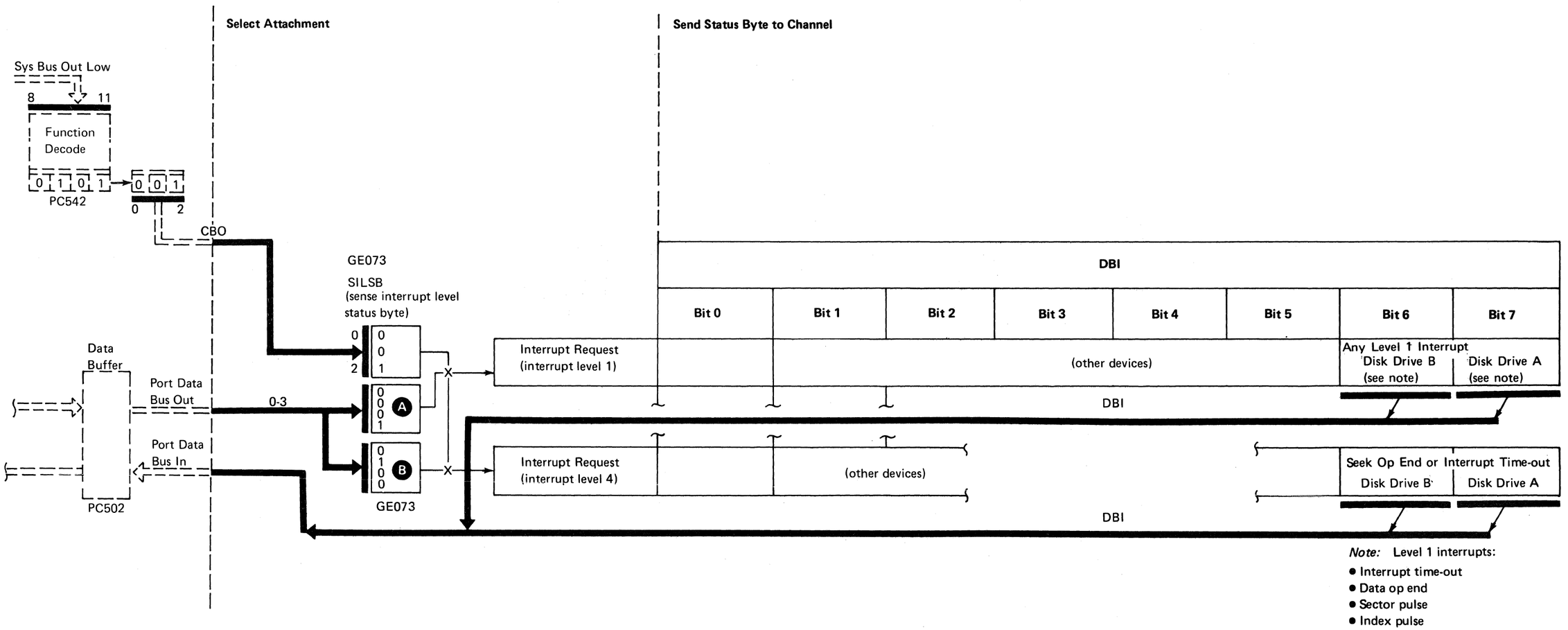
Sense Interrupt Level Status Byte Command

This command senses all interrupt requests on either interrupt level 1 or interrupt level 4. The information sensed by this command indicates which devices are interrupting on the interrupt level specified by the device address. Address 0001 (A) is used when sensing interrupt level 1, and address 0100 (B) is used when sensing interrupt level 4.

The following is an example of an interrupt sequence:

1. The control processor issues an I/O control load command, which enables the desired interrupt.
2. The enabled condition is met, so the attachment activates an interrupt request to the control processor.
3. The control processor issues this SILSB command to determine which device is interrupting, and then passes control to the highest priority device.
4. The control processor issues an I/O sense command to determine the interrupting condition.
5. After the interrupt is processed, the control processor issues an I/O load command to reset the interrupt.

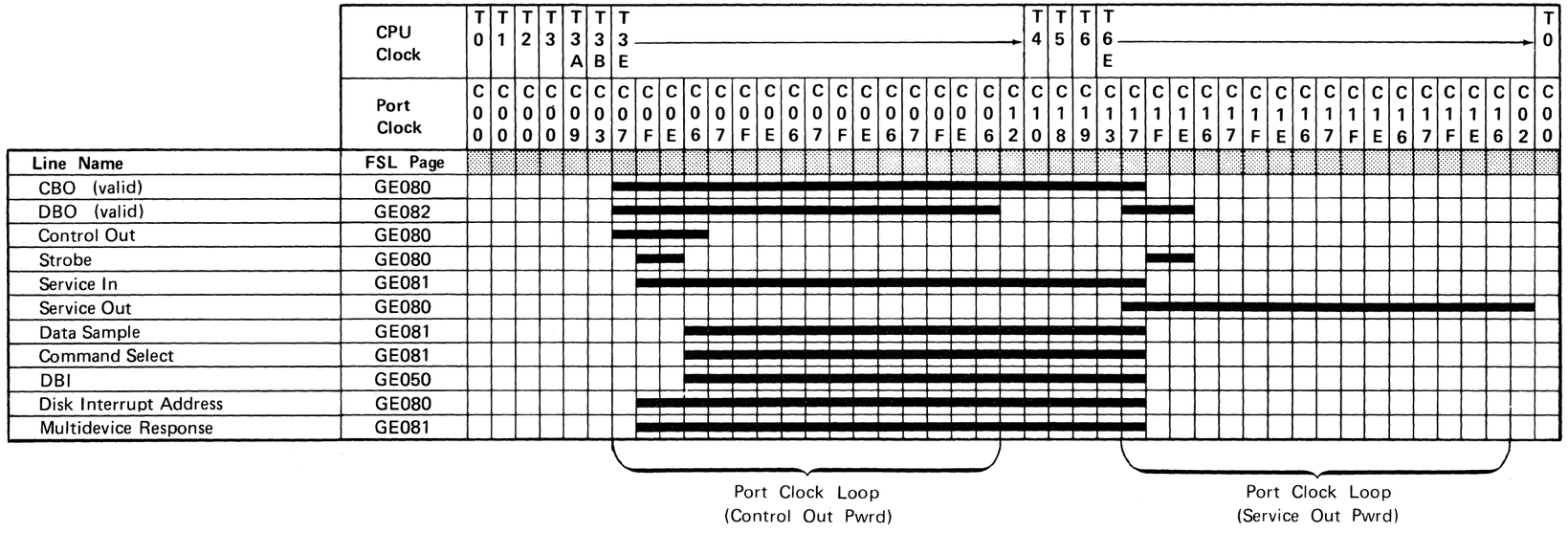
See *Sense Interrupt Level Status Byte* under *Operations* in the *Channel* section of this manual.



Note: Level 1 interrupts:

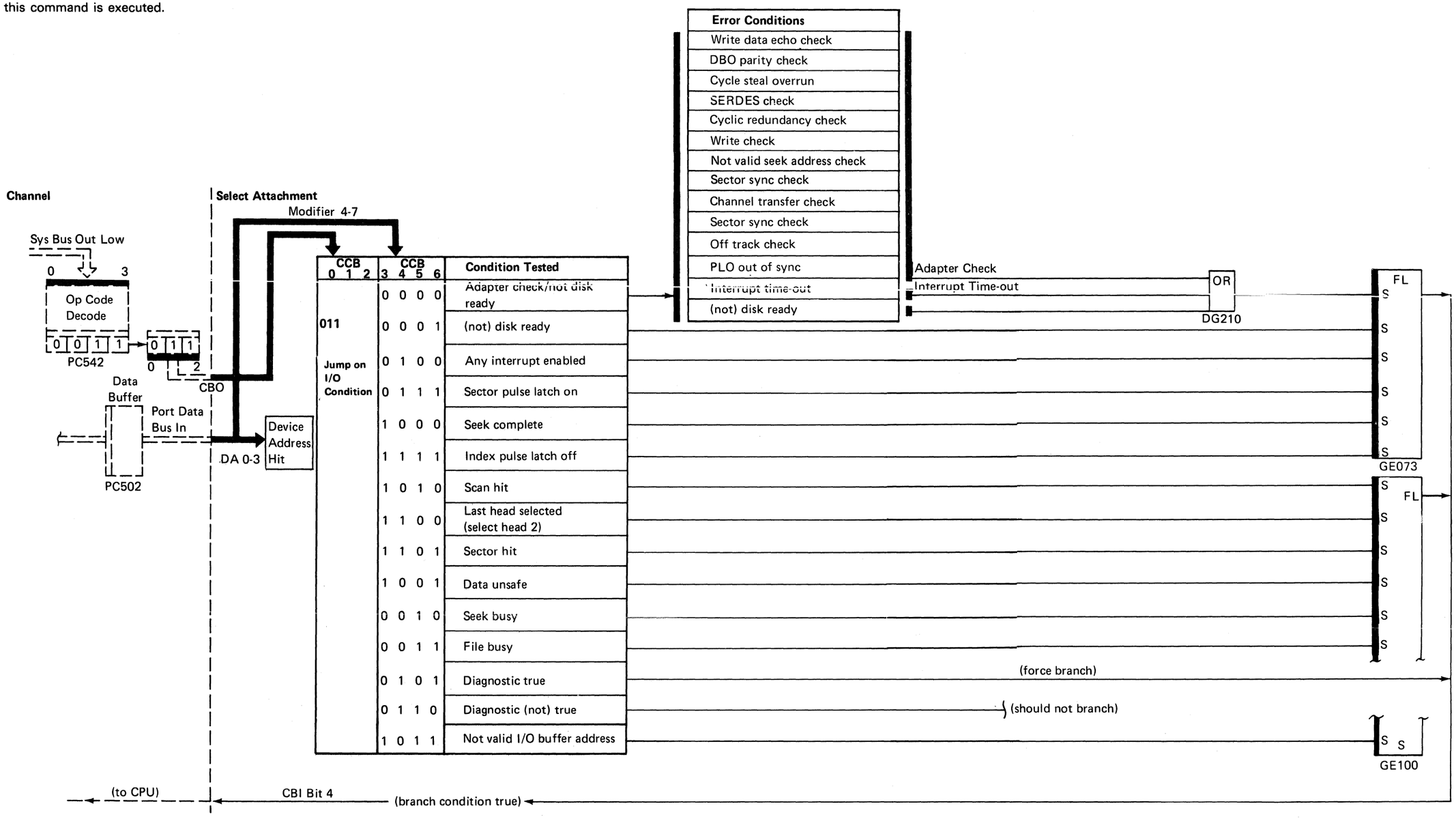
- Interrupt time-out
- Data op end
- Sector pulse
- Index pulse
- Seek op end

For more information, see *Interrupt Time-out Check* later in this section.

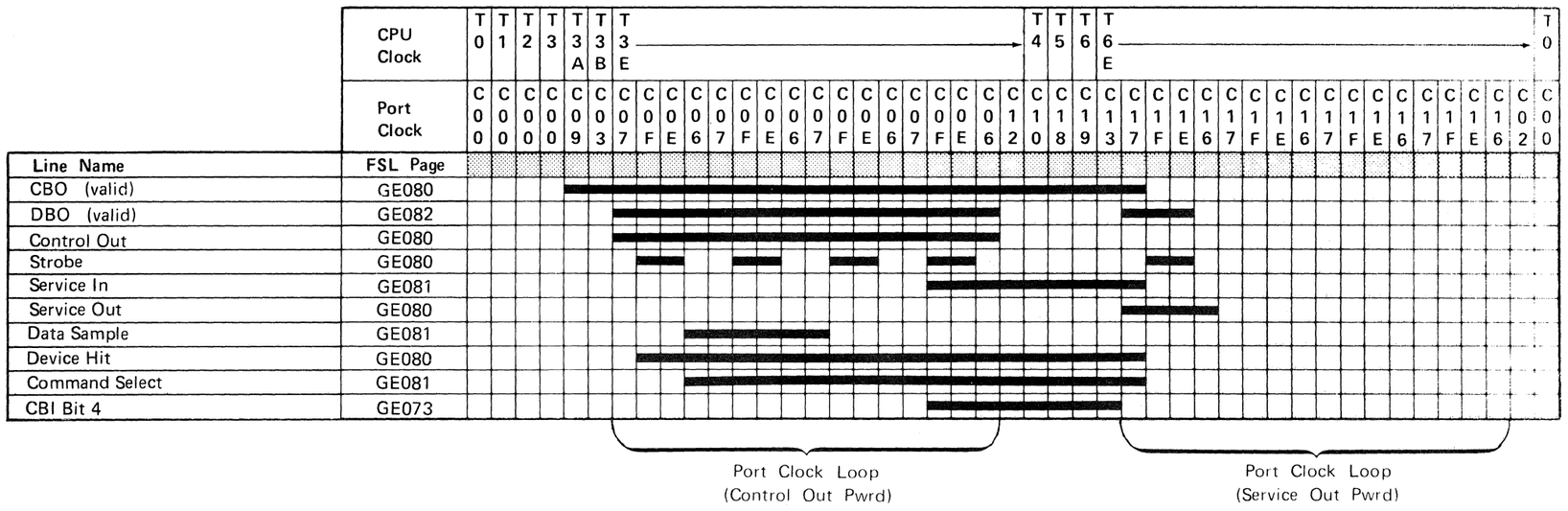

CPU Clock
T0 T1 T2 T3 T3A T3B T3E T4 T5 T6 T6E T0
Port Clock
C000 C000 C000 C000 C009 C003 C007 C00F C00E C006 C007 C00F C00E C006 C007 C00F C00E C006 C012 C110 C118 C119 C113 C117 C11F C11E C116 C117 C11F C11E C116 C117 C11F C11E C116 C117 C11F C11E C116 C102 C000
Line Name
FSL Page
CBO (valid) GE080
DBO (valid) GE082
Control Out GE080
Strobe GE080
Service In GE081
Service Out GE080
Data Sample GE081
Command Select GE081
DBI GE050
Disk Interrupt Address GE080
Multidevice Response GE081
Port Clock Loop
(Control Out Pwrd)
Port Clock Loop
(Service Out Pwrd)

Jump on I/O Command

This command tests the attachment for a specific condition, as shown in this figure. If the condition is active, a positive response is sent to the control processor by activating the 'CBI bit 4' line. See *Commands* in the *Channel* section of this manual for a description of how this command is executed.



Jump on I/O Command (continued)



ERROR CONDITIONS

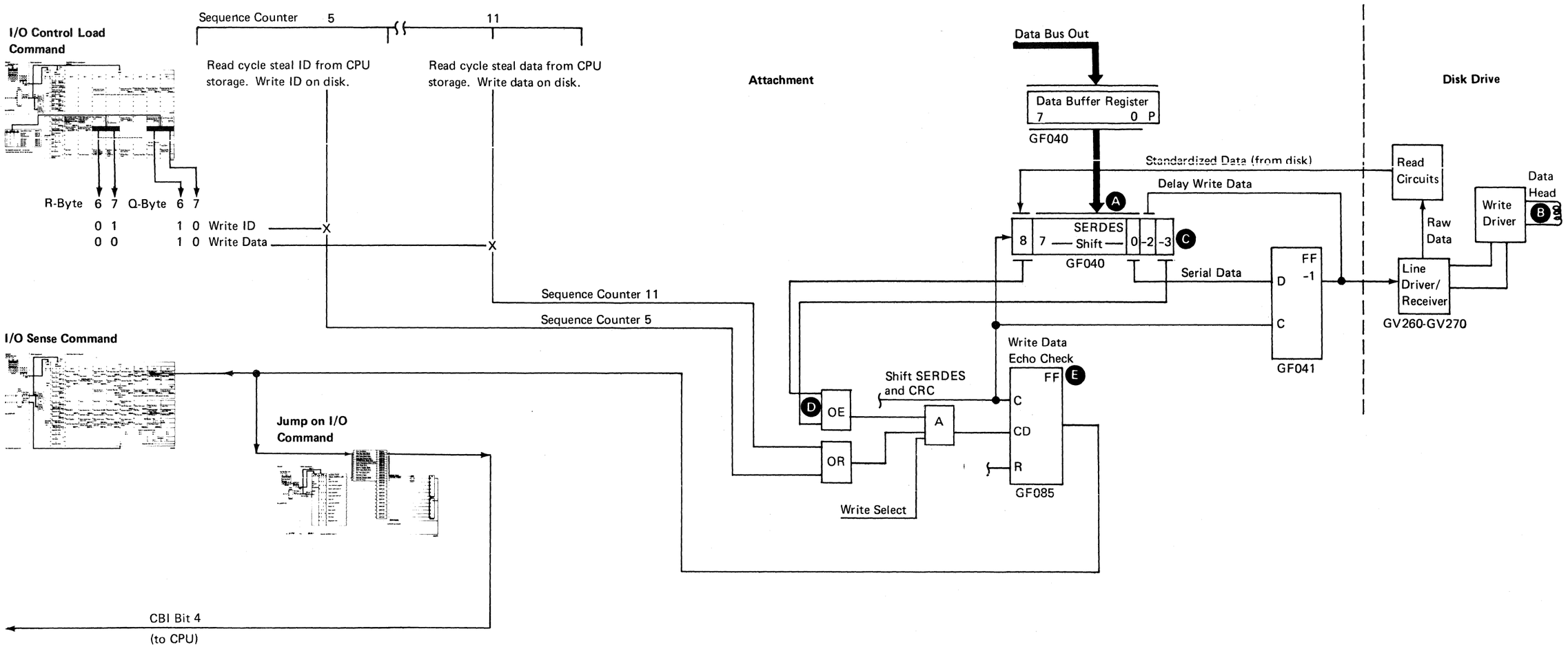
Write Data Echo Check

This check verifies the operation of the data separator. As the write data is being written on the disk, it is also being decoded by the read circuits and returned as standardized data. A 2-bit time delay is generated by this process.

A write data echo check can be indicated during a write identification or write data operation.

As each identification byte or data byte is read from the control processor, it goes to the data bus out, to the data buffer register, and then to the serializer/deserializer (A). The contents of the serializer/deserializer are moved out of position 0 one bit at a time and delayed by one bit time to sync the write data with the write clock. The delayed write data is sent to the data head (B) and written on the disk. It is also sent to the serializer/deserializer position -2 (C).

By the time a bit written on the disk is moved into position -3, the bit should also appear on the 'standardized data' line and serializer/deserializer position 8. The position -3 bit is compared (D) to the serializer/deserializer position 8. If the bits written do not compare with the bits read, the 'write data echo check' FF (E) is turned on.

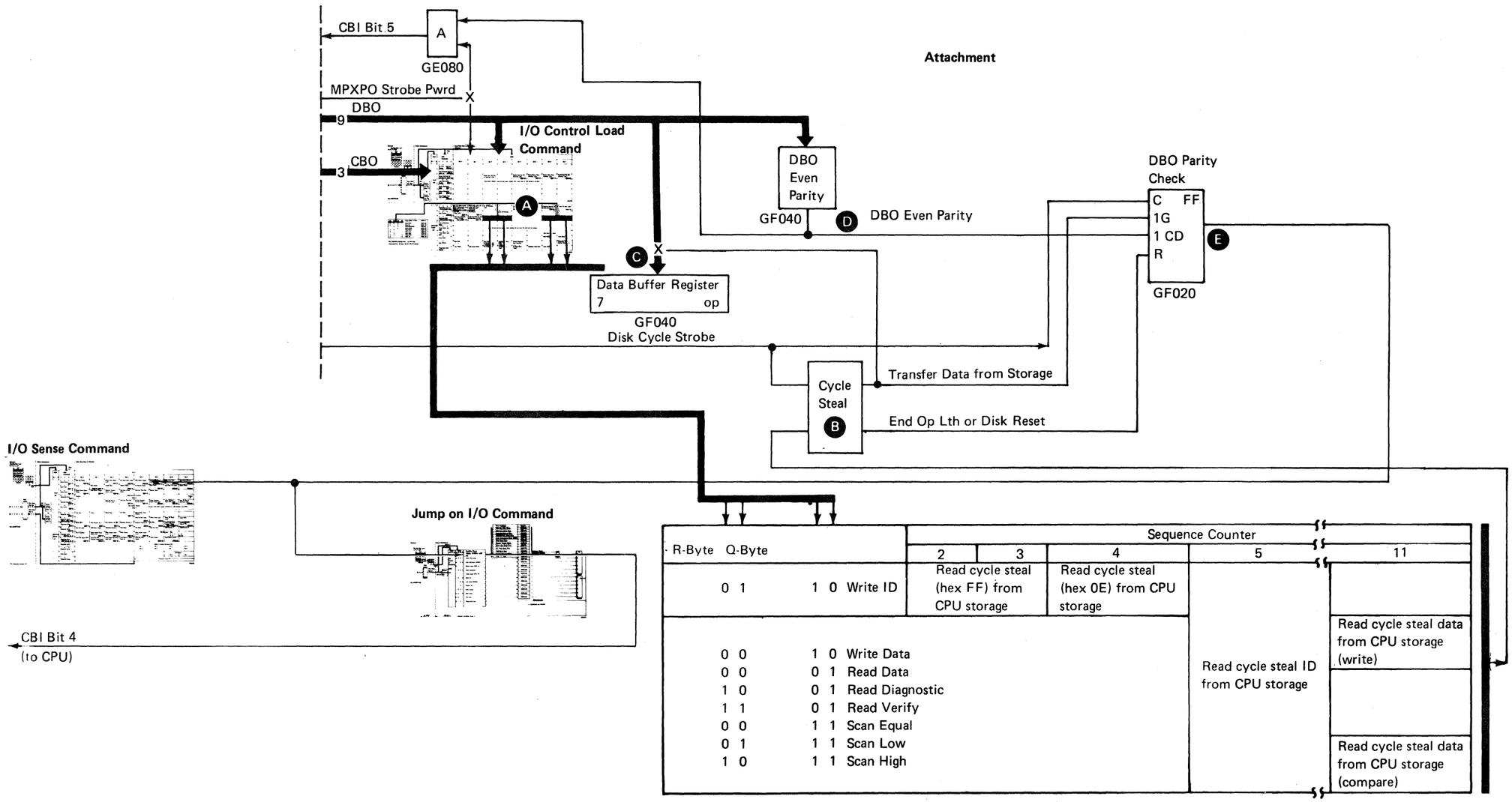


DBO Parity Check

A DBO (data bus out) parity check can be indicated during a cycle steal from either main storage or control storage.

The DBO should be odd parity.

During read, write, or scan data operations (A), data is sent by cycle steal (B) from the control processor to the disk attachment data buffer register (C). If even parity is indicated (D), the 'DBO parity check' FF (E) is activated.



R-Byte	Q-Byte		Sequence Counter 2	3	4	5	11
0 1	1 0	Write ID	Read cycle steal (hex FF) from CPU storage		Read cycle steal (hex 0E) from CPU storage		
0 0	1 0	Write Data				Read cycle steal ID from CPU storage	Read cycle steal data from CPU storage (write)
0 0	0 1	Read Data					
1 0	0 1	Read Diagnostic					
1 1	0 1	Read Verify					
0 0	1 1	Scan Equal					
0 1	1 1	Scan Low					Read cycle steal data from CPU storage (compare)
1 0	1 1	Scan High					

Cycle Steal Overrun Check

During a write operation, each byte from the data bus out is gated (A) to the data buffer register, and then is gated (B) to the serializer/deserializer. A cycle steal overrun occurs when the gating sequence is not correct. A not correct gating sequence occurs:

- When 1 byte has been gated from the data bus out to the data buffer register, but 2 bytes have been gated from the data buffer register to the serializer/deserializer.

- When 2 bytes have been gated from the data bus out to the data buffer register without gating the first byte to the serializer/deserializer.

During a read operation, each byte is gated (C) from the serializer/deserializer to the data buffer register, and then to the data bus in. A cycle steal overrun occurs when the gating sequence is not correct. A not correct gating sequence occurs:

- When 2 bytes have been gated to the data bus in, but no bytes have been gated from the serializer/deserializer.

- When 2 bytes have been gated from the serializer/deserializer without gating the first byte to the data bus in.

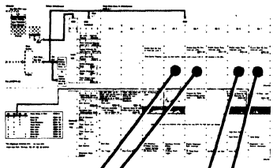
A cycle steal overrun check can be indicated during any read, write, or scan operation.

Overrun Circuit Description

Example 1: During a write identification operation, the head select byte (D) is strobed (E) into the data buffer register (A). Also, the singleshot (F) turns on the FF (G). If the FF is on and the singleshot (F) is fired again before the data register is gated to the serializer/deserializer, a cycle steal overrun (H) is indicated.

Example 2: During a read identification operation, the cylinder select byte is gated from the serializer/deserializer to the data buffer register. A cycle steal is requested (J). The cylinder select byte is strobed (K) to the control processor. Also, singleshot (L) is fired and turns on the FF (G). If the FF is on and the singleshot (L) is fired again before the data buffer register is loaded, a cycle steal overrun (H) is indicated.

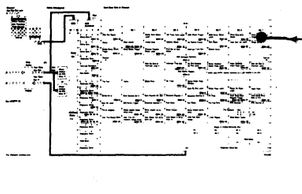
A cycle steal overrun check error condition can be detected when any one of the following read or write operations is transferring ID or data from or to the CPU storage.



I/O Control Load Command

R-Byte	Q-Byte		2	3	4	5	11
0 1	1 0	Write ID	Fr	Fr	Fr	Fr	
0 1	0 1	Read ID				To	
0 0	1 0	Write Data				Fr	Fr
0 0	0 1	Read Data				Fr	To
1 0	0 1	Read Diagnostic				Fr	To
1 1	0 1	Read Verify				Fr	
0 0	1 1	Scan Equal					
0 1	1 1	Scan Low				Fr	Fr/To
1 0	1 1	Scan High					

Sequence Counter



I/O Sense Command

Jump on I/O Command

CBI Bit 4 (to CPU)

Attachment

ID Field: F C C H S

Sequence Counter → 5

Byte Counter → 1 2 3 4 5

Bit Ring → 0 70 70 70 70 7

C H (D) S

Disk Cycle Steal Request

Disk Cycle Strobe (E)

C H

Transfer Data to Storage

Gate Data Buffer to SERDES

F C C H

Gate SERDES to Data Buffer Register

(J) Cycle Steal Request F C C H

Disk

CSY Trg to Channel

CSY Clock

(K) (DBI strobed by channel at rise of CSY)

DBI

Cycle Steal Overrun (H)

FF S1 S2 R — GF021

A A N

FF T1 T2 R N R S (G) — GF021

Transfer Data from Storage

Bit Ring 7

A0 (data buffer register loaded)

A0 (data buffer register unloaded)

SS (F) GF021

SS (L) GF021

DBO

Gate DBO to Data Buffer

(A) X

Data Buffer Register 7 0 P — GF040

Serialized Data (from disk)

X (B)

SERDES 8 7 Shift 0 -1 -2 -3 — GF040

X (C)

Delay Write Data

Disk Drive

Read Preamp

Data Head

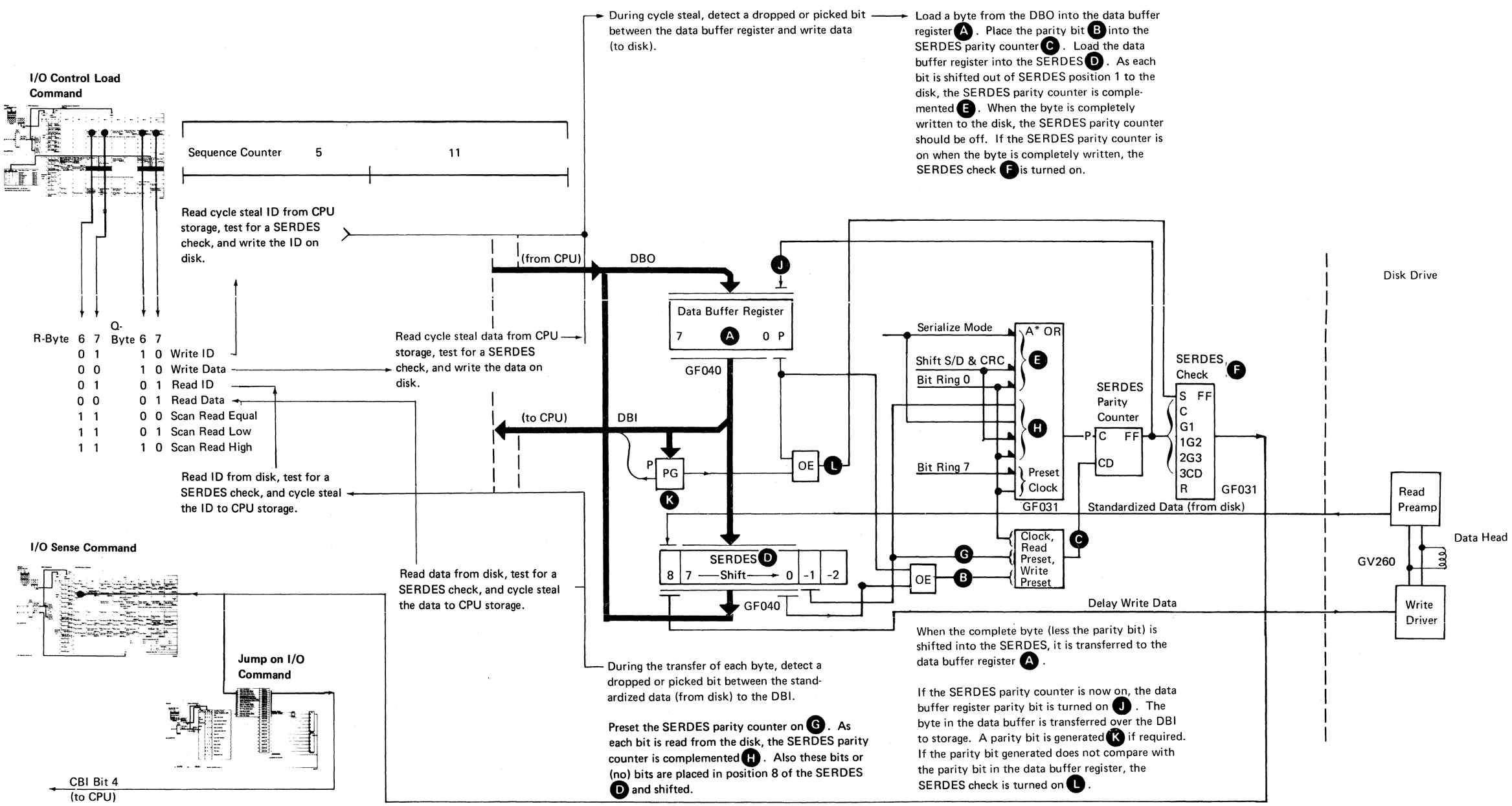
GV260

Write Driver

SERDES Check

The SERDES (serializer/deserializer) check occurs when even parity is detected while moving data through the SERDES.

A SERDES check can be indicated during any read, write, or scan operation.

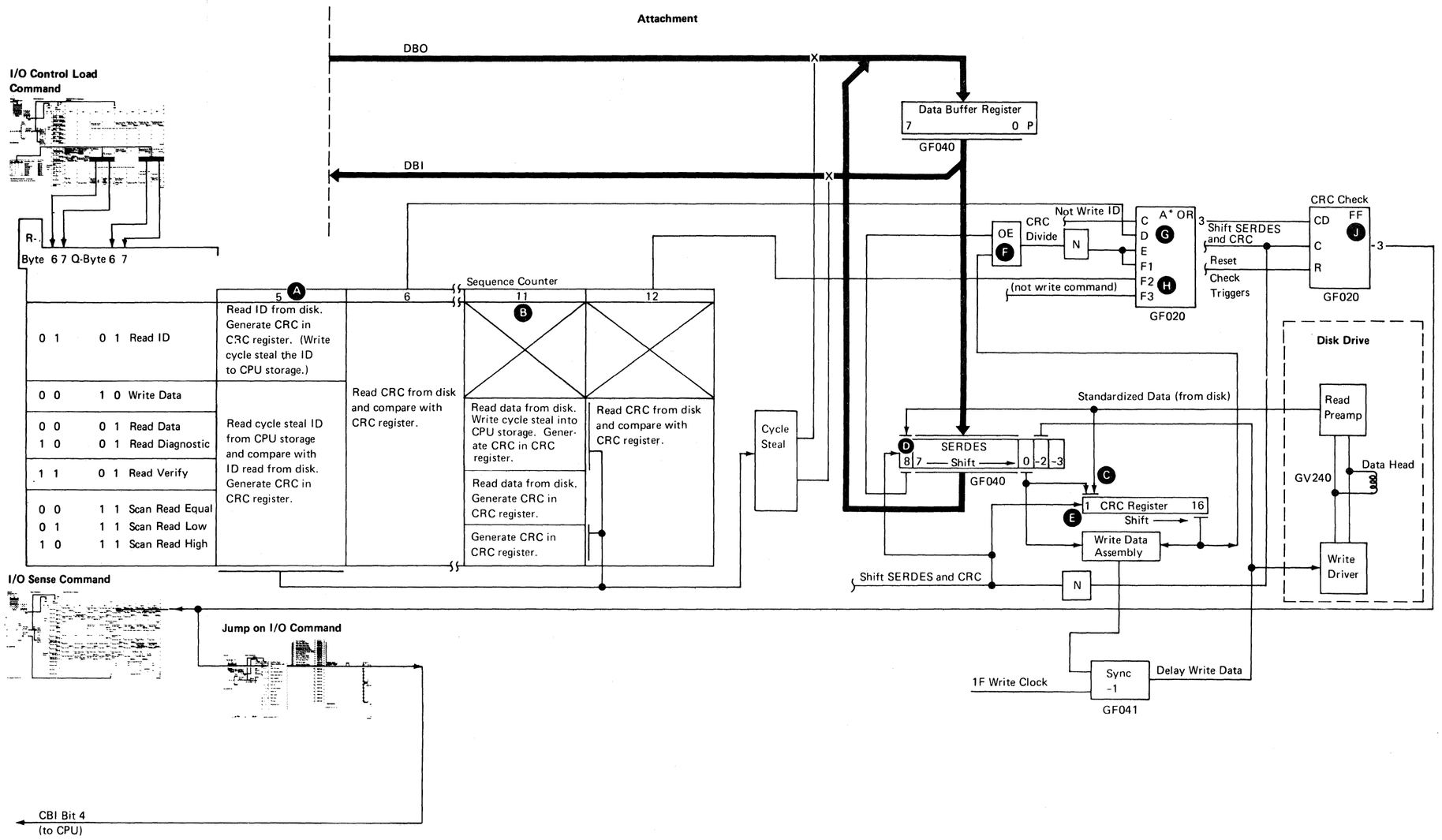


Cyclic Redundancy Check

This check indicates that either the identification cyclic redundancy check character field or the data cyclic redundancy check character field read from the disk did not compare with the cyclic redundancy character generated from either the identification field or the data field from the disk.

A cyclic redundancy check can be indicated during any read, write, or scan operation.

During sequence counter 5 (A) or 11 (B), as identification or data is read from the disk, the cyclic redundancy check character is generated in the cyclic redundancy check register (C). During sequence counter 6 or 12, as the cyclic redundancy check character is read from the disk into serializer/deserializer position 8 (D), the cyclic redundancy check register is out of position 16 (E). The serializer/deserializer position 8 and cyclic redundancy check character register position 16 are compared bit for bit (F). If they do not compare equal during sequence counter 6 (G) or 12 (H), a cyclic redundancy check is indicated (J).



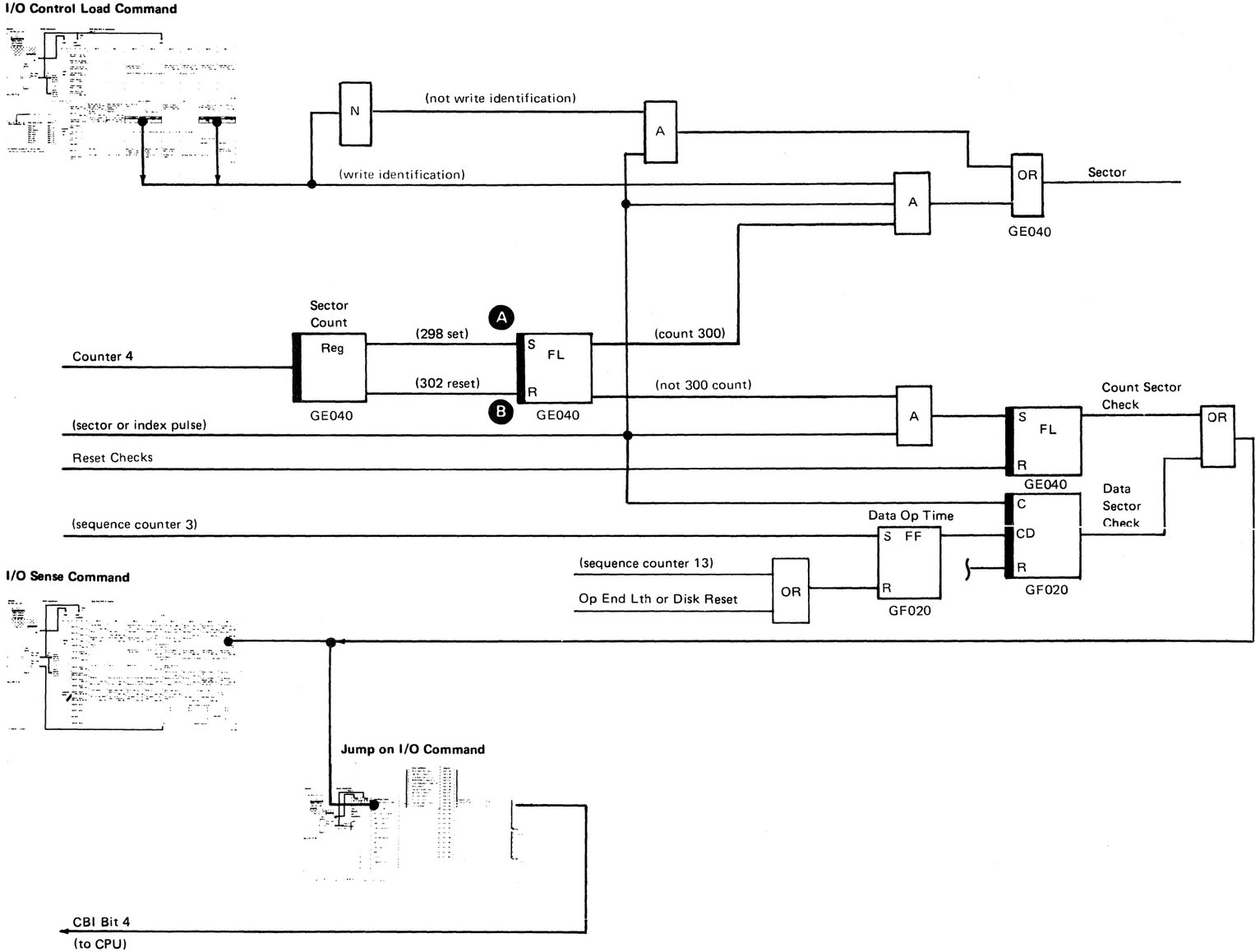
Sector Check

When power is on and the disk drive is turning, the sector check circuit can determine if there is a sector check condition. A sector check is generated if the distance between sectors or between the sector and the index is not 300 bytes. A sector check is also generated if a sector pulse or index pulse occurs while reading, writing, or scanning a sector.

Read data, write data, and scan data operations are active between sequence counter 3 and sequence counter 13. Read identification and write identification operations are active between sequence counter 3 and operation end. If a sector pulse or index pulse occurs during these times, a sector check is generated.

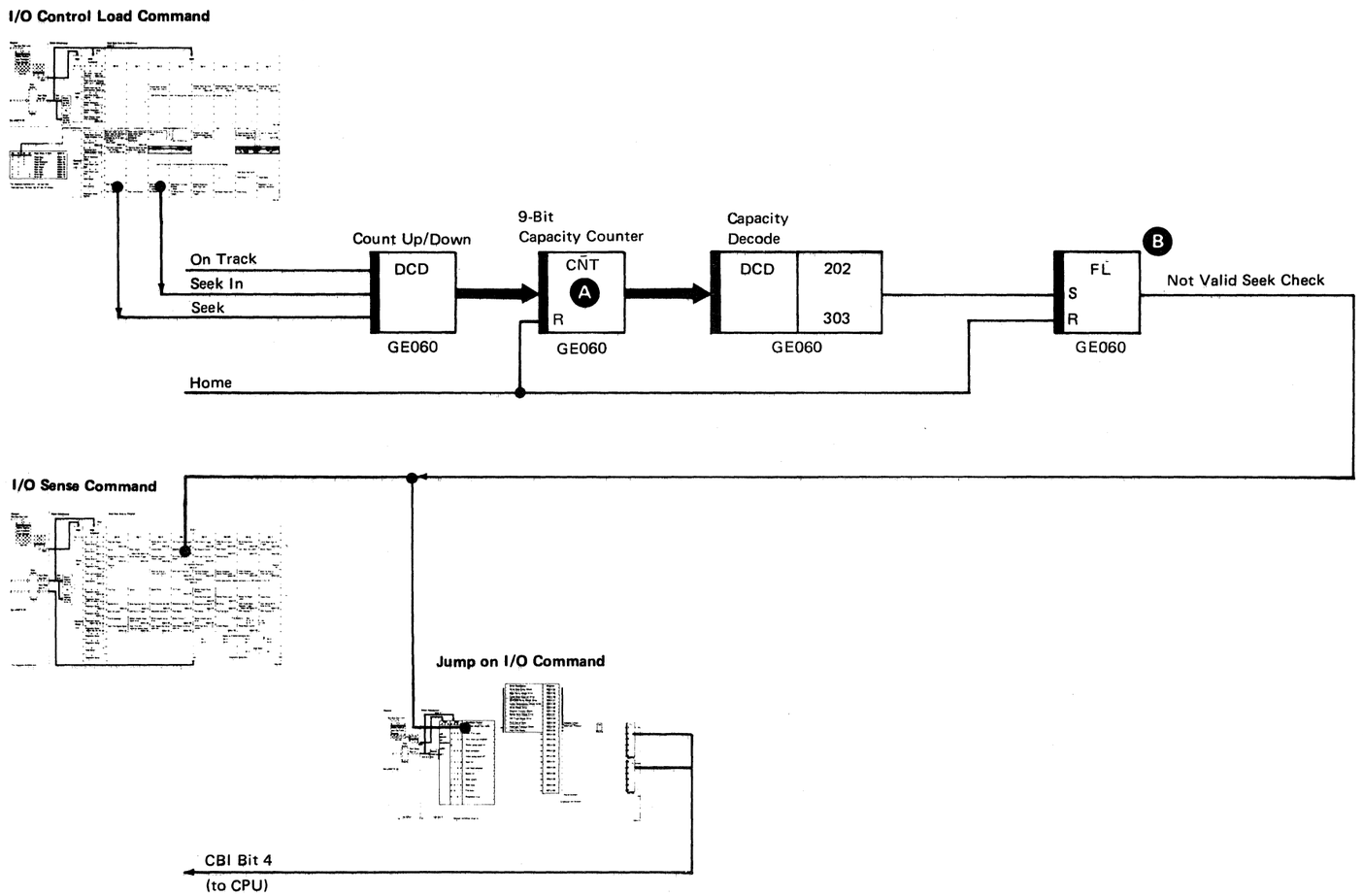
Sector Check Circuit Description

The continuously running phase lock oscillator 'counter 4' pulse is generated at 2-byte intervals. Each 'counter 4' pulse increases the sector counter by 2. At sector byte count 298, the latch is set (A). At sector byte count 302, the latch is reset (B). If a sector pulse or index pulse occurs other than during sector byte count 300, the 'count sector check' line is activated. If a sector check occurs before a write identification operation, the sector pulse to the read and write circuits is de-activated. This prevents the identification field from being written wrongly. The sector check circuit is reset and synchronized after every seek or recalibrate operation.



Not Valid Seek Address

The 9-bit capacity counter (A) contains the number of the cylinder where the actuator is located. The not valid seek address FL (B) is turned on when the 9-bit capacity counter is 202 or larger for an 8.6-megabyte disk or 303 or larger for a 13.2-megabyte disk. The not valid seek address FL keeps the adapter check active. A recalibrate operation is needed to activate home, which then de-activates the adapter check.



Write Check

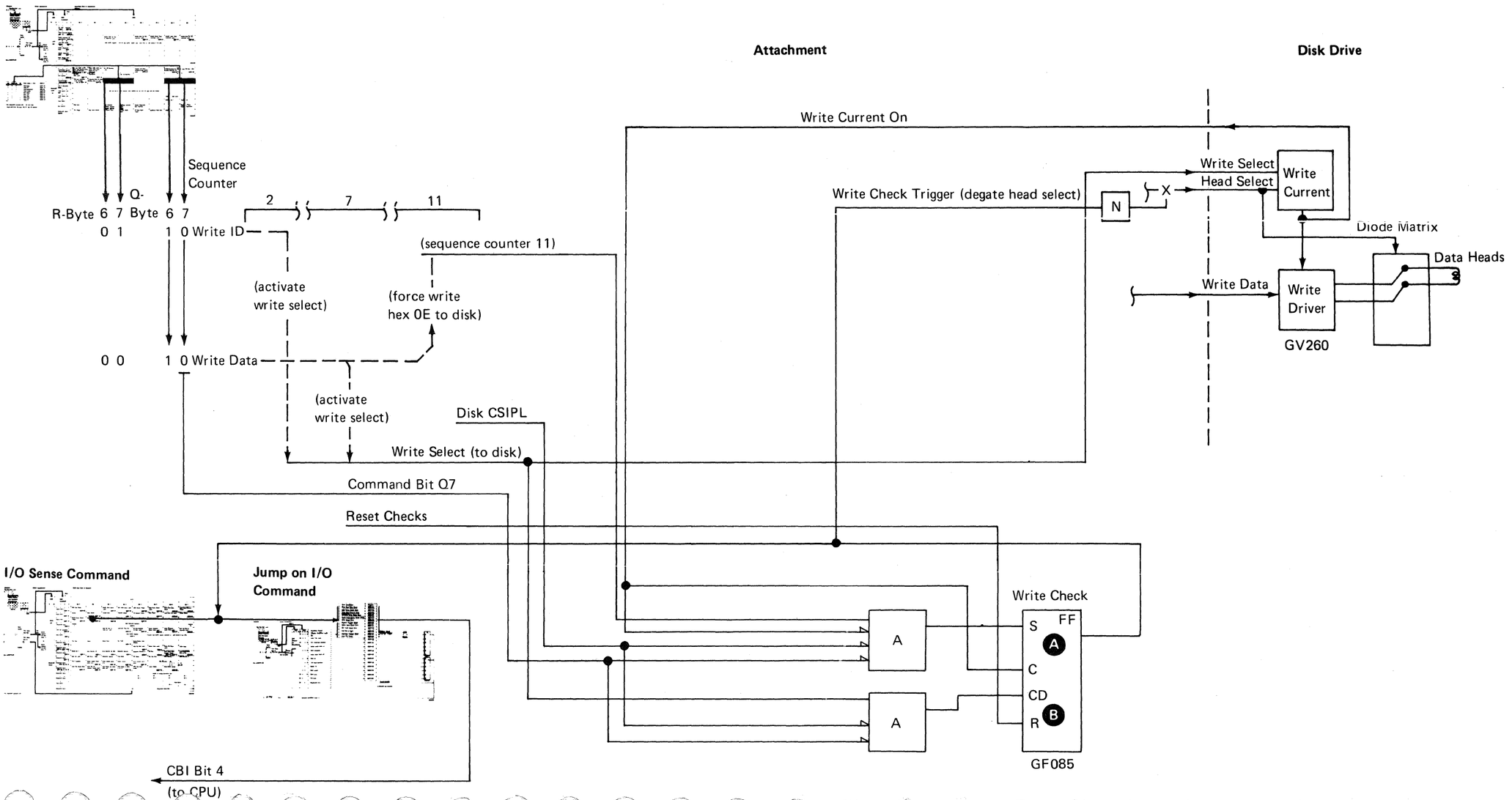
A write check occurs if the 'write current on' line to the data heads is active when it should not be, or if the 'write current on' line to the data heads is not active when it should be.

A write check can be indicated when either a write identification or write data operation is executing.

The 'write current on' line should be active during all write operations, and not active for all other operations.

Write current to the data head is checked in two ways:

- During a write data operation when the data field is being written, the 'write current on' line should be active. If not, a write check is indicated (A).
- If the 'write current on' line comes on during the control storage initial program load cycle and the 'write select' line is not active, or when Q-byte bit 7 is active (indicating a read operation), write check is set (B).

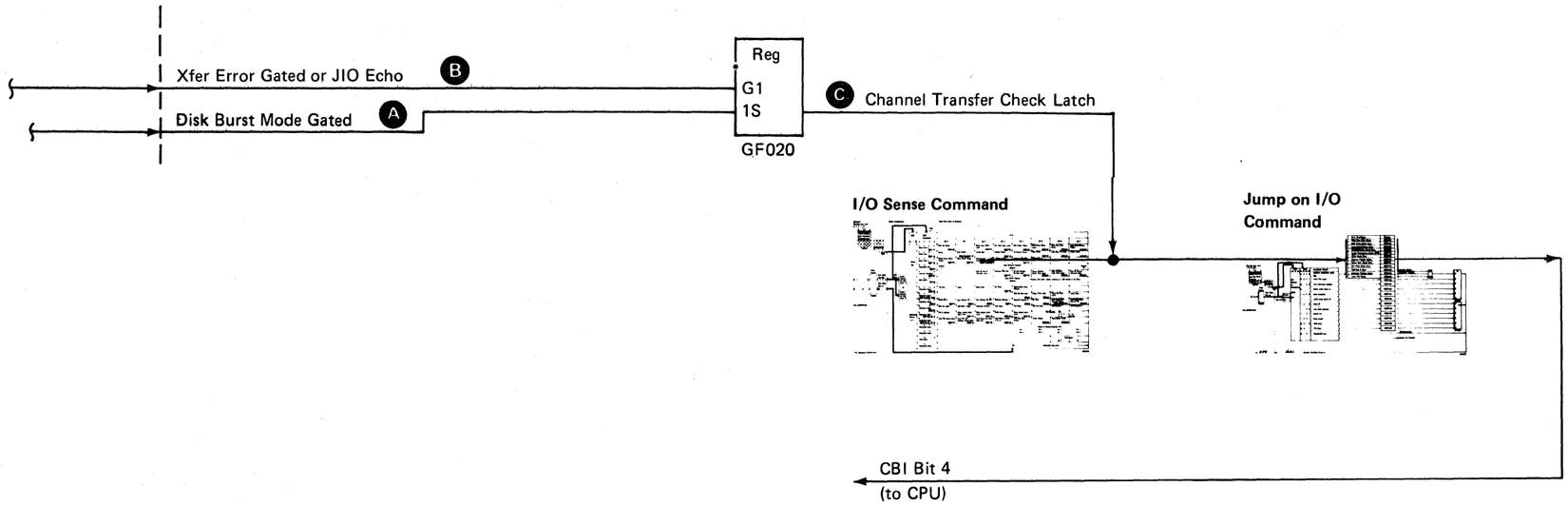


Channel Transfer Check

A channel transfer check indicates a DBI parity error during a cycle steal to the control processor.

A channel transfer check can be indicated during any cycle steal to the control processor.

When a data operation is executing, the 'disk burst mode gated' line (A) is active and cycle steals send data to the control processor. During this time, if a control processor check or channel check occurs (B), a channel transfer check is indicated (C).

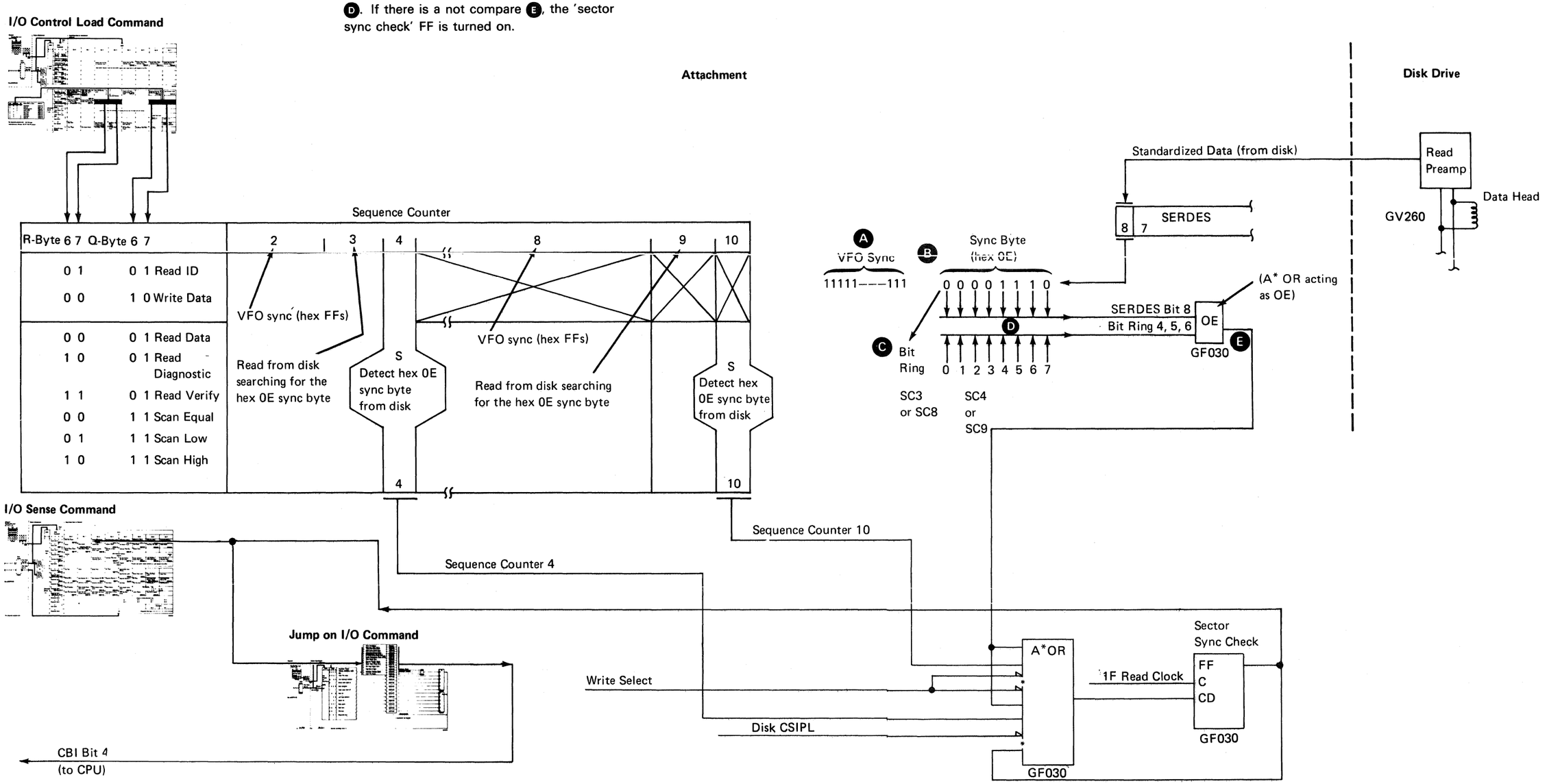


Sector Sync Check

A sector sync check occurs when the sync byte read from the disk does not compare with the hexadecimal 0E byte generated by the bit ring.

A sector sync check can be indicated during any read, write, or scan operation.

The variable frequency oscillator field (hexadecimal FFs) (A) is read from the disk through serializer/deserializer position 8. The first 0-bit (B) during sequence counter 3 or 9 advances the counter to 4 or 10. This also starts the bit ring (C). During bit ring 4, 5, and 6, 1-bits are compared against SERDES bit 8 (D). If there is a not compare (E), the 'sector sync check' FF is turned on.

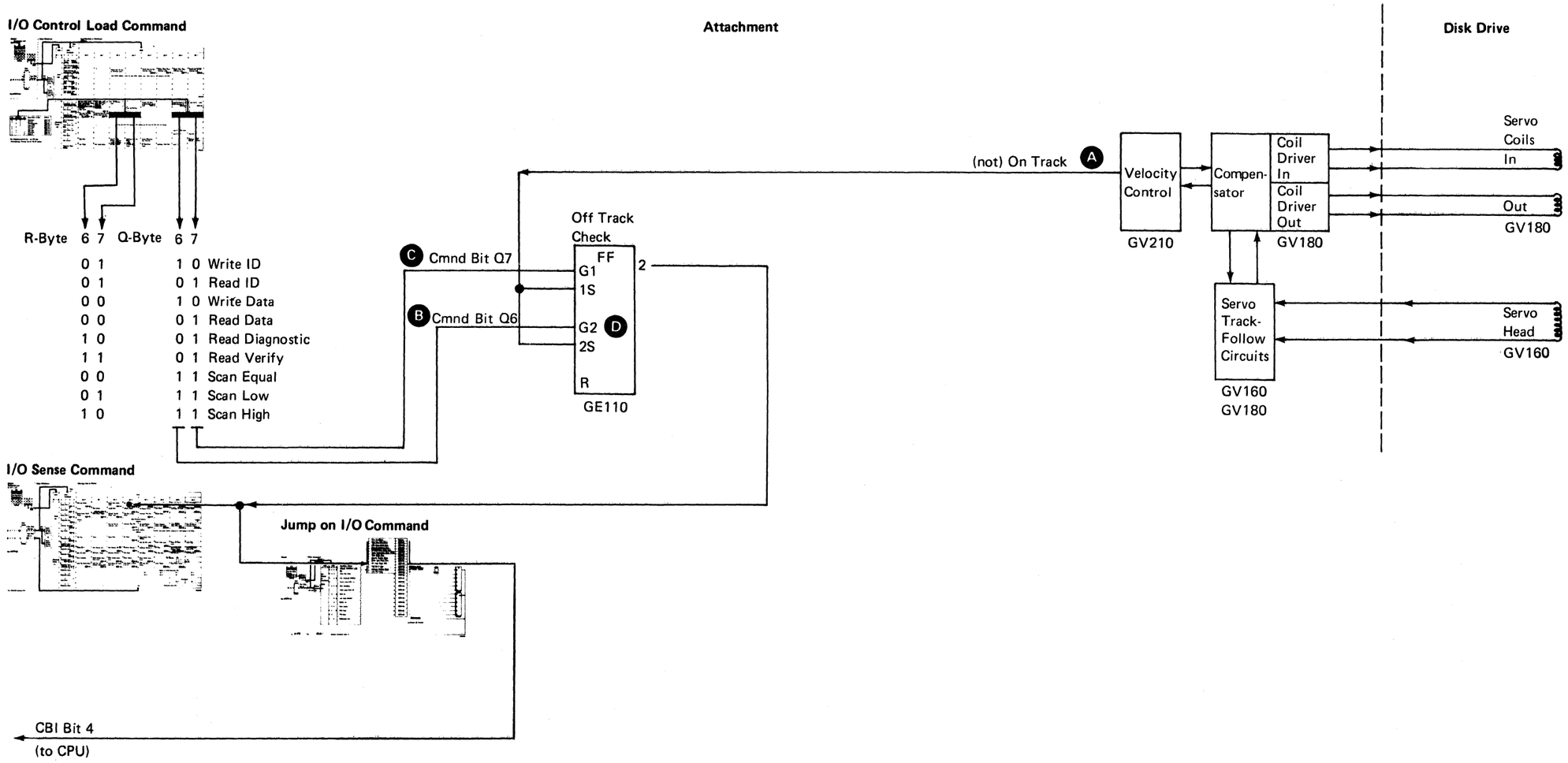


Off Track Check

An off track check is indicated if the actuator arm moves off track (A) during a data operation.

An off track check can be indicated during any read, write, or scan operation.

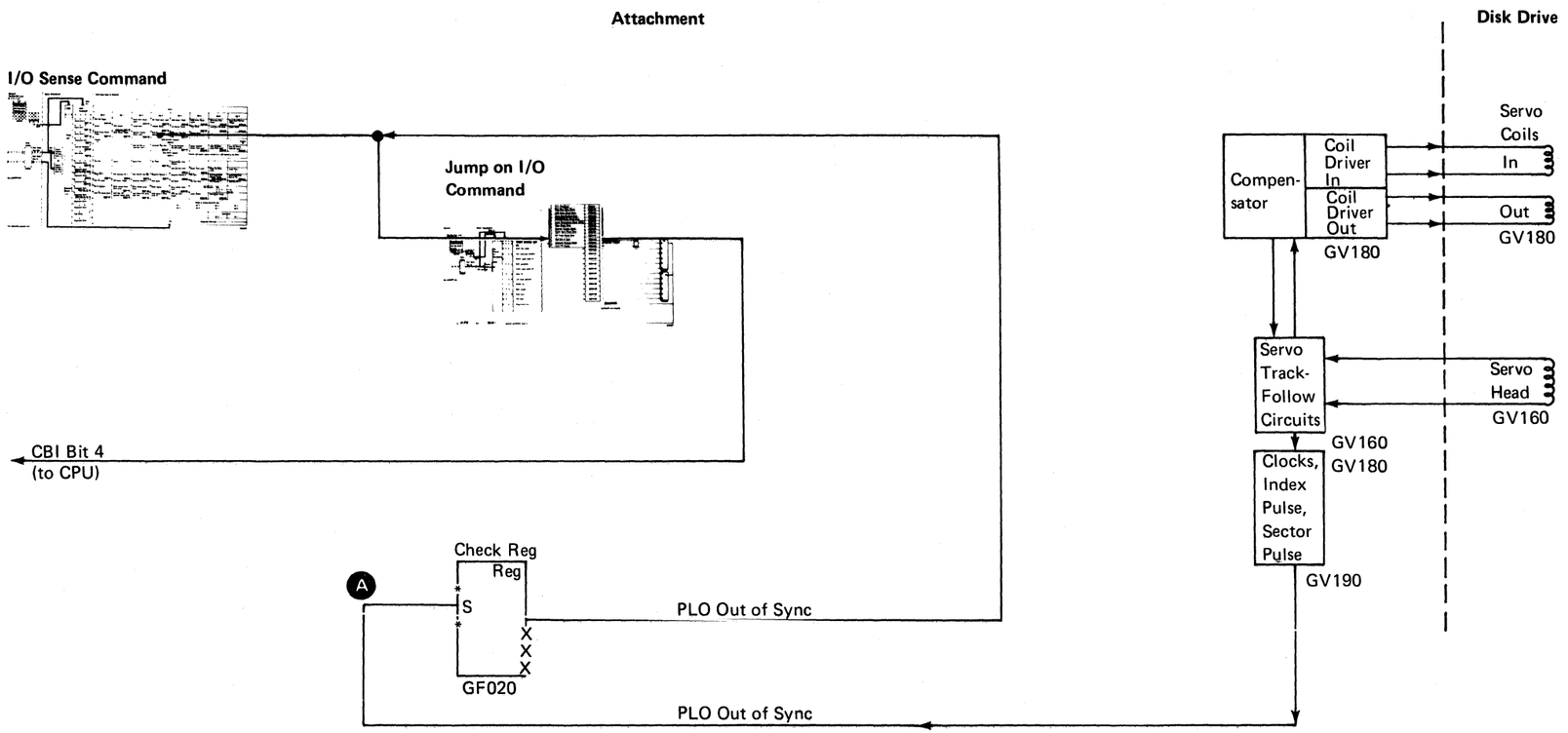
During a read, write, or scan operation, either Q-byte bit 6 (B) is active or Q-byte bit 7 (C) is active. If the servo head goes off track, an off track error is indicated (D).



PLO Out of Sync

The 'PLO out of sync' line (A) becomes active when there is a loss of four or more servo clock pulses or when there is a 90-degree phase error.

For more information on PLO out of sync, see *Phase Lock Oscillator* earlier in this section.



Interrupt Time-out Check

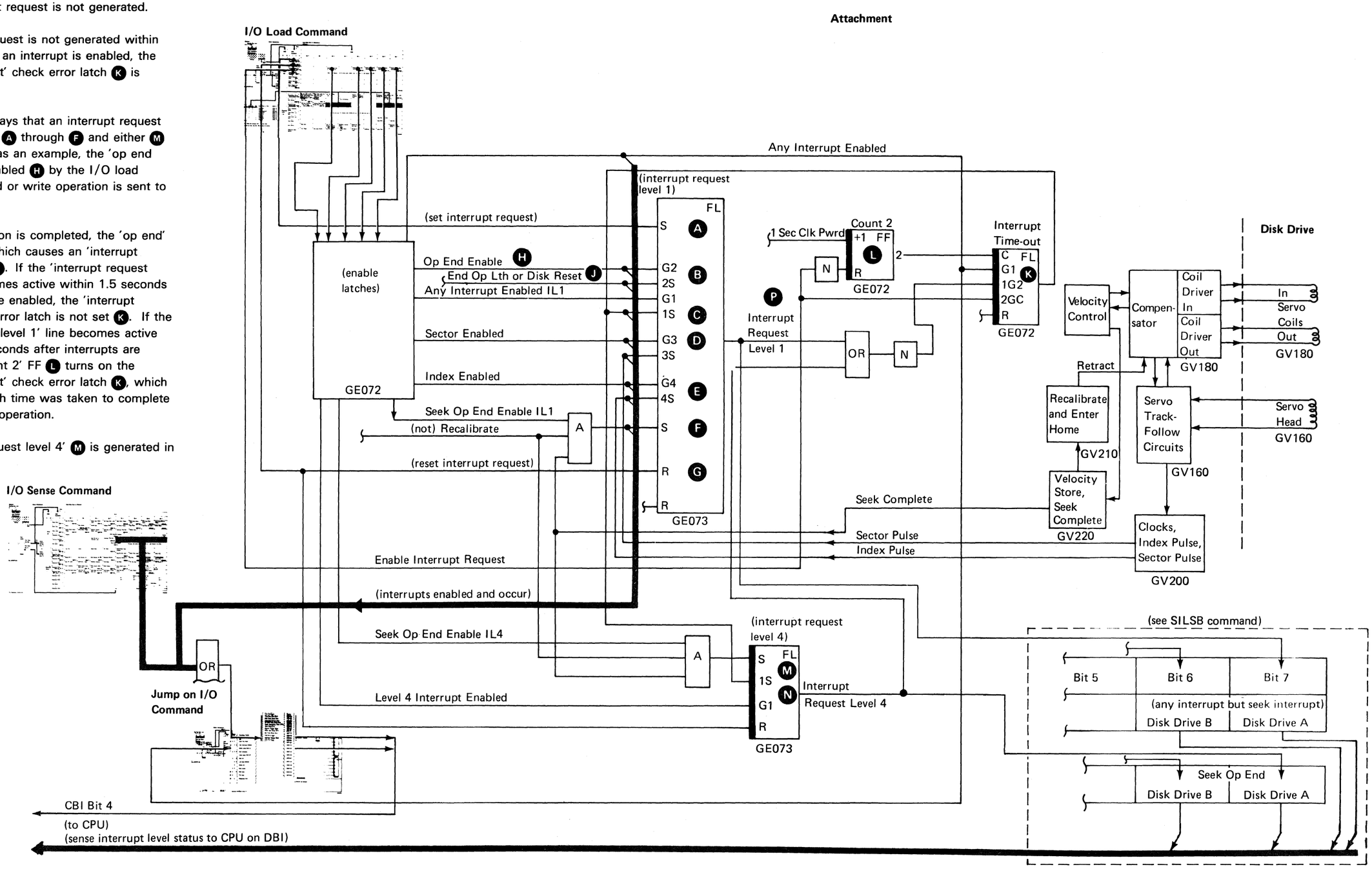
An interrupt time-out check occurs if an expected interrupt request is not generated.

If an interrupt request is not generated within 1.5 seconds after an interrupt is enabled, the 'interrupt time-out' check error latch (K) is turned on.

There are eight ways that an interrupt request can be generated (A) through (F) and either (M) or (N). Using (B) as an example, the 'op end enable' line is enabled (H) by the I/O load command. A read or write operation is sent to the attachment.

When the operation is completed, the 'op end' latch is set (J), which causes an 'interrupt request level 1' (P). If the 'interrupt request level 1' line becomes active within 1.5 seconds after interrupts are enabled, the 'interrupt time-out' check error latch is not set (K). If the 'interrupt request level 1' line becomes active more than 1.5 seconds after interrupts are enabled, the 'count 2' FF (L) turns on the 'interrupt time-out' check error latch (K), which indicates too much time was taken to complete the read or write operation.

The 'interrupt request level 4' (M) is generated in a similar way.



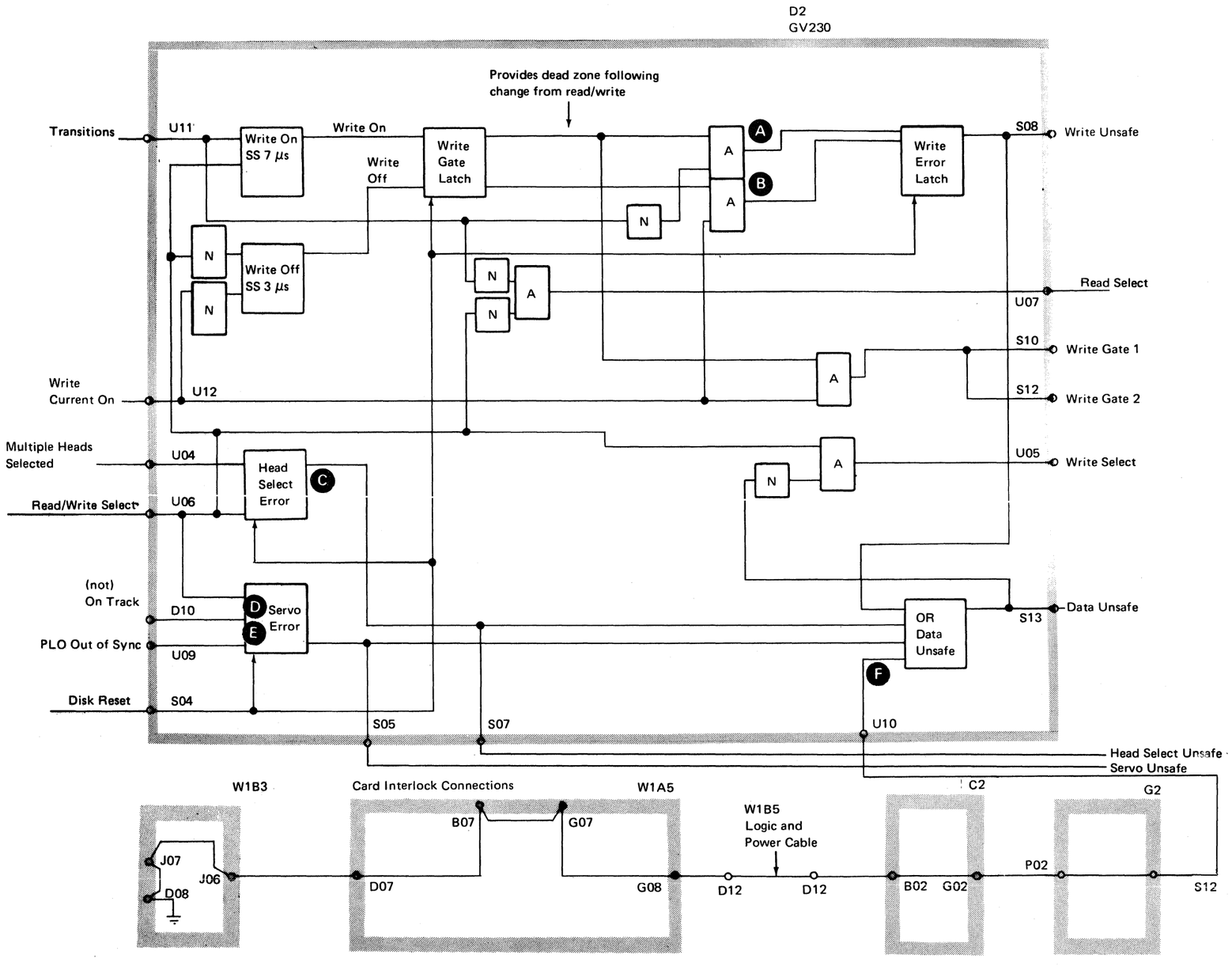
Data Unsafe

When the 'data unsafe' line is active, it indicates one or more of the following error conditions:

Error Condition	Latch Set
Write selected but no write bits generated (A)	Write error
Write current source on but not write selected (B)	Write error
Write selected and more than one head selected (C)	Head select error
Write selected and off track indicated (D)	Servo error
Write selected and PLO out of sync (E)	Servo error
Any data channel card that is not plugged or seated correctly (F)	No latch set, but data unsafe indicated

CAUTION

Continuous pulsing of the 'disk reset' line to attempt to clear an unsafe condition can cause data to be erased. During a data unsafe condition, all read and write operations are inhibited. The 'ready' latch is turned off and then is turned on by a recalibrate operation after the data unsafe condition is cleared.



JUMP ON I/O CONDITIONS

Five jump on I/O conditions are shown on this figure.

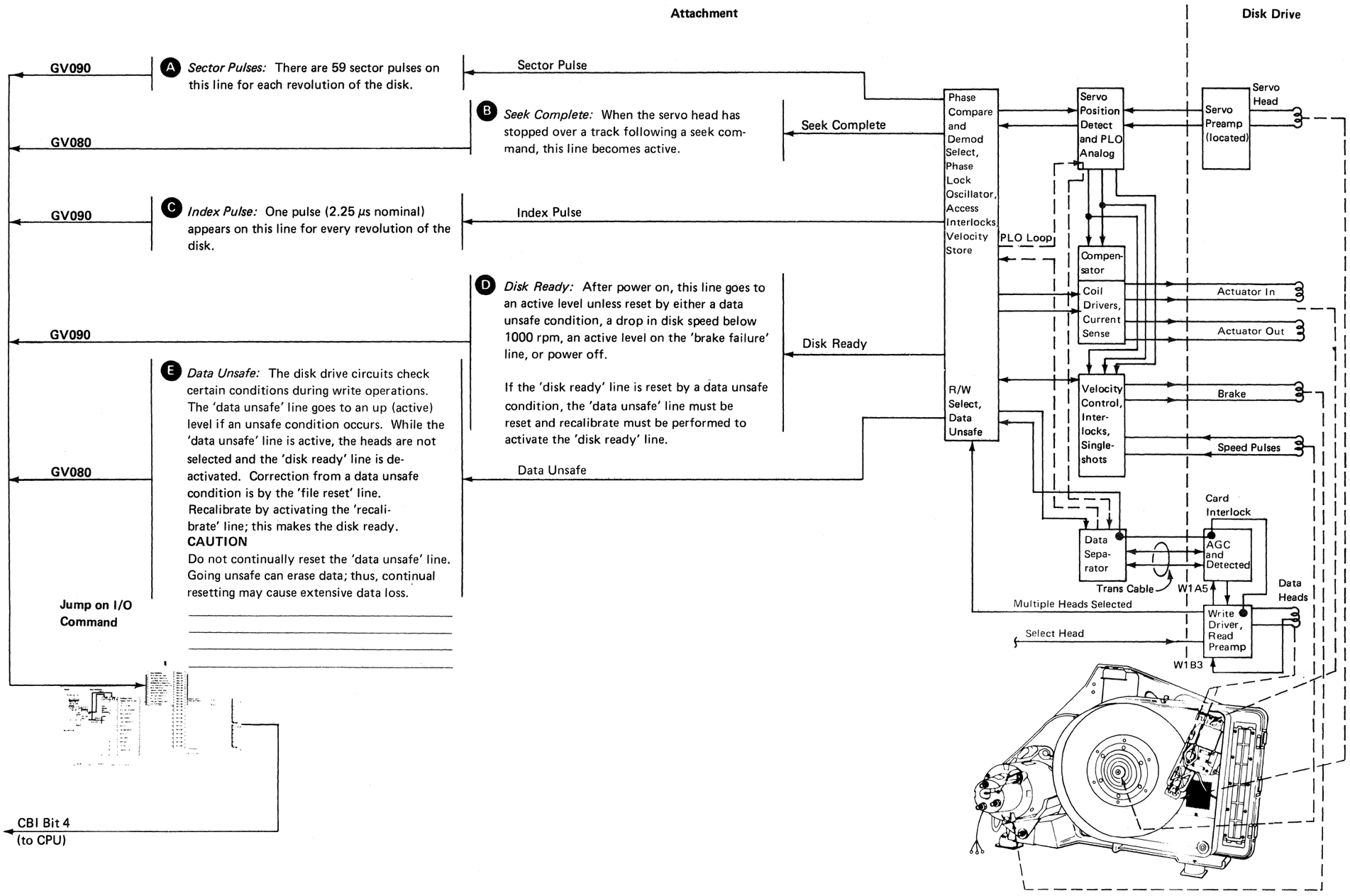
Sector Pulses A

Seek Complete B

Index Pulse C

Disk Ready D

Data Unsafe E



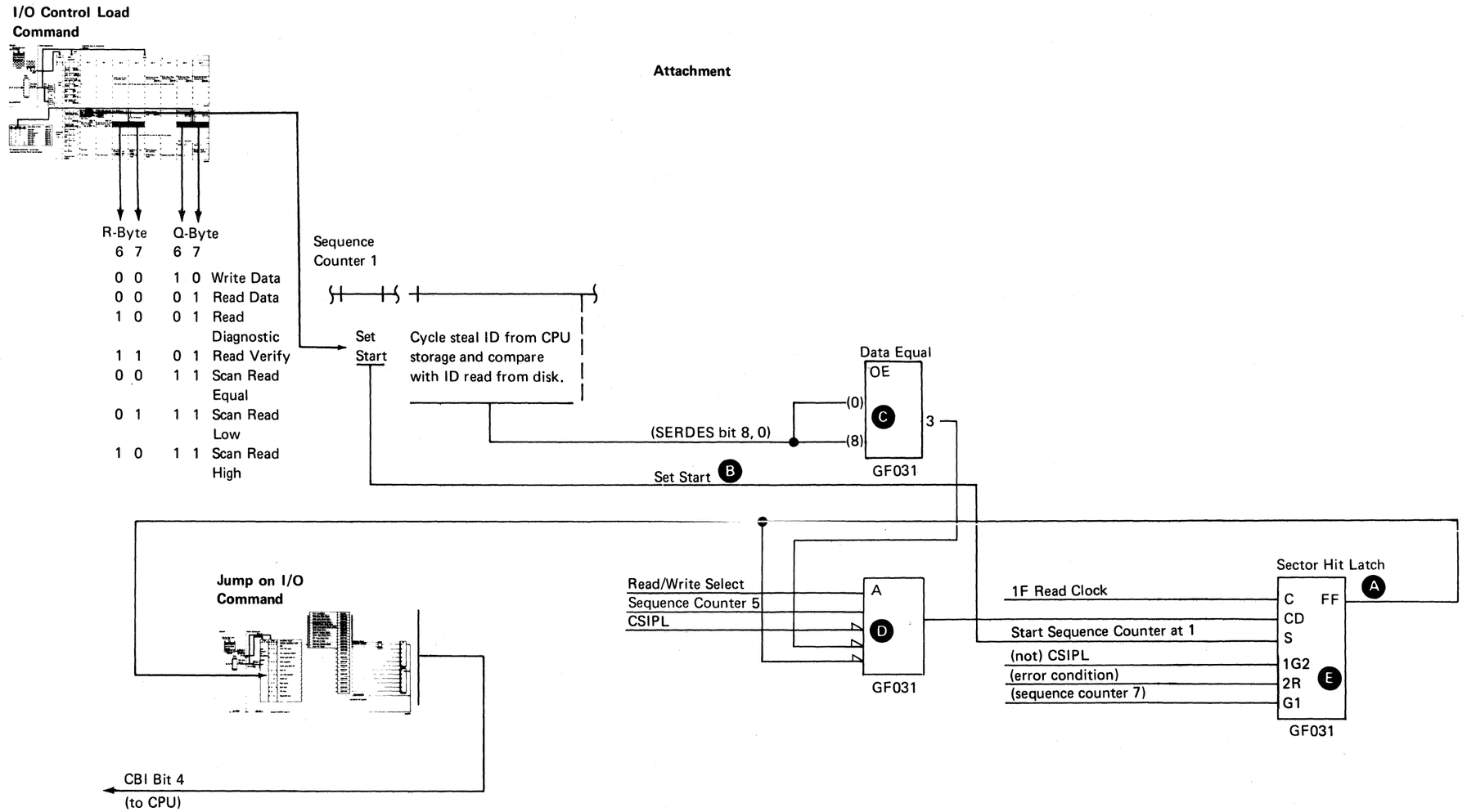
Sector Hit

The sector hit jump on I/O condition is tested on this figure.

The 'sector hit' latch (A) indicates that the control processor identification field and the disk identification field compare equal.

When a data operation is started, the 'set start' line (B) turns on the 'sector hit' latch (A). During sequence counter 5, identification fields are compared (C) for equal. If the identification fields compare equal, the 'sector hit' latch remains on. If the identification fields do not compare equal, the 'sector hit' latch is reset (D). If an error condition occurs while the identification field is being read, the 'sector hit' latch is reset (E).

A sector hit is searched for during the following read and write data operations.



Scan Hit

The scan hit jump on I/O condition is tested on this figure.

The 'scan hit' line (A) indicates that the equal condition, the low or equal condition, or the high or equal condition (control processor data field being compared to the disk data field) is met.

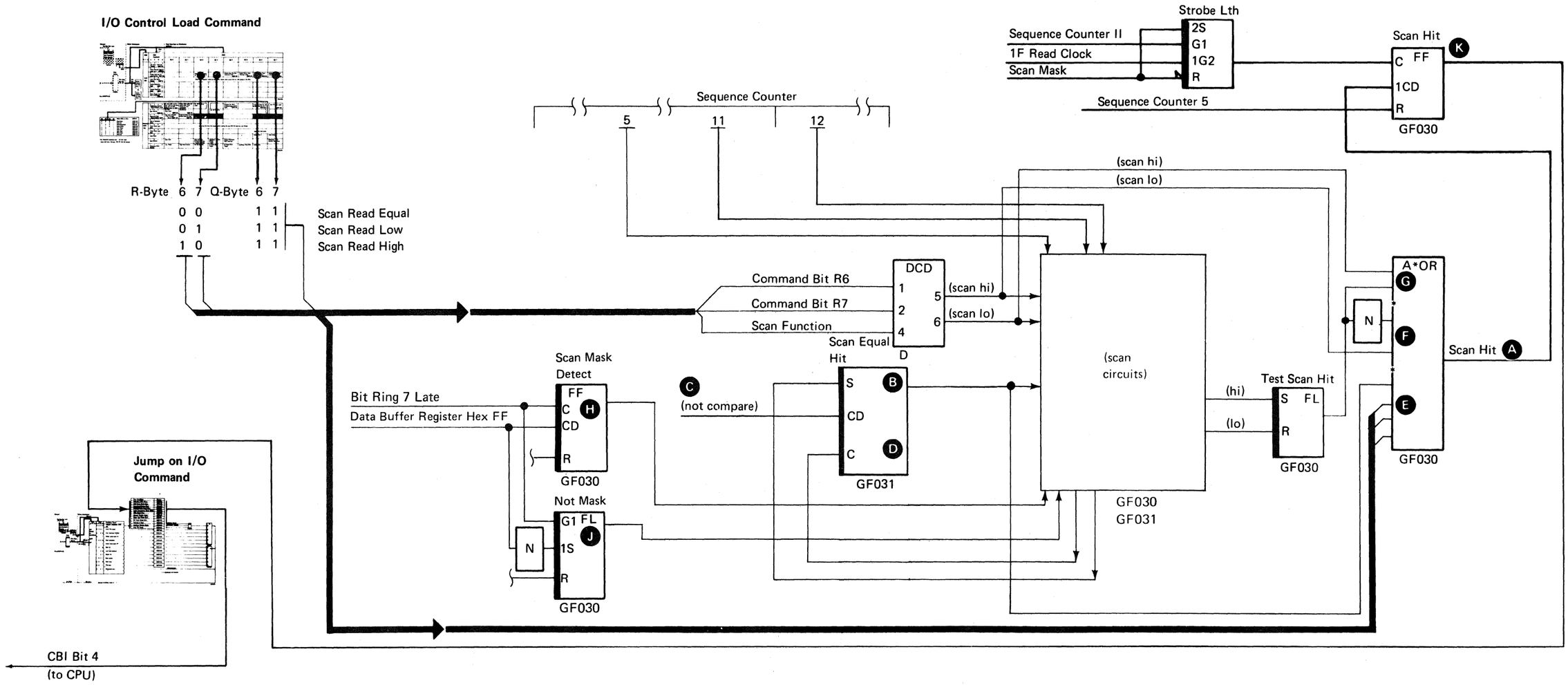
During sequence counter 5 of a scan read equal operation, the 'scan equal hit' latch is set on (B). During sequence counter 11, read data from the disk is compared (C) to read data from the control processor. If the data does not compare, the 'scan equal hit' latch is set off (D). If the data does compare, the 'scan equal hit' latch is not set off and a scan hit (E) is indicated.

During a scan read low or equal data operation, if data from the disk compares low or equal to the data from the control processor, a scan hit (F) is indicated.

During a scan high data operation, if data from the disk compares high to the data from the control processor, a scan hit (G) is indicated.

If a hexadecimal FF is sent from the control processor, the 'scan mask detect' latch (H) prevents a compare for that byte time. Also, if the 'not mask' latch (J) is not turned on during a scan data operation, it indicates that control processor compared data is all hexadecimal FFs; therefore, the 'scan hit' latch (K) is not on at the end of the data compare.

A scan hit is searched for during the following scan read data operations.



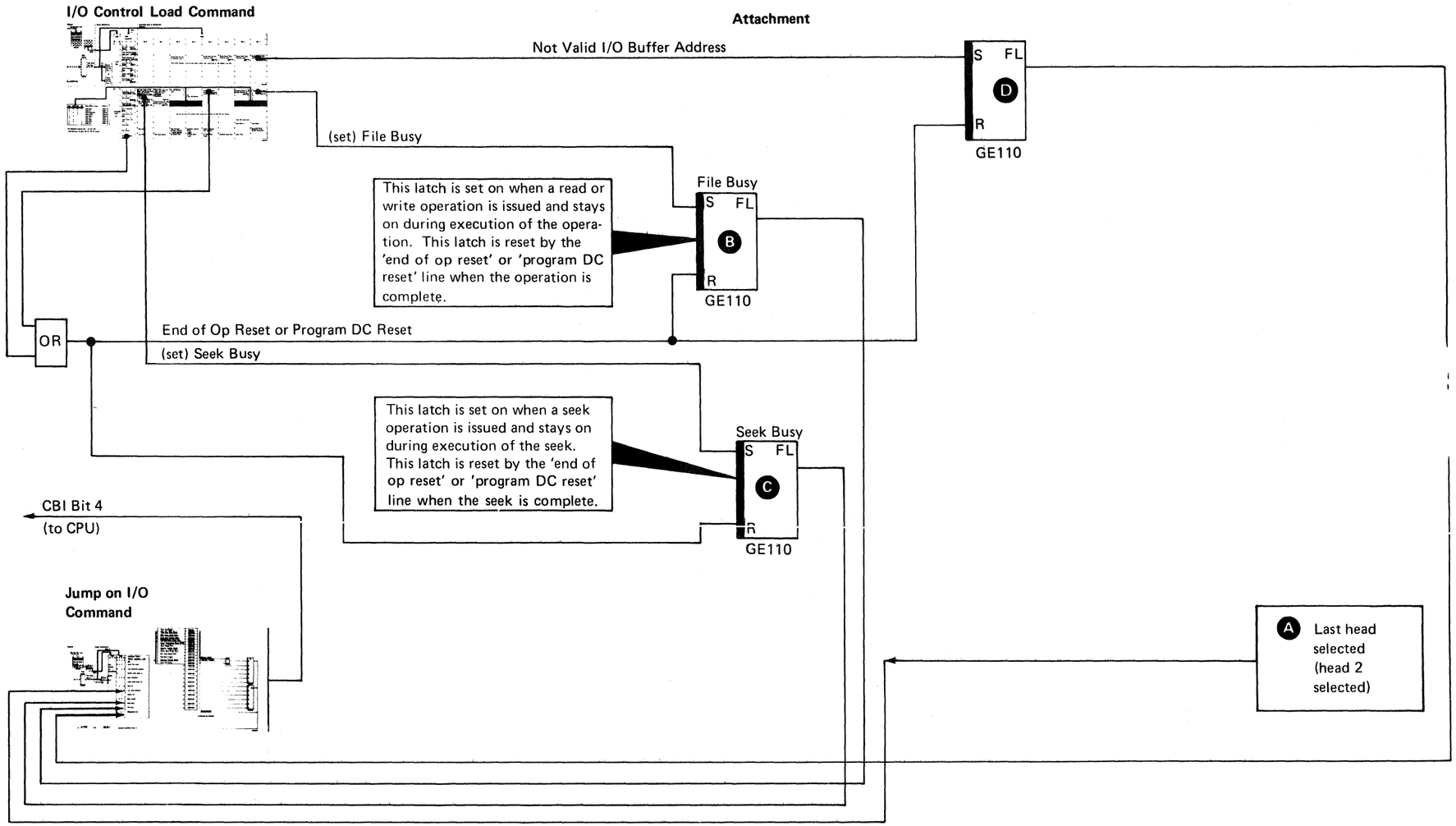
Four jump on I/O conditions are tested on this figure:

Last Head Selected Ⓐ

File Busy Ⓑ

Seek Busy Ⓒ

Not Valid I/O Buffer Address Ⓓ



INPUT/OUTPUT AND SENSE LINES

Output Bus Lines

See *Data Flow* earlier in this section.

Line	Indicates/Purpose	Cause/Conditions
Standardized data	Carries data read from the disk and echoes data being written.	
Read clock 1F		Gated by the read oscillator.
Data unsafe	Failure condition.	Brought up by a write error, a head select error, a servo error, or an incorrectly plugged card.
Write unsafe	Unsafe condition.	Caused by a write selected and no write current condition or by a write not selected and write current condition.
Select unsafe	Unsafe condition.	Caused by a write selection when more than one head or no head is selected.
Servo unsafe	Unsafe condition.	Caused by a write selection when the data heads are off track or the phase lock oscillator is out of sync.
Write clock 1F	Used as a reference during a write operation.	Gated by the phase lock oscillator.
Disk ready	The disk is ready to be used.	1. The disk is up to speed. 2. The data heads are at cylinder 0 (power on). 3. No data unsafe condition. 4. An electrical failure in the drive motor brake.
Index pulse	Indicates the track starting point.	Active once per revolution of the disk.
Home	The data heads are at cylinder 0.	Active only after: 1. Power on. 2. Recalibration. 3. An access that forces the data heads into the guard band.
Behind home	The data heads are between cylinder 0 and the landing zone.	Active during guard band.
Guard band	The servo head is in the guard band.	No sector, index, or sector midpoint pulses.
Seek complete	Active when not seeking.	
On track	The data heads are at a data track.	
Speed pulses	Used to calculate the disk speed.	Active once per revolution of the disk.
Brake failure	An electrical failure in the drive motor brake.	
Counter 4	Used to time the interval between sectors.	2.2-μs clock
DBI bits 4-7	Used for diagnostic sense.	

Input Bus Lines

See *Data Flow* earlier in this section.

Line	Indicates/Purpose	Cause/Conditions
Read/write operation	Inactive during seeks.	
Fast sync	Gates continuous 1's to the read clock to reach fast synchronization with the read data.	
Write	Selects read (inactive) or write (active).	
Write zeros	Carries the data to be written on the disk: up for 0, down for 1.	
Disk reset	Resets latches in the disk drive during power on or after an unsafe condition.	
Power on delay	A power on or power off is in operation.	Permits the disk to reach speed before any actions can occur.
Byte select bit 1 Byte select bit 2	Decode the load or sense pulse.	
Load pulse	Causes DBO bits 0-7 to be latched.	
Sense pulse	For diagnostic purposes.	
DBO bits 0-7	Loads seek commands and the track count.	
Recalibrate	Moves the access heads to cylinder 0.	After a power on delay or an access error.
Head degate	When a write check occurs, head select is de-activated.	
Access interrupt	For diagnostic purposes.	

Sense Lines Used with MAPs

Line	Indicates/Purpose	Cause/Conditions
PLO out of sync	The phase lock oscillator is not synchronized to the servo clock pulses.	
Select out drive	The actuator is driven away from the spindle.	
Select in drive	The actuator is driven toward the spindle.	
VFL (velocity follow latch)	The 'velocity follow' latch gates the seek controls to the actuator.	Active during all seek operations.
Linear region	The servo head is over a track.	Comes from the error signal that is generated when the access arm moves across a track.
Sector pulse	The beginning of each sector.	Comes from the servo track. Sector 0 uses the index pulse.
Too fast	Slows the arm during access.	Generated by desired velocity and actual actuator velocity.