5.6. MAGNETIC CORE STORAGE SYSTEM

a. GENERAL PRINCIPLES OF MAGNETIC CORE STORAGE

(1) CORES. - Each core is a small toroid of a material possessing an almost rectangular hysterisis loop. Five wires or "elements" pass through eac core as shown in Figure 2-1; The horizontal X element, the vertical Y elemen the Diagonal S element, the horizontal I_1 element, and the vertical I_2 eleme The core and the five elements form a bistable device capable of storing a " or a "0", depending upon the direction of magnetization in the core. In gen the "1" or the "0" state is produced when two current pulses of the same pol rity pass simultaneously through the X and Y elements, the resulting "1" or " depending upon the polarity of the current pulses.

Reading or writing is accomplished by a sequence of current pulses on the elements. Graphs showing the specific pulse sequences for reading or writing both a "1", and a "0", are shown in Figure 2-2.

The writing of information in a single core is accomplished in three steps. These may be designated as the "clear", the "write" and the "disturb" steps. The "clear" step is executed by two coincident current pulses on the X and Y elements. The amplitude of these pulses is such that the combined effect of both pulses is sufficient to force the core from the "1" to the "0" state, but the occurrence of a pulse on only one of these elements does not affect the state of the core. This choice of amplitude provides an "and" logic function that is used to select one particular core during writing, as explained in sub-paragraph b(2) below, Address Selection System. After the "clear" step has forced the core to "0", the "write" step is executed which either leaves the core in the "0" state or forces the core to the "1" state. If a "1" is to be written, two simultaneous pulses of polarity opposite to the "clear" step pulses are applied to the X and Y elements to force the core to the "1" state. These

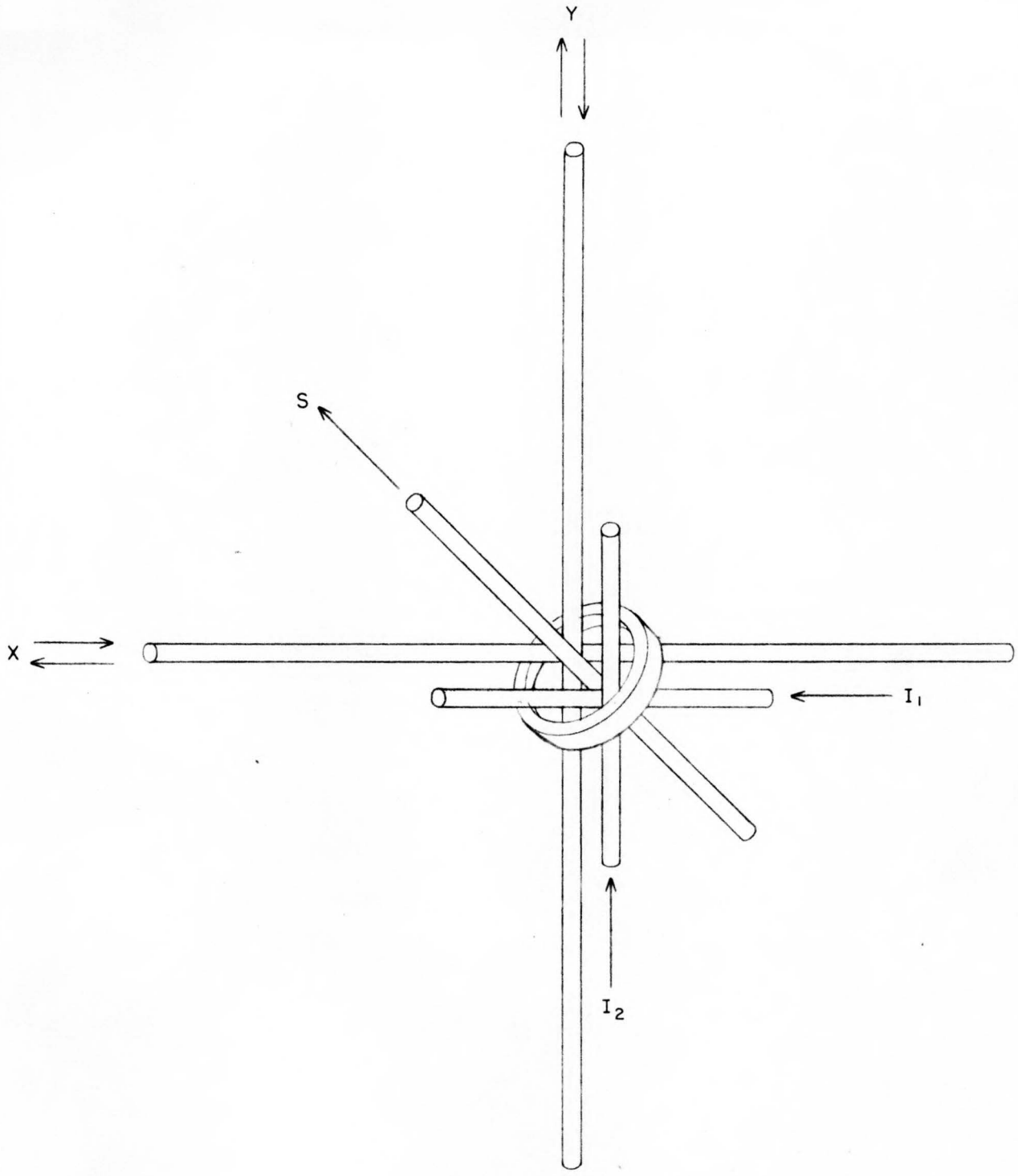


Figure 2-1. Typical Magnetic Core and Element Wires. Arrows Indicate Direction of Current Flow During Reading or Writing

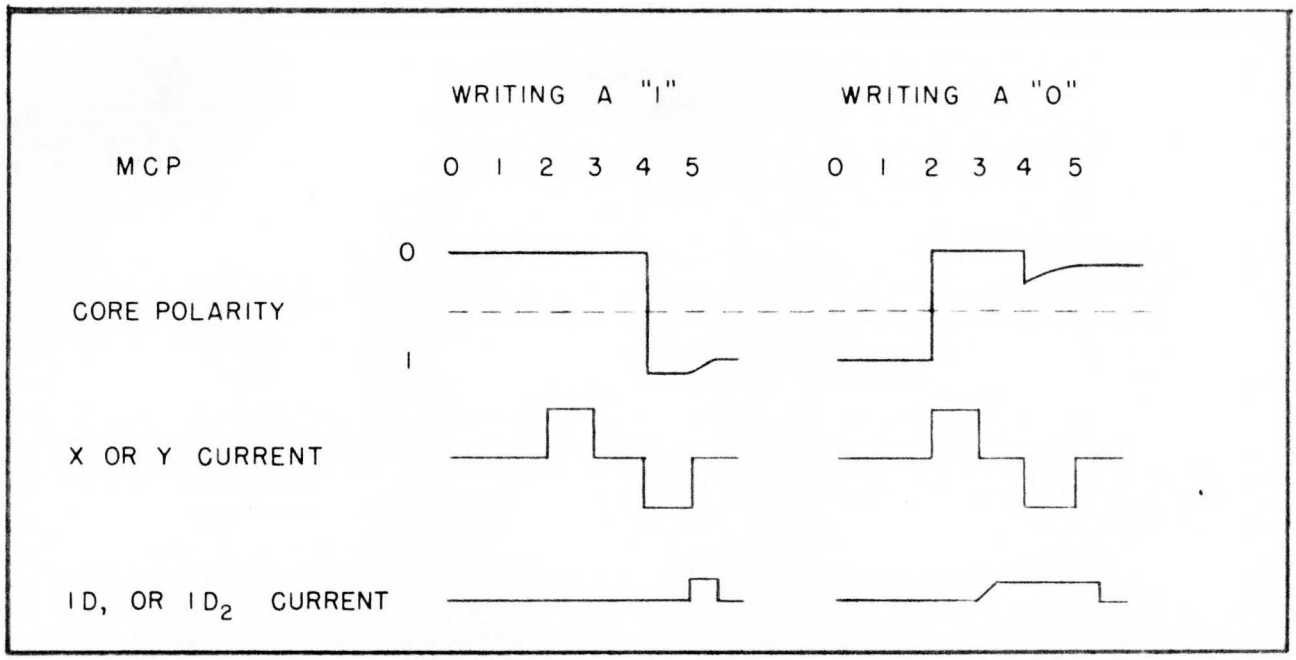


Figure 2-2. Pulses Occurring During Writing

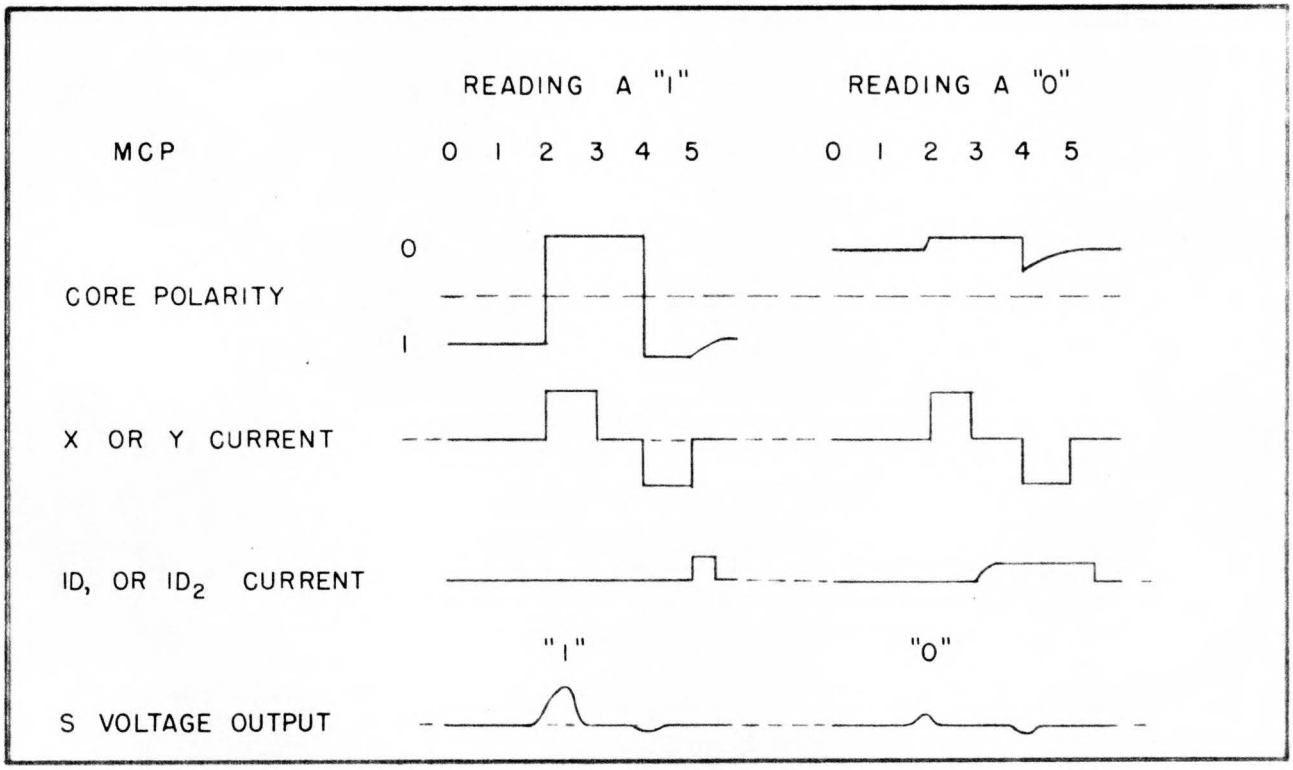


Figure 2-3. Pulses Occurring During Reading

pulses are also of an amplitude such that both must be present to affect the core. If a "0" is to be left in the core, the two current pulses are applied to the X and Y elements, but their effect upon the core is cancelled by the presence of a positive INHIBIT pulse on the I_1 and I_2 elements. The amplitude of the conditionally-present INHIBIT pulse is equal to about one-half of amplitude of the pulses used on the X and Y elements, a value which suffices to cancel the effect of writing a "1". The third or "disturb" step is executed by a DISTURB pulse of short duration which is applied to the I_1 and I_2 elements. If the core is in the "1" state, this pulse alters the flux to a standard "1" value which is fairly stable in the presence of positive "noise" pulses which may occur in the system.

The reading of information from a single core is also accomplished in three steps. These may be designated as the "read", the "restore", and the "disturb" steps. The "read" step is similar to the first step of writing in that it is executed by two coincident current pulses on the X and Y elements. If the core was initially in the "1" state the resulting flux change occurring when the core is forced from "1" to "0" produces a SENSE voltage pulse on the S element. Therefore, during this step the reading of a "1" is represented by the presence of a SENSE pulse, and the reading of a "0" is represented by the absence of a SENSE pulse, on the S element. Because the first or "read" step destroys the presence of a "1", it is necessary to restore the "1" so that repeated readings may be made from the core. This is accomplished by the second or "restore" step. This "restore" step is similar to the second step of writing. If a "1" was read from the core, the restoring of the "1" is accomplished by two coincident pulses of polarity opposite to the "read" step pulses on the X and Y elements. These pulses are also present on X and Y if a "0" was read, but their effect upon the core is cancelled by the presence of a positive INHIBIT pulse

on the I_1 and I_2 elements, so that the core is left in the "0" state. The third "disturb" step is identical to the third step of writing.

(2) MAGNETIC CORE MATRICES. - Each matrix consists of 1024 magnetic cores and their element wires, positioned in a 32-by-32 array so that the element wires all lie in the same plane. The cores are held in position by the element wires which are soldered to a rectangular printed-circuit frame. A typical magnetic core matrix is shown in Plate 2-1.

In each matrix, all 1024 cores transmit and receive information to and from the same stage of the X register. This system arrangement is economical in that it permits the 1024 cores to share common S and I elements. Furthermore, the 32-by-32 square arrangement requires only 32 X elements and 32 Y elements for 1024 cores. The circuit of the X, Y, S, and I elements are shown in Unit Signal Diagram, 55500, found on page of Volume 2. This diagram illustrates that there are 32 X elements, 32 Y elements, one diagonal S element which passes through each core once, and one I element which passes through each core twice.

Many design factors are incorporated to minimize cross-talk or "splash" between cores and elements. Because the cores are of toroidal shape, a low-reluctance path is provided which confines the flux to a small space. Because the cores are positioned so that the toroidal axis of each core is perpendicular to the axis of neighboring cores, the flux pattern in any one core has little effect on the adjacent cores. The path of the element wires are chosen so that the effects of redundant signals in these elements are subtractive rather than additive. For example, the diagonal S element passes back and forth over each X or Y element an even number of times so that transients produced on S by a pulse on one X or Y element cancel each other.

When reading or writing is to be performed in a particular core address, a Magnetic Core Read or Magnetic Core Write sequence produced by the Magnetic Core Access Control first sends READ (CLEAR) pulses simultaneously to one of the 32 X elements and to one of the 32 Y elements. In the core located at the junction of these two lines, the additive effect of both pulses performs the first step of reading or writing by forcing the core to the "0" state. On the pulsed X and Y elements, 62 other cores each receive only a single pulse and therefore are not affected. Next, a WRITE (RESTORE) pulse on the opposite polarity on the same X and Y elements attempts to force the selected core to the "1" state. If the core is to be left in the "0" state, a positive INHIBIT - DISTURB enable present at this time is gated to the matrix I element so that the effect of the WRITE pulse is partially cancelled and the core remains in the "0" state.

During the first part of a reading sequence, when a "1" is changed to a "0", the pulse induced on the diagonal S element is clipped and shaped to form a positive SENSE pulse which indicates that a "1" is being read. Although positive pulses may be induced on the S element during a writing sequence, these are not utilized by the system.

(3) MAGNETIC CORE MATRIX ASSEMBLY. - The Magnetic Core Matrix Assembly consists of a vertical stack of 40 matrices, mounted in the 55000 cabinet. This assembly is shown in Plate 2-2. Although electrical connections are provided for all 40 of the matrices, only 36 matrices are used for storage and the remaining four are spares.

Vertical jumpers connect the X and Y elements of the 40 matrices to provide 64 series paths through these elements for the X and Y current pulses. This includes 32 paths for elements X0 through X31, and 32 paths for elements Y0 through Y31. The 32 READ/WRITE X inputs are connected to the bottom right and bottom left edges of the stack, and the 32 READ/WRITE Y inputs are connected to

the bottom front and bottom rear of the stack. At the top end of the stack, the 64 series circuits are connected to terminating resistors which are mounted above the stack.

On each matrix, two wires connected to the left front corner provide connection for the I element and two wires on the right front corner provide connection for the S element. The electrical connections to these terminals and to the 64 X and Y circuits are tabulated in the Unit Signal Diagram, 555000 found on pages and , Volume 2.

b. SEQUENCES OF OPERATION

(1) GENERAL SEQUENCE. - Four different sequences are produced, one for reading and three for writing. An MCS Read Sequence transmits the contents of an SAR-specified magnetic core address to X, and an MCS Write Sequence transmits the contents of X into an SAR-specified magnetic core address. MCS Write 0-14 and an MCS Write 15-29 sequences provide means of writing in only the u and v portions of storage addresses.

When a reference is made to the Magnetic Core Storage System, an INITIATE READ MCS, INITIATE WRITE MCS, INITIATE WRITE MCS (0-14), or INITIATE WRITE MCS (15-29) signal from the Storage Class Control initiates one of the four sequences by setting or clearing Magnetic Core Pulse Distributor and Magnetic Core Access Control flip-flops. The particular settings of these flip-flops determines the type of sequence that is performed.

The MCS Read and MCS Write sequences are similar in that many of the operations used in reading are identical to operations used in writing. During the first half of either an MCS Read or a Write sequence, simultaneous READ/CLEAR current pulses are sent to one X element circuit and one Y element circuit. During the last half of either a Read or Write sequence, WRITE/RESTORE current pulses sent to the same X and Y elements conditionally write or restore "1"s in

the cores, depending upon the presence or absence of INHIBIT pulses on the I elements. For all sequences, a DISTURB pulse is present on the I elements after writing or restoring has been completed.

The READ/CLEAR and WRITE/RESTORE pulses for the X and Y elements are produced by the Magnetic Core Address Selection System. When any of the four MCS sequences is initiated, the contents of the lower-order 10 stages of SAR is transmitted to an ADDRESS REGISTER (AR). During the Read or Write sequences, a READ ENABLE, WRITE ENABLE, READ PULSE, and WRITE PULSE formed by the Magnetic Core Access Control are combined with the outputs of the Address Register to form the READ/CLEAR and WRITE/RESTORE Pulses.

The INHIBIT and DISTURB pulses for the I elements are produced by Digit Control circuits. Each of the 36 matrices is controlled by one of these circuits during writing or restoring. If a "0" is to be left in the selected core, a "0" enable from an Input-Restore flip-flop allows an INHIBIT-DISTURB ENABLE to pass as a current pulse to the I element. This pulse is of slightly longer duration then the WRITE/RESTORE pulse. The portion of the enable which exists during the WRITE/RESTORE pulse inhibits the writing of a "1", and the remaining portion performs the "disturb" function. If a "1" is to be written or restored in the selected core, only the final DISTURB portion of this enable is applied to the I element.

(2) MC ADDRESS SECTION SYSTEM. - The circuits used in address selection, shown on the Block Diagram on page 2 of Volume 2, consist of the Address Register, the Read/Write Pulse Generators, the Read/Write Enable Generators, and the X and Y Drivers. These circuits distribute READ/CLEAR and WRITE/RESTORE current pulses to the matrix assembly X and Y elements so that reading or writing is executed in one particular core address.

When a read or a write reference is made to the Magnetic Core Storage System, circuits of the CXPA equipment Control System transmit the contents of SAR stages 0 through 9 to the 10-stage Magnetic Core Address Register (AR). During each MCS Read or Write sequence, the Read/Write Pulse Generators and Read/Write Enable Generators combine the AR enables with the READ ENABLE, WRITE ENABLE, READ pulse and WRITE pulse from the Magnetic Core Access Control. The resulting signals operate the X and Y Drivers which send positive and negative pulses to the X and Y elements.

(a) READ OR CLEAR PORTION OF CYCLE. - During the first step in an MCS Read or Write Sequence, the lower-order 10 stages of AR designated as AR_0 through AR_4 provide enables for generating the X element pulses. The enables from AR_3 and AR_4 and a READ ENABLE from MCAC combine in the crystal "and" circuits of the Read/Write Enable Generators to form one of the following four READ enables: READ 00XXX, READ 01XXX, READ 10XXX, or READ 11XXX. The enables from AR_0, AR_1, and AR_2 and a READ PULSE (the first pulse to arrive on the READ/WRITE pulse line from MCAC) are combined by the Read/Write Pulse Generators to form one of the following eight READ pulses: READ/WRITE XX000, READ/WRITE XX001, READ/WRITE XX010, READ/WRITE XX011, READ/WRITE XX100, READ/WRITE XX101, READ/WRITE XX110, or READ/WRITE XX111.

The X Drivers produce one of 32 current pulses, i.e., READ X0, READ X1, READ X2, etc., depending upon the particular READ pulse produced by the Read/Write Pulse Generators and the particular READ enable produced by the Read/Write enable generator. This is accomplished because the driver tubes are connected in an array that permits the use of "and" logic in the selection of each driver tube. For example, only one of the 64 X Drivers produces READ X13, and this driver tube, a dual triode, is connected so that it will only produce READ X13 when a READ 01XXX enable is present on the grids, AND a Read/Write XX101 pulse is present on

WRITE pulse. During the read (clear) portion of the sequence the former is selected, but during the write (restore) portion of the cycle the latter is selected. Because of the manner in which the triodes are connected to the output transformer, the WRITE pulse is of opposite polarity to the READ pulse.

(3) DIGIT CONTROL CIRCUITS. - A Digit Control circuit is associated with each of the 36 magnetic core matrices. Each of these is essentially one stage of a 36-stage Input Register, which serves as a temporary storage medium for the bits of a word written into or read from a core address.

(a) OPERATION DURING A READ SEQUENCE - During an MCS Read sequence, the Digit control circuits function as a 36-bit recirculation register, which restores "1" bits that are cleared by the reading operation.

At the beginning of the sequence, MCP-1 clears all 36 flip-flop stages to "0". During the remainder of the sequence, the particular operations performed in each Digit Control circuit depends upon whether or not a "1" is read from the associated matrix. Because each Digit Control circuit is similar electrically to any of the 35 other circuits, only the functioning of Digit Control circuit 0 (IR_0) is explained below.

If a "1" is present in the selected address of Matrix 0, a SENSE signal is received from the matrix SENSE element during the first "read" step of the sequence. This signal enables two gates. Gate V03-25l passes an MCS X pulse received from MCAC at this time, to produce a "1" from MCS_0 pulse which sets stage 0 of the X register to "1". Gate V04-25l passes a RESTORE MCS 0-14 pulse, also received simultaneously with the SENSE pulse, to set IR_0 to "1". During the second or "restore" step of the sequence, the selected core of Matrix 0 is reset to "1", and as a result the "1" read from the core is restored. During the third or "disturb" step, a third gate, V06-25l, is enabled by a DISTURB enable from MCAC and pulsed by an ENABLE INHIBIT-DISTURB signal

the cathodes. It should be noted that the combination of the "1" and "0" bits in the names READ 01XXX and READ/WRITE XX101 forms 11101, the binary equivalent of 13. This number corresponds to the number of the X elements that receives the current pulse, i.e., the X 13 elements of all matrices receive the READ X13 pulse.

The other portions of the MC Address Selection System consisting of AR_5 through AR_9, the Y Drivers, and the remaining Read/Write pulse and enable generators function in a manner similar to the X half, described above. During the first step in an MCS Read or Write Sequence, the contents of AR_5 through AR_9 provides enables for generating one of 32 current pulses, i.e., READ Y0, READ Y1, READ Y2, etc.

In each core matrix, the receipt of one of the 32 READ X current pulses and one of the 32 READ Y pulses reads or clears one of the 1024 cores positioned in one of the 1024 intersections of the X and Y elements. In this manner, each of the 1024 possible values in AR directs reading operations to one core in each of the 36 matrices. The values in AR represent 10-bit addresses obtained from SAR, and therefore the MC Address Selection System provides access to 1024 addresses each having 36 bits.

(b) WRITE OR RESTORE PORTION OF CYCLE. - During the second step in an MCS Read or Write sequence, the Address Selection System functions in a manner similar to that described in the preceding subparagraph, except that the presence of a WRITE ENABLE from MCAC causes the Read/Write Enable Generators to produce WRITE enables designated as WRITE 00XXX, WRITE 01XXX, WRITE 00YYY, etc.

In the X Drivers, and also in the Y Drivers, the circuit used to produce READ and WRITE pulses for one matrix element consists of a pair of duo-triodes connected in "push-pull" fashion to an output transformer. One duo-triode is used only to produce a READ pulse, and the other is used only to produce a

also from MCAC. The resulting DISTURB pulse, applied to the Matrix I element, standardizes the flux patter in the cores.

If a "0" is present in Matrix 0, no SENSE signal is received. As a result, IR_0 will remain in the "0" state and no signal will be sent to the X register. During the second or "restore" step of the sequence the "0" enable from IR_0 enables gate V06-251 so that the ENABLE INHIBIT-DISTURB signal from MCAC produces an INHIBIT current on the I element of the matrix, and as a result the writing of a "1" in the core is inhibited. The core remains in the "0" state. During the "disturb" step the DISTURB enable from MCAC holds V06-251 enabled, and the final portion of the ENABLE INHIBIT-DISTURB signal from MCAC passes through the gate to form a DISTURB pulse, applied to the I element of the matrix.

The above operations are similar for Digit Control circuits 1 through 35. During the "restore" step circuits 0 through 14 receive RESTORE MCS 0-14, circuits 15 through 29 receive RESTORE MCS 15-29, and circuits 30 through 35 receive RESTORE MCS 30-35.

(b) OPERATION DURING A WRITE SEQUENCE. - During an MCS Write Sequence, the Digit Control Circuits function as a 36-bit input register which stores "0" or "1" bits while they are being written in one core address.

At the beginning of the sequence, MCP-1 clears all 36 stages to "0". During the remainder of the sequence, the particular operations performed in each Digit Control circuit depends upon the type of writing operation being executed, and whether a "1" or a "0" is to be written.

If one of the partial write sequences is initiated, writing will occur in only 15 of the Digit Control circuits, and the remaining circuits will execute operations similar to the Read sequence operations, except that the absence of an MCS X pulse from MCAC prevents "1" pulses from being transmitted to X. If the initiating signal is INITIATE WRITE MCS 0-14, only Digit Control circuits

0 through 14 execute writing operations, and if the initiating signal is INITIATE WRITE MCS 15-29, writing is executed only by circuits 15 through 29. If INITIATE WRITE MCS is received, writing occurs in all 36 circuits. The operation of Digit Control circuit 0 is explained below.

If writing is to be executed in stage 0 and a "1" is present in X_0, the first or "clear" step in the sequence serves only to clear the selected core of Matrix 0 to "0". At the beginning of the second or "write" step, a WRITE MCS 0-14 pulse from MCAC passes through gate V05-251 to set IR_0 to "1". The WRITE X and WRITE Y current pulses from the MC Address Selection System force the core to the "1" state. The third or "disturb" step is similar to the "disturb" step of the Read sequence, and is produced by the simultaneous presence of the ENABLE INHIBIT-DISTURB and DISTURB enables from MCAC.

If writing is to be executed and a "0" is in X_0, the first or "clear" step also clears the core to "0". However, the absence of a "1" enable from X_0 leaves gate V05-251 disabled so that at the beginning of the "write" step the WRITE MCS 0-14 pulse fails to set IR_0 to "1". The "0" enable from IR_0 enables V06-251 so that the ENABLE INHIBIT DISTURB signal produces an INHIBIT current on the matrix I element, the writing of a "1" is inhibited, and thus the core is left in the "0" state. Thbe third "disturb" step is produced during the last portion of ENABLE INHIBIT-DISTURB, when the DISTURB enable is received from MCAC.

The above operations are similar for each of the other circuits 1 through 36 if writing is being executed in those stages. Digit Control Circuits which are writing receive one of the following signals from MCAC: WRITE MCS 0-14, WRITE MCS 15-29, or WRITE MCS 30-35. Circuits which are not writing receive one of the following instead: RESTORE MCS 0-14, RESTORE MCS 15-29, or RESTORE MCS 30-35.

(4) MAGNETIC CORE PULSE DISTRIBUTOR. - The Magnetic Core Pulse Distributor is a three-stage binary counter which distributes CLOCK PULSES as a series of magnetic core control pulses, MCP-1 through MCP-5. Preceding these, control pulse MCP-0 is produced when INITIATE READ MCS or any of the three INITIATE WRITE MCS signals is received from SCC. This pulse sets the count in the MCPD flip-flops to the binary value 001. The resulting MCPD enables cause the next CLOCK PULSE to be distributed as MCP-1. This MCP-1 pulse advances the count in MCPD to 010 and the next CLOCK PULSE is distributed as MCP-2. Similar operations occur for MCP-3 and MCP-4. The last pulse, MCP-5, clears all three MCPD flip-flops to "0" and no additional pulses are produced until the next read or write reference is made to Magnetic Core Storage.

(5) MAGNETIC CORE ACCESS CONTROL. - During each sequence of six MCP's, the MCAC flip-flop circuits produce signals for operating the Address Location System, the Address Monitor, and the Digit Control Circuits.

The Address Location System, which produces the READ and WRITE/RESTORE current pulses for the matrix X and Y elements, is operated by a READ ENABLE, a WRITE ENABLE, a READ PULSE, and a WRITE PULSE. During the first half of either a read or a write sequence, the READ ENABLE is started when MCP-0 sets the Enable Read flip-flop to "0", and is terminated when MCP-3 clears this flip-flop. During the last half of the sequence, the WRITE ENABLE is started when MCP-3 sets the Enable Write flip-flop to "1", and is terminated by MCP-5. The Read/Write I and II flip-flops are set and cleared in a manner so that their combined "0" and "1" outputs produce two enables of short duration, one starting at MCP-1 called the READ pulse, and one starting at MCP-3 called the WRITE pulse. In the Address Location System, these pulses are used to operate drivers which produce the READ and WRITE/RESTORE current pulses for the matrices.

The Address Monitor, which provides a visual indication of the address to which a reference is being made, is controlled partially by MONITOR GRID PULSES produced by the Monitor Intensity flip-flop. During either an MCS read or an MCS Write sequence, MCP-1 sets the Monitor Intensity flip-flop to "1" and MCP-5 clears this flip-flop to "0". The resulting eight-microsecond MONITOR GRID PULSE increases the intensity of the cathode ray beam so that the address being referenced is represented on the Address Monitor screen as a bright spot.

The Digit Control Circuits, which control the writing or restoring of "1"s and "0"s in core matrices, are operated by the INHIBIT-DISTURB ENABLE, the DISTURB signal, and by combinations of MCS X, RESTORE MCS 0-14, RESTORE MCS 15-29, RESTORE MCS 30-35, WRITE MCS 0-14, WRITE MCS 15-29, and WRITE MCS 30-35.

During either a read or a write sequence, the INHIBIT-DISTURB ENABLE is started when MCP-3 sets the Enable I/D flip-flop to "1", and is terminated by delayed MCP-5. The resulting enable, which is started coincidently with the WRITE ENABLE, is conditionally gated in the Digit Control circuits to inhibit the writing of a "1". The DISTURB signal is started when MCP-5 clears the Disturb II flip-flop to "0" and is terminated when delayed MCP-5 clears the Disturb I flip-flop. This signal operates in the digit control circuit so that the last one microsecond of the INHIBIT-DISTURB ENABLE is always applied to the I elements of the matrices, regardless of whether a "1" or a "0" is being written. It is this portion of the INHIBIT-DISTURB ENABLE which disturbs the cores to make them assume a standard flux value.

The combinations of other signals used to operate the Digit Control circuits depend upon the type of initiating signal received from SCC. If an INITIATE READ MCS signal has been received, the Read to X flip-flop will be in the "1" state, and delayed MCP-2 produces an MCS X signal which transmits the 36-bit word read from the cores to the X register. If an INITIATE WRITE 0-14 signal

has been received, the W/R 0-14 flip-flop will be in the "1" state, and MCP-3 produces a WRITE MCS 0-14 signal to matrices 0 through 14. If an INITIATE WRITE 15-29 signal has been received, the W/R 15-29 flip-flop will be in the "1" state so that MCP-3 produces WRITE 15-29. If INITIATE WRITE MCS has been received, WRITE MCS 0-14, WRITE MCS 15-29, and WRITE MCS 30-35 will be sent to the 36 Digit Control circuits. In all four sequences, Digit Control circuits which do not receive one of these three types of WRITE signals on MCP-3 receive a correspondingly numbered RESTORE MCS 0-14, RESTORE MCS 15-29, or RESTORE MCS 30-35 signal on MCP-3. These WRITE and RESTORE signals cause the Digit Control circuits either to write or restore "1"s or "0"s in the cores.

The four sequences are shown in tabular form in Tables 2-1 through 2-4 below. The waveforms occurring during these sequences are shown in the Appendix in the back of this volume.

c. ADDRESS MONITOR. - The Address Monitor, a five-inch cathode ray tube mounted at the top of the Maintenance Panel, is similar to the Address Monitor used in the Navy Model CXPA equipment in that it provides an indication in one of 1024 positions each time a read or a write reference is executed in the 1024-address rapid access storage system. However, electrically this unit differs from the preceding unit in that additional circuits were, of necessity, provided to convert the binary count in the Address Register into two analogue voltages for the X and Y deflection plates of the cathode ray tube.

TABLE 2-2

MC WRITE 0-35 SEQUENCE

SCC SUBCOMMAND	MCP	MCAC SUBCOMMAND
INIT. WRITE MCS →	(MCP-0)	SAR → AR (Start MCPD) Set Enable Read to "1" (begin READ ENABLE) Set Disturb II to "1" Set W/R 0-14 to "1" Set W/R 15-29 to "1" Set W/R 30-35 to "1"
	MCP-1	Set Monitor Intensity to "1" Clear Input Register 0-35
	MCP-2	Set Disturb I to "1" Set Read/Write I to "1" (begin READ PULSE)
	MCP-3	Clear Enable Read to "0" (end READ ENABLE) Set Read/Write II to "1" (end READ PULSE) Set Enable Write to "1" (begin WRITE ENABLE) Set Enable ID to "1" (begin INHIB. -DIST. ENABLE) WRITE MCS 0-14 WRITE MCS 15-29 WRITE MCS 30-35
	MCP-4	Clear Read/Write II to "0" (begin WRITE PULSE) MCS RESUME
	MCP-5	Clear Enable Write to "0" (end WRITE ENABLE) Clear Read/Write I to "0" (end WRITE PULSE) Clear Disturb II to "0" (begin DISTURB) Clear Monitor Intensity to "0" Clear W/R 0-14 Clear W/R 15-29 Clear W/R 30-35
	MCP-5 + delay	Clear Enable ID to "0" (end INHIB. -DIST. ENABLE) Clear Disturb I to "0" (end DISTURB)

PX 71368

TABLE 2-3

MC WRITE 0-14 SEQUENCE

SCC SUBCOMMAND	MCP	MCAC SUBCOMMAND
INIT. WRITE MCS 0-14 →	(MCP-0)	SAR ⟶ AR (Start MCPD) Set Enable Read to "1" (begin READ ENABLE) Set Disturb II to "1" Set W/R 0-14 to "1"
	MCP-1	Set Monitor Intensity to "1" Clear Input Register 0-35
	MCP-2	Set Disturb I to "1" Set Read/Write I to "1" (begin READ PULSE)
	MCP-2 + delay	RESTORE MCS 15-29 RESTORE MCS 30-35
	MCP-3	Clear Enable Read to "0" (end READ ENABLE) Set Read/Write II to "1" (end READ PULSE) Set Enable Write to "1" (begin WRITE ENABLE) Set Enable ID to "1" (begin INHIB. -DIST. ENABLE) WRITE MCS 0-14
	MCP-4	Clear Read/Write II to "0" (begin WRITE PULSE) MCS RESUME
	MCP-5	Clear Enable Write to "0" (end WRITE ENABLE) Clear Read/Write I to "0" (end WRITE PULSE) Clear Disturb II to "0" (begin DISTURB) Clear Monitor Intensity to "0" Clear W/R 0-14
	MCP-5 + delay	Clear Enable ID to "0" (end INHIB. -DIST. ENABLE) Clear Disturb I to "0" (end DISTURB)

TABLE 2-4

MC WRITE 15-29 SEQUENCE

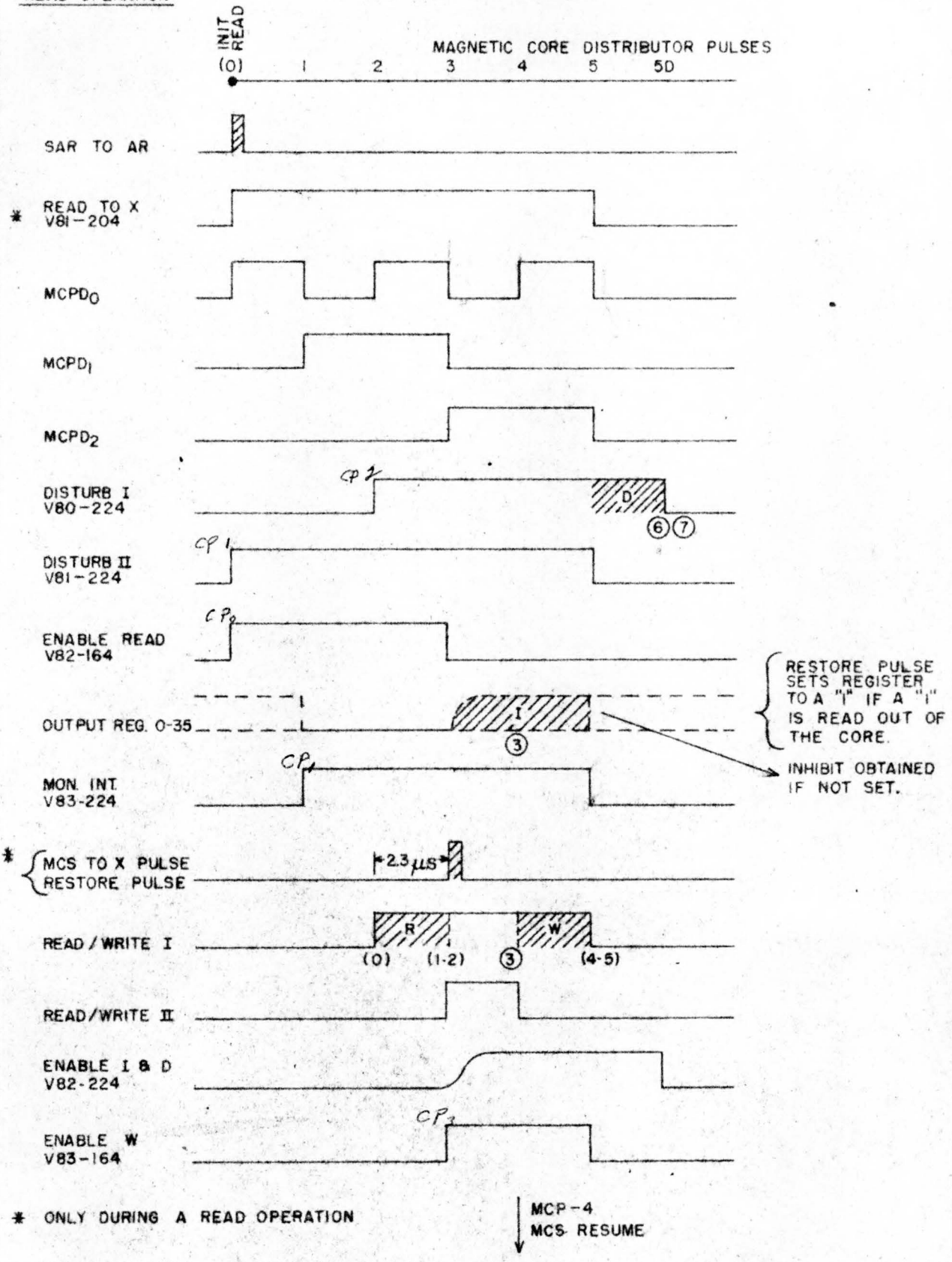
SCC SUBCOMMAND	MCP	MCAC SUBCOMMAND
INIT. WRITE MCS 15-29 →	(MCP-0)	SAR → AR (Start MCPD) Set Enable Read to "1" (begin READ ENABLE) Set Disturb II to "1" Set W/R 15-29 to "1"
	MCP-1	Set Monitor Intensity to "1" Clear Input Register 0-35
	MCP-2	Set Disturb I to "1" Set Read/Write I to "1" (begin READ PULSE)
	MCP-2 + delay	RESTORE MCS 0-14 RESTORE MCS 30-35
	MCP-3	Clear Enable Read to "0" (end READ ENABLE) Set Read/Write II to "1" (end READ PULSE) Set Enable Write to "1" (begin WRITE ENABLE) Set Enable ID to "1" (begin INHIB. -DIST. ENABLE) WRITE MCS 15-29
	MCP-4	Clear Read/Write II to "0" (begin WRITE PULSE) MCS RESUME
	MCP-5	Clear Enable Write to "0" (end WRITE ENABLE) Clear Read/Write I to "0" (end WRITE PULSE) Clear Disturb II to "0" (begin DISTURB) Clear Monitor Intensity to "0" Clear W/R 15-29
	MCP-5 + delay	Clear Enable ID to "0" (end INHIB. -DIST. ENABLE) Clear Disturb I to "0" (end DISTURB)

TABLE 2-1

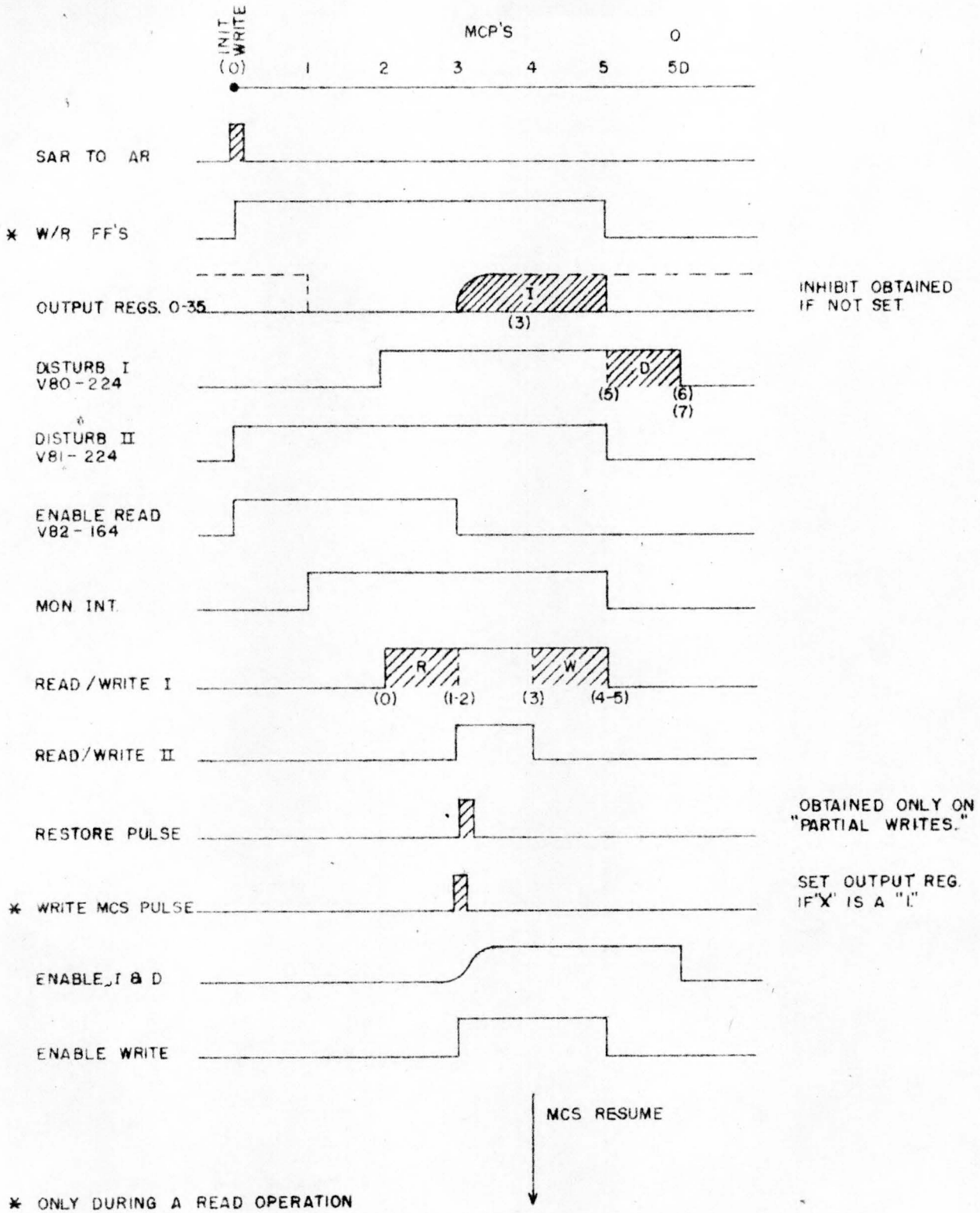
MC READ SEQUENCE

SCC SUBCOMMAND	MCP	MCAC SUBCOMMAND
INIT. READ MCS →	(MCP-0)	SAR → AR (Start MCPD) Set Enable Read to "1" (begin READ ENABLE) Set Disturb II to "1" Set Read to X to "1"
	MCP-1	Set Monitor Intensity to "1" Clear Input Register 0-35
	MCP-2	Set Disturb I to "1" Set Read/Write I to "1" (begin READ PULSE)
	MCP-2 + delay	MCS → X RESTORE MCS 0-14 RESTORE MCS 15-29 RESTORE MCS 30-35
	MCP-3	Clear Enable Read to "0" (end READ ENABLE) Set Read/Write II to "1" (end READ PULSE) Set Enable Write to "1" (begin WRITE ENABLE) Set Enable ID to "1" (begin INHIB. -DIST. ENABLE)
	MCP-4	Clear Read/Write II to "0" (begin WRITE PULSE) MCS RESUME
	MCP-5	Clear Enable Write to "0" (end WRITE ENABLE) Clear Read/Write I to "0" (end WRITE PULSE) Clear Disturb II to "0" (begin DISTURB) Clear Monitor Intensity to "0" Clear Read to X to "0"
	MCP-5 + delay	Clear Enable ID to "0" (end INHIB. -DIST. ENABLE) Clear Disturb I to "0" (end DISTURB)

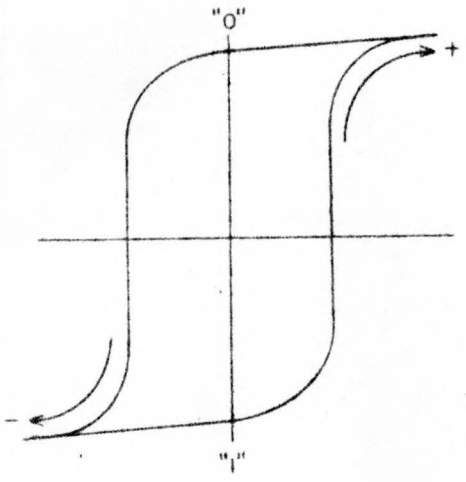
READ OPERATION



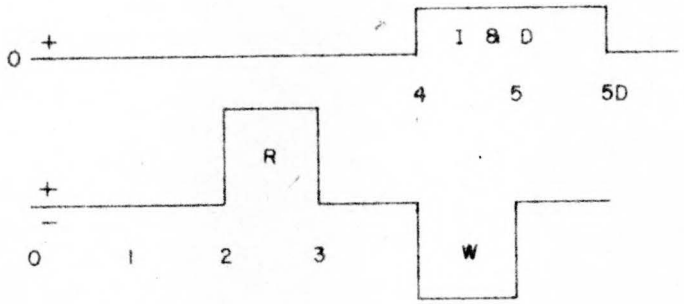
WRITE OPERATION



* ONLY DURING A READ OPERATION



ARBITRARILY ESTABLISHED THAT (+) PULSE PRODUCES CURRENT IN THIS DIRECTION



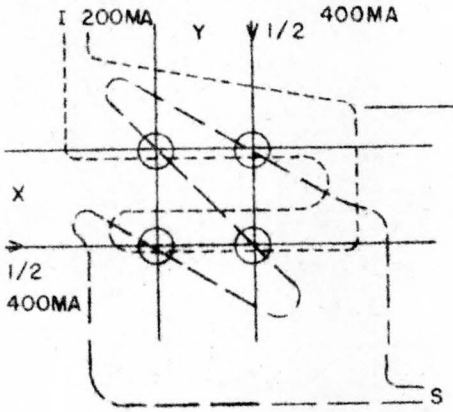
SEQUENCES

READ
1. READ
2. RESTORE
3. DISTURB

WRITE
1. *READ (USED TO CLEAR CORES)
2. WRITE
3. DISTURB

WINDINGS

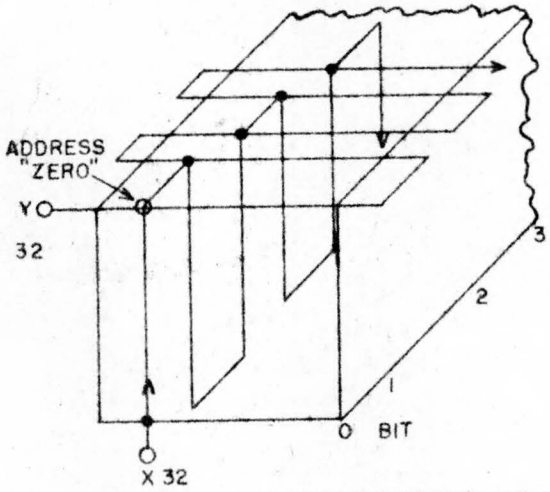
5 LINES: X, Y, 2I, S



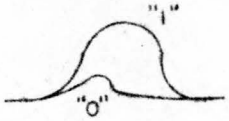
ACTUALLY "INHIBIT" LINE MAKES 2 PASSES THRU EACH CORE. LINES ARE RESTRICTED TO INDIVIDUAL PLANES. (PARTICULAR BIT OF ANY ADDRESS.)

SENSE WINDINGS ARE ALSO RESTRICTED TO INDIVIDUAL PLANES.

X & Y WINDINGS PASS THRU ALL 36 CORES OF A WORD.

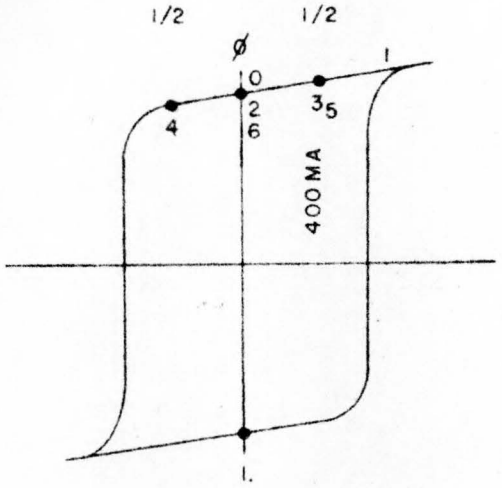


SENSE OUTPUT

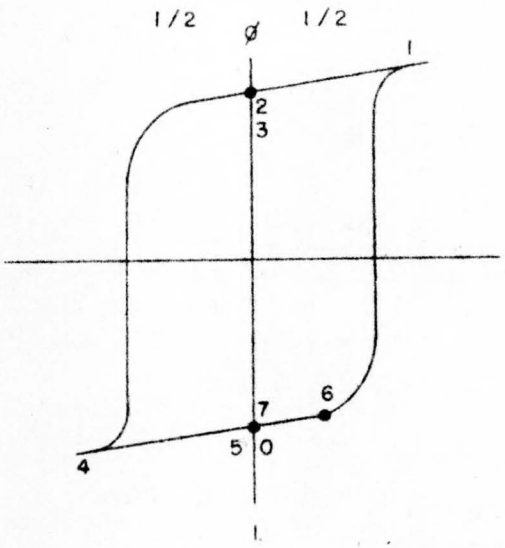


THE X & Y WINDINGS WOULD INTERSECT AT EACH OF THE 36 POINTS OF A SELECTED ADDRESS.

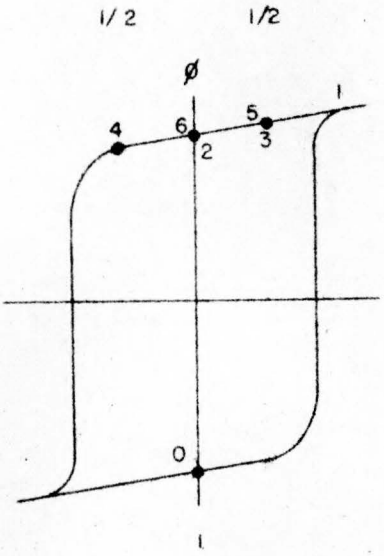
READING A "Ø"



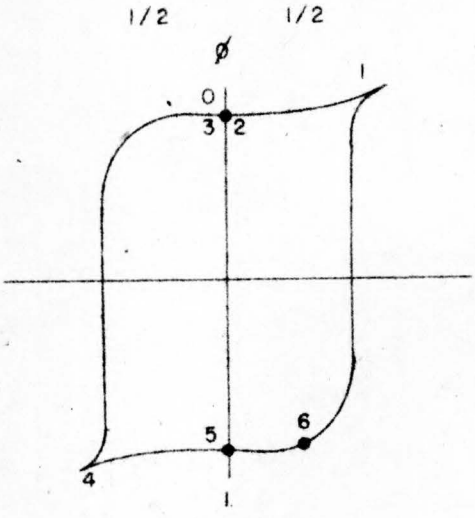
READING A "1"

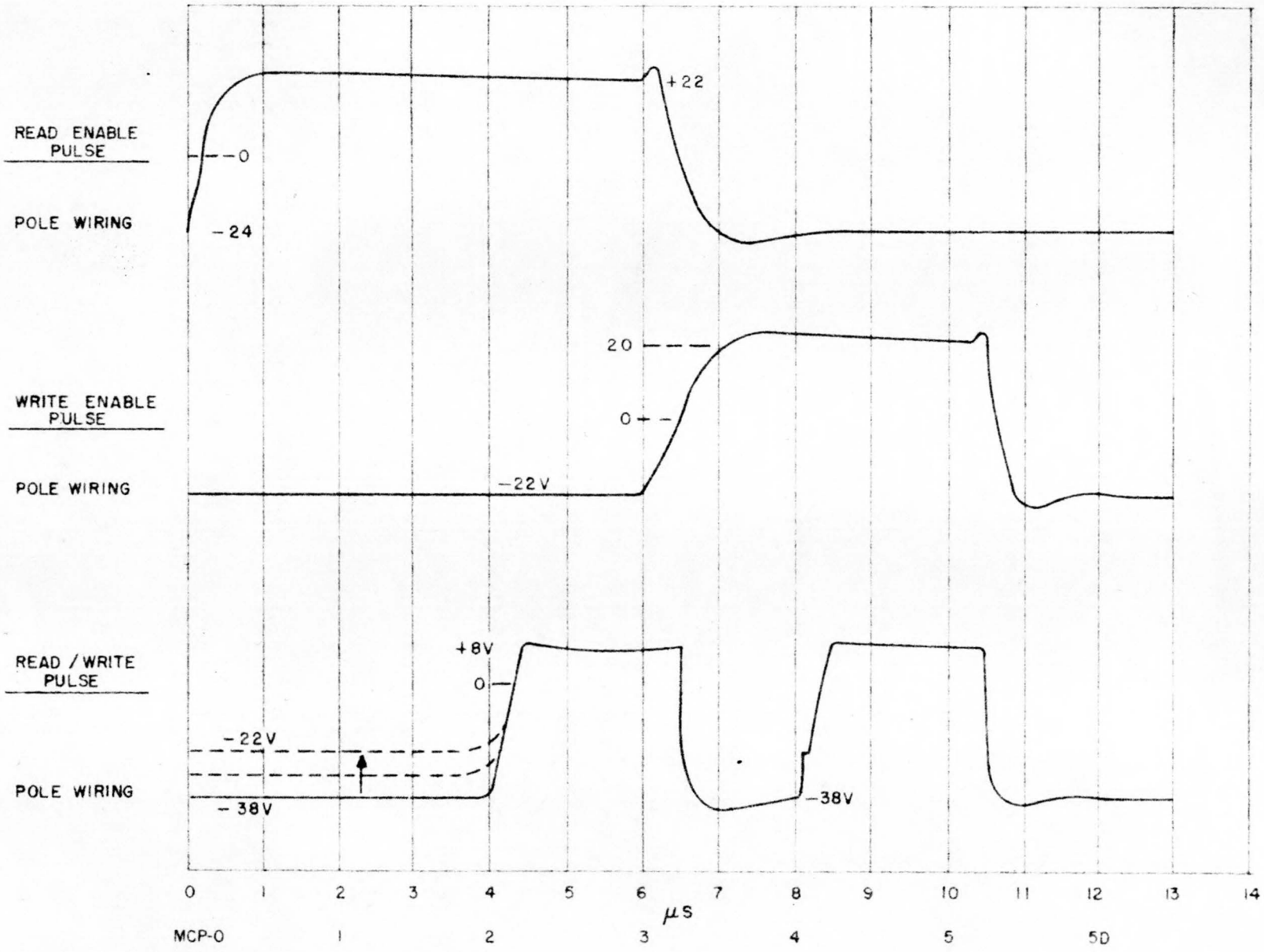


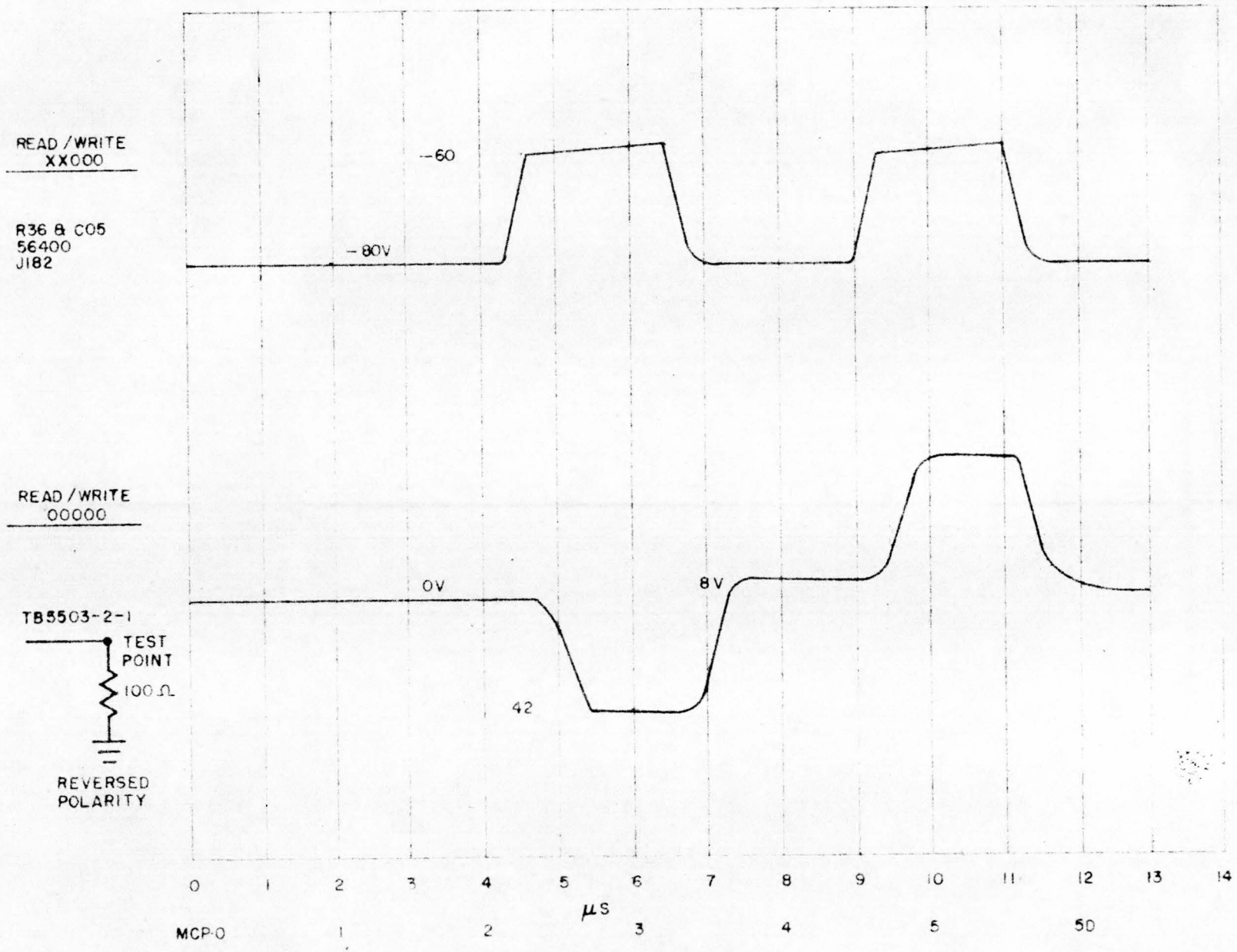
WRITING A "Ø"
OVER A "1"

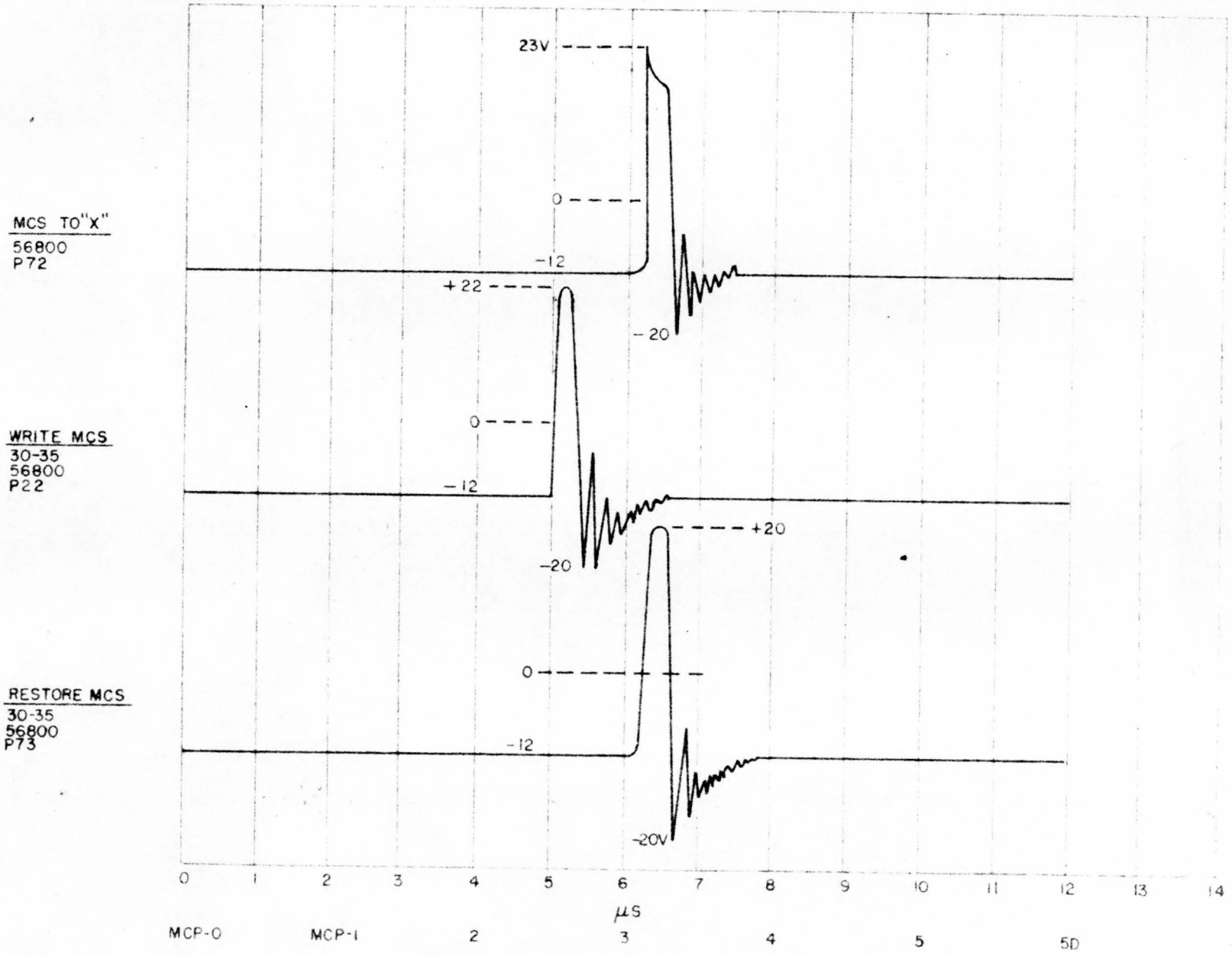


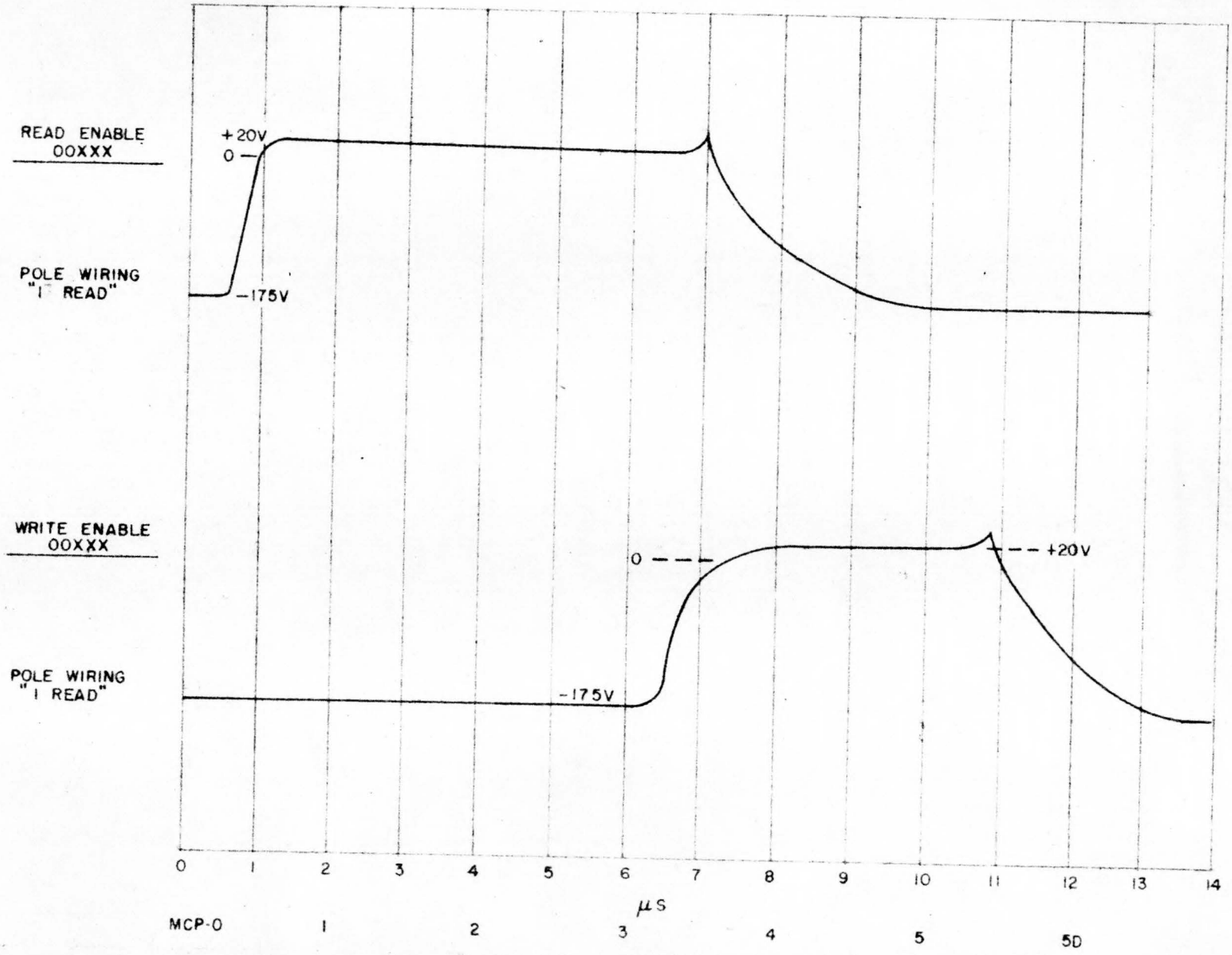
WRITING A "1"
OVER A "Ø"

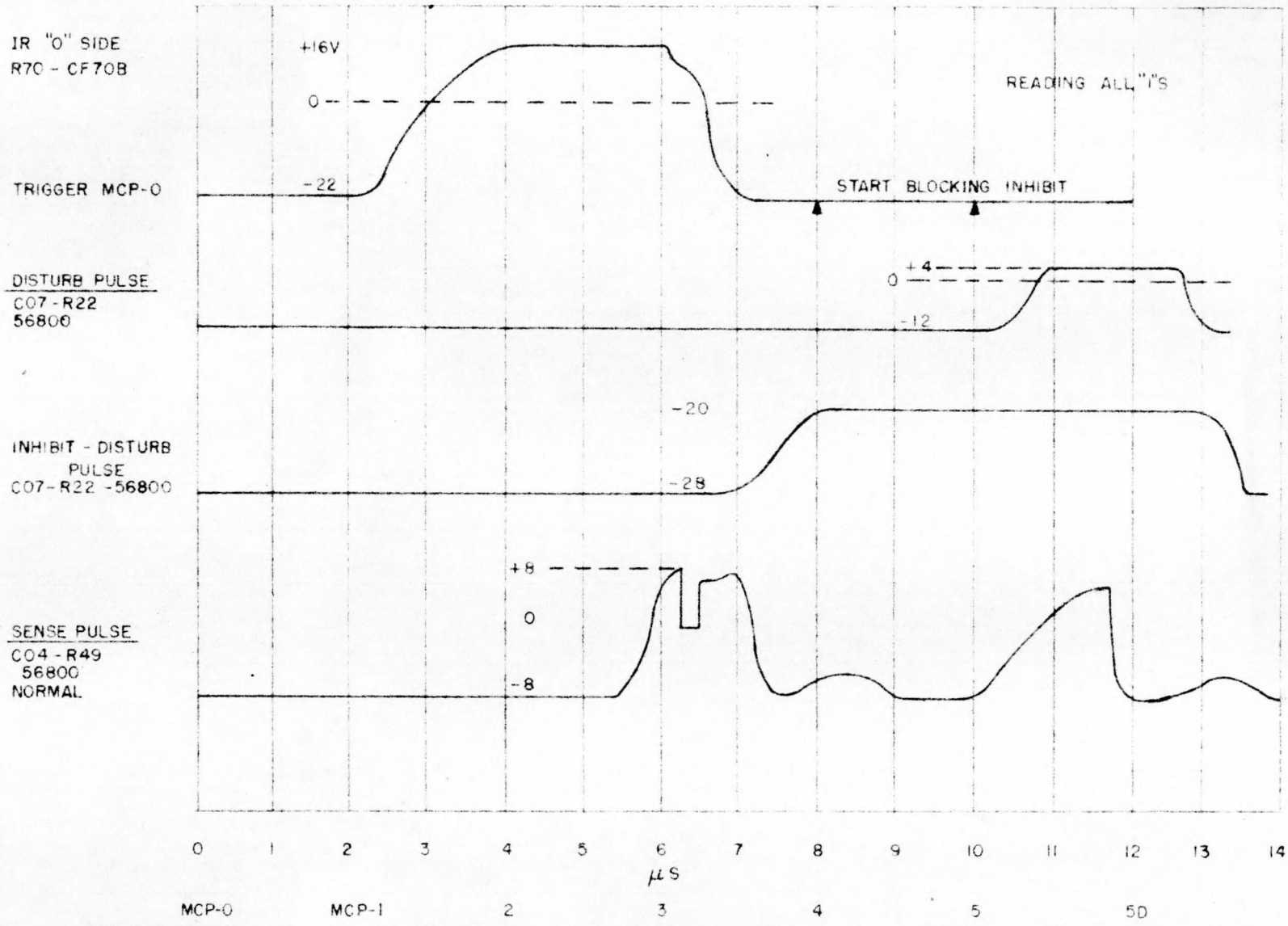


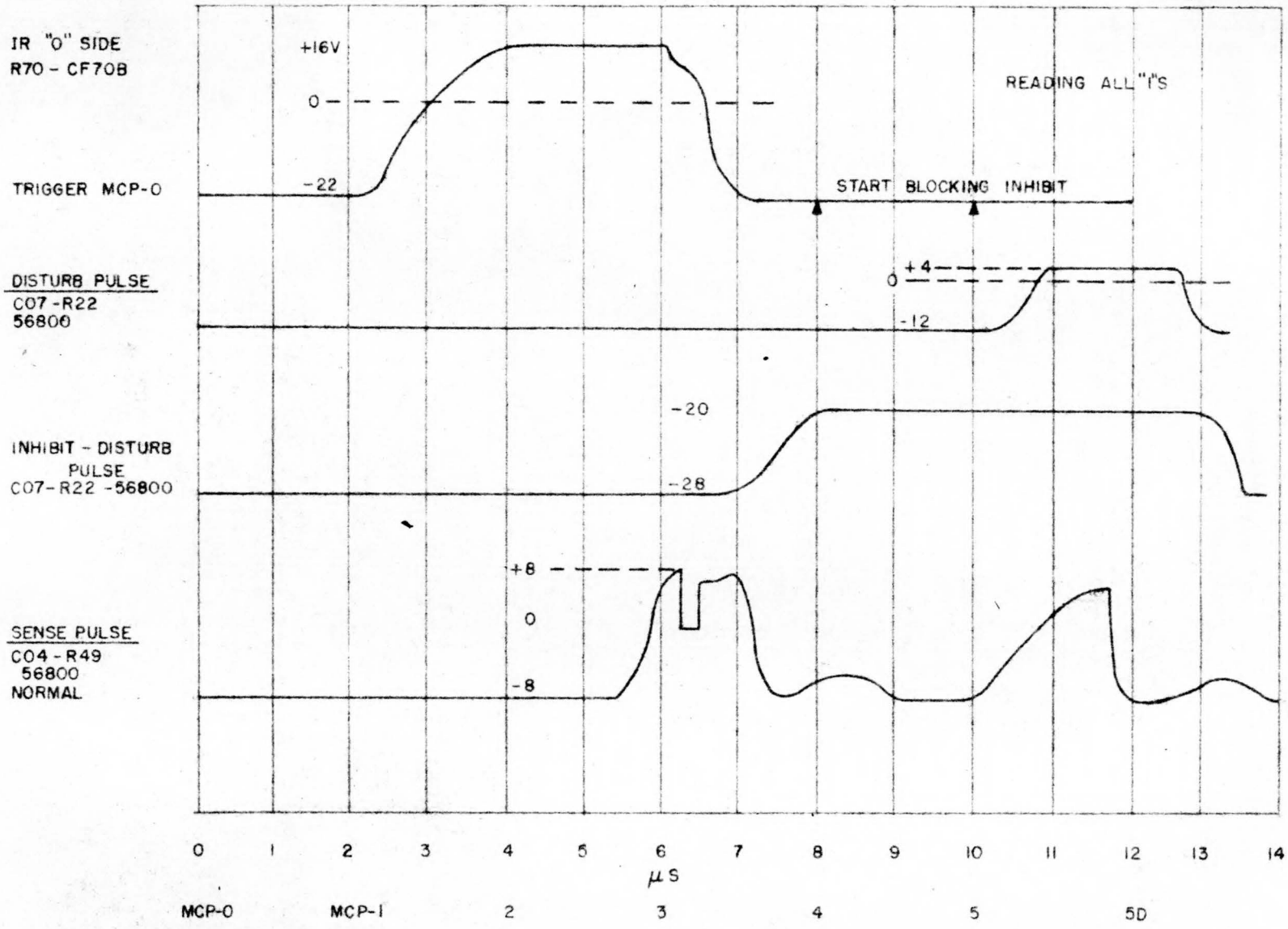

READ ENABLE PULSE
POLE WIRING
WRITE ENABLE PULSE
POLE WIRING
READ / WRITE PULSE
POLE WIRING
+22
0
-24
20
0
-22V
+8V
0
-22V
-38V
-38V
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
μs
MCP-0 1 2 3 4 5 5D


READ / WRITE
XX000
R36 & C05
56400
J182
-60
-80V
READ / WRITE
00000
0V
8V
42
TB5503-2-1
TEST
POINT
100 Ω
REVERSED
POLARITY
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
μS
MCP-0
1
2
3
4
5
50


MCS TO "X"
56800
P72
WRITE MCS
30-35
56800
P22
RESTORE MCS
30-35
56800
P73
23V
0
-12
+22
-20
0
-12
-20
+20
0
-12
-20V
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
μS
MCP-0
MCP-1
2
3
4
5
5D


READ ENABLE
00XXX
+20V
0
POLE WIRING
"1" READ
-175V
WRITE ENABLE
00XXX
0
+20V
POLE WIRING
"1" READ
-175V
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
μS
MCP-0
1
2
3
4
5
5D


IR "0" SIDE
R70 - CF70B
+16V
0
-22
READING ALL "1"S
START BLOCKING INHIBIT
TRIGGER MCP-0
DISTURB PULSE
C07 - R22
56800
+4
0
-12
INHIBIT - DISTURB
PULSE
C07 - R22 -56800
-20
-28
SENSE PULSE
C04 - R49
56800
NORMAL
+8
0
-8
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
μS
MCP-0
MCP-1
2
3
4
5
50


IR "0" SIDE
R70 - CF70B
+16V
0
-22
READING ALL "1"S
TRIGGER MCP-0
START BLOCKING INHIBIT
DISTURB PULSE
C07 - R22
56800
+4
0
-12
-20
INHIBIT - DISTURB
PULSE
C07 - R22 -56800
-28
+8
0
SENSE PULSE
C04 - R49
56800
NORMAL
-8
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
μS
MCP-0
MCP-1
2
3
4
5
5D