b. ELECTROSTATIC STORAGE SYSTEM.

(1) GENERAL. - The Electrostatic Storage System, ES, located in the 50000 cabinet, provides rapid access storage for 1024 36-bit words. The octal addresses 00000 through 01777 are assigned to the system. Since the information stored in ES is volatile a procedure of continuous regeneration must be used to retain the contents while being used, and, if the contents are to be retained after using, the stored words must be transferred to non-volatile storage such as the Output System, the Magnetic Drum Storage System, or the Magnetic Tape Storage System.

ES is divided into several parts. The 36 cathode ray tubes, CRT, provide the actual storage of digital information. The Electrostatic Storage Output Register, ESO, provides temporary storage for words being transferred in or out of CRT. The locating system is composed of the Deflection Register, DR, the Dash Deflection Register, DDR, the Deflection Generator, DG, and the Regeneration Counter, RK. The generation of the storage sequences is performed by the combination of the Electrostatic Storage Access Control, ESAC, and the Electrostatic Pulse Distributor, EPD.

(2) ELECTROSTATIC STORAGE.

(a) CATHODE RAY TUBES. - Electrostatic storage utilizes specially manufactured cathode ray tubes which have five-inch blue phosphor screens of medium persistance luminescence. Both the phosphor coating and the glass serve as the dielectric medium for storage. The pickup electrode which is mounted externally in front of the screen is made of wire mesh whose transparency allows direct observation of the tube screen. The electrode provides a capacitive coupling to the tube's screen allowing any change in charge pattern to produce an external signal.

(b) PRINCIPLES OF ELECTROSTATIC STORAGE. - The screen of the tube is divided into 1024 elemental areas, termed cells; these cells are arranged in

a 32 x 32 grid pattern. The spacing between adjacent cells is approximately three times the electron beam diameter, a distance sufficient to prevent undesirable transfer, or "spilling over", of charges between adjacent cells.

The electron beam is directed at a particular corner of the cell but is prevented from reaching the screen by the control grid. Then a pulse of approximately one microsecond duration is applied to the control grid allowing the beam to reach the screen. The beam must be of sufficient intensity (velocity) to cause secondary emission at the screen; in other words, more electrons must be driven out of the screen than are introduced by the beam. The net result is that a "well" is formed in the corner of the cell by the impinging beam. A "well" in this corner of the cell is identified as a binary "0"; conversely, the absence of a "well" in this corner of the cell is identified as a binary "1". The forming of a "well" where none existed causes a change in charge pattern which is picked up by the wire mesh electrode thus notifying the system that a "1" is present in the cell. If, however, a "well" exists before the beam is turned on, no change (or very little change) is made in the charge pattern, and the pickup electrode receives no signal thus notifying the system that a "0" is present in the cell.

If a "1" is present and therefore a well is formed by the beam, the "1" is changed to a "0" by the beam and the "1" is destroyed. In this case the "1" must be restored. Always, just after the sampling signal applied to the control grid is removed, the electron beam is deflected diagonally across the cell. If a "1" is detected by the original sampling signal, the pickup electrode notifies external circuitry of this fact and a second signal of approximately one microsecond duration is applied to the control grid. This second signal coincides with the diagonal deflection of the beam and "digs a furrow" diagonally across the cell. As the furrow proceeds, the ejected electrons fill the well formed by the first sampling signal as well as most of the "furrow", and, ultimately, a "well" is formed in the diagonally opposite corner of the cell. However, since this new "well" is never probed by the sampling signal, its presence is incidental.

If a "0" is originally present, the pickup electrode finds no change in charge pattern; consequently, no external signal is generated, and no signal is applied to the control grid during the interval in which the beam is being diagonally deflected. Therefore, the "well" is not filled in and the "0" is retained.

Since a "well" slowly fills in with electrons in the absence of an impinging electron beam, the "well" will ultimately disappear or "decay". To prevent decay, all 1024 cells are continuously sampled, one by one, in a systematic manner during those intervals when no storage references (reading or writing) are being made. This procedure is called "regeneration". In the strict sense, only the "0"s need be regenerated since a "1" cannot decay; the "well" in the diagonally opposite corner of the cell from position of a "well" representing a "0" also fills in slowly, but the total absence of such a "well" will not affect the detection of a "1". However, a set sequence is performed for writing, reading, and regeneration, and, since the circuitry cannot establish the content of a cell before sampling, the "1"s are regenerated as well as the "0"s. The regeneration procedure is interrupted during a writing or reading sequence, but a circuit is provided to "remember" the location of the last cell that was regenerated so that the regeneration may continue from that point after the storage reference sequence is completed.

(3) ELECTROSTATIC STORAGE OUTPUT REGISTER. - The Electrostatic Storage Output Register, ESO, is more than its name implies. ESO serves as a temporary storage for words being written in or read from ES. ESO consists of 36 flip-flops and their associated gates. One flip-flop and its gates are associated with each CRT. During each operational cycle, whether writing, reading, or regeneration, ESO is cleared as the cycle is initiated. The following sub paragraphs discuss the operation for the three cycles. The discussion is limited to a single stage of ESO since all stages operate alike.

(a) WRITING. - The ESO flip-flop V51980 is initially cleared. The PROBE signal is applied to the control grid of CRT sampling the content of a cell

and writes a "0" if a "1" exists or strengthens an existing "0". If a "1" is detected, the pickup electrode sends an enable to gate V51903, but since this is a writing operation, the RESTORE signal is not issued. Instead, the WRITE signal is issued which, if a "1" enable is applied to gate V51904 by the X-Register, sets the ESO flip-flop V51980 to the "1" state enabling gate V51901. The DASH signal then passes through V51901 and restores the "1" in CRT. Conversely, if no "1" enable is supplied by the X-Register, gate V51904 is disabled and the WRITE signal is blocked leaving the ESO flip-flop in the "0" state which in turn keeps gate V51904 disabled blocking the DASH signal. Thereby the "0" created by the PROBE signal in CRT is allowed to remain and effectively a "0" in the X-Register stage is written in the corresponding CRT.

(b) READING. - The ESO flip-flop V51980 is initially cleared. Then the PROBE signal is applied to the control grid of CRT sampling the content of a cell and writes a "0" if a "1" exists or strengthens an existing "0". If a "1" is detected, the pickup electrode enables gate V51903 allowing the RESTORE signal to set ESO flip-flop V51980 to the "1" state. Gates V51901 and V51902 are enabled.. the former allows the DASH signal to restore the "1" in CRT, and the latter passes the READ signal which becomes a "1" FROM ES signal. The "1" FROM ES signal is sent to the X-Register setting the corresponding stage to "1". If the PROBE detects a "0" in CRT, nothing further takes place and the corresponding stage in the X-Register is left cleared denoting that a "0" is present in ES.

(c) REGENERATION. - In the absence of either a writing or reading reference the regeneration cycle is repeated continuously each cycle being enacted on a different cell in CRT. After 1024 such cycles have been performed, regeneration starts over with the first cell again. The sequence used for regeneration is exactly like the reading sequence except that no READ signal is produced and therefore no information is transmitted to the X-Register.

(4) LOCATING SYSTEM. - The locating system is used to direct the electron beams in all 36 storage tubes to the same cell position or address. A sec-

ondary function is to provide the dash deflection voltages used for restoration and writing "1"s. The system consists of the Address Source flip-flop, the Deflection Register, DR, the Dash Deflection Register, DDR, the Deflection Generator, DG, and the Regeneration Counter, RK.

(a) ADDRESS SOURCE. - The source of the address to be used in an operation can be either SAR or the Regeneration Counter, RK. Control over the choice of address is controlled by the Address Source flip-flop, V80 located on the chassis of Jack 50063. This stage has gates on both enables. When writing or reading is to take place, the INITIATE WRITE signal or INITIATE READ signal set the flip-flop to the "1" state enabling the gate on the "1" side which allows EP-0 (a distributed clock pulse discussed below) to sample gates enabled by SAR and thus provides the SAR address to the system. EP-0 also resets the flip-flop to the "0" state. When in the "0" state the flip-flop enables its "0" gate allowing EP-0 to sample gates enabled by RK and thus provides the regeneration address to the system. Therefore if reading or writing is to take place, ES receives its address from SAR, otherwise the address is taken internally from RK.

(b) DEFLECTION REGISTER. - The Deflection Register, DR, receives the ES address from SAR or RK and provides enables to the Deflection Generator, DG. DR consist of 10 flip-flops and is divided into two parts of five flip-flops each. One half receives the five lower order address bits and provides enables for the horizontal deflection generators. The other half receives the five higher order address bits and provides enables for the vertical deflection generators. The 10-bit address received by DR may come from either SAR or RK depending on the operation to be performed.

(c) DASH DEFLECTION REGISTER. - The Dash Deflection Register, DDR, supplies enables to the deflection generator which ultimately deflect the electron beams in CRT diagonally across the referenced cells. This deflection is coincident with the DASH signal and is used to write "1"s. DDR consists of two flip-flops; the enables from DD I are applied to the horizontal deflection generator and the enables from DD II are applied to the vertical deflection generator. Since these enables are applied simultaneously, the net result is to generate voltages in both

generators that drive the beams at 45° or diagonally across the cells. The DDR enables last approximately three microseconds and the DASH signal occupies approximately the first microsecond of that interval.

(d) DEFLECTION GENERATOR. - The Deflection Generator, DG, generates pairs of push-pull deflection voltages that are applied to the electrostatic deflection plates in CRT. DG consists of 12 stages of current adding networks; six stages are associated with the horizontal deflection and six stages with the vertical deflection. Five stages in each set develop the deflection voltages used in the cell (address) location and the sixth stage in each set supplies a component of the dash deflection. Each stage consists of a pair of triode amplifiers with the exception of the dash deflection stage which has a pair of pentode amplifiers. The stages differ from one another by having different cathode load resistors arranged in a descending geometric series (see following paragraph). The enables from DR and DDR are applied to the control grids of the tubes thus allowing conduction or cutoff depending on the state of the register flip-flops. In each stage, the "0" enable from the register leads to one amplifier and the "1" enable leads to the other amplifier. In the horizontal generator, the plate leads of the "0" amplifiers are tied together and lead to one of a set of horizontal electrostatic electrodes in CRT. The plate leads of the "1" amplifiers are also tied together and go to the opposing electrostatic electrodes. The same circuitry is used in the vertical generator.

The amplifiers leading to the lowest order DR flip-flop (DR_0) both have cathode load resistors of a value, R. The amplifiers associated with DR_1 have cathode load resistors of a value R/2. The amplifiers associated with the fifth stage (highest order), DR_4, have cathode resistors of a value R/16 thus establishing a binary progression. Since the "0" amplifiers in the horizontal generator have their plates tied together, all stages that are conducting draw current proportionate to their respective cathode resistor values. These currents are summed and the resultant voltage across the plate resistor is applied to one side of the

horizontal electrodes of a set in CRT. The voltage developed across the common plate resistor of the "1" amplifiers is applied to the opposing electrodes of a set in CRT. These voltages operating in push-pull deflect the electron beams in all 36 CRT to the same point horizontally. The vertical generator performs in like manner and thus a particular cell location is selected.

While in that location, equal voltages are applied later to both the horizontal and vertical electrodes by the dash generators. (These stages have cathode resistors of a value 2R.) These new current summations reflect the beam diagonally across the cell.

Because of the nature of the adding networks a short period of time must be allowed for the summation currents to stabilize and select a cell position before applying the PROBE signal. For this reason, the distributed clock pulse, EP-1 (discussed later), is not used since this time interval is needed to allow the electron beams to come to rest. However, during the dash interval, the movement of the beam as the dash deflection voltages are applied are capitalized upon by applying the DASH signal coincidentally thus digging the "furrows" as the beams move the length of one cell position diagonally.

(e) REGENERATION COUNTER. - The Regeneration Counter, RK, is used to provide and keep track of the orderly sequence of regeneration addresses. RK is a ten-stage binary counter which counts from 0 to 1023 (decimal). The enables from RK lead to gates which are sampled by EP-0 when the address is not being supplied by SAR. EP-0 is also used to advance the count in RK except during a storage reference when SAR is used as an address source.

The count from RK is not supplied consecutively to DR. It will be noted that the interlace provides orderly but not consecutive addresses. This is done to prevent repeated references to the same portion of CRT which could develop undesirable "splash". Splash is an effect of secondary emission in which the ejected electrons fall into adjacent cells. Splash, of course, is always present to a li-

mited extent but the problem is to prevent excessive splash by probing too small an area. Accordingly the regeneration address are interlaced to widen the probed area as much as possible.

(5) SEQUENCE GENERATION. - The electrostatic storage sequence is derived by the combination of the Electrostatic Pulse Distributor and the Electrostatic Storage Access Control.

(a) ELECTROSTATIC PULSE DISTRIBUTOR. - The Electrostatic Pulse Distributor, EPD, is used to provide a four-pulse cycle which governs the sequences in ES. This cycle is derived from the 500 kc CLOCK PULSES and is repeated every eight microseconds. EPD consists of two flip-flops, four gates and associated "and" circuits. The flip-flops form a two-stage binary counter. Each set of four CLOCK PULSES produces a cycle in which the issued pulses are two microseconds apart. Only three of the four pulses are sent to the Electrostatic Storage Access Control; these, in a single cycle, are the first, third and fourth pulses, identified respectively as EP-0, EP-2, and EP-3. The second pulse, EP-1, is used only within EPD and the time interval caused by this gap is used to allow the deflection voltages in DG to stabilize.

(b) ELECTROSTATIC STORAGE ACCESS CONTROL. - The Electrostatic Storage Access Control, ESAC, provides the signals that govern the ES sequences for writing, reading, and regeneration. During each sequence, ESAC allows the EPD signals to produce a specific pattern of sub commands which perform the storage operation. If no signal is received from Main Control, such as one of the initiate write signals or the INITIATE READ ES signal, the regeneration sequence is performed. If a signal is received from Main Control, the operation is varied accordingly.

During the regeneration sequence and when the equipment is in the TEST condition, the contents of ES can be changed manually by the operation of the FORCE ONES switch or the FORCE ZEROS switch. When not in TEST condition but in the NORMAL condition, K30013 is energized. The contacts of K30013 apply -80vdc to the screen grids of the amplifiers V06 & V07-091 and V03-091. When in the TEST

condition these contacts are open allowing the FORCE ONES and FORCE ZEROS switches to be operative. If its is desired to write all "0"s in ES, opening the FORCE ZEROS switch, S40220, removes screen grid voltage on the amplifier preventing the production of the DASH signal and dash deflection voltages. Thereafter, no "1"s are written and after 1024 cycles all cells in ES will contain "0". If it is desired to write all "1"s in ES, the FORCE ONES switch, S42019 is opened removing screen grid voltage from the associated amplifiers. This action blocks the CLEAR ESO signal. Then each ESO stage is manually set to "1" and after 1024 cycles all cells in ES will contain "1"s.

(6) ADDRESS MONITOR.- The Address Monitor is a five-inch cathode ray tube mounted above the Maintenance Panel. It is used to give a visual display of the addresses (cells) being referred to in ES. It is especially useful if the ES references get into an iterative loop. The display of such a loop becomes more intense and the address references may be seen easily. The deflection voltages used to position the beams in the storage tubes go also to the electrostatic deflection electrodes of the monitor tube. At the end of each storage reference, EP-3 causes an ES RESUME signal to be sent to Pulse Distributor Control; this same signal is shaped in an ESAC chassis (in J50063) and applied to the control grid of the Address Monitor tube allowing the beam to reach the screen. This causes a display of the cell being referred to. Since the beam is turned on for several microseconds only, the display is not conspicuous unless repeated a number of times at the same address. In this way repeated references indicating an iterative loop become apparent.

TABLE 2-
WRITE SEQUENCE (0-35)

SCC Command	EP	ESAC Command
Init Write ES (0-35) →		Set WR Sync (0-35) FF Set Address Source FF
	EP-0	Clear DD I FF Clear DD II FF Set Probe II FF Clear Dash I FF Clear ESO stages SAR → DR Clear Address Source FF Set WR/REST (0-14) FF Set WR/REST (15-29) FF Set WR/REST (30-35) FF Clear WR Sync (0-35) FF
	EP-2	Set Probe I FF, begin Probe Set Dash II FF Initiate 1.1 u-sec delay
	EP-2+1.1 u-sec delay	Write (0-14) Write (15-29) } (X → ESO) Write (30-35) Clear WR/REST (0-14) FF Clear WR/REST (15-29) FF Clear WR/REST (30-35) FF Clear Probe II FF, end Probe Set DD I FF Set DD II FF } begin Dash (ESO → ES) Set Dash I FF Initiate 1.1 u-sec delay
	EP-3	Clear Probe I FF ES Resume (to ARAC)
	EP-2+2.2 u-sec delay	Clear Dash II FF, end Dash

TABLE 2-
WRITE SEQUENCE (0-14)

SCC Command	EP	ESAC Command
Init Write ES (0-14) →		Set WR Sync (0-14) FF Set Address Source FF
	EP-0	Clear DD I FF Clear DD II FF Set Probe II FF Clear Dash I FF Clear ESO stages SAR → DR Clear Address Source FF SET WR/REST (0-14) FF Clear WR Sync (0-14) FF
	EP-2	Set Probe I FF, Begin Probe Set Dash II FF Initiate **I.1 u-sec** delay
	EP-2+1.1	Write (0-14) (X → ESO 0-14) Restore (15-29) Restore (30-35) (ES → ESO 15-35) Clear WR/REST (0-14) FF Clear Probe II FF, end Probe Set DD I FF Set DD II FF begin Dash (ESO → ES) Set Dash I FF Initiate 1.1. u-sec delay
	EP-3	Clear Probe I FF ES Resume (to ARAC)
	EP-2+2.2 u-sec delay	Clear Dash II FF, end Dash

TABLE 2-
WRITE SEQUENCE (15-29)

SCC Command	EP	ESAC Command
Init Write (15-29)		Set WR Sync (15-29) FF SET ADDRESS SOURCE FF
	EP-0	Clear DD I FF Clear DD II FF Set Probe II FF Clear Dash I FF Clear ESO stages SAR → DR Clear Address Source FF Set WR/REST (15-29) FF Clear WR Sync (15-29) FF
	EP-2	Set Probe I FF, begin Probe Set Dash II FF Initiate 1.1 u-sec delay
	EP-2+1.1 u-sec delay	Write (15-29) (X → ESO 15-29) Restore (0-14) } (ES → ESO 0-14,30-35) Restore (30-35) } Clear WR/REST (15-29) FF Clear Probe II FF, end Probe Set DD I FF } Set DD II FF } begin Dash (ESO → ES) Set Dash I FF } Initiate 1.1 u-sec delay
	EP-3	Clear Probe I FF ES Resume (to ARAC)
	EP-2+2.2 u-sec delay	Clear Dash II FF, end Dash

TABLE 2-
READ SEQUENCE

SCC Command	EP	ESAC Command
Init Read ES →		Set RD Sync FF Set Address Source FF
	EP-0	Clear DDI FF Clear DD II FF Set Probe II FF Clear Dash I FF Clear ESO stages SAR → DR Clear Address Source FF Clear RD Sync FF
	EP-2	Set Probe I FF, begin Probe Set Dash II FF Initiate 1.1 u-sec delay
	EP-2+1.1 u-sec delay	Restore (0-14) Restore (15-29) } (ES → ESO) Restore (30-35) Clear Probe II FF,,end Probe Set DD I FF Set DD II FF } begin Dash (ESO → ES) Set Dash I FF Initiate 1.1 u-sec delay
	EP-3	Read (ESO → X) Clear Probe I FF Clear Read FF ES Resume (to ARAC)
	EP-2+2.2 u-sec delay	Clear Dash II FF, end Dash

TABLE 2-
REGENERATE SEQUENCE

SEC Command	EP	ESAC Command
(none) →	EP-0	Clear DD I FF Clear DD II FF Set Probe II FF Clear Dash I FF Clear ESO stages - RK → DR Advance RK
	EP-2	Set Probe I FF, begin Probe Set Dash II FF Initiate 1.1 u-sec delay
	EP-2+1.1 u-sec delay	Restore (0-14) Restore (15-29) } (ES → ESO) Restore (30-35) Clear Probe II FF, end Probe Set DD I FF Set DD II FF } begin Dash (ESO → ES) Set Dash I FF Initiate 1.1 u-sec delay
	EP-3	Clear Probe I FF
	EP-2+2.2 u-sec delay	Clear Dash II FF, end Dash