MAGNETIC PERIPHERALS, INC.
a Control Data Company

INTERFACE SPECIFICATION

FOR iPi-2

INTELLIGENT PERIPHERAL INTERFACE

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a Control Data Company

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INTERFACE SPECIFICATION

FOR IPI-2

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Released

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1.0 SCOPE

This document defines the Level 2 Intelligent Peripheral Interface (IPI-2) used on Magnetic Peripherals Inc. Disk Drive products.

2.0 APPLICABLE DOCUMENTS

SPEC 64731602 - Interface Specification - IPI Physical Level Applicable Disk Drive Product Specification

3.0 GENERAL DESCRIPTION

3.1 Introduction

The IPI-2 is an implementation of the IPI Physical Interface Standard and the IPI Device Specific Command Set for disk drives. The Physical level defines the cables, connectors and drivers/receivers as well as the bus protocol and state sequences. The logical level defines the device level command set, the disk format and timing critical operations.

The IPI-2 is a 16-bit parallel disk drive interface designed for high speed transfer of commands, status and data between a controller and a disk drive. The controller provides control for up to 8 disk drives through the IPI with a device level set of commands and data transfers. Commands and responses are transferred in the interlocked mode. Data is transferred in the non-interlocked mode. Data rates of up to 80 MHz can be obtained in the non-interlocked mode, depending on driver and receiver classes.

The IPI is a state driven interface. Only 1 control line changes on the interface per valid state transition. The control lines are defined in 8.1 of this specification. The state of the interface is determined by the condition of the control lines. The valid IPI states are defined in 8.2. The valid paths between states are defined by the state sequences. These sequences are defined in 8.3.

3.2 Controller Responsibility

- Data buffering
- Data management - interleaving
- Header management
- Defect management - defect skipping, revectoring, spare sectors
- Error correction and detection - retries, ECC, CRC
- Command generation
- Formatting diagnostic track

3.3 Drive Responsibility

- Sectoring - fixed or variable length sectors
- Formatting - multiple fields
- Gap management - PLO, pads, interfield gaps
- Read Gate and Write Gate control
- PLO, bit and octet synchronization
- Header verification for write commands
- Command execution
- Response generation
- Optional error detection and correction
- Internal diagnostics execution

4.0 GLOSSARY OF TERMS

Bus Control - The octet issued on Bus A by the controller during the Bus Control sequence. It is used to define the bus configuration and information type for the subsequent Information Transfer. The 3 Bus Control types are; Command Control, Response Control and Data Control.

Command - The information transferred from the controller to the drive following a Command Control. The information contains command specific parameters.

Command Control - A Bus Control which specifies that command information is to be transferred from the controller to the drive during the Information Transfer and identifies the command to be executed.

Controller Status - The status issued by the controller during the Ending Status sequence after the Information Transfer. -

Data Control - A Bus Control which specifies that data information is to be transferred during the Information Transfer, and various data transfer requirements including the orientation of the data on the disk.

Defect Map - A list of the defects on the media, which is written on the last cylinder. This information is supplied by the manufacturer.

Drive Status - The status issued by the drive during the Ending Status sequence after an Information Transfer.

Format Specification - An ordered list of parameters which specify the format of the tracks and sectors on the disk.

Information Transfer - The transfer of commands, responses and data.

Native - This term refers to the unique disk drive before the IPI-2 configuration is added.

Response - The information transferred from the drive to the controller following a Response Control. The information contains parameters specific to the response type.

Response Control - A Bus Control which specifies that response type information is to be transferred from the drive to the controller during the Information Transfer and identifies the type of response.

Signal Nomenclature - The nomenclature used to define voltage levels, signal states, logic states and their correlation (see Table 1). Bits/Bytes referred to as "Reserved" are defined to be logic zero.

Status Response - The status supplied to the controller when executing a Read Status Response which contains the exception status bits.

Target Sector - The physical sector designated by the controller for RPS and Data Controls which operate on target sectors.

Time Dependent Operation (TDO) - An operation that requires mechanical action and cannot be completed for some "time" i.e. a seek.

5.0 ACCESSORIES

Accessory items required by the IPI-2, but not furnished with the device, are listed in Table 2.

6.0 PHYSICAL INTERFACE

The IPI interface provides a terminated, differential transmission system for long distances and/or noisy electrical environments. A IPI subsystem configuration may consist of up to 8 IPI-2 disk drives daisy-chained to a disk controller (see Figure 1). The total cable length of the daisy-chain must not exceed 150 feet per port.

6.1 Cables, Connectors, and Mating Components

The IPI has a single 50 conductor I/O cable per port. Shielded cables are used to meet FCC/VDE requirements. Shielding is utilized to minimize cross-talk and reduce inductive coupling due to static discharge as well as control impedance variations regardless of cable lay.

Each cable is manufactured with a male cable connector on one end and a female connector on the other end. This connector scheme allows cables to be joined if a drive has to be removed from the daisy-chain. Such cable abutments should be limited to minimize signal degradation.

The controller must provide a female connector for each port. The drive provides both a female and male panel connector for each port. Each drive port connector supports both flat and round cable connectors. Connector retention is provided with a Jackscrew assembly (see Figure 2). The innermost Jackscrew pair is for round cable connectors. The outermost pair is for flat cable connectors.

- Round Cable (Shielded)

Type:	Bundled twisted pair with overall shield
Number of Conductors:	50 (25 twisted pair)
Impedance:	120 ±12 Ω
Wire Size:	28 AWG
Propagation Delay:	1.7 ±0.2 ns/foot
Maximum Cable Length:	150 ft. cumulative
Part Number:	CDC 15473035

- Cable Connector (50 Position Subminiature "D")

Plug:	CDC	10129660
	AMP	205212-3
Receptacle:	CDC	10129655
	AMP	205211-2

- Connector Retention Hardware

Female Screwlock:	AMP	205817-3
Male Standoff Stud:	AMP	747865-1
Female Jackscrew Kit:	AMP	747863-3
Male Jackscrew Kit:	AMP	747784-3

6.2 Signal Lines

See Table 4 for I/O pin assignments.

7.0 ELECTRICAL INTERFACE

The IPI Interface allows powering on and off individual units without glitching the interface. Any unit(s) may be powered off without loss of transmission noise margin. In the case of the ATTENTION IN signal, it is possible that up to 8 drives may be simultaneously signalling an attention condition. The receiver output will remain active when any combination of the 8 drives are signalling attention. The drive will complete a power on reset with all transmitters enabled.

7.1 Transmitters and Receivers

Transceivers of the type DS3695 are used to provide a terminated, differential transmission system. This transceiver meets the requirements of the EIA Standard RS-485 which specifies the electrical characteristics of drivers and receivers for use in a balanced, digital multipoint system.

7.1.1 Differential Driver Characteristics

Driver Type:	Differential, Glitchless
Driver Input:	TTL compatible
Input Low Level Voltage:	0.8 V max
Input High Level Voltage:	2 V min
Driver Common Mode Voltage:	3.0 V max (R_L = 54 Ω)
Diff. Driver Output Voltage:	1.5 V min (With load, R_L = 54 Ω)
Driver Tri-State Output Current:	± 100 µA max
Propagation Delay:	
Driver Input to Output:	22 ns max
Driver Skew (Output To Output):	8 ns max
Driver Enable to Output High:	50 ns max
Driver Disable Time:	30 ns max
Recommended Part Number:	CDC 15125805 National Semiconductor DS3695

7.1.2 Differential Receiver Characteristics

Receiver Type:	Differential, Glitchless
Receiver Output:	TTL compatible
Receiver Common Mode Voltage:	-7 V to +12 V
Input Low Level Voltage:	0.8 V max
Input High Level Voltage:	2 V min
Voltage, Output Low:	0.5 V max
Voltage, Output High:	2.4 V min
Receiver Hysteresis:	70 mV typ.
Diff. Input Threshold Voltage:	± 0.2 V
Receiver Input Resistance:	12 kΩ min
Receiver Output Off Current:	± 20 µA max
Propagation Delay:	
Receiver Input to Output:	37 ns max
Receiver Enable to Output:	20 ns max
Receiver Disable:	16 ns max
Recommended Part Number:	CDC 15125805 National Semiconductor DS3695

7.2 Termination

Each signal pair shall be terminated at both the controller and the last drive on the daisy-chain. This resistance is provided on the drive with a 150 Ω (±5%) resistor from signal pin (+) to signal pin (-) (see Figure 3).

7.3 Line Bias

Each signal line pair shall be biased at the controller by installing a 560 Ω (±5%) resistor from signal (-) to +5 V and a 560 Ω (±5%) resistor from signal (+) to ground. The line bias is required to enforce an inactive (zero) state when the signal pair is released. The controller end of the transmission line is terminated with a 150 Ω (±5%) resistor as part of the line bias network (see Figure 3).

8.0 PROTOCOL

This section provides signal definitions, state, sequence and Maintenance Mode descriptions. The terms In and Out are always used in reference to the controller.

Command, Response, and Data type information exchanges are transferred in the double octet (16-bit) mode. Even numbered octets are transmitted on BUS A and odd numbered octets are transmitted on BUS B, i.e., the octet on BUS A is considered as being transmitted before the octet on BUS B. The most significant octet is transferred first in multi-octet parameters (see Table 5).

For Command and Response information, bit 7 of an octet is the most significant bit. For data information, there is no definition to the ordering of bits or octets. The order of the octets read is the same as that which were written.

8.1 Signal Definitions

The IPI interface consists of 24 signal lines (see Figure 4). The control signals (SELECT OUT, SLAVE IN, MASTER OUT, SYNC IN and SYNC OUT) are used to determine the state of the interface. The bidirectional bus signals (BUS A and BUS B) are used to transfer information between the controller and the drive. The asynchronous ATTENTION IN signal notifies the controller that the drive requires service.

8.1.1 BUS A

BUS A consists of 9 lines (Bits 7 - 0 plus parity). Parity is odd. BUS A is released by all drives when SELECT OUT is negated. BUS A is used by the controller for all control sequences.

8.1.2 BUS B

BUS B consists of 9 lines (Bits 7 - 0 plus parity). Parity is odd. BUS B is used by the drive for all control sequences.

8.1.3 Select Out

SELECT OUT is sent from the controller to the drive(s) to select a drive and maintain selection. When SELECT OUT is inactive all drives release BUS A.

8.1.4 Slave In

SLAVE IN is sent by the drive to indicate acknowledgment of controller initiated control sequences, to terminate Information Transfers, or to acknowledge Request sequences.

8.1.5 Master Out

MASTER OUT is used by the controller to initiate or terminate Information Transfers, Request Interrupts, Request Drive Interrupts, Request Transfer Settings, or Reset Drive(s).

8.1.6 Sync In

When the drive asserts SYNC IN during transfers In, information is valid on the bus(es). When SYNC IN is asserted during transfers Out the drive is ready to accept information. SYNC IN is also asserted to acknowledge the Bus Control Byte during the Bus Control sequence.

8.1.7 Sync Out

When the controller asserts SYNC OUT during transfers In the information has been accepted. When SYNC OUT is asserted during transfers Out information is valid on the bus(es). SYNC OUT is also asserted to initiate the Bus Control sequence.

During any reset, SYNC OUT is asserted without response.

8.1.8 Attention In

ATTENTION IN is a common wired "OR" signal for one or more drives to inform the controller that service is requested. The controller has the responsibility to service the interrupts as required.

The ATTENTION IN signal is activated by the drive when the RPS Interrupt, Command Completion Interrupt, No Longer Busy Interrupt, or Status Pending Interrupt is active. Command functions are provided to enable and disable the individual interrupts that generate an Attention on a port basis. All Attention generation except No Longer Busy is enabled upon RESET. The Busy to Not Busy Attention is enabled only in response to the Enable No Longer Busy Command.

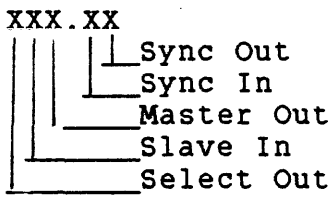
The ATTENTION IN signal does not contribute to determining the state of the interface. It will not be asserted if the drive is selected nor will it be driven inactive.

8.2 States

The IPI-2 is a state driven interface, i.e., only 1 control line changes on the interface for each state transition. The state of the interface is defined by the condition of the control signals; SELECT OUT, SLAVE IN, MASTER OUT, SYNC IN, and SYNC OUT. With the exception of non-interlocked transfers, these signals are interlocked between the controller and the drive.

Figure 5 illustrates the defined states and the possible paths (sequences) between them. Not all sequences are valid. The valid sequences are defined in 8.3.

State Definition:



8.2.1 Idle (000.00)

The IDLE state is entered when all of the control signals are inactive. Abnormal entries to this state occur whenever the controller and drive(s) recognize an undefined state or state transition. The buses are released prior to entering the IDLE state except during the Request Interrupts and Master Reset sequences.

8.2.2 Maintenance (0X0.X1)

The MAINT state initiates Maintenance Mode on all drives. The controller initiates the Maintenance Mode by executing a Master Reset sequence. The MAINT State is an emergency state and is used by the Controller to exit any condition of protocol hang on the IPI-2.

8.2.3 Request (001.00)

The REQUEST state causes the drive(s) to respond with its significant address bit in the Radial Address Octet, the Drive Interrupts Octet, the Transfer Settings Octet, or to initiate Selective Reset.

8.2.4 Request Acknowlege (011.00)

The REQUACK state is entered by the drive in response to the REQUEST state. The REQUACK state is used to present the Transfer Settings and the current Drive Interrupts to the controller

8.2.5 Selective Reset 1 (001.01)

The RESETSEL 1 state initiates a reset of the drive identified by the Selective Reset Control Octet on BUS A, and terminates Maintenance Mode.

8.2.6 Selection (100.00)

The SELECT state is entered by the controller to initiate selection of the drive or to transfer Controller Status to the drive. In the SELECT state it is necessary for the controller to know the previous transition in order to respond correctly. When entered from IDLE, it is a true Selection (and the drive responds with Select Status on BUS B). When entered from SLAVEND, SELECT is an intermediate state following an Information Transfer between the controller and the selected drive

8.2.7 Slave Acknowledge (110.00)

The SLAVACK state is initiated by the drive to acknowledge either Selection, the end of a Bus Control sequence, or the end of an Information Transfer.

In the SLAVACK state it is necessary for the controller to know the previous transition because the response depends on the state from which SLAVACK was entered.

8.2.8 Deselection (010.00)

The DESEL state initiates the deselection of the drive by the controller.

8.2.9 Bus Control (110.01)

The BUSCTL state is used by the controller to initiate control of the subsequent Information Transfer.

8.2.10 Bus Acknowledge (110.11)

The BUSACK state acknowledges that the Bus Control Octet has been accepted by the drive.

8.2.11 Master End (110.10)

The MASTEND state is initiated by the controller to terminate an Information Transfer or to acknowledge acceptance of the Bus Acknowledge Octet.

8.2.12 Transfer Ready (111.00)

The XFRRDY state is initiated by the controller to transfer each word of an Information Transfer.

When beginning transfers In, the assertion of MASTER OUT indicates to the drive that the controller has released BUS A. When beginning transfers Out, the assertion of MASTER OUT directs the selected drive to release BUS B.

8.2.13 Transfer Start (111.10)

The XFRST state is initiated by the drive to acknowledge the start of an Information Transfer. For transfers Out it indicates that the drive is ready to accept information and for transfers In it is used to validate the stability of the information on the buses.

8.2.14 Transfer Response (111.11)

The XFRRES state is initiated by the controller to acknowledge the acceptance of information on the buses for transfers In, or to validate the stability of the information on the buses for transfers Out.

8.2.15 Transfer End (111.01)

The XFREND state is initiated by the drive to acknowledge the acceptance of information on transfers Out, and to complete the transferring of each word of an Information Transfer.

8.2.16 Slave End (101.00)

The SLAVEND state is initiated by the drive to terminate an Information Transfer. For transfers Out the controller releases control of BUS B. For transfers In this state acknowledges the release of BUS A by the drive.

8.2.17 Undefined State Recovery

An undefined state or state transition encountered by the controller shall cause the controller to begin deselection by releasing the bus(es) and negating all OUT signals. SELECT OUT shall be the last signal line negated. When the drive is deselected it releases the bus(es) it may be driving, then negates SYNC IN and SLAVE IN. The interface is thus returned to the IDLE state, and the controller can resume operations.

An undefined state or state transition encountered by a drive causes the drive to release the bus(es) it may be driving, then negate SYNC IN and SLAVE IN. When the controller recognizes the negation of SLAVE IN outside of a valid sequence it releases the bus(es) and negates all OUT signals. SELECT OUT shall be the last signal line negated. The interface is thus returned to the IDLE state, and the controller can resume operations.

NOTE: The negation of SLAVE IN and SYNC IN is valid during defined sequences such as SLAVEND from XFRRDY. SLAVE IN and SYNC IN are not active during REQUEST, SELECT and SLAVEND.

8.3 Sequences

This section defines all valid sequences in the state diagram (see Figure 5). The following sequences are defined by the IPI-2 interface:

- Request Interrupts Sequence
- Request Drive Interrupts Sequence
- Request Transfer Settings Sequence
- Selection Sequence
- Deselection Sequence
- Master Reset Sequence
- Selective Reset Sequence
- Bus Control Sequence
- Ending Status Sequence
- Interlocked Input Sequence
- Interlocked Output Sequence
- Non-Interlocked Input Sequence
- Non-Interlocked Output Sequence

8.3.1 Request Interrupts Sequence (001.00) (See Figure 6)

The Request Interrupts Sequence allows the controller to interrogate all drives to determine the service (or class of service) desired.

This sequence begins in the IDLE state, and proceeds to the REQUEST state after the controller issues the Request Interrupts Byte on BUS A and asserts MASTER OUT. Drives meeting any of the Request conditions respond by placing their bit significant Radial Address bit on BUS B. The drive response is dynamic as long as the controller remains in the REQUEST state. The sequence ends when the controller negates MASTER OUT to return to the IDLE state.

The response of the drives is not synchronous, and the controller must wait a time equal to that of the furthest drive to respond before latching or sampling the BUS B response. In addition, the controller must wait for a time equal to that of the furthest drive to detect the IDLE state, and release its bit significant address on BUS B before starting another sequence.

- If more than 1 Request bit is set, the drives respond to the logical "OR" of the conditions.

- If the drive detects a parity error on BUS A during the REQUEST state, it does not respond to the Request Byte. If the controller fails to receive a response from the drive within 5 us., it should retry the Request sequence.

- The BUS B response is a bit significant response, the other 8 BUS B transmitters are released. Parity should not be checked by the controller.

See Figure 7 for timing details.

8.3.1.1 Request Interrupts Byte - BUS A

Bit	Description
7	Request Interrupts - This bit is reset for the Request Interrupts sequence.
6	Report Busy Status - When this bit is set, all Busy drives place their Radial Address bit on BUS B.
5	Report Ready Status - When this bit is set, all Ready drives place their Radial Address bit on BUS B.
4	Controller Power Fail Alert - When this bit is set, the controller is informing the drives that a power fail condition has been detected. The drives respond by placing their Radial Address bit on BUS B after they have taken action to permit termination of activity.
3	Power On Status Request - When this bit is set, all drives with Power On (but not necessarily Ready) place their Radial Address bit on BUS B.
2	Status Pending Interrupt (Class 3 Interrupt) - When this bit is set, all drives with a Status Interrupt pending place their Radial Address bit on BUS B. The Status Interrupt informs the controller to read status.
1	RPS Interrupt (Class 2 Interrupt) - When this bit is set, all drives with an RPS Interrupt pending place their Radial Address bit on BUS B. This bit informs the controller that Rotational Position Sensing is active.
0	Command Completion Interrupt (Class 1 Interrupt) - When this bit is set, all drives with a Command Completion Interrupt pending place their Radial Address bit on BUS B.

8.3.1.2 Radial Address Byte - BUS B

Bit	Description
7-0 no parity	Radial Address Bits - The drives respond to the request by driving their bit significant address on BUS B and releasing all other BUS B bits.

8.3.1.3 Interrupt Classes

The ATTENTION IN signal is activated by the drive when the Status Pending Interrupt, RPS Interrupt, or Command Completion Interrupt is active and the interrupt is enabled to generate the Attention. The ATTENTION IN signal is also activated if a Not Busy transition occurs on a port where a Selection attempt previously received a Busy indication. The 3 interrupt classes are defined as follows:

Class 3 - Status Pending Interrupt - This interrupt is active when there is a status exception in the Status Response which must be reported to the controller. It is deactivated when the status bits are cleared by a Read Status control with a Successful Transfer bit set in the Controller Status or by an appropriate reset.

Class 2 - RPS Interrupt - This interrupt is active during the one sector time each disk revolution that the heads are over the target sector, after completion of a Load Position or Load RPS Target Sector Address command, when RPS is enabled. Activation of the RPS Interrupt occurs at the leading edge of the sector. RPS is disabled by setting X'FFFF' as the target sector. The interrupt is deactivated by any accepted Data Control, disabling the RPS or an appropriate reset.

Class 1 - Command Completion Interrupt - This interrupt is active when the command completes successfully and the Time Dependent bit of the Drive Status following the transfer of the command was set. It is deactivated by any accepted Bus Control or an appropriate reset.

The interrupt is not generated for a Load Position Command if the RPS is enabled.

8.3.2 Request Drive Interrupts Sequence (See Figure 8)

The Request Drive Interrupts Sequence allows the controller to interrogate a specific drive to determine the service (or class of service) desired.

The sequence begins in the IDLE state, and proceeds to the REQUEST state after the controller outputs the Request Drive Interrupts Byte on BUS A and asserts MASTER OUT. The addressed drive advances to the REQUACK state by placing the Drive Interrupts Byte on BUS B and asserting SLAVE IN. The contents of BUS B can change dynamically as long as the controller remains in the REQUACK state. The controller initiates termination of the sequence by negating MASTER OUT and advancing to the DESEL state. The drive ends the sequence by negating SLAVE IN and returning to the IDLE state.

See Figure 9 for timing details.

8.3.2.1 Request Drive Interrupts Byte - BUS A

Bit	Description
7	Request Drive Interrupts - This bit must be set for the Request Drive Interrupts sequence.
6-4	Drive Address - Bit 4 is the least significant bit of the drive address.
3	Request Drive Interrupts - This bit must be set for the Request Drive Interrupts sequence.
2-0	Request Drive Interrupts - These bits must be reset for the Request Drive Interrupts sequence.

8.3.2.2 Drive Interrupts Byte - BUS B

Bit	Description
7	Reserved
6	Busy Status - This bit is set if the drive is Busy, indicating that the drive is unable to respond to the controllers request because it is currently executing a Bus Control (previously received from this port or the alternate port), or is reserved/selected to the other port.
5	Ready Status - This bit is set if the drive is Ready, indicating that the drive is able to accept some or all Data Bus Controls.
4	Reserved
3	Priority Select Status - This bit is set if the drive is Priority Selected at the alternate port.
2	Status Pending Interrupt Active (Class 3 Interrupt) - This bit is set if the drive has an active Exception Status to be reported in the Status Response.
1	RPS Interrupt Active (Class 2 Interrupt) - This bit is set for one full sector time each disk revolution that the data heads are over the target sector.
0	Command Completion Interrupt Active (Class 1 Interrupt) - This bit is set when a command, previously transferred with the Time Dependent Operation bit set in the Drive Status Byte, completes successfully. The interrupt is not generated for a Load Position command if RPS is enabled, and is cleared by the acceptance of any Bus Control.

8.3.3 Request Transfer Settings Sequence (See Figure 10)

The Request Transfer Settings Sequence allows the controller to interrogate the specified drive as to its Information transfer characteristics. The transfer characteristics apply to Command/Response transfers only.

The sequence begins in the IDLE state, and proceeds to the REQUEST state after the controller outputs the Request Transfer Settings Byte on BUS A and asserts MASTER OUT. The addressed drive advances to the REQUACK state by placing the Transfer Settings Byte on BUS B and asserting SLAVE IN. The controller initiates termination of the sequence by negating MASTER OUT and advancing to the DESEL state. The drive ends the sequence by negating SLAVE IN and returning to the IDLE state.

See Figure 11 for timing details.

8.3.3.1 Request Transfer Settings Byte - BUS A

Bit	Description
7	This bit must be set for the Request Transfer Settings Sequence.
6-4	Drive Address - Bit 4 is the least significant bit of the drive address.
3-0	These bits must be reset for the Request Transfer Settings Sequence.

8.3.3.2 Transfer Settings Byte - BUS B

Bit	Description
7	Reset, by definition
6	Maintenance Mode Capability - This bit is reset, indicating Maintenance Mode 1 capability only.
5	Octet Mode Setting - This bit is set, indicating all Command/Response information transfers will be in the double octet (16-bit) mode.
4	Transfer Mode Setting - This bit is reset, indicating current setting is for interlocked transfers.
3	Transfer Mode Capability - This bit is reset, indicating the drive is not capable of transferring Command/Response Information in the non-interlocked mode.
2	Transfer Mode Capability - This bit is set, indicating the drive is capable of transferring Command/Response information in the interlocked mode.
1	Octet Capability - This bit is set, indicating the drive is capable of supporting double octet information transfers.
0	Octet Capability - This bit is reset, indicating the drive is not capable of supporting single octet information transfers.

8.3.4 Selection Sequence (See Figure 12)

The Selection Sequence occurs when the controller addresses a drive.

The sequence begins in the IDLE state, and proceeds to the SELECT state after the controller outputs the Selection Octet on BUS A and asserts SELECT OUT. The sequence ends when the addressed drive advances to the SLAVACK state by asserting SLAVE IN and, if not Busy, placing its bit significant Radial Address bit on BUS B. If the addressed drive does not respond, the controller must end the sequence by negating SELECT OUT and returning to the IDLE state.

The controller can detect most invalid selection conditions by analysis of the Radial Select Address, e.g., incorrect selection will have the wrong Radial Select bit posted, and multiple selection may have more than 1 bit posted. To detect multiple selection, the controller must wait at least 1 µs for all drives to respond.

- If there is a parity error on BUS A, none of the drives are selected, and SLAVE IN is not asserted.
- If the controller fails to receive a response from the addressed drive within 5 µs, it should retry the Selection sequence.
- If the drive is Busy, SLAVE IN is asserted with no bit significant Radial Address response.

See Figure 13 for timing details.

8.3.4.1 Selection Byte - BUS A

Bit	Description
7	This bit must be reset for the Selection sequence.
6-4	Drive Address - Bit 4 is the least significant bit of the drive address.
3-1	Reserved
0	Priority Select - When this bit is set, the addressed drive will cease any operations with the alternate port, release SLAVE IN and SYNC IN, and cancel any reserves at the alternate port.

8.3.4.2 Radial Address Byte - Bus B

Bit	Description
7-0, P	Radial Address Byte - The drive responds to Selection by driving its bit significant address and releasing all other bus bits to provide select status. The parity line is released by the drive and parity should not be checked by the controller.

8.3.5 Deselection Sequence (See Figure 14)

The Deselection Sequence begins in the SLAVACK state, and proceeds to the DESEL state after the controller negates SELECT OUT. The sequence ends when the selected drive negates SLAVE IN and returns to the IDLE state.

See Figure 15 for timing details.

8.3.6 Master Reset Sequence (Maintenance Mode) (See Figure 16)

The Master Reset Sequence allows the controller to initiate Maintenance Mode for all drives on a daisy chain. The Maintenance Mode provides access to the drive when normal interface communications may not be operational. Using the Maintenance Mode, the controller can force all drives on a daisy-chain to release their drivers so that interface failures can be isolated. The controller may then issue a Selective Reset sequence to 1 drive at a time to isolate the faulty unit.

When communication with the maintenance logic is required, the signals are disconnected from the functional circuits and diverted to the maintenance circuits. Maintenance Mode provides logic which is independent (as far as is practical) of the logic associated with normal functions.

The sequence starts from any state and begins when the controller negates SELECT OUT, if active. The addressed drive, if driving BUS A, is expected to release it. The controller then negates MASTER OUT and SYNC OUT and places a Master Reset byte on BUS A. The controller then asserts SYNC OUT for a minimum of 6 µs, and enters the MAINT state. If at least 2 of the 3 BUS A Data Out lines are still active a minimum of 6.0 µs after the trailing edge of SYNC OUT, the drive is reset and the drivers remain released until a Selection Sequence is issued. The drive will not enter the Maintenance Mode until the MAINT state has been active for at least 6.0 µs. The sequence ends when the controller negates the SYNC OUT signal and returns to the IDLE state.

See Figure 17 for timing details.

8.3.6.1 Master Reset Byte - BUS A

Bit	Description
7	Data Out 2 - 2 of the 3 Data Out lines must be active a minimum of 3.5 µs after the trailing edge of SYNC OUT to initiate the Master Reset.
6-5	Reserved
4	Data Out 1 - 2 of the 3 Data Out lines must be active a minimum of 3.5 µs after the trailing edge of SYNC OUT to initiate the Master Reset.
3-2	Reserved
1	Data Out 0 - 2 of the 3 Data Out lines must be active a minimum of 3.5 µs after the trailing edge of SYNC OUT to initiate the Master Reset.
0	Reserved

8.3.6.2 Bus B

Bit	Description
7-0	There is no BUS B response to a Master Reset

8.3.7 Selective Reset Sequence (See Figure 18)

The Selective Reset Sequence allows the controller to reset a single drive and to terminate the Maintenance Mode. The reception of the Selective Reset Control Octet causes the drives port drivers to be enabled.

The sequence begins in the IDLE state, and proceeds to the REQUEST state after the controller places a Selective Reset Control Octet on BUS A and asserts MASTER OUT. Up to this point, an operational drive will interpret the octet on BUS A as either a Request Drive Interrupts or a Request Transfer Settings octet. After 2 µs regardless of whether the addressed drive responds with SLAVE IN, the controller advances to the RESETSEL 1 state by asserting SYNC OUT. The drive does not initiate its reset action nor release its interface lines until RESETSEL 1 has been active for at least 6.0 µs. At this point, the addressed drive, operational or not, recognizes the octet on BUS A as a Selective Reset and performs the required action. The drive will reset the "Power On" bit in the Request Interrupts Octet to acknowledge acceptance of the Selective Reset Control Octet. The controller then advances to the REQUEST state by negating SYNC OUT. The controller initiates termination of the sequence by negating MASTER OUT and advancing to the IDLE state. The reset operation is complete when the drive sets the "Power On" bit in the Request Interrupts Octet.

The reset leaves the spindle power of the drive in whichever state it was at, ON or OFF.

See Figure 19 for timing details.

8.3.7.1 Selective Reset Control Byte - BUS A

Bit	Description
7	This bit must be set for a Selective Reset Sequence.
6-4	Drive Address - Bit 4 is the least significant bit of the drive address.
3	Disable Interface Drivers - When this bit is set, the drive will disable its drivers from the interface.
2	Reset Drive - When this bit is set, the drive is reset as at power on.
1	Reset Logical Interface - When this bit is set, the logical interface for the port is reset. The Format Specification is not affected.
0	Reset Physical Interface - When this bit is set, the physical interface for the port is reset.

8.3.7.2 BUS B BITS

Bit	Description
7-0	There is no BUS B response to a Selective Reset sequence.

8.3.8 Bus Control Sequence (See Figure 20)

The Bus Control Sequence allows the controller to establish the bus configuration and to transfer the Command/Response Control or Data Control to be executed.

The sequence begins in the SLAVACK state and proceeds to the BUSCTL state after the controller places a Bus Control Byte on BUS A and asserts SYNC OUT. The drive advances to the BUSACK state by placing the Bus Acknowledge Byte (all zeros) on BUS B, and asserting SYNC IN. The controller initiates termination of the sequence by negating SYNC OUT and advancing to the MASTEND state. The drive ends the sequence by negating SYNC IN and returning to the SLAVACK state. Note that although the interface returns to SLAVACK when the drive responds by negating SYNC IN that there is no Slave Status Byte on BUS B because it is simply an intermediate state on the way to beginning an Information Transfer.

Entering SLAVEND without an information transfer indicates to the controller that the drive did not accept the Bus Control Byte or that the Bus Control did not require an Information Transfer (e.g. Step Head). If the Bus Control was rejected, the cause of the drive rejection is reported to the controller in the Drive Status Byte during the Ending Status SLAVACK state. If the drive detects a parity error on BUS A during BUSCTL, it will not interpret the Bus Control Byte and the parity error will be reported in the Drive Status Byte.

See Figure 21 for timing details.

8.3.8.1 Bus Control Byte - BUS A

Bit Description

7 (Command or Response)/ Data - When this bit is reset, the operation will be a Command or Response transfer. When this bit is set, the operation will be a data transfer.

6 Information Out/ Information In - When this bit is reset, the subsequent information transfer will be directed to the drive. When this bit is set, the information transfer will be directed to the controller.

5 Fixed Block Data Control - This bit must be reset.

4 Head Advance - This bit is valid only if bit 7 is set, indicating a data transfer. If this bit is reset, the drives head address will not be advanced at the end of the subsequent data transfer. If this bit is set, the drives head address will be incremented at the end of a successful data transfer (see 9.6).

3-0 Bus Control Code - The Command Controls encode bits 3-0 to specify the command type. The Response Controls encode bits 3-0 to specify the response type. The Data Controls encode bits 3-0 to specify the number of fields and the orientation of the data on the disk.

8.3.8.2 Bus Acknowledge Byte - BUS B

Bit Description

7-0 The BUS B bits are not defined and zeroes are returned with valid parity during the BUSACK state.

8.3.9 Ending Status Sequence (See Figure 22)

The Ending Status Sequence allows the controller and the drive to present the status of the previous Information Transfer.

The sequence is entered from an Information Transfer whenever the drive or controller terminates a transfer. In either case, the drive begins the sequence be negating SLAVE IN and releasing BUS B (transfer In) to enter the SLAVEND state. The controller responds by setting the Controller Status Byte on BUS A, releasing BUS B (transfer Out), negating MASTER OUT, and entering the SELECT state. The drive terminates the sequence by setting the Drive Status Byte on BUS B, asserting SLAVE IN, and entering the SLAVACK state.

If the drive detects a parity error on BUS A during SELECT, it will not respond to the contents of the Controller Status Byte. It shall assume the Information Transfer, if any, was unsuccessful and set the Bus Parity Error bit in the Drive Status Byte.

If a valid Command Control is sent but the wrong number of parameters are transferred, the Successful Information bit will be reset in the Drive Status Byte.

If the Controller Status Byte indicates an unsuccessful information transfer following a Read Status Response, the drive will not clear the status conditions reported.

See Figures 23A thru 23E for timing details.

8.3.9.1 Controller Status Byte - BUS A

Bit	Description
7	Successful Information Transfer - When this bit is set, the information transfer completed successfully.
6	Bus Parity Error - When this bit is set, the controller detected a bus parity error.
5-0	Reserved

8.3.9.2 Drive Status Octet - BUS B

Bit Description

7 Successful Information Transfer - This bit is set if the drive determines that the transfer completed with no Parity Errors on the Bus Control Octet, the Information Transfer, or the Controller Status Octet.

6 Bus Parity Error - This bit is set if the drive detected a parity error on the preceding Bus Control, Information Transfer or Controller Status operation. If this bit is set, the Successful Information Transfer bit (bit 7) will be reset.

5 Odd Octet Transfer - This bit is set if the data transfer was of an odd octet length. The octet on BUS B of the last word transferred should be ignored when this bit is set.

4 Time Dependent Operation - This bit is set if the command has not been completed by the drive at the time this status is sent to the controller. A Command Completion Interrupt and an Attention, if enabled, will be generated when the command is complete. If this bit is reset, the command is now complete and there will be no Command Completion Interrupt.

3-0 Operation Ending Status - This four bit field is defined below :

BITS: 32 10

00 xx = Normal End
- 00 = Drive Available, Bus Control executed
- 01 = Drive Busy, Bus Control rejected

01 xx = Data Exception
- 00 = missed Address Mark
- 01 = missed Sync Octet
- 10 = ECC Error (optional)
- 11 = Verify Header Miscompare

10 00 = Operation Exception

11 00 = Unsolicited Exception

The three types of exceptions are defined as follows:

1. Data Exception - Indicates that the previous data bus control incurred an error.

2. Operation Exception - Indicates that the previous bus control incurred an operation error. This error may be determined by issuing a Read Status Command. If the captured status is ignored it will be cleared upon receipt of the next bus control.

3. Unsolicited Exception - Indicates that the previous bus control was rejected due to an outstanding unsolicited exception. The controller is required to read this status by issuing a read status command before any other bus control can be accepted. This status cannot be ignored.

8.3.10 Information Transfers

All information is transferred in the double octet (16-bit) mode. Command and Response information is always transferred in the interlocked mode. Data is always transferred in the non-interlocked mode. The transfer modes cannot be changed.

The Information Transfer may be terminated by either the drive or controller. Termination is normally performed by the drive since it is in control of the transfer. The controller may initiate termination prior to the expected end, e.g., a header miscompare. The drive may terminate the transfer prior to the expected end of transfer, e.g., a header non-verify on a write operation.

8.3.10.1 Interlocked Input Sequence (Response Transfer) See Figure 24

This sequence starts from the SLAVACK state, and must be immediately preceded by a Bus Control Sequence for the initial state transition to be considered valid. The sequence starts when the controller asserts MASTER OUT, advancing to the XFRRDY state. The selected drive has previously received a Response Control (bit 7 of the Bus Control Byte was reset and bit 6 was set). The drive has 2 choices at this point; output a Response parameter or if the Response received is not supported, or contained a parity error, output a Drive Status Byte.

To output a Response parameter, the drive places the high order octet of the parameter on BUS A and the low order octet on BUS B. The drive then advances to the XFRST state by asserting SYNC IN. The controller accepts the Response parameter and either terminates or continues the information transfer. To continue the transfer, the controller asserts SYNC OUT, advancing to the XFRRES state. The drive responds by negating SYNC IN to enter the XFREND state. The controller negates SYNC OUT to arrive at the XFRRDY state.

The drive has the same 2 choices it had at the beginning of the transfer loop; output a Response parameter or output a Drive Status Byte.

If the previous exchange resulted in the last parameter required by the Response Control, the drive would terminate the information transfer at this point by negating SLAVE IN to advance from XFRRDY to the SLAVEND state. The controller responds by placing a Controller Status Byte on BUS A, negating MASTER OUT, and entering the SELECT state. The drive ends the sequence by outputting the Drive Status Byte on BUS B, asserting SLAVE IN, and entering the SLAVACK state.

The controller can terminate the information transfer while in the transfer loop, in which case the Ending Status Sequence will be somewhat different. This option exists when in the XFRST state of the Interlocked Input Sequence. After accepting the Response parameter, the controller negates MASTER OUT to enter MASTEND, beginning a Controller Termination Sequence. The drive negates SYNC IN and enters the SLAVACK state. The controller then asserts MASTER OUT and enters the XFRRDY state and the drive responds by negating SLAVE IN and entering the SLAVEND state. The controller then places a Controller Status Byte on BUS A, negates MASTER OUT, and enters the SELECT state. The drive completes the sequence by outputting the Drive Status Byte on BUS B, asserting SLAVE IN, and entering the SLAVACK state.

See Figure 25 for timing details.

8.3.10.2 Interlocked Output Sequence (Command Transfer) See Figure 26

The Interlocked Output Sequence is similar to the Input Sequence. The sequence starts from the SLAVACK state and must be preceded by a Bus Control for the initial state transition to be considered valid. The sequence starts when the controller asserts MASTER OUT, advancing to the XFRRDY state. The selected drive has previously received a Command Control (bit 7 and 6 of the Bus Control Byte were reset). The drive has 2 choices at this point; read a Command parameter or if the Command received is not supported, output a Drive Status Byte.

If the drive detected a Parity Error on the Bus Control Byte or an invalid Bus Control, the Drive Status Byte would be output at this time.

To input a Command parameter, the drive asserts SYNC IN and advances to the XFRST state. The controller can either terminate or continue the information transfer at this point. To continue the transfer, it places the Command parameter on BUS A and BUS B, asserts SYNC OUT, and advances to the XFRRES state. The drive reads the BUS A and BUS B contents, negates SYNC IN, and enters the XFREND state. The controller negates SYNC OUT, arriving at XFRRDY.

The drive has the same 2 choices it had at the beginning of the transfer loop; input a Command parameter or output a Drive Status Byte.

If the last parameter transferred is the last parameter required by the Command Control, the drive would terminate the transfer. The sequence at this point is identical with the corresponding part of the Interlocked Input Sequence and is described in detail in that section. If the controller sends the wrong number of parameters for the command, the drive would output a Drive Status Byte with the Successful Information Transfer bit reset at this time.

See Figure 27 for timing details.

8.3.10.3 Non-Interlocked Information Transfers (Data Streaming)

Non-interlocked transfers enable high transfer rates (10 MB/s or less) over long cable lengths and is suited to synchronous disk data transfers. Non-interlocked transfers are accomplished by not interlocking the SYNC IN and SYNC OUT signals, which masks out round trip transmission delays.

The transfer begins with the drive asserting SYNC IN and then negating it to generate a pulse. The period between successive pulses is defined by the transfer rate. Upon recognizing the SYNC IN pulse, the controller generates a SYNC OUT pulse in response. The transmitter of the SYNC IN/SYNC OUT pulse must insure the proper set-up and hold times with respect to the active edge of its sync pulse. If the hold time is greater than the one-way cable delay plus set-up times, the effect is to cause the transfer to appear interlocked.

The non-interlocked timing requirements are:

- The SYNC IN pulses occur at the disk data rate and are generated at the rate of 1 per double octet.
- The nominal duty cycle for SYNC IN is 50%.
- Upon recognizing a SYNC IN, the controller echoes a SYNC OUT after a fixed delay. The delay at the controller shall not exceed 1 double octet time at the maximum cable length.

Drives that support ECC/CRC and have that feature enabled, will complete the sector and write uncorrectable ECC/CRC if a data underrun condition occurs during a disk write.

8.3.10.3.1 Non-Interlocked Input Sequence (Data Transfer In) See Figure 24

This sequence starts from the SLAVACK state and must have been immediately preceded by a Bus Control Sequence to be considered valid. The sequence starts when the controller asserts MASTER OUT, advancing to the XFRRDY state, and the selected drive has received a read type Data Control (bit 7 of the Bus Control Byte was set, and bit 6 was set).

When disk read data becomes available, the drive outputs the data to BUS A and BUS B and issues a SYNC IN pulse. Upon recognizing a SYNC IN pulse, the controller latches BUS A and BUS B and echoes a SYNC OUT pulse after a fixed delay. This exchange continues until the disk read operation is completed. For drive terminated transfers, after the last SYNC OUT pulse is transmitted, SLAVE IN is negated to enter the SLAVEND state. The controller places a Controller Status Byte on BUS A and negates MASTER OUT, entering the SELECT state. The drive then places the Drive Status Byte on BUS B, asserts SLAVE IN, and enters the SLAVACK state, ending the sequence.

The controller can terminate the transfer, in which case the sequence will be somewhat different. To terminate a non-interlocked transfer, the controller substitutes a SYNC OUT pulse with a pulse on the MASTER OUT signal having the same period and pulse width requirements of the SYNC OUT pulse.

See Figure 28 for timing details.

8.3.10.3.2 Non-Interlocked Output Sequence (Data Transfer Out) See Figure 26

This sequence starts from the SLAVACK state and must have been immediately preceded by a Bus Control Sequence for the initial state transition to be considered valid. The sequence starts when the controller asserts MASTER OUT, advancing to the XFRRDY state, and the drive has received a write type Data Control (Bus Control Byte bit 6 is reset and bit 7 is set). If data is not available when it must be written on the disk, a data underrun exists and the transfer is terminated by the drive.

Upon recognizing the Bus Control as a write disk operation, the drive begins generating SYNC IN pulses at the disk rate, 7 octet times before the target data segment to account for transmission and controller delays. Upon recognizing the SYNC IN pulse, the controller places the data to be written on BUS A and BUS B and echoes a SYNC OUT pulse after a fixed delay. This exchange continues until the drive is 7 octet times from the end of the write operation, when the SYNC IN pulse train is terminated on the falling edge of the next SYNC IN.

The drive begins termination of the sequence by negating SLAVE IN and enters the SLAVEND state. The controller places a Controller Status Byte on BUS A and negates MASTER OUT, entering the SELECT state. The drive ends the sequence by placing the Drive Status Byte on BUS B, and asserts SLAVE IN, entering the SLAVACK state.

The controller can terminate the transfer, in which case the sequence will be somewhat different. To terminate a non-interlocked transfer, the controller substitutes a SYNC OUT pulse with a pulse on the MASTER OUT signal having the same period and pulse width requirements of the SYNC OUT pulse.

See Figure 29 for timing details.

9.0 DRIVE FUNCTIONS

9.1 Disk Format

9.1.1 Fixed Block Format

The IPI-2 can operate in 1 of 2 sector modes described below:

- Sector Mode 1 - Every sector is of the same length, which is fixed by the drive.
- Sector Mode 2 - Every sector is of the same length, but the length is programmable.

9.1.2 Sector Control

The 2 methods of defining the start of a sector are described below:

9.1.2.1 Hard Sector (See Figure 30)

A hard sectored drive derives the start of each sector by counting the number of octets from the Index mark at the beginning of a track. The number of sectors is specified by the Format Specification (see 9.2). Each sector consists of 1 or more fields. Each field consists of a Read Gate Delay segment, a PLO Sync Field segment, a Sync Byte segment, the Field segment, a Pad segment, and a Gap segment.

The Read Gate Delay segment is used to separate the "Write Gate On" point at the beginning of the field, from the "Read Gate On" point. This is necessary to prevent the Write Splice at the beginning of the field from drifting forward of the "Read Gate On" point due to Head Scatter. This segment is the same length for all fields. The value inserted by the drive for this segment is:

Read Gate Delay (in octets) = (2 x Head Scatter) + Write Splice Length

The next segment is the PLO Sync Field segment. This segment is the same length for all fields. The purpose of the PLO Sync segment is to give the drive Read PLO a pattern to acquire bit synchronization. The value inserted by the drive is:

PLO Sync Length (in octets) = (2 x Head Scatter) + Minimum PLO sync time

The third segment is the Sync Byte segment. This segment is 1 octet in length and is the same for all fields. The purpose of the Sync Byte is to provide a data octet of known value to acquire octet synchronization.

The fourth segment is the Field segment which contains user data. This value is specified by the controller in the Format Specification.

The fifth segment is the Pad segment. This segment is 2 octets in length and is the same for all fields. This segment separates the last octet of user data from the "Write Gate Off" point.

The last segment in a Field is the Gap segment. This segment separates a field from the next field in a Sector. See Appendix A for a description of the Gap segment.

9.1.2.2 Soft Sector (See Figure 31)

A soft sectored drive makes use of Address Marks to mark the start of each sector. The number of sectors is specified by the Format Specification. Each track of the drive must be formatted with Address Marks by the Perform Sector Marking function. Soft sectoring is required for drives with removable media to account for Head Scatter. The segments in the Soft Sector format are the same as the Hard Sector format with the exception of the Guard Band segment and the Address Mark segment.

9.1.3 Format Control

The drive is responsible for format control. The drive performs the following functions under the direction of the Format Specification:

- Determine the start of each sector on the track.
- Determine the start of each field within the sector.
- Count the number of octets in each field of the sector.
- Activate Read Gate and Write Gate in accordance with the current Data Control and the Format Specification.
- PLO, bit and octet synchronization on read operations.
- Writing of PLO, bit and octet sync patterns.

9.2 Format Specification

The Format Specification is an ordered list of parameters which define how the tracks and sectors of the disk are to be organized. It is transferred to the drive by the Load Format Specification Control and the controller may retrieve it with a Read Format Specification Control. Both the controller and the drive may establish the parameters during the initialization of the Format Specification.

9.2.1 Fixed Block Format Specification

The Fixed Block Format Specification allows for sectors of up to 3 fields, but all sectors specified by this specification must have the same organization. The Fixed Block Format Specification has the following format:

OCTET	BIT	DESCRIPTION
0-1		Number of octets following: equals n-1
2		Format Type Code 1 = Fixed Block
3		Flag Byte
	7	Initialized (Format Specification Initialization complete)
	6	Manufacturers Default Format Specification
	5	Sector mode 2
	4	Sector mode 1
	3	Use soft sectoring
	2	Use hard sectoring
	1	Use field Data Controls
	0	Use sector Data Controls
4-5		Number of sectors per track
6-9		Number of physical octets per sector
A-B		Number of beginning header octets to be skipped
C-D		Number of fields per sector
E-11		Number of octets per field 0
12-13		Controller turnaround delay 0
14-17		Number of octets per field 1
18-19		Controller turnaround delay 1
1A-1D		Number of octets per field 2
1E-1F		Controller turnaround delay 2

9.2.1.1 Number of Octets

The length of the Format Specification is contained in these 2 octets. This field is not included in the octet count. The length of the Fixed Block Format Specification is always 30 octets.

9.2.1.2 Format Type Code

This single octet parameter contains the Format Type Code. If this parameter equals X'01', then the Format Specification is a Fixed Block type and is organized as such.

9.2.1.3 Flag Byte

This single octet parameter contains the Fixed Block Format Specification flag information and indicates whether the Format Specification is initialized, the format is a Manufacturers Default, which sector mode is to be used, and what data controls the controller intends to use with this Format Specification.

9.2.1.4 Number of Sectors Per Track

The IPI-2 defines a minimum of 1 sector per track and a maximum of 256 sectors per track. The number of sectors per track is arrived at by one of the following schemes:

1. Fixed Sector Drive - If the drive has a fixed sector size, the drive enters the number of sectors per track in the Format Specification every time it is read by the controller.

2. Controller Defined - If the controller is to define the number of sectors per track, it sets the number of sectors per track, the number of fields per sector and the controller turnaround delay in the Format Specification every time it is transmitted to the drive. The controller specifies (as X'FFFF') the field sizes. The drive computes the value of the unspecified quantity.

3. Calculated by the Drive - If the drive is to calculate the number of sectors that can be fitted on the track, the controller supplies it with the number of fields, the field sizes and the Controller Turnaround Delays. The controller specifies the number of sectors as X'FFFF'. The drive then enters the number of sectors in the Format Specification.

In addition to the octets of the sector required by the controller, the drive takes into consideration the number of drive controlled overhead octets.

9.2.1.5 Number of Physical Octets Per Sector

The number of physical octets per sector is supplied by the drive. Typically, this is used by the controller to determine the sector number of a defect specified by the Defect Map.

9.2.1.6 Number of Octets to be Skipped during Header Verify

This parameter is supplied by the controller to specify the number of octets, starting from the beginning of the header, to be skipped in the drive's verify of the header during execution of a Verify Header Data Control.

9.2.1.7 Number of Fields Per Sector

The number of fields per sector is usually supplied by the controller, but may be supplied by the drive. The first field is usually the header used to identify the sector. For the IPI-2, there can be a maximum of 3 fields per sector.

9.2.1.8 Number of Octets per Field

The number of octets in each field is normally specified by the controller based on system considerations. Controller managed ECC and CRC are considered as part of the user field length. A field size must be specified for each of the fields. The IPI-2 defines the maximum field size as 65,536 octets.

As viewed by the drive, a field also includes the Read Gate Delay segment, the PLO Sync Field segment, the Sync Byte segment, the Pad segment and the Gap segment.

9.2.1.9 Controller Turnaround Delay

The Controller Turnaround Delay is the time, measured in octets, required by the controller between fields to handle the Ending Status sequence from one Data Control and to initiate another. It is measured at the drive, and therefore includes transmission delays, from the time when the drive terminates a transfer (drops SLAVE IN) until the next Data Control is received at the drive.

The actual gap required between fields is the Controller Turnaround Delay increased to account for read propagation delays, transfer termination time, Drive Status turnaround time, and Data Control decoding.

The controller must provide the Controller Turnaround Delay for each of the fields. If no Data Control is to be sent to the drive after a field, the parameter for that field may be zero.

See Appendix A for Controller Turnaround Delay considerations.

9.2.2 Format Initialization

A Format Specification with its Initialized bit reset is not complete and cannot be used by the drive for format control or data transfer.

The last loaded Format Specification is saved by the drive in nonvolatile memory so it can be retrieved after power down and reset. The controller may save the current Format Specification(s) and load it into the drive. (See 14.0 for description of Format Specification storage).

A Format Specification is initialized by the following procedure:

1. The controller loads a Format Specification with its Initialized bit reset to invalidate the old specification, if any, and condition the drive to start the initialization process. The controller provides any of the parameters that it is to contribute to the Format Specification. Parameters not specified by the controller must be X'FFFF'.

   Alternatively, the controller loads a completely specified Format Specification with the Initialized bit set.

   If the drive determines that there are missing or incorrect parameters, it sets the appropriate Bus Control Exception status bit in the Status Response.

2. The controller reads an initialized Format Specification from the drive to obtain the drive's fixed and/or calculated parameters. The controller shall check the Format Specification against its requirements and adjust its own control to the specification.

9.2.3 Manufacturers Format Specification

The drive has a built-in Manufacturers Format Specification which is used primarily to write and read the Defect map. It is invoked by the Load Format Specification control with Bit 6 of the Flag Byte set and remains in effect until another Load Format Specification control is received by the drive. It may be read by a Read Format Specification control when it is invoked. The location of the Defect Map is found by issuing the Read Configuration Bus Control.

The format provides for a header and 1 data field. The header contents, CRC, and the ECC are not specified. The format is organized to allow for either sector or field type of controls.

The controller shall be capable of recovering the data from data fields formatted with this specification, without the use of the headers. Sectors shall be read in their physical order from Index.

9.3 Drive Conditions

The manner in which a drive responds to a command is determined by its condition. The conditions are:

Available - The port is capable of responding and executing commands.

Not Available - The port is not able to execute any command, e.g., when power is off, the drive is not installed, or the port is disabled. A non-available condition is detected by the controller, e.g., lack of Slave In response to a selection attempt.

Operational - The drive is capable of accepting a command from the controller, e.g., the port is available and the drive is able to handle Selection, Deselection, Bus Control and Ending Status sequences. If the drive is Not Ready, any Data Controls or Bus Controls that require access to the HDA will be rejected with a Drive Ending Status of Operation Exception, Bus Control Out of Context.

Ready - The port is Available, the drive is Operational and the HDA is capable of being accessed. The drive is able to handle Selection, Deselection, Bus Control, Ending Status sequences and any Information Transfers that are in context.

Busy - A condition which will prevent selection even though the drive is operational and ready. A busy condition occurs when the opposite port has selected or reserved the drive, whenever the drive is Active, or whenever the drive has a Time Dependent Operation taking place.

Status Pending - The drive has a Status Response for the controller. The Status Pending Interrupt is active.

Active - The drive has accepted a command and not yet generated the corresponding Drive Status with the Time Dependent Operation bit reset or activated the Command Completion Interrupt. The drive is unavailable for another command.

Inactive - The drive has no command outstanding, but is capable of receiving one from the controller.

Reset - The drive is in an initialized condition where it has no cognizance of past events. This condition can come about as a result of an external reset by the controller, an internal initialization, e.g., power on, or an unsuccessful recovery attempt from a severe drive error.

9.4 Dual Port

The dual port consists of port Enable/Disable controls and the constructs for switching the drive between 2 ports. When both ports require the use of the drive simultaneously, they must arbitrate to determine which port will gain access and which port will receive a Busy indication. The IPI-2 will allow only 1 port to gain selection of the drive at any given time. A port attempting to select, when the alternate port has already selected or reserved the drive, would receive a Busy indication at the time of selection. This method of dual port relies on the physical interface Busy mechanism. When a port is Busy and a selection attempt is made, the port will assert the SLAVE IN signal with no bit significant Radial Address during the Selection Sequence.

If a port gains selection and issues a Reserve command, the alternate port will receive a Busy indication until the reserving port issues a Release command, an appropriate Reset is received from either port or a Priority Select is received from the alternate port. This allows the reserving port to deselect, while a Busy condition is maintained on the alternate port.

If a port gains selection and issues a Priority Reserve command, a Priority Select from either port will not break the reservation. This allows the reserving port to hold the port switch regardless of the physical Selection state.

If a port gains selection and issues a command requiring the Time Dependent Operation bit to be set in the Drive Status Byte, the alternate port receives a Busy indication until the command is complete. This prevents the alternate port from selecting the drive, should the selected port deselect before the command has completed execution. The selected port will receive a Busy indication (in the Drive Status Byte) if it attempts to issue further Bus Controls before the current command completes execution. Upon command completion, the drive posts a Command Completion Interrupt (Class 1 Interrupt) to the selected port, and clears the Busy indication from both the selected and alternate ports.

9.4.1 Drive Accessibility

The drive can appear in 1 of 2 accessibility modes; Neutral or Switched. While in the Neutral mode, the drive can be accessed via either enabled port.

The drive can become switched to a port under the following conditions:

- Selection of the port. If the Reserve or Priority Reserve Function is issued, the drive will remain switched to the port after deselection.
- A Priority Select is issued during a Selection Sequence.

The drive remains switched to a port until one of the following conditions occur:

- Deselection of the port and the port is not reserved.
- Deselection of the port and a reserved port has executed a Release Function.
- An appropriate reset is executed on the port.
- The alternate port issues a Priority Select and the current port is not Priority Reserved.
- The drive is powered off.

9.4.2 Port Enable/Disable

Ports may be individually enabled or disabled by command and by manual switches. When a port is disabled, it is made Not Operational at the Physical Interface. Both ports are enabled on power on, if not disabled by manual means. The disabling of a port takes effect without regard to the state of the interface.

If a port gains selection and issues a Disable Alternate Port Command, the alternate port is made Not Operational at the physical interface until the selected port issues an Enable Alternate Port command. If a port is disabled by command, changing the manual port switch from Disabled to Enabled will cause the port to be Enabled. However, the disabling of a port by manual switch cannot be overridden by command.

The disabling of a port, either by command or switch, will cause any explicit or implicit reservation to be cleared and will cause any status associated with the disabled port to be reset.

9.4.3 Notification of Alternate Port Exception Condition

When an attempt to access a drive is rejected because it is Switched to the other port, the drive reports the cause of the Busy condition by activating the Busy bit in the Drive Interrupts Byte and the Attention signal if enabled.

The following conditions on the alternate port are reported by the drive as an Unsolicited Exception in the Status Response:

- Priority Select issued
- Power On or Selective Drive Reset complete
- Format complete - it is the controllers responsibility to issue the Notify Alternate Port of Format Changed Function for this status to be issued to the alternate port.
- Format changed - a new Format Specification is received.

9.4.4 Attention

When the drive is in the Neutral mode, Attention is sent to both ports. When the drive is switched, but not selected, the Attention is sent to the switched port. The generation of Attention from the interrupts may be enabled/disabled on a port basis by command. All Attention generation is enabled upon reset.

9.5 Reset

A reset, in the form of a Master Reset or a Selective Reset can be presented by the controller at any time regardless of the condition of the drive. It affects the port over which it is received and the drive, if not Switched to the alternate port.

The Master Reset and the Reset Physical Interface Selective Reset reset the Physical Interface but do not affect any port switch, explicit allegiance, pending interrupts, or the Format Specification.

The Reset Logical Interface type Selective Reset resets all of the logical interface including any pending interrupts and any implicit allegiance to that port. It does not affect the state of any port switch or the Format Specification.

The Reset Drive type of Selective Reset resets the entire drive including pending interrupts, any allegiance, any port switch and the Format Specification.

9.6 Head Control

The drive's head addressing register is loaded by the Load Head Address and Load Position controls. It is incremented at the end of a successful data transfer if bit 4 of the Data Control is set. A successful transfer requires that the Successful Information Transfer bit be set in both the Controller Status and the Drive Status.

The address of the first head is zero and the address of the last head is 1 less than the number of heads specified in the Configuration. The counter increments to zero after the last head address.

9.7 Rotational Position Sensing (RPS)

The RPS feature provides the ability for the drive, when on the addressed cylinder, to generate a Class 2 RPS Interrupt and, if enabled, an Attention to the controller during the sector time that the heads are over the target sector. The target sector mechanism is also used to define a target sector for target type Data Controls. The target sector is defined by the controller to occur sufficiently ahead of the desired sector to allow successful attachment and data transfer.

9.7.1 Target Sector Address

The target sector is established by transferring a valid physical sector number to the drive by a Load RPS Target Sector or Load Position control. An address of X'FFFF' disables RPS. The target sector is initialized to X'FFFF' on power-on.

9.7.2 RPS Interrupt

The RPS Interrupt is active for 1 sector time when the sector is under the heads. It is deactivated when the drive receives a Data Control or RPS is disabled. If RPS is active at the time the drive completes a seek, the normal Command Completion Interrupt is not generated. If there is status pending, the RPS Interrupt is not generated.

9.8 Drive ECC (optional)

The drive may optionally perform its own ECC on any or all fields of the sector. A Drive Status code is provided for notifying the controller of a drive detected data error. The Read Correction Vectors Control is provided to allow the controller to obtain the correction vectors from the drive. The ECC function can be disabled and enabled by Load Drive Function codes.

9.9 Power Sequencing

Power Sequencing provides a means for the controller to sequentially start the motors of the drives, so as to reduce the power line surge current, while the drives reach operating speed. The controller shall issue a Spin Up function to each drive as it becomes operational. The Command Completion interrupt for this function occurs after the drive is up to speed and reaches the Ready condition.

10.0 BUS CONTROLS (110.01)

The Bus Controls specify the condition of the bus and the information to be transferred. The 3 types of Bus Controls are; Command, Response, and Data.

10.1 Command/Response Controls

The Command and Response Controls are forms of the Bus Control Byte which allow commands to be transmitted to the drive and responses to be read from the drive. The command and response information transferred consists of ordered lists of parameters. Parameters are transmitted most significant octet first (see Table 5).

The valid Command/Response Controls and their hexadecimal codes are listed below and described in the following sections. All other Command/Response Control codes are rejected as being unsupported.

BUS CONTROL CODE	COMMAND/RESPONSE CONTROL
01	Load Drive Function
02	Load Format Specification
03	Load Drive Specific Information
04	Load Cylinder Address
05	Load Head Address
06	Load RPS Target Sector Address
07	Load Position
41	Read Configuration
42	Read Format Specification
43	Read Drive Specific Information
44	Read Status
45	Read Correction Vectors (optional)
46	Read Current Sector Address
47	Read Current Position
48	Read Extended Status

10.1.1 Load Drive Function (01)

The Load Drive Function control causes the drive to perform the function specified in the function code. The function code is carried in both octets of the 2 octets transmitted to the drive. If the 2 octets are not the same, the Command is rejected as containing an illegal parameter. The format of the command parameters are as follows:

OCTET	PARAMETERS
0	Function code
1	Function code (repeated)

The various functions and their hexadecimal codes are listed below:

CODE	FUNCTION
10	Disable Alternate Port

This function causes the drive to disable the alternate port making it Not Operational at the Physical Interface.

11	Enable Alternate Port

This function causes the drive to enable the alternate port, thereby making it Operational at the Physical Interface. Both ports are enabled at power on.

12	Disable Port

This function causes the drive to disable the port over which it received this function making it Not Operational. This function takes effect when the controller deselects from this port.

13	Priority Reserve

This function causes an unconditional reserve of the drive for this port. A Selection from the alternate port with the Priority Select bit set will override a Priority Reserve.

14	Reserve

This function causes the drive to be reserved to this port until released, a Priority Select is executed by the alternate port, or cleared by an appropriate reset.

CODE	FUNCTION

15 Release

This function causes the drive to be released from this port and to enter the Neutral mode. This function takes effect when the controller deselects from this port. Both ports are released at power on and following a reset.

16 Notify Alternate Port of Format Completion

This function sets the Format Completed bit in the Status Response for the alternate port.

18 Disable Command Completion (Class 1) Interrupt Attention

The function causes the drive to disable the Command Completion Interrupt from generating an Attention on this port.

19 Enable Command Completion (Class 1) Interrupt Attention

This function causes the drive to enable the Command Completion Interrupt to generate an Attention on this port after each command. It is enabled after a reset and power on.

1A Disable RPS (Class 2) Interrupt Attention

The function causes the drive to disable the RPS Interrupt from generating an Attention on this port.

1B Enable RPS (Class 2) Interrupt Attention

This function causes the drive to enable the RPS Interrupt to generate an Attention on this port. It is enabled after a reset and power on.

1C Disable Status Pending (Class 3) Interrupt Attention

The function causes the drive to disable the Status Pending Interrupt from generating an Attention on this port.

1D Enable Status Pending (Class 3) Interrupt Attention

This function causes the drive to enable the Status Pending Interrupt to generate an Attention on this port. It is enabled after a reset and power on.

1E Disable "No Longer Busy" Interrupt Attention

This function causes the drive to disable the "No Longer Busy" Attention on this port. "No Longer Busy" Attention is also disabled by reset and power on.

1F Enable No Longer Busy Interrupt Attention

This function causes the drive to enable the "No Longer Busy" Attention on this port.

20 No Operation

This function performs no operation.

22 Spin Up *

This function causes the drive to turn on its motor. If it cannot perform this operation an exception status is set in the Status Response. The Command Completion Interrupt is generated when the drive is up to speed and On Cylinder. If the drive motor is on, the Time Dependent bit of the Drive Status is not set. Resets do not effect the power state of the drive motor.

23 Spin Down

This function causes the drive to turn off its motor. If it cannot perform the operation, an exception is set in the Status Response. Resets do not effect the power state of the drive motor.

28 Recalibrate *

This function causes the drive to move the heads to cylinder 0. The Command Completion Interrupt is generated when the drive reaches the on cylinder condition. This movement is achieved by means other than a normal seek and should not be used other than to recalibrate a positioner that is in error.

29 Execute Internal Diagnostic *

This function causes the drive to execute its built-in diagnostic(s). The Command Completion Interrupt is generated when diagnostic execution has completed.

* Time Dependent Operation

CODE	FUNCTION
2B	Perform Sector Marking *

This function causes the drive to format the currently selected track with Address Marks in accordance with the Format Specification. If the drive cannot perform this function or if the current Format Specification does not indicate that soft sectoring is to be used, the function causes an exception.

2C Disable Drive ECC (optional)

This function causes the drive to disable the drive ECC mechanism.

2D Enable Drive ECC (optional)

This function causes the drive to enable the drive ECC.

41 Reset Offset *

This function clears any head offset. Offsets are also cleared by seeks, head select commands, power on, and logical level resets.

42 Set Positive Offset *

This function causes the drive to offset its heads in the positive direction (away from spindle).

43 Set Negative Offset *

This function causes the drive to offset its heads in the negative direction (towards spindle).

44 Same as Code 42

45 Same as Code 43

46 Same as Code 42

47 Same as Code 43

* Time Dependent Operation

CODE	FUNCTION
48	Set Normal Strobe

This function causes the drive to set normal data strobe. Strobes are cleared by seek and head select commands.

49	Set Early Strobe

This function causes the drive to set an early data strobe. Strobes are cleared by seek and head select commands.

4A	Set Late Strobe

This function causes the drive to set a late data strobe. Strobes are cleared by seek and head select commands.

81	Disable Read/Write Diagnostic Tests

This function causes the drive to disable its internal read/write disk diagnostics. The read/write diagnostic tests are enabled at power on and by an appropriate reset unless disabled by manual switches.

10.1.2 Load Format Specification (02) *

The Load Format Specification control transmits a Format Specification to the drive. The Format Specification is described in 9.2. The format of the command parameters are as follows:

OCTET	PARAMETERS
0-1	Number of octets following: equals n-1
2-3	Format Type Code and Flag Byte
4-n	Remainder of Format Specification (optional)

If the Format Type Code is "01h" and bit 6 of the Flag Byte is set, the Manufacturers Format Specification is invoked and no more parameters need be supplied by the controller.

* Time Dependent Operation

10.1.3 Load Drive Specific Information (03)

The Load Drive Specific Information transmits drive specific information to the drive. The format of the command parameters are as follows:

OCTET	PARAMETERS
0-1	Number of octets following: equals n-1
2-3	Command Identifier
4-n	Command Parameters

Load Sync Byte Value (0020)

This command allows the controller to specify the Sync Byte value to be used by the drive for Write/Read operations. If the command parameter is X'00', the drive will insert its default Sync Byte value. The default Sync Byte value can be obtained from the configuration information. The format of the command is as follows:

OCTET	PARAMETERS
2-3	Command Identifier = X'0020'
4-5	Sync Byte Value (Repeated in both octets)

CAUTION

If a "Load Sync Byte Value" command is used in conjunction with a "Load Format Specification" command, the latter must precede the former.

Load Device Unique Identifier (0021)*

This command allows the controller to load the Device Unique Identification Number. The Device Unique ID can be read by issuing the Read Configuration Response. The format of the command is as follows:

OCTET	PARAMETERS
2-3	Command Identifier = X"0021'
4-B	Device Unique Identifier

* Time Dependent Operation

Load Read Gate Delay Value (0022)

This command allows the controller to specify the Read Gate Delay Value to be used by the drive for write/read operations. If the command parameter is X'00', the drive will insert its default Read Gate Delay Value. The default Read Gate Delay Value can be obtained from the configuration information. The format of the command is as follows:

OCTET	PARAMETERS
2-3	Command Identifier = X'0022'
4-5	Read Gate Delay Value (repeated in both octets)

CAUTION

If a "Load Read Gate Delay Value" command is used in conjunction with a "Load Format Specification" command, the former must precede the latter.

If the Read Gate Delay Value is changed and not restored to the original value prior to powering down the device, the manufacturers default specification will be loaded at the next device power up.

10.1.4 Load Cylinder Address (04) *

The Load Cylinder Address control causes the drive to seek to the cylinder specified in the 4 octets transmitted to the drive. Any head or strobe offset is cleared. The format of the command parameters are as follows:

OCTET	PARAMETERS
0-3	Cylinder address

* Time Dependent Operation

10.1.5 Load Head Address (05)**

The Load Head Address control causes the drive to select the head specified in the 2 octets transmitted to the drive. Any head or strobe offset is cleared. When head or strobe offsets are cleared by the Load Head Address command, the command becomes a Time Dependent Operation. The format of the command parameters are as follows:

OCTET	PARAMETERS
0-1	Head address

10.1.6 Load RPS Target Sector Address (06)

The Load RPS Target Sector Address control causes the drive to select the physical sector specified in the 2 octets transmitted to the drive for the target. The RPS function is disabled if the sector address is X'FFFF'. The command completes with the Time Dependent Operation bit in the Drive Status Byte reset. The format of the command parameters are as follows:

OCTET	PARAMETERS
0-1	RPS target sector address

10.1.7 Load Position (07) *

The Load Position control causes the drive to seek to the specified cylinder, select the specified head and select the specified RPS target sector. Any head or strobe offset is cleared. If RPS is enabled, the normal Command Completion Interrupt is not generated. If the RPS target sector address is set to X'FFFF', then RPS is disabled. If the RPS is disabled, only the Command Completion Interrupt is generated. The format of the command parameters are as follows:

OCTET	PARAMETERS
0-3	Cylinder address
4-5	Head address
6-7	RPS target sector address

* Time Dependent Operation
** Time Dependent Operation for some conditions

10.1.8 Read Configuration (41)

The Read Configuration control causes the drive to transfer configuration information to the controller. See the appropriate Product Specification for configuration details. The format of the command parameters are as follows:

OCTET	BIT	PARAMETERS
0-1		Number of octets following: equals n-1
2		Device Class Code (X'01' = disk)
3		Drive type Flag Byte
	7	Non-removable disk
	6	Removable disk
	5	Reserved
	4	Fixed head disk
	3	Moving head disk
	2	Reserved
	1	Reserved
	0	Reserved
4		Capability Flag Byte
	7	Reserved
	6	Variable Block Mode
	5	Fixed Block Mode, fixed sector length
	4	Fixed Block Mode, programmable sector length
	3	Soft sector
	2	Hard sector
	1	Field Data Controls
	0	Sector Data Controls
5		Feature Flag Byte
	7	RPS
	6	Dual port
	5	Drive ECC
	4	Reserved
	3	Drive Responds to adjacent odd-even select addresses for dual actuators
	2	Drive responds to adjacent odd-even select addresses for dual devices per actuator
	1	Drive restores last loaded Format Specification
	0	Fixed Format Specification

OCTET	BIT	PARAMETERS
6-9		Address of last data cylinder
A-D		Address of last Defect List cylinder
E-F		Number of heads per cylinder
10-11		Number of fixed sectors per track
12-15		Number of octets per track: equals total octets -1
16-19		Single cylinder seek time (µs)
1A-1D		Average seek time (µs)
1E-21		Maximum seek time (µs)
22-25		Rotation time (µs)
26-29		Head switching time (µs)
2A-2D		Write-to-read recovery time (µs)
2E-31		Manufactures Identification (ASCII)
32-39		Model number (ASCII)
3A-3D		Revision number (ASCII)
3E-45		Unique Unit ID Number
46		Switch Settings (MSB=00)
47		Switch Settings (LSB)
	7	Local/Remote
	6	Disable Port B
	5	Disable Port A
	4	Disable R/W diagnostics
	3	Microcode ID 3 *
	2	Microcode ID 2 *
	1	Microcode ID 1 *
	0	Microcode ID 0 *
48		Default Sync Octet Value
49		Default Read Gate Delay Value

* Refer to the individual drive product specifications to determine the switch settings.

10.1.8.1 Number of Octets

This 2 octet parameter contains the octet count for the Configuration Response. It does not include itself in the octet count.

10.1.8.2 Device Class Code

This single octet parameter contains the device class code. The IPI-2 defines a single code, which is for magnetic disk drives.

10.1.8.3 Drive Type Flag Code

This single octet parameter contains the drive type flag. This parameter indicates whether the drive contains removable and/or non-removable media, and has fixed and/or moving heads.

10.1.8.4 Capability Flag Byte

This single octet parameter contains the drive capability flag. This parameter indicates whether the drive can operate in Variable Block Mode and/or Fixed Block Mode. If the drive functions in Fixed Block Mode then this parameter indicates whether the drive supports Sector Mode 1 and/or Sector Mode 2; soft sector and/or hard sector marks; or the Field Data Controls and/or Sector Data Controls.

10.1.8.5 Feature Flag Byte

This single octet parameter contains the drive feature flag. This parameter indicates whether the drive supports RPS, Dual Port, Drive ECC, and adjacent odd-even select addresses for dual actuators.

10.1.8.6 Address of Last Data Cylinder

This 4 octet parameter contains the address of the last user data cylinder on this drive. The first cylinder has an address of zero.

10.1.8.7 Address of Last Defect List Cylinder

This 4 octet parameter contains the address of the Defect Map cylinder on this drive.

10.1.8.8 Number of Heads per Cylinder

This 2 octet parameter contains the number of heads on this drive.

10.1.8.9 Number of Fixed Sectors per Track

This 2 octet parameter contains the number of fixed sectors per track on this drive. If the drive is not fixed sectored, this parameter will contain X'FFFF'.

10.1.8.10 Number of Octets per Track

This 4 octet parameter contains the number of physical octets per track on this drive.

10.1.8.11 Single Cylinder Seek Time

This 4 octet parameter contains the value of the single cylinder seek time in µs for this drive.

10.1.8.12 Average Seek Time

This 4 octet parameter contains the value of the average seek time in microseconds for this drive. The average seek time equals the sum of the times to perform all possible seeks divided by the number of all possible seeks.

10.1.8.13 Maximum Seek Time

This 4 octet parameter contains the value of the maximum seek time in microseconds for this drive.

10.1.8.14 Rotation Time

This 4 octet parameter contains the value of the maximum rotational latency in microseconds for this drive.

10.1.8.15 Head Switching Time

This 4 octet parameter contains the value of the maximum head switching time in microseconds for this drive.

10.1.8.16 Write-to-Read Recovery Time

This 4 octet parameter contains the value of the maximum write-to-read recovery time in microseconds for this drive. This value must be used by the controller for calculating the Controller Turnaround Delay between the last field in a sector and the first field in the next sector.

10.1.8.17 Manufacture Identification

This 4 octet parameter contains the drive manufacturers identification in ASCII.

10.1.8.18 Model Number

This 8 octet parameter contains the drive model number in ASCII.

10.1.8.19 Revision Number

This 4 octet parameter contains the drive revision number in ASCII.

10.1.8.20 Unique Unit I.D. Number

This 8 octet parameter contains the drive Unit Identification Number. The default value for this parameter is the IPI-2 Interface Logic Card serial number entered in ASCII. This value may be altered by the controller by issuing the Load Device Unique Identifier command.

10.1.8.21 Switch Settings

This 2 octet parameter contains the value of switch settings the drive reports via the Configuration Response.

10.1.8.22 Default Sync Octet Value

This 1 octet parameter contains the value of the Sync Octet used by the drive for PLO Synchronization. The Sync Octet value can be altered for defect handling by issuing the Modify Sync Octet Value command.

10.1.8.23 Default Read Gate Delay Value

This single octet parameter contains the value of the Read Gate Delay (in octets) used by the drive for read and write operations. The Read Gate Delay Value can be altered for defect handling by issuing the Load Drive Specific Information command with a Load Read Gate Delay Value command identifier.

10.1.9 Read Format Specification (42)

The Read Format Specification control causes the drive to transfer the current Format Specification to the controller. The response has the following format:

OCTET	PARAMETERS
0-1	Number of octets following: equals n-1
2-3	Format Type Code and Flag Octet
4-n	Remainder of Format Specification

10.1.10 Read Drive Specific Information (43)

The Read Drive Specific Information control causes the drive to transfer drive specific information to the controller with the following response format:

OCTET	PARAMETERS
0-1	Number of octets following: equals n-1
2-n	Drive specific information

The Read Diagnostic Status Response causes the drive to transfer the following Diagnostic Status to the controller:

OCTET	PARAMETER
2-17	Native Controlled Internal Diagnostic Status Codes
18-21	Native Controlled Internal Diagnostic Field Replaceable Unit codes
22-29	Native Controlled Internal Diagnostic Fault codes IPI Controlled Internal Diagnostic Status codes IPI Controlled Internal Diagnostic Field Replaceable Unit codes IPI Controlled Internal Diagnostic Fault codes

See the drive maintenance manual for a detailed description of the codes.

10.1.11 Read Status (44)

The Read Status control causes the drive to transfer up to 8 octets of status to the controller with the following response format:

OCTET	PARAMETER
0	Exception Status
1	Unsolicited Exception Status
2	Bus Control Exception Status
3-7	Drive Exception Status

The drive may terminate the transfer at any point if the remaining octets are zeroes. Reading the status will cause it to be cleared if the Controller Status sent to the drive indicates a successful transfer.

10.1.12 Read Correction Vectors (45) (optional)

The Read Correction Vectors control causes the drive to transfer the ECC correction vectors to the controller. If the optional Drive ECC is not implemented, this control is rejected as unsupported. The format of the response is as follows:

OCTET	PARAMETERS
0-1	Number of octets following: equals n-1
2	Error Pattern
3-5	Error octet location from start of last field transferred
6-n	Octets 2-5 repeated as needed for additional vectors

The error pattern octet is exclusive-ORed with the data octet at the specified location. If an error is in the ECC octets, no vectors are returned.

10.1.13 Read Current Sector Address (46)

The Read Current Sector Address control causes the drive to transfer the current sector address to the controller with the following response format:

OCTET	PARAMETERS
0-1	Current sector address

If the drive cannot determine the current sector address, it returns X'FFFF'. The address received by the controller may be 1 sector behind the actual sector because of the time required to transfer the response.

10.1.14 Read Current Position (47)

The Read Position control causes the drive to transfer the current position to the controller with the following response format:

OCTET	PARAMETERS
0-3	Current cylinder address
4-5	Current head address
6-7	Current RPS target sector address
8-9	Current sector address

If the RPS function is not enabled, the current RPS target sector address is X'FFFF'. If the drive cannot determine the current sector address, the current sector address is X'FFFF'. The current sector address received by the controller may be 1 sector behind the actual sector because of the time required to transfer the response.

10.1.15 Read Extended Status (48)

The Read Extended Status control causes the drive to transfer drive dependent Extended Status to the controller. The Extended Status is transferred in the following format:

OCTET	PARAMETERS
0	Interface Flags
1	Data Recovery Flags
2	Drive Control Flags
3	Drive Status
4	Drive Alarms
5-7	Reserved

10.2 Data Controls

The Data Controls provide for reading and writing on the disk. They specify the direction of the transfer, the fields involved, the orientation of those fields and Step Head control.

10.2.1 Definitions and Use

10.2.1.1 Data Control Types

There are 2 types of Data Controls, field and sector. The field controls specify operations on a single field or a pair of fields. The sector controls are composite controls which specify operations on sectors having a header and 1 or 2 data fields. The sector controls which operate on the header field only are also field controls. When using field controls, the previous field must have been operated on by a field or sector Data Control.

10.2.1.2 Head Advance Control

When bit 4 is set in any Data Control, the head counter advances at the end of a successful transfer. It is also advanced unconditionally by the Step Head control.

10.2.1.3 Orientation with the Disk

It is essential that the controller's issuing of Data Controls stays oriented with the disk and that no sectors or fields, which are intended to be operated on, are missed. A Data Control which is not received in time for the drive to act on the next sector or field following the previous Data Control causes orientation to be lost and is rejected. To prevent the first Data Control of a series from being rejected when there is no orientation, orientation must be restarted by; starting with a target type Data control or issuing a read or verify header type Data Control.

A field Data Control that operates on the header field sets sector orientation for that sector.

Orientation is not lost by a header verify miscompare or a controller initiated termination of a transfer.

10.2.1.4 Target Sector

A group of read and write Data Controls operate on the "target sector". The target is the sector set by a Load RPS Target Sector Address or Load Position command.

10.2.1.5 Data Control Reject

The Data Control can be rejected for several reasons including:

- The Format Specification is not initialized.
- The drive is active on the alternate port.
- The Data Control is a write type and the drive is write protected.
- Lost orientation.
- Invalid Data Control type.

10.2.1.6 Data Control Coding

The Data Control, which is a form of Bus Control, has the following coding:

BIT	DESCRIPTION
7	1 = Data Control, 0 = Command/Response Control
6	1 = Information In (Read), 0 = Information Out (Write)
5	0 = Fixed Block Control
4	Step Head Control
3	Header Field Operation
2	Modifier Bit Selects Target Sector for Read/Write Header operations Selects Verify Header for write operation Selects Skip Header for read operation
1	Data Field 2 operation
0	Data Field 1 operation

The above coding results in 8 groupings of Data Controls plus a special control as shown below:

DATA CONTROL			DESCRIPTION
80-83	91-93	*	Skip/Write Data Field
84-87	94-97	***	Verify Header, Write Data
88-8B	98-9B	**	Write Header, Write Data
8C-8F	9C-9F	***	Write Header, Write Data at Target
C0-C3	D1-D3	*	Skip/Read Data Field
C4-C7	D4-D7	**	Skip Header, Read Data
C8-CB	D8-DB	***	Read Header, Read Data
CC-CF	DC-DF	***	Read Header, Read Data at Target
	90		Step Head
	D0		Reserved

* Requires field orientation
** Requires sector orientation
*** Does not require orientation

10.2.2 Field Data Controls (80-83, 91-93, C0-C3, D0-D3)

The field type controls described in this section operate on a single field or a pair of fields. If one of these controls is used for the first field (header) of a sector it causes orientation to be lost and is rejected. The sector type controls which operate only on the header are a form of field controls and must be used for the first field of a sector.

The controls are described in the following sections. The first hexadecimal code is for no head step; the second is for head step.

10.2.2.1 Skip Field (80)

The Skip Field control causes the drive to skip the next field. No data is transferred.

10.2.2.2 Skip Two Fields (C0)

The Skip Two Fields control causes the drive to skip the next 2 fields. No data is transferred.

10.2.2.3 Write Field (81, 91)

The Write Field control causes the drive to write the next field with data transferred from the controller.

10.2.2.4 Skip Field and Write Field (82, 92)

The Skip Field and Write Field causes the drive to skip the next field and then write the following field with data transferred from the controller.

10.2.2.5 Write Two Fields (83, 93)

The Write Two Fields control causes the drive to write the next 2 fields with data transferred from the controller.

10.2.2.6 Read Field (C1, D1)

The Read Field control causes the drive to transfer the next field to the controller.

10.2.2.7 Skip Field and Read Field (C2, D2)

The Skip Field and Read Field control causes the drive to skip the next field and then transfer the following field to the controller.

10.2.2.8 Read Two Fields (C3, D3)

The Read Two Fields control causes the drive to transfer the next 2 fields to the controller.

10.2.3 Sector Data Controls (84-8F, 94-9F, C4-CF, D4-DF)

The sector type controls operate on sectors consisting of a Header Field, Data Field 1 and (optional) Data Field 2. The following sections describe these controls. The first of the 2 hexadecimal codes is for no head step; the second is for head step.

10.2.3.1 Verify Header (84, 94)

The Verify Header control causes the drive to verify the next header field against data transferred from the controller. If the header verifies, the drive will indicate a Successful Information Transfer in the Drive Status; otherwise the Header Not Verified status will be sent.

10.2.3.2 Verify Header and Write Data Field 1 (85, 95)

The Verify Header and Write Data Field 1 control causes the drive to verify the next header field against data transferred from the controller and, if the header verifies, continues to write Data Field 1 with data transferred from the controller. If the header does not verify, the transfer terminates after the header.

10.2.3.3 Verify Header and Write Data Field 2 (86, 96)

The Verify Header and Write Data Field 2 control causes the drive to verify the next header field against data transferred from the controller and if the header verifies, continues to write Data Field 2 with data transferred from the controller. If the header does not verify, the transfer terminates after the header.

10.2.3.4 Verify Header and Write Data Fields 1 and 2 (87, 97)

The Verify Header and Write Data Fields 1 and 2 control causes the drive to verify the next header field against data transferred from the controller and if the header verifies, continues to write Data Fields 1 and 2 with data transferred from the controller. If the header does not verify, the transfer terminates after the header.

10.2.3.5 Write Header (88, 98)

The Write Header control causes the drive to write the next header field with data transferred from the controller.

10.2.3.6 Write Header and Data Field 1 (89, 99)

The Write Header and Data Field 1 control causes the drive to write the next header field and Data Field 1 with data transferred from the controller.

10.2.3.7 Write Header and Data Field 2 (8A, 9A)

The Write Header and Data Field 2 control causes the drive to write the next header and Data Field 2 with data transferred from the controller.

10.2.3.8 Write Header and Data Fields 1 and 2 (8B, 9B)

The Write Header and Data Fields 1 and 2 control causes the drive to write the next head field and Data Fields 1 and 2 with data transferred from the controller.

10.2.3.9 Write Header at Target (8C, 9C)

The Write Header at Target control causes the drive to write the header field at the target sector with data transferred from the controller.

10.2.3.10 Write Header and Data Field 1 at Target (8D, 9D)

The Write Header and Data Field 1 at Target control causes the drive to write the header field and Data Field 1 at the target sector with data transferred from the controller.

10.2.3.11 Write Header and Data Field 2 at Target (8E, 9E)

The Write Header and Data Field 2 at Target control causes the drive to write the header field and Data Field 2 at the target sector with data transferred from the controller.

10.2.3.12 Write Header and Data Fields 1 and 2 at Target (8F, 9F)

The Write Header and Data Fields 1 and 2 at Target control causes the drive to write the header field and Data Fields 1 and 2 at the target sector with data transferred from the controller.

10.2.3.13 Skip Header (C4, D4)

The Skip Header control causes the drive to skip the next header field. No data is transferred and the drive initiates the Ending Status sequence at the end of the header field.

10.2.3.14 Skip Header and Read Data Field 1 (C5, D5)

The Skip Header and Read Data Field 1 control causes the drive to skip the next header field and transfer Data Field 1 to the controller.

10.2.3.15 Skip Header and Read Data Field 2 (C6, D6)

The Skip Header and Read Data Field 2 control causes the drive to skip the next header field and transfer Data Field 2 to the controller.

10.2.3.16 Skip Header and Read Data Fields 1 and 2 (C7, D7)

The Skip Header and Read Data Fields 1 and 2 control causes the drive to skip the next header field and transfer Data Fields 1 and 2 to the controller.

10.2.3.17 Read Header (C8, D8)

The Read Header control causes the drive to transfer the next header field to the controller.

10.2.3.18 Read Header and Data Field 1 (C9, D9)

The Read Header and Data Field 1 control causes the drive to transfer the next header field and Data Field 1 to the controller.

10.2.3.19 Read Header and Data Field 2 (CA, DA)

The Read Header and Data Field 2 control causes the drive to transfer the next head field and Data Field 2 to the controller.

10.2.3.20 Read Header and Data Fields 1 and 2 (CB, DB)

The Read Header and Data Fields 1 and 2 control causes the drive to transfer the next header field and Data Fields 1 and 2 to the controller.

10.2.3.21 Read Header at Target (CC, DC)

The Read Header at Target control causes the drive to transfer the header at the target sector to the controller.

10.2.3.22 Read Header and Data Field 1 at Target (CD, DD)

The Read Header and Data Field 1 at Target control causes the drive to transfer the header field and Data Field 1 at the target sector to the controller.

10.2.3.23 Read Header and Data Field 2 at Target (CE, DE)

The Read Header and Data Field 2 at Target control causes the drive to transfer the header field and Data Field 2 at the target sector to the controller.

10.2.3.24 Read Header and Data Fields 1 and 2 at Target (CF, DF)

The Read Header and Data Field 1 and 2 at Target control causes the drive to transfer the header and Data Fields 1 and 2 at the target sector to the controller.

10.2.4 Special Data Controls

Step Head (90) - The Step Head control causes the drive to step to the next head address. No data is transferred.

11.0 STATUS

11.1 Status Response (See Table 6)

The status bits of the Status Response indicate exception conditions. They are set on the occurrence of an exception event. The setting of any exception status bit activates the Status Pending Interrupt and the Attention In signal, if enabled.

The drive transfers the Status Response to the controller upon receiving a Read Status Bus Control and clears all exception status bits if the Controller Status Octet indicates a successful transfer. The exception status bits are also cleared by a Reset Logical Interface. All exception status bits except the Unsolicited Exception bits (octet 0, bit 6 and octet 1, bits 7 thru 0) are also cleared upon the acceptance of any Bus Control. If the Controller Status Octet indicates unsuccessful information transfer, the drive will not clear the reported Status conditions.

Drive faults are cleared when the Status Response is read if the fault no longer exists.

The Status Response has the following format:

OCTET	BIT	DESCRIPTION
0		Exception Status Byte
	7	Status Response - This bit is always reset for a Status Response.
	6	Unsolicited Exception - This bit is set when the drive has incurred an unsolicited exception condition. At least one bit will be set in octet 1 describing the exception type. This bit and the bits in octet 1 can only be reset by issuing a Read Status Bus Control followed by a Controller Status Octet with the Successful Information Transfer bit set. The drive will reject all other bus controls as long as the Unsolicited Exception exists or until the exception is gone and a Read Status command has been succesfully executed.
	5	Bus Control Exception - This bit is set when the drive rejects the Bus Control as invalid, containing an invalid parameter, unsupported, out of context, or late. At least one bit will be set in octet 2 to describe the type of Exception.

OCTET	BIT	DESCRIPTION
	4	Read Fault - This bit is set when the drive detects an error while executing a Read/Verify type Data Control. At least one bit will be set in octets 3 thru 7 to describe the type of read exception.
	3	Write Fault - This bit is set when the drive detects an error while executing a Write type Data Control. At least one bit will be set in octets 3 thru 7 to describe the type of write exception.
	2	Seek Fault - This bit is set when the drive detects a seek error while executing a Seek Command, a Read/Verify Data, or Write Data type Bus Control. At least one bit will be set in octets 3 thru 7 to describe the seek exception.
	1	Spindle Fault - This bit is set when the drive detects a spindle error while executing a Spin Up or Spin Down, a Read/Verify Data, or Write Data Bus Control. At least one bit will be set in octets 3 thru 7 to describe the spindle exception.
	0	Execution Fault - This bit is set when the drive detects an execution error other than a Read, Write, Seek, or Spindle fault during the execution of a Command or Data Bus Control. At least one bit will be set in octets 3 thru 7 to describe the exception.
1		Unsolicited Exception Status
	7	Reset Complete - This bit is set when the drive has completed execution of a reset that affects this port.
	6	Alternate Port Priority Select - This bit is set when the alternate port issues a Selection Byte with the Priority Select bit set.
	5	Alternate Port Format Changed This bit is set when the alternate port issues a new Format Specification to the drive.
	4	Alternate Port Format Complete - This bit is set when the alternate port receives a Load Drive Function Code 16, Notify Alternate Port of Format Completion.

OCTET	BIT	DESCRIPTION
	3	Reserved
	2	Not Ready Transition - This bit is set when the drive goes from a ready to not ready condition.
	1	Ready Transition - This bit is set when the drive goes from a not ready to ready condition.
	0	Media Change - This bit is set with Ready Transition bit (bit 1) if the drive detects the media was removed and replaced previous to the Not Ready to Ready transition.
2		Bus Control Exception Status
	7	Invalid Bus Control - This bit is set when a Bus Control was received that is not defined for the IPI-2 interface.
	6	Invalid Parameter - This bit is set when a valid Command Control was received with an invalid parameter.
	5	Unsupported Bus Control - This bit is set when a valid Bus Control is received that is not supported in this drive .
	4	Bus Control Context - This bit is set when a valid Bus Control is received but can not be executed because it conflicts with the current context of the drive.
	3	Data Control Late - This bit is set when a valid Data Control is received later than the orientation window for the next field.
	2-0	Reserved
3		Drive Exception Status
	7	Speed Fault - This bit is set if the drive did not reach the required speed in the required time during the execution of a Spin Up Function, or loses speed during a Data Control.
	6	Off Cylinder Fault - This bit is set if the drive did not come On Cylinder in the required time during the execution of a Seek Command, or loses On Cylinder during a Data Control.

OCTET	BIT	DESCRIPTION
	5	Head Select Fault - This bit is set if the drive detects an invalid head selection during the execution of a Head Select Command, Position Command, or Data Control.
	4	Reserved
	3	Reserved
	2	Voltage Fault - This bit is set if the drive detects a voltage out of range condition.
	1	Logic Temperature Fault - This bit is set if the drive detects an over temperature condition in the drive electronics.
	0	Reserved
4		Drive Exception Status
	7	Write Protect Fault - This bit is set when a write type Data Control is received and the drive is write protected.
	6	Reserved
	5	Write Transition Fault - This bit is set by the drive if no write transitions are detected by the drive during the execution of a write type Data Control
	4	Head Offset Fault - This bit is set if the data heads were in an offset position when a write type Data Control was Received.
	3	Data Strobe Fault - This bit is set if the drive receives a write type Data Control when early or late data strobes are active.
	2-0	Reserved
5		Drive Exception Status
	7	Diagnostic Status Valid This bit is set if a failure occurs while executing internal diagnostics (command 29), and indicates that diagnostic status is available for the controller. See Read Drive Specific Information (43).

OCTET BIT DESCRIPTION

6 Diagnostic Test Incomplete - This bit is set when the drive fails to execute a diagnostic test.

5 Write/Read Diagnostic Tests Disabled - This bit is set when the write/read diagnostic tests are disabled.

4-0 Reserved

6-7 Reserved

11.2 EXTENDED STATUS RESPONSE (See Table 7)

The drive transfers the Extended Status Response to the controller upon receiving a Read Extended Status Bus Control. The Extended Status bits are static indications of the current flag states and drive conditions.

The Extended Status Response has the following format:

OCTET BIT DESCRIPTION

0 Interface Flags

7 Extended Status - This bit is always set for an Extended Status Response.

6 Port Number - 0 = Even Port, 1 = Odd Port

5 Alternate Port Enabled - This bit is set when the alternate port is enabled.

4 Reserve Active - This bit is set when this port has reserved the drive.

3 Command Complete Interrupt Enabled - This bit is set when Command Complete Interrupts are enabled to generate an Attention on this port.

2 RPS Interrupt Enabled - This bit is set when RPS Interrupts are enabled to generate an Attention on this port.

1 Status Pending Interrupt Enabled - This bit is set when Status Pending Interrupts are enabled to generate an Attention on this port.

0 Format Specification Present - The drive currently has a valid Format Specification loaded.

OCTET	BIT	DESCRIPTION
1		Data Recovery Flags
	7	Offset Direction - If a Head Offset is in effect this bit indicates the direction of offset. This bit is cleared when positive offset (away from the spindle) is in effect, and set when negative offset (towards the spindle) is in effect.
	6	Offset MSB - This bit is the most significant bit of the Head Offset magnitude.
	5	Offset LSB - This bit is the least significant bit of the Head Offset magnitude. If bits 6 and 5 of this octet are cleared, then no head offset is in effect and bit 7 has no meaning.
	4	Early Data Strobe - This bit is set if an Early Data Strobe is active.
	3	Late Data Strobe - This bit is set if a Late Data Strobe is active.
	2	Reserved
	1	Header Field ECC/CRC Enabled - This bit is set if the drive ECC/CRC feature (optional) is enabled.
	0	Data Field ECC/CRC Enabled - This bit is set if the drive ECC/CRC feature (optional) is enabled.
2		Drive Control Flags
	7	Write Protected - This bit is set if the drive is currently write protected.
	6	Spindle Power On - This bit is set if a Spin Up Function code is in effect.
	5-0	Reserved
3		Drive Status
	7	Speed - This bit is set if the drive spindle is at operating speed.
	6	On Cylinder - This bit is set if the drives actuator is On Cylinder.
	5-2	Reserved

OCTET	BIT	DESCRIPTION
	1	HDA Ready - This bit is set when the drives spindle is up to speed, the actuator is on track and the heads are loaded.
	0	Media Present - This bit is set when the drive media is present.
4		Drive Alarms
	7	Reserved
	6	Reserved
	5	Illegal Head Select - This bit is set when the drive has the wrong head selected, multiple heads selected, or no head selected.
	4	Reserved
	3	Reserved
	2	Voltage Range Error - This bit is active when the drive has 1 or more voltages out of range.
	1	Logic Over Temperature - This bit is active when the drive logic is over maximum operating temperature.
	0	Reserved
5-7		Reserved

12.0 DIAGNOSTICS

The drive initialization and diagnostic tests provide a method for establishing a basic confidence level in the drive. Predefined tests are invoked automatically during dc power up, upon receipt of the Execute Internal Diagnostic Function (Function Code 29), or by issuing a Reset Drive Selective Reset.

If Read/Write diagnostics are to be utilized, it is the responsibility of the controller to be able to format the diagnostic track; i.e., if the diagnostic track is missing or has been destroyed, the controller must be capable of recreating the track.

If the drive detects any failures during execution, testing is terminated and the failure is reported via the Read Drive Specific Information Response. See Drive Exception Status (octet 5) of the Status Response for a description of the diagnostic failure. See the individual Product Specifications for a description of the Diagnostic Status Information, FRU and fault descriptions.

Successful completion of the diagnostic tests will leave the drive actuator on cylinder zero, with head zero selected.

The following drive initialization and diagnostic tests will be performed when the dc power on switch is enabled:

1. I/O Test

   This test executes a sequence of tests to determine the functionality of the IPI-2 I/O hardware. The tests include microprocessor self-tests and SERDES tests.

2. Drive Microprocessor Self-test

   This test executes the drive microprocessor self-test routine. See the appropriate product specifications for a description of tests.

Successful completion of these tests will allow the start up test to begin.

The following drive initializations and diagnostic tests will be performed when the start switch is enabled.

1. Servo Test

   This test automatically performs the following seek operations:

   - Return to Zero
   - Single Track Seek
   - Servo Recalibrate (Servo MPU)
   - Maximum Seek

   Successful completion of this test will allow the Head Select test to begin if Write/Read diagnostics is enabled.

2. Head Select Test

   Same as head select test defined in Execute Internal Diagnostic Function tests. Successful completion of this test will allow the Write/Read tests to begin.

3. Write/Read Test

   Same as head select test defined in Execute Internal Diagnostic Function tests. Successful completion of this test will allow the handshake test to be completed.

4. Handshake Test

   This test verifies that the drive has completed the requested tests, updated status and that the drive is in the Ready condition.

The following diagnostic tests will be performed upon receipt of the Execute Internal Diagnostic Function:

1. Access Test

   This test performs the following seek operations:

   - Return to Zero
   - Single Track Seek
   - Servo Recalibrate (Servo MPU)
   - Maximum Seek
   - Random Seek

   Successful completion of this test will allow the Head Select test to begin if the Disable Write/Read Diagnostic bit is not set. The head select and Write/Read tests can be disabled by issuing the Disable Read/Write Diagnostics Function Code or by manual switch.

2. Head Select Test

This test performs a seek to the Diagnostic cylinder, waits for on cylinder, and sequentially selects all heads on the cylinder.

Successful completion of this test will allow the Write/Read tests to begin.

3. Write/Read Test

The write and read tests are executed if the drive is in the Ready condition, is not write protected and no faults are present.

The header is read and verified on the Diagnostic cylinder and if no errors reported then the Write/Read test begins.

Data patterns are written to the Diagnostic cylinder. The patterns are then read and verified.

The maximum execution time for the diagnostic tests is 60 s.

Diagnostic Track Format Specification

The controller can format or restore the diagnostic R/W track by issuing a Load Format Specification Control selecting these options.

Number of octets following	=X' 0012'
Format typecode	=X' 01'
Flag byte	=X' 27'
Number of sectors per track	=X' 0001'
Number of octets per sector	=X' FFFFFFFF'
Number of beginning octets to be skipped	=X' 0000'
Number of fields per sector	=X' 0001'
Number of octets per field 0	=X' FFFFFFFF'
Controller turnaround delay 0	=X' 0000'

The Drive will calculate the number of octets per field and the number of octets per sector. The Controller can determine the length of the fields by using a Read Format Specification Control.

The Sync Byte value must be changed to X'AD' by issuing a Load Drive Specific Information Control. The Controller must write the diagnostic cylinder in the format shown in Figure 33.

13.0 DEFECT MAP

The drive supports a Defect Map containing a list of defects found by the manufacturer. This Defect Map is for use by the controller to reallocate or map/mask out defective storage when formatting the drive. The tracks used for the Defect Map are formatted with the Manufacturers Format Specification (see 9.2.3).

13.1 Map Location

The Defect Map is written starting on the last track of the cylinder identified in the Configuration Information as the Address of the Defect Map Cylinder. The map continues on tracks of decreasing address, if additional storage is needed.

13.2 Defect Map Contents

Each sector in the Defect Map is self identifying. A defect map set consists of a sector repeated 3 times, with each data field identified as to whether it is the first, second or third sector of a set. If a data field is not readable without errors at the factory, then it will be identified. A set may consist of more than 3 sectors, being made up of 3 readable data fields and any data fields with read errors.

13.3 Defect Format

Each defect entry in the map is 12 octets in length. The defects in the Defect Map are stored in order of increasing physical addresses. An exception is made for defects that are detected after the initial map was recorded, and are added to the end of the defect map during final manufacturing test. Any additions that are made out of sequence are indicated by setting the Flag bit within that data field.

13.4 Map Format

The map is recorded with each sector recorded error free 3 times sequentially. Each data field in a set is identical to the other two. The following describes the contents per field, with the implicit understanding that each sector is physically recorded 3 times.

The format of each data field is shown below:

OCTET	BIT	DESCRIPTION
0-1		Number of octets following: equals n-1
2		Flag Byte
	7	Last data field of Defect Map
	6	Defect Map continues on next lower cylinder
	5	Sector Defect list used
	4	Defect Fields option used
	3	Defect Entries in this sector out of sequence
	2-0	Reserved
3		Number of this sector within a set 00 = First 01 = Second 02 = Third 03-FE = Illegal FF = Ignore
4-5		Number of Sets in Defect Map
6-7		Number of this set in the Defect Map
8-B		Cylinder Address of Format Specification Storage
C-D		Head Address of Format Specification Storage
E-11		Cylinder Address of Defect
12-13		Head address of defect
14-17		Offset of defect from Index (octets)
18-19		Length of defect (bits)
(M-B)-(M-8)		Cylinder address of defect
(M-7)-(M-6)		Head address of defect
(M-5)-(M-2)		Offset of defect from Index (octets)
(M-1)-M		Length of defect (bits)
(M+1)-(n-2)		Zero (if any octets not filled by defect entries)
(n-1)-n		CRC-16

13.4.1 Number of Bytes

Each data field of the map starts with a 2 octet count of the number of octets used in the field, not including itself.

13.4.2 Flag Byte

The first data octet is the Flag Byte which describes the format of the field.

13.4.3 Number of Sector Within the Set

All sectors within the Defect Map are identified by their sector number within a set or are set to X'FF' to be ignored.

13.4.4 Number of Sets

The Number of Sets in the Defect Map, and the Number of this Set within the map occupies the next 2 fields.

13.4.5 Address of Format Specification Storage

The following 2 fields provide the address of the first track at which the controller may store the Format Specifications and attributes in the Manufactures Default format. This field is initialized to the next available track following the Defect Map.

13.4.6 Defect Entry

These octets are used to describe the defect itself. The last 12 octet defect entry cannot be split, therefore any remainder of less than 12 octets will be zeros. Similarly, the remainder following the last defect entry will be padded with zeros.

13.4.7 CRC-16

The 2 octet CRC-16 ($X^{16} + X^{15} + X^2 + 1$) is the last 2 octets in the data field, and is considered part of the data area. It is the controllers responsibility to check the CRC.

14.0 FORMAT SPECIFICATION STORAGE

The controller typically has the need to store Format Specifications and Attributes on the disk. The storage of the Format Specification is the controllers responsibility, and may be stored anywhere on the media in the preferred format of the controller. If the controller records them in the area according to the Manufactures Default Format Specification, the address of the area is defined in each Defect Map data field. The recommended format of each data field is as follows:

OCTET	BIT	DESCRIPTION
0-1		Number of octets following: equals n-1
2		Flag Byte
	7	Last data field of storage
	6-0	Reserved
3		Number of this Sector within a Set
		00 = First
		01 = Second
		02 = Third
		03-FE = Illegal
		FF = Ignore
4-5		Number of Sets in Format Specification Storage
6-7		Number of this Set in the Format Specification storage
8		Partition
9		Alias address
A-D		Number of octets per Data Block
E		Flags
	7	Data Block same size as Physical Block
	6	Data Block multiple of Physical Block
	5	Data Block non-multiple of Physical Block
	4-1	Reserved
	0	Interleaves performed by controller
F		Cylinder interleave factor
10		Head interleave factor
11		Sector interleave factor
12		Number of alternate cylinders per Partition
13		Number of spare sectors per track
14-17		Partition starting cylinder address
18-1B		Number of cylinders in Partition
1C-1D		Number of octets in Format Specification m-1
1E-(m+19)		Format Specification (see 9.2) repeat octets 4-(m+19) for additional Partitions
(m+1A)-(n-2)		Zero (if any octets not filled by entries)
(n-1)-(n)		CRC-16

If the drive is not used with the IPI Level 3 interface, octets 8-1B are not used and shall be zeroes.

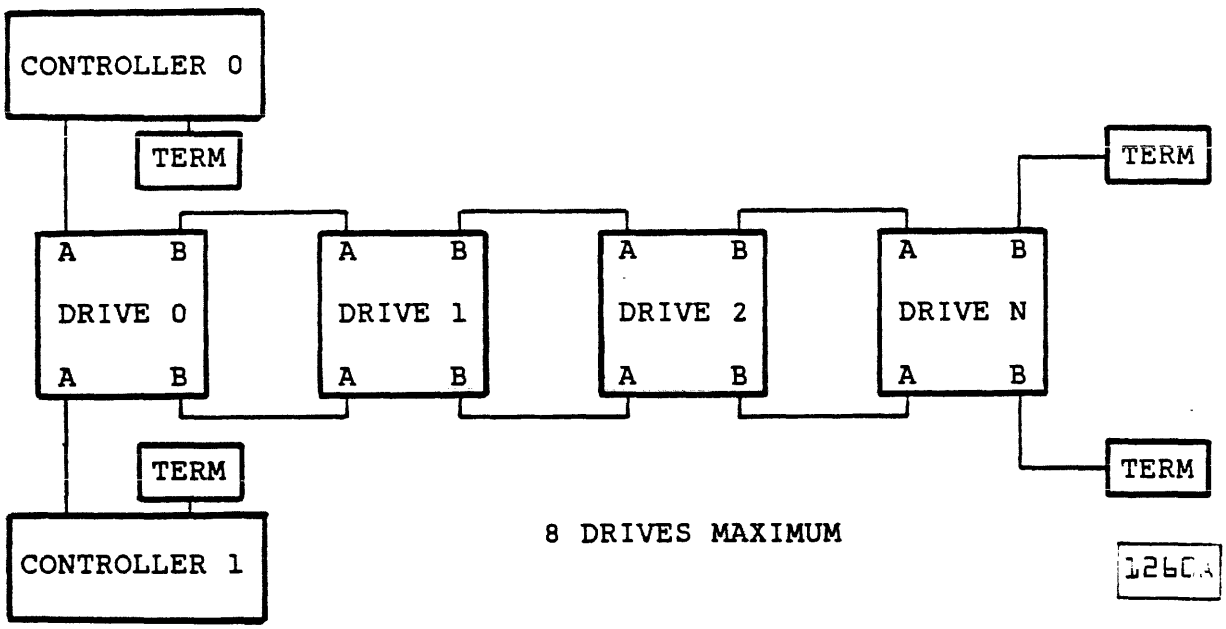


FIGURE 1. IPI CONFIGURATION

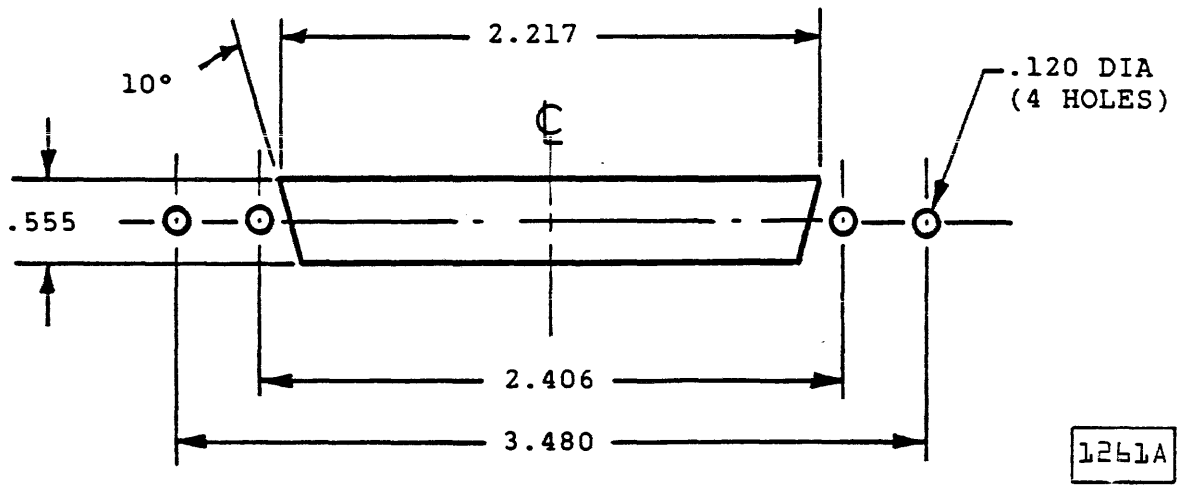


FIGURE 2. CONNECTOR RETENTION

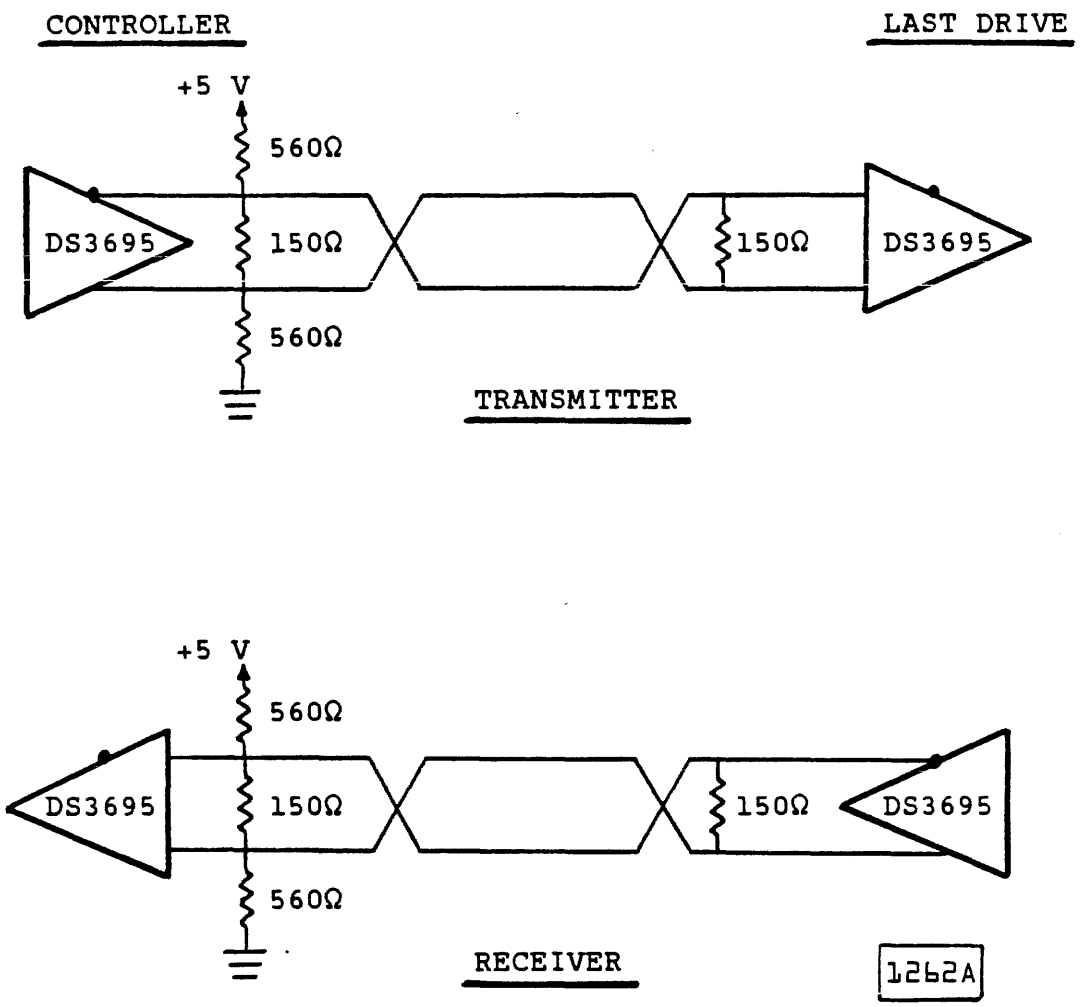


FIGURE 3. TRANSMITTER/RECEIVER TERMINATION AND BIASING

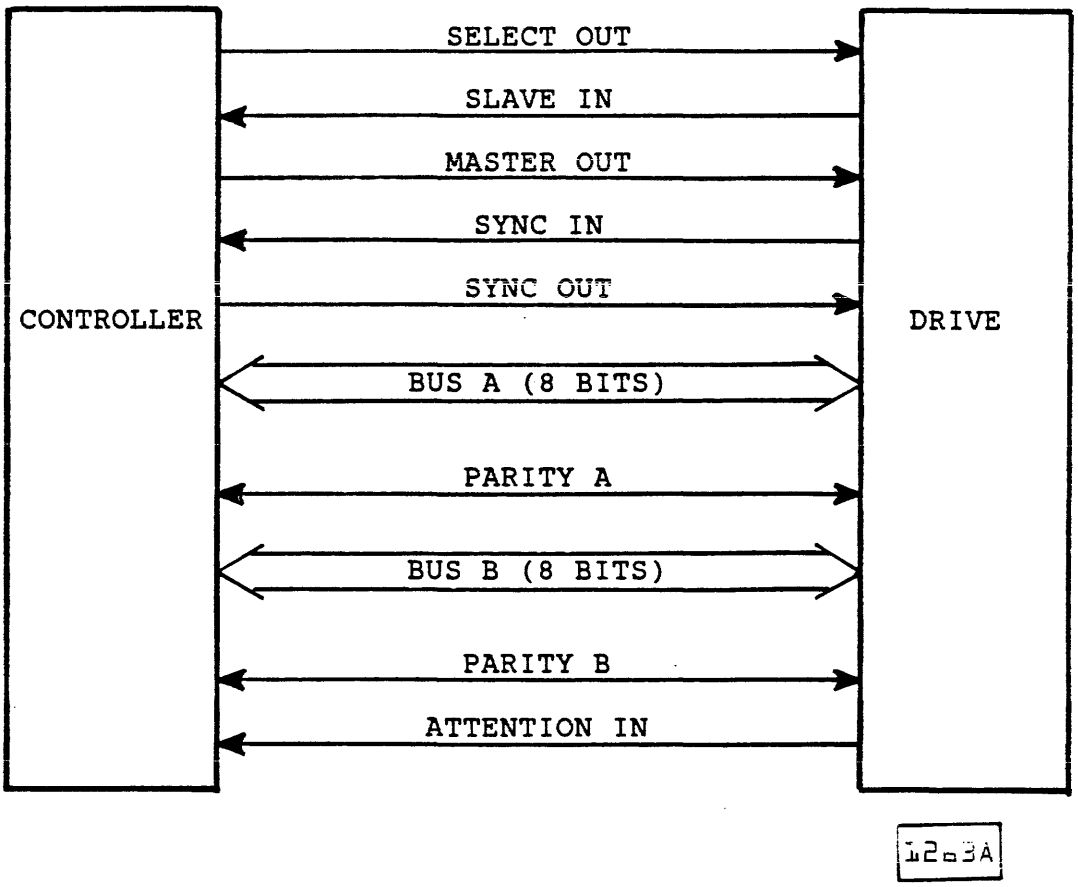
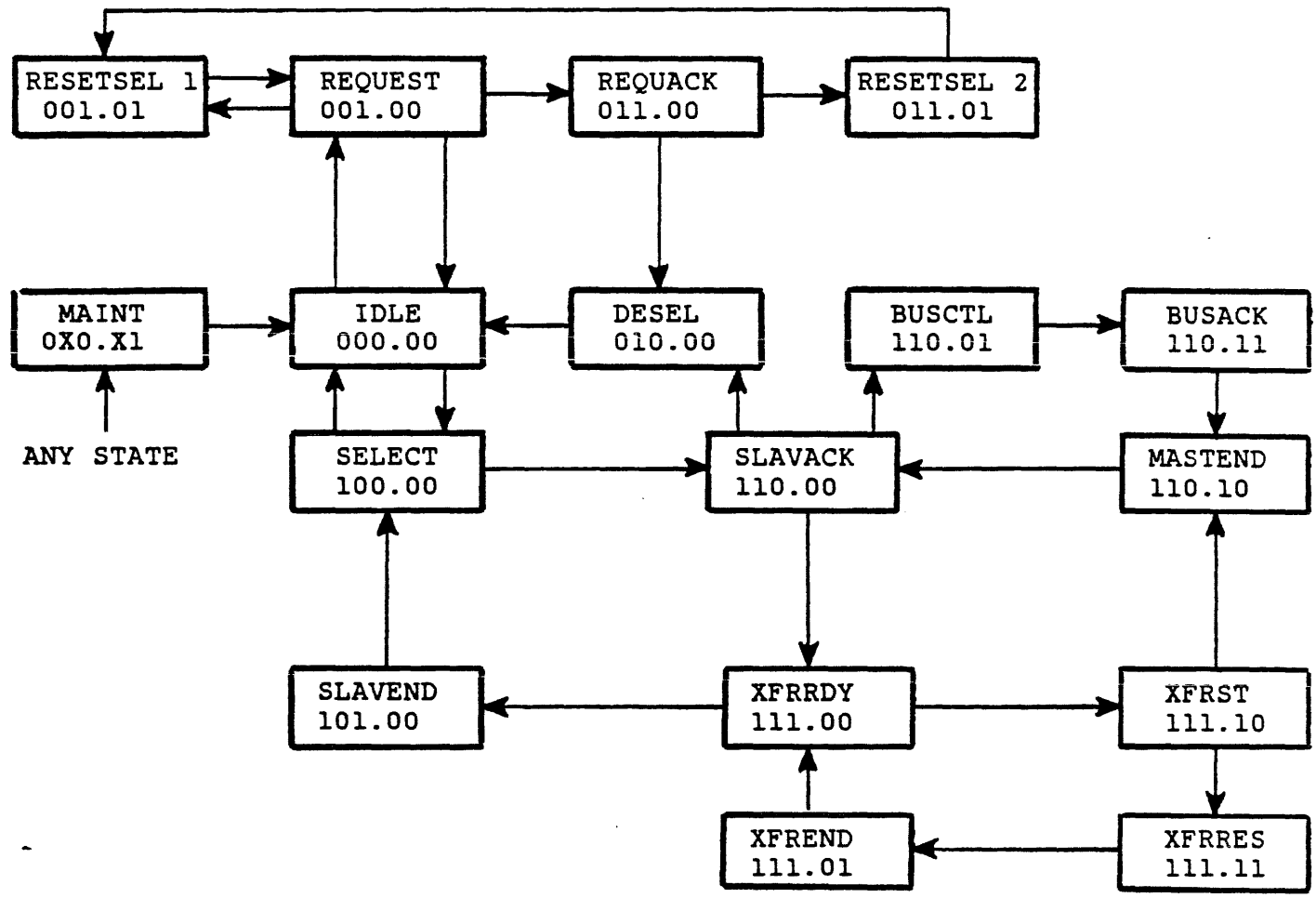


FIGURE 4. IPI INTERFACE SIGNALS



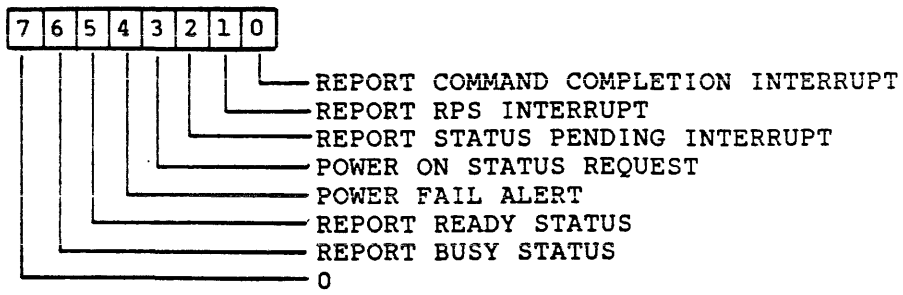
DEFINITION: XXX.XX

- SYNC OUT
- SYNC IN
- MASTER OUT
- SLAVE IN
- SELECT OUT

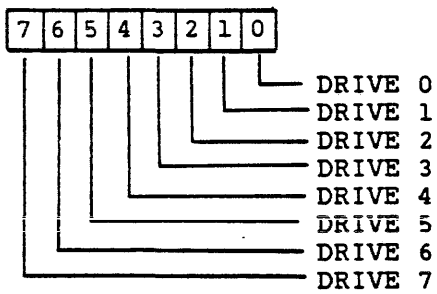
1264A

FIGURE 5. BUS STATE DIAGRAM

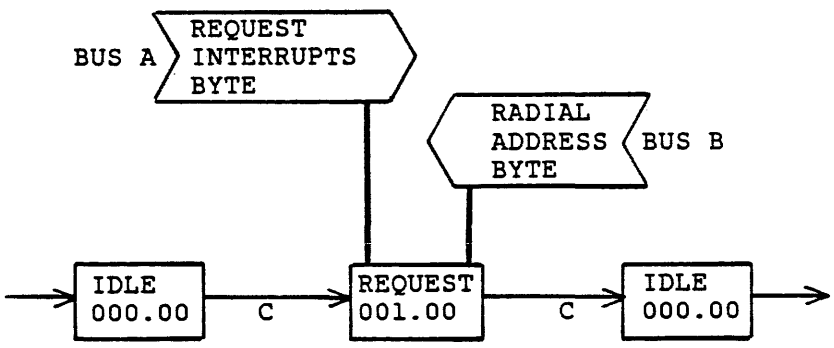
REQUEST INTERRUPTS BYTE (CONTROLLER)



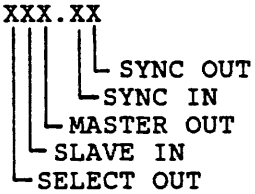
RADIAL ADDRESS BYTE (DRIVE)



REQUEST INTERRUPTS SEQUENCE

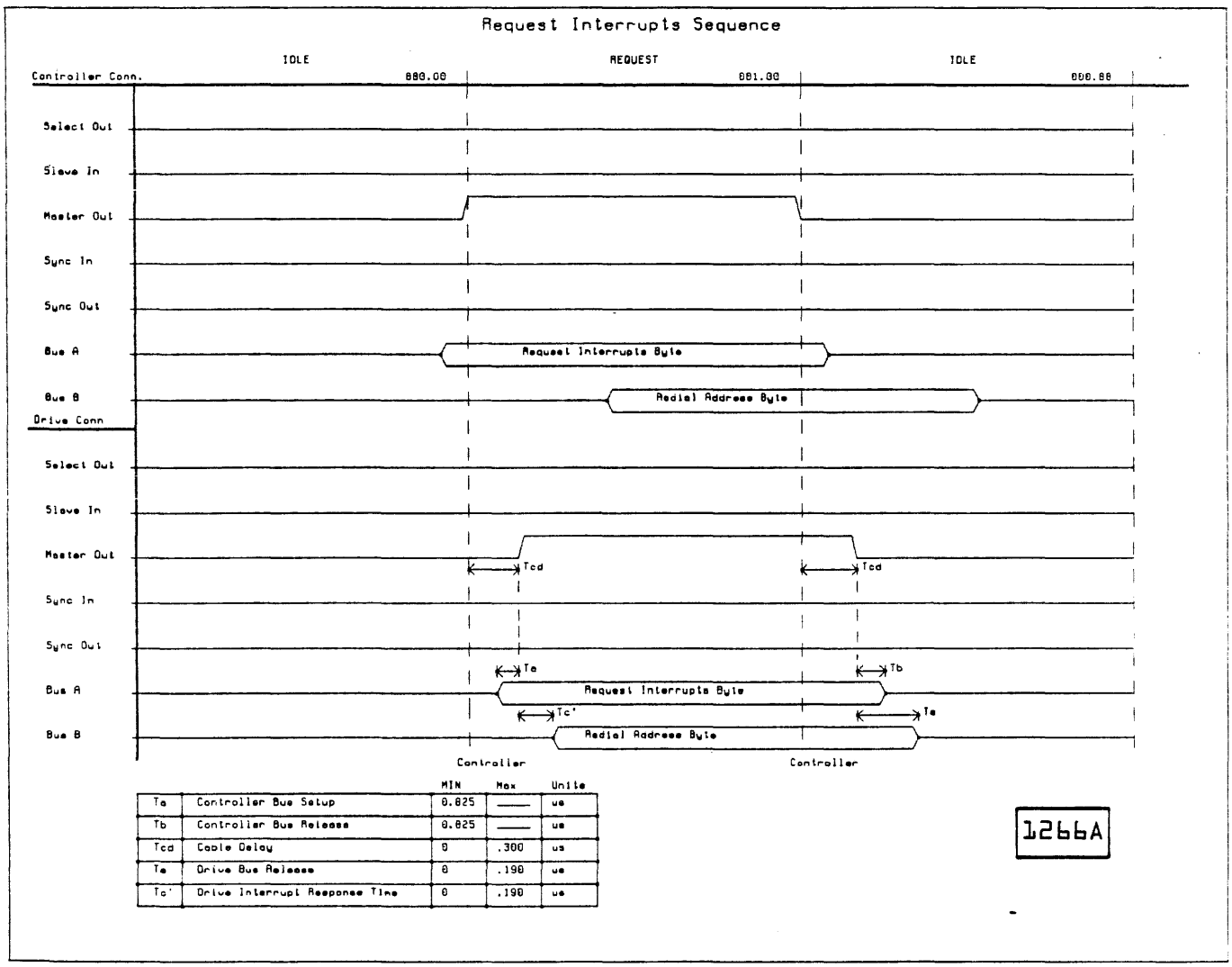


DEFINITION: XXX.XX



1265A

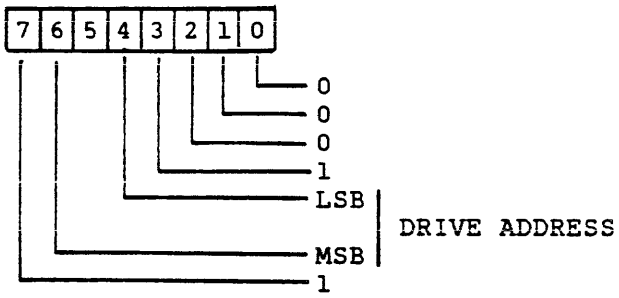
FIGURE 6. REQUEST INTERRUPTS SEQUENCE



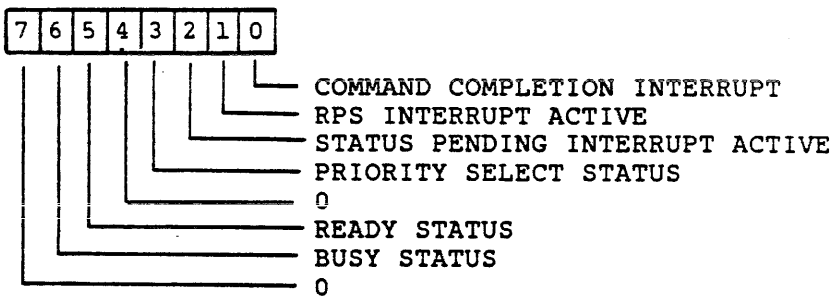
		MIN	Max	Units
Ta	Controller Bus Setup	0.825	——	us
Tb	Controller Bus Release	0.825	——	us
Tcd	Cable Delay	0	.300	us
Te	Drive Bus Release	0	.190	us
Tc'	Drive Interrupt Response Time	0	.190	us

FIGURE 7. REQUEST INTERRUPTS TIMING

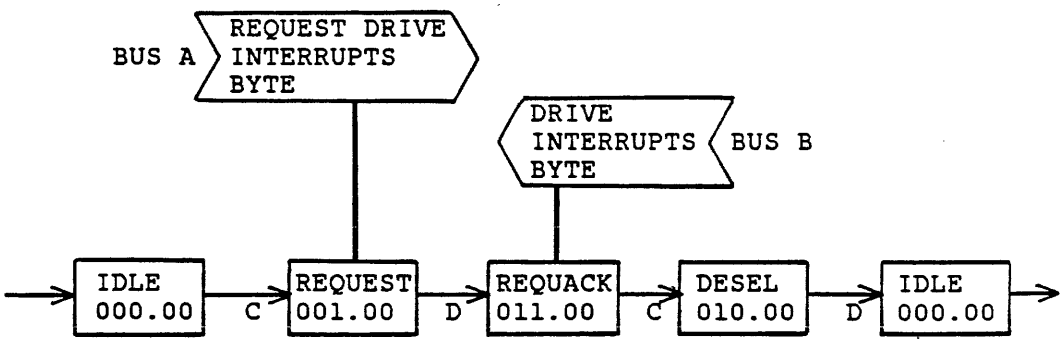
REQUEST DRIVE INTERRUPTS BYTE (CONTROLLER)



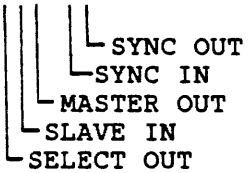
DRIVE INTERRUPTS BYTE (DRIVE)



REQUEST DRIVE INTERRUPTS SEQUENCE

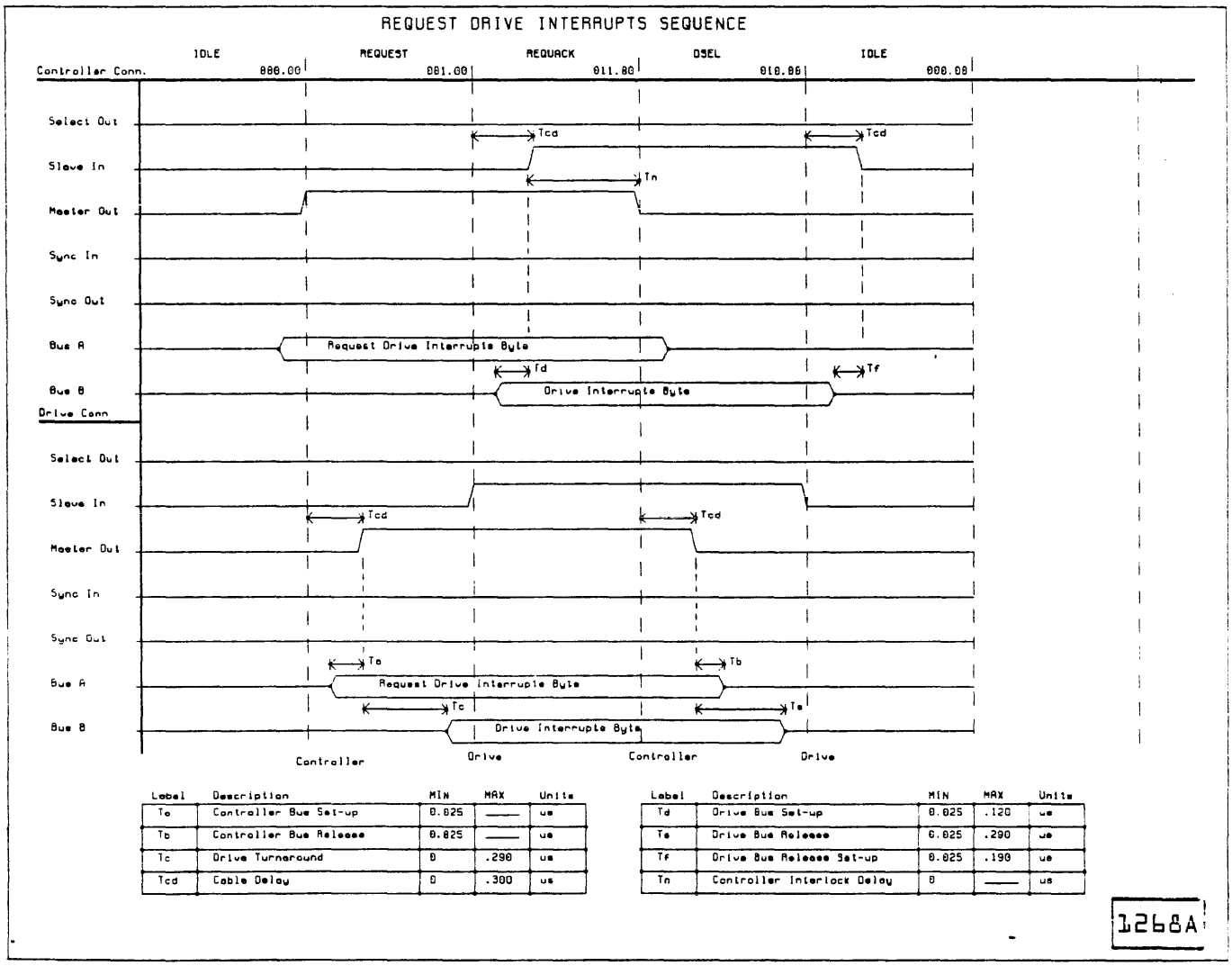


DEFINITION: XXX.XX



1267A

FIGURE 8. REQUEST DRIVE INTERRUPTS SEQUENCE

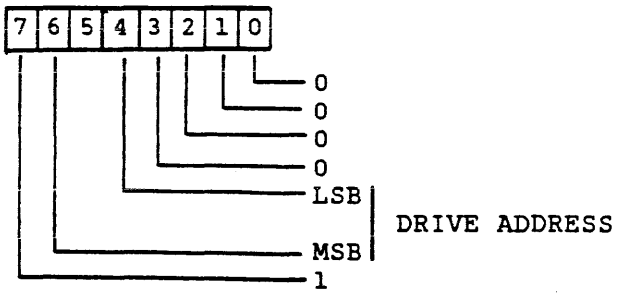


Label	Description	MIN	MAX	Units
Ta	Controller Bus Set-up	0.025	——	us
Tb	Controller Bus Release	0.025	——	us
Tc	Drive Turnaround	0	.290	us
Tcd	Cable Delay	0	.300	us

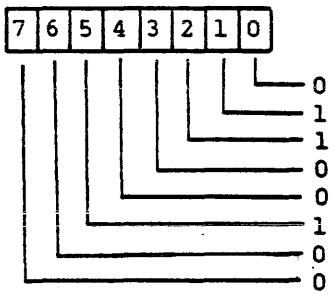
Label	Description	MIN	MAX	Units
Td	Drive Bus Set-up	0.025	.120	us
Te	Drive Bus Release	0.025	.290	us
Tf	Drive Bus Release Set-up	0.025	.190	us
Tn	Controller Interlock Delay	0	——	us

FIGURE 9. REQUEST DRIVE INTERRUPTS TIMING

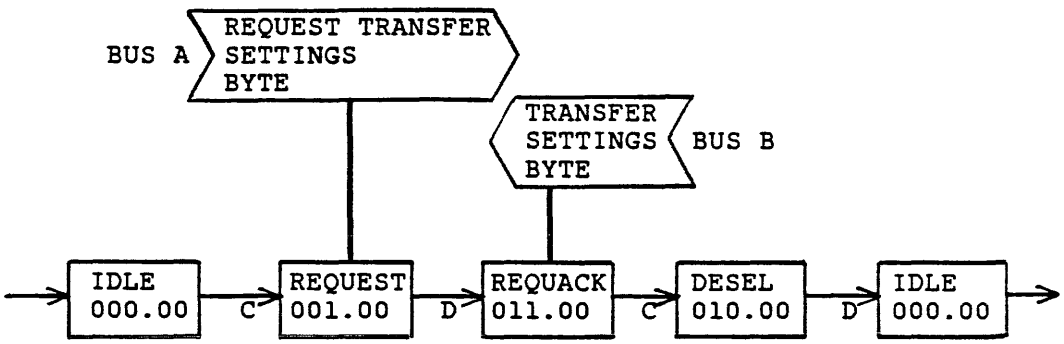
REQUEST TRANSFER SETTINGS BYTE (CONTROLLER)



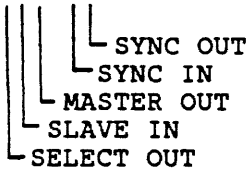
TRANSFER SETTINGS BYTE (DRIVE)



REQUEST TRANSFER SETTINGS SEQUENCE

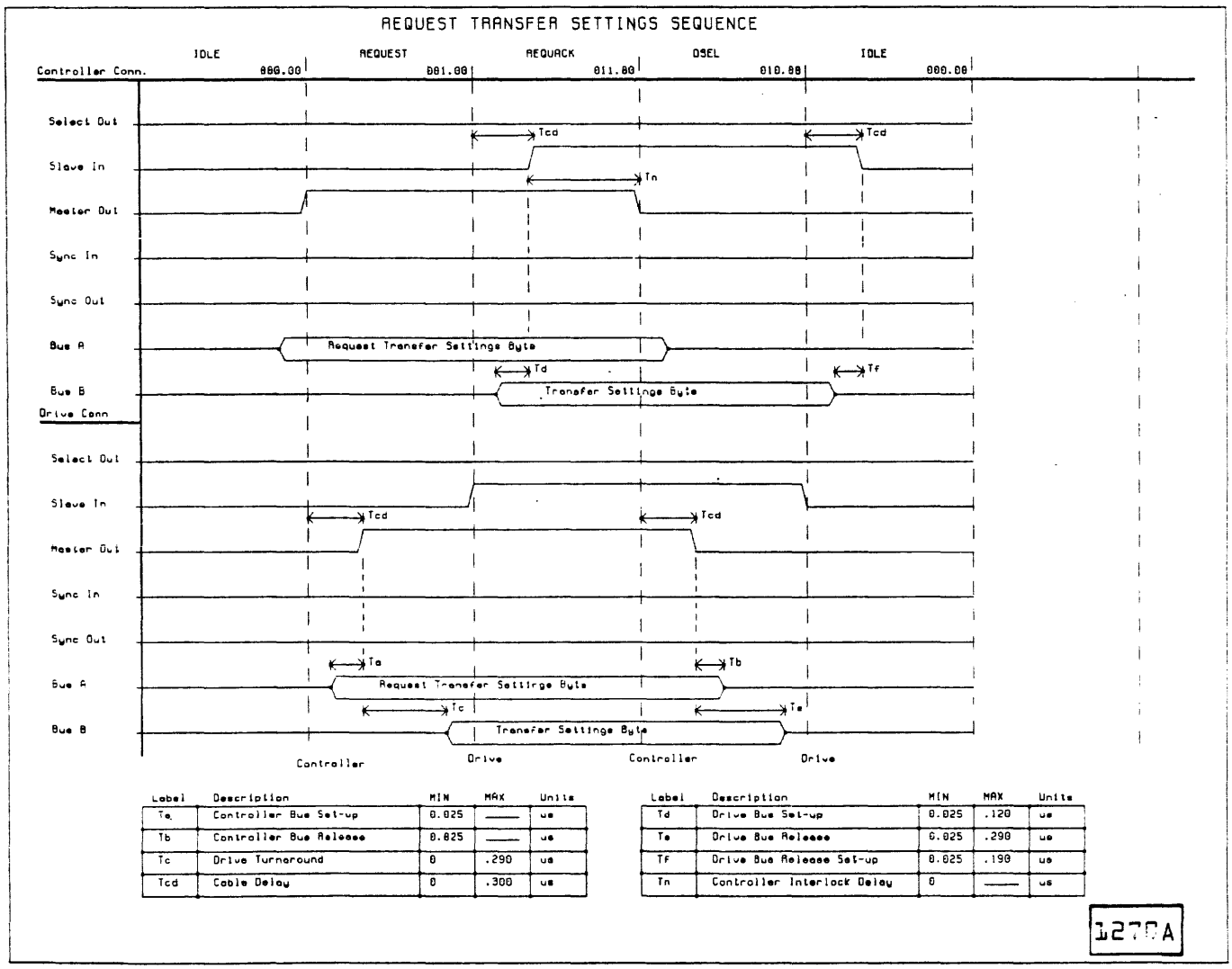


DEFINITION: XXX.XX



1269A

FIGURE 10. REQUEST TRANSFER SETTINGS SEQUENCE

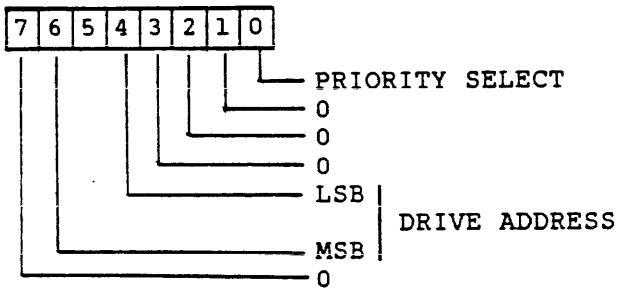


Label	Description	MIN	MAX	Units
Ta	Controller Bus Set-up	0.025	——	us
Tb	Controller Bus Release	0.025	——	us
Tc	Drive Turnaround	0	.290	us
Tcd	Cable Delay	0	.300	us

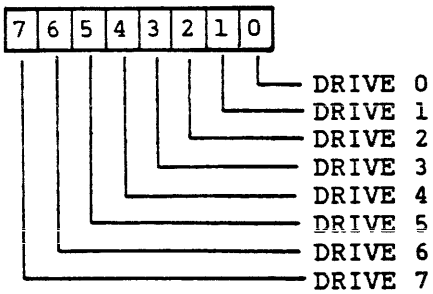
Label	Description	MIN	MAX	Units
Td	Drive Bus Set-up	0.025	.120	us
Te	Drive Bus Release	0.025	.290	us
TF	Drive Bus Release Set-up	0.025	.190	us
Tn	Controller Interlock Delay	0	——	us

FIGURE 11. REQUEST TRANSFER SETTINGS TIMING

SELECTION BYTE
(CONTROLLER)



RADIAL SELECT ADDRESS
(DRIVE)



SELECTION SEQUENCE

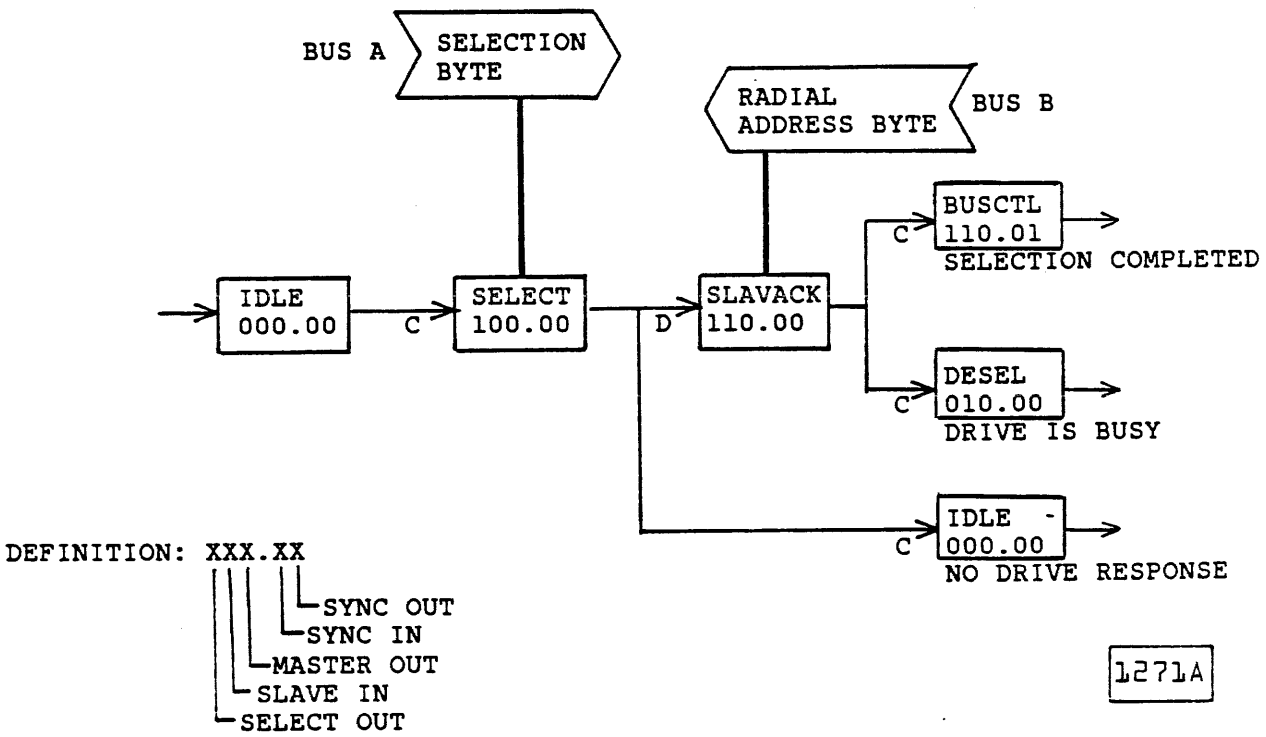
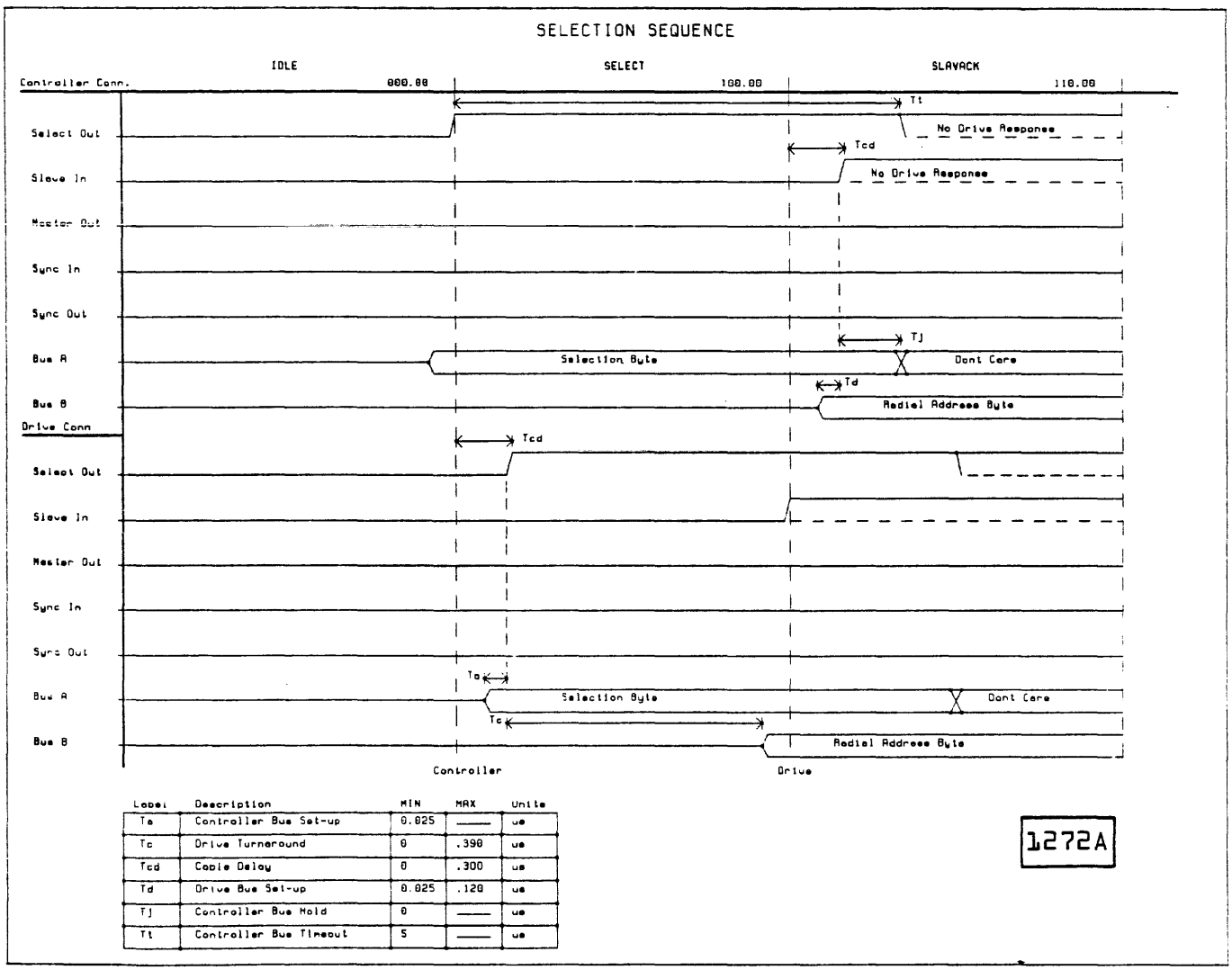


FIGURE 12. SELECTION SEQUENCE



Label	Description	MIN	MAX	Units
Ta	Controller Bus Set-up	0.025	——	us
Tc	Drive Turnaround	0	.390	us
Tcd	Cable Delay	0	.300	us
Td	Drive Bus Set-up	0.025	.120	us
TJ	Controller Bus Hold	0	——	us
Tt	Controller Bus Timeout	5	——	us

1272A

FIGURE 13. SELECTION TIMING

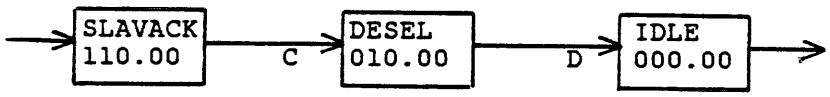
BUS A
(BUS A IS NOT DEFINED FOR THE DESELECTION SEQUENCE)

7	6	5	4	3	2	1	0

BUS B
(BUS B IS NOT DEFINED FOR THE DESELECTION SEQUENCE)

7	6	5	4	3	2	1	0

DESELECTION SEQUENCE

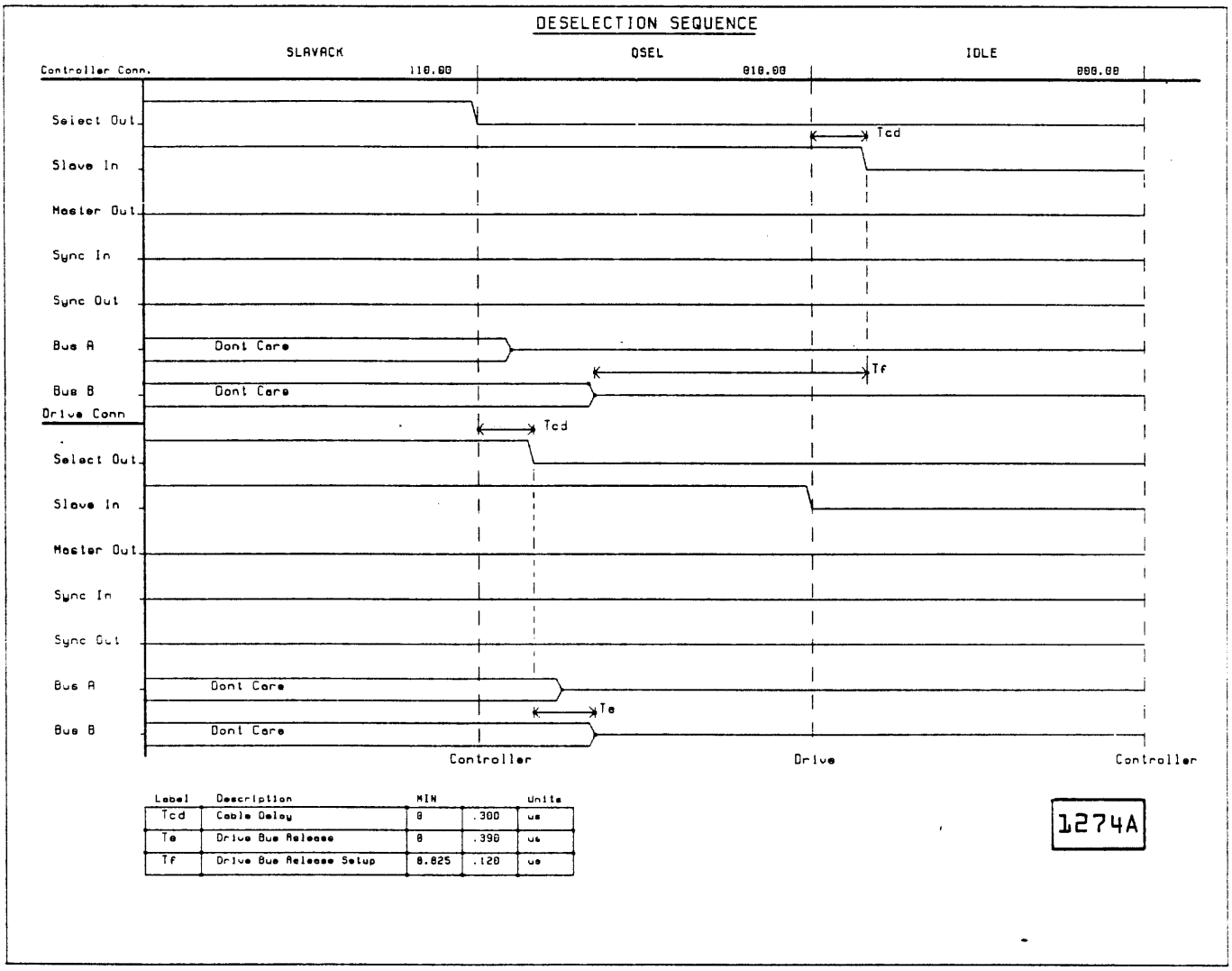


DEFINITION: XXX.XX

- SYNC OUT
- SYNC IN
- MASTER OUT
- SLAVE IN
- SELECT OUT

1273A

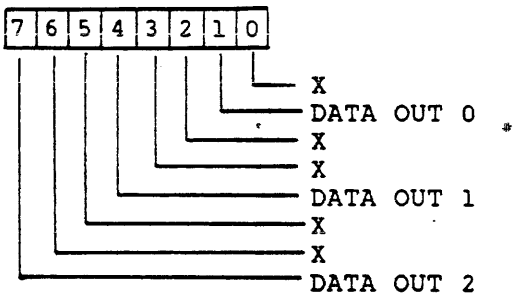
FIGURE 14. DESELECTION SEQUENCE



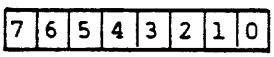
Label	Description	MIN		Units
Tcd	Cable Delay	0	.300	us
Te	Drive Bus Release	0	.390	us
Tf	Drive Bus Release Setup	0.825	.120	us

FIGURE 15. DESELECTION TIMING

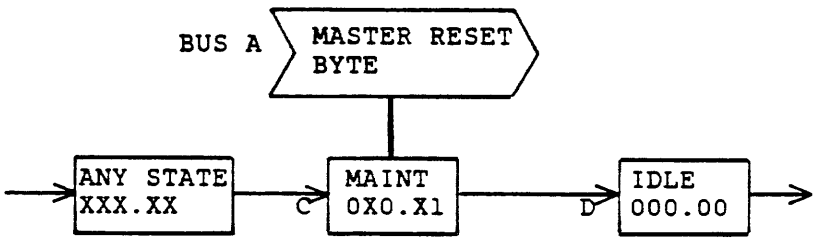
BUS A
MASTER RESET BYTE
(CONTROLLER)



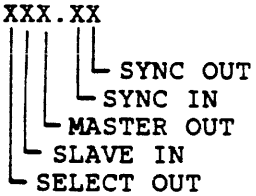
BUS B
(THERE IS NO BUS B
RESPONSE TO A
MASTER RESET)



MASTER RESET SEQUENCE



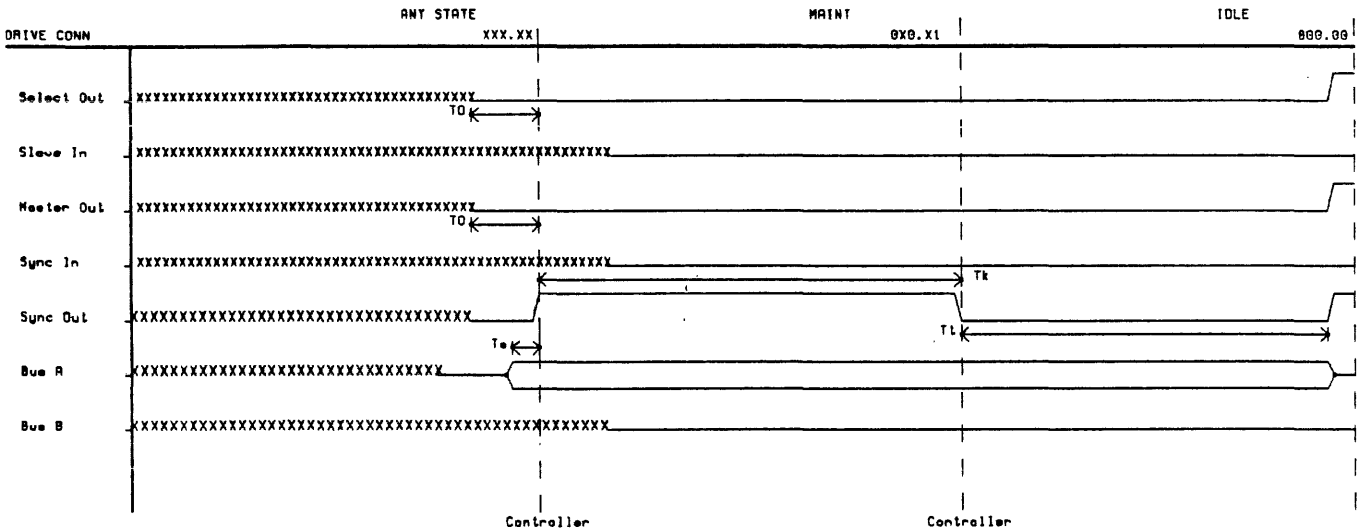
DEFINITION: XXX.XX



12758

FIGURE 16. MASTER RESET SEQUENCE

MASTER RESET SEQUENCE

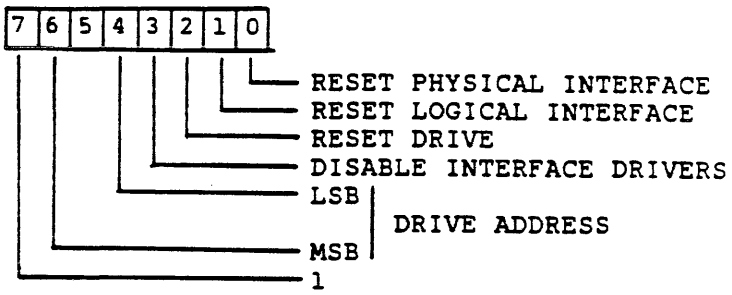


Label	Description	min	Max	Units
Te	Controller Bus Set-up	0.025	—	us
Tk	SYNC OUT pulse width for MAINT	6	—	us
Tl	IDLE following MAINT	6	—	us
TO	RELEASE OUT SIGNALS	1	—	us

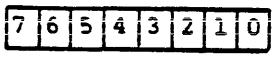
1276A

FIGURE 17. MASTER RESET TIMING

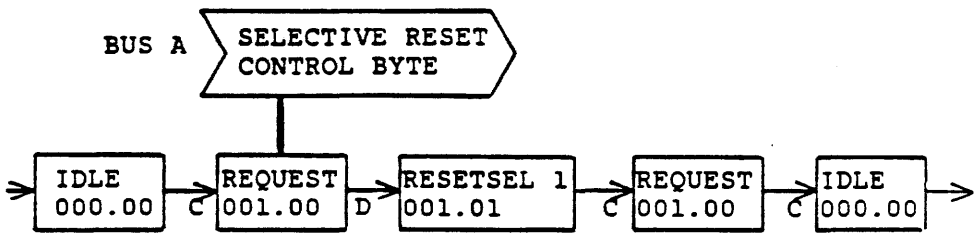
SELECTIVE RESET CONTROL BYTE (CONTROLLER)



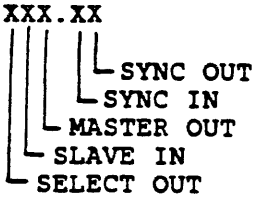
THERE IS NO BUS B RESPONSE TO A SELECTIVE RESET



SELECTIVE RESET SEQUENCE



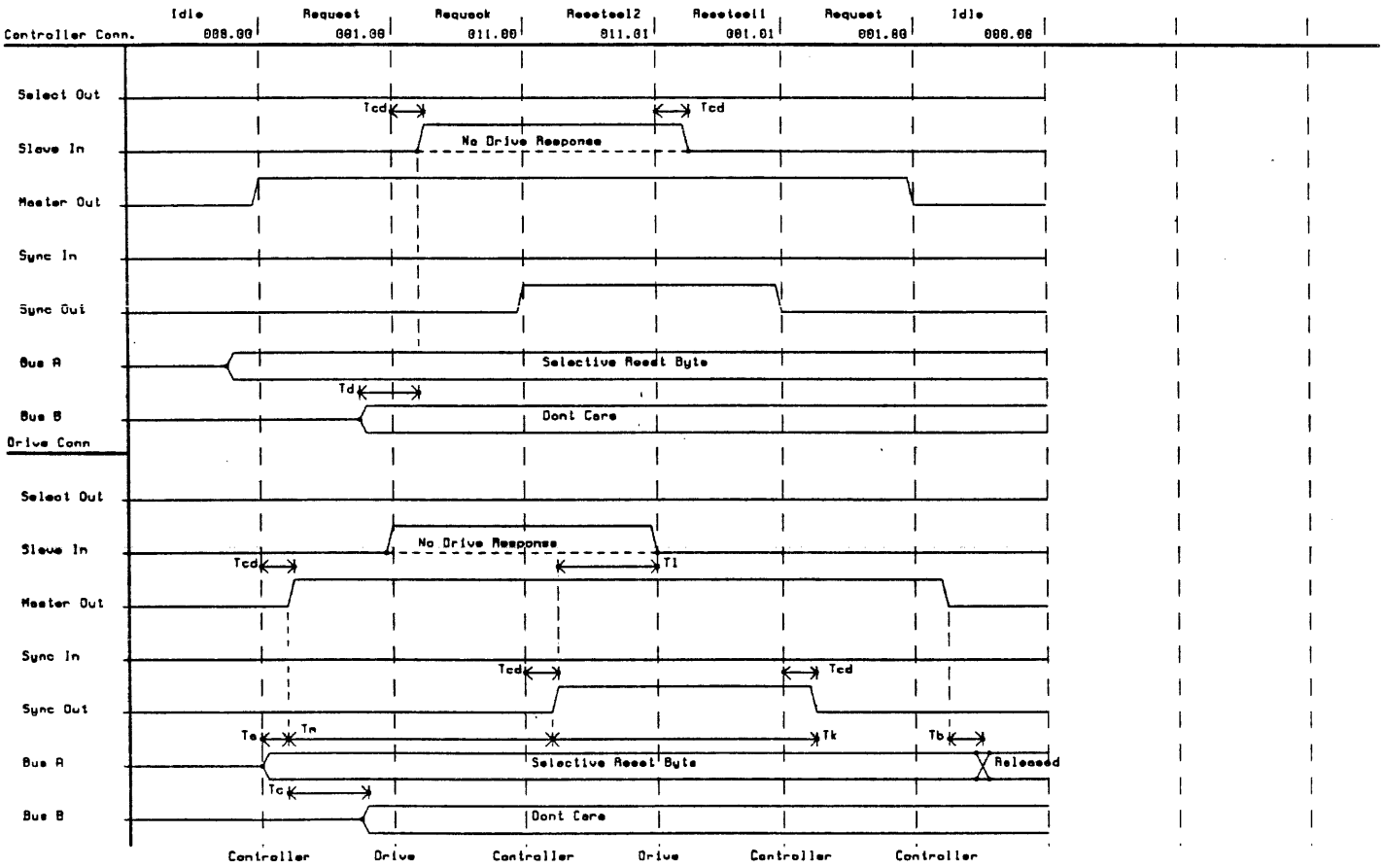
DEFINITION: XXX.XX



12778

FIGURE 18. SELECTIVE RESET SEQUENCE

SELECTIVE RESET SEQUENCE



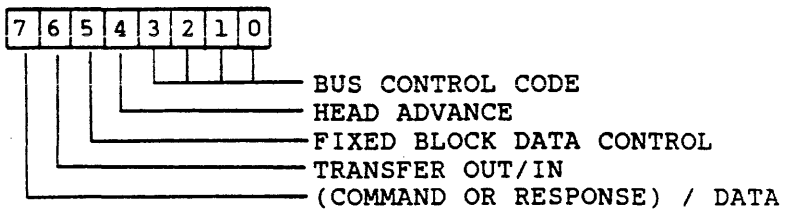
Label	Description	Min	Max	Units
Ta	Controller Bus Set-up	0.025	——	us
Tb	Cont. Bus Release From Master Out	0.025	——	us
Tc	Drive Turnaround	0	.290	us
Tcd	Cable Delay	0	.300	us

Label	Description	min	Max	Units
Td	Drive Bus Set-up	0.025	.120	us
Tk	Sync Out Pulse width For Reset	6	——	us
Tl	Drive Reset Response	2	5	us
Tm	Master Out to Sync Out Set-up	1	——	us

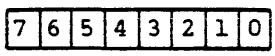
1278A

FIGURE 19. SELECTIVE RESET TIMING

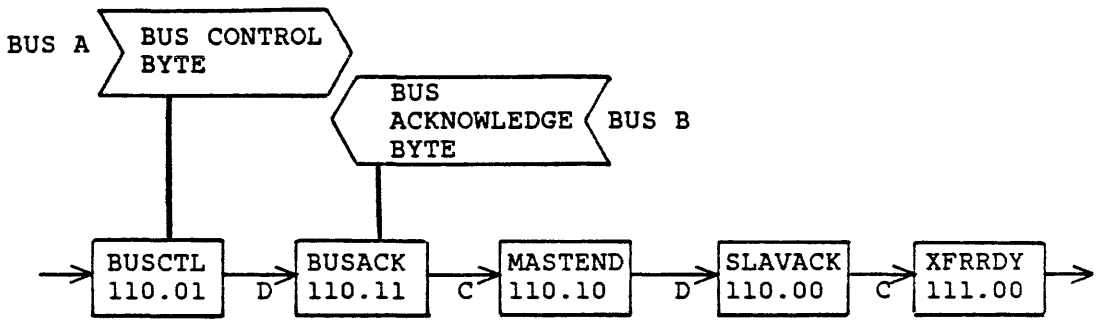
BUS CONTROL BYTE
(CONTROLLER)



BUS ACKNOWLEDGE BYTE
(DRIVE)
BUS B IS NOT DEFINED
ZEROS WILL BE RETURNED



BUS CONTROL SEQUENCE

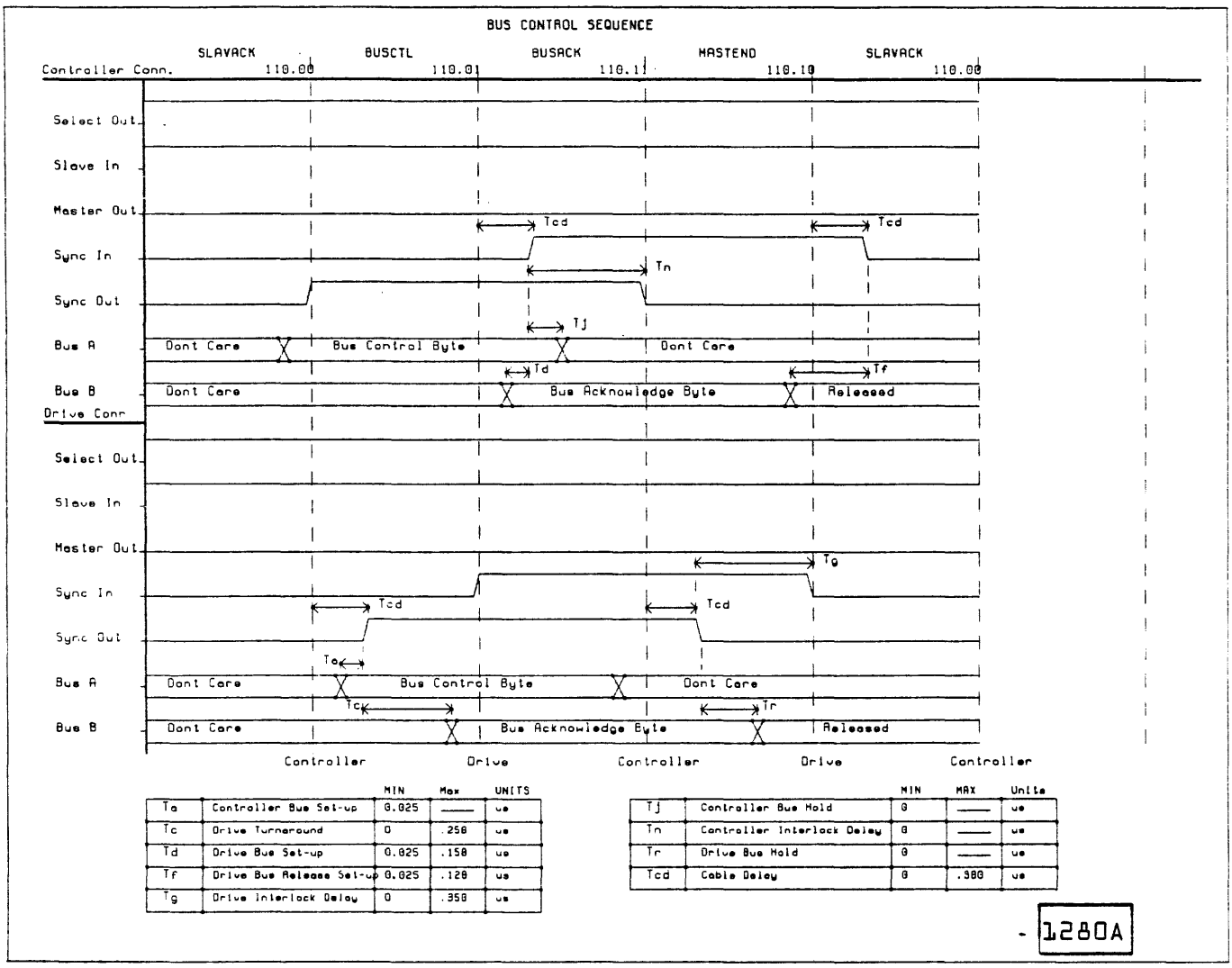


1279A

DEFINITION: XXX.XX

- SYNC OUT
- SYNC IN
- MASTER OUT
- SLAVE IN
- SELECT OUT

FIGURE 20. BUS CONTROL SEQUENCE



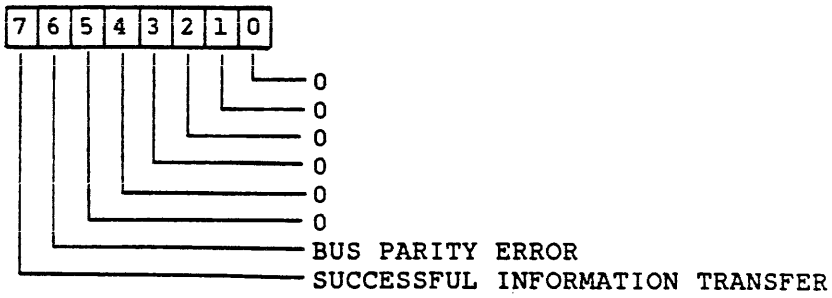
		MIN	Max	UNITS
Ta	Controller Bus Set-up	0.025	——	us
Tc	Drive Turnaround	0	.250	us
Td	Drive Bus Set-up	0.025	.150	us
Tf	Drive Bus Release Set-up	0.025	.120	us
Tg	Drive Interlock Delay	0	.350	us

		MIN	MAX	Units
Tj	Controller Bus Hold	0	——	us
Tn	Controller Interlock Delay	0	——	us
Tr	Drive Bus Hold	0	——	us
Tcd	Cable Delay	0	.380	us

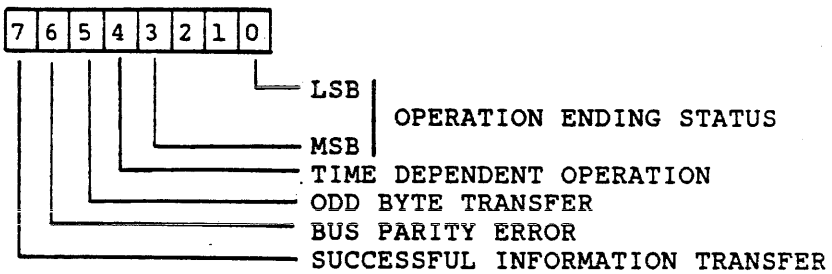
1280A

FIGURE 21. BUS CONTROL TIMING

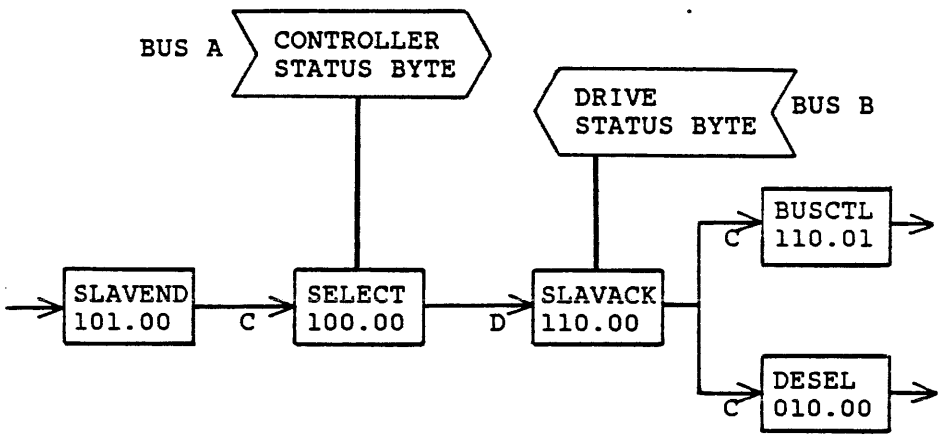
CONTROLLER STATUS BYTE
(CONTROLLER)



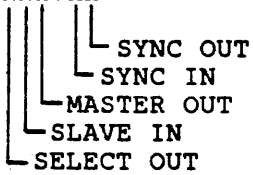
DRIVE STATUS BYTE
(DRIVE)



ENDING STATUS SEQUENCE

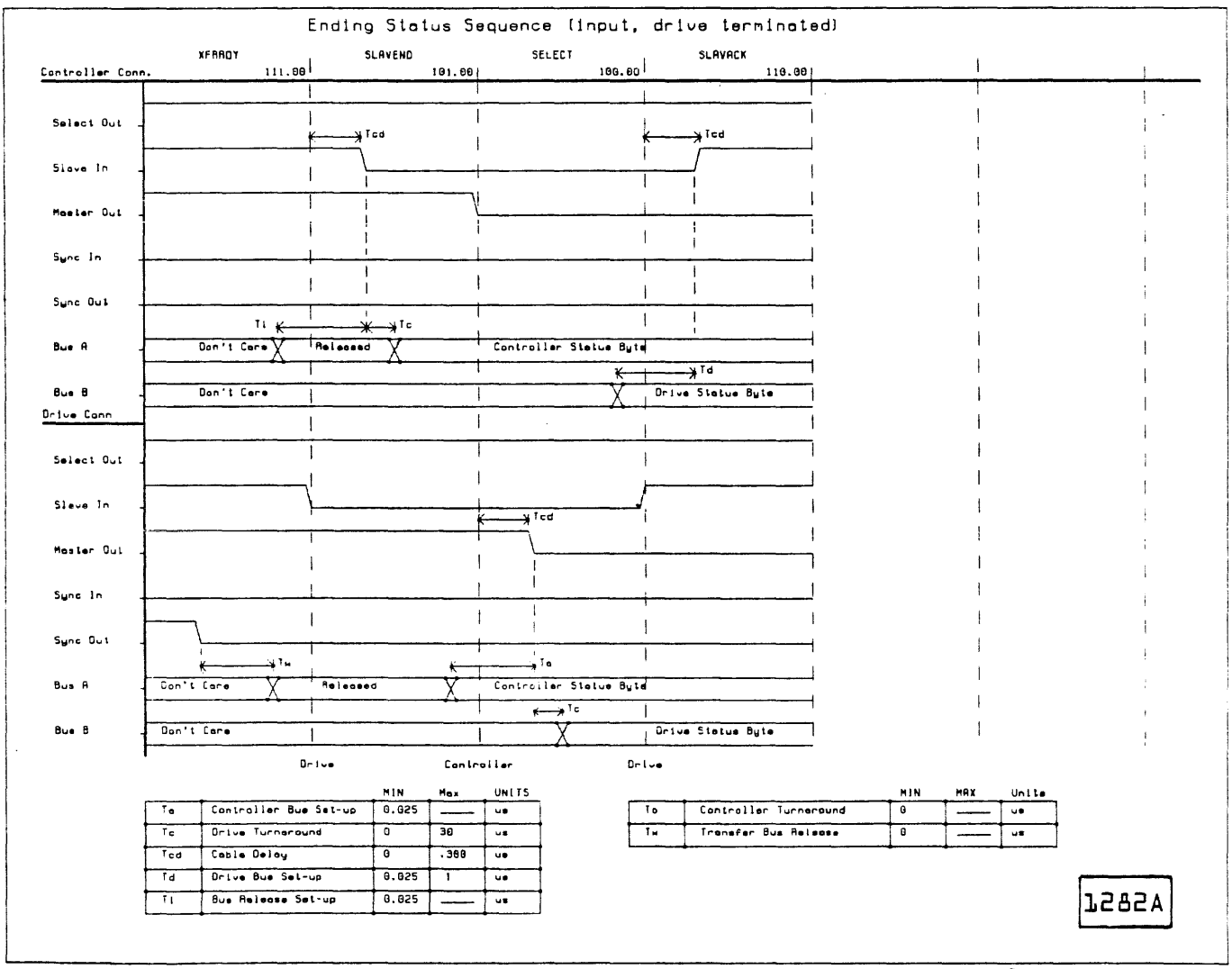


DEFINITION: XXX.XX



1281A

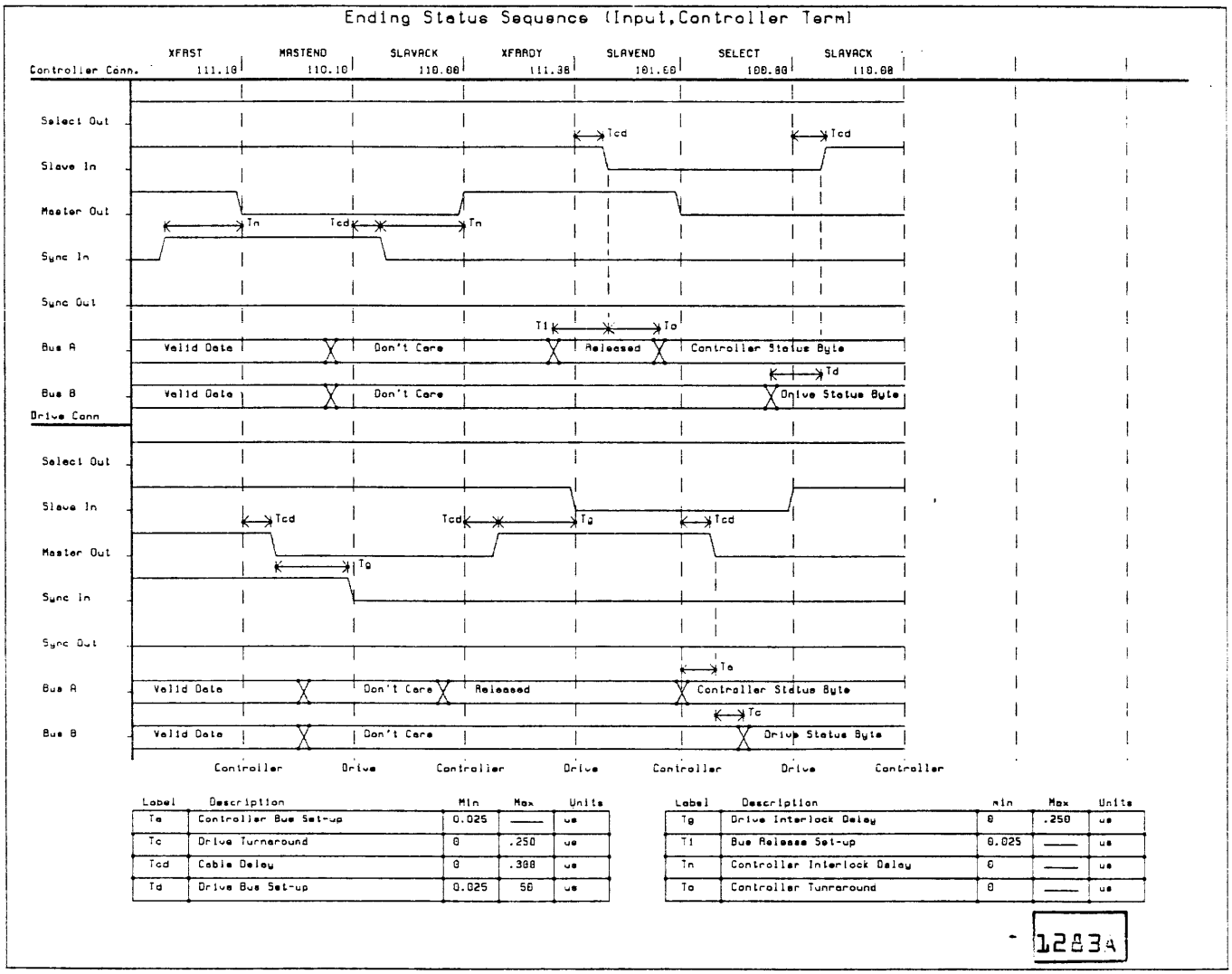
FIGURE 22. ENDING STATUS SEQUENCE



		MIN	Max	UNITS
Te	Controller Bus Set-up	0.025	——	us
Tc	Drive Turnaround	0	30	us
Tcd	Cable Delay	0	.380	us
Td	Drive Bus Set-up	0.025	1	us
Ti	Bus Release Set-up	0.025	——	us

		MIN	MAX	Units
To	Controller Turnaround	0	——	us
Tw	Transfer Bus Release	0	——	us

FIGURE 23A. ENDING STATUS TIMING (INPUT, DRIVE TERMINATED)

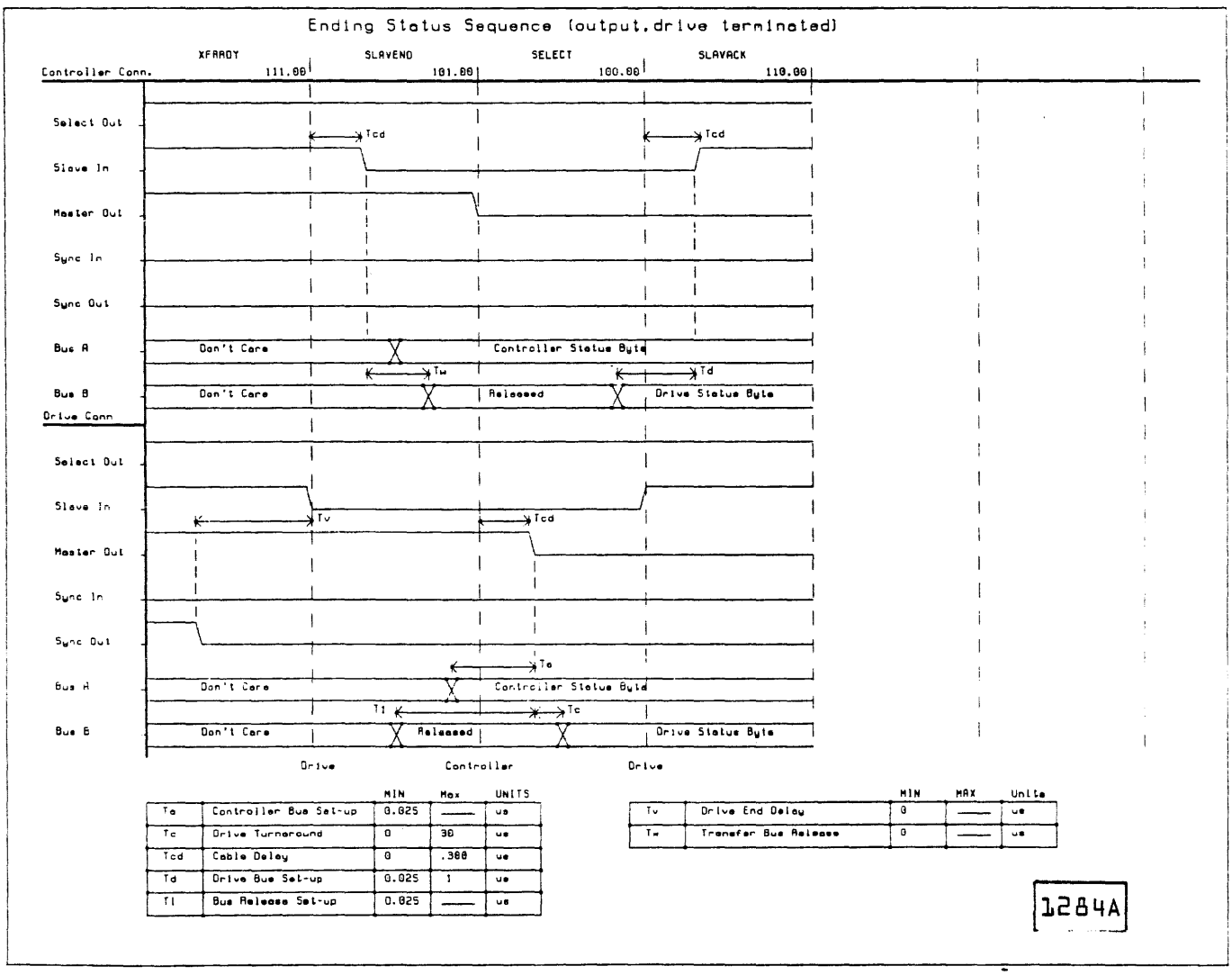


Label	Description	Min	Max	Units
Ta	Controller Bus Set-up	0.025	——	us
Tc	Drive Turnaround	0	.250	us
Tcd	Cable Delay	0	.300	us
Td	Drive Bus Set-up	0.025	50	us

Label	Description	min	Max	Units
Tg	Drive Interlock Delay	0	.250	us
Tf	Bus Release Set-up	0.025	——	us
Tn	Controller Interlock Delay	0	——	us
To	Controller Turnaround	0	——	us

1283A

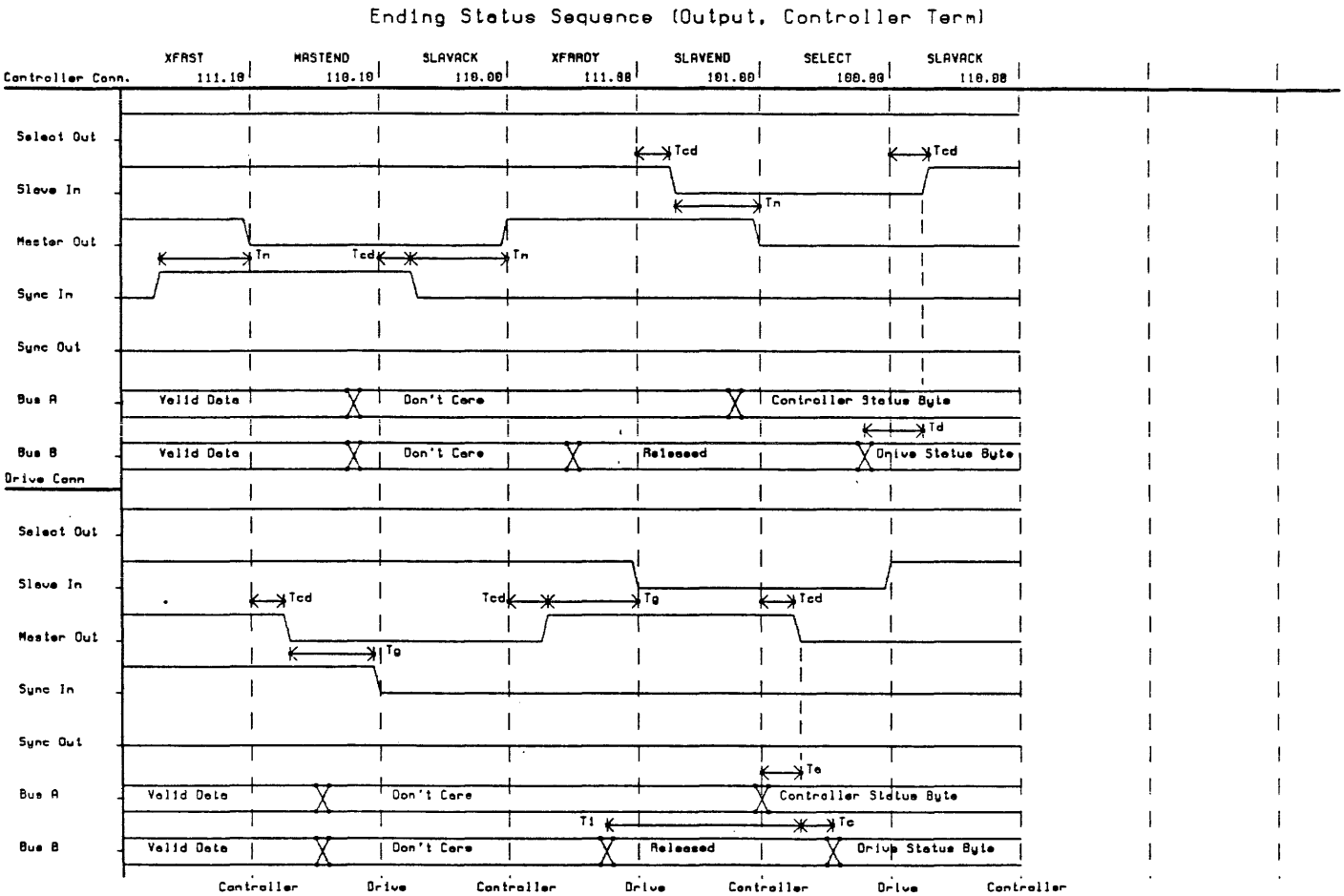
FIGURE 23B. ENDING STATUS TIMING (INPUT, CONTROLLER TERMINATED)



		MIN	Max	UNITS
Te	Controller Bus Set-up	0.025	——	us
Tc	Drive Turnaround	0	30	us
Tcd	Cable Delay	0	.380	us
Td	Drive Bus Set-up	0.025	1	us
Tl	Bus Release Set-up	0.025	——	us

		MIN	MAX	Units
Tv	Drive End Delay	0	——	us
Tw	Transfer Bus Release	0	——	us

FIGURE 23C. ENDING STATUS TIMING (OUTPUT, DRIVE TERMINATED)



Label	Description	Min	Max	Units
Te	Controller Bus Set-up	0.025	———	us
To	Drive Turnaround	0	.250	us
Tcd	Cable Delay	0	.300	us
Td	Drive Bus Set-up	0.025	50	us

Label	Description	min	Max	Units
Tg	Drive Interlock Delay	0	.250	us
Ti	Bus Release Set-up	0.025	———	us
Tn	Controller Interlock Delay	0	———	us

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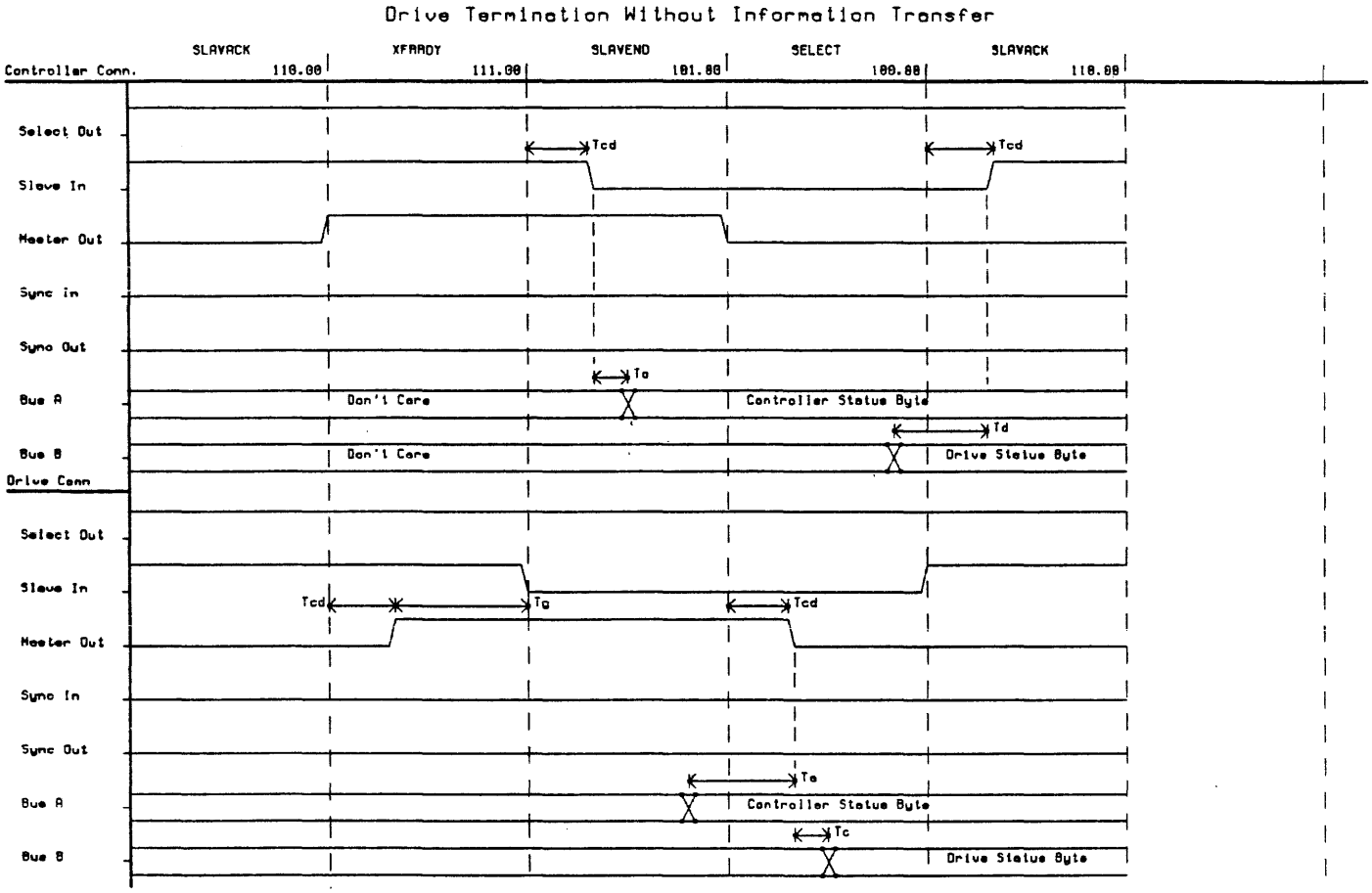
FIGURE 23D. ENDING STATUS TIMING (OUTPUT, CONTROLLER TERMINATED)



Label		MIN	MAX	Units
Ta	Controller Bus Set-up	0.025	——	us
Tc	Drive Turnaround	0	.250	us
Tcd	Cable Delay	0	.300	us

Label		MIN	MAX	Units
Td	Drive Bus Set-up	0.025	50	us
Tg	Drive Interlock Delay	0	.250	us
To	Controller Turnaround	0	——	us

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FIGURE 23E. ENDING STATUS WITHOUT INFORMATION TRANSFER TIMING

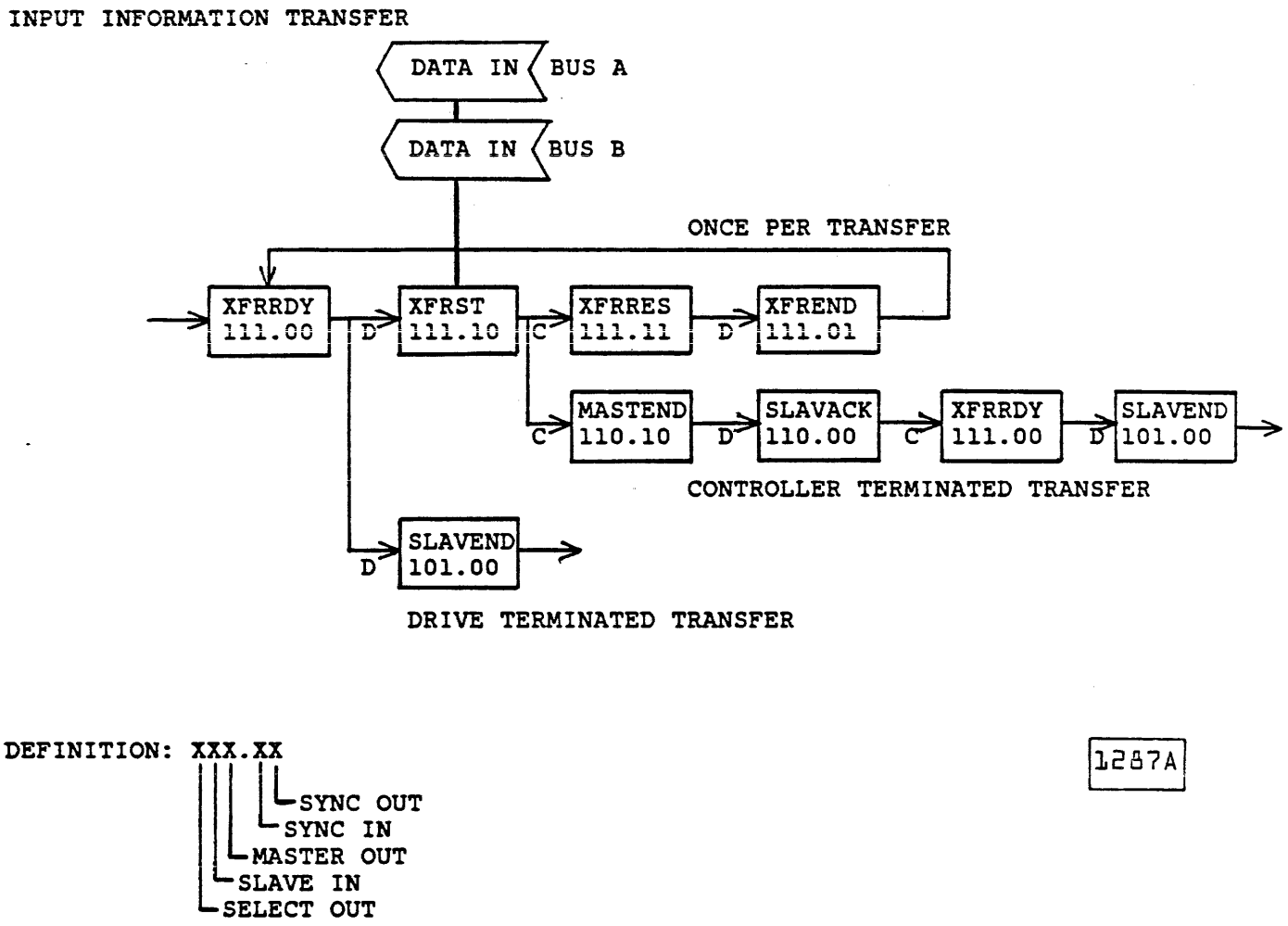
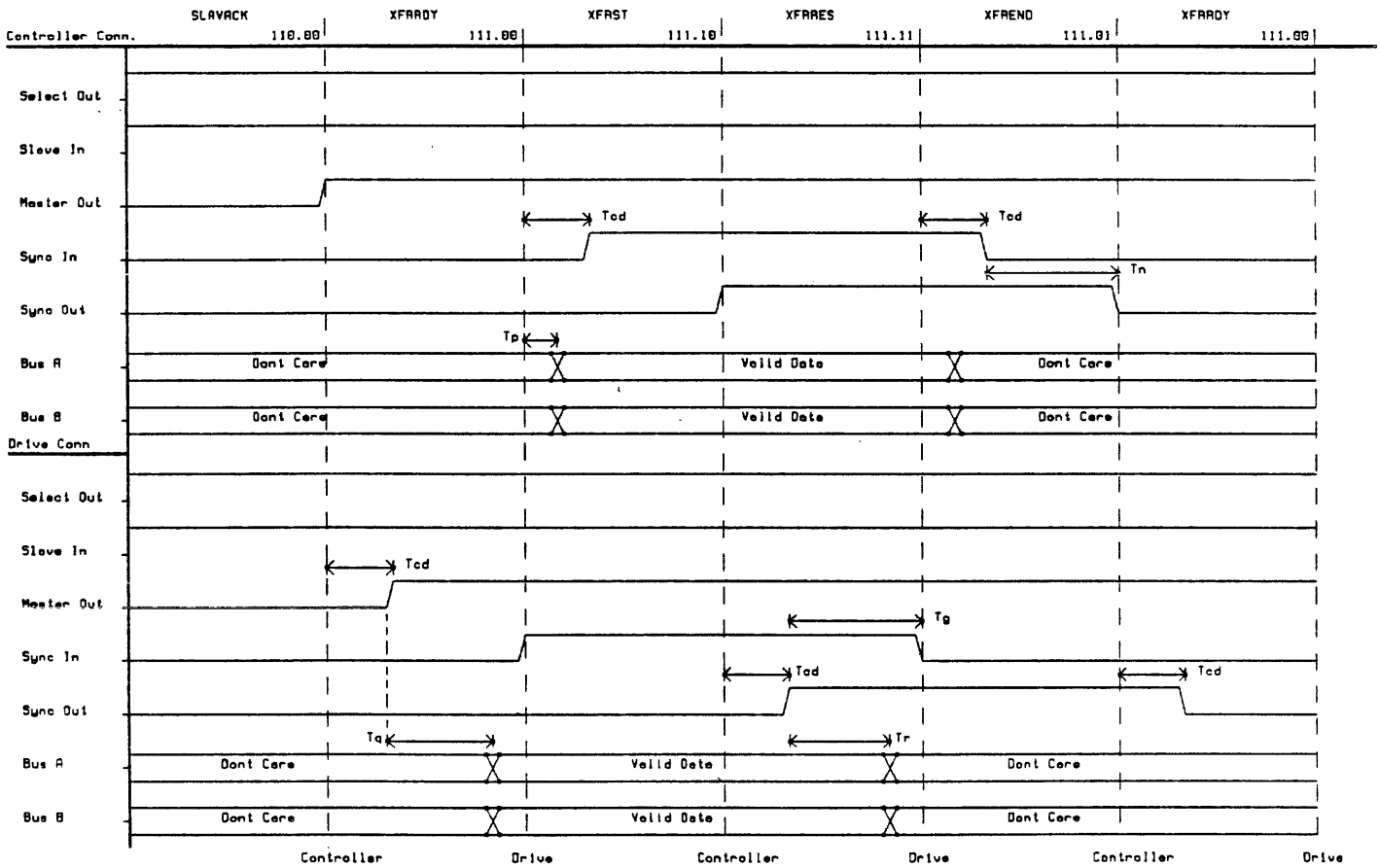


FIGURE 24. INPUT INFORMATION TRANSFER SEQUENCE

INTERLOCKED INPUT SEQUENCE



		Min	Max	Units
Tcd	Cable Delay	0	.300	us
Tg	Drive Interlock Delay	0	.250	us
Tn	Controller Interlock Delay	0	____	us
Tp	Drive Data Set-up	0.025	____	us
Tq	Drive Data Turnaround	0	____	us
Tr	Drive Bus Hold	0	____	us

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FIGURE 25. INTERLOCKED INPUT TIMING

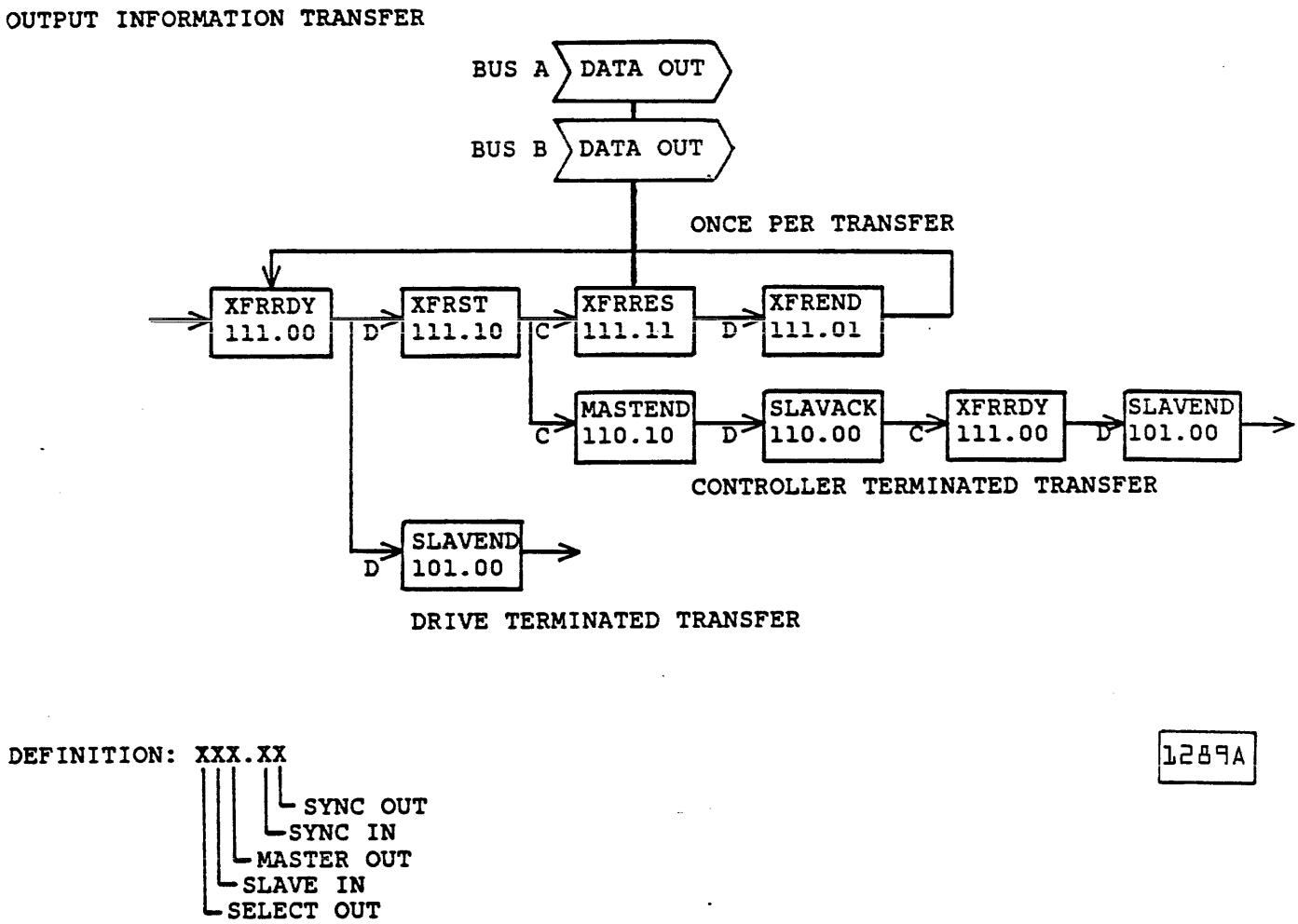
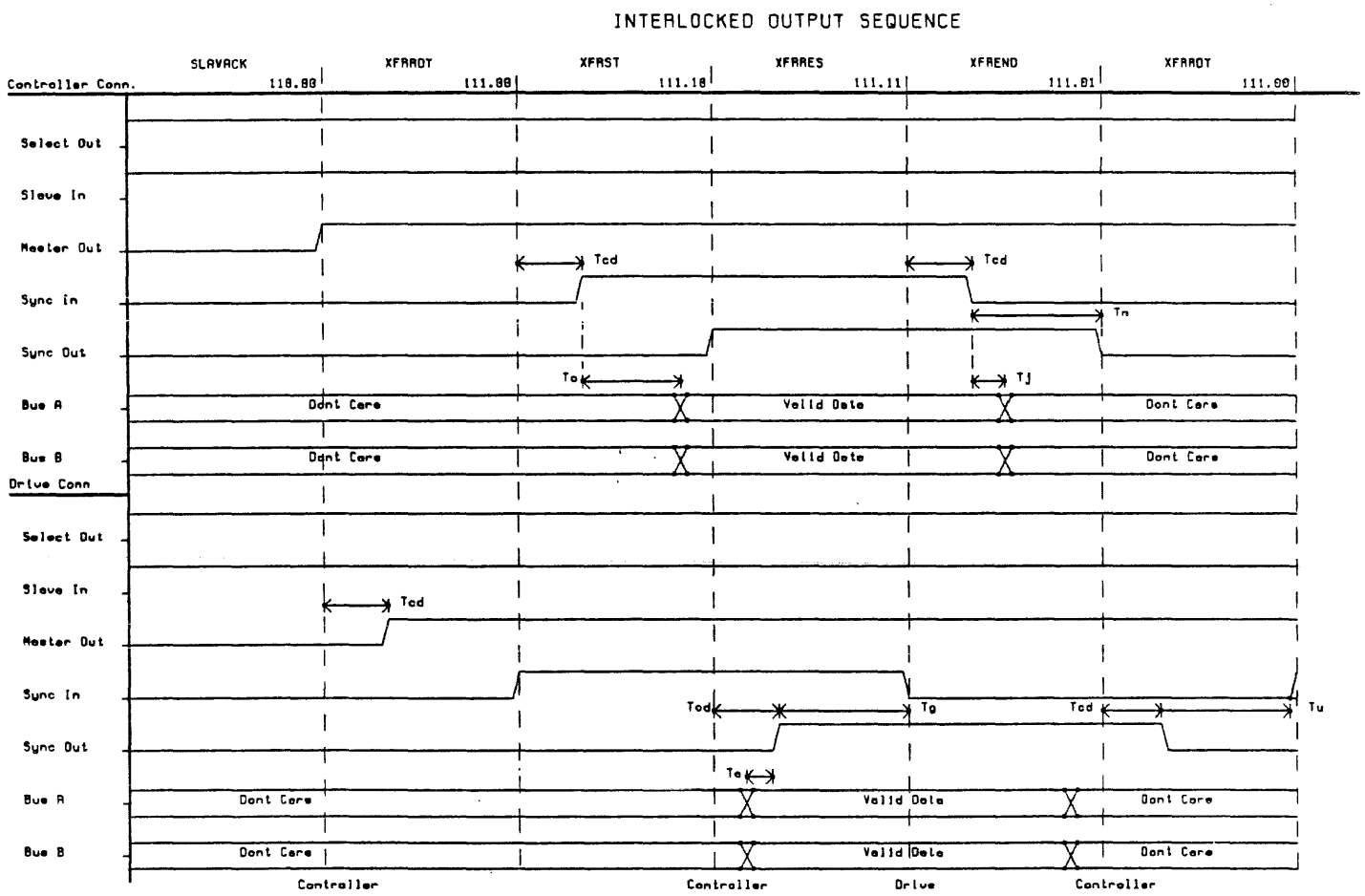


FIGURE 26. OUTPUT INFORMATION TRANSFER SEQUENCE



Label	Description	Min	Max	Units
Ta	Controller Bus Set-up	0.025	——	us
Tcd	Cable Delay	0	.300	us
Tg	Drive Interlock Delay	0	.250	us
T1	Drive Bus Release Set-up	0.025	——	us
TJ	Controller Bus Hold	0	——	us

		Min	Max	Units
Tn	Controller Interlock Delay	0	——	us
To	Controller Turnaround	0	——	us
Tu	Drive SYNC IN Delay	0	——	us
Tw	Drive Transfer Bus Release	0	——	us

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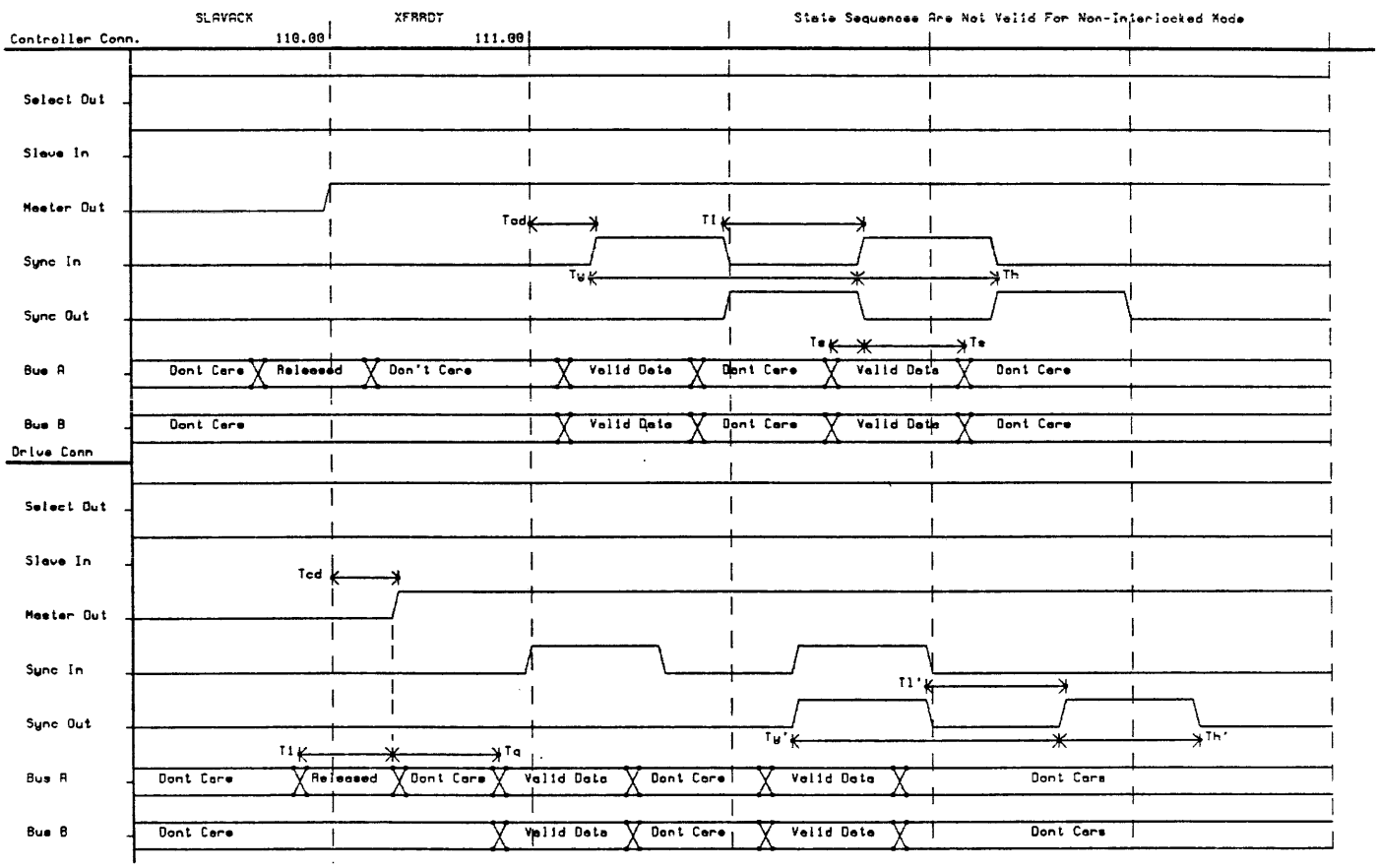
FIGURE 27. INTERLOCKED OUTPUT TIMING

Non-Interlocked Input Sequence



Label	Description	Min	Max	Units
Tcd	Cable Delay	0	.300	us
Th	SYNC IN pulse active	note 2		us
Th'	Sync Out Pulse Active	note 3		us
TI	Bus Release Setup	0.825	——	us
TI	Sync In Pulse Inactive	note 2		us
TI'	Sync Out Pulse Inactive	note 3		us

Label	Description	Min	Max	Units
Te	Set-up/Hold	.830	——	us
Tq	Drive Data Turnaround	0	——	us
Ty	SYNC IN Period	note 1		us
Ty'	SYNC OUT Period	note 1		us

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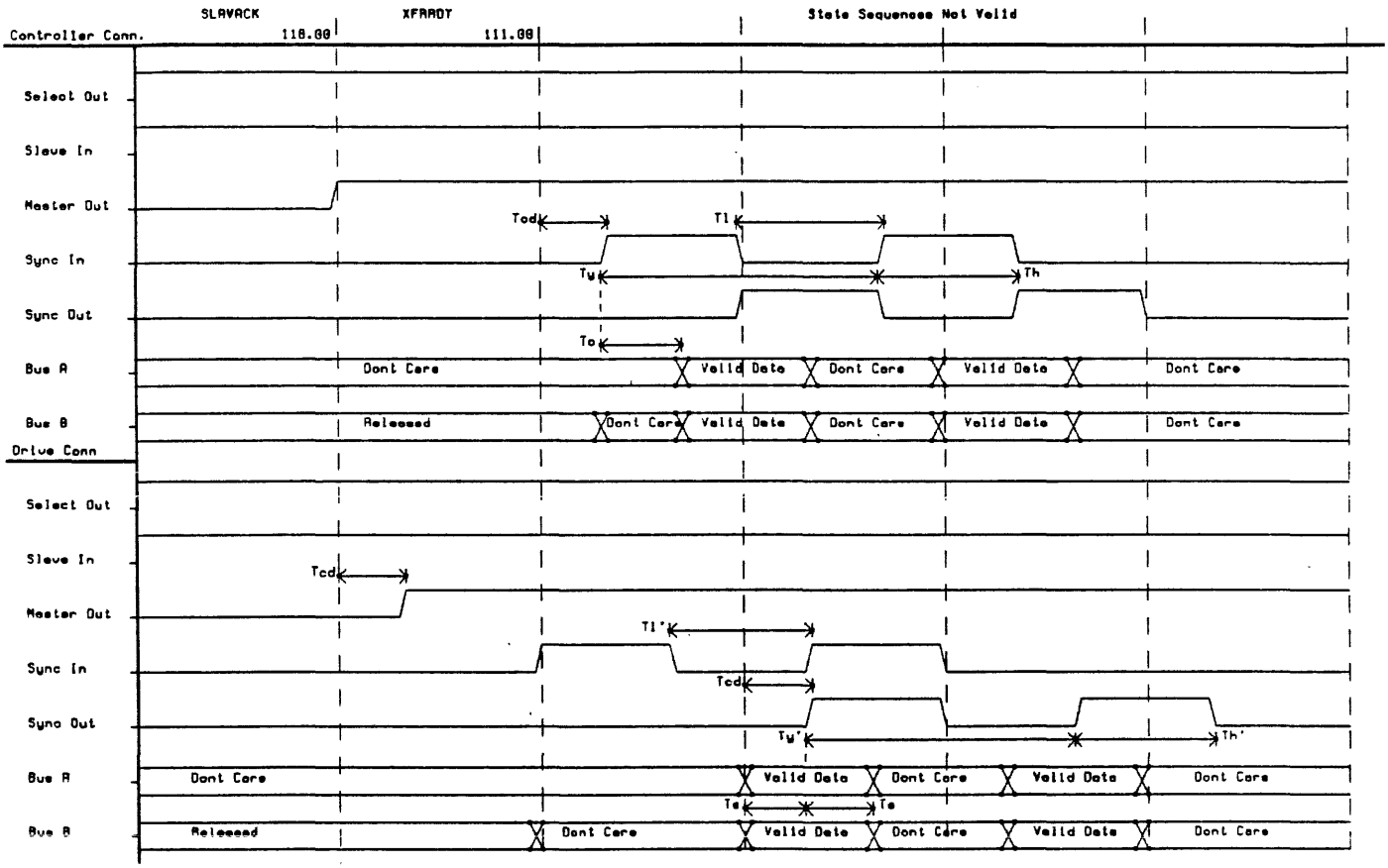
FIGURE 28. NON-INTERLOCKED INPUT TIMING

Non-Interlocked Output Sequence



Label	Description	Min	Max	Units
Tod	Cable Delay	0	.300	us
Th	SYNC IN Pulse Active	note 2		us
Th'	Sync Out Pulse Active	note 3		us
Tl	Sync In Pulse Inactive	note 2		us
To	Controller Turnaround	0	——	us

Label	Description	Min	Max	Units
Te	Set-up/Hold	.030	——	us
Tl'	Sync Out Pulse Inactive	note 3		us
Ty	SYNC IN Period	note 1		us
Ty'	SYNC OUT Period	note 1		us

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NOTES:

1. The minimum and maximum Sync In and Sync Out period can be calculated by:

$$\frac{16}{\text{Data Rate of Drive}} - \frac{16}{\text{Data Rate of Drive}} \times \text{Spindle Motor Tolerance}$$

2. The Sync In Active/Inactive times can be calculated by:

$$\frac{1.6}{\text{Sync In Period}}$$

3. The Sync Out Active/Inactive times can be calculated by:

0.8 X Sync In Active/Inactive

FIGURE 29. NON-INTERLOCKED OUTPUT TIMING

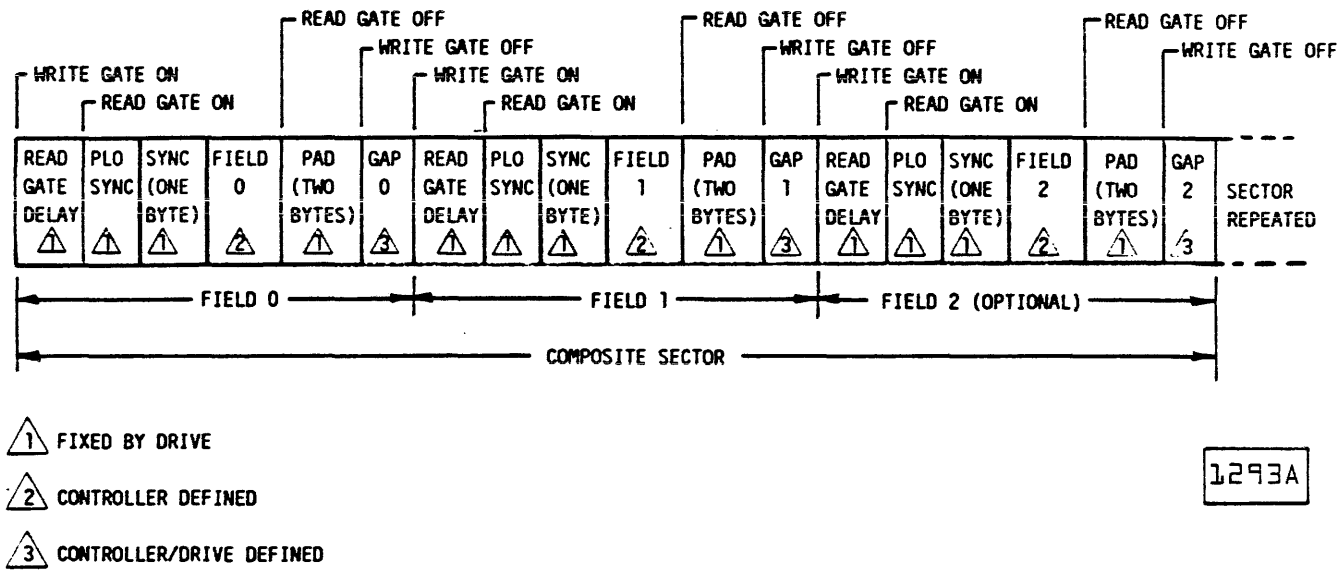
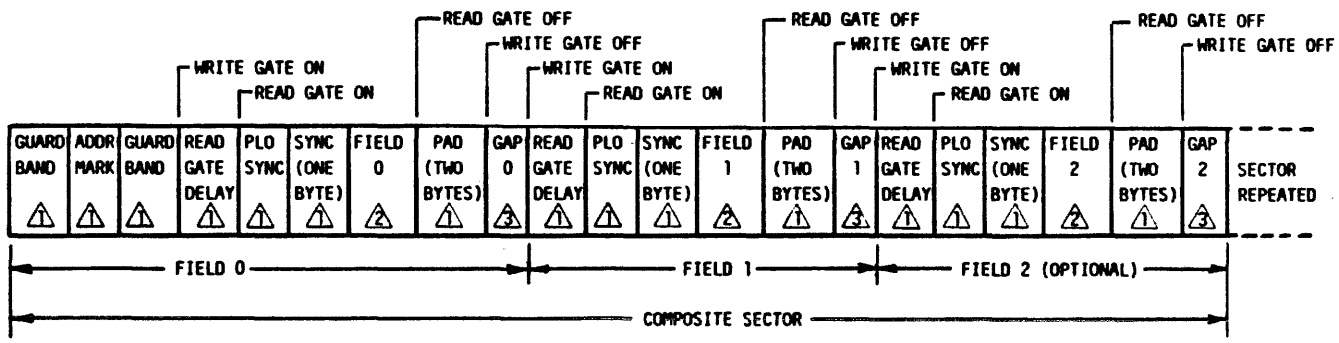


FIGURE 30. HARD SECTOR DISK FORMAT



1 FIXED BY DRIVE

2 CONTROLLER DEFINED

3 CONTROLLER/DRIVE DEFINED

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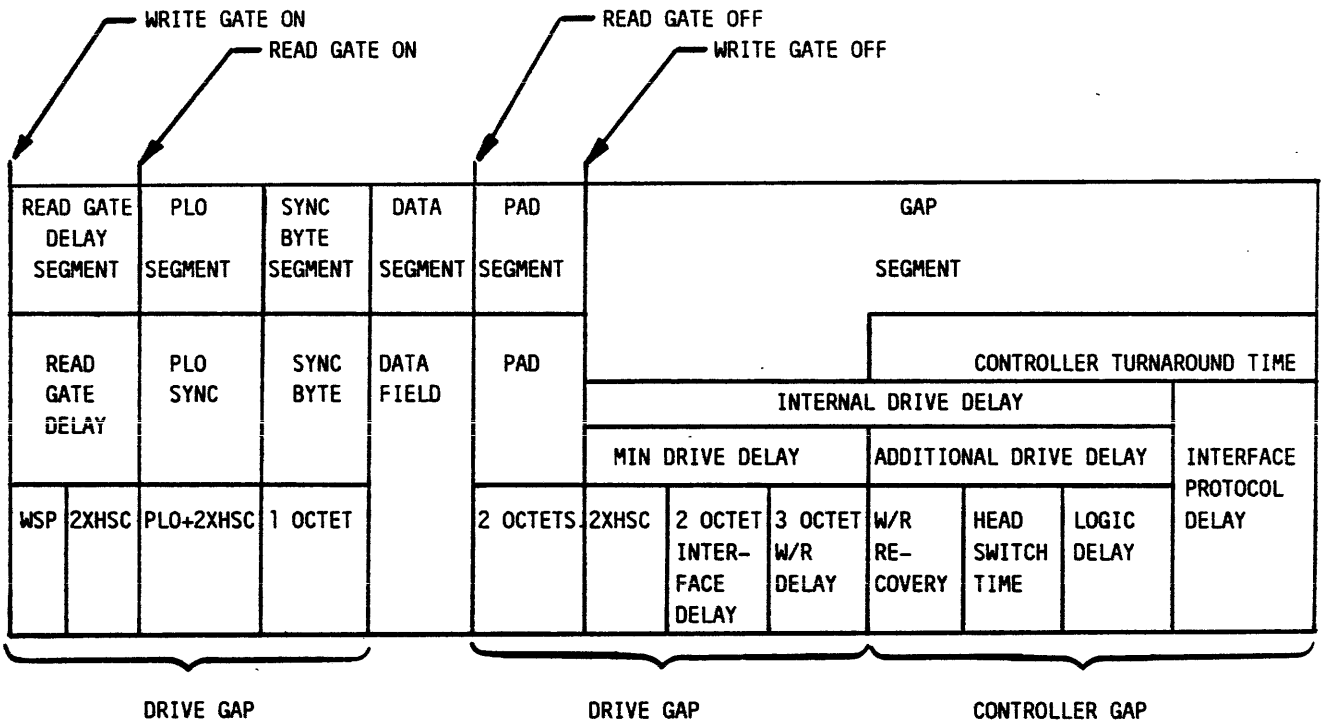
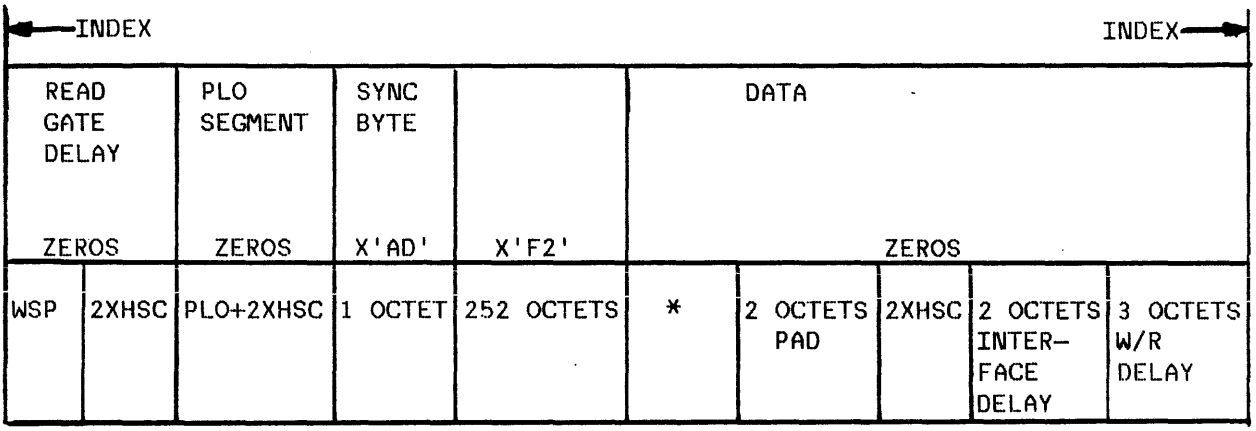
FIGURE 31. SOFT SECTOR DISK FORMAT



WSP = WRITE SPLICE (IN OCTETS)
HSC = HEAD SCATTER (IN OCTETS)
PLO = MINIMUM PLO SYNC TIME (IN OCTETS)

FIGURE 32. FIELD COMPONENTS



WSP = WRITE SPLICE (IN OCTETS)
HSC = HEAD SCATTER (IN OCTETS)

* = NUMBER OF OCTETS PER TRACK-(READ GATE DELAY+PLO SEGMENT+ SYNC BYTE LENGTH+252+PAD+2XHSC+INTERFACE DELAY+W/R DELAY). THE NUMBER OF OCTETS PER TRACK IS OBTAINED BY READING THE DRIVE CONFIGURATION RESPONSE

FIGURE 33. DIAGNOSTIC TRACK FORMAT

TABLE 1. SIGNAL NOMENCLATURE

VOLTAGE LEVEL	SIGNAL CONDITION	LOGICAL TRANSITION	LOGICAL CONDITION		
High	Active	Assert	1	one	set
Low	Inactive	Negate	0	zero	reset
Released *	Inactive	Degate	Z	high imped-ence	float

* Tri-state Condition

TABLE 2. ACCESSORY ITEMS

DESCRIPTION	QUANTITY REQUIRED	NOTES	PART NUMBER
Cable (shielded)	One per port	1,2,3	153868XX
Terminator Assembly	One per port on end drive of daisy chain.	1	15458851

NOTES:

1. In systems using the dual port feature, twice the number of cables and terminators are required.
2. See Table 3 for I/O cable lengths.
3. See Figure 1

TABLE 3. I/O CABLE LENGTHS AND TABS

CABLE LENGTH IN FEET	10	25	50	75	100	150				
CABLE TABS 153868XX	54	55	56	57	58	59				

TABLE 4. I/O PIN ASSIGNMENTS

SIGNAL NAME	SIGNAL SOURCE	ROUND CABLE SIGNAL PIN (+),(-)
DC GROUND	----------	1,34
ATTENTION IN	DRIVE	20, 4
SYNC OUT	CONTROLLER	41,25
SLAVE IN	DRIVE	39,23
SYNC IN	DRIVE	15,48
MASTER OUT	CONTROLLER	45,29
SELECT OUT	CONTROLLER	43,27
BUS B - BIT 0	DRIVE(CONTROLLER)	32,16
1	DRIVE(CONTROLLER)	49,33
2	DRIVE(CONTROLLER)	3,36
3	DRIVE(CONTROLLER)	7,40
4	DRIVE(CONTROLLER)	24, 8
5	DRIVE(CONTROLLER)	9,42
6	DRIVE(CONTROLLER)	18, 2
7	DRIVE(CONTROLLER)	35,19
BUS B - PARITY	DRIVE(CONTROLLER)	17,50
BUS A - BIT 0	CONTROLLER(DRIVE)	13,46
1	CONTROLLER(DRIVE)	30,14
2	CONTROLLER(DRIVE)	22, 6
3	CONTROLLER(DRIVE)	26,10
4	CONTROLLER(DRIVE)	11,44
5	CONTROLLER(DRIVE)	28,12
6	CONTROLLER(DRIVE)	37,21
7	CONTROLLER(DRIVE)	5,38
BUS A - PARITY	CONTROLLER(DRIVE)	47,31

NOTE: The outer shield of the 50 conductor shielded cable is to be tied to the drive frame via the connector.

TABLE 5. OCTET MODE DEFINITION

	BUS A	BUS B
MSB	Octet 0	Octet 1
	Octet 2	Octet 3
	Octet 4	Octet 5
LSB	Octet n	Octet n+1

Example: Load Position Command (07)

Load zeros	00
Cylinder	317
Head	07
RPS Target	24

	BUS A	BUS B
MSB	00	00
	03	17
	00	07
LSB	00	24

TABLE 6. STATUS RESPONSE BLOCK

	7	6	5	4	3	2	1	0
EXCEPTION STATUS	STATUS RESPONSE	UNSOILICITED EXCEPTION	BUS CNTL EXCEPTION	READ FAULT	WRITE FAULT	SEEK FAULT	SPINDLE FAULT	EXECUTION FAULT
UNSOLICITED EXCEPTIONS	RESET COMPLETE	ALTER PORT PRIOR SEL	ALTER PORT FMT CHG	ALTER PORT FMT CMPLT	RESERVED	NOT READY TRANSITION	READY TRANSITION	MEDIA CHANGE
BUS CONTROL EXCEPTIONS	INVALID BUS CNTL	INVALID PARAMETER	UNSUPPORTED BUS CNTL	BUS CNTL CONTEXT	DATA BUS CNTL LATE	RESERVED	RESERVED	RESERVED
DRIVE EXCEPTIONS	SPEED FAULT	OFF CYL FAULT	HEAD SEL FAULT	RESERVED	RESERVED	VOLTAGE FAULT	LOGIC TEMP FAULT	RESERVED
DRIVE EXCEPTIONS	WRITE PROT FAULT	RESERVED	WRITE TRANS FAULT	HEAD OFFSET FAULT	DATA STROBE FAULT	RESERVED	RESERVED	RESERVED
DRIVE EXCEPTIONS	DIAG STAT VALID	DIAG TEST INCOMPLETE	W/R DIAG TEST DISABLE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
DRIVE EXCEPTIONS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
DRIVE EXCEPTIONS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

TABLE 7. EXTENDED STATUS BLOCK

	7	6	5	4	3	2	1	0
INTERFACE FLAGS	EXTENDED STATUS	PORT NUMBER	ALTER PORT ENABLED	RESERVE ACTIVE	CMD CMPT INT EBLD	RPS INT EBLD	STAT PEND INT EBLD	FMT SPEC PRESENT
DATA RECV FLAGS	OFFSET DIRECTION	OFFSET MSB	OFFSET LSB	EARLY STROBE	LATE STROBE	RESERVED	HEADER ECC ENABLED	DATA ECC ENABLED
DRIVE CNTL FLAGS	WRITE PROTECTED	SPINDLE POWER ON	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
DRIVE STATUS	SPEED	ON CYLINDER	RESERVED	RESERVED	RESERVED	RESERVED	HDA READY	MEDIA PRESENT
DRIVE ALARMS	RESERVED	RESERVED	ILLEGAL HD SELECTED	RESERVED	RESERVED	VOLTAGED RANGE ERROR	LOGIC OVER TEMP	RESERVED
VENDOR DEFINED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
VENDOR DEFINED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
VENDOR DEFINED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

APPENDIX A

CONTROLLER TURNAROUND DELAY CONSIDERATIONS

A1.0 SCOPE

This appendix gives an illustration of the calculations of gap sizes involved in controller turnaround delay (see 9.2.1.9).

A2.0 Introduction

The Controller Turnaround Delay is the time, measured in bytes, required by the controller between fields to handle the Ending Status Sequence from the previous data control to initiate another. The actual Gap used by the drive is the Controller Turnaround increased to account for internal drive delays.

To calculate the Gap sizes of Figures 30 and 31, it is necessary to break the Gap Segment into two components (1)the Interface Protocol Delay and (2)the internal drive data delay.

A2.1 Interface Protocol Delay

The Interface Protocol Delay is the time required to execute the Ending Status Sequence and the Bus Control Sequence between Data Controls. See Figures 20 and 22. These Sequences consist of the following state transitions:

XFRRDY → SLAVEND → SELECT → SLAVACK → BUSCTL → BUSACK → MASTEND → SLAVACK → XFRRDY

From the timing diagrams, the Interface Protocol Delay can be defined as follows:

$$\text{Interface Protocol Delay} = 8T_{cd} + 4T_{cnt} + 2T'_{drv} + 2T_{drv}$$

Where:

T_{cd} = (cable delay x cable length) + transceiver delays

T_{cnt} = Controller Turnaround Time

T'_{drv} = Drive Turnaround Time when a byte is output on the bus

T_{drv} = Drive Turnaround Time

For IPI-2 drives:

transceiver delay = 59 ns max
cable delay = 1.9 ns/ft max
T_{drv} = 250 ns
T'_{drv} = 350 ns

A2.2 Internal Drive Data Delays (Figure 32)

The drive inserts a minimum gap for each field to prevent the write splice following the Pad Segment from drifting forward into the next field. The minimum Gap size is:

Gap Segment (min) = (2 x Head Scatter) + (2 Byte interface delay)
+ (3 Byte R/W circuit delay)

The following considerations must also be taken into account:

1. If a Data Control is to be executed between fields, the controller must insert the following value to account for internal drive logic delays:

   logic delay = 3.1 microseconds

2. If a Write type Data Bus Control is to be executed followed by a Read type Data Bus Control, the controller must account for the Write-to-Read Recovery time in the Controller Turnaround Delay. The value of the drives Write-to-Read Recovery time can be determined by issuing the Read Configuration Response.

3. If a head switch is to take place between fields, the controller must account for the head switch time in the Controller Turnaround Delay. The value of the drives head switch time can be determined by issuing the Read Configuration Response Control.

4. If no Data Bus Controls are to be executed between fields, the Controller Turnaround Delay for that field may be zero. The drive will automatically insert a minimum Gap between the fields.

See the individual drive Product Specification for the following values:

- Head Scatter
- Write Splice Length
- Drive Data Rate
- Minimum PLO sync time
- Address Mark Length
- Guard Band Length