CYBER 170 ECS
THEORY TRAINING

STUDENT MANUAL

CONTROL DATA CORPORATION

REVISION RECORD

REVISION	DESCRIPTION
01	
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75442340

E. S. Education, MNPFAC

This manual contains all necessary Student Materials for the subject course and is to be retained by the student.

The following sections will normally be included in this manual. However, if they are not included, it is because they have not been developed at this time.

- Course and Learning Objectives - The Course Objectives identify student performance, and the Learning Objectives identify the steps needed to accomplish the Course Objectives.
- Course Chart - This is a layout of the course on a daily basis, and can be used by the student in planning his time in the course.

  Handouts - These are normally drawings that are used for clarification or to provide supplementary information.
- Workbook - This is assigned by the instructor either as homework or work to be done in the lab while waiting for machine time. The workbook is not assigned as "Busy Work," but is an integral part of the course.
- Student Lab Manual - This is used by the student as a guide in the lab. There may be projects to perform, questions to answer or reading assignments to complete, and like the workbook this is another important element of the course and should be completed in a timely manner.

CONTENTS

ECS Theory Training

Terminal and Enabling Objectives

The Terminal Objectives for this course have been written to reflect job orientated tasks namely Preventative Maintenance and Emergency Maintenance. Each terminal objective contains a note for clarification.

The Enabling Objectives that are common to all the Terminal Objectives and that identify background material are numbered E.O. 0.X.

The remaining Enabling Objectives support the individual Terminal Objective, the first number identifies the Terminal Objective for example E.O. 1.X, the 1 identifies Terminal Objective 1.

The criteria for evaluating the Enabling Objective will be a score of 70% accuracy on daily quizzes unless stated otherwise.

The procedure taught for troubleshooting the ECS system employs modular substitution. This implies both modules and packs depending on the logic packaging. During modular substitution the original location should always contain the original logic (module/pack).

E.O. 0.1 GIVEN: Cyber 173/175 System Block Diagrams (HO 5A and 5)

THE STUDENT WILL: List the purpose and relationship of the following on a CYBER 17X system.

a. CPU

b. CMC

c. CM

d. Coupler

e. Controller

f. Bay

g. DDP

E.O. 0.2 GIVEN: Course handouts # HO-5 through HO-5A and Reference Manual #60430000 and student written notes.

THE STUDENT WILL: describe in writing terms used in ECS COURSE and associated manuals to include:

a. ECS Record

b. Error Exit

c. Full Exit

d. Half Exit

e. Fake Read

f. Illegal Address

g. Bay

h. Controller Accept

i. Controller Abort

E.O. 0.3 GIVEN: ECS Instruction Format, Address Format and ECS Instruction handouts 1 through 4.

THE STUDENT WILL: List the purpose of the following;

a. fmi designator 011 and 012

b. Bj +K

c. Ao Register

d. Xo Register

e. Word Select Bits

f. Bank Bits

g. Bay Bits

h. Word group address

i. RA ECS

j. FL ECS

k. Flag Register

l. Flag Function Bits

E.O. 0.4 GIVEN: ECS Instruction Handout 4.

THE STUDENT WILL: List conditions which will cause the ECS instruction to full exit and half exit.

E.O. 0.5 GIVEN: 6640 manual # 60186000

THE STUDENT WILL: list or describe the purpose of 1/2 ECS mode in the 6640 and trace to module level address bits from the coupler to the Common Address Register in 1/2 ECS mode and normal mode. This will include the purpose of all switches at locations A01 and A04 and tracing output of switches to module level to the address path.

E.O. 0.6 GIVEN: ECS II Bay Manual # 60404700

THE STUDENT WILL: trace to a module level paths used by the ECS read and write operation in the ECS II Bay. This will include:

a. Control

b. Address

c. Data

E.O. 0.7 GIVEN: ECS Bay Manual # 60404700

THE STUDENT WILL: list the purpose of every module in the ECS II Bay.

E.O. 0.8 GIVEN: ECS II Bay Manual # 60404700

THE STUDENT WILL: List or describe the purpose and functions of the maintenance panel and describe the procedure for using maintenance module and maintenance panel.

E.O. 0.9 GIVEN: ECS SMM Diagnostic Pub. #75442330

THE STUDENT WILL: List the following for the diagnostics MCS, ECM, ECX and DDP.

a. Purpose for each

b. Loading procedure for each

c. Parameters Entries

d. Display and keyboard entries

e. Error/messages and displays

E.O. 0.10 GIVEN: Course terminal and enabling objectives.

THE STUDENT WILL: List what is expected concerning performance after completing the course.

E.O. 0.11 GIVEN: 7030-1XXECS Subsystem 6642-2 DDP Hardware Reference Manual #60430000.

THE STUDENT WILL: describe the purpose of Distributive Data Path (6642).

E.O. 0.12 GIVEN: 7030-1XXECS and 6642-2 DDP Hardware Reference Manual #60430000.

THE STUDENT WILL: List the functions and uses of function codes for the DDPII list conditions in the DDP by reading status response codes and write short programs that could be used for maintenance of DDP.

E.O. 0.13 GIVEN: Block diagrams handouts HO-80 through HO-87.

THE STUDENT WILL: describe in writing the basic system configuration of a computer system with DDP and ECS and the purpose of all major parts of the DDP logic.

E.O. 0.14 GIVEN: DDP Reference Manual #60376300.

THE STUDENT WILL: List the functions and uses of function codes for the DDP and write short programs that could be used for maintenance of DDP.

E.O. 0.15 GIVEN: DDPI Customer Engineering Manual publication #60369400.

THE STUDENT WILL: locate sections of manual needed for installation procedure and check out of DDP, theory of operation, logic diagrams, maintenance procedures and power diagrams maintenance aid and wiring and know when to use each section in maintenance.

E.O.0.16 GIVEN: DDPII Hardware Maintenance Manual publication #60425800.

THE STUDENT WILL: Locate sections of manual needed for installation data and checkout, theory of operation, logic diagrams and maintenance.

T.O. 1 GIVEN: CAMS listings and CE manuals for couplers, controllers, bays, DDPs and diagnostics. The following are the publications numbers.

Manual	Publication Number
175 Coupler	60428800
173 Coupler	19984700
6640 A/B	60186000
6640 D/E	60440500
6635	60212200
Maintenance Aids	60289200
ECS II	60404700
DDP	60369400
DDP II	60425800
SMM Manual	

THE STUDENT WILL: Perform Preventative Maintenance on ECS and associated hardware to include:

a. Couplers

b. Controllers

c. Bays

d. DDP

NOTE: Because of theory only, students have been shown procedures, but because of course prerequisites they should be able to preform the tasks. If hardware failures occur on PM this course will direct this to terminal objective T.O. 2.

CRITERIA: As per CAMS specifications.

E.O. 1.1 GIVEN: DDP manual pub. #60369400 and handouts HO-106 through HO-111.

THE STUDENT WILL: locate the Preventative Maintenance procedure and requirements for DDPI.

E.O. 1.2 GIVEN: ECSII Bay manual pub. #60404700.

THE STUDENT WILL: locate the Preventative maintenance procedure and requirements for the ECSII bay.

T.O. 2 GIVEN: ECS System Malfunction (Emergency Maintenance or Corrective Maintenance) CE Manuals for Couplers, Controllers, Bays, DDPs and diagnostics. The following are the Publication Numbers.

Manuals	Publication Number
175 Coupler	60428800
174 Coupler	19984700
6640 A/B	60186000
6640 D/E	60440500
6635	60212200
Maintenance Aids	60289200
ECS II	60404700
DDP	60369400
DDP II	60425800
SMM Manual	

THE STUDENT WILL: Isolate and repair malfunction for pack or module failures on all ECS and associated hardware to include couplers, controllers, bays and DDP.

Note: Because of theory only, students have been shown procedure for locating failing modules and stack repair and replacement procedures, but because of prerequisites for course they should be able to perform these tasks.

CRITERIA: Within a two hour time limit or call for assistance.

E.O. 2.1 GIVEN: ECS Reference Manual #60430000.

THE STUDENT WILL: list operations which will occur if an exchange jump interrupts an ECS transfer.

E.O. 2.2 GIVEN: 175 Coupler Block Diagram handout # 10.

THE STUDENT WILL: list the purpose of all registers in the 175 coupler.

E.O. 2.3 GIVEN: 175 Coupler Block Diagram handout #10, 175 Block Diagram HO-5.

THE STUDENT WILL: list the purpose of all signal exchange between the 175 coupler and the controller, 175 coupler and CPU, CPU and CMC, and coupler and CMC.

E.O. 2.4 GIVEN: 175 CPU logic handouts HO-40 through HO-43.

THE STUDENT WILL: list the purpose and trace signal flow to module level in the 175 CPU.

a. Ao + (Bj + k) - FLcm check
b. Xo + (Bj + k) - FLecs check
c. ECS coupler request
d. Bj + k to coupler
e. Xo + RA ecs to coupler
f. Exchange abort ECS
g. Ao + RA cm to CMC
h. ECS write bit
i. Force zero parity code

E.O. 2.5 GIVEN: 175 CMC logic handouts HO-44 through HO-46.

THE STUDENT WILL: list the purpose and trace signals to a module level of the following in the 175 CMC.

a. Accept to ECS Coupler
b. Data on line (go ECS)
c. CSU address parity error, coupler
d. CMC double error, coupler

e. CMC input error, coupler

f. Data and parity - SECDED

g. Address and parity

h. Go Bank

i. Go Refresh

j. Write

E.O. 2.6 GIVEN: 6640 Manual # 60186000

THE STUDENT WILL: list or describe the purpose of the following signals and major parts of the 6640. (Block Diagram)

a. Request

b. Accept to Coupler

c. Address path

d. Service Register

e. Counters

f. Flag register

g. Parity generator checker

h. Channel bit register

i. Accept logic

E.O. 2.7 GIVEN: 6635 Manual # 60212200

THE STUDENT WILL: list or describe the purpose of the following signals and major part of the 6635 Bay. (Block diagram)

a. Bank address register

b. Scan counter

c. Bank timer

d. Stack (memory)

e. Sense amp

f. Sense amp register

g. Bank data register

h. Bay data register

i. Bay address register

j. Bank bit translator

k. Store and request signals

E.O. 2.8 GIVEN: 175 Coupler logic diagram handouts 7 through 39.

THE STUDENT WILL: trace to pack level control signals, address and data thru the CPU, coupler, CMC on an ECS read and write operation of at least three ECS records. This will include listing, the contents of the following registers in the 175 coupler for each record.

a. X

b. K

c. Y

d. P

E.O. 2.9 GIVEN: 175 Coupler logic diagram handouts 7 through 39

THE STUDENT WILL: list events that cause end time to occur in the 175 Coupler and trace signals to pack level from coupler to CPU and CMC.

E.O. 2.10 GIVEN: 175 Coupler logic diagram handouts 7 through 39

THE STUDENT WILL: list the conditions that cause a fake read operation to take place and trace all signals and data to a module level to CMC. This will include all differences compared to a normal read operation.

E.O. 2.11 GIVEN: Course handout numbers HO-1 - HO-49 .

THE STUDENT WILL: list or describe the purpose of a flag operation and describe all differences from a normal data transfer operation in the 175 CPU, Coupler and CMC.

E.O. 2.12 GIVEN: ECS Instruction flow chart and 173 CPU logic diagrams handouts HO-50 - HO-52.

THE STUDENT WILL: list or describe the purpose of the ECS sequence and trace to pack level control signals in the 173 CYBER computer.

E.O. 2.13 GIVEN: Coupler diagrams manual Publication # 19984700.

THE STUDENT WILL: list or describe the purpose of the following in the 173 coupler.

a. X

b. K

c. Y

d. P

e. All signals from and to CPU

f. All signals from and to CMC

g. All signals from and to controller

E.O. 2.14 GIVEN: 173 CPU/CMC logic diagrams handouts # HO-50 - HO-56 and Coupler diagrams # 19984700

THE STUDENT WILL: trace to pack level signals, data and address for an ECS read and write operation in the CPU, Coupler, and CMC in the CYBER 173.

E.O. 2.15 GIVEN: Coupler diagrams # 19984700.

THE STUDENT WILL: list or describe the conditions that cause a fake read operation to take place and trace signals to a module level in the 173 system. This will include all differences compared to a normal read operation.

E.O. 2.16 GIVEN: 173 CPU/CMC logic diagrams handout # HO-50 - HO-55 and coupler diagrams #19984700.

THE STUDENT WILL: list or describe conditions that cause end time to occur in the 173 coupler and trace signals from coupler to CPU and CMC to pack level.

E.O. 2.17 GIVEN: Coupler diagrams #19984700.

THE STUDENT WILL: list or describe the purpose of a flag operation and trace to a pack level signals that are different from a normal read or write operation in the CPU and coupler.

E.O. 2.18 GIVEN: Coupler diagrams # 19984700.

THE STUDENT WILL: Trace all signals for a read and write operation to pack level of at least 3 ECS records in the CPU, CMC and coupler and will list contents of X, K, Y and P for each record in the coupler.

E.O. 2.19 GIVEN: 6640 manual # 60186000.

THE STUDENT WILL: trace to module level to include output and input pins the request from coupler to the accept F/F and describe all conditions needed for accept I, II and III. This will include signal flow to a module level to generate accept I, II and III.

E.O. 2.20 GIVEN: 6640 Manual # 60186000.

THE STUDENT WILL: trace to module level accept logic to:

a. Return accept to coupler

b. Advance counter assigner

c. Gate address bit to bay

d. Clear service register

e. Start counter

f. Release scanner

g. Abort logic

E.O. 2.21 GIVEN: 6640 Manual # 60186000.

THE STUDENT WILL: list the uses of counter translations and be able to trace the operation of the following to module level including input and output pins.

a. Counters and decoders

b. Address and bay selection

c. Data flow and gates

d. Channel bit register

e. Parity generator and checker

f. All signals including address and data to and from controller.

g. All signals including data to and from coupler.

E.O. 2.22 GIVEN: 6640 Manual # 60186000.

THE STUDENT WILL: trace to module level address bits to the flag register and flag logic to bring up an accept or abort signal for a flag operation.

E.O. 2.23 GIVEN: 6640 Manual # 60186000.

THE STUDENT WILL: list all conditions that an abort signal is returned to coupler and be able to trace logic to module level for these conditions.

E.O. 2.24 GIVEN: 6635 manual # 60212200.

THE STUDENT WILL: trace to module level the request from the controller and bank bits translations to the bay address register.

E.O. 2.25 GIVEN: 6635 manual # 60212200.

THE STUDENT WILL: trace to module level address bits to correct bank and signals required to start the running of the bank timer.

E.O. 2.26 GIVEN: 6635 Manual # 60212200.

THE STUDENT WILL: trace all logic to module level to bring up a complete memory cycle. This will include the following:

a. Read dummy

b. Read drive

c. Read return

d. Write dummy and write drive

e. Write return

E.O. 2.27 GIVEN: 6635 Manual # 60212200 and course handout numbers 57-62c.

THE STUDENT WILL: Describe how the memory stack is wired to include X and Y lines, diode blocks and how a read and write cycle effect the lines.

E.O. 2.28 GIVEN: 6635 Manual # 60212200, ECS Installation and Checkout Maintenance manual publication number 60289200.

THE STUDENT WILL: locate wires that need changing for degrading memory and also list the reasons for degrading the stack.

E.O. 2.29 GIVEN: ECS Installation and Checkout Maintenance manual #60289200.

THE STUDENT WILL: locate procedure for stack repair and stack maintenance and list at least 4 reasons for using the procedure.

E.O. 2.30 GIVEN: 6635 manual # 60212200.

THE STUDENT WILL: trace to module level all signals used to assemble or disassemble records for read or write data. This will include every module from memory to controller or controller to memory. The following areas are included:

a. Scan counter
b. Go bit storage
c. Sense amp
d. Sense amp register
e. Augment logic
f. Data path

E.O. 2.31 GIVEN: 6635 Manual # 60212200.

THE STUDENT WILL: locate possible bad modules for theoretical failures such as:

a. Sense amp failure
b. Augment failure
c. BB or BA module failures
d. Data failure
e. Address failures
f. Assemble or disassemble failures

E.O. 2.32 GIVEN: 6635 Manual #60212200.

THE STUDENT WILL: describe the purpose of the maintenance panel and list purposes of all switches and logic associated with the maintenance panel. This will include tracing signals and data to module level for associated logic.

E.O. 2.33 GIVEN: 6640 D/E handouts HO-64 through HO-79.

THE STUDENT WILL: trace address, address parity data, data parity, parity disable logic and error signals to a module level through the 6640. This will include only major differences in the 6640 D/E compared to 6640 A/B.

E.O. 2.34 GIVEN: 6640 D/E Manual #60440500.

THE STUDENT WILL: list the differences in 6640 D/E compared to 6640 A/B model. This will include:

a. Address parity
b. Data parity
c. Parity disable logic
d. Error signals

E.O. 2.35 GIVEN: ECSII Bay Manual #60404700.

THE STUDENT WILL: locate possible bad modules for theoretical failures such as:

a. Data failures
b. Addressing failures
c. Memory failures

E.O. 2.36 GIVEN: ECS Timing and flowchart handouts # HO-6 through HO-49.

THE STUDENT WILL: list or describe in general terms what is happening at a given time on an ECS operation. This will include both read and write transfer and should include:

a. Coupler

b. CMC and CM

c. Controller

d. Bay

E.O. 2.37 GIVEN: Theoretical failures and all course material.

THE STUDENT WILL: list general area of logic that could cause failure. This has no restrictions as to the equipment.

CRITERIA: Answering questions asked on homework and during classroom time as directed by instructor.

E.O. 2.38 GIVEN: 6640 D/E diagrams handouts HO-78 and HO-79.

THE STUDENT WILL: Trace to module level the signals for changing bank selections when controller is in degrade mode and bit 20 of address is received from coupler.

E.O. 2.39 GIVEN: ECS II Bay Manual Pub. #60404700.

THE STUDENT WILL: Describe the procedure for using spare bits on memory modules in the ECS II bay.

E.O. 2.40 GIVEN: DDP handouts HO-90 through HO-101 and DDP diagrams publication #60369400.

THE STUDENT WILL: Trace all signals, address and data paths used to read ECS using DDP in the DDPI to a module level.

E.O. 2.41 GIVEN: DDP handouts HO-90 through HO-101 and DDP diagrams publication #60369400.

THE STUDENT WILL: Trace all signals, address and data paths to a module level used to write ECS using DDP in the DDPI.

E.O. 2.42 GIVEN: DDP handouts HO-90 and HO-91 and DDP diagrams publication #60369400.

THE STUDENT WILL: Trace all signals and data paths used for functions of 5010 and 5004 in the DDP to a module level.

E.O. 2.43 GIVEN: DDP diagrams publication #60369400.

THE STUDENT WILL: Trace to module level all signals used on a flag function in the DDPI.

E.O. 2.44 GIVEN: DDP diagrams publication #60369400.

THE STUDENT WILL: Trace to module level clock signals and locate procedure for tuning clocks.

E.O. 2.45 GIVEN: DDPII diagrams publication #60425800.

THE STUDENT WILL: trace to module level signals used to read ECS in DDPII.

E.O. 2.46 GIVEN: DDPII diagrams publication #60425800.

THE STUDENT WILL: trace to module level signals used to write ECS in DDPII.

E.O. 2.47 GIVEN: DDPII diagrams publication #60425800.

THE STUDENT WILL: trace to module level signals used to Master Clear Port function in DDPII.

E.O. 2.48 GIVEN: DDPII diagrams publication #60425800.

THE STUDENT WILL: trace to module level signals used to status the DDPII in the DDPII.

E.O. 2.49 GIVEN: DDPII diagrams publication #60425800.

THE STUDENT WILL: trace to module level signals used to complete a flag function in DDPII.

E.O. 2.50 GIVEN: Error display handouts HO-102 through HO-105, DDP C.E. manual #60369400 and SMM publication #75442338.

THE STUDENT WILL: list general areas in the logic that could cause the failures shown on the DDP diagnostic display.

CYBER 17X ECS THEORY COURSE
COURSE CHART

	DAY 1	DAY 2	DAY 3	DAY 4	DAY 5
1	Introduction to Course	Review and Quiz	Review and Quiz	Review and Quiz	Review
	Introduction to ECS				Bank Bit
2	Inst. Format	175 Coupler	6640 Introduction Block Diagram	6635 Introduction	Data Path and Control
	Add. Format		6640 Logic	Request and Address Logic	
	Flag Functions				
3	175 Coupler Block Diagram			Two Wire Memory	
4	6640 A/B Block Diagram	175 CMC		Stack Physical Description	Maintenance Mode
		CYBER 173 Block Diagram			Installation and check-out Manual: Review
	6635 Block Diagram				
5		173 CPU CMC Coupler		Address Bit Assignments	
	175 CPU and CMC Logic as Related to ECS		Flag Function	Word Line Selection	Diagnostics and Failure Analysis
6				Degrade	
			Master Clear Clocks Failure Analysis	Failure Analysis	
7					
8					

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	DAY 6	DAY 7	DAY 8	DAY	DAY
1	Review and Quiz	Review	Review		
		DDP I Block Diagrams	Clocks		
2	Introduction to 6640 D/E		P. M. EPS		
	6640 D/E Parity Logic	Programming	Diagnostics		
3		Introduction to Manual	Failure Analysis		
	6640 D/E 1/2 Access				
4	Introduction to ECS II	DDP I Logic	Programming DDP II		
	Address System Rev.		Manual		
5	Bay Logic		DDP II Logic		
6	Failures and Maintenance		Failure Analysis		
7					
8					

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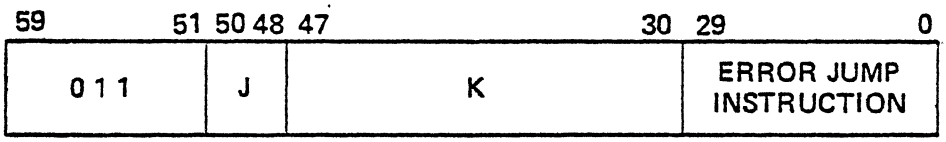
TABLE OF CONTENTS

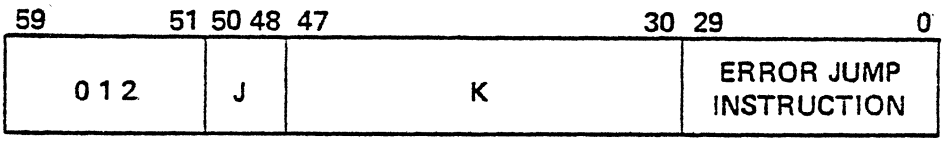
ECS INSTRUCTIONS

Read Extended Core Storage



011 RE Bj + K

Write Extended Core Storage



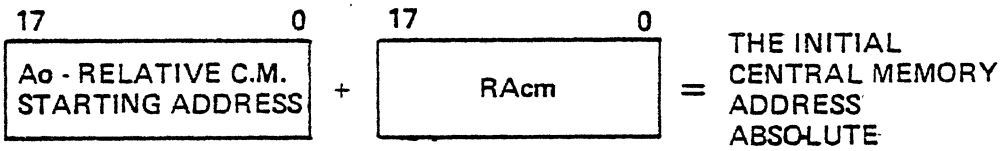
012 WE Bj + K

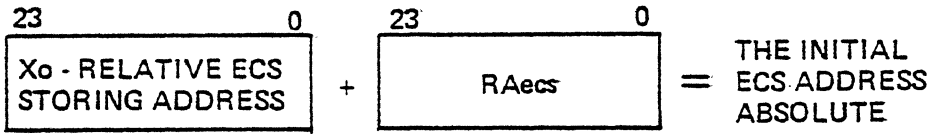
Word Count

Bj + K = Number of 60 Bit Words To Be Transfered

Xo and Ao Registers

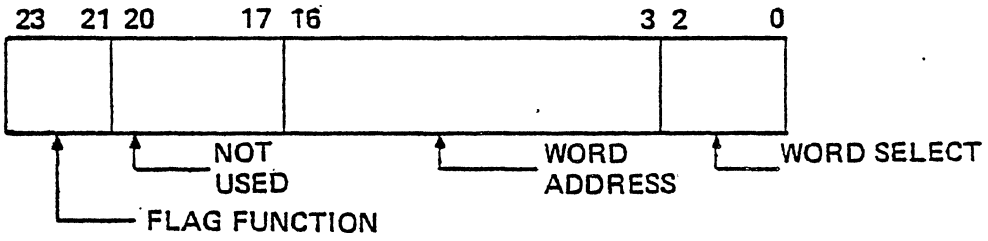
Data Must Be Loaded Into Xo and Ao Before ECS Instruction Is Executed



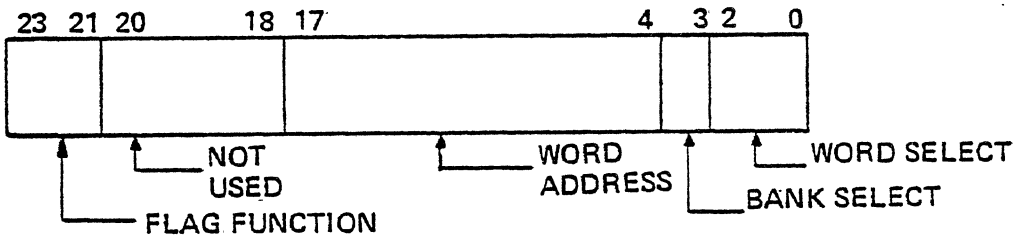


ECS II Address Formats

ECS II 131k System



ECS II 262k System



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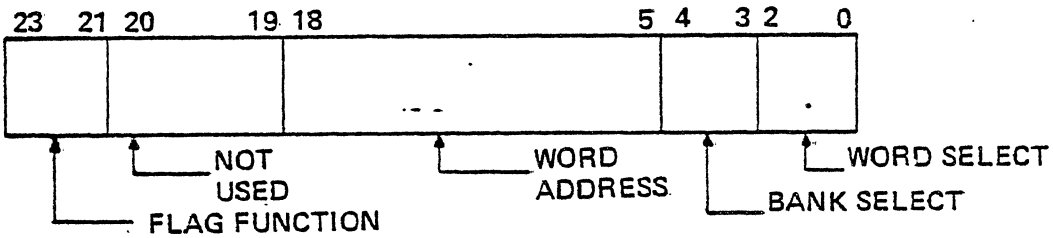
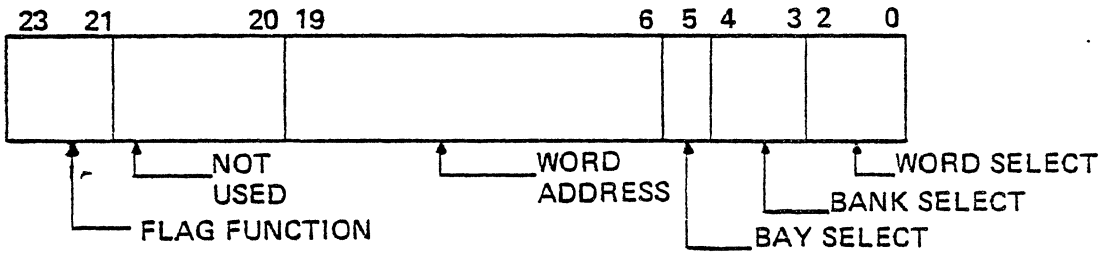
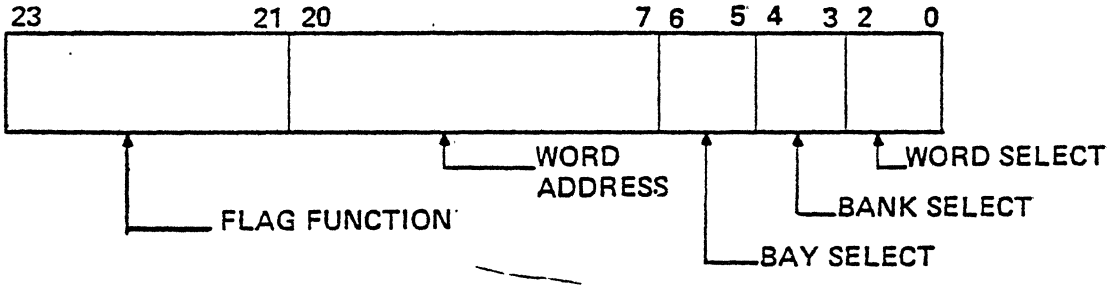


ECS II 1048k System



ECS II 2096k System



ECS Instruction Exit Conditions

Full Exit - Next Instruction at Parcel No. 0, at P + 1

- Normal Termination of ECS Instruction

Half Exit - Next Instruction at Parcel No. 2, at P

- Error Termination of ECS Instruction
- Error Conditions

  Central Processor Parity Error

  CMC Double Error

  CSU Address Parity Error

  CMC Data Parity Error

  ECS Bank Parity Error

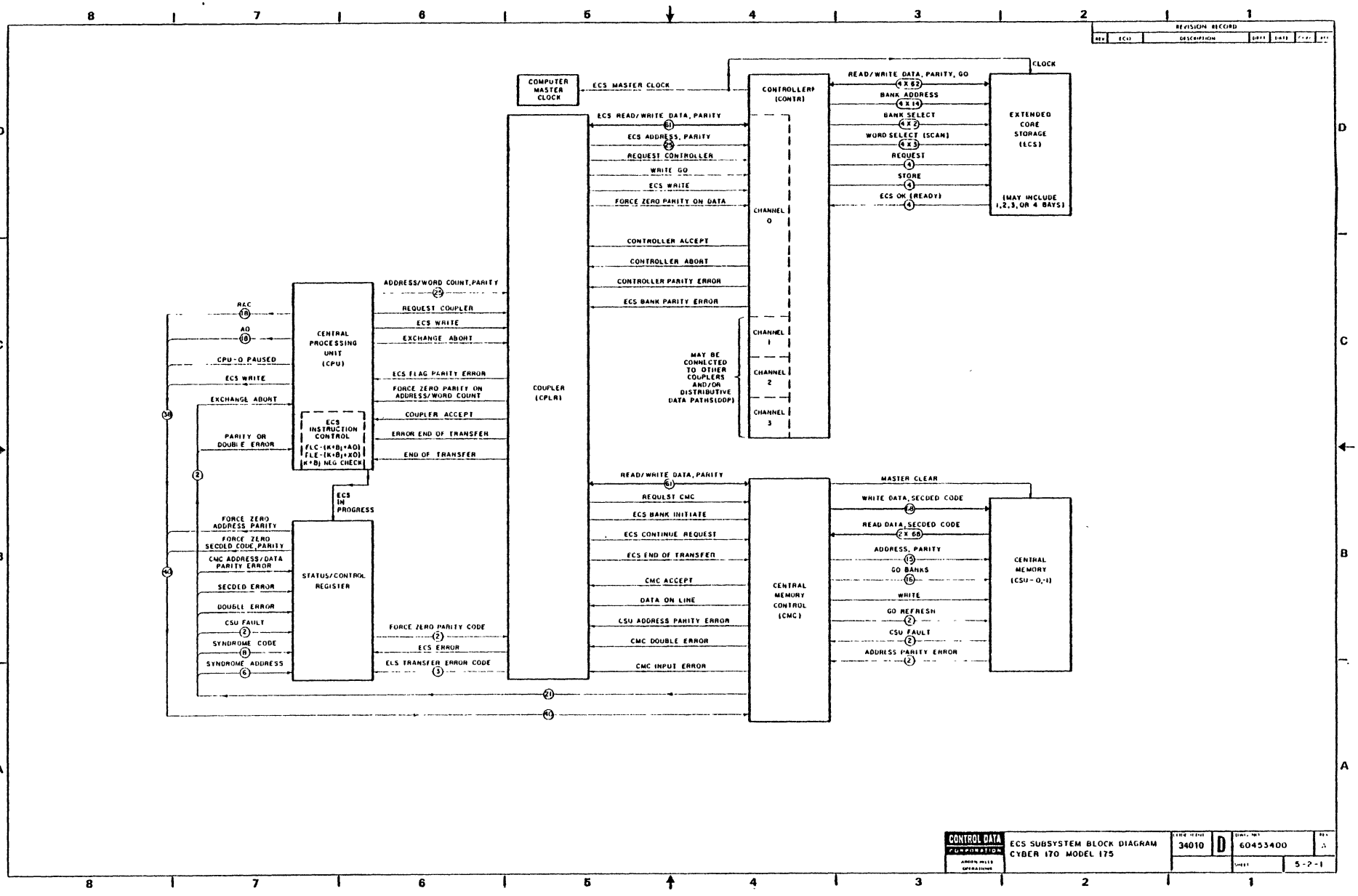
  ECS Controller Data Parity Error

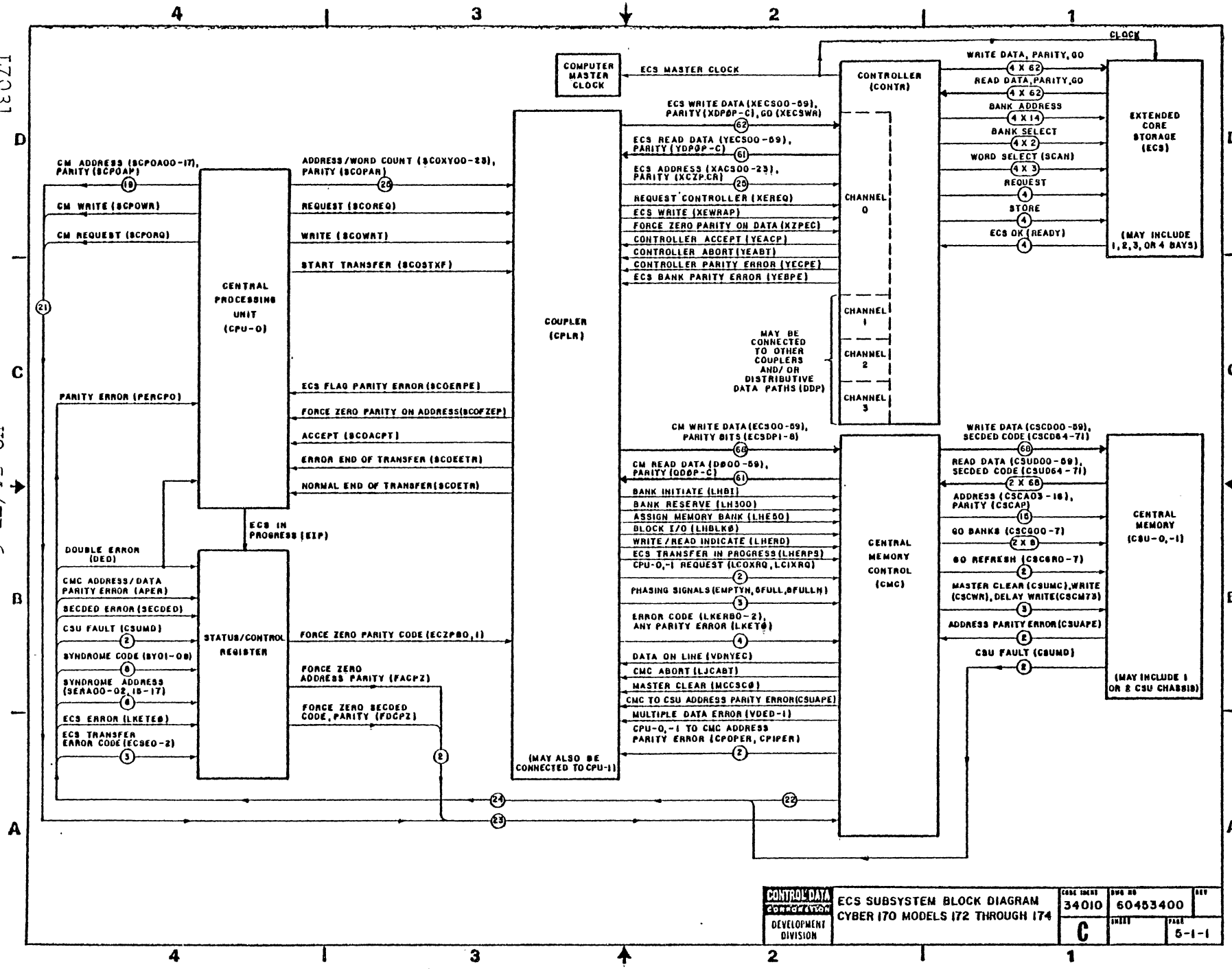
  ECS Controller Address Parity Error

Exchange Jump During ECS Instruction

If an Exchange Jump occurs while an ECS transfer is in progress, the exchange waits until completion of a record. Action is then as follows:

1. If the record just completed is the last record of the block transfer and the transfer was error free, the Central Processor exits to (P) + 1. The Exchange Jump then takes place.
2. If the record just completed is the last record of the block transfer and an error condition exists, the Central Processor exits to the lower instruction, executes it, and then the Exchange Jump is performed.
3. If the record just completed does not complete the block transfer, the transfer is terminated and the Exchange Jump is performed. A return Exchange Jump to this program begins execution with the ECS Read or Write instruction and restarts the transfer. Note the transfer does not resume at the point it was interrupted; rather, the entire transfer must be repeated.


REVISION RECORD
REV
ECO
DESCRIPTION
DATE
DRAFT
CHK
APP
COMPUTER MASTER CLOCK
ECS MASTER CLOCK
CLOCK
CONTROLLER (CONTR)
READ/WRITE DATA, PARITY, GO
4 X 62
BANK ADDRESS
4 X 14
BANK SELECT
4 X 2
WORD SELECT (SCAN)
4 X 3
REQUEST
4
STORE
4
ECS OK (READY)
4
EXTENDED CORE STORAGE (ECS)
(MAY INCLUDE 1,2,3, OR 4 BAYS)
ECS READ/WRITE DATA, PARITY
61
ECS ADDRESS, PARITY
23
REQUEST CONTROLLER
WRITE GO
ECS WRITE
FORCE ZERO PARITY ON DATA
CHANNEL 0
CONTROLLER ACCEPT
CONTROLLER ABORT
CONTROLLER PARITY ERROR
ECS BANK PARITY ERROR
CHANNEL 1
CHANNEL 2
CHANNEL 3
MAY BE CONNECTED TO OTHER COUPLERS AND/OR DISTRIBUTIVE DATA PATHS (OOP)
COUPLER (CPLR)
ADDRESS/WORD COUNT, PARITY
22
REQUEST COUPLER
ECS WRITE
EXCHANGE ABORT
ECS FLAG PARITY ERROR
FORCE ZERO PARITY ON ADDRESS/WORD COUNT
COUPLER ACCEPT
ERROR END OF TRANSFER
END OF TRANSFER
A&C
18
A0
18
CPU-0 PAUSED
ECS WRITE
EXCHANGE ABORT
34
PARITY OR DOUBLE ERROR
2
CENTRAL PROCESSING UNIT (CPU)
ECS INSTRUCTION CONTROL
FLC-(K+B)+A0)
FLE-(K+B)+X0)
(K+B) NEG CHECK
ECS IN PROGRESS
FORCE ZERO ADDRESS PARITY
FORCE ZERO SECDED CODE PARITY
CMC ADDRESS/DATA PARITY ERROR
SECDED ERROR
DOUBLE ERROR
CSU FAULT
2
SYNDROME CODE
8
SYNDROME ADDRESS
6
40
STATUS/CONTROL REGISTER
FORCE ZERO PARITY CODE
2
ECS ERROR
ECS TRANSFER ERROR CODE
3
21
10
READ/WRITE DATA, PARITY
61
REQUEST CMC
ECS BANK INITIATE
ECS CONTINUE REQUEST
ECS END OF TRANSFER
CMC ACCEPT
DATA ON LINE
CSU ADDRESS PARITY ERROR
CMC DOUBLE ERROR
CMC INPUT ERROR
CENTRAL MEMORY CONTROL (CMC)
MASTER CLEAR
WRITE DATA, SECDED CODE
40
READ DATA, SECDED CODE
2 X 68
ADDRESS, PARITY
19
GO BANKS
16
WRITE
GO REFRESH
2
CSU FAULT
2
ADDRESS PARITY ERROR
2
CENTRAL MEMORY (CSU-0,-1)
CONTROL DATA CORPORATION
ARDEN HILLS OPERATIONS
ECS SUBSYSTEM BLOCK DIAGRAM
CYBER 170 MODEL 175
STOCK NUMBER
34010
D
DWG. NO.
60453400
REV
A
SHEET
5-2-1



I7031

HO-5A/TR-5

Part 3

EXTENDED CORE STORAGE (ECS) COUPLER

MANUAL TAKEN FROM REV. LEVEL A
5/3/76

PRIMARY BLOCK DIAGRAM
ECS COUPLER

L7031

The ECS coupler is the connecting link between the computer system and the optional ECS subsystem that augments the central memory (CM) of the computer system. The following paragraphs describe the interface signals used by the ECS coupler to complete a transfer operation.

CENTRAL PROCESSOR UNIT INTERFACE SIGNALS

REQUEST COUPLER

The CPU generates this signal when it has decoded either a read ECS (011 instruction) or a write ECS (012 instruction) and needs the coupler to transfer information. The coupler uses the signal to prepare its logic circuits for the receipt of the transfer word count and the starting ECS address for the information.

COUPLER ACCEPT

The coupler generates this signal if it is not busy with a previous request and is ready to receive the word count and starting ECS address to start the transfer.

H0-7

WORD COUNT

The word count bits (0 through 17) plus one odd parity bit (bit 24) indicate the number of 60-bit words in the transfer operation.

ADDRESS

The address bits (0 through 23) plus one odd parity bit (bit 24) indicate the starting ECS address for the transfer operation.

ECS WRITE

The CPU sends this signal to the coupler when an 012 instruction is decoded and data is to be written into ECS. The absence of this signal indicates an ECS read (011 instruction).

EXCHANGE ABORT ECS

The CPU generates this signal if the CMC receives an exchange request from the peripheral processor subsystem or the CPU. The receipt of this signal in the coupler causes it to abort the transfer at the end of the current record of information.

ECS TRANSFER ERROR AND CODE 0 THROUGH 2

The coupler error code generator generates this signal if an error is detected during a transfer operation. The coupler sends the transfer error signal with the 3-bit error code for the error detected to the CPU along with the error end-of-transfer signal.

FORCE ZERO PARITY ON ADDRESS/WORD COUNT

The coupler sends this signal to the CPU to force zero parity on the address and word count for the coupler. This is used to check the capability of the coupler to detect a parity error on the address and word count.

ERROR END OF TRANSFER

The coupler sends this signal to the CPU when an error was detected during the transfer operation. Certain errors cause the transfer operation to abort at the end of the record while others allow the transfer to be completed.

Errors aborting the transfer at the end of the record are:

- Word count or address parity error (CPU to CPLR).
- Address parity error (CPLR to ECS controller).
- ECS bank addressed is not available due to maintenance mode or loss of power. (This error does not cause an abort during an ECS read operation.)

Errors allowing the transfer to complete are:

- Address parity error (CMC to CSU).
- Data parity error (CMC to ECS controller).
- Data parity error (ECS controller to CMC).
- Data parity error (ECS controller to ECS memory).
- Double error detected in data read from CM.

END OF TRANSFER

The coupler sends this signal to the CPU when the transfer operation is completed normally.

FORCE ZERO PARITY CODE 0 AND 1

The CPU sends these code bits to the coupler for translation. The code is translated for zero parity instructions to the ECS controller or the CPU.

CENTRAL MEMORY CONTROL INTERFACE SIGNALS

ECS REQUEST CMC

The coupler sends this signal to request CM access after the coupler has received the address and word count from the CPU.

CMC ACCEPT

The CMC sends this signal to the coupler when the CM access request (ECS request CMC) has been accepted. The coupler must send the ECS continue request signal and bank initiate signal after the CMC accept to start the CM memory cycle.

ECS CONTINUE REQUEST

The coupler sends this signal to the CMC to reserve the CM banks for the transfer operation.

ECS BANK INITIATE

The coupler sends this signal to the CMC 400 nanoseconds after the ECS continue request signal to cause the CMC to send the address and a go signal to CM and start a CM memory cycle.

ECS END OF TRANSFER

The coupler sends this signal to the CMC when the last record has been received. The signal clears the ECS in progress status in the CMC.

ECS FLAG PARITY ERROR

The coupler sends this signal to the CMC when a parity error is detected in the address received by the ECS controller during a flag register operation.

DATA ON LINE (GO ECS)

This signal accompanies the CM read data to the coupler to indicate the data lines contain valid information.

CSU ADDRESS PARITY ERROR

The coupler receives this signal when an address parity error occurs on the CMC address to the CSU for an ECS related CM reference.

CMC DOUBLE ERROR

The coupler receives this signal when the single error correction double error detection (SECDED) circuit detects a double error on data read from CM during an ECS transfer operation.

CMC INPUT ERROR

The coupler receives this signal when a parity error is detected on the data received by the CMC from ECS.

DATA (CM READ) BITS 0 THROUGH 59, PARITY

These are the 60 data bits read from CM and their odd parity bit for an ECS write operation.

DATA (CM WRITE) BITS 0 THROUGH 59, PARITY

These are the 60 data bits to be written into CM and their odd parity bit for an ECS read operation.

ECS CONTROLLER INTERFACE SIGNALS

REQUEST CONTROLLER

The coupler receives this signal prior to each record of data to be transferred. The first and last records may not be full records but they still require request controller signals.

CONTROLLER ACCEPT

The controller sends this signal to the coupler when it is ready for a transfer of one record.

ECS ADDRESS BITS 0 THROUGH 23

The coupler sends these bits containing the bank address to the controller for the ECS record to be transferred. The address bits are transmitted at the same time as the request controller signal.

ECS ADDRESS PARITY BIT

The coupler sends the odd parity bit with the address bits to the controller.

ECS WRITE

The coupler sends this signal to the controller to indicate the data transfer is an ECS write operation. The ECS write is transmitted at the same time as the request controller signal. The absence of this signal indicates the transfer operation is an ECS read operation.

CONTROLLER ABORT

The controller sends this signal to the coupler to indicate the data transfer was aborted. The transfer is aborted by the controller due to one or more of the following reasons.

- ECS bank address referenced does not exist.
- ECS bank is in maintenance mode.
- ECS bank does not have power.
- Address parity error has been detected at the controller.

FORCE ZERO PARITY ON DATA

The coupler sends this signal to the controller to force zero parity on data transferred to the CMC. This tests the capability of the parity error detection circuit in the CMC to detect parity errors.

CONTROLLER PARITY ERROR

The controller sends this signal to the coupler when the controller detects a parity error on the address or data received from CMC. If an address parity error is detected, the controller sends an abort signal at the same time as the parity error signal.

ECS BANK PARITY ERROR

The controller sends this signal to the coupler when a parity error is detected on data going to or from the ECS banks.

DATA (ECS WRITE) BITS 0 THROUGH 59

The coupler sends 60 bits of data to the controller during an ECS write operation.

DATA (ECS READ BITS 0 THROUGH 59)

The controller sends 60 bits of data to the coupler during an ECS read operation.

DATA (ECS READ) PARITY

The controller sends an odd parity bit to the coupler with the data transferred during an ECS read operation.

DATA (ECS WRITE) PARITY, GO

The coupler sends an odd parity bit to the controller with the data transferred during an ECS write operation. A go signal to the controller referred to as a data-on-the-line signal, indicates valid transfer data.

GENERAL DESCRIPTION

The ECS coupler is activated when the central processor initiates a read or write ECS operation and issues a request coupler signal to the coupler. When the coupler receives the request, it sends a coupler accept signal to the CPU. The CPU sends the word count 350 nanoseconds after it receives the coupler accept signal and 50 nanoseconds later it sends the ECS starting address. The word count enters the word count control Y register and the address enters the X and K registers. The CPU sends an ECS write signal at the same time as the request coupler signal for an ECS write operation (012 instruction). The absence of the write signal or a not write signal indicates an ECS read operation (011 instruction).

The coupler transmits the request controller signal, ECS starting address, and the ECS write signal (if present), to the ECS controller. If the ECS is not busy performing another ECS operation, the ECS controller sends a controller accept signal to the coupler. If this is an ECS write operation, the coupler responds to the controller accept signal by issuing an ECS continue request signal and 400 nanoseconds later issues an ECS bank initiate signal to CMC. In an ECS read operation, the ECS continue request signal is not issued for 1300 nanoseconds and then 400 nanoseconds later the ECS bank initiate is issued. In an ECS write operation, data is passed from the CMC through the 16-word random access memory (RAM) data buffer, the data registers and then transmitted to the ECS controller. During an ECS read operation, data passes directly through the coupler via the data registers. In either mode of operation the transmission of data continues until the transfer is completed or an error signal is detected by the coupler. If an error is detected during an ECS read operation and an error signal is generated, the remaining words transferred to the CMC are all zeros. If the error is detected in an ECS write operation and an error signal generated, the request controller signal is blocked to end the data transfer and prevent data from possibly being written into an incorrect address and destroying other data.

The 18 bit Y register keeps track of the word count and decrements each time a word is received. The decrementing of the Y register continues until Y is reduced to zero and the end time control circuit activates to end the transfer operation.

The CPU provides the 23-bit ECS starting address to the X and K registers for the transfer operation. The address register is incremented in octal addresses of ten for each location of a record in ECS. The 24th address bit is not used by the X register as part of the address but is routed through the coupler and used by the ECS controller for a flag operation.

The Y and K registers provide the P select with the lower 3 bits of both the address and the word count. The P select circuit output switches from the K bits to the Y bits when the coupler transmits the last record. The P counter and P equals zero check circuit controls the number of words transferred during each record.

The error register receives external error signals from the CMC, CPU, and ECS controller and internally a parity error signal if the address/word count from the CPU has a parity error. The error signals are converted to an error code that is transmitted to the status and control register via the CPU.

The status and control register via the CPU sends the coupler a force zero parity code during diagnostics to force zero parity to the ECS controller and the CPU to create a parity error. The error detection circuits should detect the parity error and return an error signal to the error register in the coupler.

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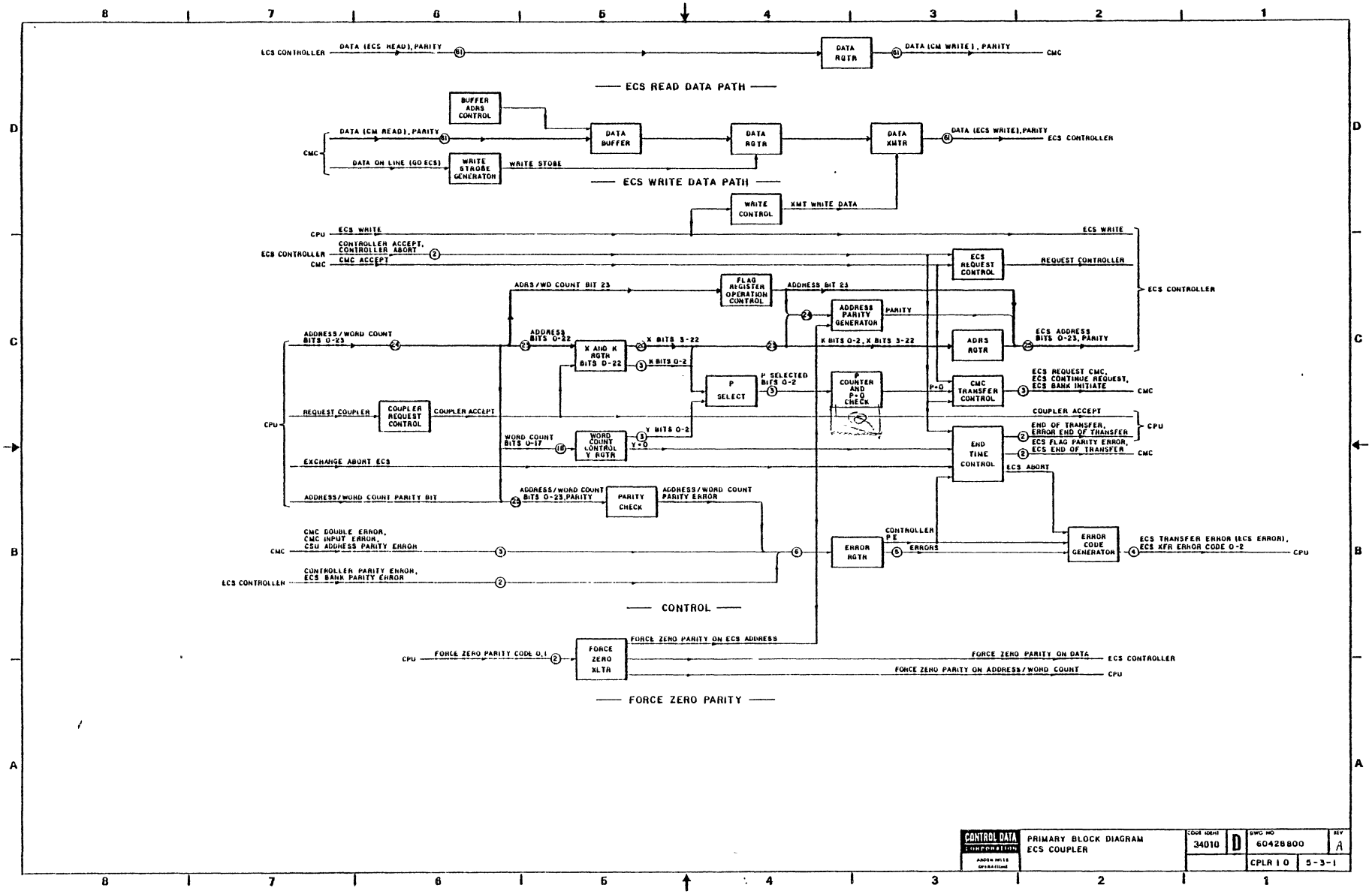
HO-10/TR-8



CONTROL DATA CORPORATION	PRIMARY BLOCK DIAGRAM ECS COUPLER	CODE IDENT 34010	D	DWG NO 60428800 REV A
				CPLR 10 5-3-1

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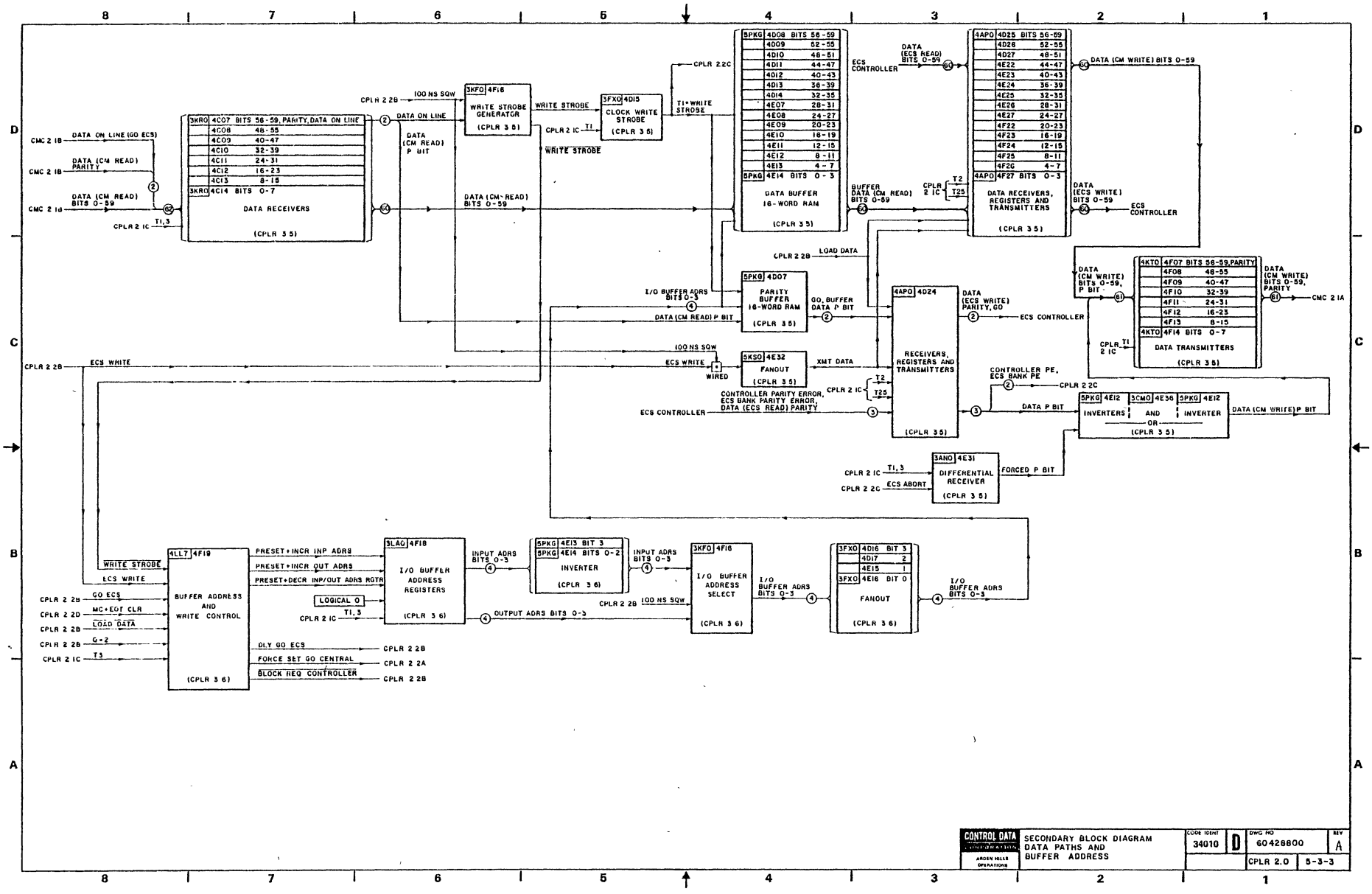

CONTROL DATA	SECONDARY BLOCK DIAGRAM DATA PATHS AND BUFFER ADDRESS	CODE IDENT 34010	D	DWG NO 60428800	REV A
ARDEN HILLS OPERATIONS				CPLR 2.0	5-3-3

HO-11

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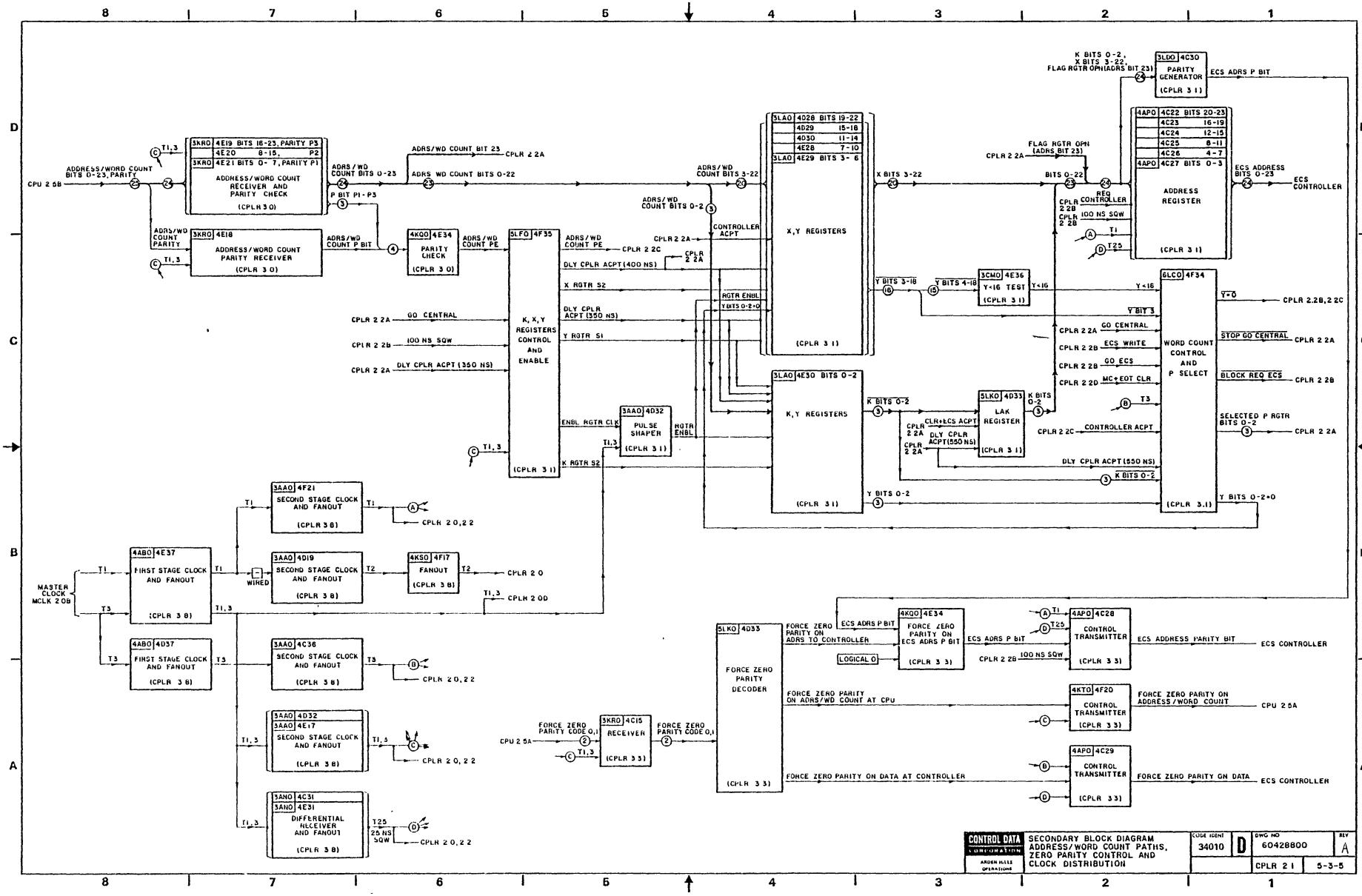
H0-12


ADDRESS/WORD COUNT BITS 0-23, PARITY
CPU 2 5B
3KRO 4E19 BITS 16-23, PARITY P3
3KRO 4E20 8-15, P2
3KRO 4E21 BITS 0-7, PARITY P1
ADDRESS/WORD COUNT RECEIVER AND PARITY CHECK (CPLR 3 0)
ADRS/WD COUNT PARITY
3KRO 4E18
ADDRESS/WORD COUNT PARITY RECEIVER (CPLR 3 0)
ADRS/WD COUNT BITS 0-23
ADRS/WD COUNT BIT 23
CPLR 2 2A
ADRS WD COUNT BITS 0-22
P BIT P1-P3
ADRS/WD COUNT P BIT
4KQO 4E34
PARITY CHECK (CPLR 3 0)
ADRS/WD COUNT PE
5LFO 4F35
ADRS/WD COUNT BITS 3-22
ADRS/WD COUNT BITS 0-2
CONTROLLER ACPT
CPLR 2 2C
DLY CPLR ACPT (400 NS)
X RGTR S2
RGTR ENBL
Y BITS 0-2+0
DLY CPLR ACPT (350 NS)
Y RGTR S1
CPLR 2 2A GO CENTRAL
CPLR 2 2B 100 NS SQW
CPLR 2 2A DLY CPLR ACPT (350 NS)
K, X, Y REGISTERS CONTROL AND ENABLE
(CPLR 3 1)
ENBL RGTR CLK
3AAO 4D32
PULSE SHAPER (CPLR 3 1)
RGTR ENBL
K RGTR S2
5LAO 4D28 BITS 19-22
4D29 15-18
4D30 11-14
4E28 7-10
5LAO 4E29 BITS 3-6
X,Y REGISTERS
(CPLR 3 1)
5LAO 4E30 BITS 0-2
K,Y REGISTERS
(CPLR 3 1)
X BITS 3-22
Y BITS 3-18
Y BITS 4-18
3CMO 4E36
Y=16 TEST (CPLR 3 1)
Y=16
Y BIT 3
K BITS 0-2
5LKO 4D33
LAK REGISTER (CPLR 3 1)
CLR+ECS ACPT
CPLR 2 2A DLY CPLR ACPT (550 NS)
DLY CPLR ACPT (550 NS)
Y BITS 0-2
K BITS 0-2, X BITS 3-22, FLAG RGTR OPN (ADRS BIT 23)
5LDO 4C30
PARITY GENERATOR (CPLR 3 1)
ECS ADRS P BIT
FLAG RGTR OPN (ADRS BIT 23)
CPLR 2 2A
BITS 0-22
REQ CONTROLLER
CPLR 2 2B 100 NS SQW
4APO 4C22 BITS 20-23
4C23 16-19
4C24 12-15
4C25 8-11
4C26 4-7
4APO 4C27 BITS 0-3
ADDRESS REGISTER (CPLR 3 1)
ECS ADDRESS BITS 0-23
ECS CONTROLLER
6LCO 4F34
WORD COUNT CONTROL AND P SELECT
(CPLR 3.1)
CPLR 2 2A GO CENTRAL
CPLR 2 2B ECS WRITE
CPLR 2 2B GO ECS
CPLR 2 2D MC+EOT CLR
CPLR 2 2C CONTROLLER ACPT
Y=0
CPLR 2.2B, 2 2C
STOP GO CENTRAL
CPLR 2 2A
BLOCK REQ ECS
CPLR 2 2B
SELECTED P RGTR BITS 0-2
CPLR 2 2A
Y BITS 0-2+0
MASTER CLOCK MCLK 20B
4ABO 4E37
FIRST STAGE CLOCK AND FANOUT (CPLR 3 8)
WIRED
4ABO 4D37
FIRST STAGE CLOCK AND FANOUT (CPLR 3 8)
3AAO 4F21
SECOND STAGE CLOCK AND FANOUT (CPLR 3 8)
CPLR 2 0, 2 2
3AAO 4D19
SECOND STAGE CLOCK AND FANOUT (CPLR 3 8)
4KSO 4F17
FANOUT (CPLR 3 8)
CPLR 2 0
CPLH 2 0D
3AAO 4C36
SECOND STAGE CLOCK AND FANOUT (CPLR 3 8)
3AAO 4D32
3AAO 4E17
SECOND STAGE CLOCK AND FANOUT (CPLR 3 8)
3ANO 4C31
3ANO 4E31
DIFFERENTIAL RECEIVER AND FANOUT (CPLR 3 8)
T25 25 NS SQW
FORCE ZERO PARITY CODE 0,1
CPU 2 5A
3KRO 4C15
RECEIVER (CPLR 3 3)
FORCE ZERO PARITY DECODER (CPLR 3 3)
FORCE ZERO PARITY ON ECS ADRS P BIT
ECS ADRS P BIT
LOGICAL 0
4KQO 4E34
FORCE ZERO PARITY ON ECS ADRS P BIT (CPLR 3 3)
4APO 4C28
CONTROL TRANSMITTER (CPLR 3 3)
ECS ADDRESS PARITY BIT
ECS CONTROLLER
FORCE ZERO PARITY ON ADRS/WORD COUNT AT CPU
4KTO 4F20
CONTROL TRANSMITTER (CPLR 3 3)
FORCE ZERO PARITY ON ADDRESS/WORD COUNT
CPU 2 5A
FORCE ZERO PARITY ON DATA AT CONTROLLER
4APO 4C29
CONTROL TRANSMITTER (CPLR 3 3)
FORCE ZERO PARITY ON DATA
ECS CONTROLLER
CONTROL DATA CORPORATION
ARDEN HILLS OPERATIONS
SECONDARY BLOCK DIAGRAM ADDRESS/WORD COUNT PATHS, ZERO PARITY CONTROL AND CLOCK DISTRIBUTION
CODE IDENT 34010
D
DWG NO 60428800
REV A
CPLR 2 1
5-3-5

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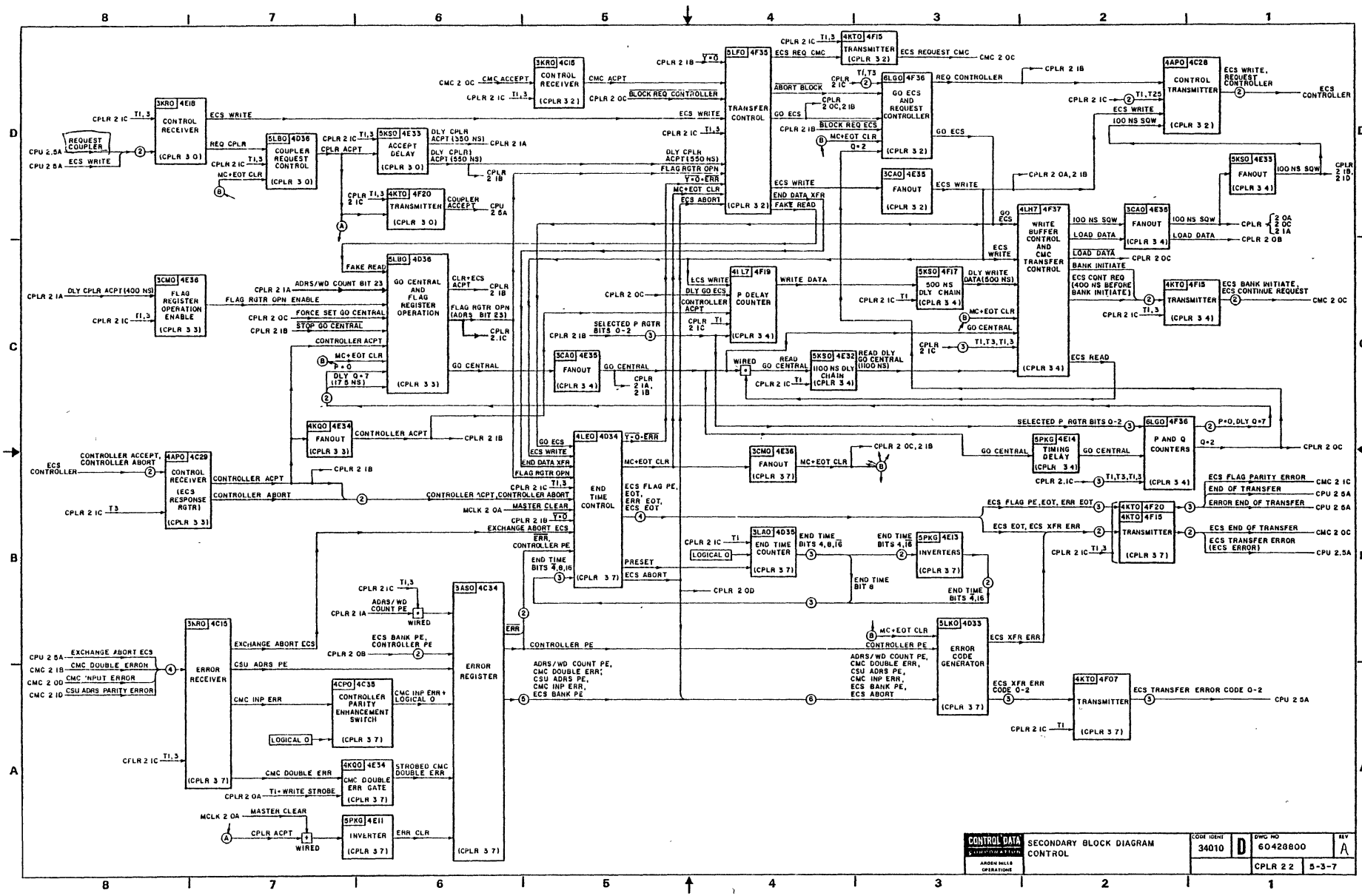
H0-13


REQUEST COUPLER
CONTROL RECEIVER
COUPLER REQUEST CONTROL
ACCEPT DELAY
TRANSMITTER
FANOUT
CONTROL RECEIVER
TRANSFER CONTROL
TRANSMITTER
GO ECS AND REQUEST CONTROLLER
FANOUT
CONTROL TRANSMITTER
FANOUT
WRITE BUFFER CONTROL AND CMC TRANSFER CONTROL
FANOUT
FANOUT
FLAG REGISTER OPERATION ENABLE
GO CENTRAL AND FLAG REGISTER OPERATION
P DELAY COUNTER
500 NS DLY CHAIN
TRANSMITTER
FANOUT
FANOUT
FANOUT
FANOUT
CONTROL RECEIVER (ECS RESPONSE RGTR)
END TIME CONTROL
END TIME COUNTER
INVERTERS
TIMING DELAY
P AND Q COUNTERS
ERROR RECEIVER
CONTROLLER PARITY ENHANCEMENT SWITCH
CMC DOUBLE ERR GATE
INVERTER
ERROR REGISTER
ERROR CODE GENERATOR
TRANSMITTER
TRANSMITTER
TRANSMITTER
CONTROL DATA SECONDARY BLOCK DIAGRAM CONTROL
CODE IDENT 34010
D
DWG NO 60428800
REV A
CPLR 2 2
5-3-7

DETAILED-PAK DIAGRAM

CPU INTERFACE FOR COUPLER REQUEST CONTROL, ADDRESS/WORD COUNT, AND ECS WRITE

COUPLER REQUEST CONTROL

An ECS operation begins when the CPU sends a request coupler signal to the ECS coupler. If the request is for a write ECS operation (012 instruction), the request coupler signal is accompanied by an ECS write signal. The absence of the ECS write signal (not ECS write) indicates a read ECS operation (011 instruction).

The request coupler signal sets a latch register (3KR0 pak) which in turn sets the request hold flip-flop (5LB0 pak). The request hold flip-flop holds the request coupler signal if the request flip-flop is not in a reset mode (clear). The request flip-flop is cleared by the master clear signal or the end-of-transfer clear signal generated at the completion of each ECS operation. If the request flip-flop is clear, the output signal of the request hold flip-flop sets the request flip-flop at time T1, 3. The output signal of the request flip-flop disables its own clock input, clears the request hold flip-flop in preparation for the next request, and sets the ECS IP (in progress) flip-flop. The request flip-flop and the ECS IP flip-flop are connected in a one-shot pulse-forming combination. In this combination, the request flip-flop sets on the trailing edge of a clock pulse and forms the leading edge of the coupler accept signal. The ECS IP flip-flop sets 50 nanoseconds later on the trailing edge of the next clock pulse. Since the inverted output signal of the ECS IP flip-flop is ANDed with the output signal of the request flip-flop, the setting of the ECS IP flip-flop breaks the AND gate and forms the trailing edge of the 50-nanosecond coupler accept pulse. The request flip-flop and the ECS IP flip-flop remain set until cleared by the end-of-transfer clear signal at the completion of the transfer operation or the master clear signal.

The coupler accept pulse clears the error register (CPLR 3.7) of any errors detected in the previous transfer operation and indicates to the CPU, via a latch register and transmitter (4KT0 pak), that the coupler accepts the request for the transfer operation. The accept delay chain (5KS0 pak) delays the coupler accept pulse 350 and 550 nanoseconds. The register enable and request CMC circuits use the two delayed coupler accept pulses as timing signals.

ADDRESS/WORD COUNT

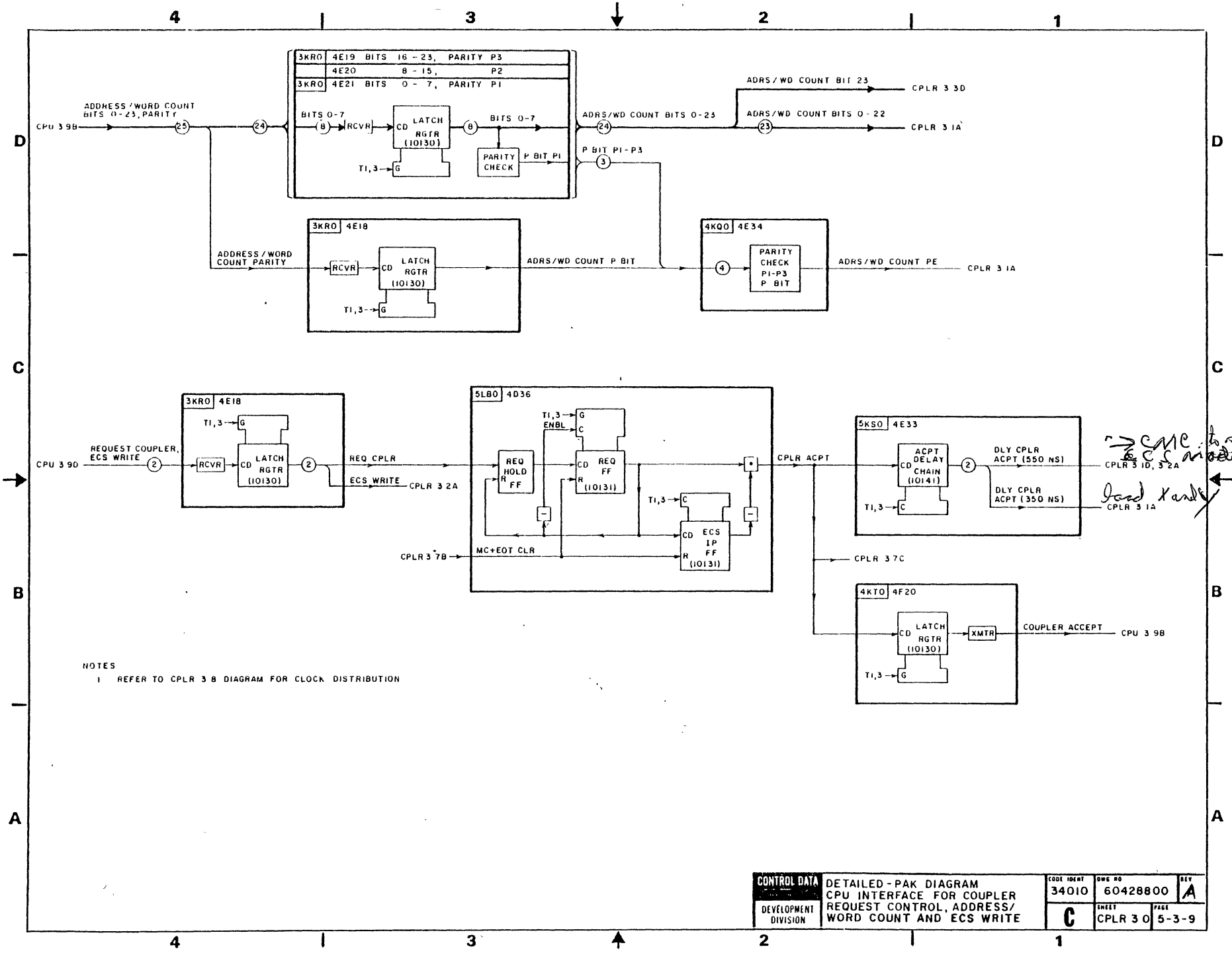
The CPU sends the transfer operation word count and its odd parity bit to the coupler 350 nanoseconds after receiving the coupler accept signal. The word count enters the latch registers which in turn transfer the count at time T1, 3 to the Y register (CPLR 3.1). The parity checker (3KR0 pak) checks the word count in the latch registers in three 8-bit groups for parity errors. The parity checker generates a parity bit for each of the three groups. These parity bits, designated P1 through P3, are merged with the parity bit that accompanied the word count from the CPU in a second parity check circuit (4KQ0 pak). When the 4KQ0 pak parity check circuit detects a parity error in the parity bits, it generates a word count parity error signal for the error register (CPLR 3.7). The parity error signal transfers to the error register via a timing select circuit on the register enable pak (CPLR 3.1).

The CPU sends the transfer operation ECS starting address and its parity bit to the coupler 50 nanoseconds after the word count, which is 400 nanoseconds after the CPU receives the coupler accept signal. The address enters the latch registers (3KR0 pak) which in turn transfer the lower address bits 0 through 22 to the X and K registers (CPLR 3.1). The two parity checkers (3KR0 and 4KQ0 paks) check the address and the address parity bit for parity errors in the same manner they check the word count for parity errors. The parity check circuit (4KQ0 pak) transfers an address parity error signal via a timing select circuit on the register enable pak (CPLR 3.1) to the error register (CPLR 3.7).

The CPU sends the ECS starting address with bit 23 set when it wants the ECS controller to perform a flag register operation. The latch register (3KR0 pak) transfers address bit 23 at time T1, 3 to the flag register operation flip-flop (CPLR 3.3). The flag register operation flip-flop merges address bit 23 back with the lower 23 bits of the address in the address register (CPLR 3.1) and performs control functions on coupler circuits for the duration of the flag register operation. The ECS controller performs the flag register function using bits 20 through 22 of the address as the instructions. The controller accomplishes the flag register operation without further instructions or information.

CPLR 3.0 TEST POINTS

Module	Location	Test Point	Description
3KR0	4E19-21	3 (T)	Adrs/Wd Count Bit N
3KR0	4E19-21	5 (T)	Adrs/Wd Count Bit N +1
3KR0	4E19-21	2 (T)	Adrs/Wd Count Bit N +2
3KR0	4E19-21	6 (T)	Adrs/Wd Count Bit N +3
3KR0	4E19-21	13 (T)	Adrs/Wd Count Bit N +4
3KR0	4E19-21	9 (T)	Adrs/Wd Count Bit N +5
3KR0	4E19-21	12 (T)	Adrs/Wd Count Bit N +6
3KR0	4E19-21	8 (T)	Adrs/Wd Count Bit N +7
3KR0	4E19-21	7 (T)	Clock Time T1, 3
3KR0	4E18	3 (T)	Adrs/Wd Count Parity Bit
3KR0	4E18	1 (F)	Adrs/Wd Count Parity Bit
3KR0	4E18	5 (T)	ECS Write
3KR0	4E18	6 (T)	Req Cplr
3KR0	4E18	7 (T)	Clock Time T1, 3
4KQ0	4E34	10 (T)	Parity Bit P1
4KQ0	4E34	9 (T)	Parity Bit P2
4KQ0	4E34	8 (T)	Parity Bit P3
5LB0	4D36	3 (T)	Req Cplr
5LB0	4D36	2 (F)	MC + EOT CLR
5LB0	4D36	1 (T)	Clock Time T1, 3
5KS0	4E33	5 (F)	Dly Cplr Acpt (350NS)
5KS0	4E33	4 (T)	Dly Cplr Acpt (550NS)
5KS0	4E33	13 (T)	Clock Time T1, 3
4KT0	4F20	9 (T)	Cplr Acpt
4KT0	4F20	2 (T)	Clock Time T1, 3



CONTROL DATA DEVELOPMENT DIVISION	DETAILED-PAK DIAGRAM CPU INTERFACE FOR COUPLER REQUEST CONTROL, ADDRESS/ WORD COUNT AND ECS WRITE	CODE IDENT 34010	DWG NO 60428800	REV A
		C	SHEET CPLR 3 0	PAGE 5-3-9

DETAILED-PAK DIAGRAM

REGISTER ENABLE K, X, Y REGISTERS AND P SELECT

Y REGISTER (WORD COUNT)

The CPU sends the 23-bit word count for the data transfer operation 350 nanoseconds after it receives the coupler accept signal. The Y register must be in a preset mode at that time to load the data word count. The Y register monitors and outputs the data word count to the coupler control circuits for the duration of the transfer operation.

The input signals to functional control inputs S1 and S2 of the Y register (3LA0 pak) control its mode of operation. The 50-nanosecond coupler accept signal that was delayed 350 nanoseconds is passed directly through the register enable pak (5FL0 pak) to input S2 of the Y register. The delayed coupler accept (350 nanoseconds) signal is delayed an additional 50 nanoseconds by the 50-nanosecond delay flip-flop (5LF0 pak) before providing an input to S1 of the Y register. Since the output signal of the 50-nanosecond delay flip-flop (that goes to input S1 of the Y register) is inverted, the Y register is in a preset mode until the flip-flop sets. The Y register remains in the preset mode for 50 nanoseconds (350 to 400 nanoseconds after the coupler accept signal). The data transfer operation word count bits 0 through 22 arrive at the Y register 350 nanoseconds after the coupler accept signal and enter the register. The data word count is contained in the lower 19 bits. The upper 4 bits are ignored.

The 50-nanosecond delay flip-flop sets 400 nanoseconds after the coupler accept signal, forcing the Y register into a hold mode. The Y register remains in the hold mode for 50 nanoseconds while the X register loads the ECS starting address. When the 50-nanosecond delay flip-flop clears, it forces the Y register into a decrement mode. Since the Y register contains the number of data words in the ECS transfer operation and is in a decrement mode, it is ready to monitor the data transfer count when enabled. The enable signal to the Y register is the result of the ECS controller accepting the first transfer operation request or the previous transfer of eight 60-bit data words (record). The coupler generates the go central signal from the ECS controller accept signal. The go central signal is ANDed with the 100-nanosecond square wave and generates the enable register clock signal. The clock signal is synchronized with the clock pulse (3AA0 pak) to enable the clock input of the Y register. The clock synchronized register enable signal enables the Y register at the transfer rate of once every 100 nanoseconds unless stopped by the loss of the go central signal. The enable signal decrements the data word count in the Y register at the data transfer rate until the count equals zero.

The 3CM0 and 6LC0 paks monitor the data word count from the Y register for a word count of zero. The complemented Y register bits 4 through 18 are ANDed in the 3CM0 pak which generates the Y register count is less than 16 signal. The Y bits 0 through 2 equal zero test circuit (6LC0 pak) generates an output signal when the bits equal zero. The Y is less than 16 signal and the Y bits 0 through 2 equals zero signal are ANDed with the complement of bit 3 from the Y register. When the word count in the Y register is at zero, all these signals are present, and the AND gate generates the Y equals zero signal that sets the word count equals zero flip-flop. During an ECS write operation, the controller accept signal gates the word count equals zero flip-flop output signal to the end time circuits that starts the timing sequence to end the transfer operation. The coupler receives the controller accept signal after the transfer of the last data word that caused the Y register to go to a zero word count. This ensures that the controller receives the last word of the transfer operation before the end time circuits receive the Y equals zero signal to start the timing sequence and end the transfer operation.

During an ECS read operation, the last word of the transfer operation has left the ECS controller when the word count reaches zero. Therefore, the ECS read signal gates the Y equals zero signal to start the timing sequence and end the transfer operation.

X AND K REGISTERS (ADDRESS)

The coupler X and K registers receive the ECS starting address for the transfer operation from the CPU. The register control circuits increment the X and K registers from the starting address to generate the additional ECS addresses for the data of the transfer operation.

The ECS memory is organized in records (eight 60-bit words) of data. Memory references to ECS normally require a specific address for each record. The exception is the first record of a transfer operation which could contain less than the normal eight words and is referred to as a partial record. The X register provides the normal record address while the K register provides the address of a word within the first record.

The CPU sends the 23-bit starting address 400 nanoseconds after it receives the coupler accept signal. The X and K registers (3LA0 pak) must be in a preset mode 400 nanoseconds after the coupler accept signal to load the ECS starting address.

The coupler accept signal that was delayed 350 nanoseconds is delayed an additional 50 nanoseconds by the 50-nanosecond delay flip-flop (5LF0 pak). The delay flip-flop provides the delayed coupler accept signal (400 nanoseconds) to functional control input S1 of the X register for 50 nanoseconds. Since the complemented delayed coupler accept signal (350 nanoseconds) to input S2 of X register has ended, S1 and S2 are in the proper state to preset the register.

The same delayed coupler accept signal (400 nanoseconds) provided to S1 of the X register is provided to S1 of the K register. The delayed coupler accept signal (400 nanoseconds) from the 50-nanosecond delay flip-flop is ANDed with the 100-nanosecond square wave signal to provide an input to S2 of the K register. Inputs S1 and S2 of the K register are in the proper state to preset the K register at the same time the X register presets.

The X and K registers are in the preset mode for 50 nanoseconds (400 to 450 nanoseconds after the coupler accept signal). During this time, the address bits 0 through 22 arrive and load into the X and K registers. The ECS address uses all 23 bits.

When the 50-nanosecond delay flip-flop clears, the X register goes into the increment mode and the K register goes into the hold mode. The registers remain in their respective modes until the ECS controller returns a controller accept signal to indicate it is ready for the transfer of data and requires the ECS address. After receiving the controller accept signal, the coupler generates the go ECS and go central signals. The go ECS is necessary to start the 100-nanosecond square wave signal. The go central and the 100-nanosecond square wave combine to form the K register S2 signal that alternates the K register from the hold to the increment mode.

With both registers in the increment mode, the register enable signal to the clock input increments the address in the registers. The go central signal is ANDed with the 100-nanosecond square wave and generates the enable register clock signal. The clock signal is synchronized with the clock pulse (3AA0 pak) to enable the clock input of the X and K registers. The clock synchronized register enable signal increments the X and K registers at the transfer rate of once every 100 nanoseconds unless stopped by the loss of the go central signal. The incrementing continues until the transfer is complete and the end time circuits stop the go central signal.

The K register contains zeros except when the first record of a transfer operation is a partial record. The K register allows references to specific 60-bit word locations for the number of words contained in the partial record. The delayed coupler accept signal (550 nanoseconds) gates the first record K register bits (lower 3 bits of the address) into the LAK register (5LK0 pak). The ECS accept signal from the ECS controller clears the LAK register. The ECS accept signal indicates the ECS controller received the first address of the transfer. Since the delayed coupler accept signal (550 nanoseconds) occurs only once every transfer operation, only the lower address bits of the first address from the K register are gated into the LAK register. All remaining addresses will have zeros in the lower 3 bits. Therefore, each time the address registers increment one, the address to ECS increments ten (octal).

The request controller signal gates the address bits into the address register (4AP0 pak). The 100-nanosecond square wave and the T25 clock pulse (25-nanosecond square wave) gate the address bits in the address registers to the transmitter. The T25 clock pulse synchronizes the address bits within the 100-nanosecond square wave for transfer to the ECS controller. The clock time T1 resets the address register in preparation for the next address from the X and K registers.

PARITY GENERATOR

The address bits 0 through 23 provided to the address register (4AP0 pak) for transmission to the ECS controller are also provided to the parity generator (3LD0 pak). The parity generator generates an odd parity bit for each address and transfers the parity bit via the zero parity circuits (CPLR 3.3) to the ECS controller.

ADDRESS/WORD COUNT PE ENABLE

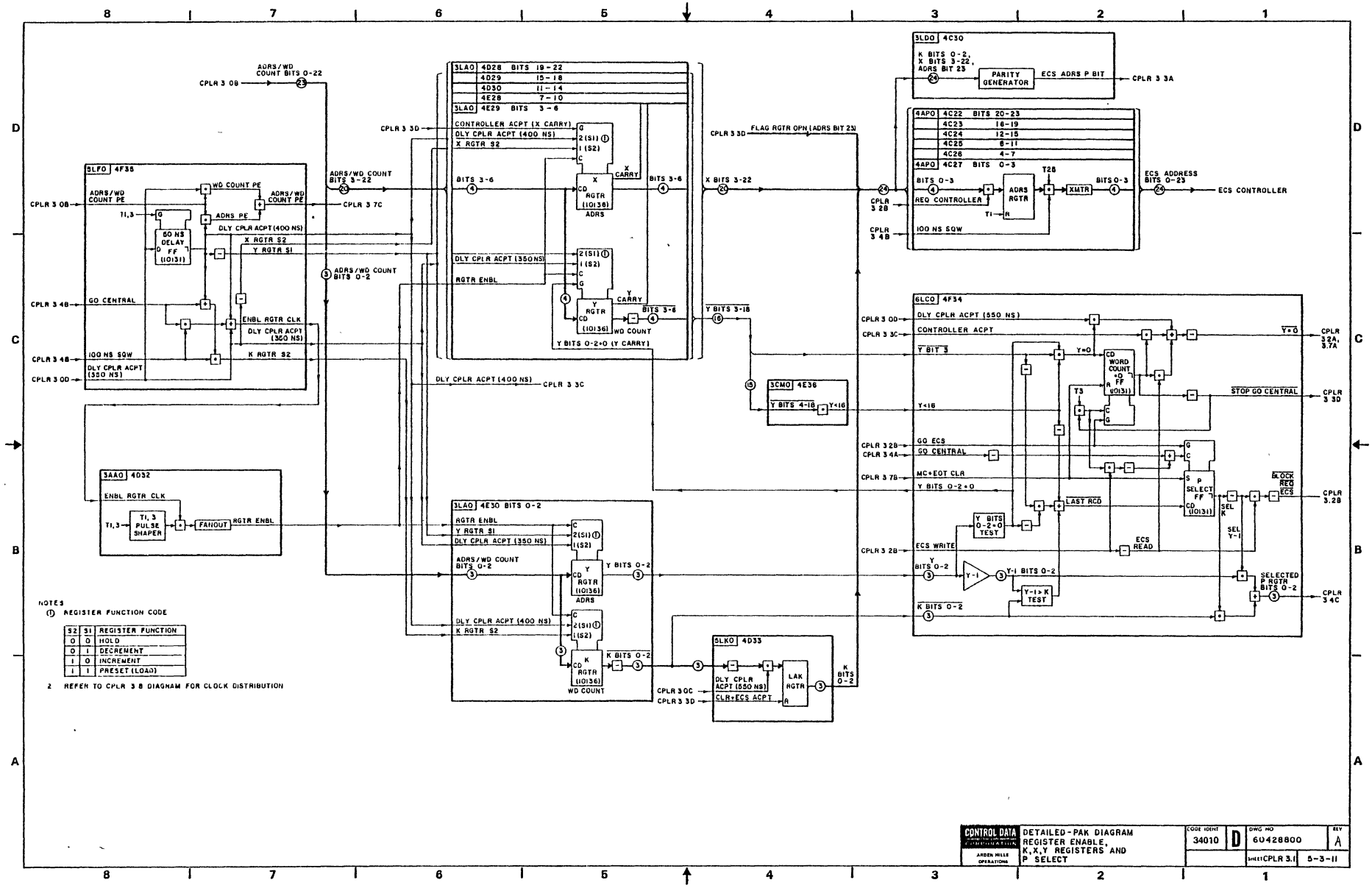
The address/word count parity error (if detected) requires an enable signal synchronized with the appropriate address or word count to pass the error signal on to the error register. The coupler accept signal (350 nanoseconds) gates a word count parity error signal (5LF0 pak) through the select circuit. The delayed coupler accept signal (400 nanoseconds) from the 50-nanosecond delay flip-flop gates an address parity error through the other half of the select circuit. These gating signals perform the synchronizing function that differentiates a word count parity error from an address parity error for the error register.

P SELECT

The P counter (CPLR 3.4) keeps track of the number of words in the record transferred. The P select circuit (6LC0 pak) provides the P counter with the appropriate bits to accomplish that function. The K register (3LA0 pak) provides the complemented lower 3 bits of the address to the Y minus 1 is greater than K test circuit and the P select circuit. The K register contains the lower three address bits which are normally zero except in the case of a partial first record. Since the K register is normally zero, the complemented bits provide a seven to the Y minus 1 is greater than K test circuit and the P select circuit. The Y register (3LA0 pak) provides the 3 bits of the word count to the Y minus 1 circuit (6LC0 pak) which in turn provides its output to the Y minus 1 is greater than K test circuit and the P select circuit. The Y minus 1 is greater than K test circuit controls the P select flip-flop that selects the appropriate bits for the P counter. The go ECS signal that indicates the CMC is ready for a data transfer gates the P select flip-flop. Assuming that Y (data word count) is greater than eight, there is at least part of another record to be transferred. The P select flip-flop selects the K bits (seven) for the P register. The P counter decrements from the number provided by the selected bits at the data transfer rate of one a clock period (100 nanoseconds) until P equals zero indicating the end of one record. The count and bit selections are repeated until Y minus 1 is less than K. When Y minus 1 is less than K, the last record is ready for transfer and the P select flip-flop selects the Y minus 1 value as the selected P register bits. When the P counter decrements to zero this time, the Y count equals zero signal sets the word count equals zero flip-flop. The word count equals zero flip-flop generates the stop go central signal for the go central memory flip-flop (CPLR 3.3) and the Y equals zero signal for end time circuit (CPLR 3.7). The end time circuits generate an end of transfer signal to end the ECS transfer operation.

CPLR 3.1 TEST POINTS

Module	Location	Test Point	Description	Module	Location	Test Point	Description
5LF0	4F35	3 (T)	Clock Time T1, 3	5LK0	4D33	9 (T)	K Rgtr Bit 2
5LF0	4F35	4 (F)	MC + EOT CLR	5LK0	4D33	13 (T)	Dly Cplr Acpt (550 ns)
5LF0	4F35	9 (T)	Dly Cplr Acpt (350 ns)	3CM0	4E36	11 (F)	Y < 16
5LF0	4F35	14 (T)	Go Central	4AP0	4C22-27	13 (F)	Adrs Rgtr Bit N
5LF0	4F35	12 (T)	Dly Cplr Acpt (400 ns)	4AP0	4C22-27	12 (F)	Adrs Rgtr Bit N +1
3AA0	4D32	4 (F)	Rgtr Enbl	4AP0	4C22-27	3 (F)	Adrs Rgtr Bit N +2
3AA0	4D32	9 (F)	Rgtr Enbl	4AP0	4C22-27	14 (F)	Adrs Rgtr Bit N +3
3AA0	4D32	10 (F)	Rgtr Enbl	4AP0	4C22-27	11 (T)	Req Controller
3LA0	4D28,30,	1 (T)	Adrs/Wd Count Bit N	4AP0	4C22-27	9	100 ns SQW
3LA0	4E28,29	2 (T)	Adrs/Wd Count Bit N +1	4AP0	4C22-27	4 (F)	Clock Time T1
3LA0		13 (T)	Adrs/Wd Count Bit N +2	4AP0	4C22-27	2 (T)	ECS Adrs Bit N
3LA0		14 (T)	Adrs/Wd Count Bit N +3	4AP0	4C22-27	5 (T)	ECS Adrs Bit N +1
3LA0		12 (T)	Y Rgtr Carry	4AP0	4C22-27	8 (T)	ECS Adrs Bit N +2
3LA0		3 (T)	X Rgtr Carry	4AP0	4C22-27	10 (T)	ECS Adrs Bit N +3
3LA0		7 (T)	Clock Time T1, 3	4AP0	4C22-27	1	T 25 (25 ns SQW)
3LA0		11 (T)	Y Rgtr Bit N	6LC0	4F34	2 (T)	Y<16
3LA0		8 (T)	Y Rgtr Bit N +1	6LC0	4F34	11 (T)	Word Count = 0
3LA0	4D28,30	9 (T)	Y Rgtr Bit N +2	6LC0	4F34	5 (T)	Y Bit 3
3LA0	4E28,29	10 (T)	Y Rgtr Bit N +3	6LC0	4F34	6 (T)	Y Bits 0 - 2 = 0 Test
3LA0	4E30	1 (T)	Adrs/Wd Count Bit 0	6LC0	4F34	3 (T)	Go Central
3LA0	4E30	2 (T)	Adrs/Wd Count Bit 1	6LC0	4F34	4 (T)	Y - 1 >K Test
3LA0	4E30	13 (T)	Adrs/Wd Count Bit 2	6LC0	4F34	14 (T)	Select K
3LA0	4E30	7 (T)	Clock Time T1, 3	6LC0	4F34	1 (T)	K Bit 0
3LA0	4E30	11 (T)	K Rgtr Bit 0	6LC0	4F34	9 (T)	K Bit 1
3LA0	4E30	8 (T)	K Rgtr Bit 1	6LC0	4F34	8 (T)	K Bit 2
3LA0	4E30	9 (T)	K Rgtr Bit 2	6LC0	4F34	13 (T)	Y - 1 Bit 0
5LK0	4D33	12 (T)	K Rgtr Bit 0	6LC0	4F34	10 (T)	Y - 1 Bit 1
5LK0	4D33	8 (T)	K Rgtr Bit 1	6LC0	4F34	12 (T)	Y - 1 Bit 2



CONTROL DATA CORPORATION ARDEN HILLS OPERATIONS	DETAILED - PAK DIAGRAM REGISTER ENABLE, K,X,Y REGISTERS AND P SELECT	CODE IDENT 34010	D	DWG NO 60428800 REV A
				SHEET CPLR 3.1 5-3-11

DETAILED-PAK DIAGRAM
TRANSFER CONTROL

The basic control center of the coupler during a transfer operation is the transfer control circuit (5LF0 pak). When the CPU initiates a data transfer operation, the coupler must generate a request for the CMC. To generate an ECS request CMC signal, the flag register operation signal must not be present, the Y register must contain a word count, and a parity error must not have been detected in the word count or starting ECS address. When these conditions are available, the Y not equal to zero signal, the not error signal, and the complemented not flag register operation signal are ANDed with the delayed coupler accept (550 nanoseconds) to generate the ECS request CMC signal. The ECS request CMC signal is a 50-nanosecond pulse that occurs once during each transfer operation, 550 nanoseconds after the coupler accepts a transfer operation request from the CPU. The ECS request CMC signal is transmitted to the CMC via a latch register (4KT0 pak) and transmitter at time T1, 3.

The ECS request CMC is not generated if the flag register operation signal is present, Y is equal to zero, or an address/word count parity error signal is present, but an end data transfer signal is generated. The end data transfer signal, 550 nanoseconds after the coupler accepts a transfer operation, sets the end time flip-flop (CPLR 3.7) to end the transfer operation before a data transfer occurs. The ending of the transfer operation before a transfer of data occurs does not affect a flag register operation as it does not require a transfer of data. The word count in the Y register is zero for a flag register operation. The ending of a transfer operation by a starting address/word count parity error prevents data from transferring to an incorrect address in ECS and possibly destroying other data.

If a flag register operation is requested by the CPU, the address received by coupler has bit 23 set. Address bit 23 sets the flag register operation flip-flop (CPLR 3.3) that generates the flag register operation signal. The ECS controller requires only the address with bit 23 set to perform a flag register operation. The flag register operation signal is ANDed (5LF0 pak) with the coupler accept signal that was delayed 550 nanoseconds and synchronized by time T1, 3 to set the accept go flip-flop. The accept go flip-flop generates the go ECS signal. The go ECS signal sets the go ECS flip-flop (6LG0 pak) that is connected with the request controller flip-flop in a pulse forming combination. The go ECS flip-flop sets on the trailing edge of a clock pulse and forms the leading edge of the request controller signal. The request controller flip-flop sets 50 nanoseconds later on the trailing edge of another clock pulse. The setting of the request controller flip-flop breaks the pulse forming AND gate and forms the trailing edge of the request controller signal. The request controller signal is required during a flag register operation since the ECS controller performs the flag operation internally. The Y register is equal to zero indicating no word count since a transfer of data is not required. The complemented flag register operation signal (5LF0 pak) prevents making the pulse forming AND function that generates the ECS request CMC signal since the CMC is not required.

The CMC sends the CMC accept signal when central memory is ready for the requested data transfer operation. The CMC accept signal proceeds through the receiver and latch register (3KR0 pak) and unconditionally sets the accept go flip-flop (5LF0 pak). The accept go flip-flop generates the go ECS signal that gates the P select circuit (CPLR 3.1), enables the buffer address circuit (CPLR 3.6), and sets the go ECS flip-flop (6LG0 pak).

The go ECS flip-flop sets at time T3 and sends its output signal to the request controller flip-flop. The request controller flip-flop is initially in a reset mode at the start of each transfer operation. The output signal of the go ECS flip-flop is ANDed with the complemented output signal of the request controller flip-flop in a pulse forming network that generates the request controller signal, unless an abort block signal is present. The request controller flip-flop sets at the next time T1 after the go ECS signal is available. The setting of the request controller flip-flop breaks the AND gate and ends the request controller signal. Since the go ECS signal is generated at time T3 and the request flip-flop set at the next time T1, the request coupler accept signal duration is 50 nanoseconds. The request controller pulse gates the address bits from the X and K registers into the address register (CPLR 3.0) for transmission to the ECS controller. The go ECS signal is also used by the buffer control (CPLR 3.4) and the end time control (CPLR 3.7) circuits.

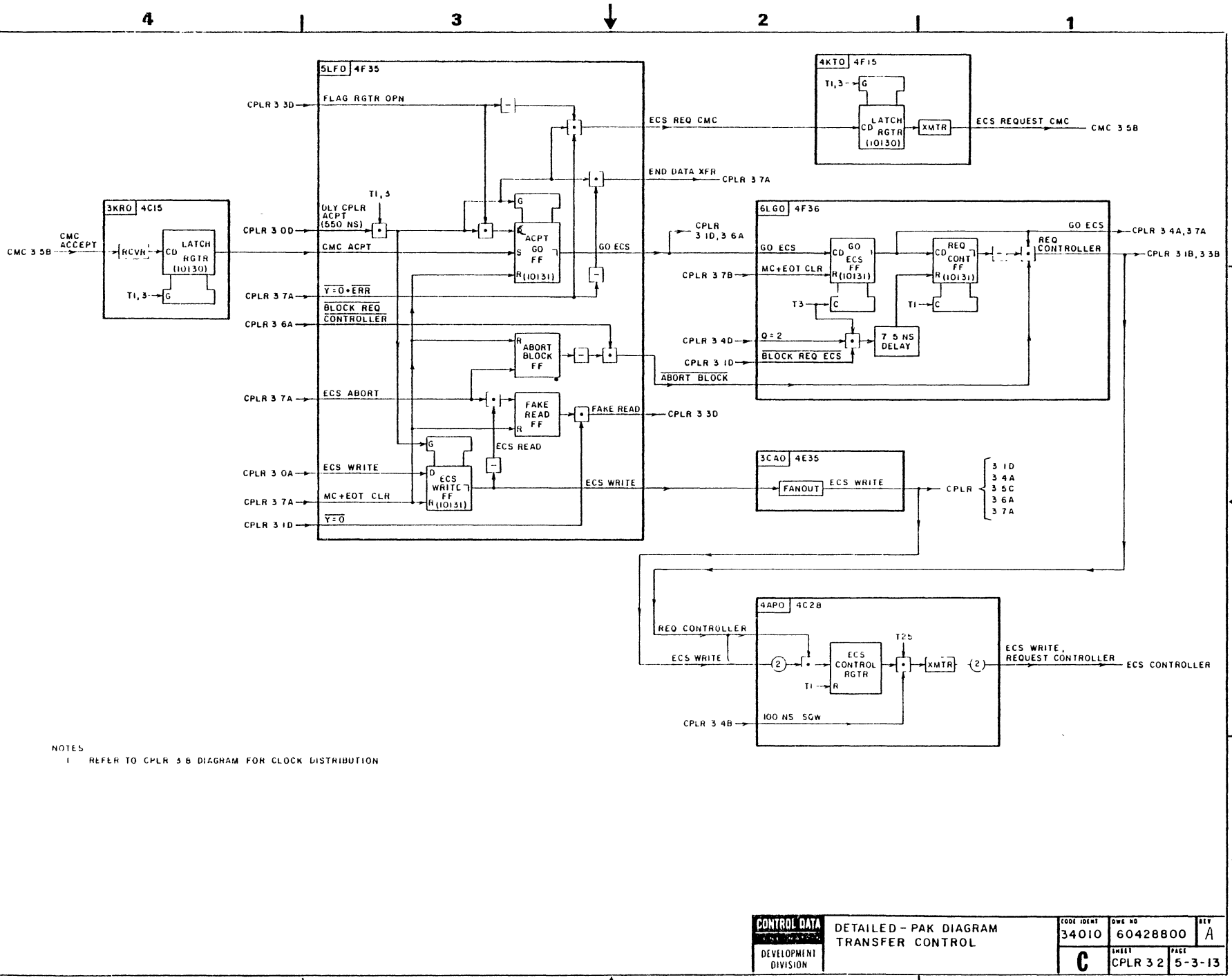
The request controller flip-flop is initially in the reset mode as the start of a transfer operation if the block request ECS signal is not present and Q does not equal two. The Q counter is in synchronization with the number of words written or read in ECS. When two words have been transferred, Q equals 2 and the request controller flip-flop is reset in preparation for the next go ECS signal. The not block request ECS signal gates the Q equals 2 signal to the delay circuit which resets the request controller flip-flop. During a read operation when the Y register (word count) indicates the last record is being read, the block request ECS signal is generated (CPLR 3.1). The block request ECS signal prevents the Q equals 2 signal from resetting the request controller flip-flop. Since the indication is that the last record of the transfer operation is being read, the ECS controller is no longer required and another request controller signal is not necessary.

The ECS controller sends an ECS abort signal to the coupler if an error is detected during a data transfer operation. The ECS abort signal sets the abort block flip-flop (5LF0 pak) to prevent the generation of another request controller signal. If the ECS abort signal occurs during an ECS read operation, the ECS abort signal sets the fake read flip-flop along with the abort block flip-flop. The fake read flip-flop generates the fake read signal that along with the Q counter keeps the go central memory flip-flop (CPLR 3.3) set long enough to transfer the data out of ECS. When the the transfer operation is complete, the word count in the Y register is zero and the Y equals zero signal breaks the AND gate on the output of the fake read flip-flop ending the fake read signal. The ending of the fake read signal causes the go central memory flip-flop to reset.

The CPU ECS write signal via the coupler interface circuits (CPLR 3.1) sets the ECS write flip-flop (5LF0 pak) for an ECS write operation. The ECS write signal from the ECS write flip-flop is fanned out (3CA0 pak) to appropriate circuits within the coupler requiring notification of an ECS write mode of operation. The ECS write signal is transmitted to the ECS controller via an ECS control register (4AP0 pak) and transmitters. A request controller signal gates the ECS write signal into the ECS control register. Requiring the request controller signal as a gate for the ECS write signal ensures the ECS controller that the request for this particular transfer operation is a write operation. The absence of the ECS write signal to the ECS write flip-flop indicates an ECS read operation. Therefore, the absence of the ECS write signal into the ECS control register at the time of the request coupler signal indicates to the ECS controller that the request is for a read operation. The ECS write flip-flop is cleared at the end of each transfer operation or by a master clear signal.

CPLR 3.2 TEST POINTS

Module	Location	Test Point	Description
3KR0	4C15	3 (T)	CMC Acpt
3KR0	4C15	1 (F)	CMC Acpt
5LF0	4F35	1 (T)	CMC Acpt
5LF0	4F35	4 (F)	MC + EOT CLR
5LF0	4F35	6 (T)	ECS Abort
5LF0	4F35	11 (T)	Flag Rgtr Opn
5LF0	4F35	3 (T)	Clock Time T1, 3
4KT0	4F15	11 (T)	ECS Req CMC
4KT0	4F15	2 (T)	Clock Time T1, 3
3CA0	4E35	8 (T)	ECS Write
3CA0	4E35	9 (T)	ECS Write
3CA0	4E35	10 (F)	ECS Write
3CA0	4E35	11 (F)	ECS Write
6LG0	4F36	12 (T)	Go ECS
6LG0	4F36	3 (T)	Abort Block
6LG0	4F36	14 (T)	Block Req ECS
6LG0	4F36	13 (T)	Clock Time T1
6LG0	4F36	2 (T)	Clock Time T3
4AP0	4C28	1	T25 (25 ns SQW)
4AP0	4C28	4 (T)	Clock Time T1
4AP0	4C28	6 (T)	ECS Write
4AP0	4C28	9	100 ns SQW
4AP0	4C28	11 (T)	Req Controller
4AP0	4C28	12 (F)	Req Controller
4AP0	4C28	14 (F)	ECS Write


L7031
H0-22
5LF0 4F35
FLAG RGTR OPN
CPLR 3 3D
ECS REQ CMC
END DATA XFR
CPLR 3 7A
DLY CPLR ACPT (550 NS)
T1, 3
CPLR 3 0D
CMC ACPT
GO ECS
CPLR 3 7A
Y=0+ERR
BLOCK REQ CONTROLLER
CPLR 3 6A
ABORT BLOCK FF
CPLR 3 7A
ECS ABORT
FAKE READ FF
FAKE READ
CPLR 3 3D
ECS READ
CPLR 3 0A
ECS WRITE
MC+EOT CLR
CPLR 3 7A
Y=0
CPLR 3 1D
ECS WRITE FF R(10131)
ECS WRITE
3KR0 4C15
CMC ACCEPT
CMC 3 5B
RCVR
LATCH RGTR (10130)
T1, 3
4KT0 4F15
T1, 3
LATCH RGTR (10130)
XMTR
ECS REQUEST CMC
CMC 3 5B
6LG0 4F36
CPLR 3 1D, 3 6A
GO ECS
MC+EOT CLR
CPLR 3 7B
GO ECS FF R(10131)
REQ CONT FF R(10131)
REQ CONTROLLER
GO ECS
CPLR 3 4A, 3 7A
CPLR 3 1B, 3 3B
T3
T1
CPLR 3 4D
Q=2
7.5 NS DELAY
CPLR 3 1D
BLOCK REQ ECS
ABORT BLOCK
3CA0 4E35
FANOUT
ECS WRITE
CPLR
3 1D
3 4A
3 5C
3 6A
3 7A
4AP0 4C28
REQ CONTROLLER
ECS WRITE
T25
ECS CONTROL RGTR
T1
XMTR
ECS WRITE, REQUEST CONTROLLER
ECS CONTROLLER
CPLR 3 4B
100 NS SQW
NOTES
1 REFER TO CPLR 3 8 DIAGRAM FOR CLOCK DISTRIBUTION
CONTROL DATA
DEVELOPMENT DIVISION
DETAILED - PAK DIAGRAM
TRANSFER CONTROL
CODE IDENT 34010
DWG NO 60428800
REV A
C
SHEET CPLR 3 2
PAGE 5-3-13

DETAILED-PAK DIAGRAM
ZERO PARITY CONTROL, FLAG REGISTER OPERATION AND GO CENTRAL

ZERO PARITY CONTROL

The CPU sends a force zero parity code that originates in the status and control register of the central processor when a test is required of the parity error detection networks. The code bits are received and passed through the latch register (3KR0 pak) at time T1, 3 to the force zero parity decoder (5LK0 pak). The decoder checks the bits and carries out the coded instructions. Normally both of the bits are zeros and an output signal from the decoder is not required.

If the force zero parity on address/word count at CPU is decoded, the force zero parity signal is transmitted via a latch register and transmitter (4KT0 pak) at the next time T1, 3 to the CPU. If a force zero parity on address to controller is detected, the decoder sends the force zero parity signal to a gating select circuit (4KQ0 pak). The force zero parity signal makes the AND gate in the select circuit that gates a logical zero as the ECS address parity bit through the select circuit to the ECS control register (4AP0 pak). The complemented force zero parity on ECS address signal breaks the AND gate in the select circuit and blocks the address parity bit that accompanied the address from the CPU. This address parity bit path through the select circuit is the path that the address parity bit takes for a normal transfer operation. The request coupler signal gates the ECS address parity bit, real or logical zero, into the ECS control register (4AP0 pak) to ensure the ECS address parity bit is associated with the proper address and request. The ECS control register transmits the ECS address parity bit to the ECS controller at the 100-nanosecond data transfer rate under control of the timing pulses. The ECS control register is reset each clock period to prepare it for the next ECS address parity bit. If the force zero parity decoder (5LK0 pak) detects a force zero parity on data at the controller, the signal is transmitted via an ECS control register (4AP0 pak) that does not require an input gating signal to the ECS controller. The ECS controller generates zero parity for the ECS parity check circuits.

ECS RESPONSE REGISTER

The ECS controller sends a controller accept signal to the coupler for every successful transfer of a record and also to indicate that it is ready for another record. The controller accept signal is received and loaded into the ECS response register (4AP0 pak). The ECS response register sends the controller accept signal to various coupler locations including the go central circuit (5LB0 pak). The coupler accept signal along with the not stop go central signal (CPLR 3.1) and the not flag register operation signal set the go central memory flip-flop. The go central memory flip-flop generates the go central signal that is necessary for the coupler circuits to perform any data transfer operation.

The ECS controller sends a controller abort signal to the coupler if the controller detects an error during the data transfer operation. The controller abort signal is received and loaded into the ECS response register. The ECS response register sends a controller abort signal to the error register (CPLR 3.7) for determination to immediately end the data transfer operation in the case of an ECS write operation or to continue the data transfer operation to its normal conclusion in the case of an ECS read operation.

GO CENTRAL AND FLAG REGISTER OPERATION

The controller accept signal sets the go central memory flip-flop (5LB0 pak) if the flag register operation flip-flop is not set and the word count equals zero flip-flop (CPLR 3.1) that generates the stop go central signal is not set. The go central signal, indicating that the ECS controller has accepted the transfer request, fans out to appropriate coupler circuits. The go central signal allows data transfer to begin between the ECS and CMC via the coupler. The go central memory flip-flop is also set when the initial go ECS and ECS write signals result in the generation of the force set go central signal. This initial go central signal results in a bank initiate signal that transfers to CMC before the ECS controller responds with its first controller accept signal. This is required since the ECS controller is ready to accept data immediately with its acceptance of the transfer request while it takes longer for the CMC to get data out of central memory. The P equals zero signal, indicating that all the words of the active record have transferred, resets the go central memory flip-flop. This requires the ECS controller to generate a controller accept signal after receipt of each record to set the go central memory flip-flop again.

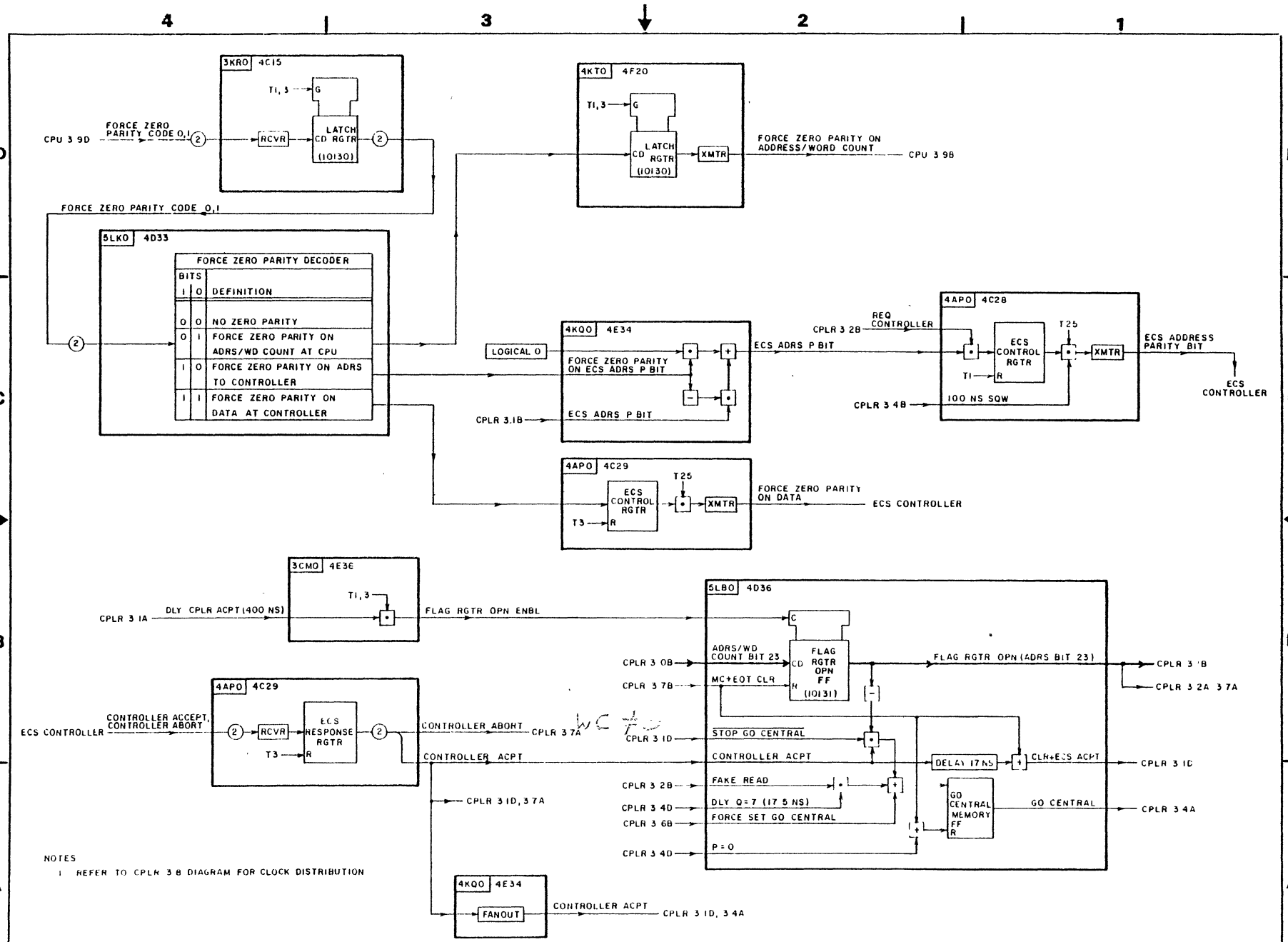
The 17.5-nanosecond delayed Q equals 7 signal and the fake read signal are ANDed to set the go central memory flip-flop should an ECS abort occur. The ECS abort causes the generation of the stop go central signal resulting in the clearing of the go central memory flip-flop at the end of the record. The fake read signal is generated only during a read ECS operation. The go central memory flip-flop remains set allowing the transfer of all zeros to CMC for the remaining words of the ECS read transfer operation.

The controller accept signal is delayed, and then ORed with the master clear or end of transfer clear signal to generate a reset signal for the LAK register (CPLR 3.1). This signal resets the LAK register containing the lower 3 bits of the address after each successful transfer of a record.

The flag register operation flip-flop is set if address bit 23 is set at the time the flip-flop is clocked by the flag register operation enable signal. This signal coincides with the time the address arrives from the CPU. The flag register operation flip-flop output signal requests the ECS controller and passes the flag operation function on to the ECS controller. Address bits 20 through 22 of the associated address are interpreted by the ECS controller as to what is required during the flag register operation function. The ECS controller requires no information other than the address with bit 23 set. The coupler sends no request for information to the CMC. The output signal of the flag register operation flip-flop is inverted and prevents the controller accept signal from setting go central memory flip-flop and allowing a data transfer to take place. Since no data transfer takes place during a flag register operation, the flag register operation flip-flop depends on the clear signal for the next transfer operation request to reset the flip-flop.

CPLR 3.3 TEST POINTS

Module	Location	Test Point	Description
3KR0	4C15	5 (T)	Force Zero Parity Code 0
3KR0	4C15	2 (T)	Force Zero Parity Code 1
3KR0	4C15	7 (T)	Clock Time T1, 3
4KT0	4F20	11 (T)	Force Zero Parity on Adrs/Wd Count
4KT0	4F20	2 (T)	Clock Time T1, 3
4KQ0	4E34	13 (T)	Force Zero Parity on ECS Adrs P Bit
4AP0	4C28	13 (F)	ECS Adrs P Bit
4AP0	4C28	11 (T)	Req Controller
4AP0	4C28	4 (T)	Clock Time T1
4AP0	4C28	9	100 ns SQW
4AP0	4C28	1	T25 (25 ns SQW)
4AP0	4C28	14 (F)	ECS Write
4AP0	4C29	7 (T)	Force Zero Parity on Data at Controller
4AP0	4C29	13 (F)	Controller Acpt
4AP0	4C29	12 (F)	Controller Abort
5LB0	4D36	2 (F)	MC + EOT CLR
5LB0	4D36	10 (T)	Dly Q = 7
5LB0	4D36	11 (T)	Fake Read
5LB0	4D36	12 (T)	Controller Acpt
5LB0	4D36	14 (T)	$\overline{\text{Stop Go Central}}$
5LB0	4D36	13 (F)	P = 0
5LB0	4D36	9 (T)	Adrs/Wd Count Bit 23



CONTROL DATA DEVELOPMENT DIVISION	DETAILED-PAK DIAGRAM ZERO PARITY CONTROL, FLAG REGISTER OPERATION AND GO CENTRAL	CODE IDENT 34010	DWG NO 60428800	REV A
		SIZE C	SHEET CPLR 3 3	PAGE 5-3-15

DETAILED-PAK DIAGRAM
CMC TRANSFER CONTROL, P AND Q COUNTERS AND WRITE BUFFER CONTROL

TRANSFER CONTROL (WRITE)

The ECS controller sends an accept signal to the coupler to indicate that the initial request has been accepted. When the coupler receives the accept signal, it generates the go central signal (CPLR 3.3). The go central signal is fanned out (3CA0 pak) to the appropriate coupler circuits. One of the go central signals is ANDed with the ECS write signal (4LH7 pak) to set the 300-nanosecond shift register and the ECS continue request flip-flop at time T1. The ECS continue request flip-flop transmits the ECS continue request signal (4KT0 pak) to the CMC to reserve a memory bank in central memory 400 nanoseconds ahead of each successive bank initiate signal. The output of the 300-nanosecond shift register sets the bank initiate flip-flop at the next time T1 (300-nanosecond shift plus 100-nanosecond clock period equals 400 nanoseconds). The 100-nanosecond square wave that gates the data into the data holding register in preparation for transmission to the ECS controller also gates the bank initiate signal to the latch register (4KT0 pak) for transmission to the CMC. The bank initiate signal arrives at the CMC 400 nanoseconds after the continue request signal to initiate the addressed bank in central memory to send its data to the coupler buffer.

TRANSFER CONTROL (READ)

During an ECS read operation, a go central signal from the fanout (3CA0 pak) is gated into the 1100-nanosecond delay chain (5KS0 pak) by the ECS read (not ECS write) signal. A further delay occurs as the signal is passed through two 100-nanosecond delay flip-flops (4LH7 pak) to the 300-nanosecond shift register and the ECS continue request flip-flop. The ECS continue request signal transfers to the CMC while the 300-nanosecond shift register delays the setting of the bank initiate flip-flop for an additional 300 nanoseconds plus one clock period. The total delay in an ECS read operation before a bank initiate signal reaches the CMC is at least 1700 nanoseconds. This amount of time is required for the ECS to get the data out of memory after it has accepted the transfer operation request. The CMC is not required until the memory cycle is complete and data transfer starts. Once the transfer starts, it continues at the transfer rate of one word every 100 nanoseconds.

P COUNTER

The selected P register bits 0 through 2 are selected by the P select circuit (CPLR 3.1) for the P counter. The P counter (6LG0 pak) keeps track of the number of words in the record being transferred. The selection circuit therefore provides the K register output (lower 3 bits of address) which is normally a 7 as the input to the P counter until the Y register output (word count) is equal to or less than the K register output. When the last record is in the process of being transferred, the Y minus 1 signal is supplied to the P counter as the number of words in the record.

The P counter is loaded with the selected P register bits 0 through 2 when the counter is in the preset mode. The go central signal, indicating an ECS controller accept, sets the one-shot flip-flop at clock time T1, 3. This forces the P counter into a decrement mode and allows the count to be decremented by one every clock period. The output of the P counter is monitored by the P test circuit until P equals 0. When P equals 0, the last word of the record has transferred and the P test circuit sends the P equals 0 signal to reset the go central flip-flop (CPLR 3.3). The go central flip-flop requires the ECS controller to send back an accept signal to set it again. The ending of the go central signal returns the P counter to the preset mode and allows the loading of the word count of the next record. The process continues until the last word of the last record is transferred.

Q COUNTER

The Q counter (5LG0 pak) is reset to zero at the same time the P counter goes to a decrement mode. This is accomplished by the one-shot flip-flop not being set by the go central signal until time T1, 3. The Q counter increments once each clock time T1. The Q test circuit outputs a signal when Q equals 2. During an ECS write operation, the Q equals 2 signal indicates that two words have transferred from CMC to the coupler buffer. The Q equals 2 signal sets write block request controller flip-flop (CPLR 3.6) which allows the first request controller signal of the transfer operation to transfer to the ECS controller. After the Q equals 2 signal has once set the write block request controller flip-flop, it is not required again until after an end of transfer has taken place. However, the Q counter is continually reset for each record and incremented for each word. The Q equals 2 signal also resets the request controller flip-flop (CPLR 3.2) to allow the generation of the next request for the ECS controller.

The Q test circuit also generates a Q equals 7 signal that in combination with the fake read signal (CPLR 3.3) sets the go central flip-flop. This keeps the go central flip-flop set so that all zeros are written into CM for the remaining words of an ECS read operation if an ECS abort occurs.

P DELAY COUNTER

The P holding register (4LL7 pak) receives the selected P register bits that contain the word count of the next record. These bits are clocked into the holding register by the combination of the delayed go ECS, controller accept, and clock time T1 signals. The selected P register bits enter the P delay counter when the controller accept signal forces the counter into a preset mode. When the controller accept signal ends, the counter goes into a decrement mode. The counter is decremented each clock time T1 during an ECS write operation. When the counter reaches zero, the P delay test circuit outputs a signal to reset the write data flip-flop at the end of the record.

The write data flip-flop is set by the ECS write signal and the controller accept signal from the initial or previous record. The write data flip-flop output signal is delayed 500 nanoseconds (5KS0 pak) and ANDed with the 100-nanosecond sqaure wave (4LH7 pak) to generate the load data signal. The load data signal is fanned out to gate the data from the coupler buffer (CPLR 3.5) into the data holding register. The data is then transmitted to the ECS controller. The buffer address circuit uses a complemented load data signal for synchronization of the address to the data (CPLR 3.6). The 500-nanosecond delay (5KS0 pak) affects the write data signal on the first word of the first record only in the transfer operation. The timing of the clock pulse to the reset time of the write data flip-flop is such that the 500-nanosecond delay flip-flop does not see the signal drop at the end of the record unless a a gap occurs to delay the controller accept signal. A delay caused by a gap would still only delay the output from producing another load data signal for as long as the gap occurred.

CPLR 3.4 TEST POINTS

Module	Location	Test Point	Description
4LL7	4F19	3 (T)	ECS Write
4LL7	4F19	12 (T)	P Bit 0
4LL7	4F19	9 (T)	P Bit 1
4LL7	4F19	10 (T)	P Bit 2
4LL7	4F19	13 (T)	Dly P Rgtr Bit 0
4LL7	4F19	11 (T)	Dly P Rgtr Bit 1
4LL7	4F19	14 (T)	Dly P Rgtr Bit 2
4LL7	4F19	2 (T)	P = 0
3CA0	4F35	3 (T)	Go Central
3 CA0	4F35	1 (F)	Go Central
3 CA0	4F35	2 (F)	Go Central
3CA0	4E35	6 (T)	Load Data
3CA0	4E35	5 (F)	Load Data
3CA0	4E35	4 (F)	Load Data
3CA0	4E35	13	100 ns SQW
3CA0	4E35	14	100 ns SQW
6LG0	4F36	6 (T)	P Rgtr Bit 0
6LG0	4F36	4 (T)	P Rgtr Bit 1
6LG0	4F36	5 (T)	P Rgtr Bit 2
6LG0	4F36	10 (T)	Go Central
4LH7	4F37	10	100 ns SQW
4LH7	4F37	3 (T)	Clock Time T3
4LH7	4F37	8 (T)	Bank Initiate
4LH7	4F37	7 (T)	ECS Write
4LH7	4F37	4 (T)	Clock Time T1
4LH7	4F37	5 (T)	Go Central
4LH7	4F37	9 (T)	Set ECS Cont Req
4KT0	4F15	7 (T)	ECS Bank Initiate
4KT0	4F15	6 (T)	ECS Continue Req
4KT0	4F15	2 (T)	Clock Time T1, 3
5KS0	4E33	14	100 ns SQW
5KS0	4E33	10	100 ns SQW
5KS0	4E33	3	100 ns SQW
5KS0	4E33	1	100 ns SQW
5KS0	4E33	2	100 ns SQW

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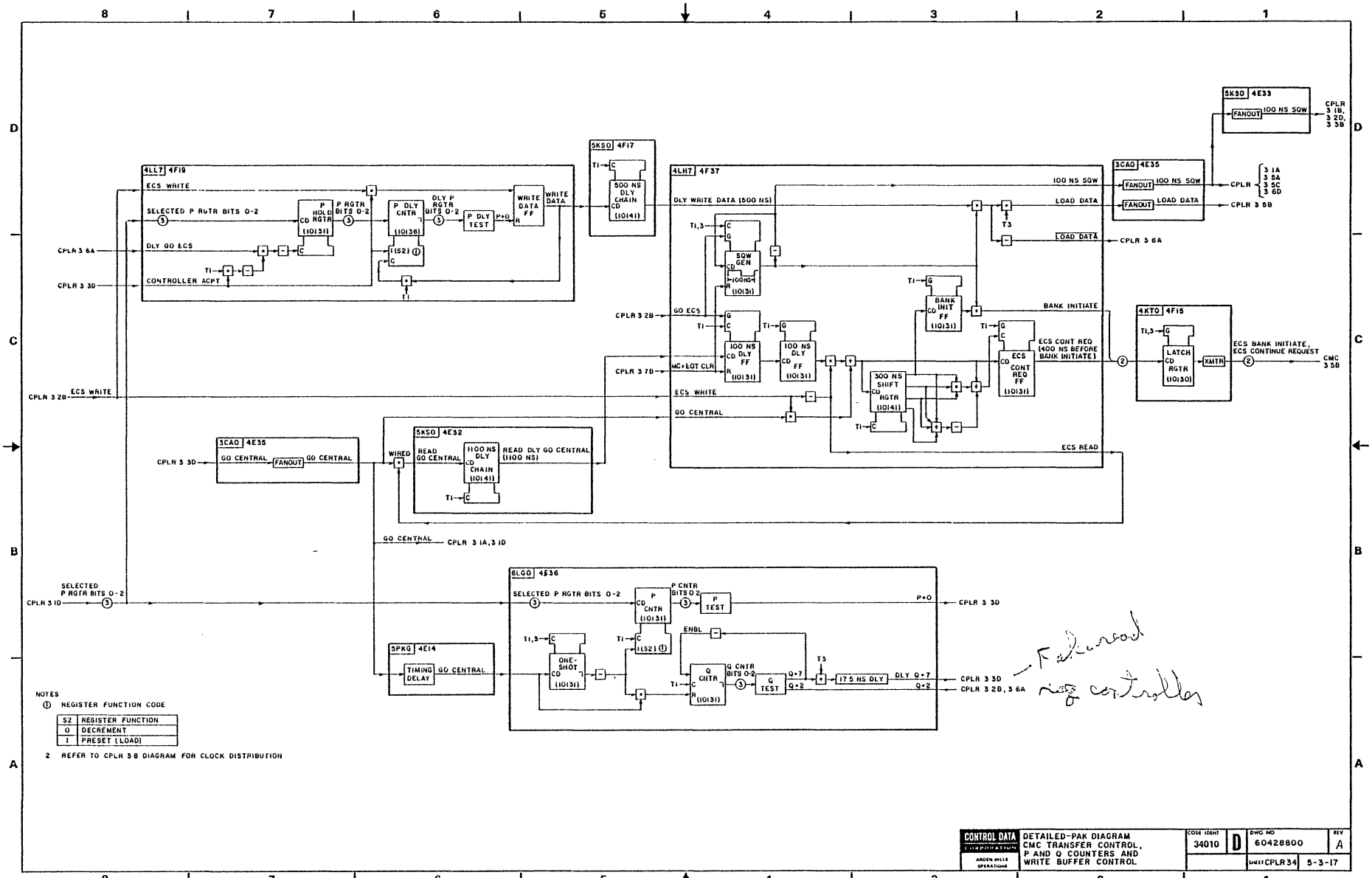
4LL7 4F19
ECS WRITE
SELECTED P RGTR BITS 0-2
P HOLD RGTR (10131)
P RGTR BITS 0-2
P DLY CNTR (10136)
DLY P RGTR BITS 0-2
P DLY TEST
P+0
WRITE DATA FF
WRITE DATA
DLY GO ECS
CPLR 3 6A
CONTROLLER ACPT
CPLR 3 3D
5KS0 4F17
500 NS DLY CHAIN CD (10141)
4LH7 4F37
DLY WRITE DATA (500 NS)
100 NS SQW
LOAD DATA
T3
SQW GEN (10131)
100NS
GO ECS
CPLR 3 2B
100 NS DLY FF (10131)
MC+EOT CLR
CPLR 3 7B
BANK INIT FF (10131)
BANK INITIATE
ECS CONT REQ FF (10131)
ECS CONT REQ (400 NS BEFORE BANK INITIATE)
300 NS SHIFT RGTR (10141)
ECS WRITE
GO CENTRAL
ECS READ
5KS0 4E33
FANOUT
CPLR 3 1B, 3 2D, 3 3B
3CA0 4E35
CPLR 3 1A 3 5A 3 5C 3 6D
CPLR 3 5B
CPLR 3 6A
4KT0 4F15
LATCH CD RGTR (10130)
XMTR
ECS BANK INITIATE, ECS CONTINUE REQUEST
CMC 3 5B
3CA0 4E35
GO CENTRAL
5KS0 4E32
WIRED
READ GO CENTRAL
1100 NS DLY CHAIN CD (10141)
READ DLY GO CENTRAL (1100 NS)
GO CENTRAL
CPLR 3 1A, 3 1D
6LG0 4E36
SELECTED P RGTR BITS 0-2
SELECTED P RGTR BITS 0-2
CPLR 3 1D
P CNTR BITS 0-2
P CNTR (10131)
P TEST
P+0
CPLR 3 3D
ENBL
ONE-SHOT (10131)
Q CNTR (10131)
Q CNTR BITS 0-2
Q TEST
Q+7
Q+2
175 NS DLY
DLY Q+7
CPLR 3 3D
CPLR 3 2B, 3 6A
5PK0 4E14
TIMING DELAY
GO CENTRAL
NOTES
① REGISTER FUNCTION CODE
S2 | REGISTER FUNCTION
0 | DECREMENT
1 | PRESET (LOAD)
2 REFER TO CPLR 3 8 DIAGRAM FOR CLOCK DISTRIBUTION
CONTROL DATA CORPORATION
ARDEN HILLS OPERATIONS
DETAILED-PAK DIAGRAM
CMC TRANSFER CONTROL, P AND Q COUNTERS AND WRITE BUFFER CONTROL
CODE IDENT 34010
D
DWG NO 60428800
REV A
SHEET CPLR 34
5-3-17

H0-28

DETAILED-PAK DIAGRAM
DATA PATHS

WRITE DATA PATH

The CM read data to be written into ECS is received and enters the latch register (3KR0 pak) at time T1, 3. The 60 bits of data and a parity bit are accompanied by a data on line signal referred to as a go ECS in the CMC. The data on line signal is clocked by a 100-nanosecond square wave in the 3KF0 pak. The resultant output signal is a 50-nanosecond write strobe and a complemented write strobe once every 100 nanoseconds. The complemented write strobe provides the buffer address control (CPLR 3.6) with a timing pulse. The write strobe signal is fanned out (3FX0 pak) to gate the data and the parity bit into the data buffer 16-word random access memory (RAM) at the address designated by the buffer control address bits (5PKG pak).

The 16-word RAM buffer stores the data coming from the CMC that the ECS controller is not ready for. The first request for the ECS controller is blocked to give the CMC a headstart as the ECS controller is able to accept data as soon as the request is made. The 16-word RAM stores the first two words from CM according to the buffer address. The coupler generates a request for the ECS coupler only after the successful transfer of two words from the CMC. If the controller can do a coupler request at this time, it sends an accept signal to the coupler which starts the transfer of data. If the ECS controller cannot take the request and does not send an accept back to the coupler, the next word from CMC is stored in the next address of the 16 word RAM. The minimum number of words in the 16-word RAM before a transfer begins is two, while a maximum of 16 depends upon when the ECS controller sends back an accept signal. The initial blocked request for the ECS controller is due to the ability of the ECS controller to accept data sooner than the CMC can get the data out of central memory. The CMC therefore, operates the CM ahead of, and semi-independent of ECS. This allows the 16-word RAM buffer to store data and have data transferred out once every 100 nanoseconds which is as fast as the ECS controller can accept data from the coupler for writing in ECS. The buffer input address which is incremented by the complemented write strobe controls the data location within the 16-word RAM. The data in the 16-word RAM is transferred out on a first-in first-out basis by the buffer output address. The 100-nanosecond square wave, 50 nanoseconds of which is for the input address and the other 50 nanoseconds for the output address accomplishes address control. The ECS accept signal indicating the ECS controller is ready for the first or next word controls the incrementing of the output address. The data output from the 16-word RAM is in sequence and at the ECS transfer rate.

The buffer CM read data enters the data holding register (4AP0 pak) by the presence of the load data signal. The load data signal is the result of the ECS write signal and the controller accept signal that operates the P delay counter for an ECS write condition. In order to get a load data signal, the ECS controller must generate the initial accept or an accept due to a successful transfer of the previous word. The transmit data signal and clock time T25 gate the data to the transmitter. The transmit data signal is a result of the ECS write signal gated by the 100-nanosecond square wave.

The CM read data parity bit also passed through a 16-word RAM buffer and holding register in synchronization with the associated data word.

A section of the 16-word RAM parity buffer generates the go signal for the ECS controller that accompanies each data word by having that section full of logical ones. Therefore, every output word selected by an output address is accompanied by a go signal indicating that data is on the line to the ECS controller.

READ DATA PATH

The ECS read data to be written into CM is received and enters the data holding registers (4AP0 pak) unconditionally. No gating or clock signals are required to enter the data. The data transfers immediately to a latch register in the data transmitters (4KT0 pak) and is clocked at time T1 to the transmitter. The data parity bit accompanies the data through the coupler along a similar path.

If an ECS abort occurs during a read operation, the ECS controller transfers the remaining words of the transfer operation as all zeros. The coupler receives the ECS abort signal and generates the forced parity bit signal (3AN0 pak) to accompany the remaining words made up of all zeros in the transfer operation.

If an error occurs in the ECS, the ECS controller sends the appropriate error signal to the coupler. The ECS controller parity error or ECS bank parity error signals enter the holding register on the 4AP0 pak. The holding register sends the error signals to the coupler error register (CPLR 3.7) and are eventually coded and transferred to the status and control registers for error identification.

CPLR 3.5 TEST POINTS

Module	Location	Test Point	Description
3KR0	4C07-14	3 (T)	Data (CM Read) Bit N
3KR0	4C07-14	5 (T)	Data (CM Read) Bit N +1
3KR0	4C07-14	2 (T)	Data (CM Read) Bit N +2
3KR0	4C07-14	6 (T)	Data (CM Read) Bit N +3
3KR0	4C07-14	13 (T)	Data (CM Read) Bit N +4, Data Parity
3KR0	4C07-14	9 (T)	Data (CM Read) Bit N +5
3KR0	4C07-14	12 (T)	Data (CM Read) Bit N +6, Data On Line
3KR0	4C07-14	8 (T)	Data (CM Read) Bit N +7
3KR0	4C07-14	7 (T)	Clock Time T1,3
5PKG	4D08-14, 4E07-14	3 (T)	Data Bit N
5PKG		2 (T)	Data Bit N +1
5PKG		10 (T)	Data Bit N +2
5PKG		9 (T)	Data Bit N +3
5PKG		7 (T)	Buffer Data Bit N
5PKG		6 (T)	Buffer Data Bit N +1
5PKG		13 (T)	Buffer Data Bit N +2
5PKG		14 (T)	Buffer Data Bit N +3
5PKG		1 (T)	Adrs Bit 0
5PKG		11 (T)	Adrs Bit 1
5PKG		8 (T)	Adrs Bit 2
5PKG		5 (T)	Adrs Bit 3
5PKG	4D08-14, 4E07-14	4 (T)	Write Strobe
5PKG	4D07	3 (T)	Data (CM Read) P Bit
5PKG	4D07	7 (T)	Buffer Data P Bit
5PKG	4D07	4 (T)	Write Strobe
5PKG	4D07	6 (T)	Go
5PKG	4D07	1 (T)	Adrs Bit 0
5PKG	4D07	11 (T)	Adrs Bit 1
5PKG	4D07	8 (T)	Adrs Bit 2
5PKG	4D07	5 (T)	Adrs Bit 3
4AP0	4D25-27, 4E22-27, 4F22-27	13 (F)	Data Holding Rgtr Bit N
4AP0		12 (F)	Data Holding Rgtr Bit N +1
4AP0		3 (F)	Data Holding Rgtr Bit N +2
4AP0		14 (F)	Data Holding Rgtr Bit N +3
4AP0		9	Transmit Data (100 ns SQW)
4AP0		11 (T)	Load Data
4AP0		4 (T)	Clock Time T2
4AP0		2 (T)	Data (ECS Write) Bit N
4AP0		5 (T)	Data (ECS Write) Bit N +1
4AP0		8 (T)	Data (ECS Write) Bit N +2
4AP0	4D25-27, 4E22-27, 4F22-27	10 (T)	Data (ECS Write) Bit N +3
4AP0	4D24	13 (F)	Controller PE/Data (CM Read) P Bit
4AP0	4D24	12 (F)	Go
4AP0	4D24	3 (F)	ECS Bank PE
4AP0	4D24	14 (F)	Data (ECS Write) Parity
4AP0	4D24	9	Transmit Data (100 ns SQW)
4AP0	4D24	11 (T)	Load Data
4AP0	4D24	4 (T)	Clock Time T2
4AP0	4D24	10 (T)	Data (ECS Write) Parity
4AP0	4D24	5 (T)	Go

CPLR 3.5 TEST POINTS (Cont'd)

Module	Location	Test Point	Description	Module	Location	Test Point	Description
4KT0	4F07-14	9 (T)	Data (CM Write) Bit N	5KS0	4E32	3	Transmit Data (100 ns SQW)
4KT0	4F07-14	7 (T)	Data (CM Write) Bit N +1	5KS0	4E32	10	Transmit Data (100 ns SQW)
4KT0	4F07-14	11 (T)	Data (CM Write) Bit N +2	5SK0	4E32	14	Transmit Data (100 ns SQW)
4KT0	4F07-14	6 (T)	Data (CM Write) Bit N +3	3FX0	4D15	2 (F)	T1 • Write Strobe
4KT0	4F07-14	10 (T)	Data (CM Write) Bit N +4, Parity	3FX0	4D15	3 (F)	T1 • Write Strobe
4KT0	4F07-14	3 (T)	Data (CM Write) Bit N +5	3FX0	4D15	6 (F)	T1 • Write Strobe
4KT0	4F07-14	8 (T)	Data (CM Write) Bit N +6	3FX0	4D15	10 (F)	T1 • Write Strobe
4KT0	4F07-14	5 (T)	Data (CM Write) Bit N +7	3FX0	4D15	11 (F)	T1 • Write Strobe
4KT0	4F07-14	2 (T)	Clock Time T1	3FX0	4D15	13 (F)	T1 • Write Strobe
3KF0	4F16	14 (T)	Data On Line	3FX0	4D15	7 (T)	Clock Time T1
3KF0	4F16	1	100 ns SQW	3FX0	4D15	14 (T)	Clock Time T1
5KS0	4E32	1	Transmit Data (100 ns SQW)	3FX0	4D15	1 (T)	Write Strobe
5KS0	4E32	2	Transmit Data (100 ns SQW)				

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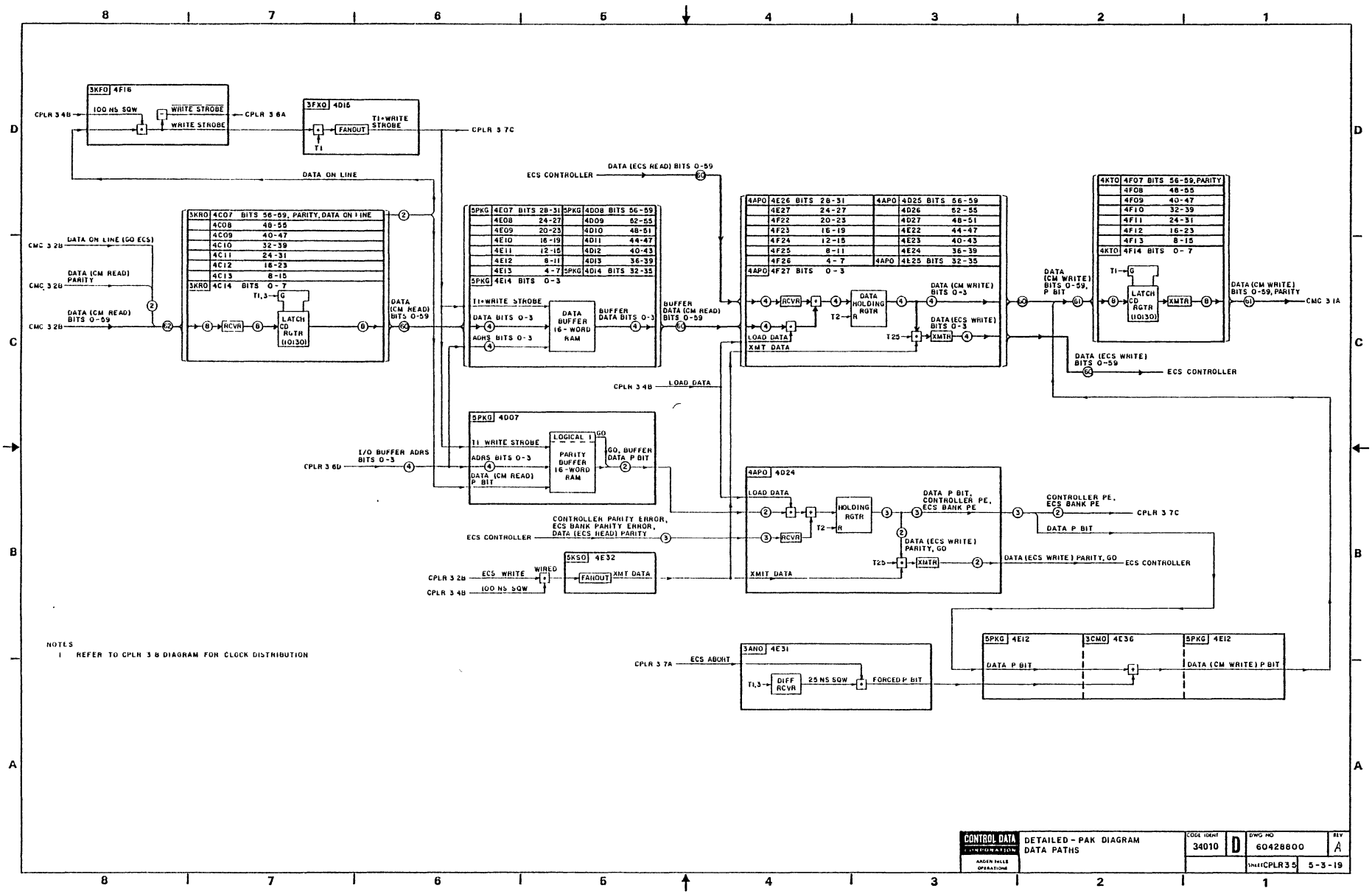


NOTES

1 REFER TO CPLR 3 8 DIAGRAM FOR CLOCK DISTRIBUTION

CONTROL DATA CORPORATION ARDEN HILLS OPERATIONS	DETAILED - PAK DIAGRAM DATA PATHS	CODE IDENT 34010	D	DWG NO 60428800	REV A
				SHEET CPLR 3 5	5-3-19

DETAILED-PAK DIAGRAM
BUFFER ADDRESS

BUFFER ADDRESS

The buffer address generates the I/O addresses for the buffer 16-word RAM in the CM read data path (CPLR 3.5). The generation of the buffer address requires the go ECS signal that is generated as a result of the coupler accept signal (CPLR 3.2). The go ECS signal is ANDed with the complemented output signal of the one-shot in a pulse forming combination. The go ECS signal makes the AND gate forming the leading edge of the pulse. The go ECS signal at the next clock time T3 sets the one-shot. This could be 100 nanoseconds after the arrival of the go ECS signal depending upon the relationship of the go ECS signal to time T3. When the one-shot sets, its signal breaks the AND gate forming the trailing edge of the pulse. This pulse provides an input signal to functional control input S2 of the I/O address registers (3LA0 pak) that generate the buffer address. The output signal of the pulse forming AND gate is also complemented to break two AND gates. The complemented outputs of these AND gates provide input signals to input S1 of the I/O address registers. With the signals as described at this time, the I/O address registers are in a preset mode and load all zeros. When the one-shot sets at time T3, the signal from the pulse forming AND gate ends removing the input signals to S1 and S2. This forces the I/O address registers into a hold mode. The write strobe signal, which is generated each time a word arrives from CMC, controls the input signal to S2 of the input address. The write strobe forces the input address register into the increment mode for each word. The clock pulse increments the input address register at the transfer rate of once every 100 nanoseconds. The address is incremented each time a write strobe occurs until all 16 addresses have been used; then the address register returns to zero and starts all over again.

The output address register operates in the same manner as the input address register except that the load data signal forces the output address register into the increment mode. The load data signal is the result of the controller accept signal. The controller accept signal occurs once every 100 nanoseconds after the initial ECS request is accepted. The initial ECS request is not generated until at least two words have arrived from the CMC. The incrementing of the I/O address register continues each clock time there is a write strobe or load data for their respective registers until the transfer operation is complete. The next go ECS signal for the next transfer operation results in loading of all zeros into the I/O address registers to begin the process all over again.

The address bits from the input address register are complemented externally (5PKG pak) while the bits from the output address register are complemented internally (3LA0 pak). The 100 nanosecond square wave signal (3KF0 pak) gates the complemented I/O address bits so that every 50 nanoseconds either the input or the output address is fanned out (3FX0 pak) to the data path buffer 16-word RAM (CPLR 3.5).

FORCE SET GO CENTRAL CONTROL

The CPU request for an ECS write operation requires the coupler to generate request signals for the ECS controller and the CMC. The ECS controller is capable of accepting data as soon as the request for use is accepted. Since it takes more time for the CMC to get data out of central memory and to the coupler, the force set go central circuit (4LL7 pak) generates a signal to initiate the CMC ahead of the ECS controller.

The go ECS signal that is a result of the coupler accepting the CPU request for a transfer operation is ANDed in a pulse forming combination with the output of the one-shot and ECS write signal. The pulse ends when the one-shot sets at time T3, which then sets the force set flip-flop. The flip-flop sends the force set go central signal to set the go central flip-flop (CPLR 3.3). The go central flip-flop causes the generation of the first bank initiate signal for the CMC. The coupler has not yet issued a request for the ECS controller to perform a transfer operation. The ECS controller accepting the request for a transfer operation is the normal control signal that sets the go central flip-flop during a transfer operation.

WRITE BLOCK REQUEST CONTROLLER CONTROL

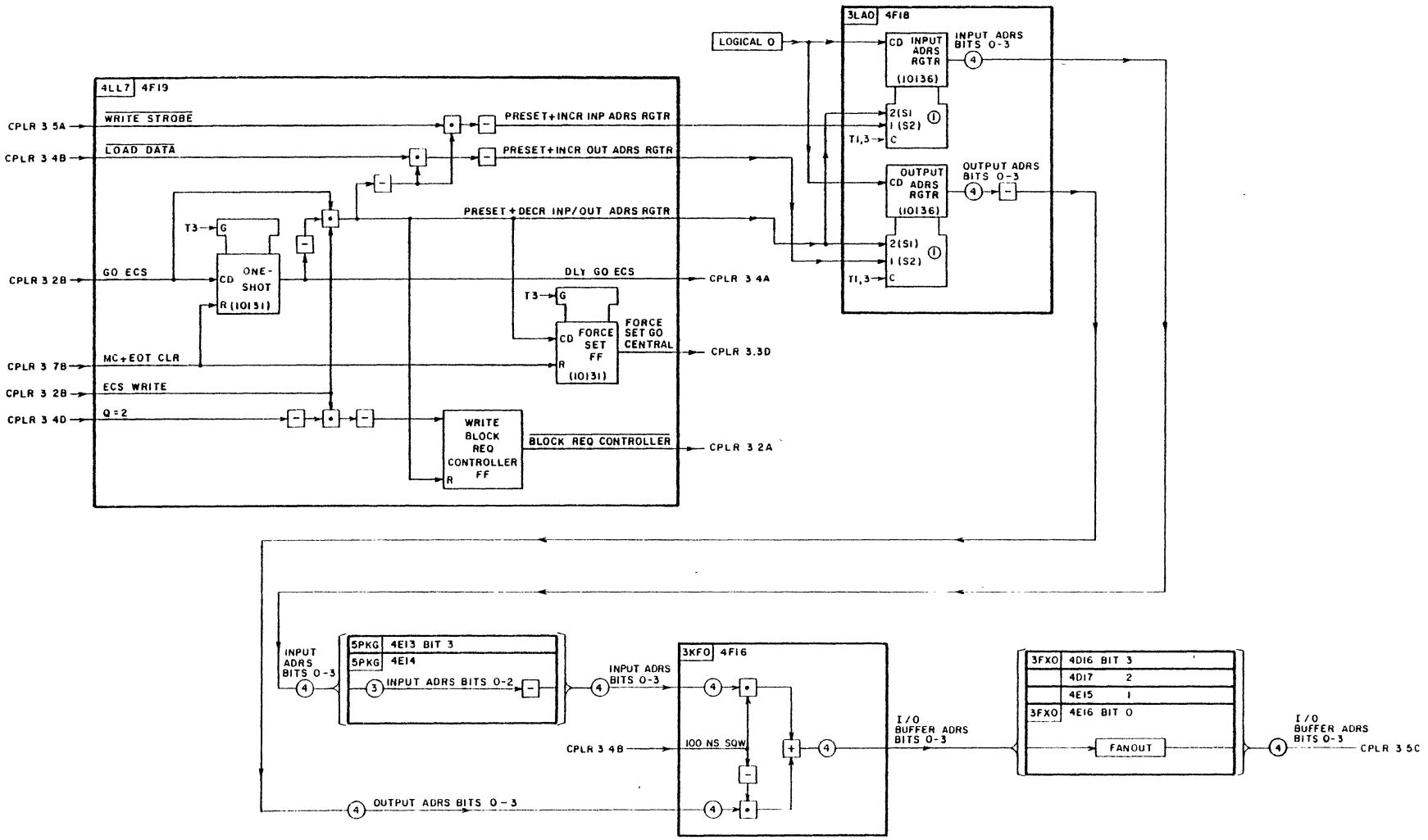
The write block request controller circuit (4LL7 pak) generates the signal that prevents the coupler from generating a request for the ECS controller until at least two words from the CMC are in the coupler data path buffer.

The same pulse that sets the force set go central flip-flop resets the write block request controller flip-flop. The reset mode of the flip-flop generates a block request controller signal that prevents the coupler from sending the first request controller signal (CPLR 3.2) to the ECS controller. The coupler does send a request to the CMC at this time. When two words have transferred into the data path buffer from the CMC, the Q counter which is equal to the P counter (word count) sends the Q equals 2 signal. The Q equals 2 signal is complemented, ANDed with the ECS write signal, and the result complemented to set the write block request controller flip-flop. The setting of the write block request controller flip-flop removes the block request controller signal. This now allows the coupler to request the ECS controller as there are at least two words of data in the data path buffer and possibly more on the way.

During a read ECS transfer operation, a delay of the ECS request controller signal is not required. The absence of the ECS write signal sets the write block request controller flip-flop immediately as the Q equals 2 signal is not required. Since the flip-flop is set, a block request controller signal is not present, the coupler is allowed to generate the request for the ECS coupler.

CPLR 3.6 TEST POINTS

Module	Location	Test Point	Description
4LL7	4F19	7 (T)	Clock Time T3
4LL7	4F19	5 (F)	Load Data
4LL7	4F19	6 (F)	MC + EOT CLR
4LL7	4F19	3 (T)	ECS Write
3LA0	4F18	1 (T)	Logical 0
3LA0	4F18	2 (T)	Logical 0
3LA0	4F18	11 (T)	Output Adrs Bit 0
3LA0	4F18	8 (T)	Output Adrs Bit 1
3LA0	4F18	9 (T)	Output Adrs Bit 2
3LA0	4F18	10 (T)	Output Adrs Bit 3
3LA0	4F18	7 (T)	Clock Time T1, 3
3KF0	4F16	1	100 ns SQW
3KF0	4F16	8 (F)	Input Adrs Bit 0
3KF0	4F16	7 (F)	Input Adrs Bit 1
3KF0	4F16	6 (F)	Input Adrs Bit 2
3KF0	4F16	13 (F)	Input Adrs Bit 3
3KF0	4F16	10 (F)	Output Adrs Bit 0
3KF0	4F16	4 (F)	Output Adrs Bit 1
3KF0	4F16	5 (F)	Output Adrs Bit 2
3KF0	4F16	11 (F)	Output Adrs Bit 3
3KF0	4F16	9 (F)	I/O Buffer Adrs Bit 0
3KF0	4F16	2 (F)	I/O Buffer Adrs Bit 1
3KF0	4F16	3 (F)	I/O Buffer Adrs Bit 2
3FX0	4D16, 17, 4E15, 16	1 (T)	I/O Buffer Adrs Bit 0, 1, 2, 3
3FX0	↕	2 (F)	I/O Buffer Adrs Bit 0, 1, 2, 3
3FX0	↕	3 (F)	I/O Buffer Adrs Bit 0, 1, 2, 3
3FX0	↕	6 (F)	I/O Buffer Adrs Bit 0, 1, 2, 3
3FX0	4D16, 17, 4E15, 16	13 (F)	I/O Buffer Adrs Bit 0, 1, 2, 3



NOTES

① REGISTER FUNCTION CODE

S2	S1	REGISTER FUNCTION
0	0	HOLD
0	1	DECREMENT
1	0	INCREMENT
1	1	PRESET (LOAD)

2 REFER TO CPLR 3 8 DIAGRAM FOR CLOCK DISTRIBUTION

CONTROL DATA DEVELOPMENT DIVISION	DETAILED PAK DIAGRAM BUFFER ADDRESS	CODE IDENT 34010	DWG NO 60428800	REV A
		SIZE C	SHEET CPLR 3 6	PAGE 5-3-21

DETAILED-PAK DIAGRAM

END TIME CONTROL, ERROR REGISTER, ERROR CODE GENERATOR AND PROCESSOR INTERFACE

END TIME CONTROL

The end time control circuits perform the termination functions of a successful or not so successful transfer operation for the coupler. The word count control circuit (CPLR 3.1) provides a Y equals 0 signal (word count) to the end time control (4LE0 pak) when the Y register has decremented to zero indicating that all the words for the active transfer request are accounted for. In an ECS write operation, this means the coupler received a controller accept signal for the previous word from the ECS controller; whereas, in an ECS read operation only the word count must equal zero. When these conditions are present, the transfer operation is complete and the end time control can terminate the transfer operation.

The Y equals 0 signal (4LE0 pak) is complemented and sets the start end time flip-flop if the flip-flop is not already set due to an ECS abort and there is a go ECS signal to clock the flip-flop. The go ECS signal indicates that a transfer operation is in progress. The complemented output signal of the flip-flop forces the end time counter (3LA0 pak) into an increment mode. The end time counter operates in only two modes. The preset mode loads all zeros in the counter so that when the counter goes into an increment mode, it starts at zero and increases its count once each clock period (100 nanoseconds). The counter outputs end time bits 4, 8, and 16 for the end time decoder (4LE0 pak). When bits 16 and 4 are set, 2000 nanoseconds have elapsed and when bits 16 and 8 are set 2400 nanoseconds have elapsed. End time 4 and 16 are complemented (5PKG pak) on the way to the decoder. The end time decoder interprets the count and on the next clock pulse provides the enable end time signal 2100 nanoseconds (for a read ECS operation) or 2500 nanoseconds (for a write ECS operation) after the setting of the start end time flip-flop. The enable end time signal is ANDed with the start end time flip-flop output signal to set the end time flip-flop at time T1, 3.

The end time flip-flop output signal sets the end of transfer clear flip-flop on the next time T1, 3. The end of transfer clear flip-flop generates the end of transfer clear signal for flip-flops on this pak and is fanned out to appropriate coupler circuits to indicate the end of the transfer operation.

The master clear signal serves the same purpose as the end of transfer clear signal. The resetting of the end time flip-flop ends the signal that sets the end of transfer clear flip-flop and ends the clear signal. The end time flip-flop output signal also makes an AND function if there has not been a CPU exchange abort. This results in the generation of an end of transfer signal if a controller abort or an error detected by the error register (3AS0 pak) is not present. The end of transfer signal is transmitted to the CPU via a latch register and transmitter (4KT0 pak). The end time flip-flop also sends an ECS end of transfer signal to the CPU. The fact that the coupler generates these two signals indicates to the CMC and CPU that the transfer operation completed successfully.

If the ECS controller detects an error, it sends a controller abort signal to the coupler to set the ECS abort flip-flop via a receiver and latch register (CPLR 3.3). If this occurs during an ECS read operation, the AND function on the output of the ECS abort flip-flop is not made and the output of the ECS abort flip-flop is prevented from setting the start end time flip-flop. However, the ECS abort flip-flop output signal is sent to the coupler transfer control circuit (CPLR 3.2) to set the fake read flip-flop and cause a fill of all zeros for the remaining words of the transfer operation to be written into central memory. The ECS abort flip-flop output signal is also sent to the error code generator and coded for transmission to the CPU. The ECS abort flip-flop output signal is also inverted and ANDed with the error signal. The resulting signal from this gate prevents the generation of the end of transfer signal sent by the end time flip-flop to the transmitter, and at the same time sends an error end of transfer signal to the transmitter for the CPU. If the transfer operation taking place is an ECS write operation when the controller sends an abort signal, the output of the ECS abort flip-flop sets the start end time flip-flop to begin the process of ending the transfer operation without waiting for the word count to equal zero. The transfer operation ends immediately to prevent destroying other data already in ECS.

If the CPU sends an exchange abort ECS signal, it enters the coupler via a receiver and latch register (4KR0 pak) and is gated to the CPU exchange abort flip-flop (4LE0 pak) by the go ECS signal. When the CPU exchange abort flip-flop sets, the output signal immediately sets the end time flip-flop to generate an ECS end of transfer signal. The CPU does not require the coupler to send an end of transfer signal to the CPU for the CPU exchange abort.

The transfer control circuit (CPLR 3.2) sends an end data transfer signal that immediately sets the end time flip-flop if the Y equals 0 signal (word count) or an error signal occurs within 550 nanoseconds of the coupler accept signal. The CPU sometimes sends the Y equals 0 condition along with the coupler request signal to generate a pass condition for ECS. An error signal at the time of the delayed coupler accept signal usually indicates that an address error exists and the end time flip-flop is set to prevent the transfer of data to an incorrect ECS location.

The CPU sends an address with bit 23 set as a request for a flag register operation. Bit 23 sets the flag register operation flip-flop (CPLR 3.3) that generates the flag register operation signal. This signal enters the end control circuit (4LE0 pak) and partially makes three AND functions. One AND function is completed when the ECS controller sends an accept signal back upon receipt of the address with bit 23 set. The output signal of this AND function sets the end time flip-flop and generates an end of transfer signal. The end of transfer signal is generated after receipt of the ECS coupler accept signal for the address because the CPU and CMC are not required for a flag operation. However, the end of transfer signal to the CPU does indicate that the address containing bit 23 set successfully transferred.

If the ECS controller detects a parity error in the ECS address that has bit 23 set, it sends back a controller parity error signal. The signal enters the coupler via a receiver and holding register (CPLR 3.5) and passes through the error register (3AS0 pak) to complete the AND function (4LE0 pak) with the flag register operation signal. The resulting signal from this AND function is the ECS flag register parity error signal for transmission (4KT0 pak) to the CMC. If the ECS controller sends back a controller abort signal, the function performed by the controller has had a negative result. The controller abort signal sets the ECS abort flip-flop (4LE0 pak) that causes the generation of an error end of transfer signal to indicate the negative result to the CPU.

ERROR REGISTER AND CODE GENERATOR

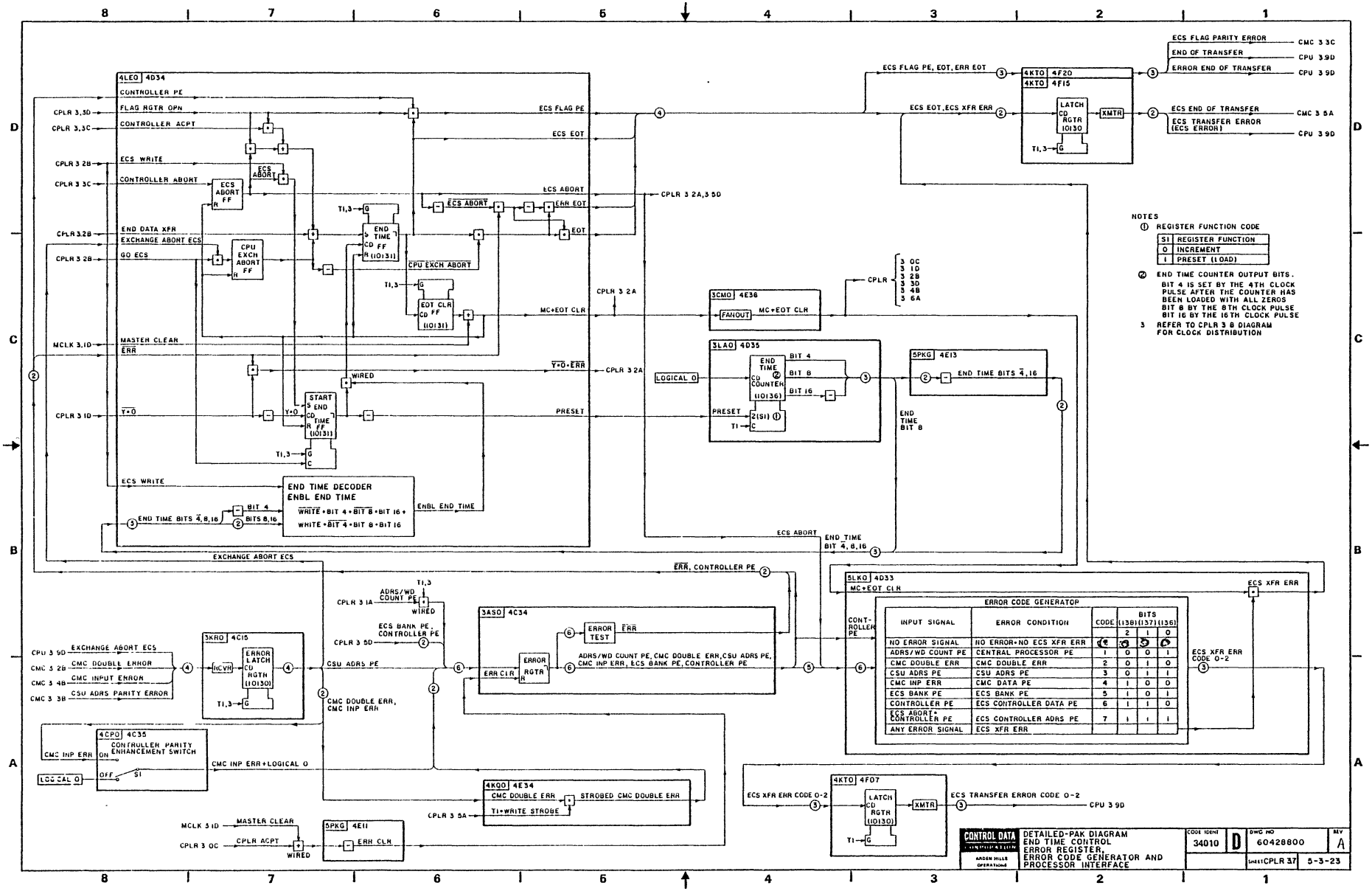
The error register (3AS0 pak) receives error signals that occur during an ECS operation from the various detection circuits. The errors detected in the CMC and CPU enter the error register via a receiver and latch register (3KR0 pak). The T1 and write strobe signal gates (4KQ0 pak) the CMC double error signal to the error register. The controller parity enhancement switch (4CP0) in the OFF position prevents the CMC input error signal from entering the error register. This switch is set in the ON position only when the ECS uses a controller that has the parity enhancement installed. The CMC would constantly indicate an input error if the controller did not have the parity enhancement circuit that sends a parity bit to the CMC and the switch was in the ON position. The errors detected in the ECS controller load into the error register via a receiver and holding register (CPLR 3.5). Any errors detected in the address and word count entering the coupler (CPLR 3.1) cause parity error signals that are gated to the error register at time T1, 3. When an error signal sets the error register, the error test circuit outputs an error signal to the end time control circuits (4LE0 pak) that causes an error end of transfer signal. The error register sends any error signals to the error code generator (5LK0 pak). The error register is reset by the coupler accept signal each time the coupler is requested for a transfer operation. This clears out all error signals in registers that were due to the previous request.

The error code generator (5LK0 pak) receives error signals from the error register and codes them for transmission via a 4KT0 pak to the CPU. When an error condition does exist, the ECS transfer error signal is always generated. The ECS transfer error signal requires the master clear or end of transfer clear signals as a gating signal to transfer to the latch register and transmitter. This causes the ECS transfer error signal to arrive at the status and control register after the end of transfer clear signal to indicate that an error occurred on the last transfer operation.

CPLR 3.7 TEST POINTS

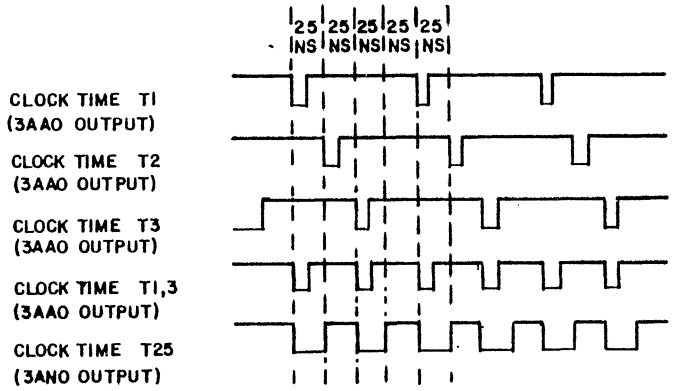
Module	Location	Test Point	Description
4LE0	4D34	8 (T)	Flag Rgtr Opn
4LE0	4D34	2 (T)	Controller Acpt
4LE0	4D34	9 (T)	ECS Write
4LE0	4D34	3 (T)	End Time FF Set
4LE0	4D34	1 (T)	Start End Time FF Set
4LE0	4D34	11 (T)	Go ECS
4LE0	4D34	13 (T)	Clock Time T1, 3
4LE0	4D34	6 (T)	Controller PE
4LE0	4D34	4 (T)	End Time Bit 4
4LE0	4D34	7 (T)	End Time Bit 8
4LE0	4D34	10 (F)	End Time Bit 16
4KT0	4F15	3 (T)	ECS Transfer Error

Module	Location	Test Point	Description
4KT0	4F15	8 (T)	ECS End of Transfer
4KT0	4F15	2 (T)	Clock Time T1, 3
4KT0	4F20	10 (T)	ECS Flag PE
4KT0	4F20	7 (T)	End of Transfer
4KT0	4F20	6 (T)	Error End of Transfer
4KT0	4F20	2 (T)	Clock Time T1, 3
3CM0	4E36	1 (F)	MC + EOT Clear
3CM0	4E36	5 (F)	MC + EOT Clear
3KR0	4C15	7 (T)	Clock Time T1, 3
3KR0	4C15	6 (T)	Exchange Abort ECS
3KR0	4C15	13 (T)	CMC Double Error
3KR0	4C15	12 (T)	CMC Input Error
3KR0	4C15	8 (T)	CSU Address Parity Error
4KQ0	4E34	4 (T)	CMC Double Err
4KQ0	4E34	12 (T)	T1 · Write Strobe
3AS0	4C34	13 (F)	ECS Bank PE
3AS0	4C34	12 (F)	Controller PE
3AS0	4C34	11 (F)	CSU Adrs PE
3AS0	4C34	14 (F)	CMC Input Err
3AS0	4C34	9 (F)	CMC Double Err
3AS0	4C34	1 (T)	Error Clear
3AS0	4C34	2 (T)	Clk Adrs/Wd Count PE
3AS0	4C34	4 (F)	Clk Adrs/Wd Count PE
5LK0	4D33	1 (T)	Adrs/Wd Count PE
5LK0	4D33	2 (T)	CMC Input Err
5LK0	4D33	3 (T)	CSU Adrs PE
5LK0	4D33	4 (T)	CMC Double Err
4KT0	4F07	2 (T)	Clock Time T1
4KT0	4F07	8 (T)	ECS Transfer Error Code Bit 0
4KT0	4F07	5 (T)	ECS Transfer Error Code Bit 1
4KT0	4F07	3 (T)	ECS Transfer Error Code Bit 2


4LEO 4D34
CONTROLLER PE
FLAG RGTR OPN
CONTROLLER ACPT
ECS WRITE
CONTROLLER ABORT
END DATA XFR
EXCHANGE ABORT ECS
GO ECS
MASTER CLEAR
ERR
Y=0
WIRED
END TIME DECODER
ENBL END TIME
WRITE•BIT 4•BIT 8•BIT 16+
WRITE•BIT 4•BIT 8•BIT 16
ECS ABORT FF
CPU EXCH ABORT FF
END TIME CD FF (10131)
EOT CLR CD FF (10131)
START END TIME CD FF (10131)
ECS FLAG PE
ECS EOT
ECS ABORT
ERR EOT
EOT
CPU EXCH ABORT
MC+EOT CLR
Y=0•ERR
PRESET
ENBL END TIME
3CMO 4E36
FANOUT
MC+EOT CLR
CPLR
3LAO 4D35
END TIME CD COUNTER (10136)
BIT 4
BIT 8
BIT 16
PRESET
2(S1)
5PKG 4E13
END TIME BITS 4,16
END TIME BIT 8
ECS FLAG PE, EOT, ERR EOT
ECS EOT, ECS XFR ERR
4KTO 4F20
4KTO 4F15
LATCH CD RGTR (10130)
XMTR
ECS FLAG PARITY ERROR
END OF TRANSFER
ERROR END OF TRANSFER
ECS END OF TRANSFER
ECS TRANSFER ERROR (ECS ERROR)
NOTES
① REGISTER FUNCTION CODE
S1 | REGISTER FUNCTION
0 | INCREMENT
1 | PRESET (LOAD)
② END TIME COUNTER OUTPUT BITS. BIT 4 IS SET BY THE 4TH CLOCK PULSE AFTER THE COUNTER HAS BEEN LOADED WITH ALL ZEROS BIT 8 BY THE 8TH CLOCK PULSE BIT 16 BY THE 16TH CLOCK PULSE
③ REFER TO CPLR 3 8 DIAGRAM FOR CLOCK DISTRIBUTION
5LKO 4D33
MC+EOT CLR
ECS XFR ERR
ERROR CODE GENERATOR
INPUT SIGNAL | ERROR CONDITION | CODE | BITS (13B)(13T)(13G)
NO ERROR SIGNAL | NO ERROR•NO ECS XFR ERR | 0 | 0 0 0
ADRS/WD COUNT PE | CENTRAL PROCESSOR PE | 1 | 0 0 1
CMC DOUBLE ERR | CMC DOUBLE ERR | 2 | 0 1 0
CSU ADRS PE | CSU ADRS PE | 3 | 0 1 1
CMC INP ERR | CMC DATA PE | 4 | 1 0 0
ECS BANK PE | ECS BANK PE | 5 | 1 0 1
CONTROLLER PE | ECS CONTROLLER DATA PE | 6 | 1 1 0
ECS ABORT•CONTROLLER PE | ECS CONTROLLER ADRS PE | 7 | 1 1 1
ANY ERROR SIGNAL | ECS XFR ERR
ECS XFR ERR CODE 0-2
3ASO 4C34
ERROR TEST
ERROR RGTR
ERR CLR
ADRS/WD COUNT PE, CMC DOUBLE ERR, CSU ADRS PE, CMC INP ERR, ECS BANK PE, CONTROLLER PE
3KRO 4C15
ERROR LATCH CD RGTR (10130)
HCVR
EXCHANGE ABORT ECS
CMC DOUBLE ERROR
CMC INPUT ERROR
CSU ADRS PARITY ERROR
CSU ADRS PE
CMC DOUBLE ERR, CMC INP ERR
4CPO 4C35
CONTROLLER PARITY ENHANCEMENT SWITCH
ON
OFF
S1
LOGICAL 0
CMC INP ERR+LOGICAL 0
4KQO 4E34
CMC DOUBLE ERR
STROBED CMC DOUBLE ERR
T1•WRITE STROBE
4KTO 4F07
MCLK 3 1D
MASTER CLEAR
CPLR ACPT
CPLR 3 0C
5PKG 4E11
ERR CLR
CONTROL DATA
DETAILED-PAK DIAGRAM
END TIME CONTROL
ERROR REGISTER,
ERROR CODE GENERATOR AND
PROCESSOR INTERFACE
CODE IDENT 34010
D
DWG NO 60428800
REV A
SHEET CPLR 37
5-3-23

DETAILED-PAK DIAGRAM
CLOCK DISTRIBUTION

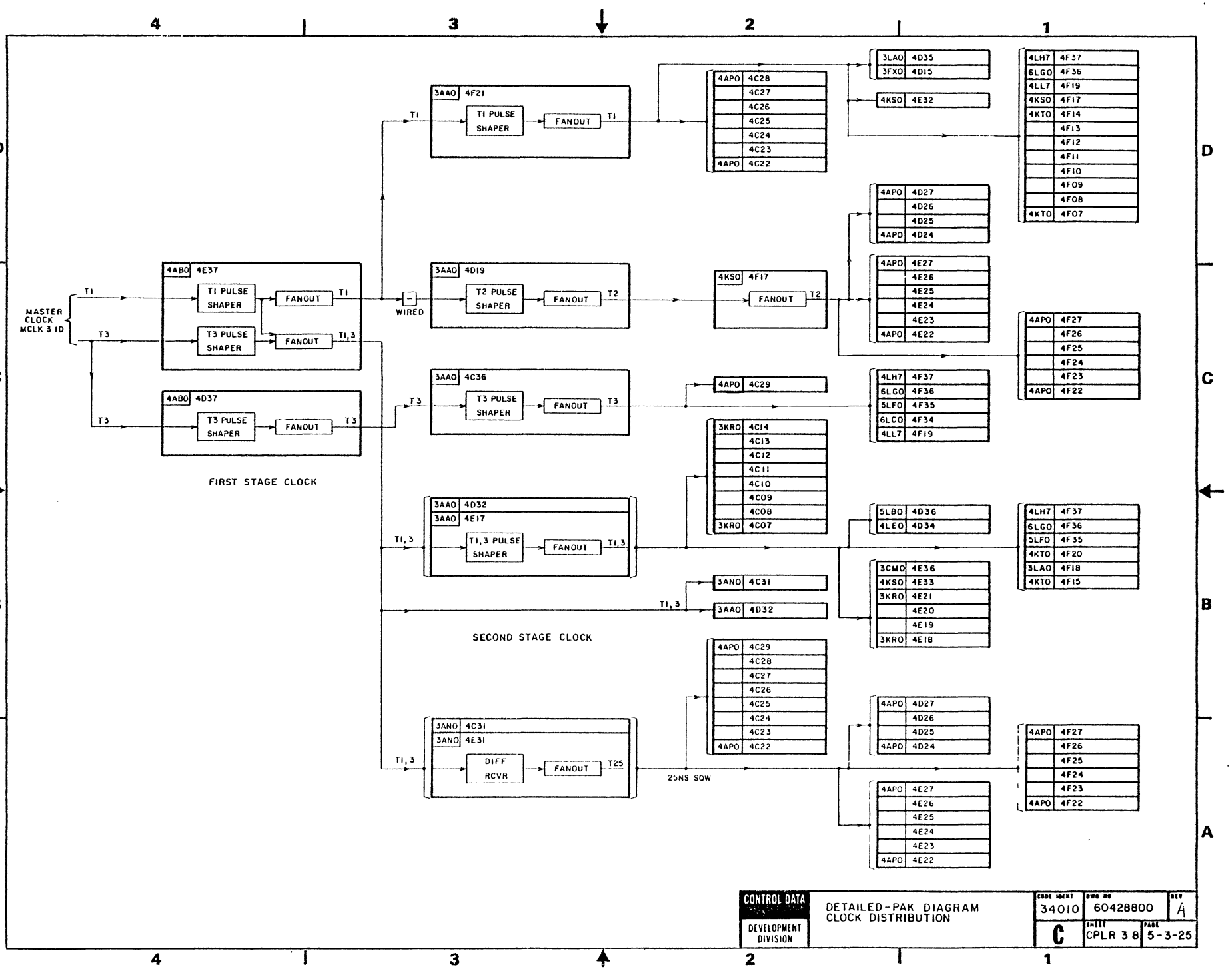
The clock distribution diagram shows the distribution of the clock pulses which are shaped and sent to the various paks within the coupler. A pak and its location is shown for each clock pulse it receives. The clock distribution timing diagram shows the relationship of the timing pulses to one another.

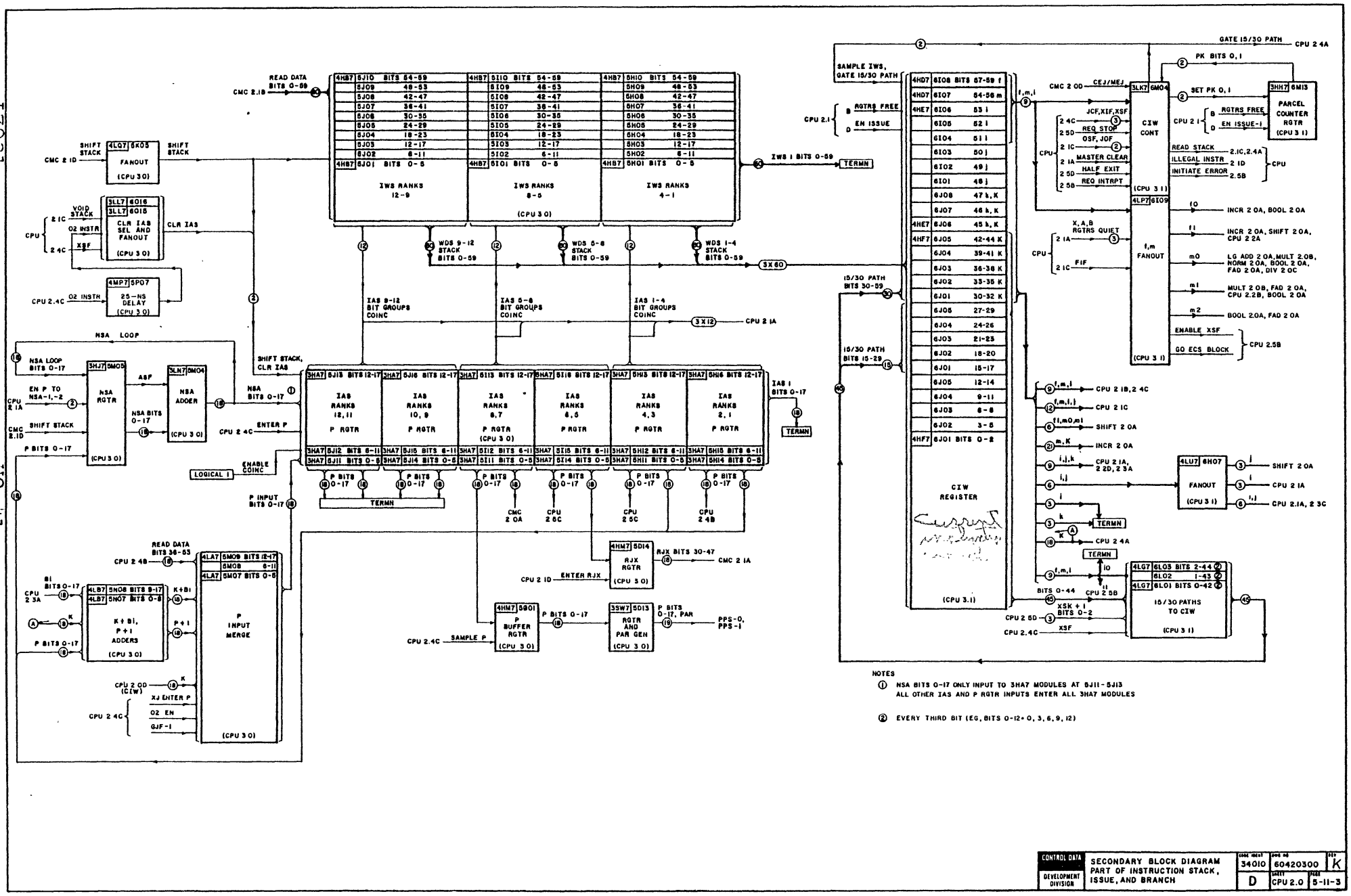


Clock Distribution Timing

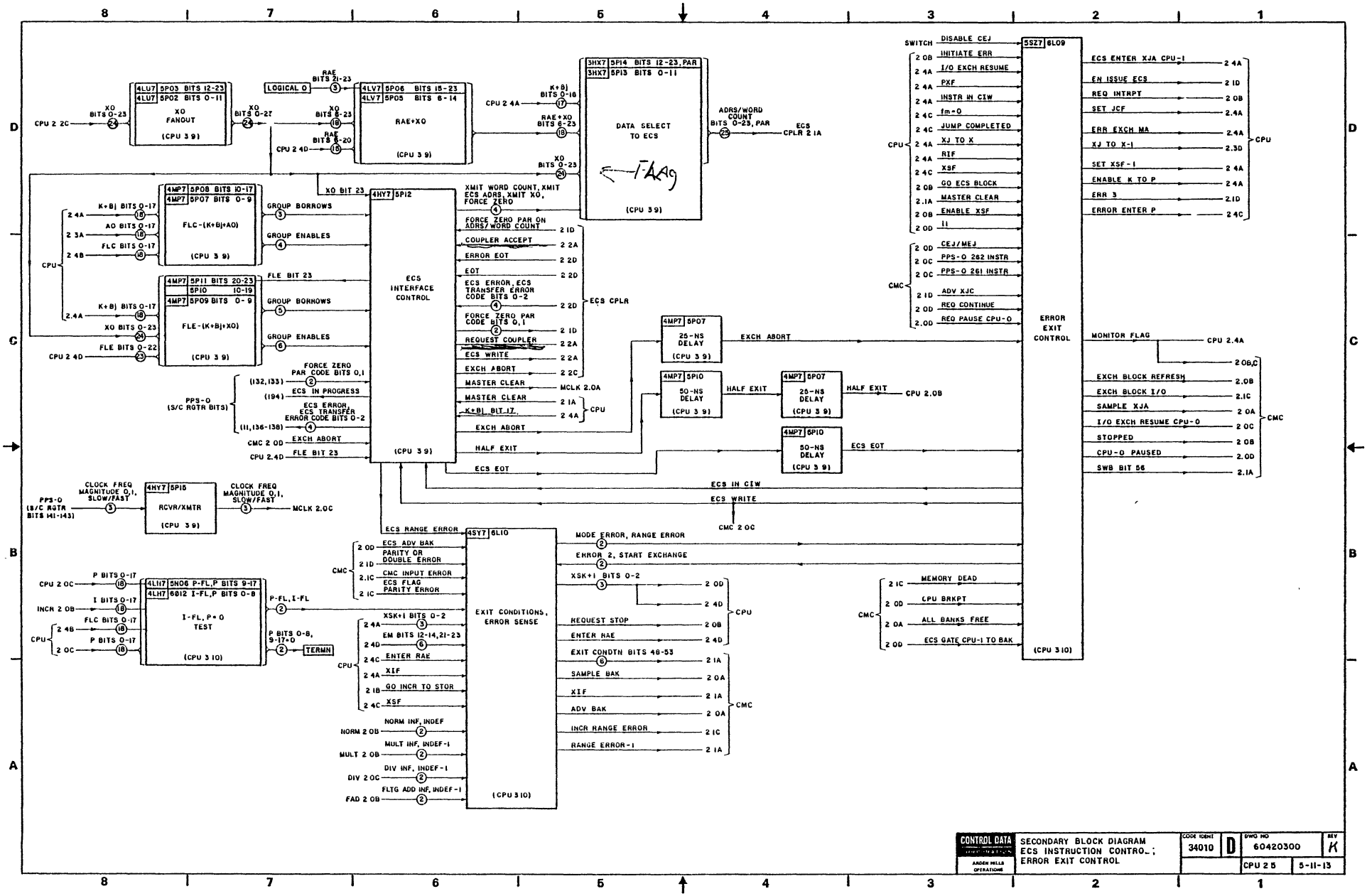
CPLR 3.8 TEST POINTS

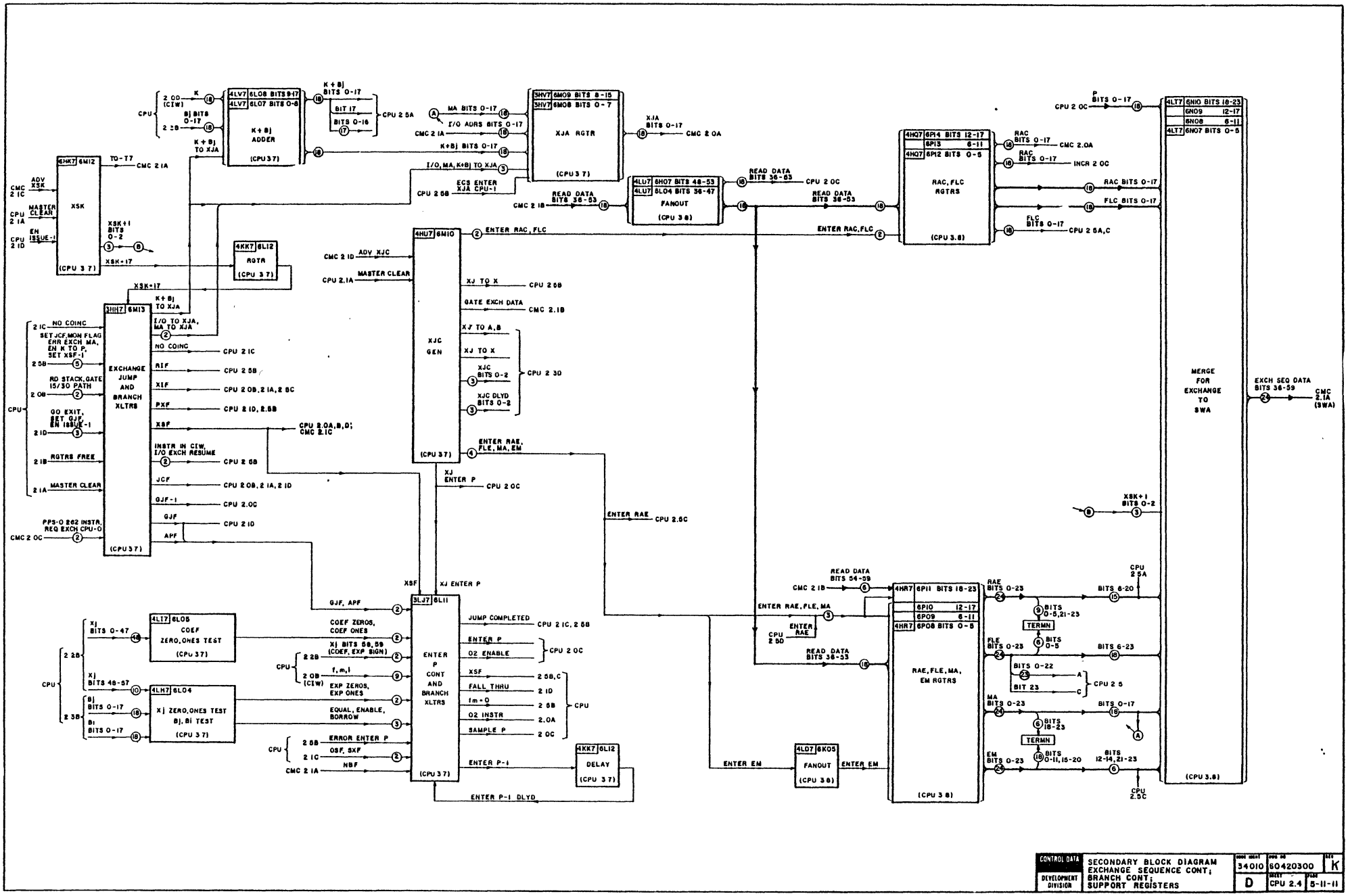
Module	Location	Test Point	Description
4AB0	4E37	8 (T)	Clock Time T1
4AB0	4E37	10 (T)	Clock Time T3
4AB0	4D37	8 (T)	Clock Time T3
3AA0	4F21	3 (T)	Clock Time T1
3AA0	4F21	1 (F)	Clock Time T1
3AA0	4F21	2 (F)	Clock Time T1
3AA0	4D19	3 (F)	Clock Time T2
3AA0	4D19	1 (T)	Clock Time T2
3AA0	4D19	2 (T)	Clock Time T2
4KS0	4F17	1 (F)	Clock Time T2
4KS0	4F17	2 (F)	Clock Time T2
4KS0	4F17	3 (F)	Clock Time T2
4KS0	4F17	10 (F)	Clock Time T2
4KS0	4F17	14 (F)	Clock Time T2
3AA0	4C36	3 (T)	Clock Time T3
3AA0	4C36	1 (F)	Clock Time T3
3AA0	4C36	2 (F)	Clock Time T3
3AA0	4D32, 4E17	3 (T)	Clock Time T1, 3
3AA0	4D32, 4E17	1 (F)	Clock Time T1, 3
3AA0	4D32, 4E17	2 (F)	Clock Time T1, 3
3AN0	4C31, 4E17	3	Clock Time T25 (25 ns SQW)
3AN0	4C31, 4E31	1	Clock Time T25 (25 ns SQW)
3AN0	4C31, 4E31	2	Clock Time T25 (25 ns SQW)


L7031
HO-40
4
3
2
1
D
C
B
A
MASTER CLOCK MCLK 3 ID
T1
T3
4ABO 4E37
T1 PULSE SHAPER
T3 PULSE SHAPER
FANOUT
T1
T1,3
4ABO 4D37
T3 PULSE SHAPER
FANOUT
T3
FIRST STAGE CLOCK
WIRED
3AAO 4F21
T1 PULSE SHAPER
FANOUT
T1
3AAO 4D19
T2 PULSE SHAPER
FANOUT
T2
3AAO 4C36
T3 PULSE SHAPER
FANOUT
T3
3AAO 4D32
3AAO 4E17
T1,3 PULSE SHAPER
FANOUT
T1,3
3ANO 4C31
3AAO 4D32
SECOND STAGE CLOCK
3ANO 4C31
3ANO 4E31
DIFF RCVR
FANOUT
T25
25NS SQW
4APO 4C28
4C27
4C26
4C25
4C24
4C23
4APO 4C22
4KSO 4F17
FANOUT
T2
4APO 4C29
3KRO 4C14
4C13
4C12
4C11
4C10
4C09
4C08
3KRO 4C07
3LAO 4D35
3FXO 4D15
4KSO 4E32
4APO 4D27
4D26
4D25
4APO 4D24
4APO 4E27
4E26
4E25
4E24
4E23
4APO 4E22
4LH7 4F37
6LGO 4F36
5LFO 4F35
6LCO 4F34
4LL7 4F19
5LBO 4D36
4LEO 4D34
3CMO 4E36
4KSO 4E33
3KRO 4E21
4E20
4E19
3KRO 4E18
4LH7 4F37
6LGO 4F36
4LL7 4F19
4KSO 4F17
4KTO 4F14
4F13
4F12
4F11
4F10
4F09
4F08
4KTO 4F07
4APO 4F27
4F26
4F25
4F24
4F23
4APO 4F22
5LBO 4D36
4LEO 4D34
4LH7 4F37
6LGO 4F36
5LFO 4F35
4KTO 4F20
3LAO 4F18
4KTO 4F15
4APO 4D27
4D26
4D25
4APO 4D24
4APO 4E27
4E26
4E25
4E24
4E23
4APO 4E22
4APO 4F27
4F26
4F25
4F24
4F23
4APO 4F22
CONTROL DATA
DEVELOPMENT DIVISION
DETAILED-PAK DIAGRAM
CLOCK DISTRIBUTION
CODE IDENT 34010
DWG NO 60428800
REV A
SIZE C
SHEET CPLR 3 8
PAGE 5-3-25

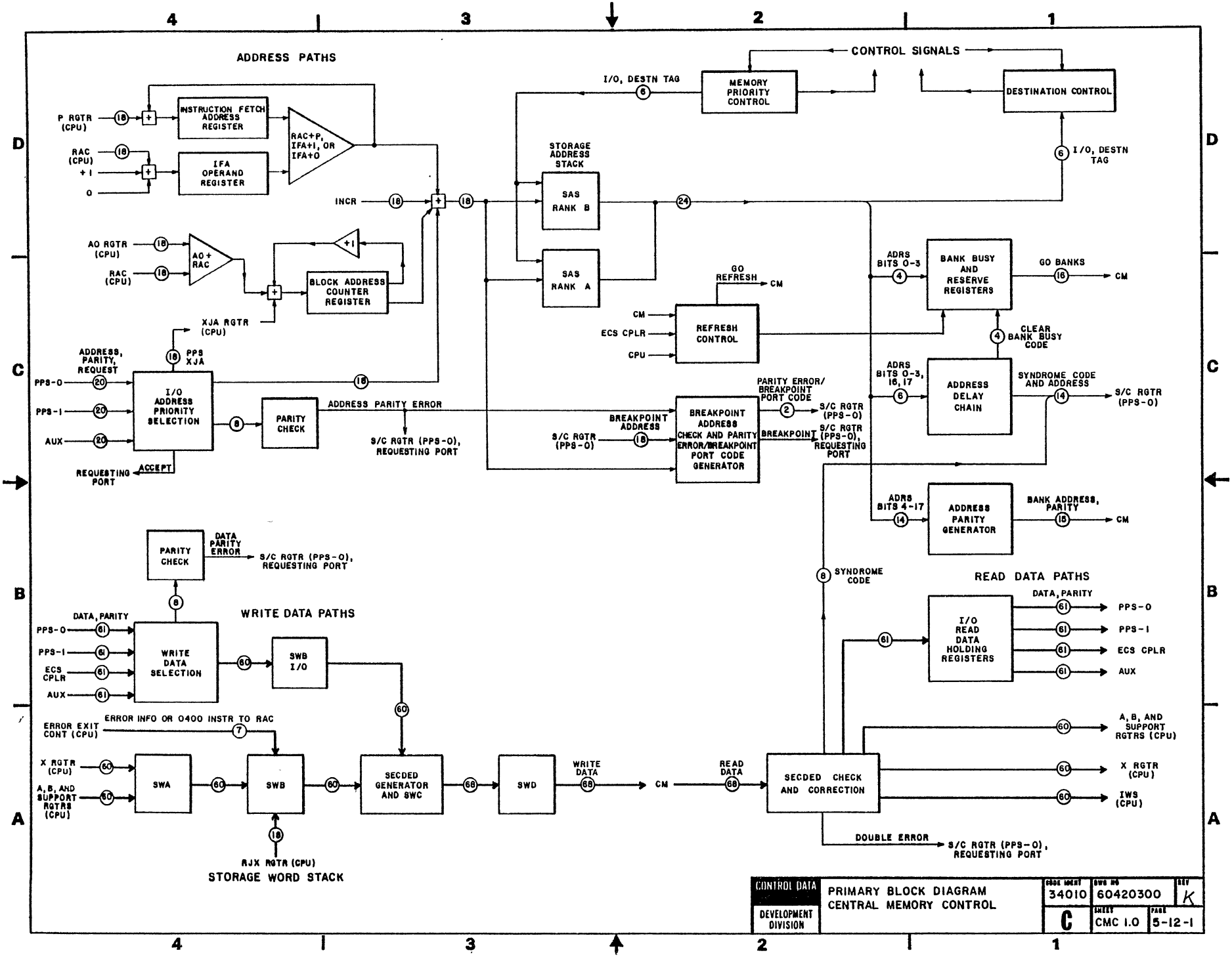


CONTROL DATA DEVELOPMENT DIVISION	SECONDARY BLOCK DIAGRAM PART OF INSTRUCTION STACK, ISSUE, AND BRANCH	34010	60420300	K
		D	CPU 2.0	5-11-3

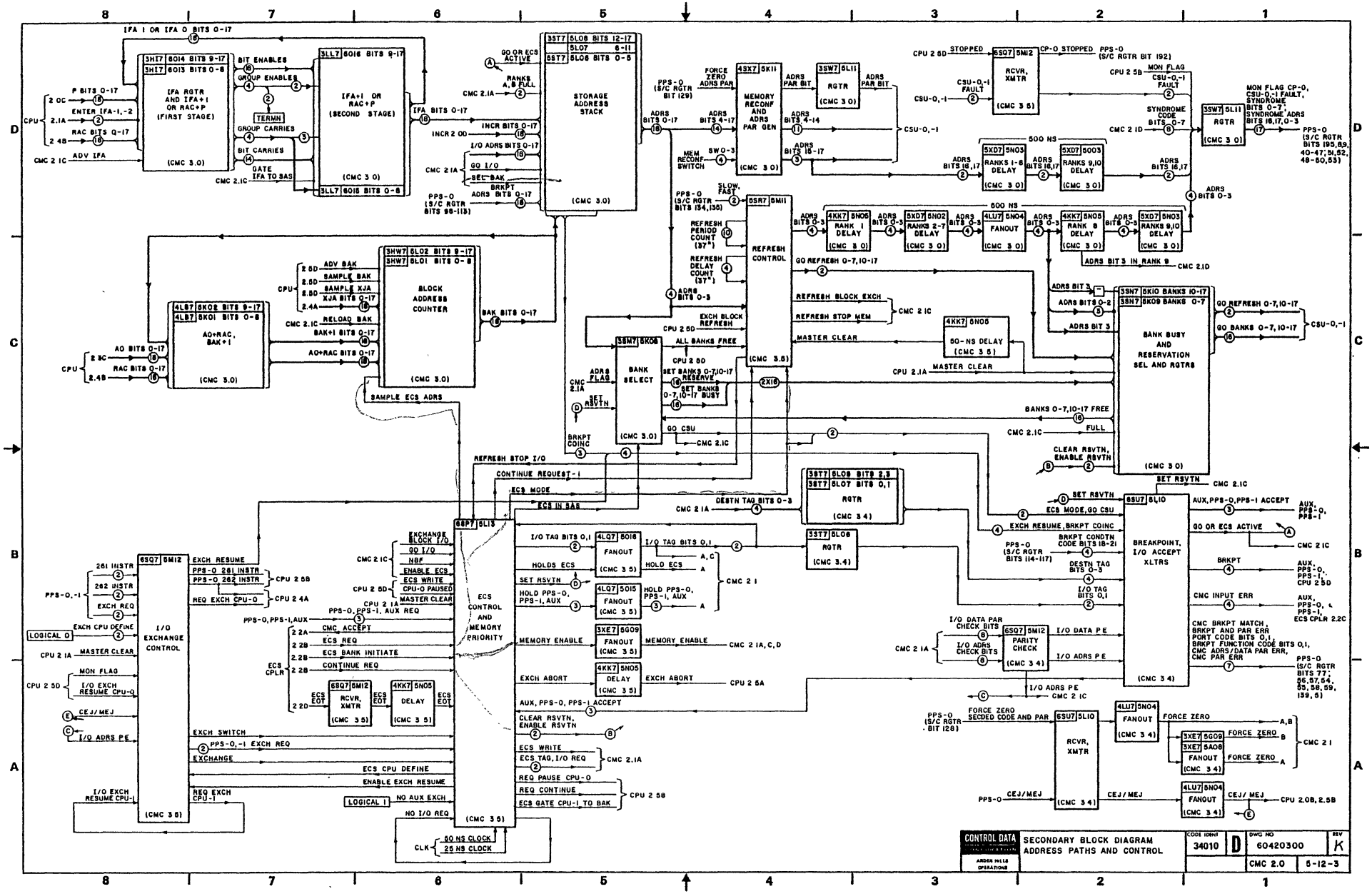

4LU7 5P03 BITS 12-23
4LU7 5P02 BITS 0-11
XO FANOUT
(CPU 3 9)
LOGICAL 0
4LV7 5P06 BITS 18-23
4LV7 5P05 BITS 6-14
RAE+XO
(CPU 3 9)
3HX7 5P14 BITS 12-23, PAR
3HX7 5P13 BITS 0-11
DATA SELECT TO ECS
(CPU 3 9)
ADRS/WORD COUNT BITS 0-25, PAR
ECS CPLR 2 1A
4MP7 5P08 BITS 10-17
4MP7 5P07 BITS 0-9
FLC-(K+B|+AO)
(CPU 3 9)
4MP7 5P11 BITS 20-23
5P10 10-19
4MP7 5P09 BITS 0-9
FLE-(K+B|+XO)
(CPU 3 9)
4HY7 5P12
ECS INTERFACE CONTROL
(CPU 3 9)
4MP7 5P07
25-NS DELAY
(CPU 3 9)
4MP7 5P10
50-NS DELAY
(CPU 3 9)
4MP7 5P07
25-NS DELAY
(CPU 3 9)
4MP7 5P10
50-NS DELAY
(CPU 3 9)
5SZ7 6L09
ERROR EXIT CONTROL
(CPU 3 10)
4HY7 5P15
RCVR/XMTR
(CPU 3 9)
4LH7 6012 I-FL,P BITS 0-8
4LL17 5N06 P-FL,P BITS 9-17
I-FL, P=0 TEST
(CPU 3 10)
4SY7 6L10
EXIT CONDITIONS, ERROR SENSE
(CPU 3 10)
CONTROL DATA
ARDEN HILLS OPERATIONS
SECONDARY BLOCK DIAGRAM
ECS INSTRUCTION CONTRO_;
ERROR EXIT CONTROL
CODE IDENT 34010
D
DWG NO 60420300
REV K
CPU 2 5
5-11-13



CONTROL DATA DEVELOPMENT DIVISION	SECONDARY BLOCK DIAGRAM EXCHANGE SEQUENCE CONT; BRANCH CONT; SUPPORT REGISTERS	34010	60420300	K
		D	CPU 2.4	5-11-11



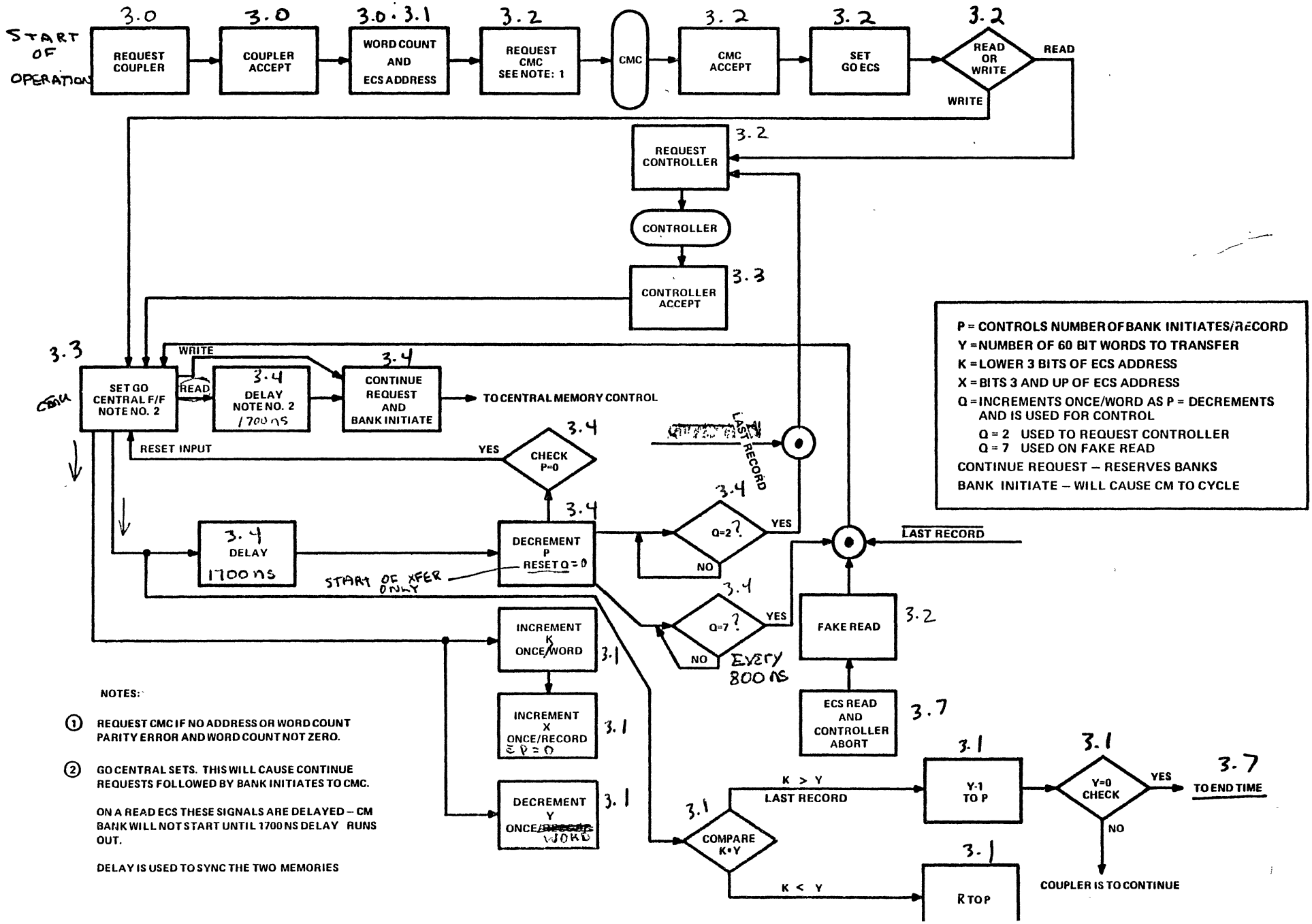
CONTROL DATA DEVELOPMENT DIVISION	PRIMARY BLOCK DIAGRAM CENTRAL MEMORY CONTROL	CODE IDENT 34010	DWG NO 60420300	REV K
		C	SHEET CMC 1.0	PAGE 5-12-1


IFA RGTR AND IFA+1 OR RAC+P (FIRST STAGE) (CMC 3.0)
IFA+1 OR RAC+P (SECOND STAGE) (CMC 3.0)
STORAGE ADDRESS STACK (CMC 3.0)
MEMORY RECONF AND ADRS PAR GEN (CMC 3.0)
RQTR (CMC 3.0)
RCVR, XMTR (CMC 3.5)
RANK 1 DELAY (CMC 3.0)
RANKS 2-7 DELAY (CMC 3.0)
FANOUT (CMC 3.0)
RANK 8 DELAY (CMC 3.0)
RANKS 9,10 DELAY (CMC 3.0)
RANKS 1-8 DELAY (CMC 3.0)
50-NS DELAY (CMC 3.5)
REFRESH CONTROL (CMC 3.5)
BLOCK ADDRESS COUNTER (CMC 3.0)
AQ+RAC, BAK+1 (CMC 3.0)
BANK SELECT (CMC 3.0)
BANK BUSY AND RESERVATION SEL AND RQTRS (CMC 3.0)
I/O EXCHANGE CONTROL (CMC 3.5)
ECS CONTROL AND MEMORY PRIORITY (CMC 3.5)
BREAKPOINT, I/O ACCEPT XLTRS (CMC 3.4)
PARITY CHECK (CMC 3.4)
RCVR, XMTR (CMC 3.5)
DELAY (CMC 3.5)
RQTR (CMC 3.4)
FANOUT (CMC 3.5)
FANOUT (CMC 3.4)
RCVR, XMTR (CMC 3.4)
I/O EXCH RESUME CPU-1 (CMC 3.5)
CLK 50 NS CLOCK 25 NS CLOCK
CONTROL DATA ARDEN HILLS OPERATIONS
SECONDARY BLOCK DIAGRAM ADDRESS PATHS AND CONTROL
CODE IDENT 34010
D
DWG NO 60420300
REV K
CMC 2.0
5-12-3

175 COUPLER FLOW CHART
FLOW FOR CONTROL ONLY
END TIME AND DATA NOT SHOWN

L7031

HO-6A/TR-7



P = CONTROLS NUMBER OF BANK INITIATES/RECORD
Y = NUMBER OF 60 BIT WORDS TO TRANSFER
K = LOWER 3 BITS OF ECS ADDRESS
X = BITS 3 AND UP OF ECS ADDRESS
Q = INCREMENTS ONCE/WORD AS P = DECREMENTS AND IS USED FOR CONTROL
Q = 2 USED TO REQUEST CONTROLLER
Q = 7 USED ON FAKE READ
CONTINUE REQUEST – RESERVES BANKS
BANK INITIATE – WILL CAUSE CM TO CYCLE

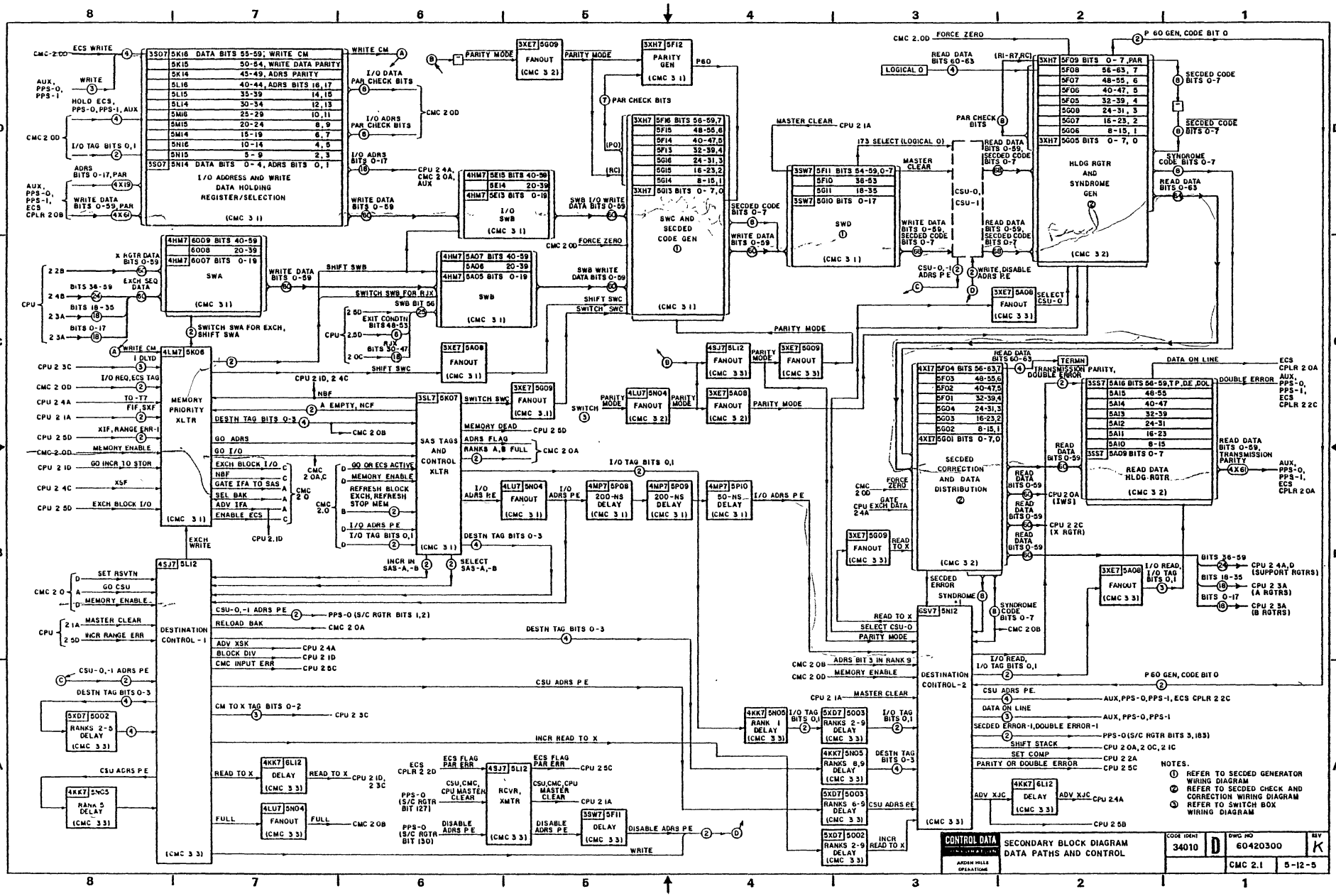
NOTES:

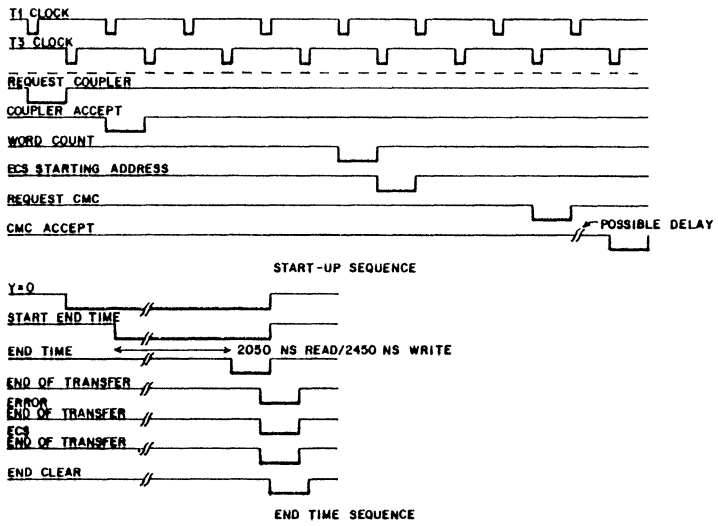
① REQUEST CMC IF NO ADDRESS OR WORD COUNT PARITY ERROR AND WORD COUNT NOT ZERO.

② GO CENTRAL SETS. THIS WILL CAUSE CONTINUE REQUESTS FOLLOWED BY BANK INITIATES TO CMC.

ON A READ ECS THESE SIGNALS ARE DELAYED – CM BANK WILL NOT START UNTIL 1700 NS DELAY RUNS OUT.

DELAY IS USED TO SYNC THE TWO MEMORIES

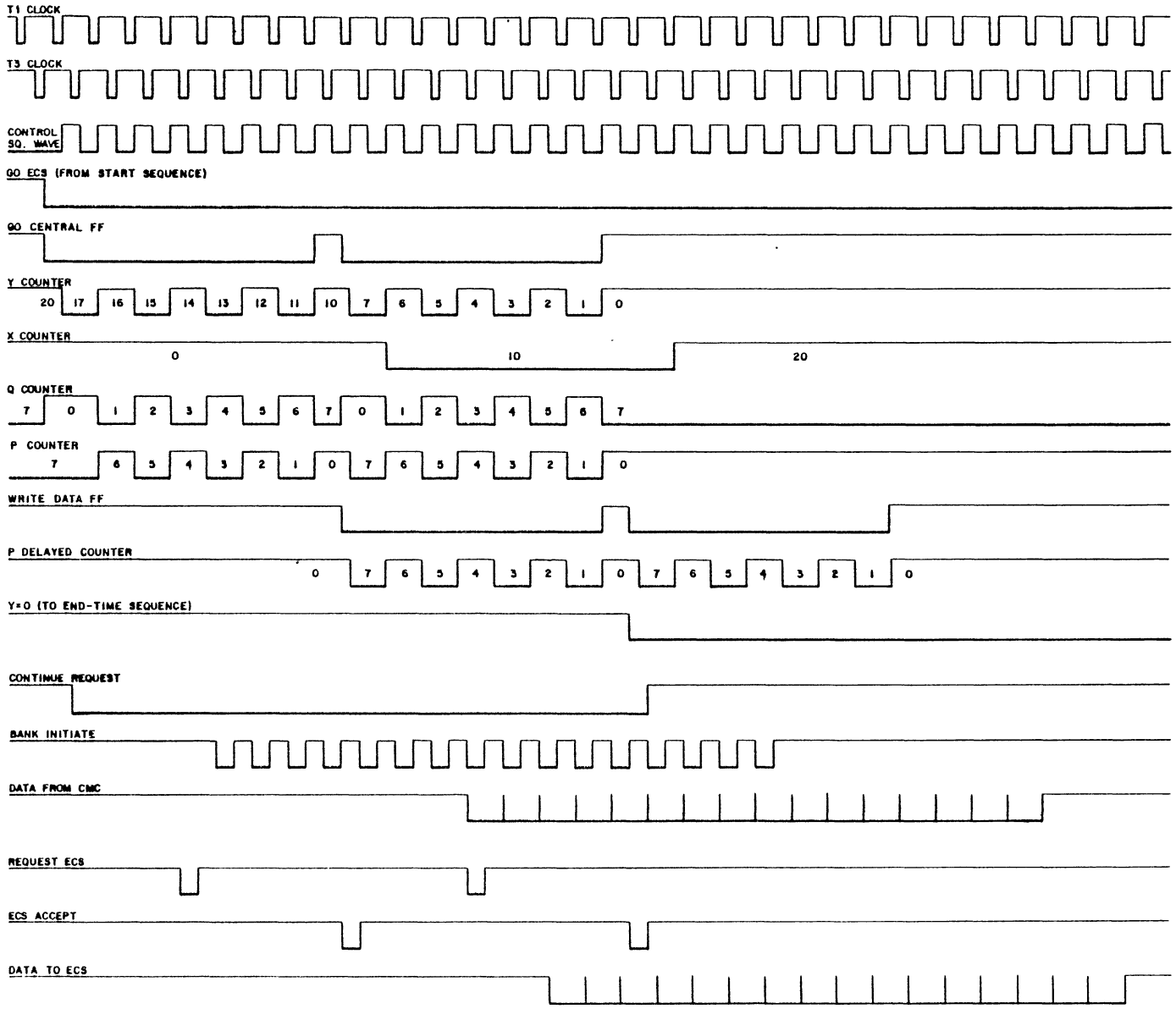

I/O ADDRESS AND WRITE DATA HOLDING REGISTER/SELECTION (CMC 3 1)
I/O SWB (CMC 3 1)
SWA (CMC 3 1)
SWB (CMC 3 1)
SWC AND SECDED CODE GEN (CMC 3 1)
SWD (CMC 3 1)
HLDG RGTR AND SYNDROME GEN (CMC 3 2)
MEMORY PRIORITY XLTR (CMC 3 1)
SAS TAGS AND CONTROL XLTR (CMC 3 1)
SECDED CORRECTION AND DATA DISTRIBUTION (CMC 3 2)
DESTINATION CONTROL-1 (CMC 3 3)
DESTINATION CONTROL-2 (CMC 3 3)
RCVR, XMTR (CMC 3 3)
CONTROL DATA
SECONDARY BLOCK DIAGRAM DATA PATHS AND CONTROL
CODE IDENT 34010
D
DWG NO 60420300
REV K
CMC 2.1
5-12-5



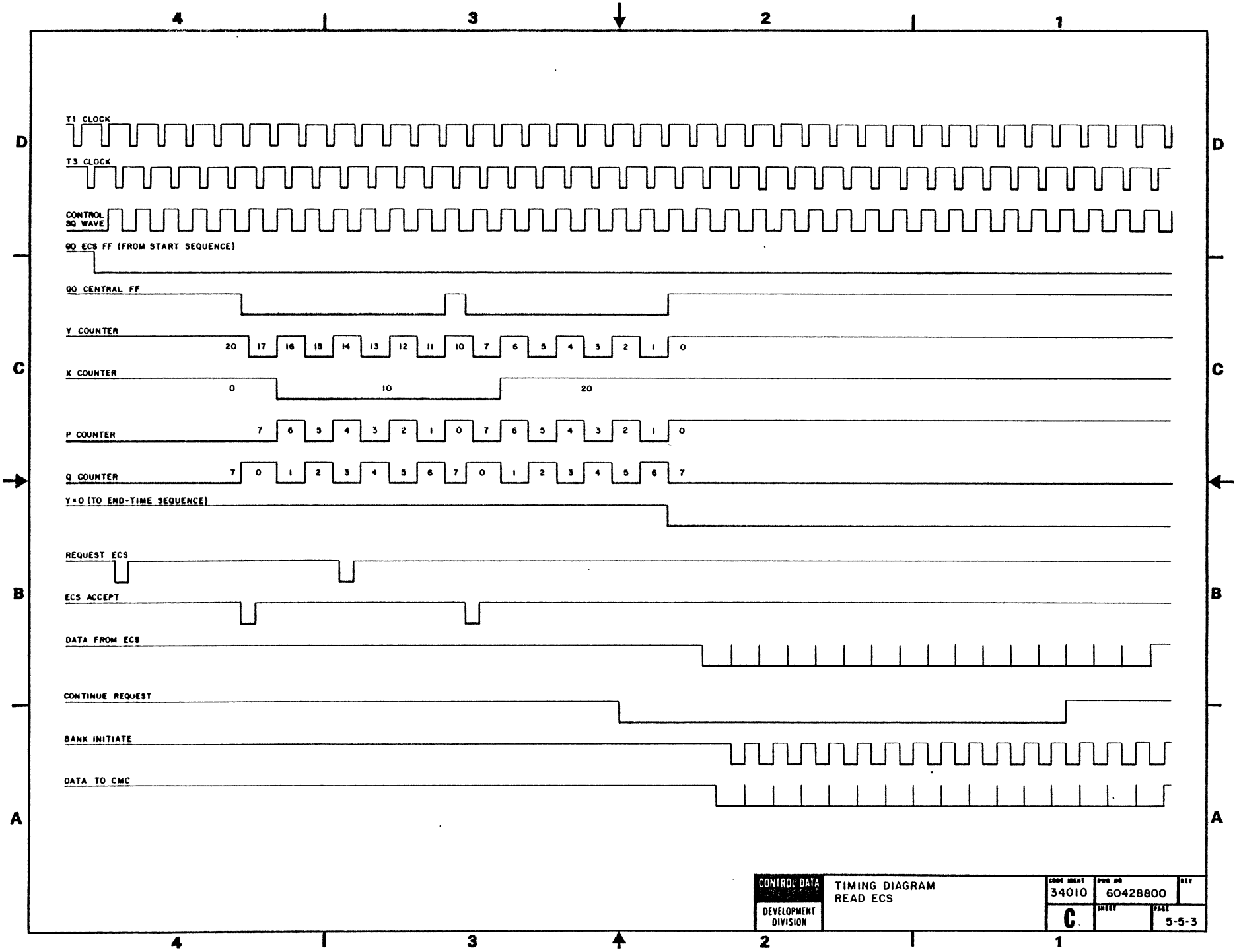
CONTROL DATA DEVELOPMENT DIVISION	TIMING DIAGRAM START-UP AND END TIME SEQUENCE	DOC IDENT 34010	DWG NO 60428800 REV
		SIZE C	SHEET 5-5-5

L7031

HO-48

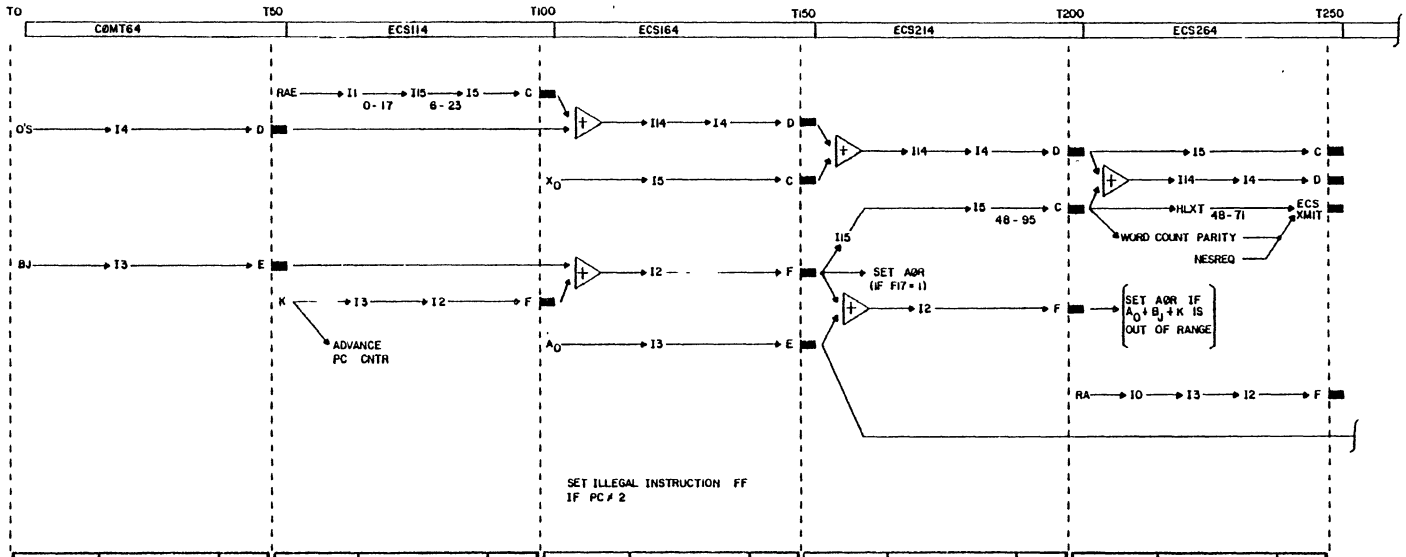


CONTROL DATA DEVELOPMENT DIVISION	TIMING DIAGRAM WRITE ECS	CODE IDENT 34010	DWG NO 60428800	REV
		SIZE C	SHEET	PAGE 5-5-1


4
3
2
1
T1 CLOCK
T3 CLOCK
CONTROL SQ WAVE
GO ECS FF (FROM START SEQUENCE)
GO CENTRAL FF
Y COUNTER
20 17 16 15 14 13 12 11 10 7 6 5 4 3 2 1 0
X COUNTER
0 10 20
P COUNTER
7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0
Q COUNTER
7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
Y=0 (TO END-TIME SEQUENCE)
REQUEST ECS
ECS ACCEPT
DATA FROM ECS
CONTINUE REQUEST
BANK INITIATE
DATA TO CMC
D
C
B
A
CONTROL DATA
DEVELOPMENT DIVISION
TIMING DIAGRAM
READ ECS
CODE IDENT
34010
DWG NO
60428800
REV
C
SHEET
PAGE
5-5-3

L7031

H0-50



TERM NAME	COMMAND OR FUNCTION	DPD NO
C0K50		15
SELDJ	SELECT BJ RGTR	2
C0MT64		15
C0MJB13	B → I3	12
KC050		15
ENABE	ENABLE E RGTR	13
KC0C4		15
14G·14I	O'S → I4	5
KC050		15
ENABLD	ENABLE D RGTR	5

TERM NAME	COMMAND OR FUNCTION	DPD NO
ECS114		27
SRAECS	RIIC → I1	27
F4CX·ES115	$I1_{0-17} \rightarrow I15_{6-23}$	8
ECS114		27
ECS1115	$I15_{0-59} \rightarrow I5_{48-95}$	27
15285	(I5S4·$\overline{I5S2}$·$\overline{I5S1}$)	7
NES114		27
SELK13	K → I3	12
ADVPC2	ADVANCE PC CNTR	12
ECS114		27
ES1312	I3 → I2	27
ENABF	ENABLE F RGTR	13

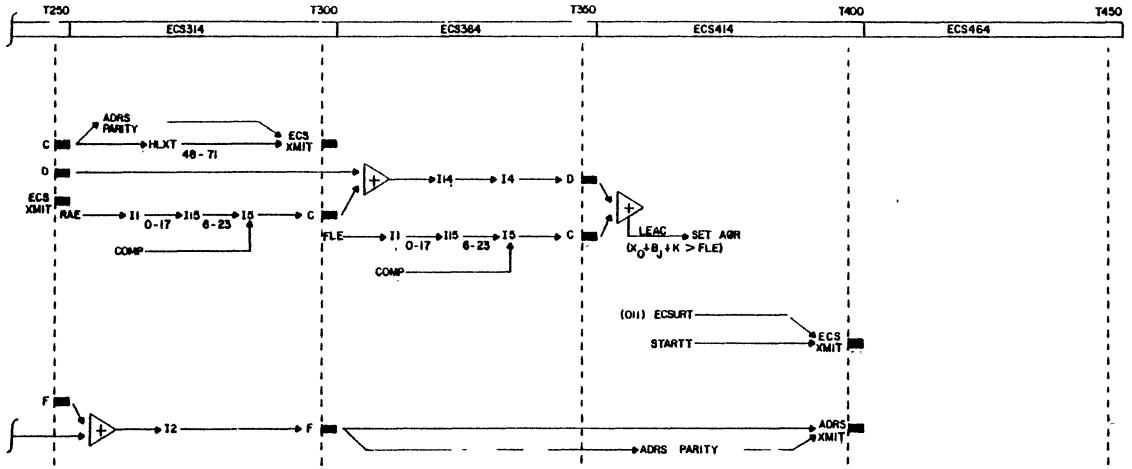
TERM NAME	COMMAND OR FUNCTION	DPD NO
ECS164		27
ECSENB	ENABLE B RGTR	27
ECSENF	ENABLE F RGTR	27
NE164		27
15185	$X_{0-59} \rightarrow I5_{48-107}$	7
ES1115		27
15285	(I5S4·$\overline{I5S2}$·$\overline{I5S1}$)	7
ECS164		27
ECSENC	ENABLE C RGTR	27
NE164		27
SELA13	A → I3	12
ENABE	ENABLE E RGTR	13

TERM NAME	COMMAND OR FUNCTION	DPD NO
ECS214		27
ECSENB	ENABLE B RGTR	27
ECSENF	ENABLE F RGTR	27
F46X·ES115	$F_{0-17} \rightarrow I15_{0-17}$	8
ECS214		27
ES1115	$I15_{0-59} \rightarrow I5_{48-95}$	27
15285	(I5S4·$\overline{I5S2}$·$\overline{I5S1}$)	7
ECS214		27
ECSENC	ENABLE C RGTR	27
ES214	[F17=1]	27
A0R	SET A0R	17

TERM NAME	COMMAND OR FUNCTION	DPD NO
NE264		27
15085	D → $I5_{48-107}$	7
I5G64		7
15136	(I5S4·$\overline{I5S2}$·$\overline{I5S1}$)	7
NE264		27
NESREQ	COUPLER REQ → ECS XMIT	27
ECS264		27
ECSENB	ENABLE B RGTR	27
EN264		27
ENABAR	ENABLE TEST A0R	17
ST00·$\overline{ST01}$·$\overline{ST02}$	RA → I0	4
NE264		27
SL1013	I0 → I3	12
ECS264		27
ES1312	I3 → I2	27
ENABF	ENABLE F RGTR	13

(Part 1 of 2)

CONTROL DATA	INSTRUCTION FLOW SEQUENCE - ECS INSTRUCTION - 011, 012	CODE IDENT 34570	D	DWG NO 19981800	REV A
		FIGURE 5-2-29		PAGE NO 5-2-56.1	



TERM NAME	COMMAND OR FUNCTION	DPD NO
ECS314		27
SRAECS	RAE → I1	27
F46X·ES115	$I1_{0-17} \rightarrow I15_{6-23}$	8
ECS314		27
ES1115	$I15_{0-59} \rightarrow I5_{48-95}$	27
I5285		7
ECS314		27
ECS15C	COMP I5	27
ECS314		
ECSENF	ENABLE F RGTR	27
ECSENC	ENABLE C RGTR	27

TERM NAME	COMMAND OR FUNCTION	DPD NO
ECS364		27
SFLECS	FLE → I1	27
F46X·ES115	$I1_{0-17} \rightarrow I15_{6-23}$	8
ECS364		27
ES1115	$I15_{0-59} \rightarrow I5_{48-95}$	27
I5285		7
ECS364		27
ECS15C	COMP I5	27
ECS364		
ECSEND	ENABLE D RGTR	27
ECSENC	ENABLE C RGTR	27

TERM NAME	COMMAND OR FUNCTION	DPD NO
ECS414		27
SETADR	[LEAC] SET ADR	17

TERM NAME	COMMAND OR FUNCTION	DPD NO
ECS464	[EIUDIRF]	
IIESETR	ENABLE RII [ERRUBT]	27
ESERRX	ENABLE SEQ EXIT	27

(Part 2 of 2)

	INSTRUCTION FLOW SEQUENCE : ECS INSTRUCTION : OII, O12	CODE IDENT 34570	D	DWG. NO. 19961800 REV A
		FIGURE 5-2-29		PAGE NO 5-2-56.2

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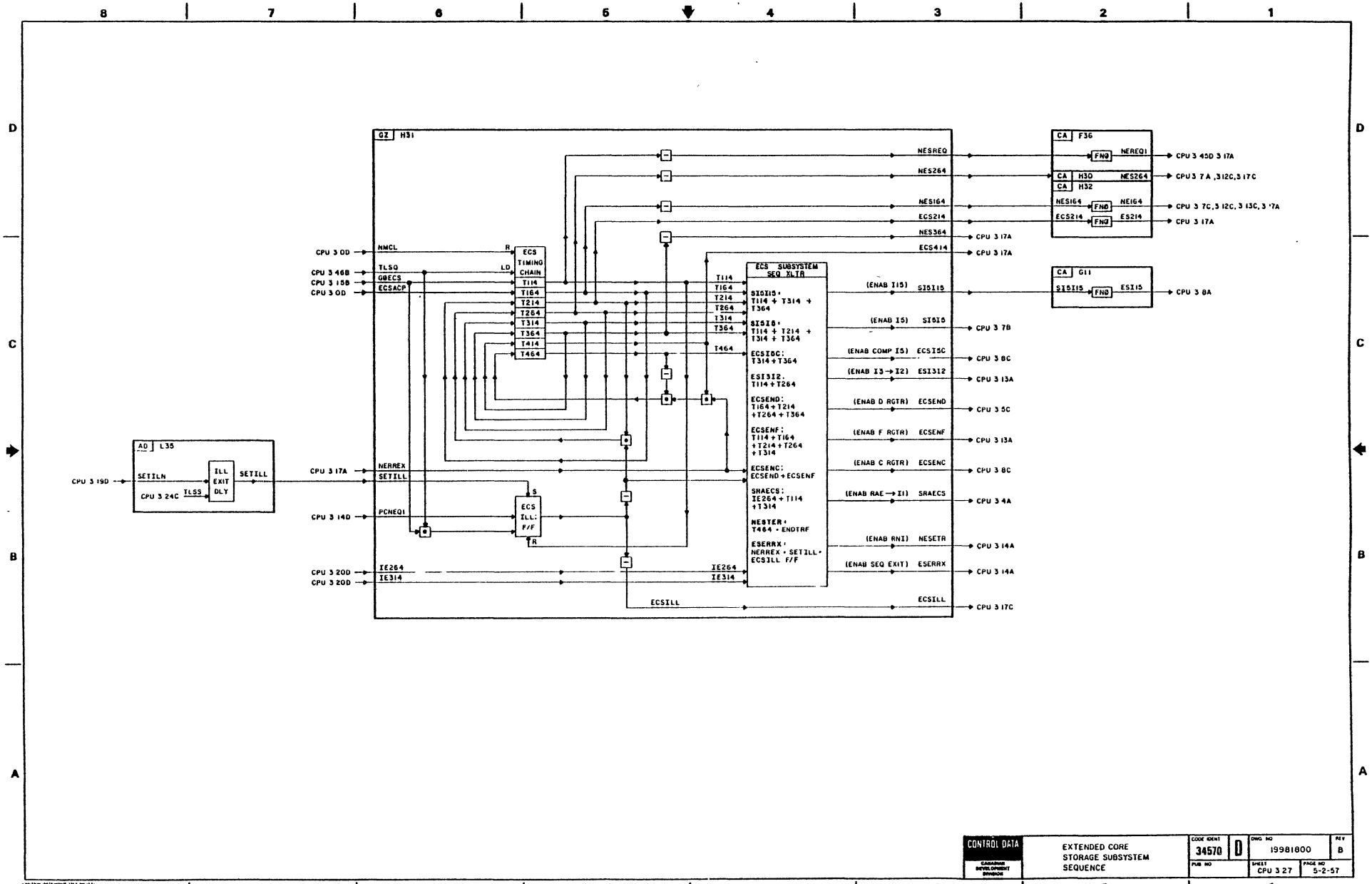
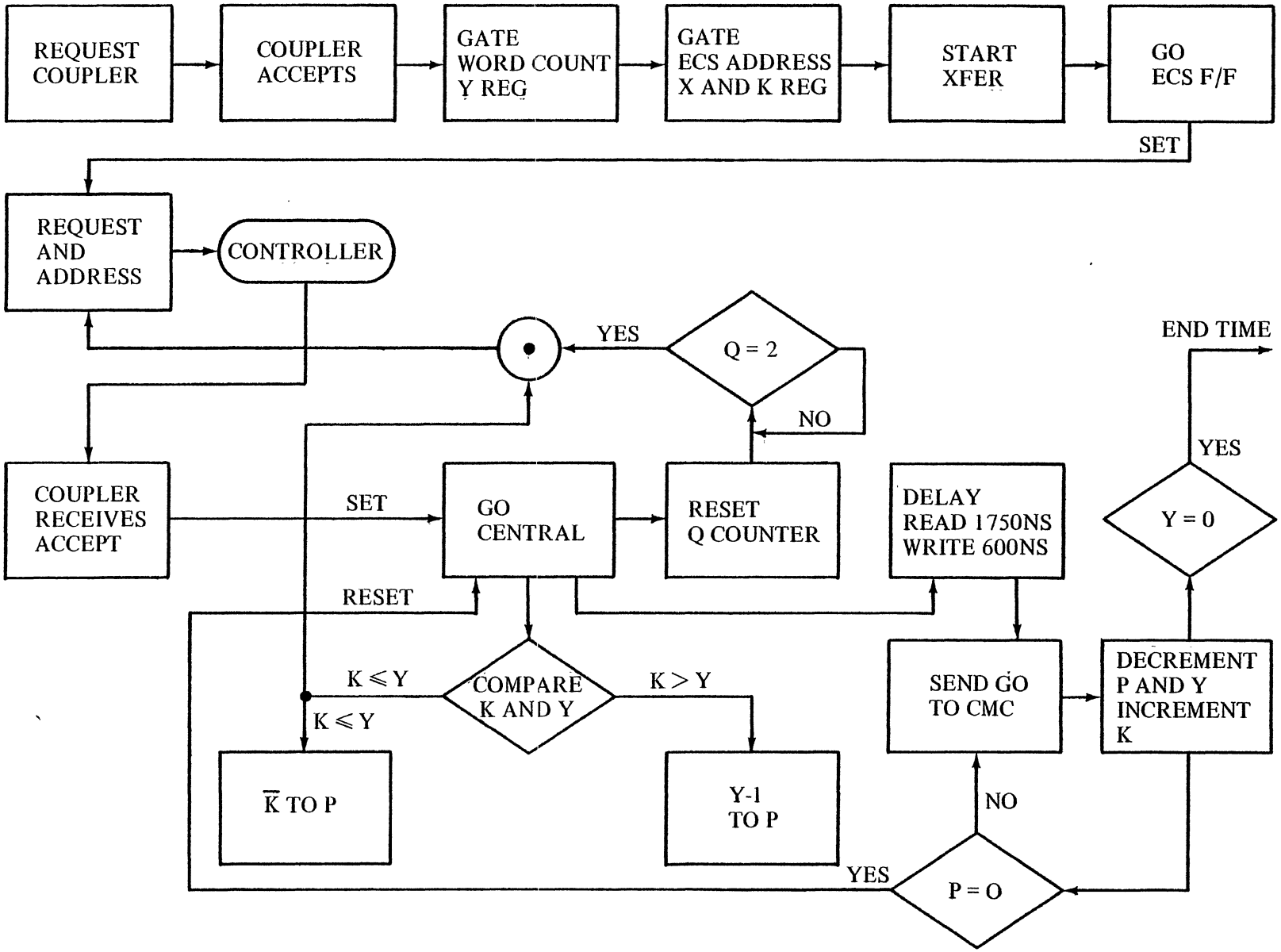


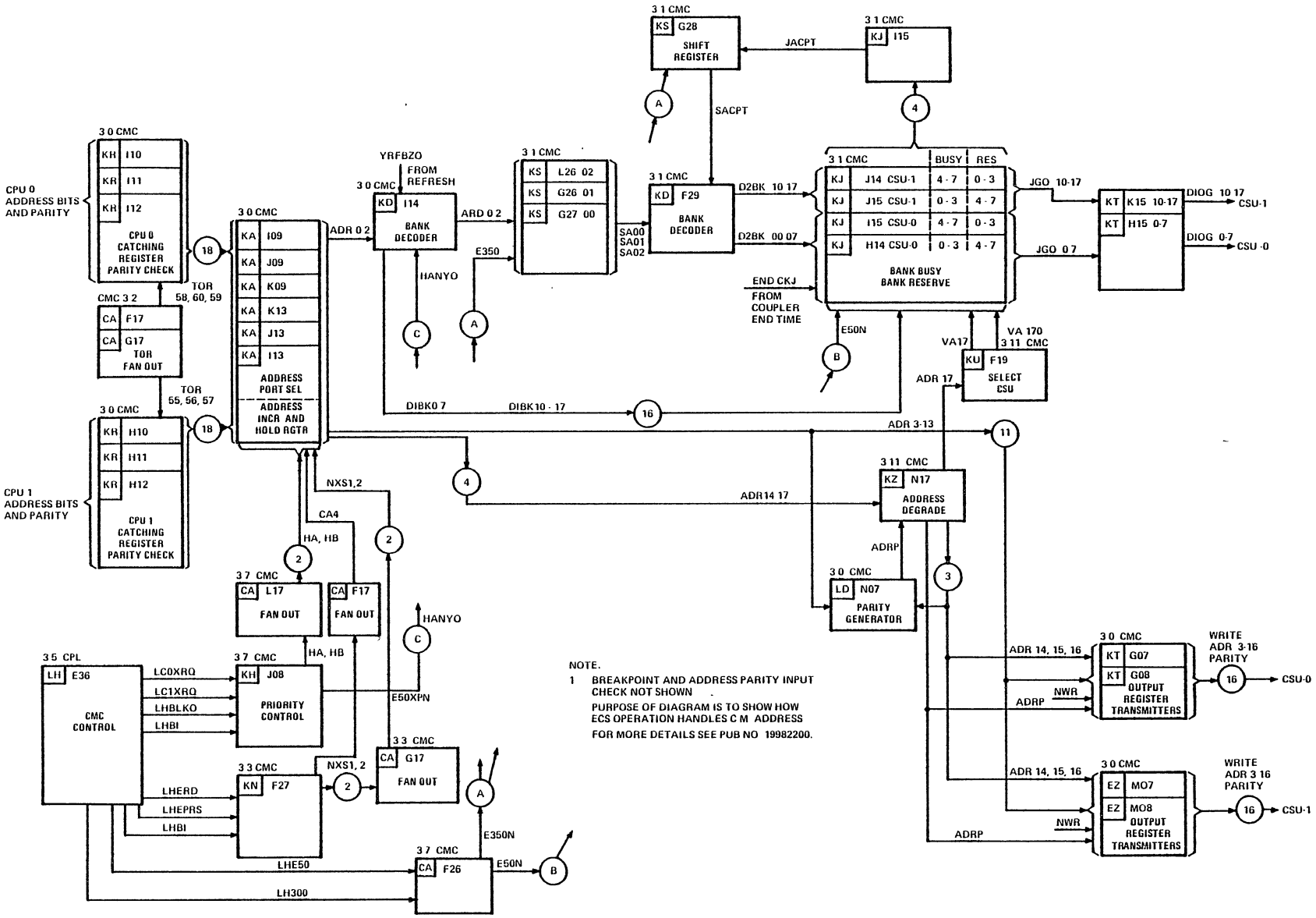
CONTROL DATA	EXTENDED CORE STORAGE SUBSYSTEM SEQUENCE	CODE IDENT 34570	D	DWG NO 19981800	REV B
		PUB NO		SHEET CPU 3 27	PAGE NO 5-2-57

173 COUPLER FLOWCHART (CONTROL)

END TIME NOT SHOWN

FAKE READ NOT SHOWN




3 1 CMC
KS G28
SHIFT REGISTER
JACPT
3 1 CMC
KJ I15
SACPT
3 0 CMC
KH I10
KR I11
KR I12
CPU 0 CATCHING REGISTER PARITY CHECK
CPU 0 ADDRESS BITS AND PARITY
TOR 58, 60, 59
CMC 3 2
CA F17
CA G17
TOR FAN OUT
TOR 55, 56, 57
3 0 CMC
KR H10
KR H11
KR H12
CPU 1 CATCHING REGISTER PARITY CHECK
CPU 1 ADDRESS BITS AND PARITY
3 0 CMC
KA I09
KA J09
KA K09
KA K13
KA J13
KA I13
ADDRESS PORT SEL
ADDRESS INCR AND HOLD RGTR
ADR 0 2
YRFBZO
FROM REFRESH
3 0 CMC
KD I14
BANK DECODER
ARD 0 2
HANYO
E350
3 1 CMC
KS L26 02
KS G26 01
KS G27 00
SA00
SA01
SA02
3 1 CMC
KD F29
BANK DECODER
D2BK 10 17
D2BK 00 07
END CKJ FROM COUPLER END TIME
3 1 CMC
BUSY
RES
KJ J14 CSU-1 4 - 7 0 - 3
KJ J15 CSU-1 0 - 3 4 - 7
KJ I15 CSU-0 4 - 7 0 - 3
KJ H14 CSU-0 0 - 3 4 - 7
BANK BUSY BANK RESERVE
JGO 10-17
JGO 0 7
KT K15 10-17
KT H15 0-7
DIOG 10 17
CSU-1
DIOG 0-7
CSU-0
E50N
VA17
VA 170
3 11 CMC
KU F19
SELECT CSU
ADR 17
DIBK0 7
DIBK10 - 17
ADR 3-13
3 11 CMC
KZ N17
ADDRESS DEGRADE
ADR14 17
ADRP
3 0 CMC
LD N07
PARITY GENERATOR
NXS1,2
CA4
HA, HB
3 7 CMC
CA L17
FAN OUT
CA F17
FAN OUT
HANYO
HA, HB
3 5 CPL
LH E36
CMC CONTROL
LC0XRQ
LC1XRQ
LHBLKO
LHBI
3 7 CMC
KH J08
PRIORITY CONTROL
E50XPN
3 3 CMC
CA G17
FAN OUT
NXS1, 2
3 3 CMC
KN F27
LHERD
LHEPRS
LHBI
LHE50
LH300
3 7 CMC
CA F26
E350N
E50N
ADR 14, 15, 16
ADRP
NWR
3 0 CMC
KT G07
KT G08
OUTPUT REGISTER TRANSMITTERS
WRITE ADR 3-16 PARITY
CSU-0
ADR 14, 15, 16
ADRP
NWR
3 0 CMC
EZ MO7
EZ MO8
OUTPUT REGISTER TRANSMITTERS
WRITE ADR 3 16 PARITY
CSU-1
NOTE.
1 BREAKPOINT AND ADDRESS PARITY INPUT CHECK NOT SHOWN
PURPOSE OF DIAGRAM IS TO SHOW HOW ECS OPERATION HANDLES C M ADDRESS
FOR MORE DETAILS SEE PUB NO 19982200.

L7031

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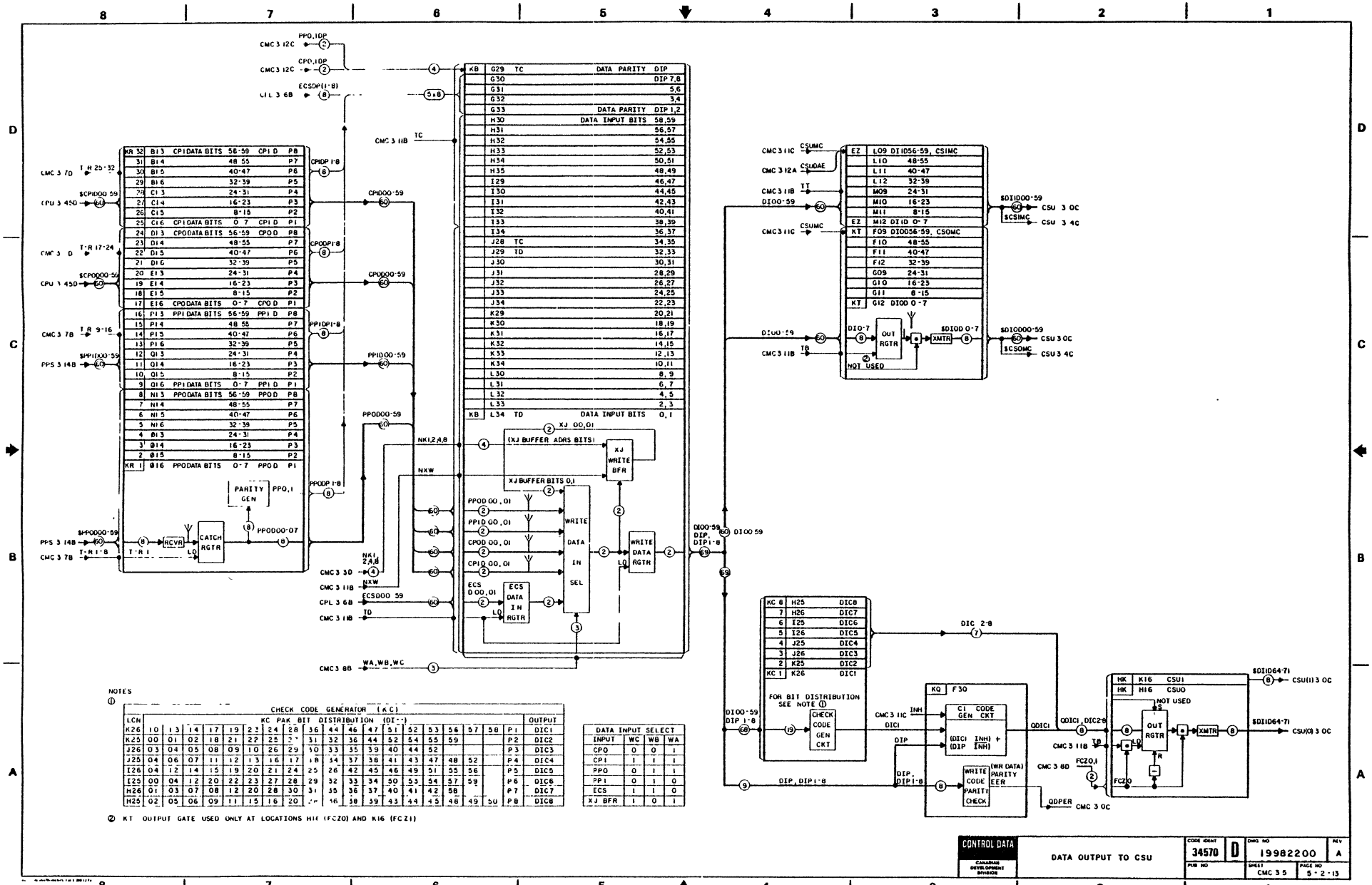


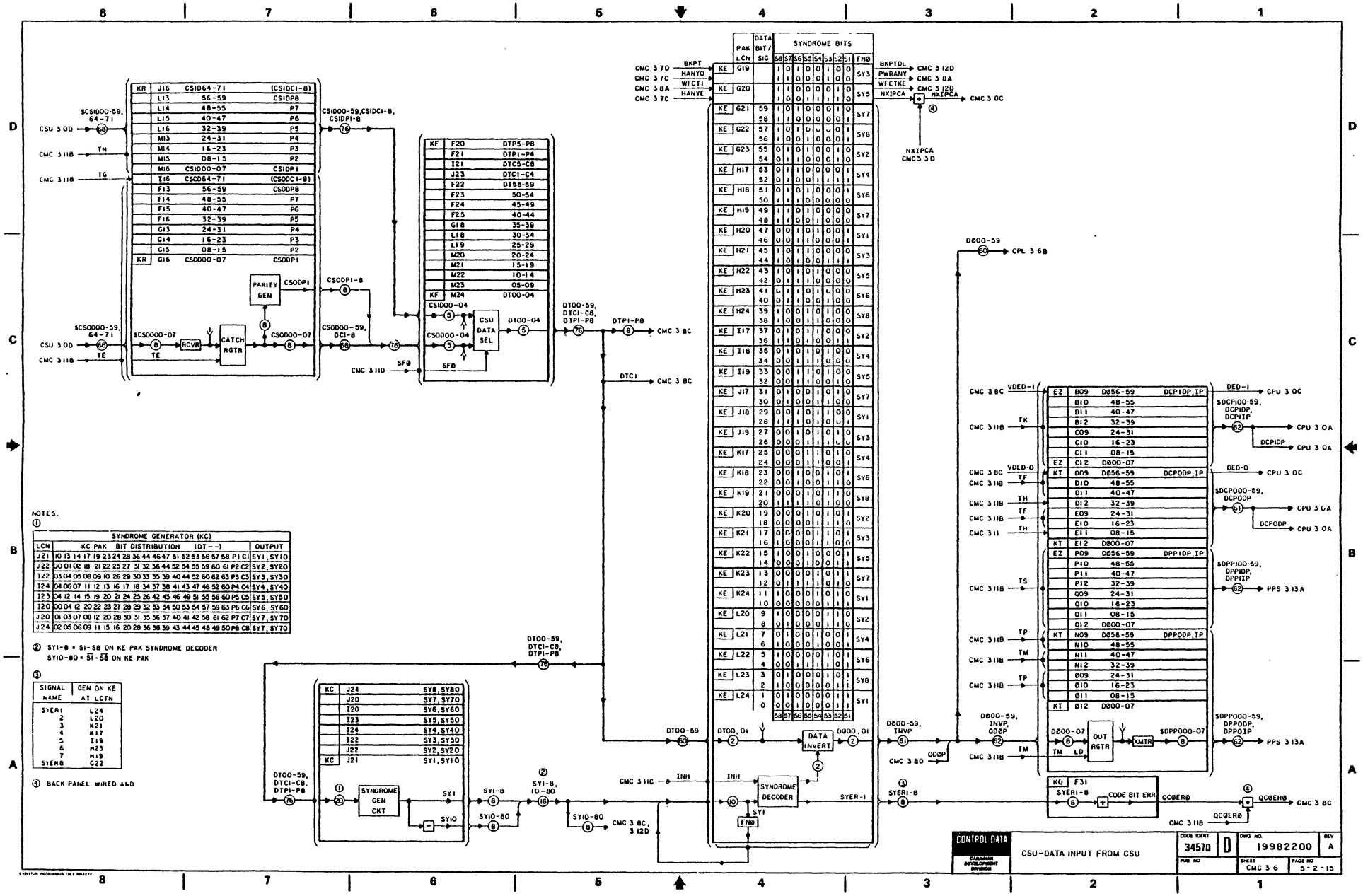
NOTES

① CHECK CODE GENERATOR (KC)

LCN	KC PAK BIT DISTRIBUTION (DI-)																	OUTPUT
K26	10	13	14	17	19	23	24	28	36	44	46	47	51	52	53	56	57	58	P1	DIC1
K25	00	01	02	18	21	22	25	27	31	32	36	44	52	54	55	59			P2	DIC2
J26	03	04	05	08	09	10	26	29	30	33	35	39	40	44	52				P3	DIC3
J25	04	06	07	11	12	13	16	17	18	34	37	38	41	43	47	48	52		P4	DIC4
I26	04	12	14	15	19	20	21	24	25	26	42	45	46	49	51	55	56		P5	DIC5
I25	00	04	12	20	22	23	27	28	29	32	33	34	50	53	54	57	59		P6	DIC6
H26	01	03	07	08	12	20	28	30	31	35	36	37	40	41	42	58			P7	DIC7
H25	02	05	06	09	11	15	16	20	27	46	38	39	43	44	45	48	49	50	P8	DIC8

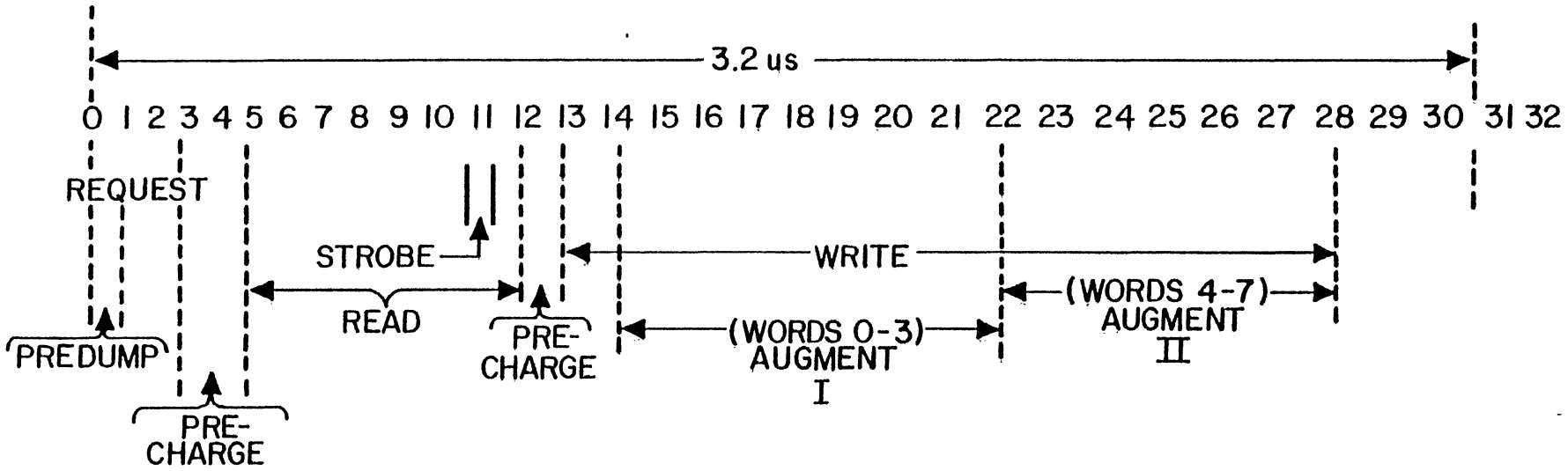
DATA INPUT SELECT			
INPUT	WC	WB	WA
CPO	0	0	1
CPI	1	1	1
PPO	0	1	1
PPI	0	1	0
ECS	1	1	0
XJ BFR	1	0	1

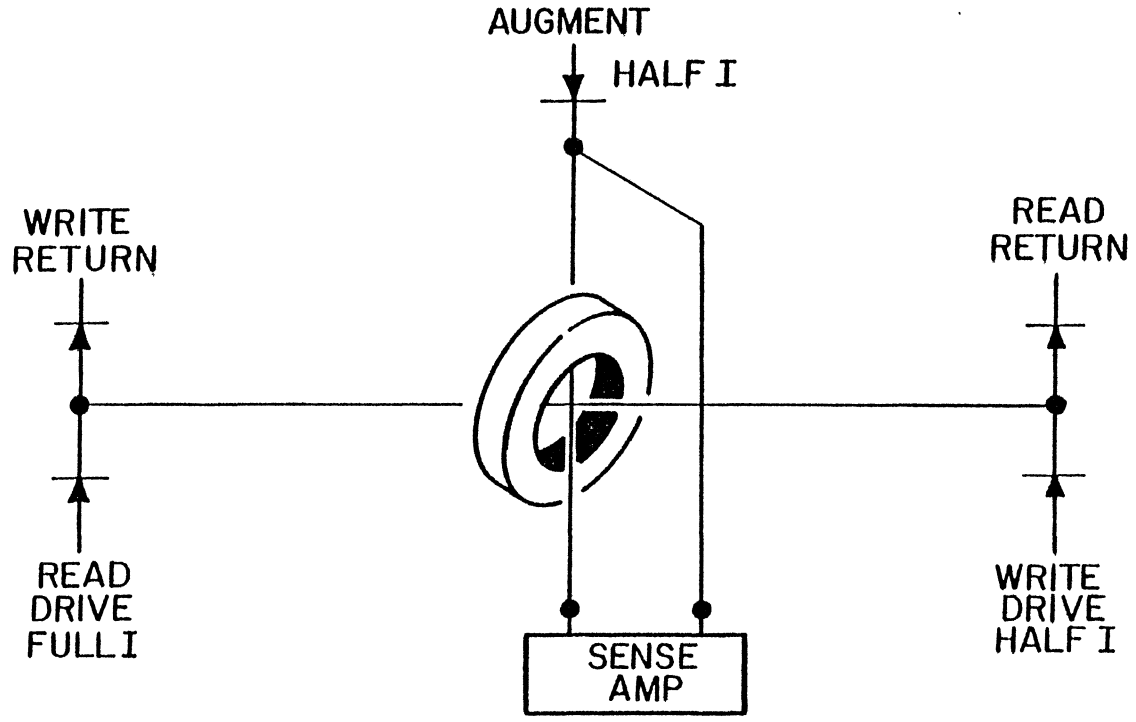
② KT OUTPUT GATE USED ONLY AT LOCATIONS H16 (FCZO) AND K16 (FCZ1)


CSU 3 0D
CMC 3 11B
CMC 3 11C
CMC 3 11D
CMC 3 8C
CMC 3 8D
CMC 3 8A
CMC 3 7D
CMC 3 7C
CPL 3 6B
CPU 3 0C
CPU 3 0A
PPS 3 13A
CMC 3 12D
CMC 3 0C
CSU DATA SEL
PARITY GEN
RCVR
CATCH AGTR
SYNDROME GEN CKT
SYNDROME DECODER
DATA INVERT
OUT AGTR
CODE BIT ERR
NOTES.
SYNDROME GENERATOR (KC)
SYNDROME BITS
CONTROL DATA
CSU-DATA INPUT FROM CSU
34570
19982200
CMC 3 6
5-2-15

L7031

STORAGE REFERENCE CYCLE ECS





HO-57/TR-3

BASIC STACK OPERATION

INTRODUCTION

ECS uses a 2-wire, word-oriented memory. The horizontal wire, or word line, is a drive line; the vertical wire is both a drive line (on a write) and a sense line (on a read).

An ECS stack stores 131,072 60-bit words. The 60-bit words are grouped into 488-bit ECS words. One ECS word holds eight 60-bit words and eight parity bits. One parity bit is used for each 60-bit word.

The stack has eight planes with core mats on each side. Each plane holds 16,384 60-bit words and each side holds 8,192 60-bit words. Therefore, each side holds 1,024 ECS words.

An ECS word is on one word line across the side. A side is therefore 488 cores wide and 1,024 lines deep.

The vertical lines carry the sense and drive currents. There are 488 of these sense/drive lines per stack, and one line goes through the same bit in each ECS word.

The 60-bit words are not arranged sequentially in an ECS word. Instead, two words are alternated with each other (See Sense Line Alternation on diagram below). Words 1 and 5 occupy the first 122 cores. The first core is bit 0 of word 1 and the next core is bit 0 of word 5 and so on including the parity bit. Words 2 and 6, words 3 and 7, and words 4 and 8 are similarly alternated. The ECS read/write cycle first writes one half of the ECS word and then the other half. Since the sense/drive lines are alternated, only every other sense/drive line can be active at any time.

When reading, the whole ECS word is read out at the same time. Both ends of the sense line are fed into sense the amplifier, (See Sense Line Detail on diagram below). The mid-point of the sense line is used to send drive current during the write operation. (See Sense Line Path on diagram below).

READ/WRITE OPERATION

Only one 488-bit word line is selected at one time. The word line is selected partially by a diode matrix and partially by the logic modules. The addressing bits enable a path to ground from a current source called the dummy (ZU module). The direction of the current is dependent upon which dummy is turned on and which pair of Drive/Return FFs are set. It is not dependent on the address bits. The read/write cycle is controlled by a timer which turns on the dummies and sets Read/Write FFs.

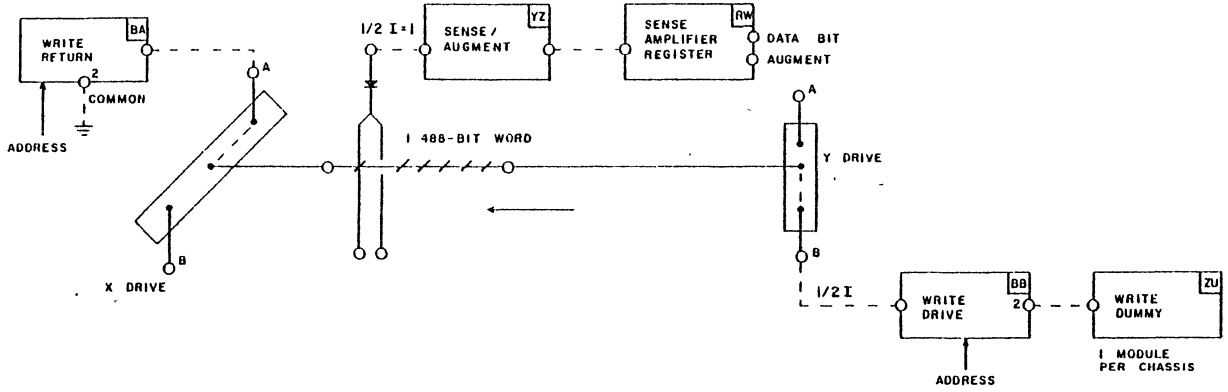
On write operations the address enables an exclusive path from the dummy to ground through the word line, (See Write on diagram below). It does this by selecting one word line by means of the write return modules and the write drive modules. Half current is then sent through this word line. If a "1" is to be stored, then half current is sent down the appropriate sense/drive line. This half current is a combination of a "1" from the data register (Sense Amplifier register) and an Augment signal. The Augment signal is used to provide sufficient current for the write. (It also controls the writing of one half of the ECS word or the other.) A core receiving full current (half from the drive line, and half from the sense line) will switch to the "1" state.

On a read operation, the line is selected and full current is sent through the line but in the reverse direction to the write operation (See Read on diagram below). All cores in the "1" state switch to a "0" and are sensed by the Sense Amplifier modules. Note that the same module type is used for the read and write dummies. This module is adjustable and can have either a half current output (write dummy) or full current output (read dummy).

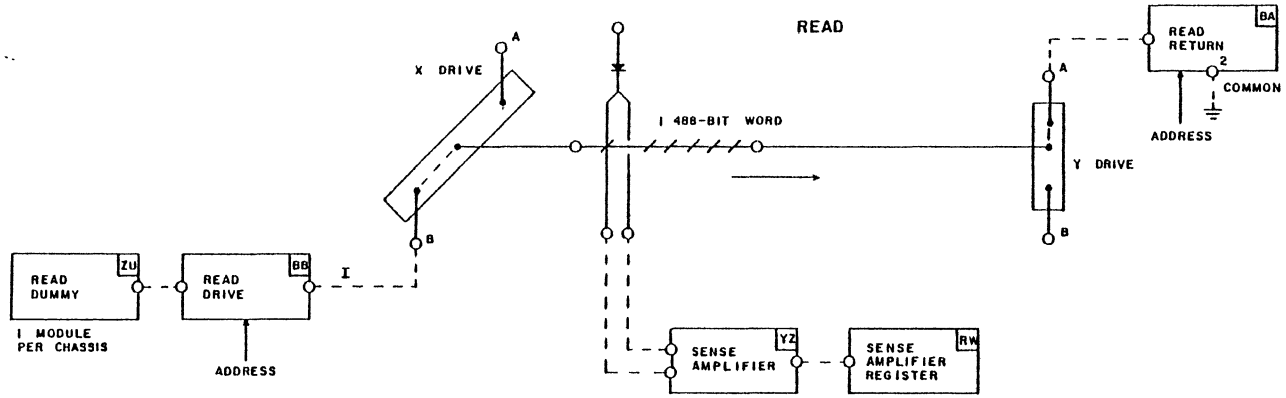
L7031

HO-59/TR-10

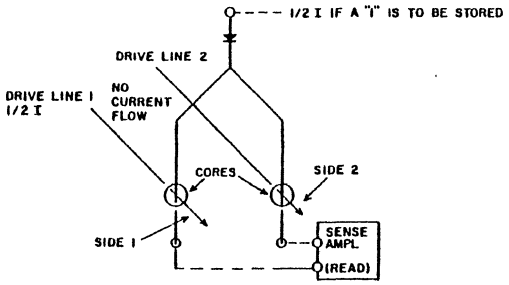
WRITE



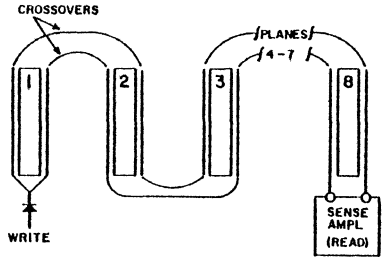
READ



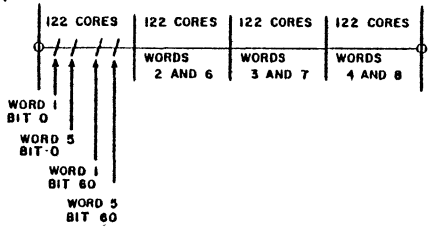
SENSE LINE DETAIL



SENSE LINE PATHS



SENSE LINE ALTERNATION



CONTROL DATA CORPORATION	TITLE	PRODUCT
DEVELOPMENT	BASIC STACK OPERATION	ECS STACK ASSEMBLY
		SIZE C · DRAWING NO 60217600 · REV. A

SELECTION OF ONE WORD BY A DIODE MATRIX

The diagram shows part of the diode matrix. Note that the diodes are used primarily to direct current flow and not to implement addressing. The same address bits enable both the write return module and the read drive module; that is, one end of the word line. The remainder of the address bits enable the other end of the word line; that is, the write drive module and the read return module. The direction of current flow is therefore determined by which pair of modules (read or write) is enabled. This in turn is done by four FFs which direct the address bits to the modules as the read/write cycle progresses.

These four FFs* and the dummies are turned on and off by a bank timer which controls the whole cycle.

The write return and read drive modules are designated the X-drive. The outputs of these modules are connected to either end of the X-drive diode packs. One such diode pack has eight word line connections. Therefore, when the read drive or the write return module are selected, eight word lines are also selected.

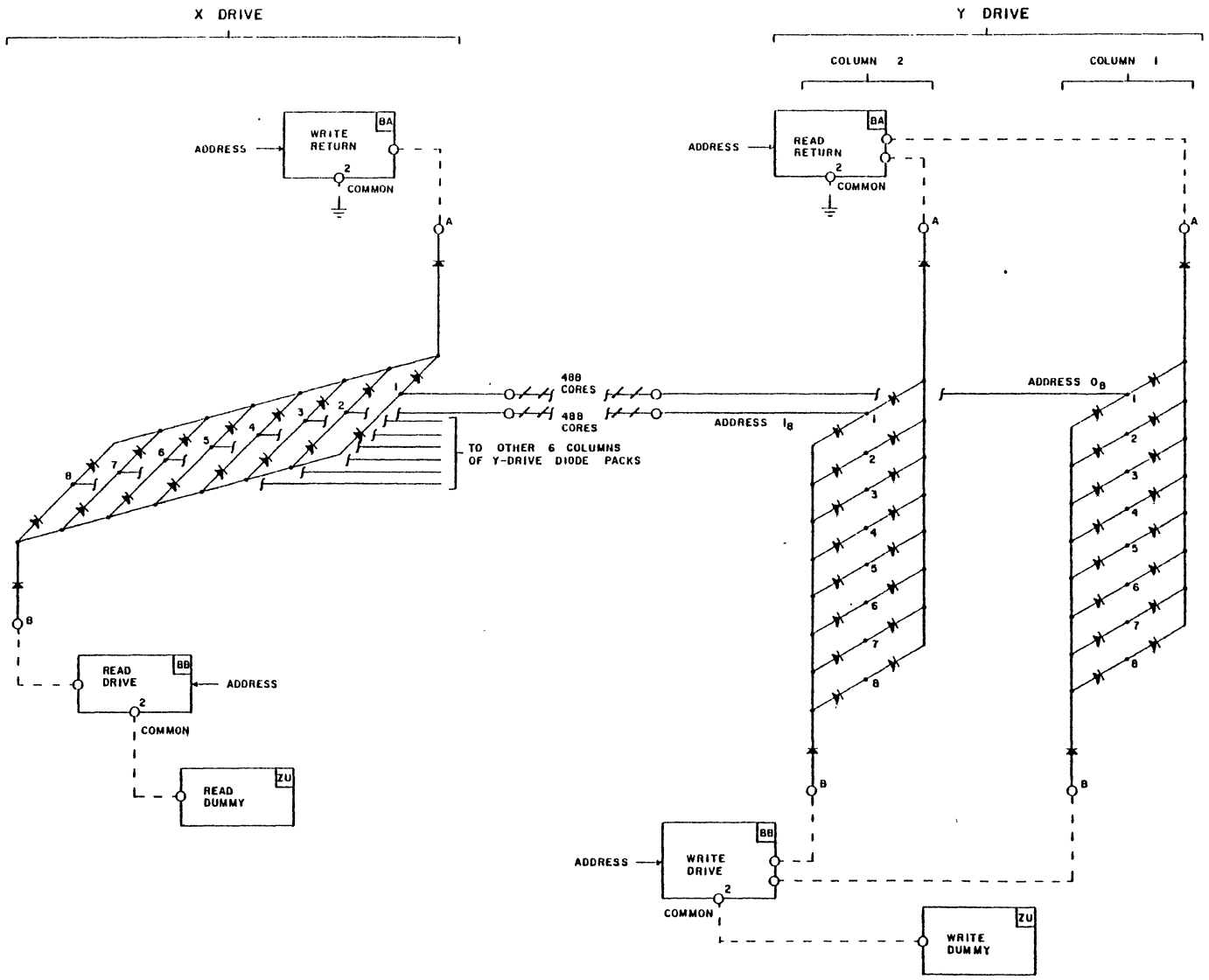
*Write Return FF, Read Return FF, Write Drive FF, and Read Drive FF. There is a fifth FF that turns on the read dummy; the Write Drive FF also turns on the write dummy. These FFs are not shown in these diagrams.

The write drive and read return modules are designated the Y-drive. The outputs of these modules are again connected to either end of the Y-drive diode pack. These packs extend down the side of the plane in columns. One connection on a Y-drive column goes to one connection on the X-drive diode pack. The next connection on this X-drive diode pack goes to the next Y-drive column. Therefore, each consecutive connection of a Y-drive column goes to a different X-drive diode pack; or each consecutive connection on an X-drive diode pack goes to eight different Y-drive columns.

When one Y-drive column and one X-drive diode pack are selected, a single word line is selected. The next Y-drive column will have to be selected for the next word line down the plane.

When this single line is selected, current will flow from right to left during the write portion of the cycle; that is, part of the address selects the write return and the remainder of the address selects the write drive. On a read operation, the current flow is from left to right. The same address bits that selected write return will select read drive, and the remainder of the address will select the read return. These are the same bits that selected the write drive.

The dummy modules always are connected to the drive modules; the return modules have the common pin connected to ground.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE SELECTION OF 1 WORD BY A DIODE MATRIX	PRODUCT ECS STACK ASSEMBLY	
		SIZE C	DRAWING NO 60217600
		REV A	
		SHEET	PAGE 1-3

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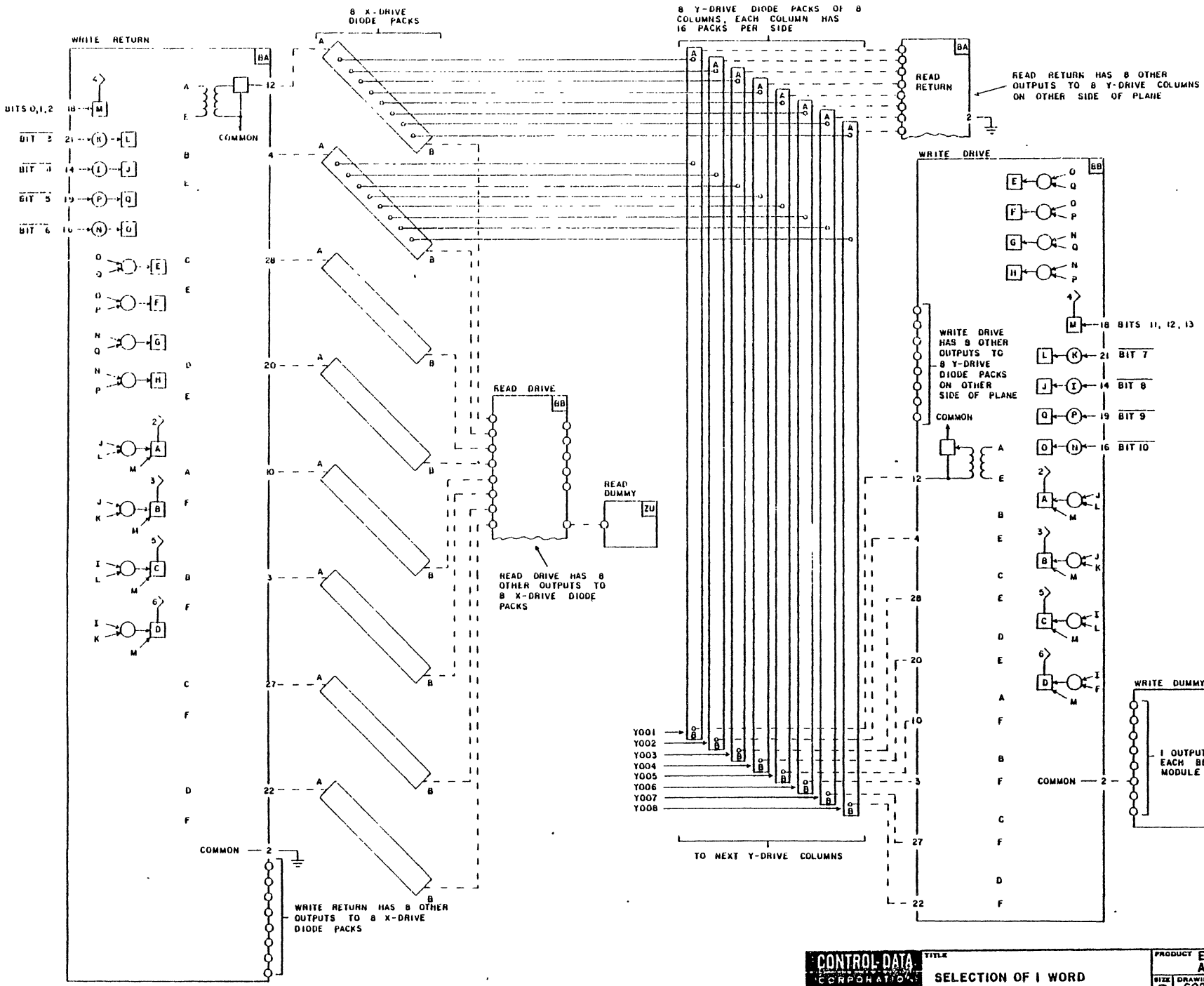
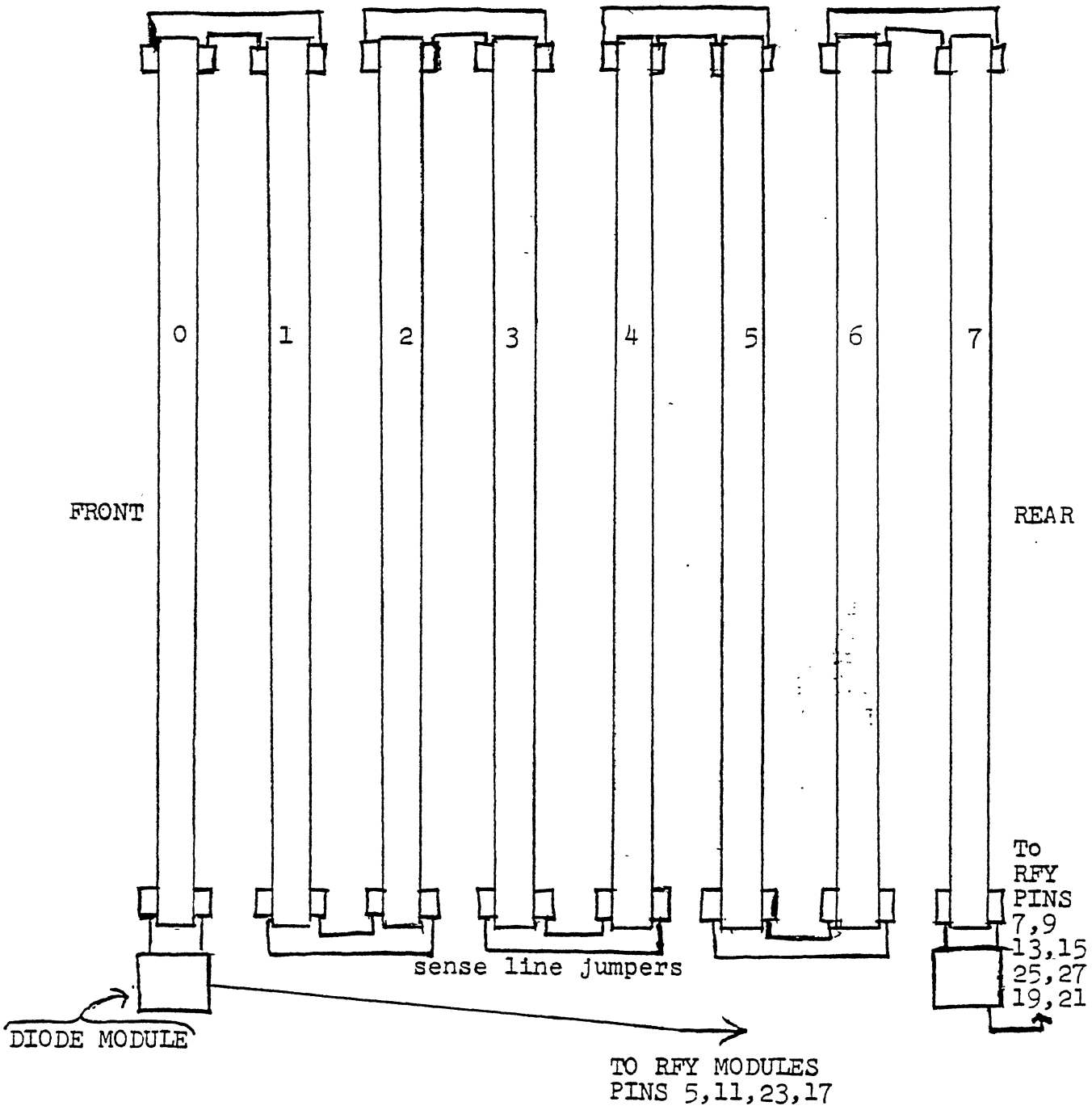
HO-62/TR-12



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE SELECTION OF 1 WORD IN A STRIP	PRODUCT ECS STACK ASSEMBLY	
		SIZE C	DRAWING NO. 60217600 REV. A
		SHEET	PAGE 1-7

SIDE VIEW OF STACK

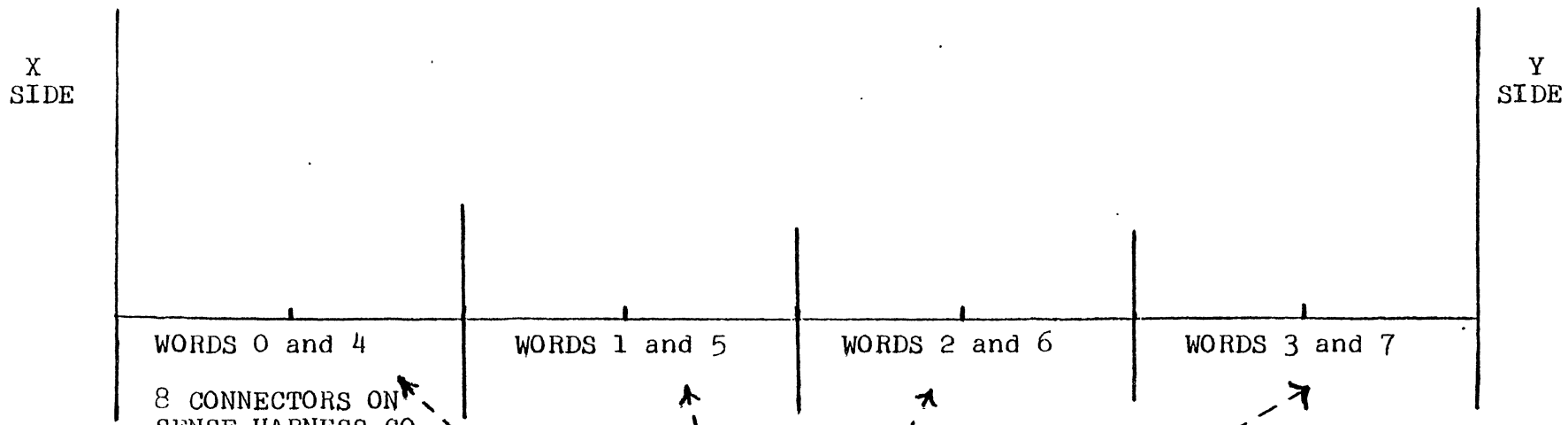


L7031

HO-62B/TR-14

PHYSICAL LOCATIONS

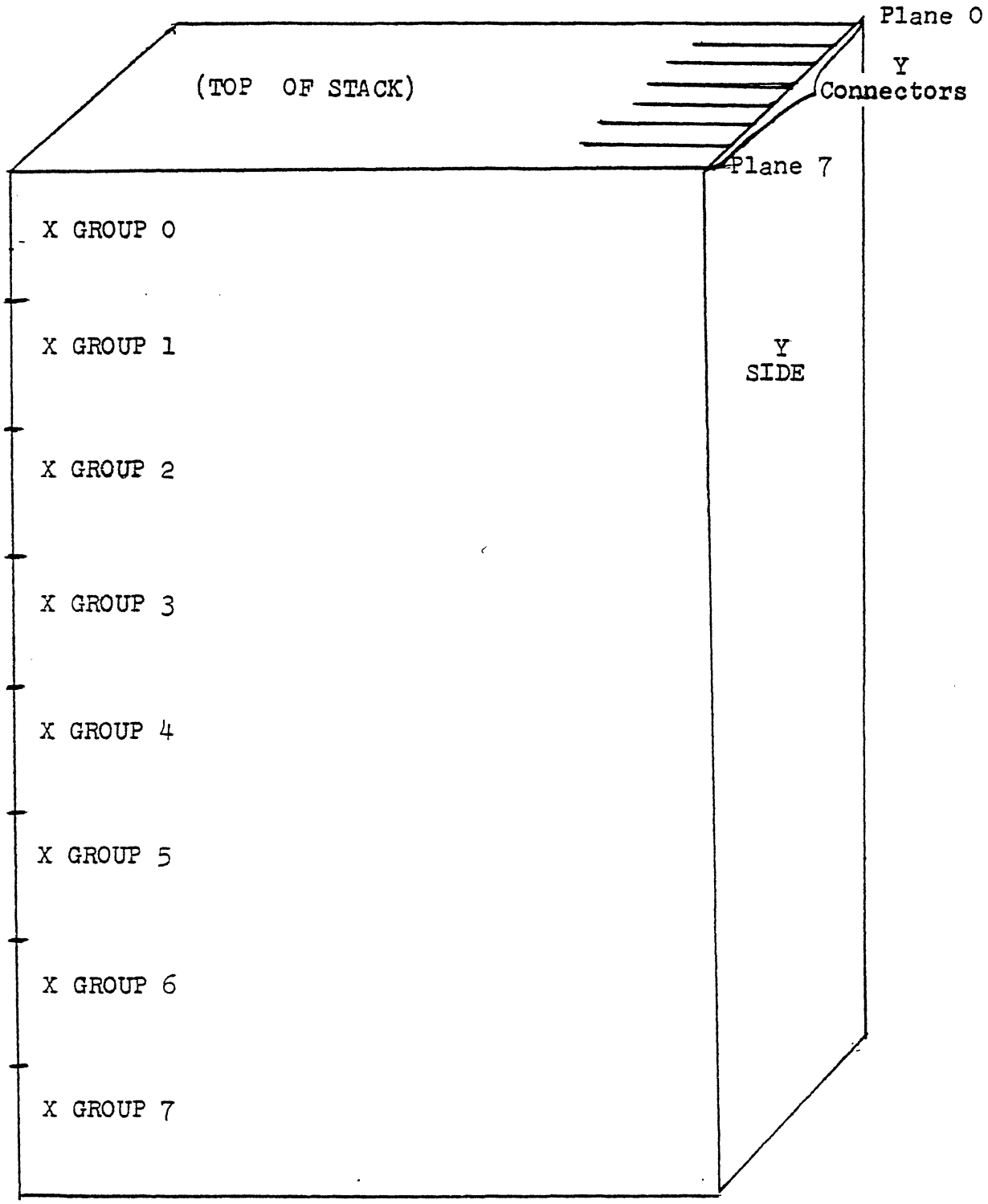
SENSE AND AUGMENT CONNECTORS



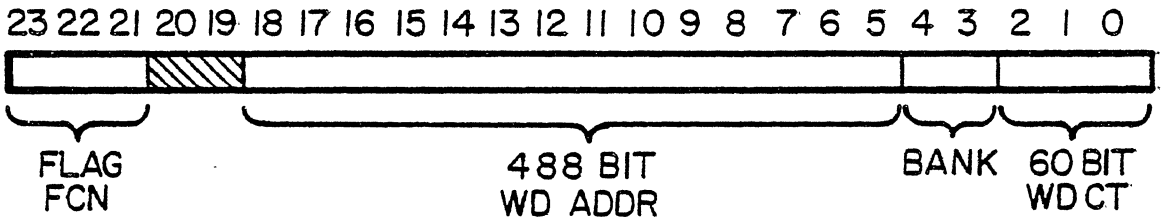
SENSE HARNESS CONNECTORS — BIT POSITION
Each connector is for bits on 2 words.

WORDS								
0 or 1 or 2 or 3 →	0-6	7-14	15-22	23-30	31-37	38-45	46-53	54-60
WORDS 4 or 5 or 6 or 7 →	0-6	7-14	15-22	23-29	30-36	37-44	45-52	53-60

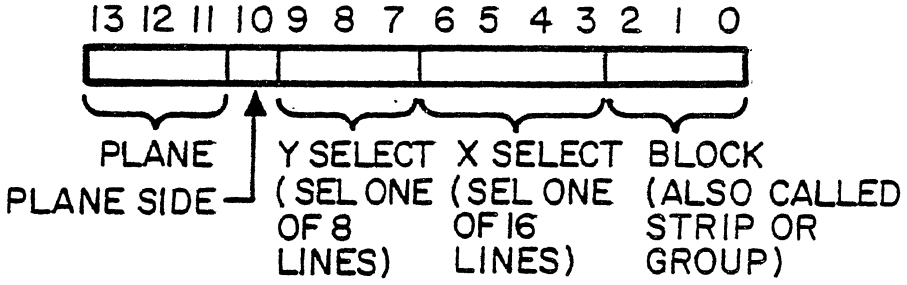
PHYSICAL LOCATIONS X GROUPS

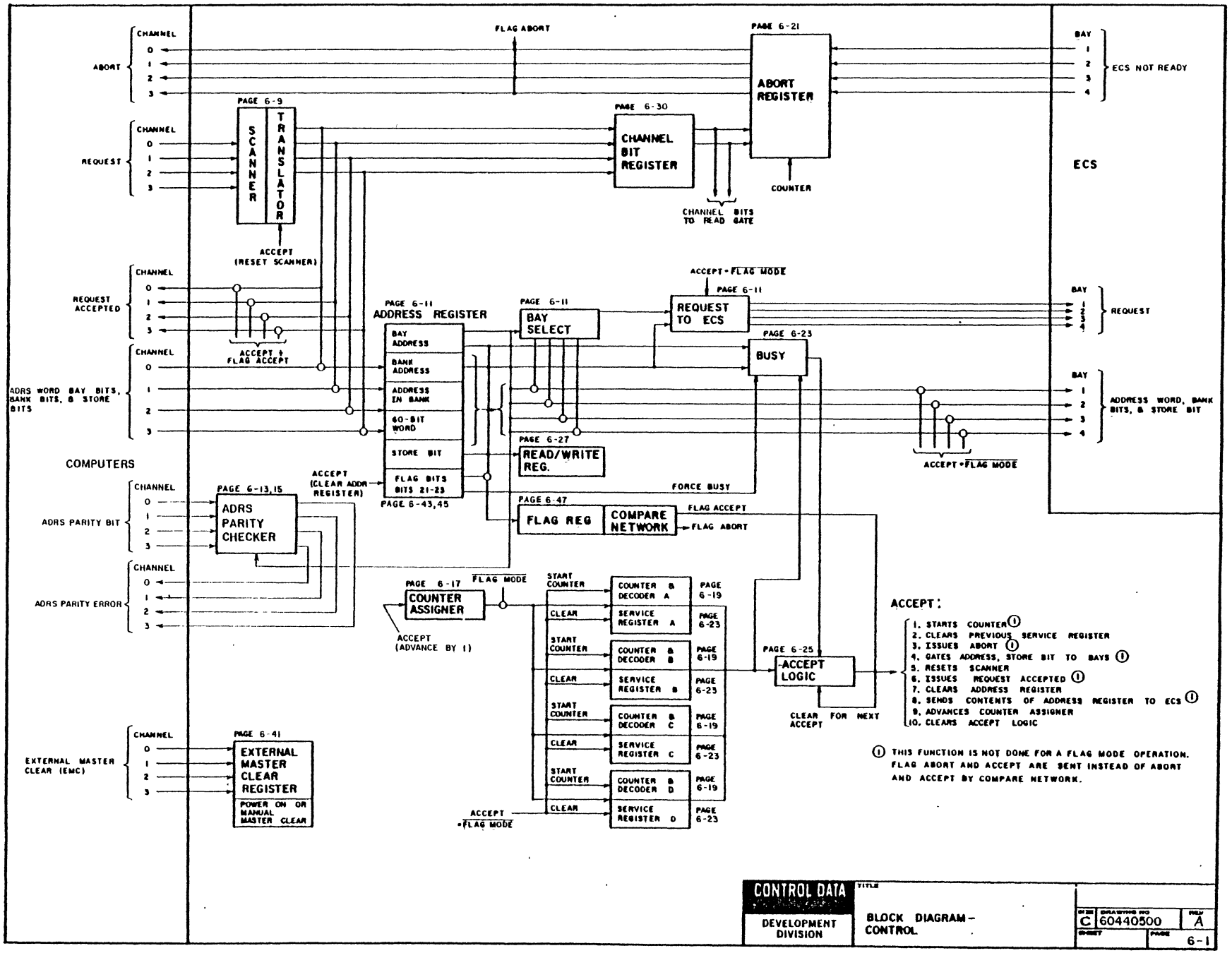


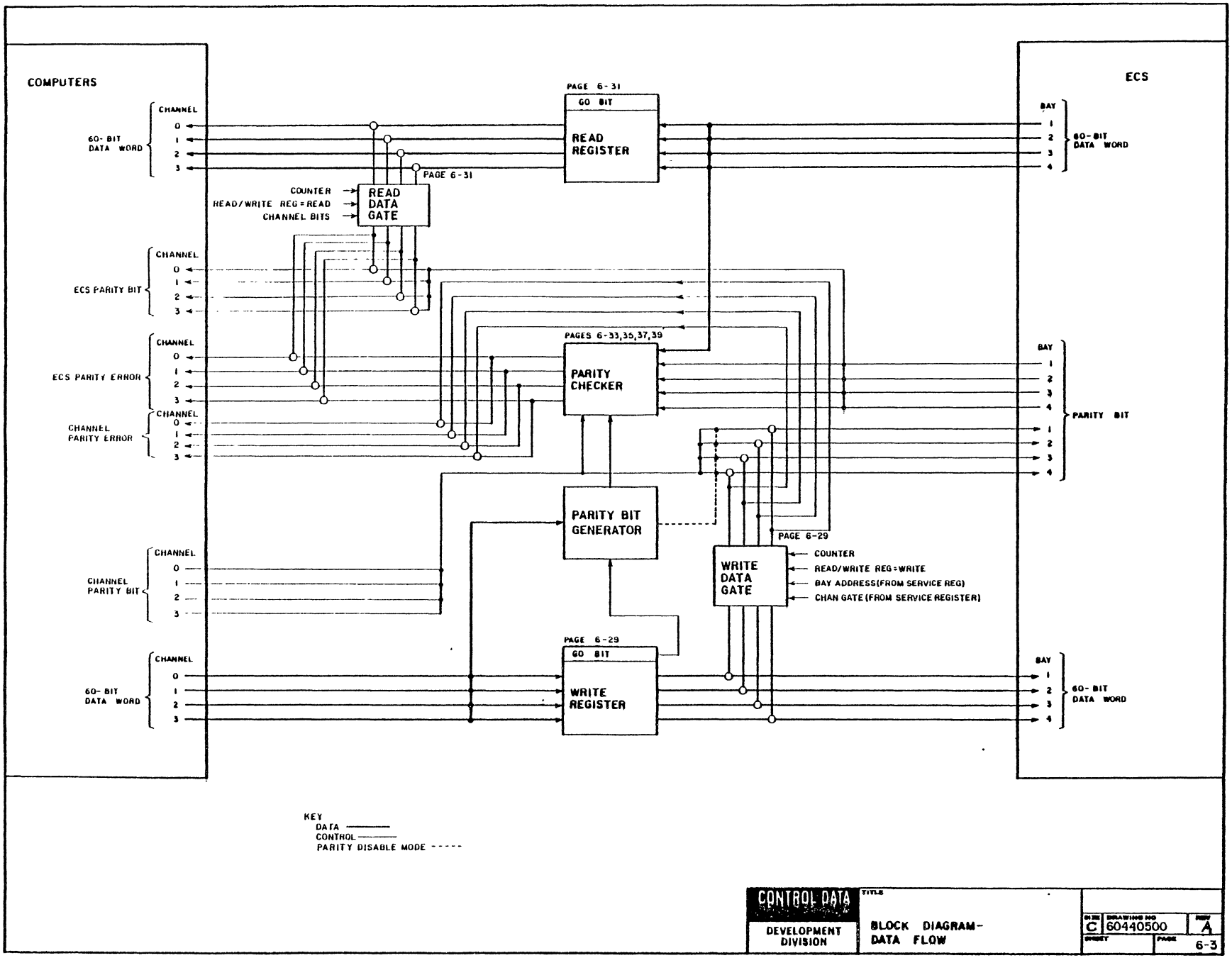
524K ADDRESS FORMAT



488 BIT WD ADDR FORMAT




CHANNEL
ABORT
0
1
2
3
FLAG ABORT
PAGE 6-21
ABORT REGISTER
BAY
ECS NOT READY
ECS
PAGE 6-9
SCANNER
TRANSLATOR
REQUEST
PAGE 6-30
CHANNEL BIT REGISTER
COUNTER
CHANNEL BITS TO READ GATE
ACCEPT (RESET SCANNER)
REQUEST ACCEPTED
ACCEPT • FLAG MODE
PAGE 6-11
REQUEST TO ECS
REQUEST
ACCEPT + FLAG ACCEPT
PAGE 6-11
ADDRESS REGISTER
BAY ADDRESS
BANK ADDRESS
ADDRESS IN BANK
60-BIT WORD
STORE BIT
FLAG BITS BITS 21-23
PAGE 6-43,45
BAY SELECT
PAGE 6-23
BUSY
ADRS WORD BAY BITS, BANK BITS, & STORE BITS
ADDRESS WORD, BANK BITS, & STORE BIT
PAGE 6-27
READ/WRITE REG.
ACCEPT • FLAG MODE
COMPUTERS
ACCEPT (CLEAR ADDR REGISTER)
PAGE 6-13,15
ADRS PARITY CHECKER
FORCE BUSY
PAGE 6-47
FLAG REG
COMPARE NETWORK
FLAG ACCEPT
FLAG ABORT
ADRS PARITY BIT
ADRS PARITY ERROR
PAGE 6-17
COUNTER ASSIGNER
FLAG MODE
ACCEPT (ADVANCE BY 1)
START COUNTER
CLEAR
COUNTER B DECODER A
COUNTER B DECODER B
COUNTER B DECODER C
COUNTER B DECODER D
SERVICE REGISTER A
SERVICE REGISTER B
SERVICE REGISTER C
SERVICE REGISTER D
PAGE 6-19
PAGE 6-23
PAGE 6-25
ACCEPT LOGIC
CLEAR FOR NEXT ACCEPT
ACCEPT:
1. STARTS COUNTER (1)
2. CLEARS PREVIOUS SERVICE REGISTER
3. ISSUES ABORT (1)
4. GATES ADDRESS, STORE BIT TO BAYS (1)
5. RESETS SCANNER
6. ISSUES REQUEST ACCEPTED (1)
7. CLEARS ADDRESS REGISTER
8. SENDS CONTENTS OF ADDRESS REGISTER TO ECS (1)
9. ADVANCES COUNTER ASSIGNER
10. CLEARS ACCEPT LOGIC
(1) THIS FUNCTION IS NOT DONE FOR A FLAG MODE OPERATION. FLAG ABORT AND ACCEPT ARE SENT INSTEAD OF ABORT AND ACCEPT BY COMPARE NETWORK.
EXTERNAL MASTER CLEAR (EMC)
PAGE 6-41
EXTERNAL MASTER CLEAR REGISTER
POWER ON OR MANUAL MASTER CLEAR
ACCEPT • FLAG MODE
CONTROL DATA
DEVELOPMENT DIVISION
TITLE
BLOCK DIAGRAM - CONTROL
SIZE C
DRAWING NO 60440500
REV A
SHEET
PAGE 6-1



CONTROL DATA DEVELOPMENT DIVISION

TITLE: BLOCK DIAGRAM- DATA FLOW

SIZE C | DRAWING NO 60440500 | REV A

SHEET | PAGE 6-3

PARITY CHECK DISABLE

A parity check disable switch is provided for each of the four channels. Parity is disabled when the switch is in the up position. During parity disable, parity bits and address and data parity errors are prevented from being transmitted to the channel. Also during parity disable, parity bits generated in the controller are sent to ECS. This feature provides parity checking of data transmission between the controller and ECS.

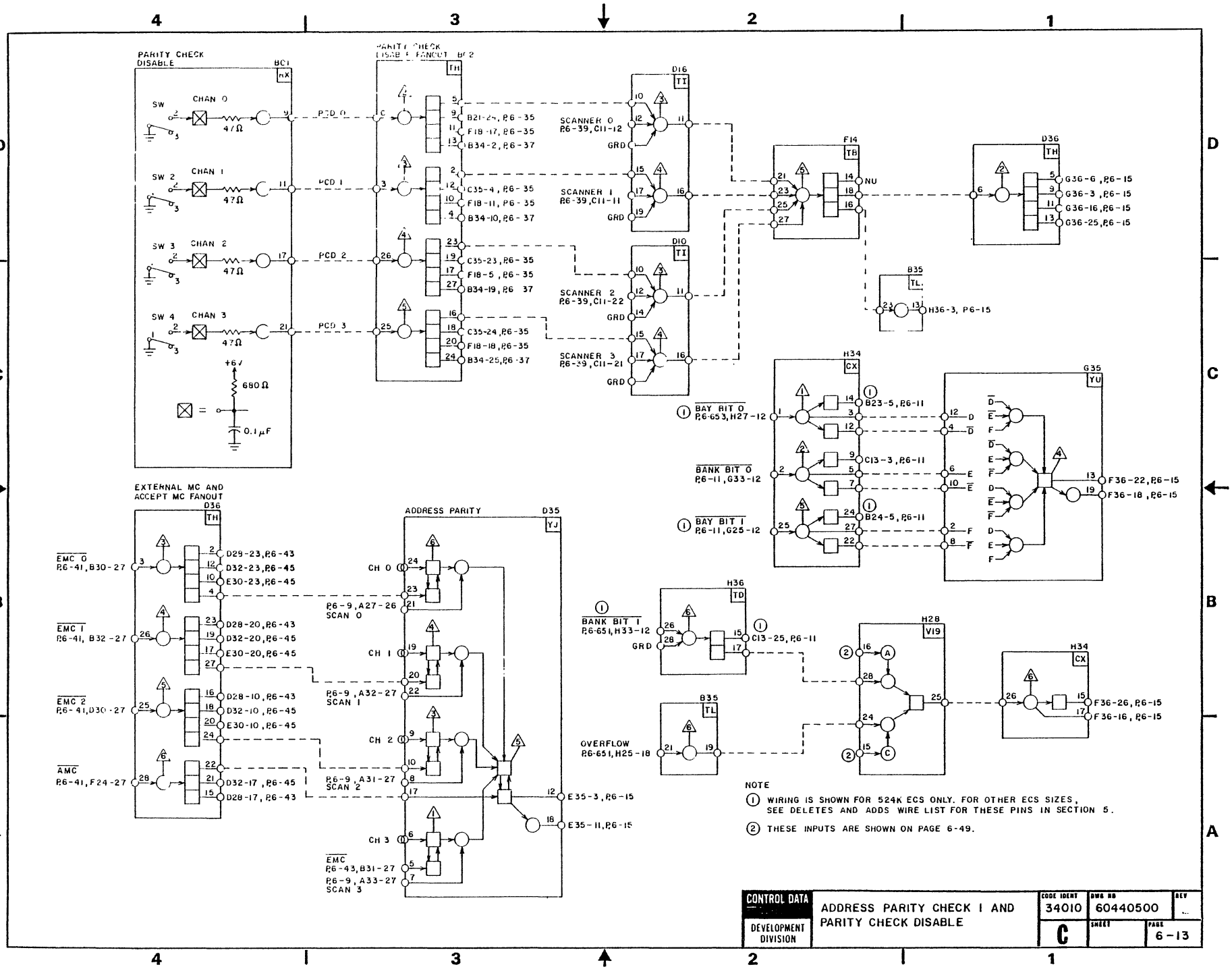
With the switch in the down or enable position, data parity is checked for the channel selected by the scanner. The received parity bit from the channel is also passed on with the data and stored in ECS regardless if a parity error occurred or not.

ADDRESS PARITY

The address parity bit is received by the address register along with the 24 address bits from the channel. The scanner in the controller selects which channel address bits and address parity bit will be gated into the address register. The address parity bit register is cleared by master clear signals from the fanout circuit.

BAY, BANK, AND OVERFLOW BITS

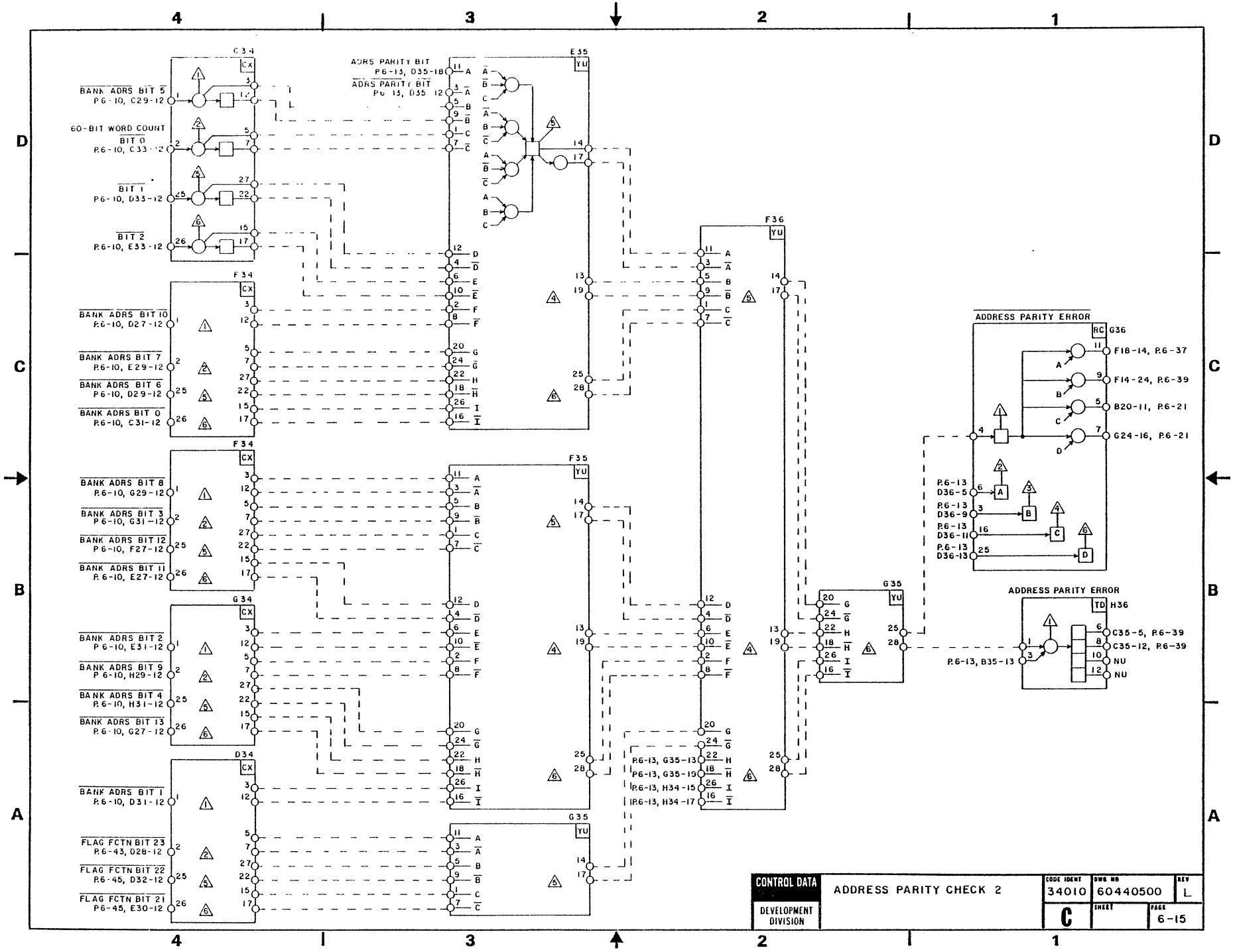
The two bay bits and two bank bits are part of the 24-bit address from the channel. During half ECS mode of operation, one of these bits is switched out of the address network into the overflow network. The bit from the overflow network is then used to determine proper parity checking.

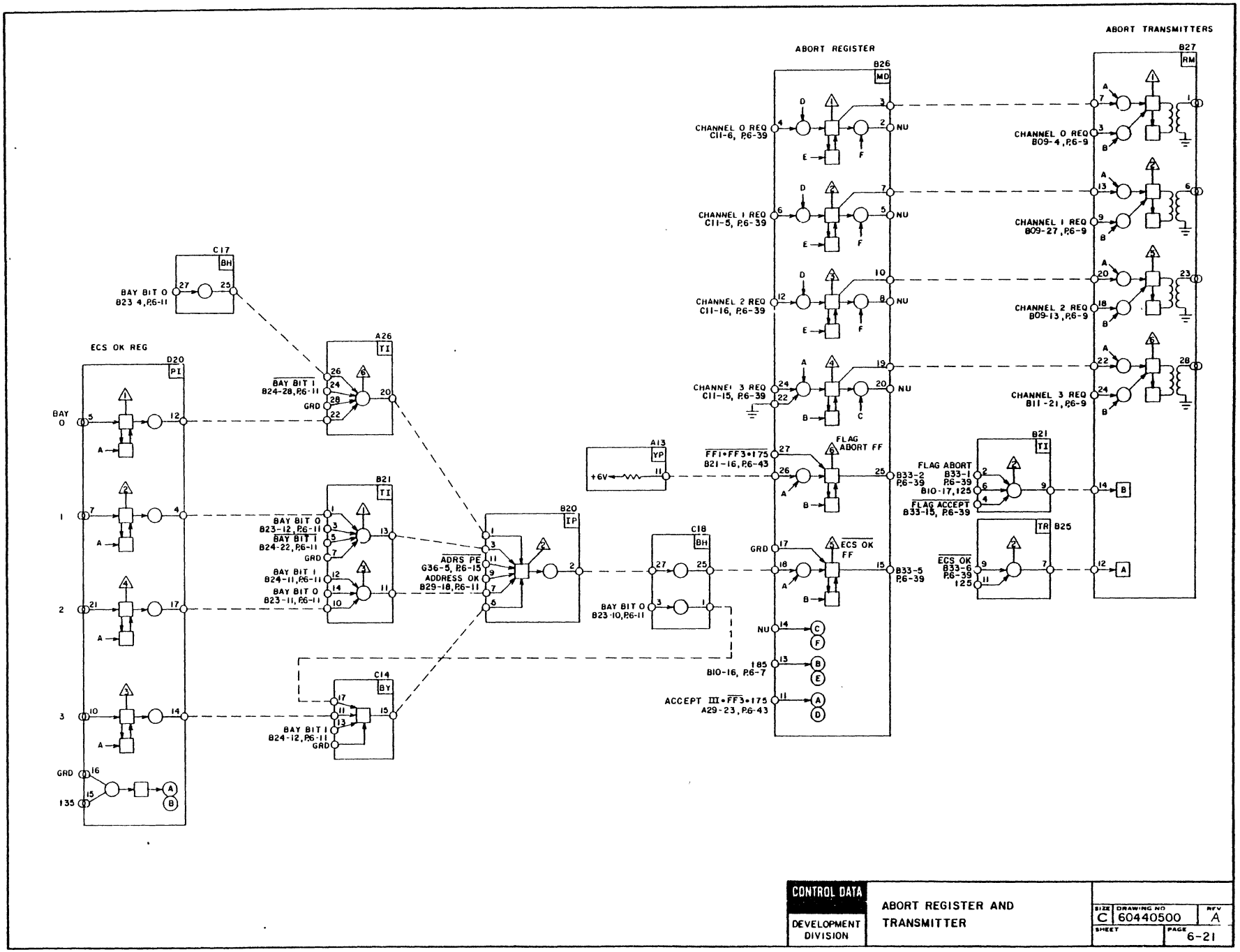

PARITY CHECK DISABLE
BC1
CHAN 0
CHAN 1
CHAN 2
CHAN 3
SW
SW 2
SW 3
SW 4
47Ω
PCD 0
PCD 1
PCD 2
PCD 3
+6V
680Ω
0.1μF
TH
TI
TB
TL
CX
YU
TD
VI9
YJ
SCANNER 0 P6-39,C11-12
SCANNER 1 P6-39,C11-11
SCANNER 2 P6-39,C11-22
SCANNER 3 P6-39,C11-21
GRD
NU
B21-24, P6-35
F18-17, P6-35
B34-2, P6-37
C35-4, P6-35
F18-11, P6-35
B34-10, P6-37
C35-23, P6-35
F18-5, P6-35
B34-19, P6 37
C35-24, P6-35
F18-18, P6-35
B34-25, P6-37
G36-6, P6-15
G36-3, P6-15
G36-16, P6-15
G36-25, P6-15
H36-3, P6-15
BAY BIT 0 P6-653, H27-12
BANK BIT 0 P6-11, G33-12
BAY BIT 1 P6-11, G25-12
B23-5, P6-11
C13-3, P6-11
B24-5, P6-11
F36-22, P6-15
F36-18, P6-15
BANK BIT 1 P6-651, H33-12
C13-25, P6-11
OVERFLOW P6-651, H25-18
F36-26, P6-15
F36-16, P6-15
EXTERNAL MC AND ACCEPT MC FANOUT
EMC 0 P6-41, B30-27
EMC 1 P6-41, B32-27
EMC 2 P6-41, D30-27
AMC P6-41, F24-27
D29-23, P6-43
D32-23, P6-45
E30-23, P6-45
D28-20, P6-43
D32-20, P6-45
E30-20, P6-45
D28-10, P6-43
D32-10, P6-45
E30-10, P6-45
D32-17, P6-45
D28-17, P6-43
ADDRESS PARITY
CH 0
CH 1
CH 2
CH 3
P6-9, A27-26 SCAN 0
P6-9, A32-27 SCAN 1
P6-9, A31-27 SCAN 2
EMC P6-43, B31-27
P6-9, A33-27 SCAN 3
E35-3, P6-15
E35-11, P6-15
NOTE
1 WIRING IS SHOWN FOR 524K ECS ONLY. FOR OTHER ECS SIZES, SEE DELETES AND ADDS WIRE LIST FOR THESE PINS IN SECTION 5.
2 THESE INPUTS ARE SHOWN ON PAGE 6-49.
CONTROL DATA
DEVELOPMENT DIVISION
ADDRESS PARITY CHECK 1 AND PARITY CHECK DISABLE
CODE IDENT 34010
DWG NO 60440500
REV
SHEET C
PAGE 6-13

The CX modules receive the address bits from the address register and pass on these bits in their true and inverted condition to the YU modules. The address parity bit in its true and inverted form is also an input to one of the YU modules.

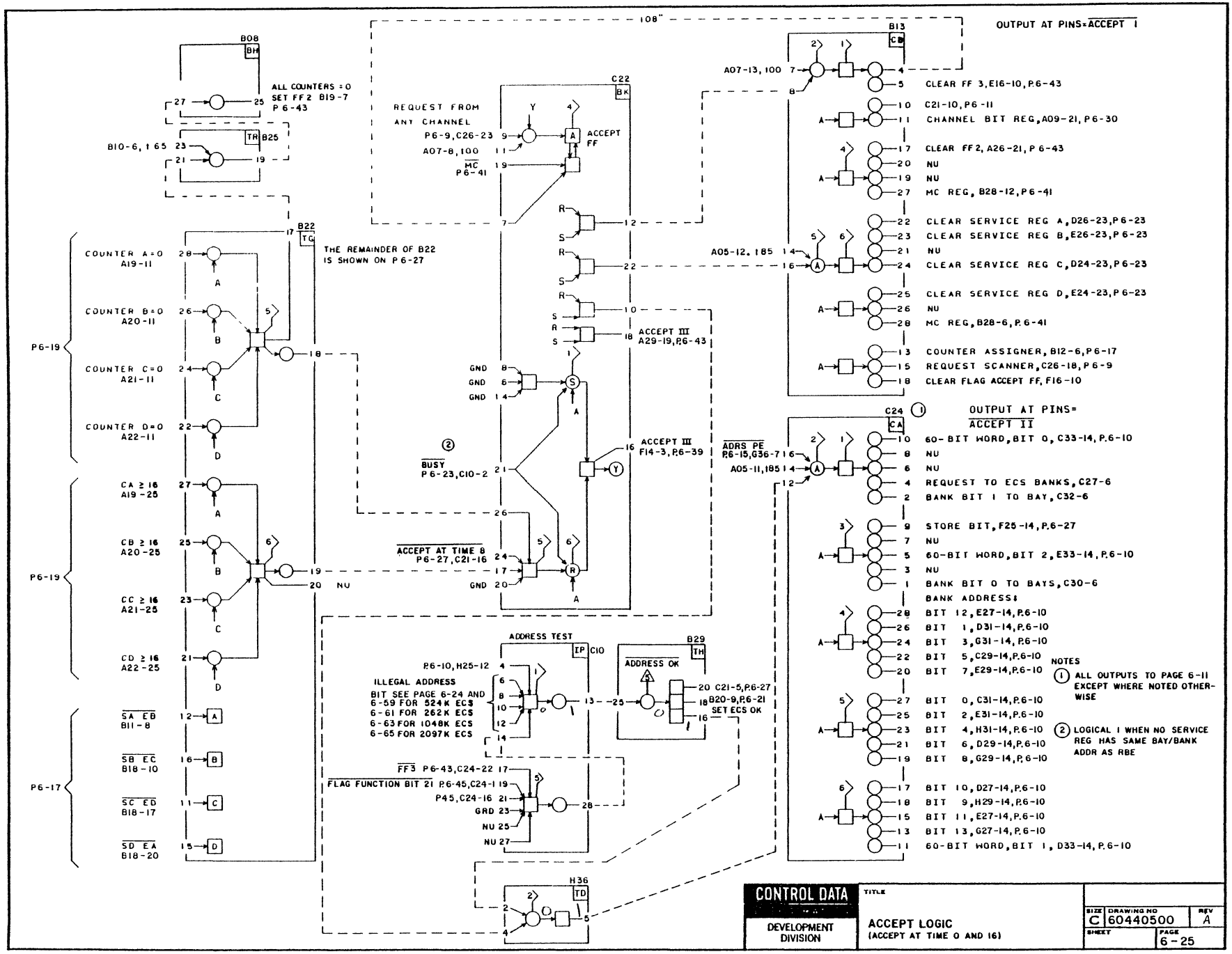
The address bits, address parity bit, and inverted states of the bits are passed through three ranks of YU modules. Parity checking for an odd number of 1 bits in the address, including the parity bit, is accomplished by exclusive OR gates in the YU modules. These gates reduce each set of three true and three inverted signals to one true and one inverted signal. The address is finally reduced until the YU module in the last rank receives only three true and three inverted signals. This enables the last rank to output an address parity error signal when the odd parity check by the network fails.

When an address parity error is detected, a 6640 parity error signal and an abort signal is sent to the channel. At the same time, an accept signal is disabled to prevent a channel request to ECS. An address parity error during a flag operation also enables a 6640 parity error signal along with a flag abort signal. The flag accept signal is disabled at this time but the flag register bits are not altered.

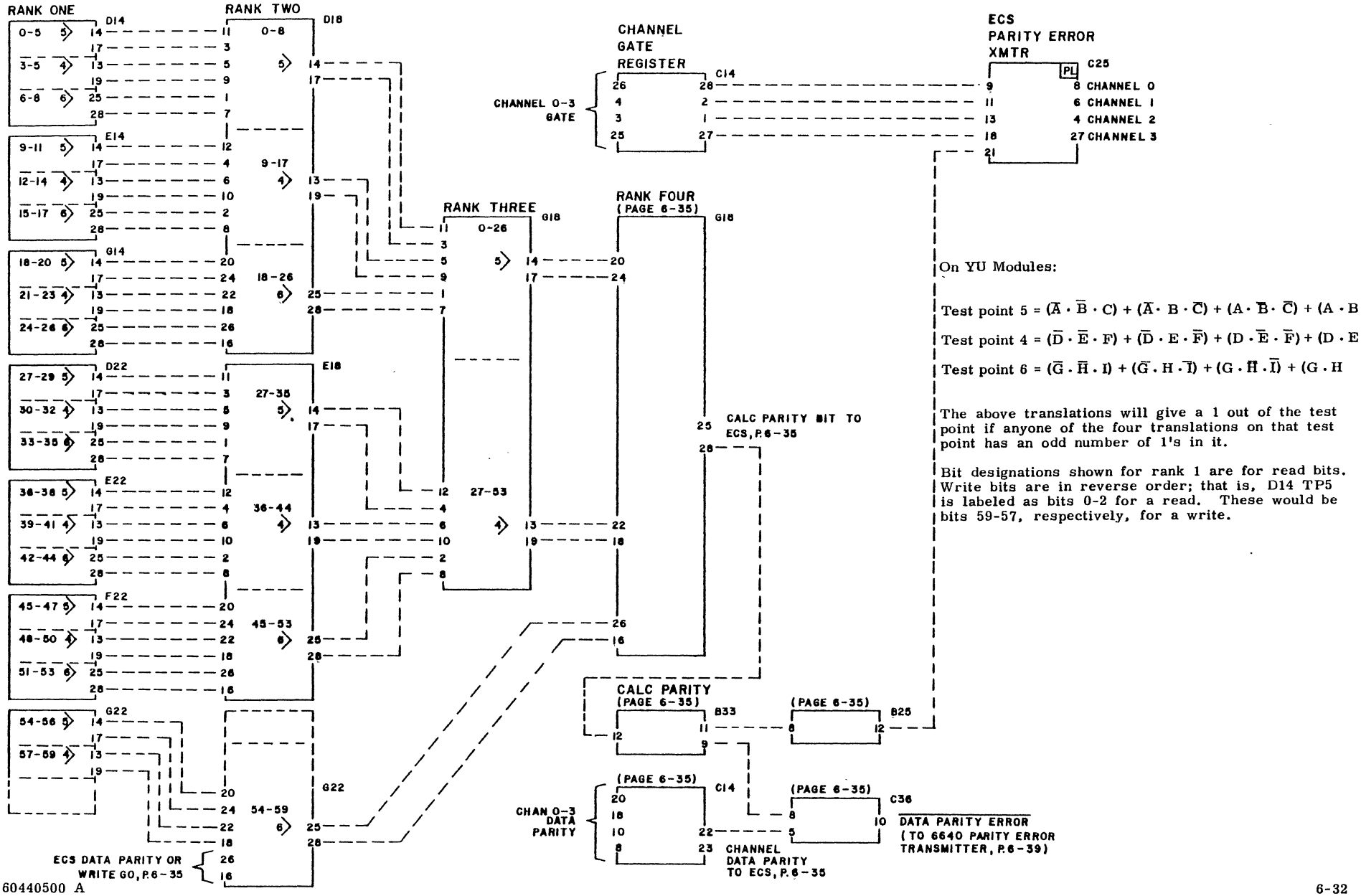

C34
CX
BANK ADRS BIT 5
P.6-10, C29-12
60-BIT WORD COUNT
BIT 0
P.6-10, C33-12
BIT 1
P.6-10, D33-12
BIT 2
P.6-10, E33-12
F34
CX
BANK ADRS BIT 10
P.6-10, D27-12
BANK ADRS BIT 7
P.6-10, E29-12
BANK ADRS BIT 6
P.6-10, D29-12
BANK ADRS BIT 0
P.6-10, C31-12
F34
CX
BANK ADRS BIT 8
P.6-10, G29-12
BANK ADRS BIT 3
P.6-10, G31-12
BANK ADRS BIT 12
P.6-10, F27-12
BANK ADRS BIT 11
P.6-10, E27-12
G34
CX
BANK ADRS BIT 2
P.6-10, E31-12
BANK ADRS BIT 9
P.6-10, H29-12
BANK ADRS BIT 4
P.6-10, H31-12
BANK ADRS BIT 13
P.6-10, G27-12
D34
CX
BANK ADRS BIT 1
P.6-10, D31-12
FLAG FCTN BIT 23
P.6-43, D28-12
FLAG FCTN BIT 22
P.6-45, D32-12
FLAG FCTN BIT 21
P.6-45, E30-12
ADRS PARITY BIT
P6-13, D35-18
ADRS PARITY BIT
P6-13, D35-12
E35
YU
F35
YU
G35
YU
F36
YU
G35
YU
P.6-13, G35-13
P6-13, G35-19
P.6-13, H34-15
P.6-13, H34-17
ADDRESS PARITY ERROR
RC G36
F18-14, P.6-37
F14-24, P.6-39
B20-11, P.6-21
G24-16, P.6-21
P.6-13
D36-5
P.6-13
D36-9
P.6-13
D36-11
P.6-13
D36-13
ADDRESS PARITY ERROR
TD H36
C35-5, P.6-39
C35-12, P.6-39
NU
NU
P.6-13, B35-13
CONTROL DATA
DEVELOPMENT DIVISION
ADDRESS PARITY CHECK 2
CODE IDENT 34010
DWG NO 60440500
REV L
SIZE C
SHEET
PAGE 6-15



CONTROL DATA	ABORT REGISTER AND TRANSMITTER	SIZE C	DRAWING NO 60440500	REV A
DEVELOPMENT DIVISION		SHEET	PAGE 6-21	


108"
B08 BH
ALL COUNTERS = 0
SET FF2 B19-7
P6-43
B10-6, I65
TR B25
B22 TG
THE REMAINDER OF B22
IS SHOWN ON P6-27
COUNTER A=0
A19-11
COUNTER B=0
A20-11
COUNTER C=0
A21-11
COUNTER D=0
A22-11
P6-19
CA ≥ 16
A19-25
CB ≥ 16
A20-25
CC ≥ 16
A21-25
CD ≥ 16
A22-25
P6-19
SA EB
B11-8
SB EC
B18-10
SC ED
B18-17
SD EA
B18-20
P6-17
C22 BK
REQUEST FROM
ANY CHANNEL
P6-9, C26-23
A07-8, 100
MC
P6-41
ACCEPT
FF
ACCEPT III
A29-19, P6-43
GND
BUSY
P6-23, C10-2
ACCEPT III
F14-3, P6-39
ACCEPT AT TIME 8
P6-27, C21-16
NU
ADDRESS TEST
IP C10
P6-10, H25-12
ILLEGAL ADDRESS
BIT SEE PAGE 6-24 AND
6-59 FOR 524K ECS
6-61 FOR 262K ECS
6-63 FOR 1048K ECS
6-65 FOR 2097K ECS
B29 TH
ADDRESS OK
C21-5, P6-27
B20-9, P6-21
SET ECS OK
FF3 P6-43, C24-22
FLAG FUNCTION BIT 21 P6-45, C24-1
P45, C24-16
GRD
NU
H36 TD
B13 CB
A07-13, 100
OUTPUT AT PINS=ACCEPT I
CLEAR FF 3, E16-10, P.6-43
C21-10, P6-11
CHANNEL BIT REG, A09-21, P6-30
CLEAR FF2, A26-21, P 6-43
NU
NU
MC REG, B28-12, P6-41
CLEAR SERVICE REG A, D26-23, P6-23
CLEAR SERVICE REG B, E26-23, P6-23
NU
CLEAR SERVICE REG C, D24-23, P6-23
A05-12, 185
CLEAR SERVICE REG D, E24-23, P6-23
NU
MC REG, B28-6, P.6-41
COUNTER ASSIGNER, B12-6, P6-17
REQUEST SCANNER, C26-18, P6-9
CLEAR FLAG ACCEPT FF, F16-10
C24 CA (1)
OUTPUT AT PINS=
ACCEPT II
ADRS PE
P6-15, G36-7
A05-11, 185
60-BIT WORD, BIT 0, C33-14, P.6-10
NU
NU
REQUEST TO ECS BANKS, C27-6
BANK BIT 1 TO BAY, C32-6
STORE BIT, F25-14, P.6-27
NU
60-BIT WORD, BIT 2, E33-14, P.6-10
NU
BANK BIT 0 TO BAYS, C30-6
BANK ADDRESS:
BIT 12, E27-14, P.6-10
BIT 1, D31-14, P.6-10
BIT 3, G31-14, P.6-10
BIT 5, C29-14, P.6-10
BIT 7, E29-14, P.6-10
BIT 0, C31-14, P.6-10
BIT 2, E31-14, P.6-10
BIT 4, H31-14, P.6-10
BIT 6, D29-14, P.6-10
BIT 8, G29-14, P.6-10
BIT 10, D27-14, P.6-10
BIT 9, H29-14, P.6-10
BIT 11, E27-14, P.6-10
BIT 13, G27-14, P.6-10
60-BIT WORD, BIT 1, D33-14, P.6-10
NOTES
(1) ALL OUTPUTS TO PAGE 6-11 EXCEPT WHERE NOTED OTHERWISE
(2) LOGICAL 1 WHEN NO SERVICE REG HAS SAME BAY/BANK ADDR AS RBE
CONTROL DATA
DEVELOPMENT DIVISION
TITLE
ACCEPT LOGIC
(ACCEPT AT TIME 0 AND 16)
SIZE C
DRAWING NO 60440500
REV A
SHEET
PAGE 6-25

ECS DATA PARITY ERROR TRANSMISSION



On YU Modules:

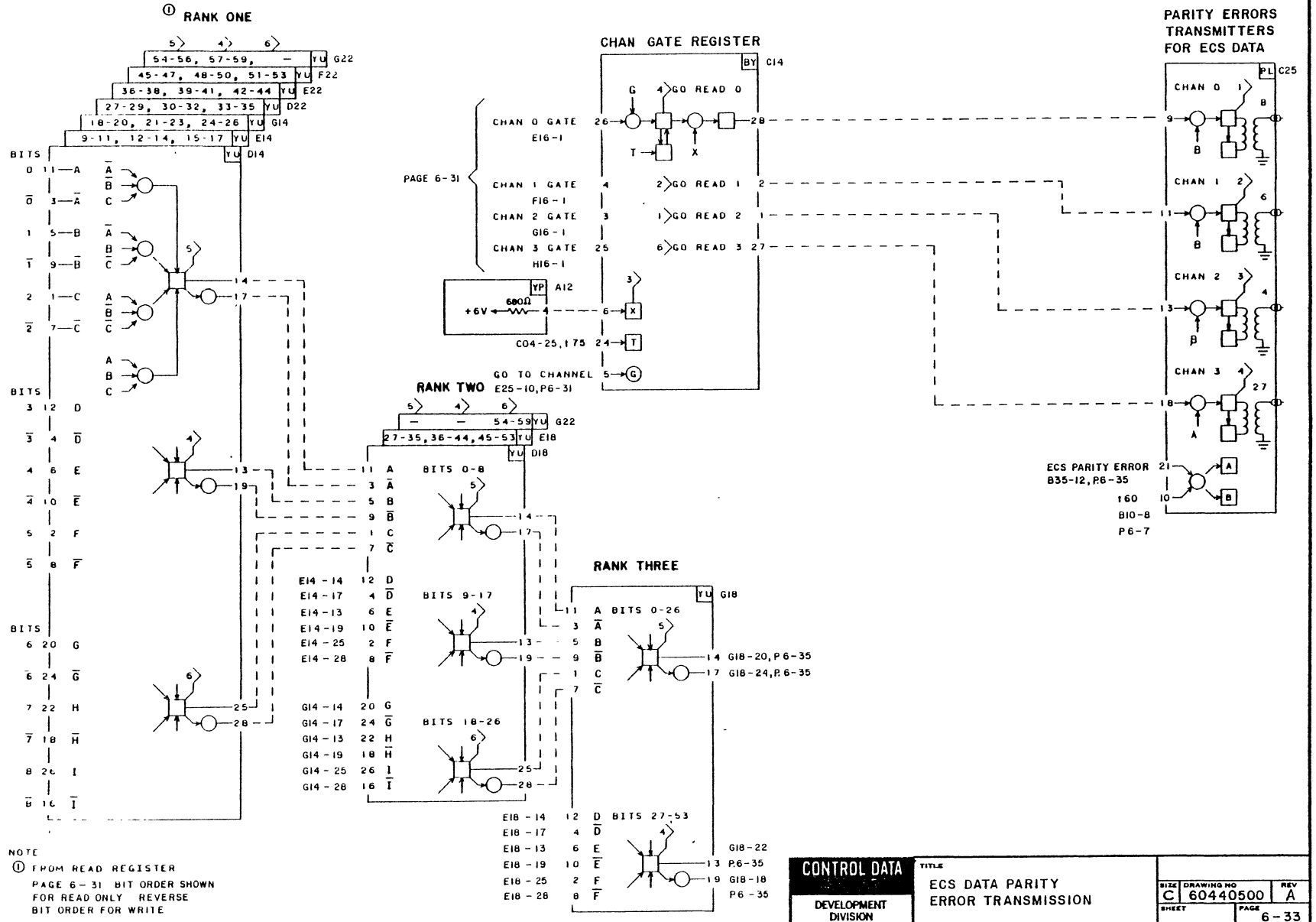
Test point 5 = $(\bar{A} \cdot \bar{B} \cdot C) + (\bar{A} \cdot B \cdot \bar{C}) + (A \cdot \bar{B} \cdot \bar{C}) + (A \cdot B \cdot C)$

Test point 4 = $(\bar{D} \cdot \bar{E} \cdot F) + (\bar{D} \cdot E \cdot \bar{F}) + (D \cdot \bar{E} \cdot \bar{F}) + (D \cdot E \cdot F)$

Test point 6 = $(\bar{G} \cdot \bar{H} \cdot I) + (\bar{G} \cdot H \cdot \bar{I}) + (G \cdot \bar{H} \cdot \bar{I}) + (G \cdot H$

The above translations will give a 1 out of the test point if anyone of the four translations on that test point has an odd number of 1's in it.

Bit designations shown for rank 1 are for read bits. Write bits are in reverse order; that is, D14 TP5 is labeled as bits 0-2 for a read. These would be bits 59-57, respectively, for a write.



NOTE
① FROM READ REGISTER PAGE 6-31 BIT ORDER SHOWN FOR READ ONLY REVERSE BIT ORDER FOR WRITE

CONTROL DATA
DEVELOPMENT DIVISION

TITLE
ECS DATA PARITY ERROR TRANSMISSION

SIZE	DRAWING NO	REV
C	60440500	A
SHEET		PAGE 6-33

GENERAL

The controller does an odd parity check on data from the channel to ECS during a write operation and also on data from ECS to the channel during a read operation.

The parity check disable (PCD) inputs to the TR module at F18 are from controller switches. There is a switch for each channel. With the switch in the normal or enable position, the data parity bit from the channel is checked by the controller and then passed on with the data to ECS. With the switch in the disable position, the data parity bit generated in the controller is sent to ECS instead of the channel parity bit. Other inputs to the TR module are from the service registers. The service register for the selected channel provides an 800-nanosecond window for gating the parity bit to ECS.

WRITE OPERATION DATA PARITY

During a write operation, data bits from the channel are passed through the four ranks of YU modules. In the rank 4 module at G18, a write go bit is added to each 60-bit data word. The write go bit enables parity checking of partial records (less than eight 60-bit words). The calculated parity bit from the TQ module at B33 is a 1 if an odd number of bits pass through the parity network. The calculated parity bit for the 60-bit word is then compared with the channel parity bit for the same word by an exclusive NOR gate in the AB module at C36. A 0 output from the AB module indicates a data parity error. A 6640 data parity error signal is then transmitted to the channel.

The channel data parity bit is also passed on with the data and stored in ECS regardless if a data parity error occurred or not. This feature enables data with bad parity to be stored in ECS. If the parity checking network detects this bad parity when the data is read back from ECS, the network is functioning properly.

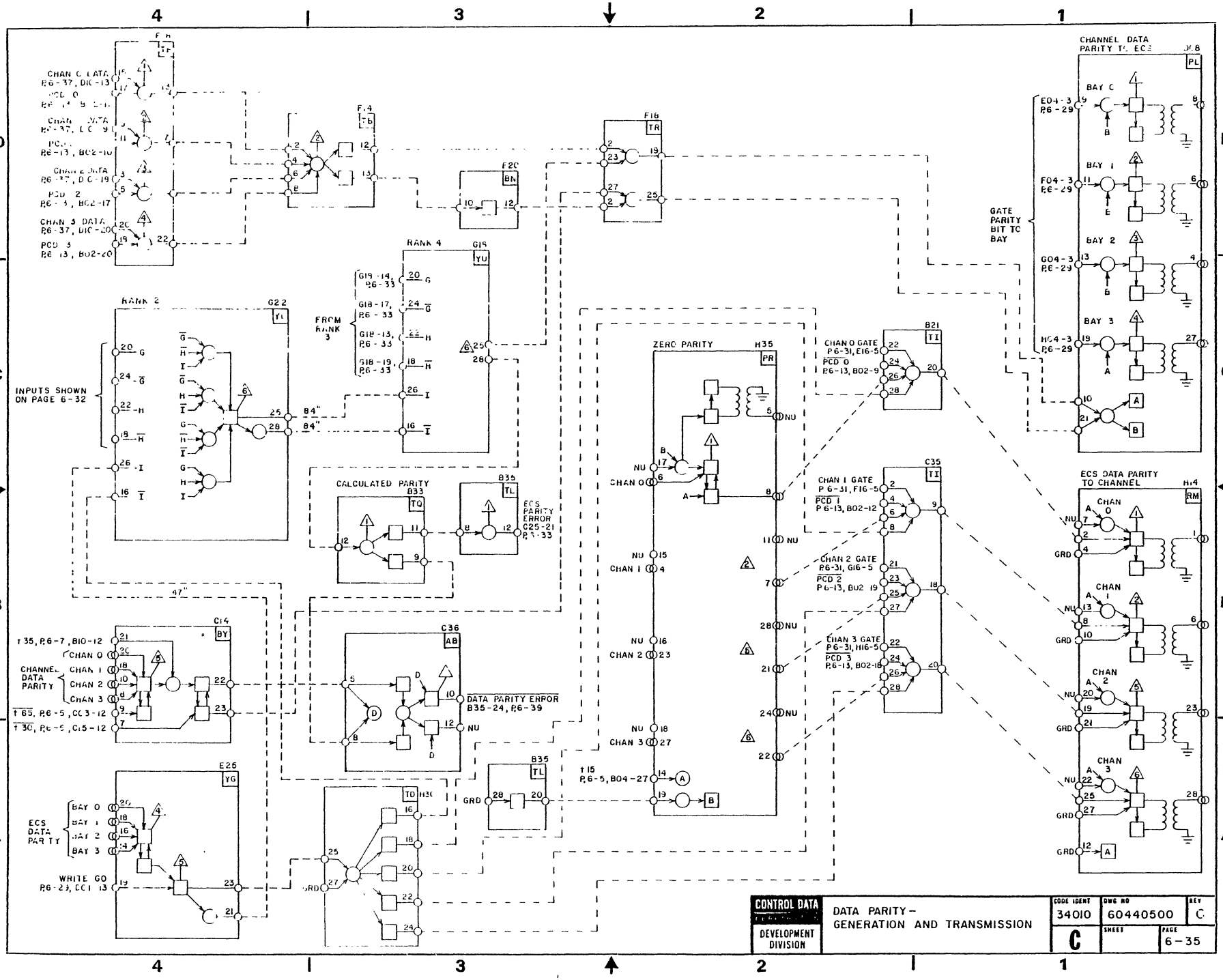
READ OPERATION DATA PARITY

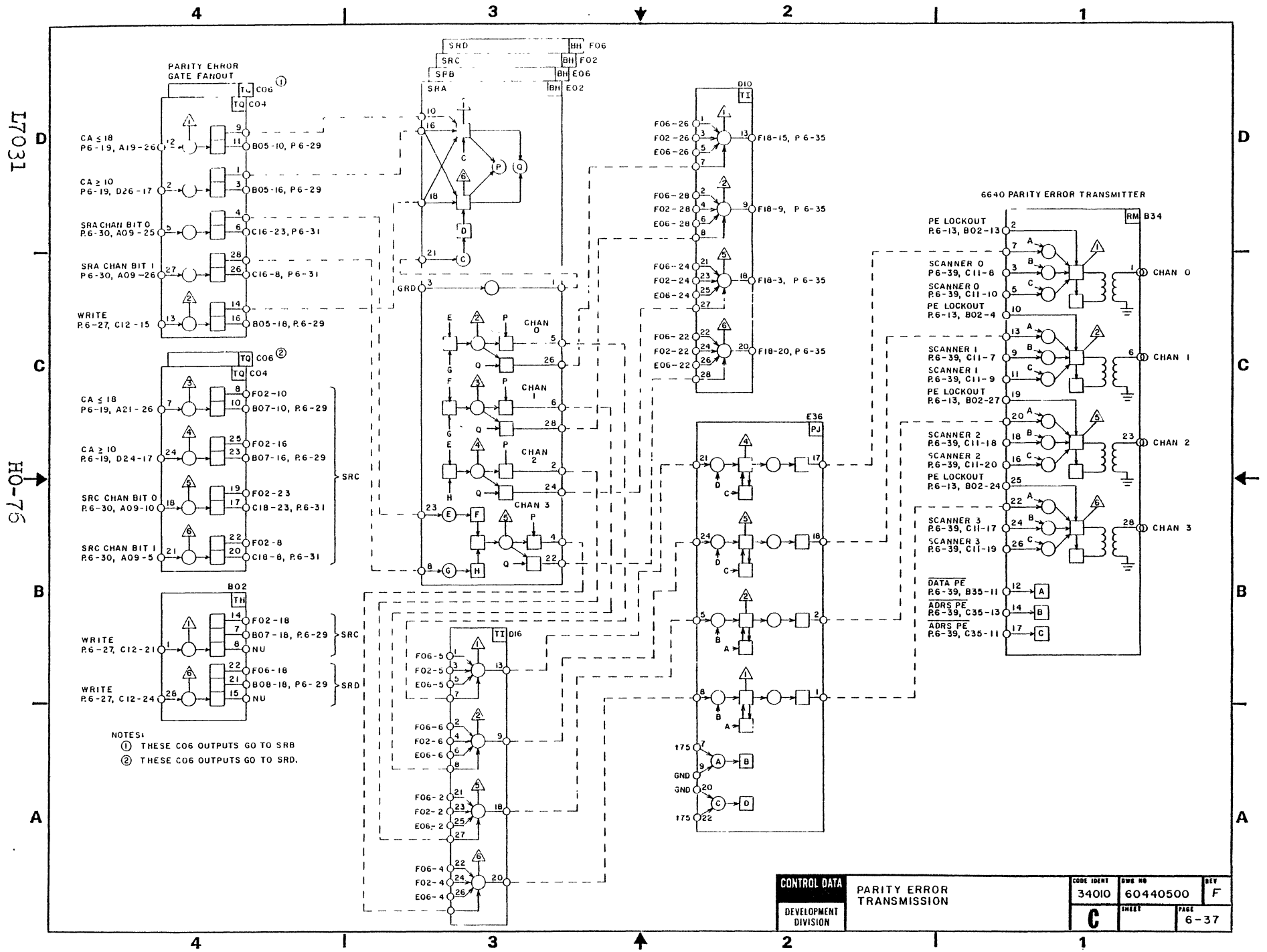
During a read operation, each 60-bit data word from ECS is passed through the four ranks of YU modules. In the rank 4 module at G18, the accompaning ECS data parity bit is added to the 60-bit data word. If an odd number of bits, including the ECS data parity bit, pass through the network, the TL module at B35 outputs a 0. If an even number of bits are detected, the TL module outputs a 1 to indicate an ECS parity error. An ECS parity error signal is then transmitted to the channel approximately 85 nanoseconds after parity error detection.

The ECS data parity bit is also passed on to the RM module at H14 and transmitted to the channel regardless if a data parity error occurred or not. When the channel receives both a data parity error signal and an incorrect parity bit, it indicates an error in ECS storage. If the channel receives incorrect parity but not a parity error, it indicates an error in transmission.

ZERO PARITY

During a read operation, a coupler may send 25-nanosecond pulses every 100 nanoseconds over the channel to coincide with the request signal. These zero parity pulses lock out the ECS data parity bits so that only 60-bit words from ECS are transmitted to the coupler. This enables the coupler to check its own parity checking circuits.

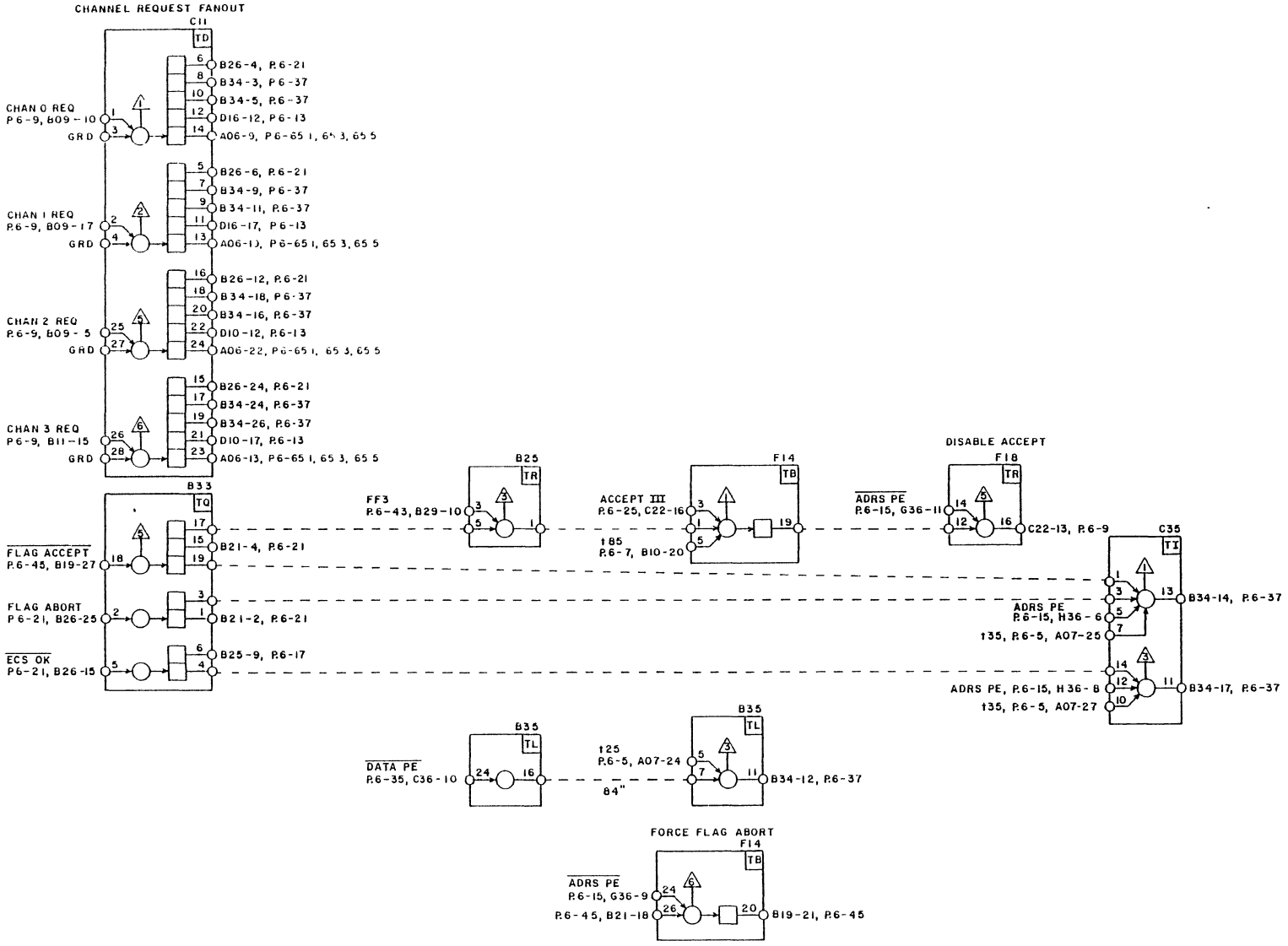

L7031
H0-75
CHAN 0 DATA
CHAN 1 DATA
PCD 1
CHAN 2 DATA
PCD 2
CHAN 3 DATA
PCD 3
INPUTS SHOWN ON PAGE 6-32
RANK 2
RANK 4
FROM RANK 3
CALCULATED PARITY
ECS PARITY ERROR
ZERO PARITY
CHAN 0
CHAN 1
CHAN 2
CHAN 3
CHAN 0 GATE
CHAN 1 GATE
CHAN 2 GATE
CHAN 3 GATE
GATE PARITY BIT TO BAY
CHANNEL DATA PARITY TO ECS
BAY 0
BAY 1
BAY 2
BAY 3
ECS DATA PARITY TO CHANNEL
CHANNEL DATA PARITY
ECS DATA PARITY
WRITE GO
DATA PARITY ERROR B35-24, R6-39
CONTROL DATA
DEVELOPMENT DIVISION
DATA PARITY - GENERATION AND TRANSMISSION
CODE IDENT 34010
DWG NO 60440500
REV C
SIZE C
SHEET
PAGE 6-35



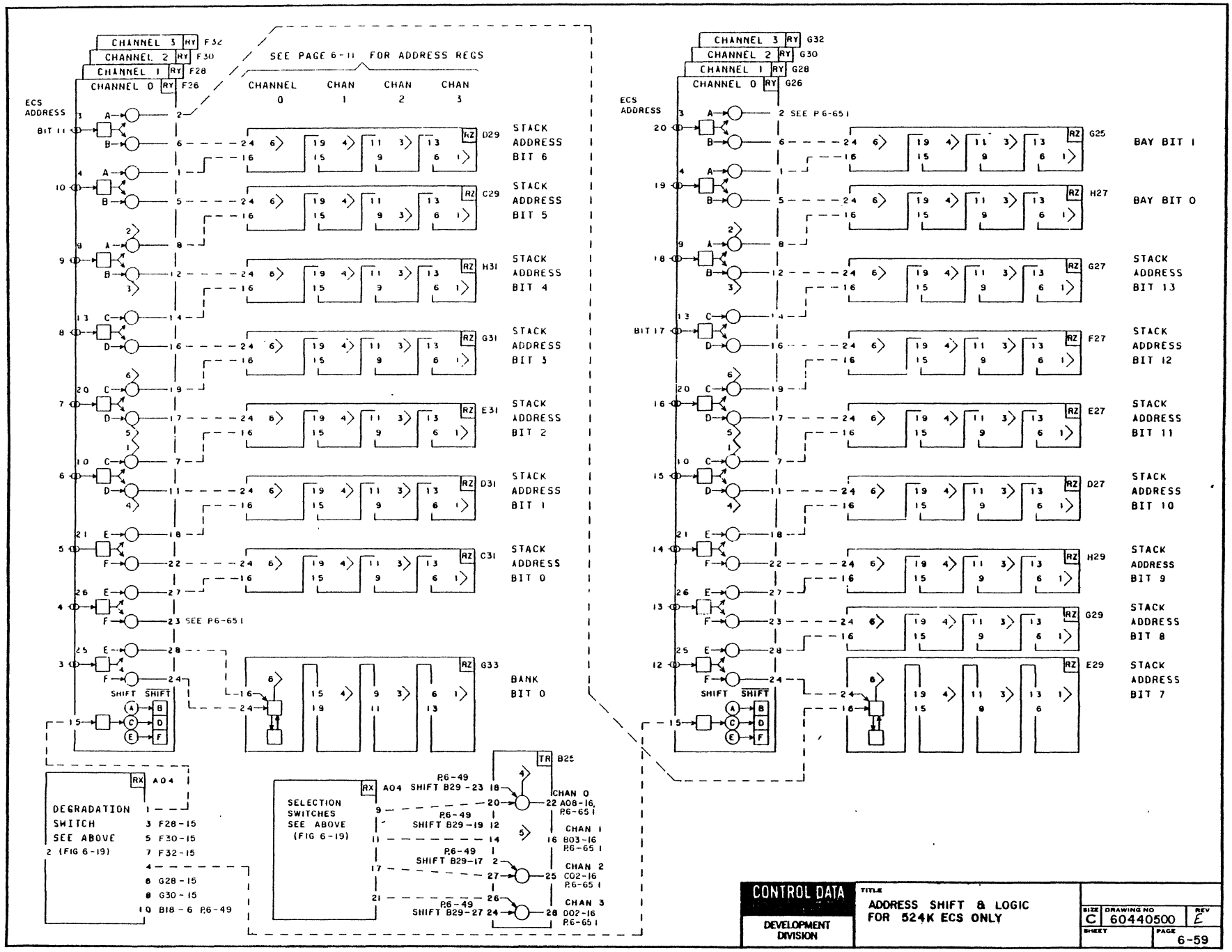
CONTROL DATA	PARITY ERROR TRANSMISSION	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		34010	60440500	F
		C	SHEET	PAGE 6-37

L7031

HO-75



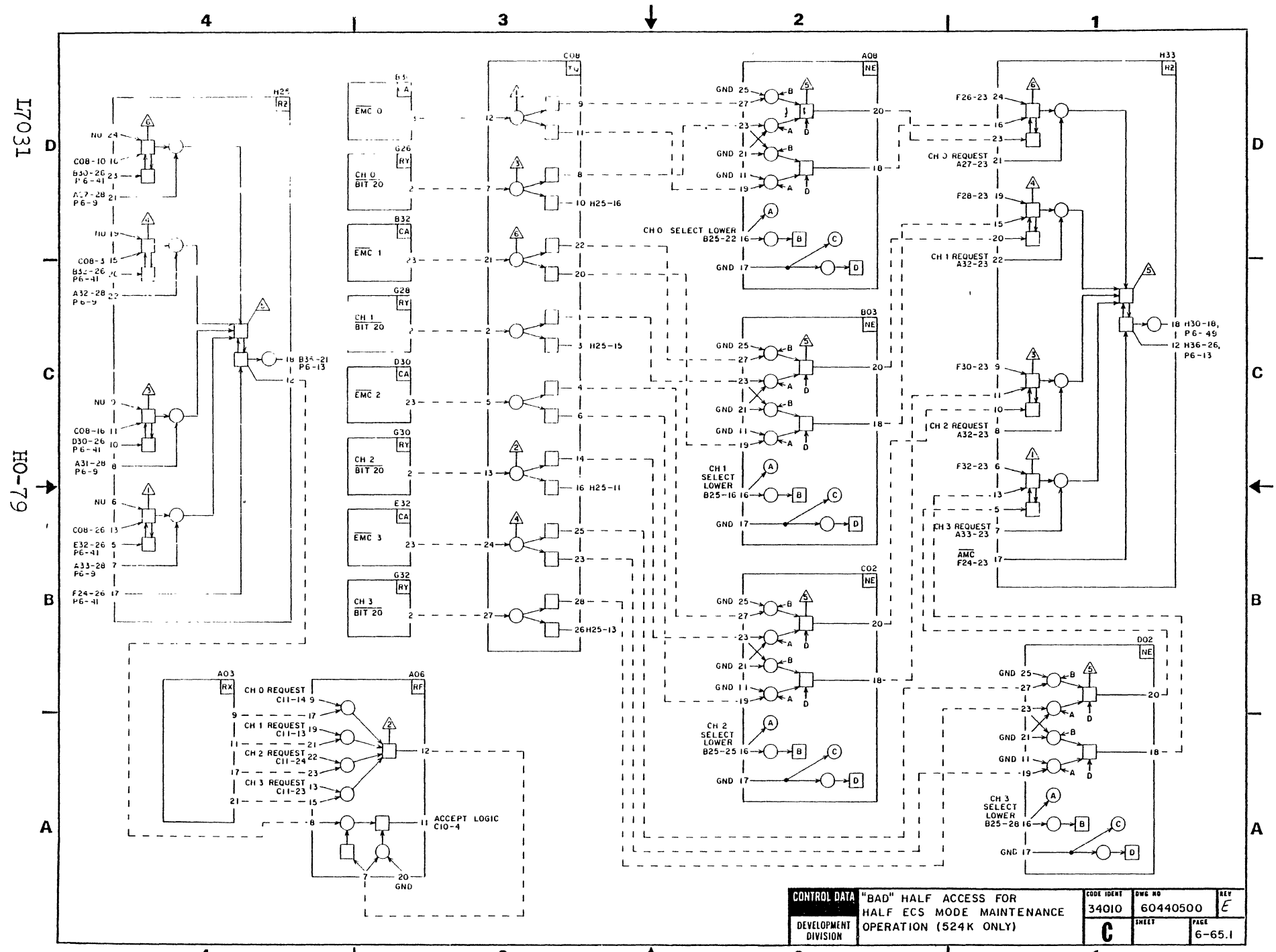
CONTROL DATA DEVELOPMENT DIVISION	MISCELLANEOUS PARITY ERROR CIRCUITS	CODE IDENT 34010 C	DWG NO 60440500 SHEET PAGE 6-39 REV L



CONTROL DATA
DEVELOPMENT DIVISION

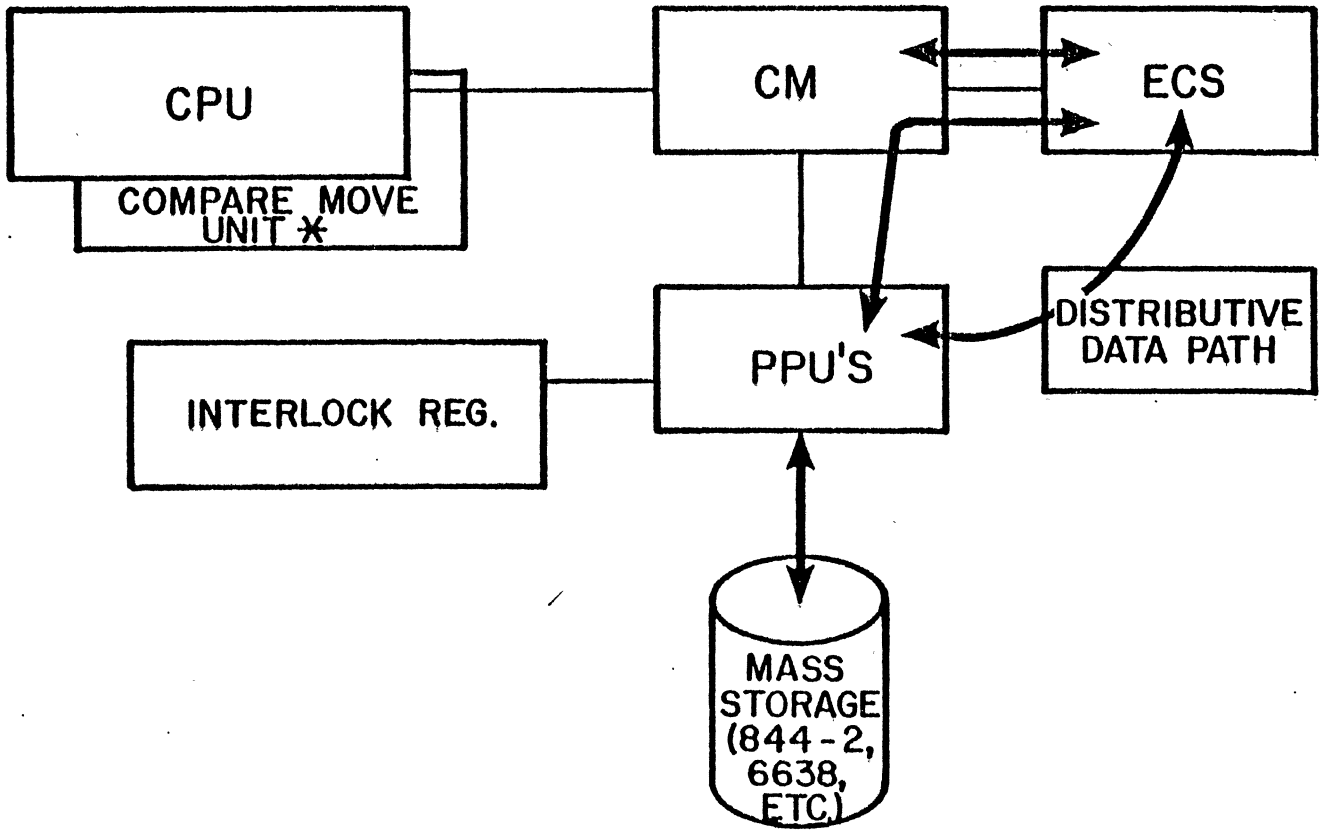
TITLE
ADDRESS SHIFT & LOGIC FOR 524K ECS ONLY

SIZE	DRAWING NO	REV
C	60440500	E
SHEET	PAGE	
	6-59	

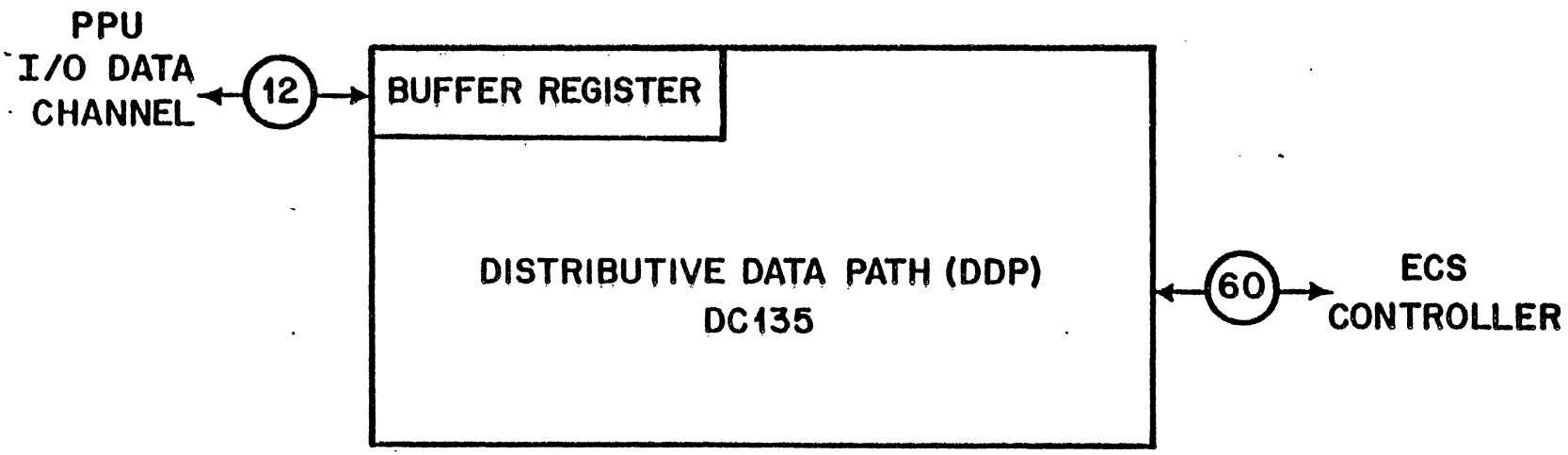

I7031
HO-79
4
3
2
1
A
B
C
D
CH 0 REQUEST C11-14
CH 1 REQUEST C11-13
CH 2 REQUEST C11-24
CH 3 REQUEST C11-23
ACCEPT LOGIC C10-4
CH 0 SELECT LOWER B25-22
CH 1 SELECT LOWER B25-16
CH 2 SELECT LOWER B25-25
CH 3 SELECT LOWER B25-28
CH 0 REQUEST A27-23
CH 1 REQUEST A32-23
CH 2 REQUEST A32-23
CH 3 REQUEST A33-23
AMC F24-23
EMC 0
EMC 1
EMC 2
EMC 3
CH 0 BIT 20
CH 1 BIT 20
CH 2 BIT 20
CH 3 BIT 20
GND
CONTROL DATA
DEVELOPMENT DIVISION
"BAD" HALF ACCESS FOR HALF ECS MODE MAINTENANCE OPERATION (524K ONLY)
CODE IDENT 34010
C
DWG NO 60440500
REV E
SHEET
PAGE 6-65.1

CYBER 70

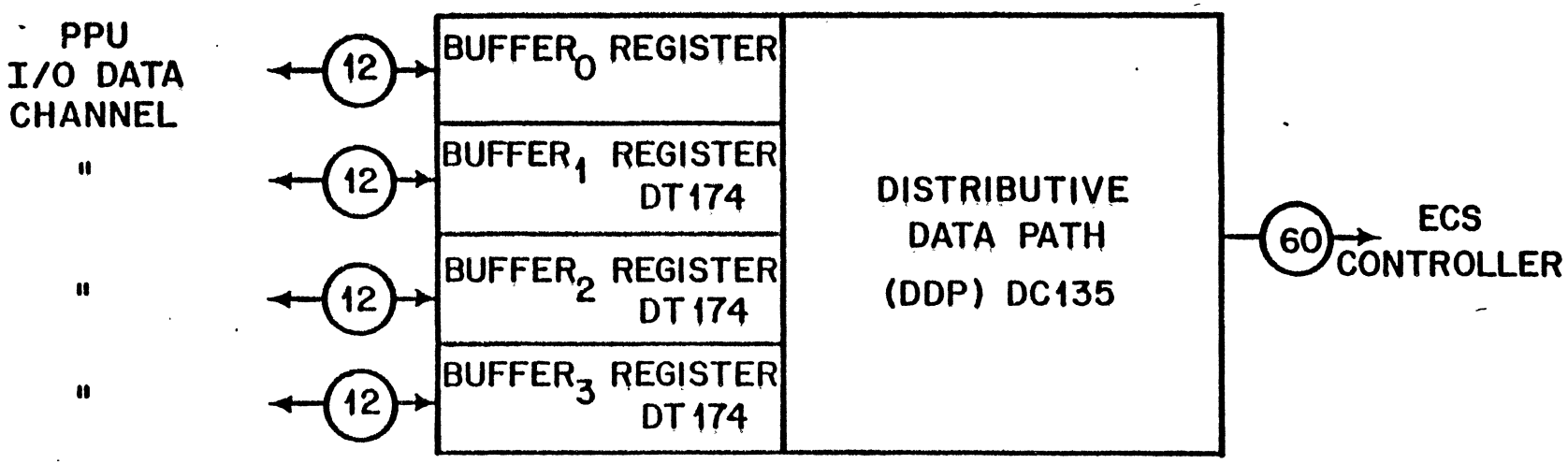
MODEL 72, 73, 74



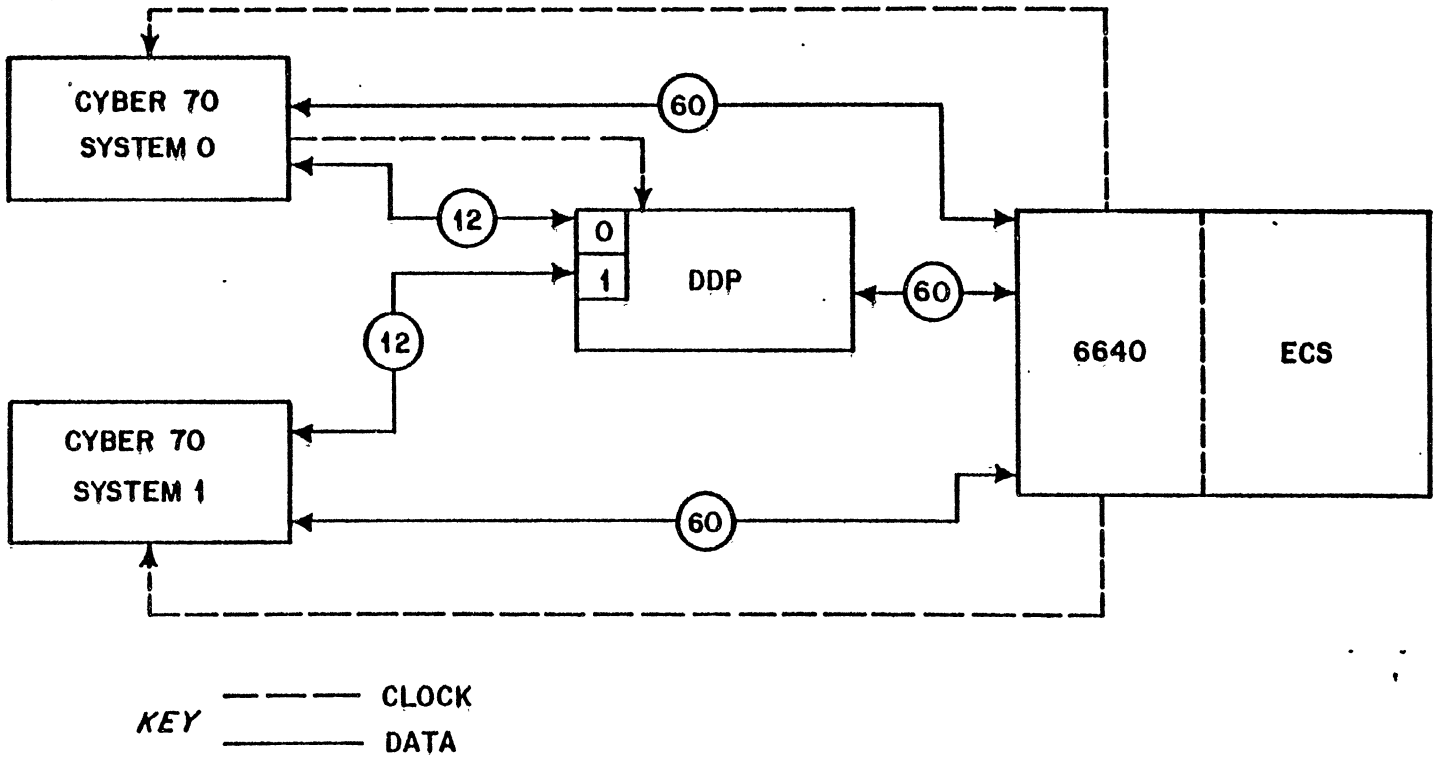
BASIC DISTRIBUTIVE DATA PATH (DDP)



DISTRIBUTIVE DATA PATH WITH OPTIONS

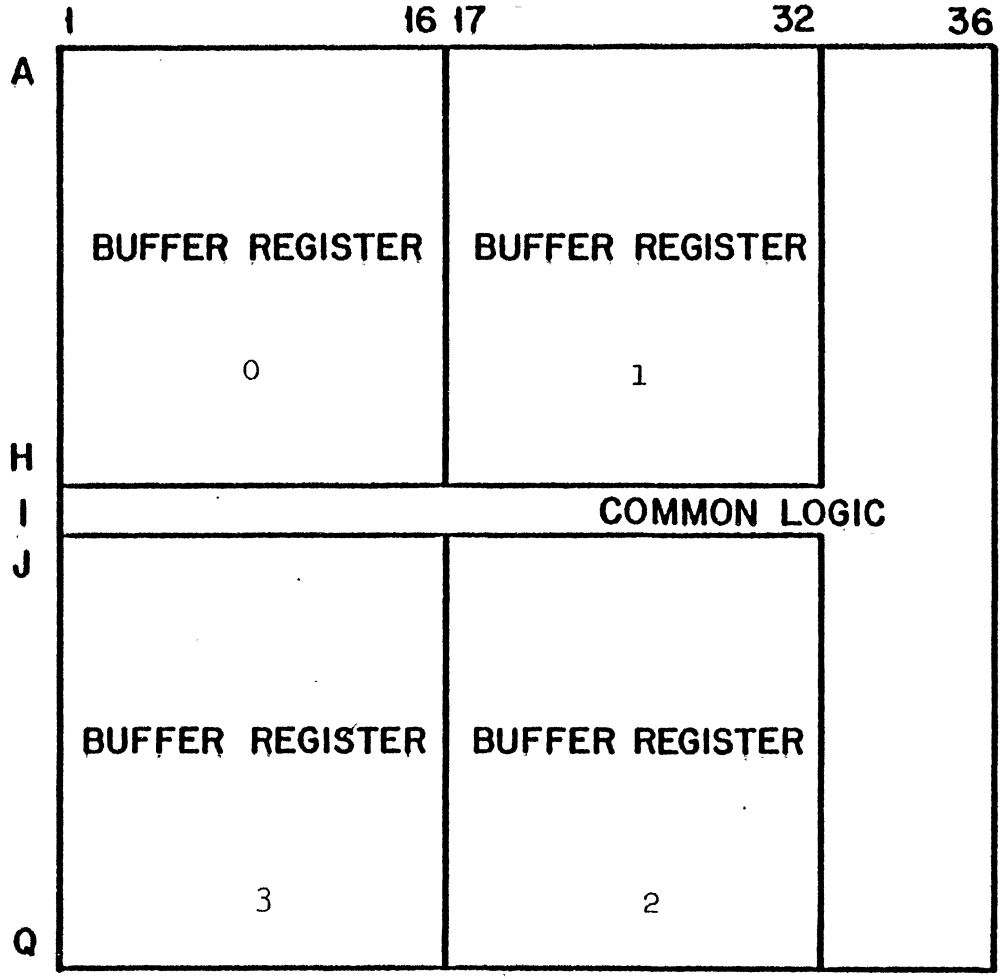


CLOCK DISTRIBUTION



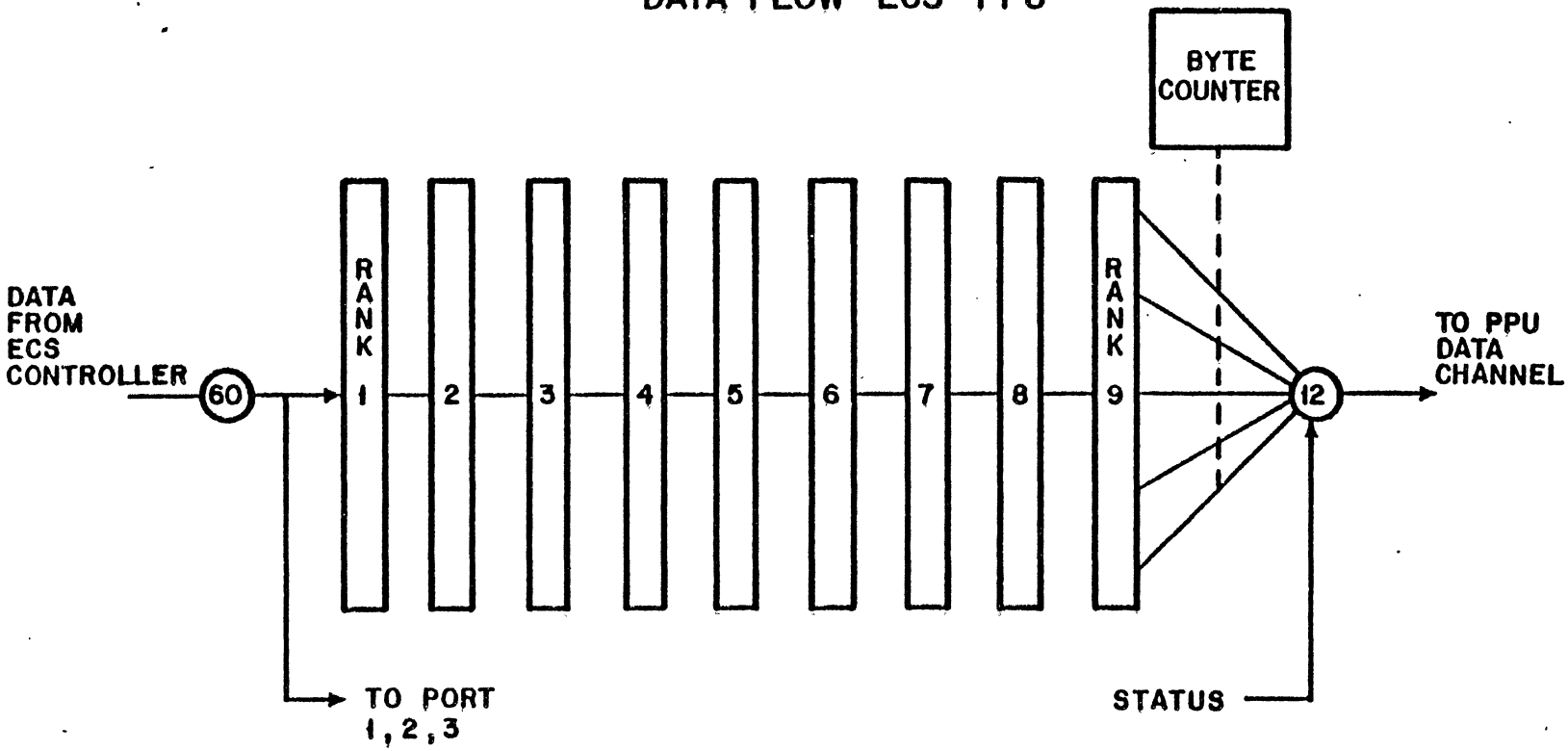
DISTRIBUTIVE DATA PATH (DDP)

CARD PLACEMENT



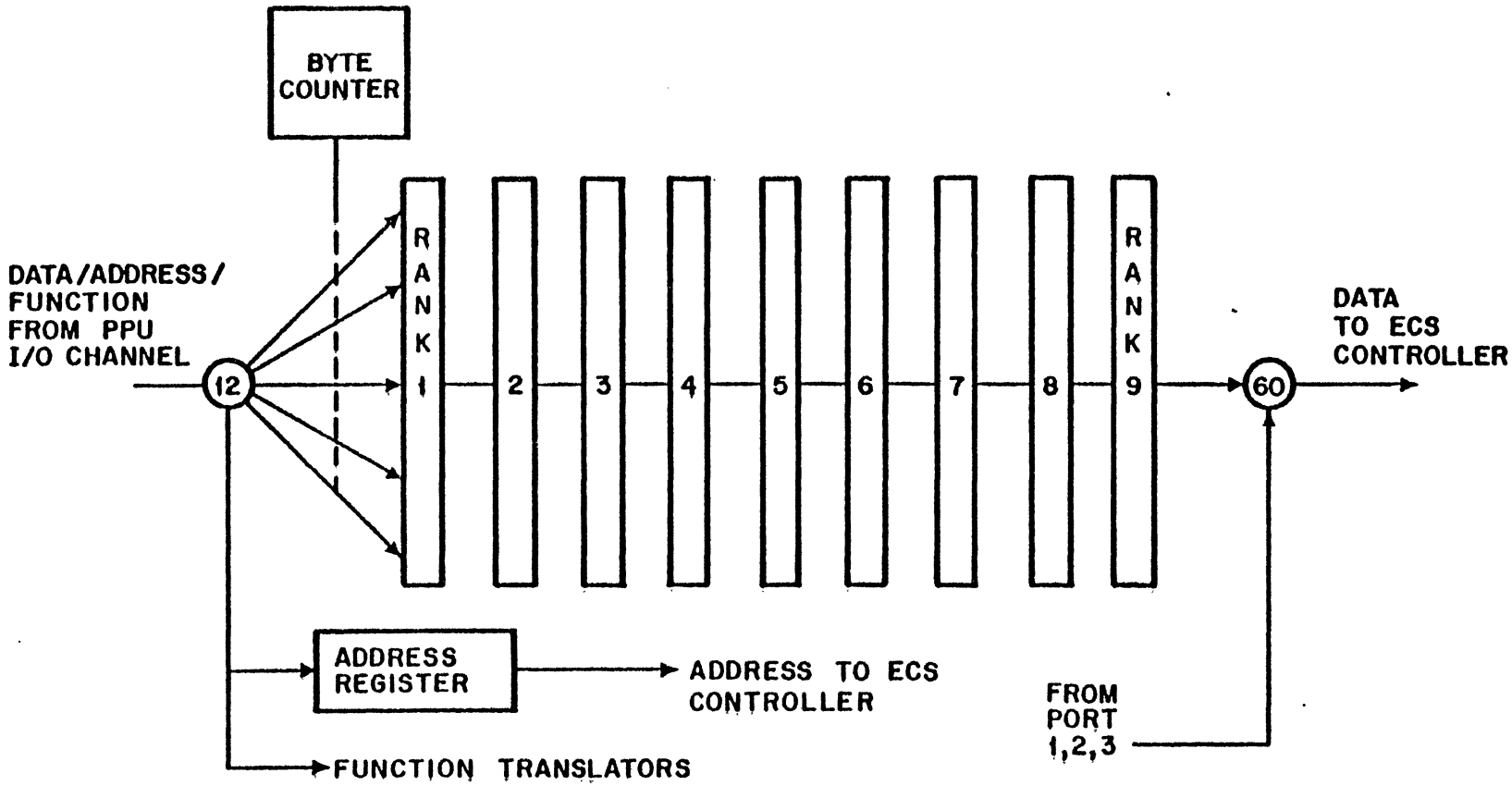
DISTRIBUTIVE DATA PATH (DDP)

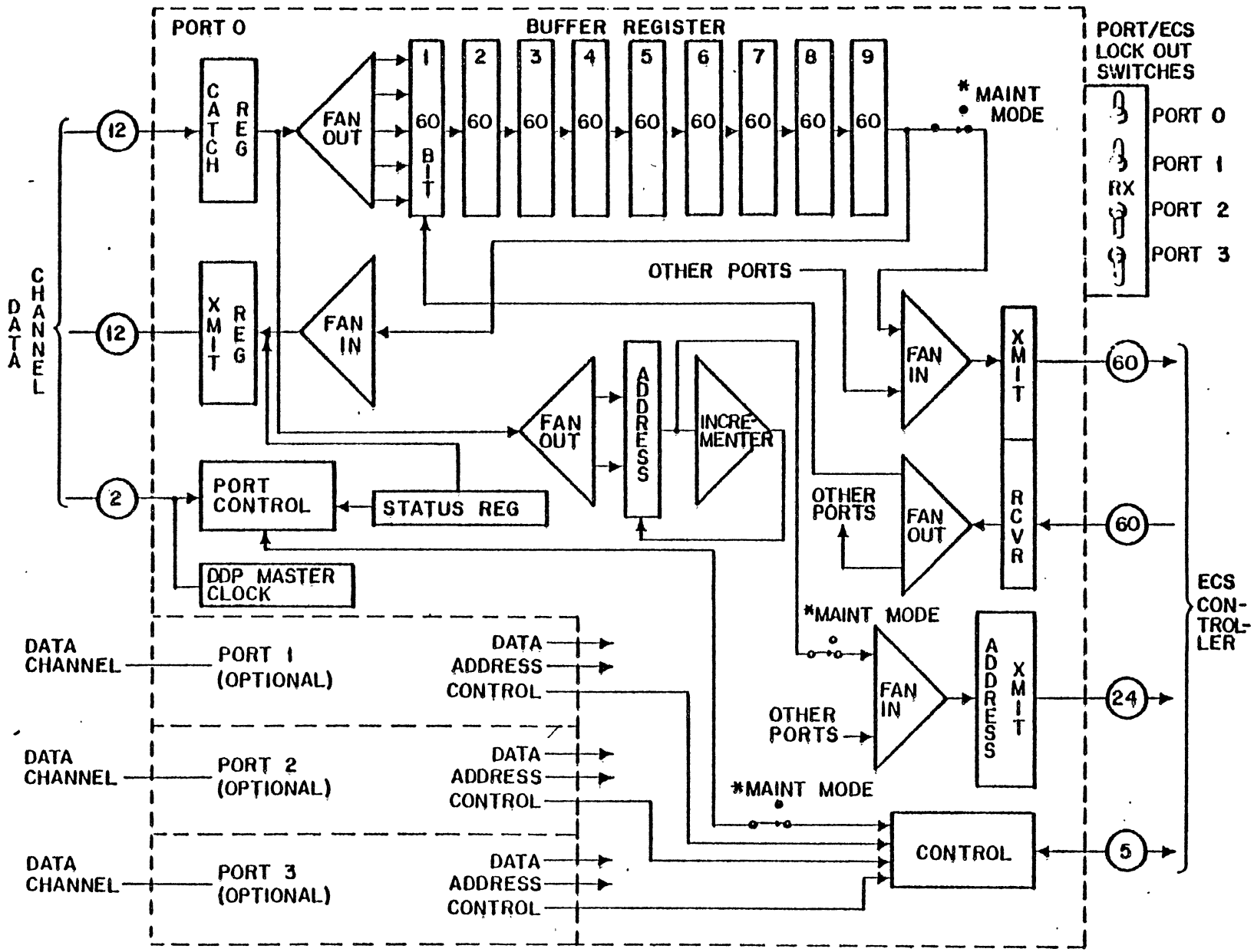
DATA FLOW ECS-PPU



DISTRIBUTIVE DATA PATH (DDP)

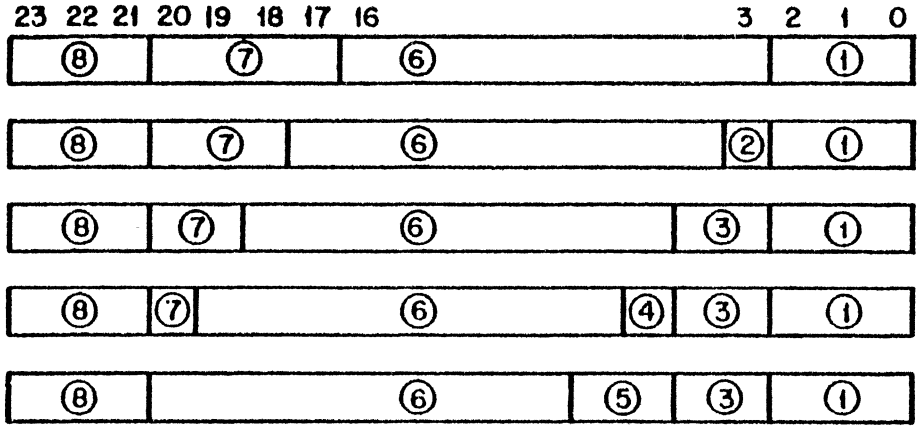
DATA FLOW PPU-ECS





DDP BLOCK DIAGRAM

ADDRESS FORMATS



125 K	1 BANK
250 K	2 BANK
500 K	4 BANK (1 BAY)
1000 K	8 BANK (2 BAYS)
2000 K	16 BANK (4 BAYS)

① 60 BIT WORD COUNT BITS

② SELECT 1 OF 2 BANKS

③ SELECT 1 OF 4 BANKS

④ SELECT 1 OF 2 BAYS

⑤ SELECT 1 OF 4 BAYS

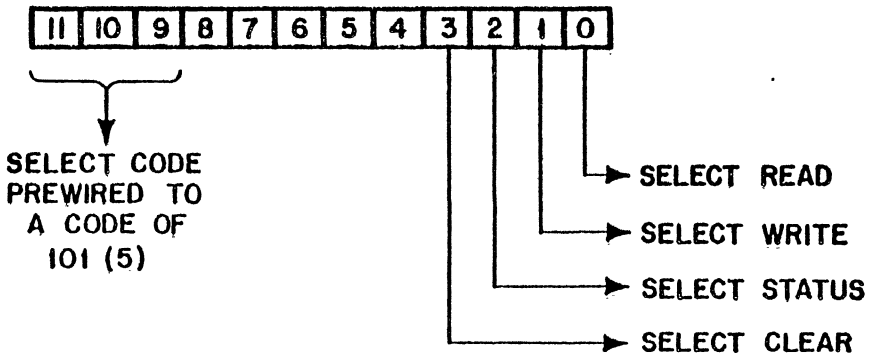
⑥ SELECT 1 488-BIT WORD IN A BANK

⑦ NOT USED

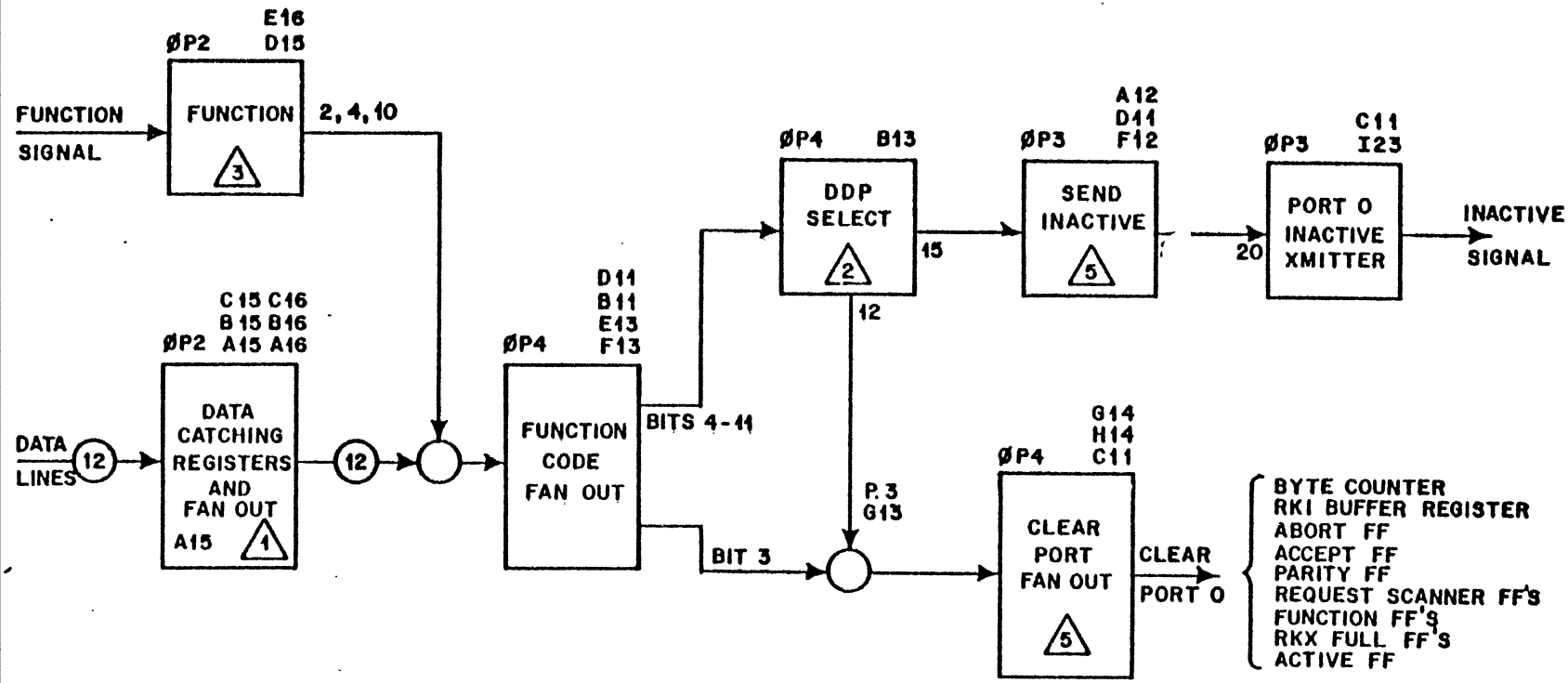
⑧

0 0 0	DATA TRANSFER MODE
0 0 1	MAINTENANCE MODE
0 1 0	READ ONE MODE
0 1 1	ILLEGAL
1 0 0	FLAG FUNCTION READY/SELECT
1 0 1	FLAG FUNCTION SELECTIVE SET
1 1 0	FLAG FUNCTION STATUS
1 1 1	FLAG FUNCTION SELECTIVE CLEAR

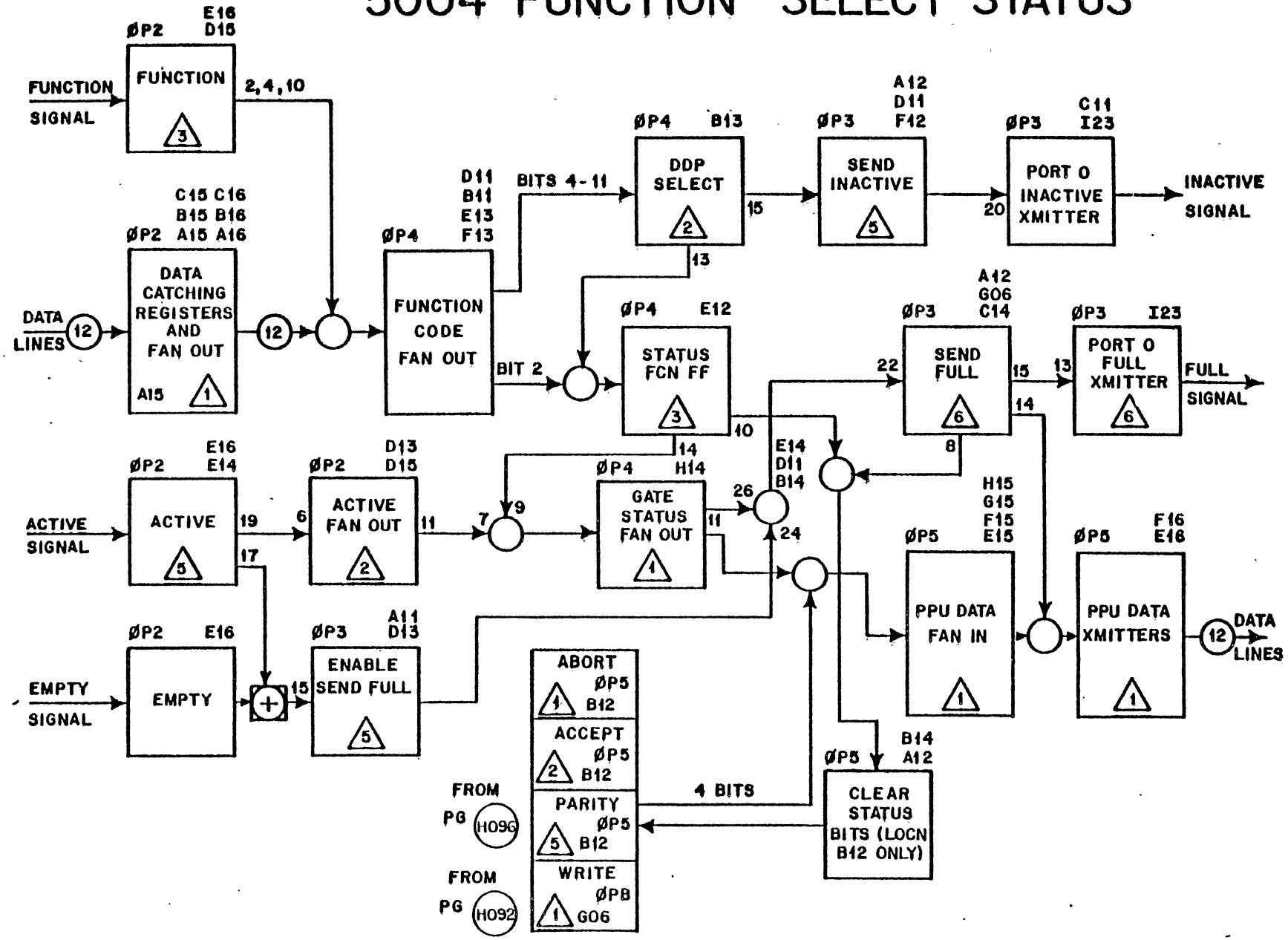
FUNCTION SELECTION



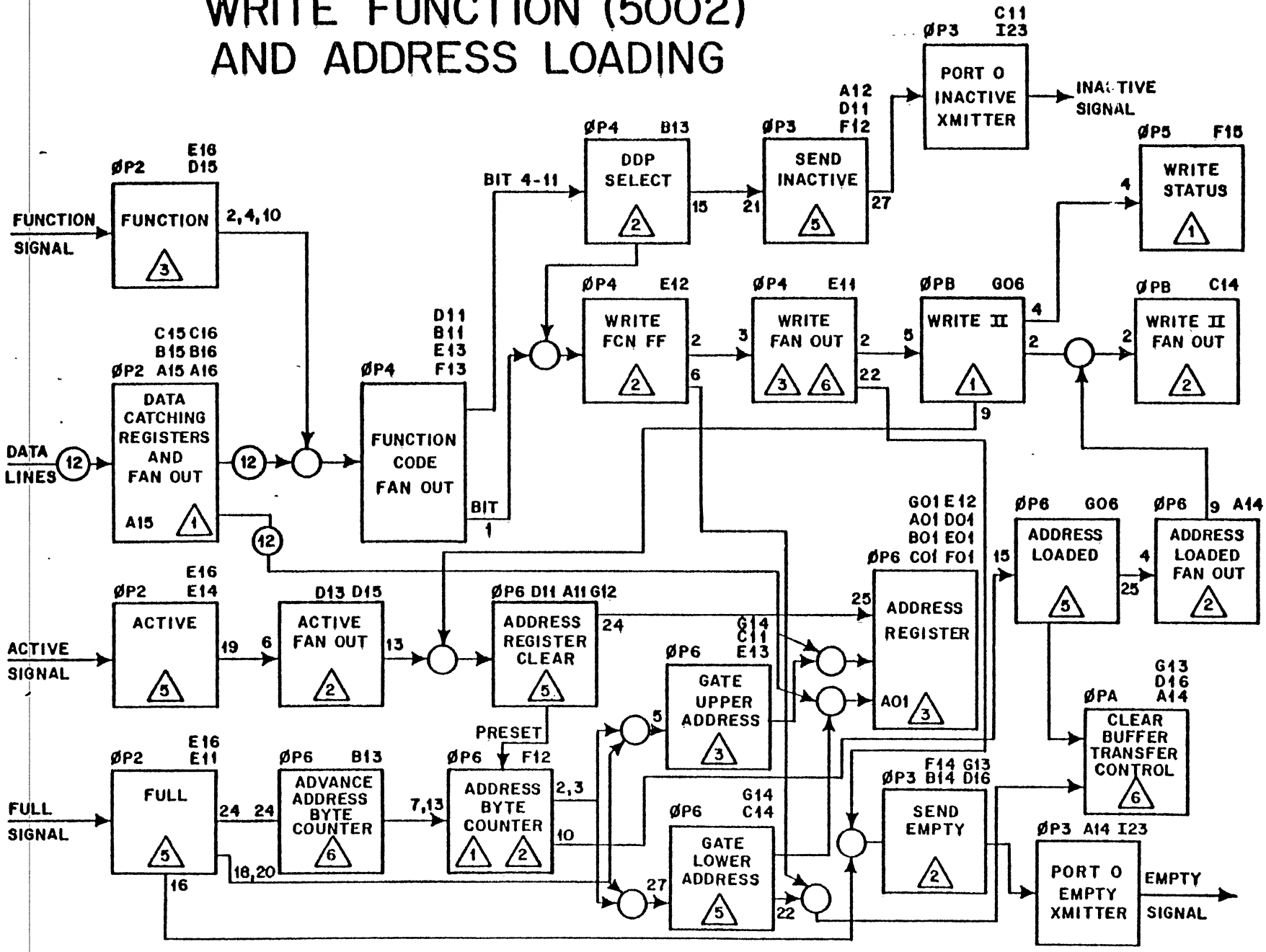
5010 FUNCTION
CLEAR PORT



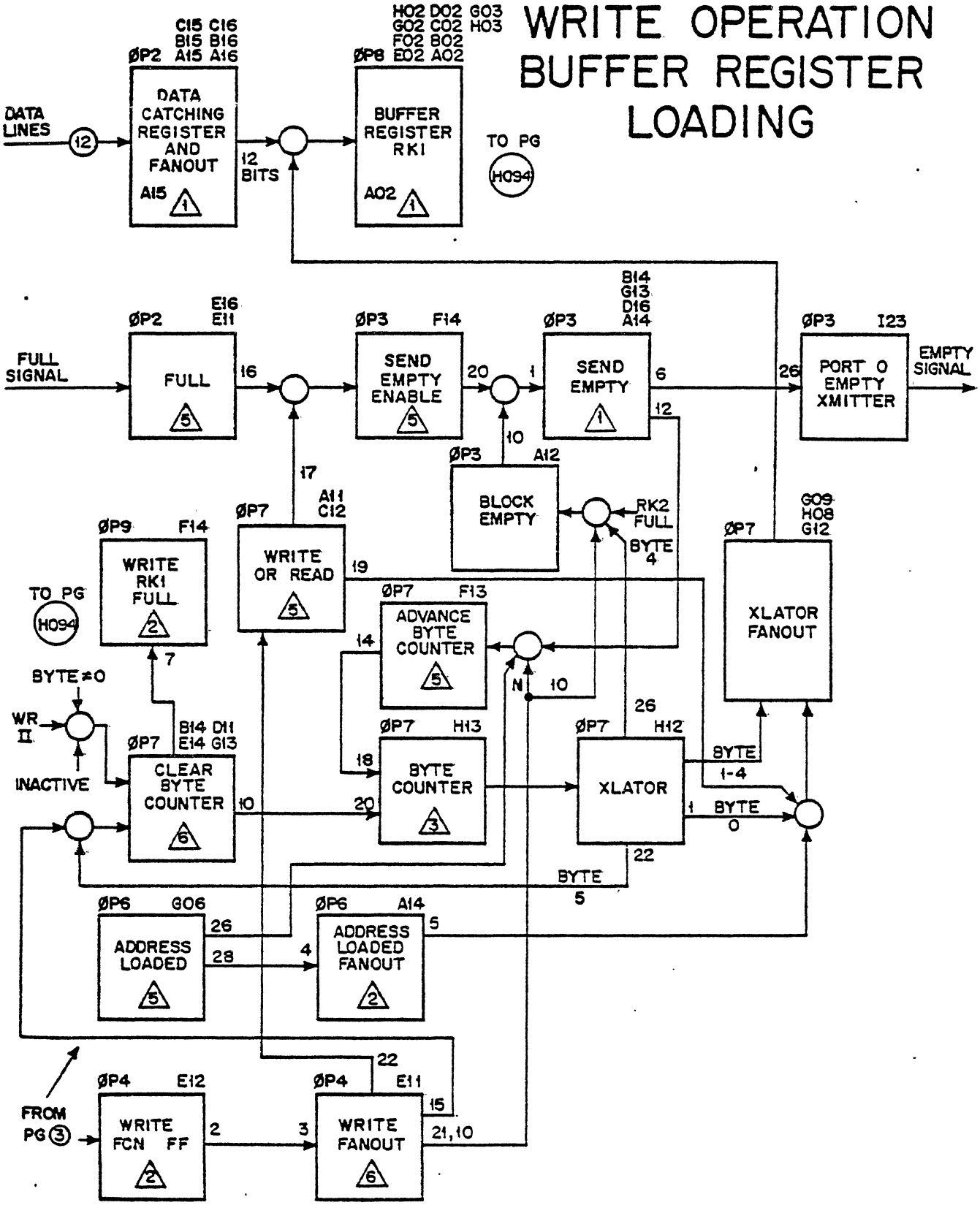
5004 FUNCTION SELECT STATUS



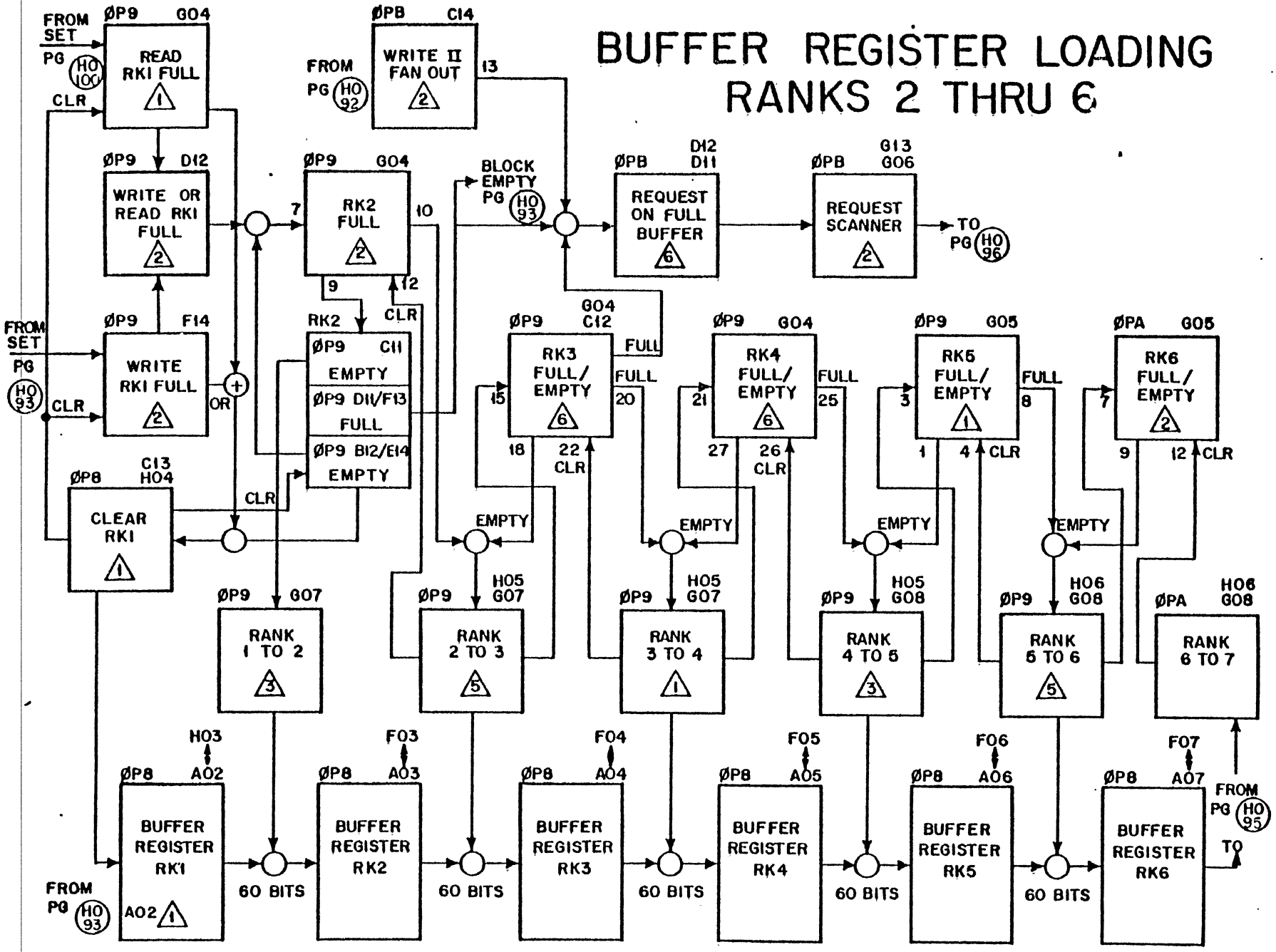
WRITE FUNCTION (5002) AND ADDRESS LOADING



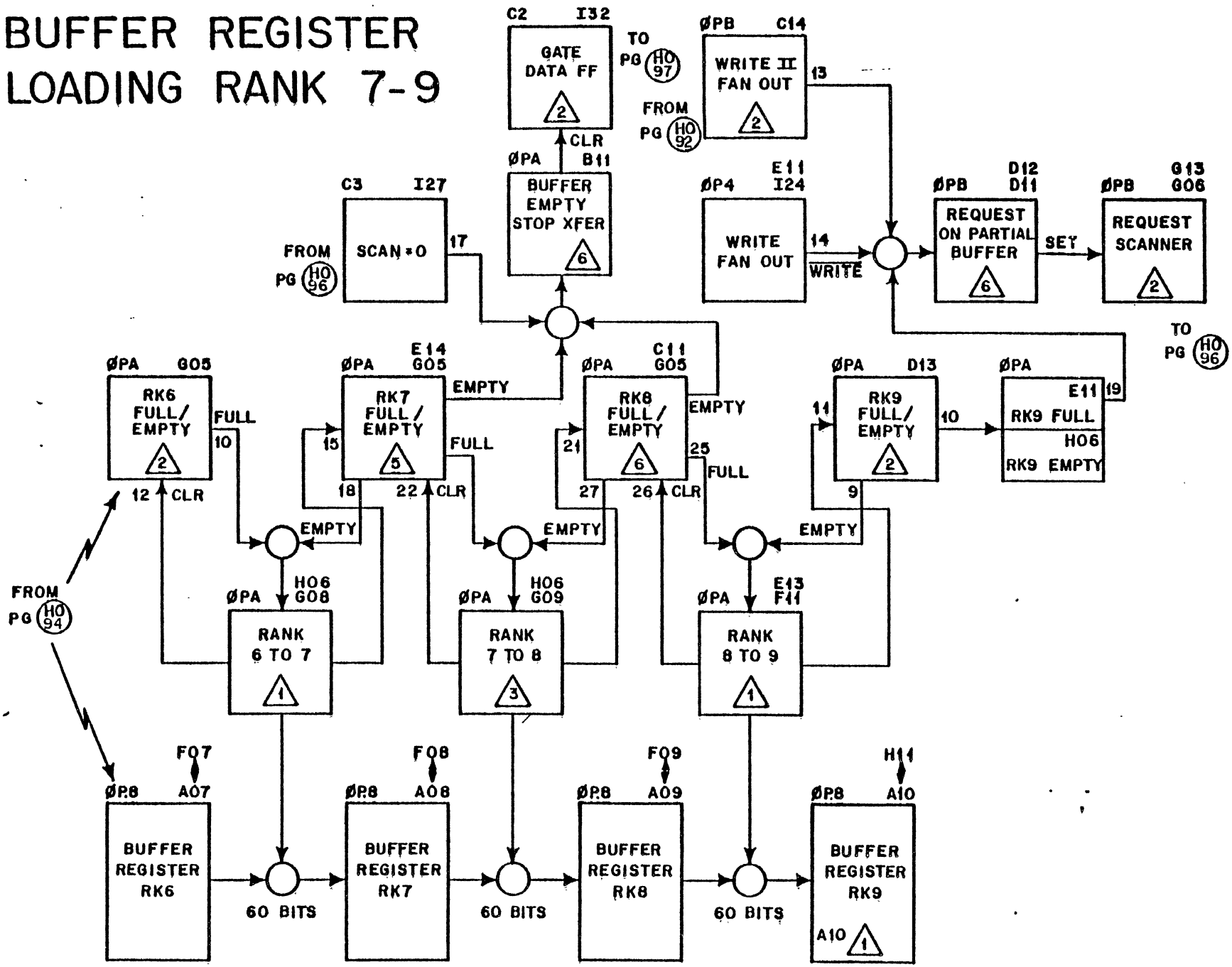
WRITE OPERATION BUFFER REGISTER LOADING

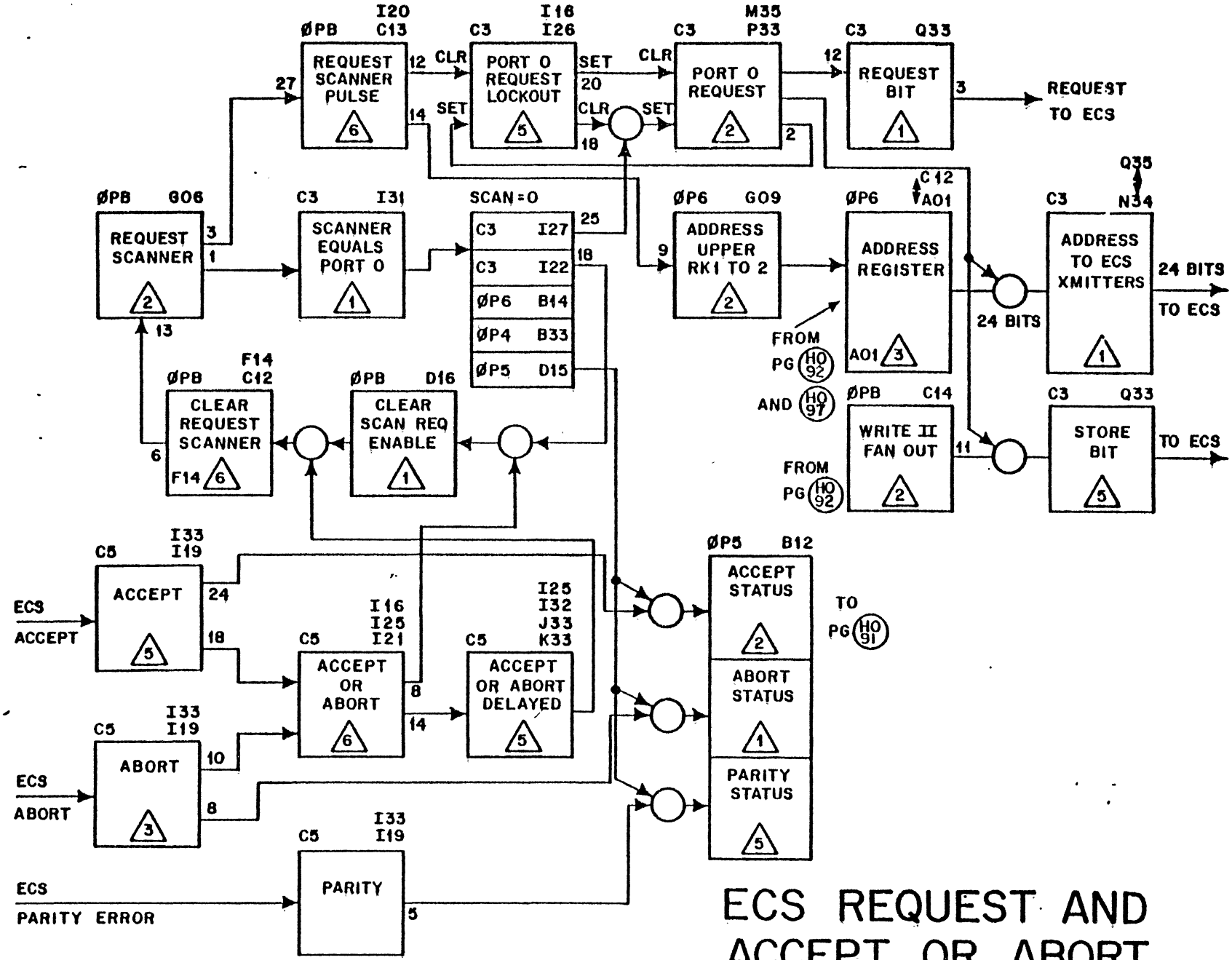


BUFFER REGISTER LOADING RANKS 2 THRU 6

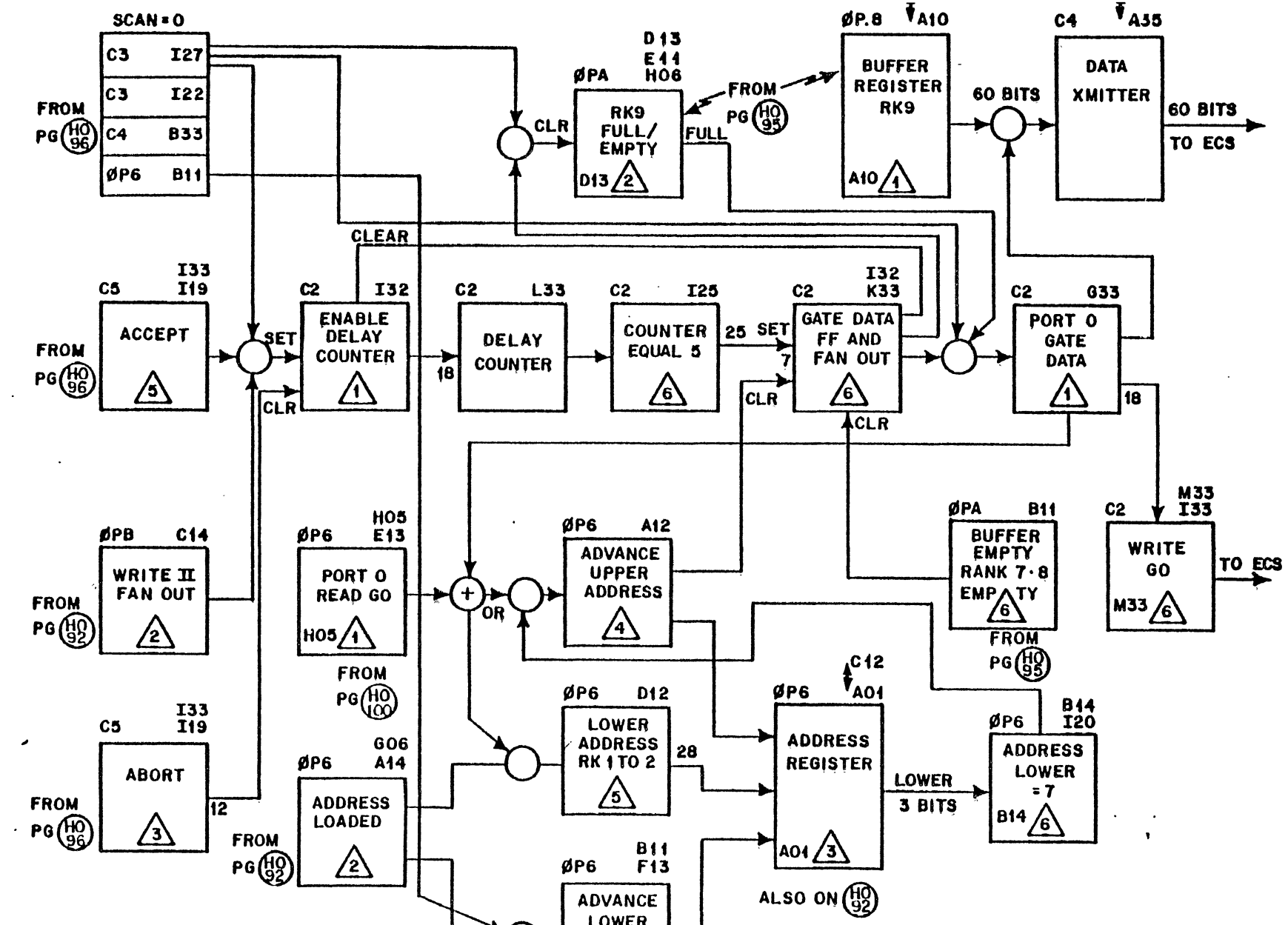


BUFFER REGISTER LOADING RANK 7-9



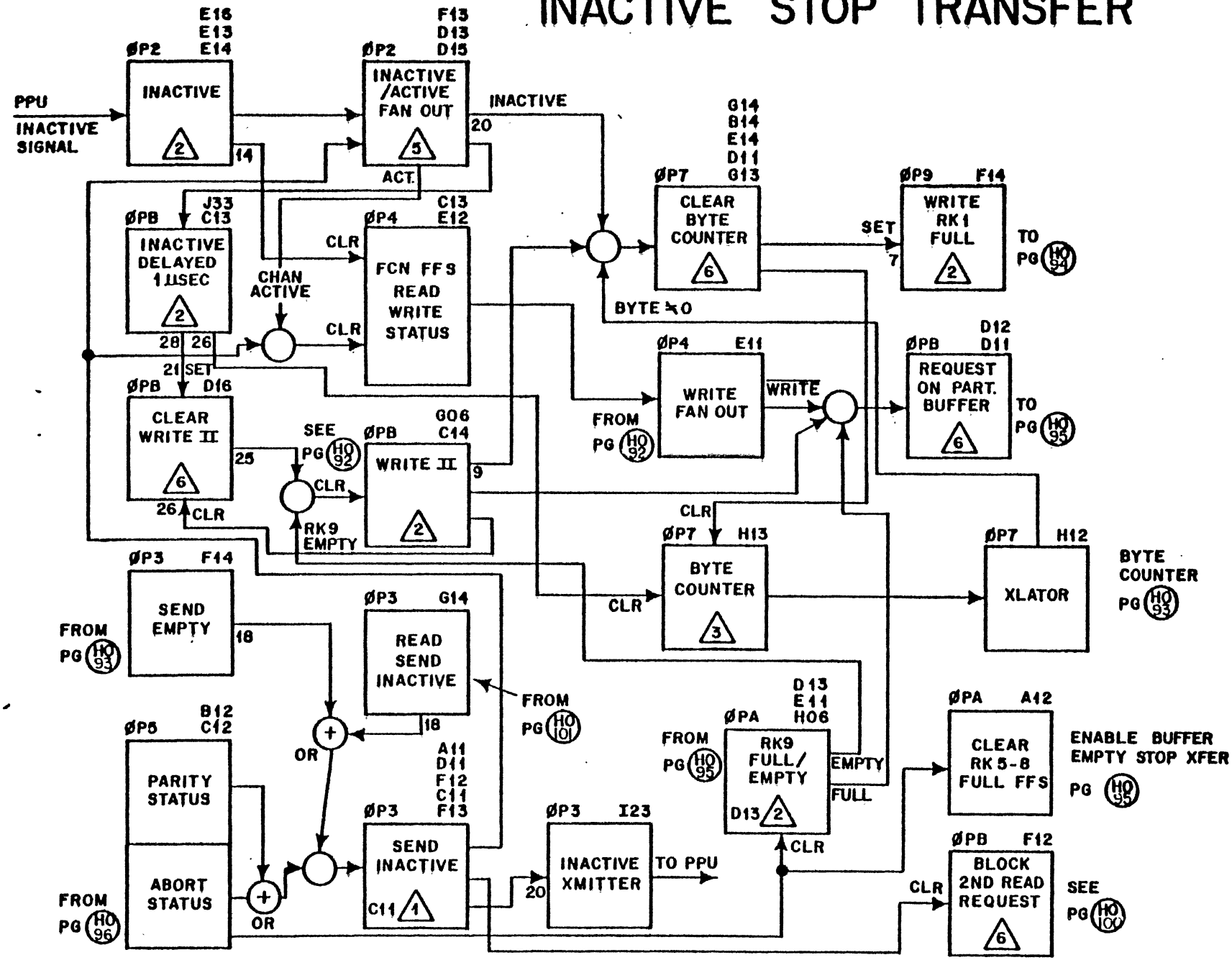


ECS REQUEST AND ACCEPT OR ABORT

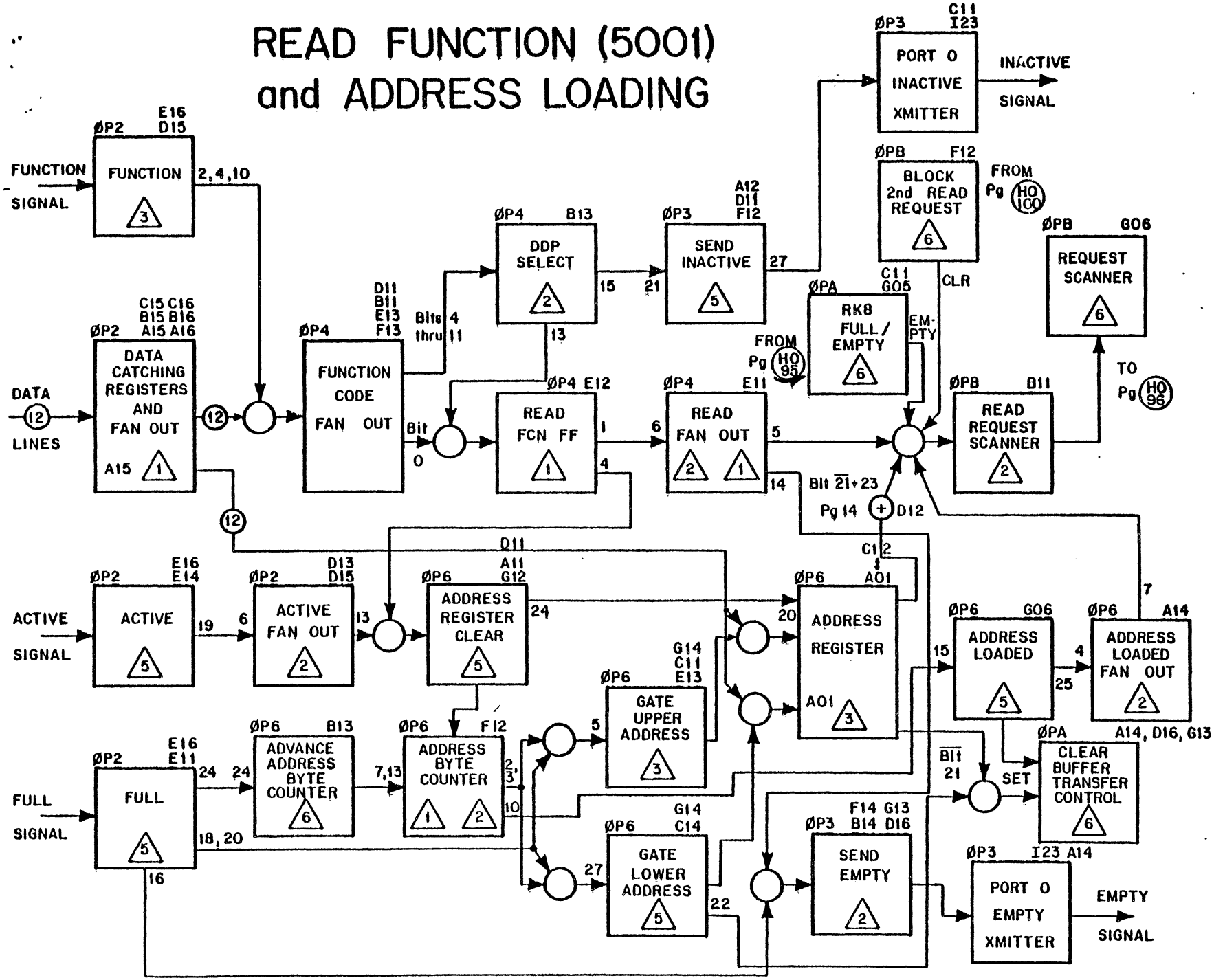


WRITE DATA TRANSFER & INCREMENT ADDRESS

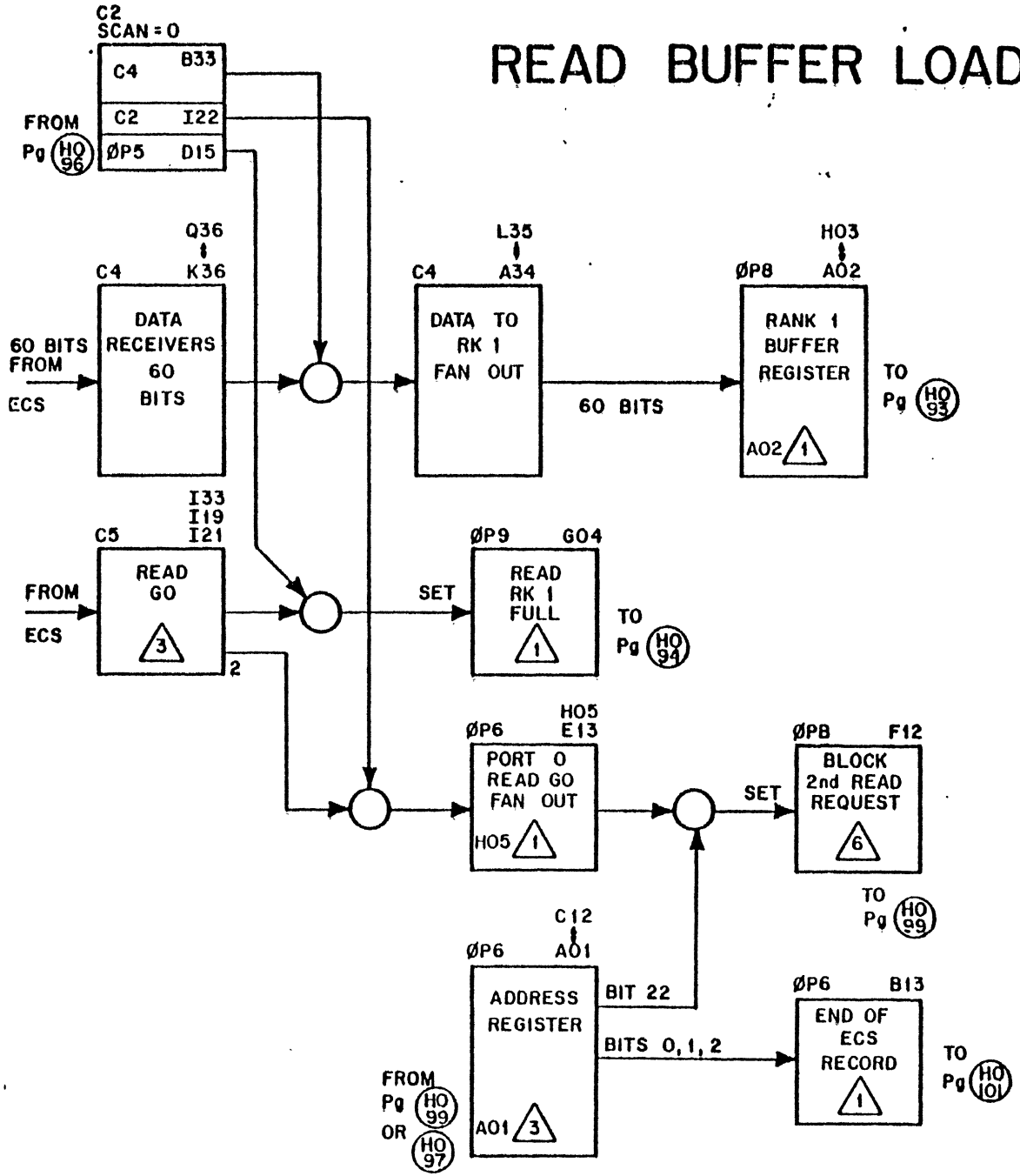
INACTIVE STOP TRANSFER



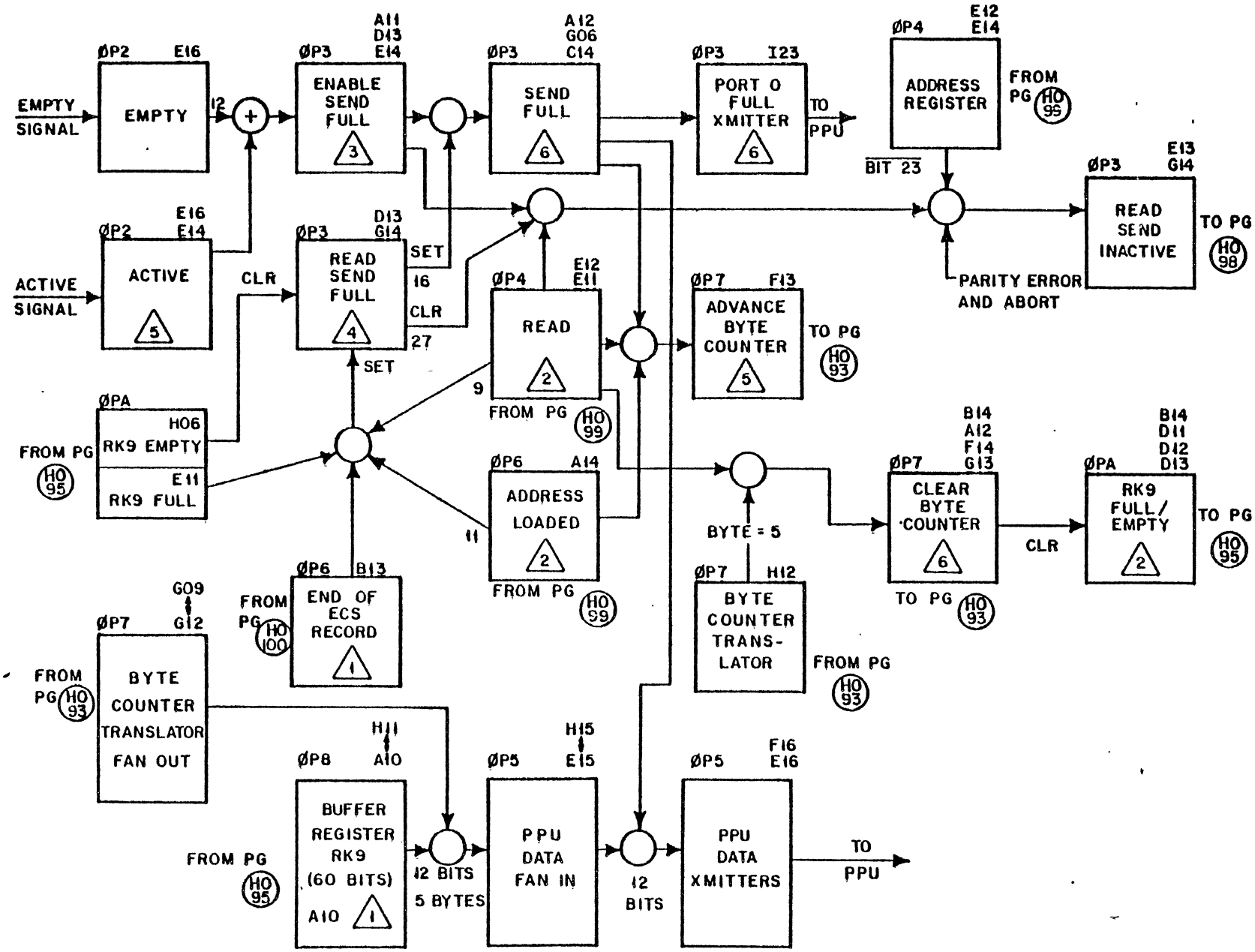
READ FUNCTION (5001) and ADDRESS LOADING



READ BUFFER LOADING



READ DATA TO PPU



PARAMETERS

Address
1500 = 0002
1501 = 1000
1502 = 0505
1507 = 0001
1510 = 7777
1512 = 0000
1513 = 0000
1514 = 0036
1515 = 5777
1516 = 0505
1517 = 7777
1520 = 7777
1521 = 7777
1522 = XXXX
1523 = 0037
1524 = 7777

Error Message

5014 0505 2 H04 Inactive 5030

History Table

7600 = 5030
7601 = 7777
7602 = 7777
7603 = 7777

PARAMETERS

Address
1500 = 0002
1501 = 1000
1502 = 0505
1507 = 0001
1510 = 7777
1512 = 0000
1513 = 0000
1514 = 0036
1515 = 5777
1516 = 0505
1517 = 7777
1520 = 7777
1521 = 7777
1522 = XXXX
1523 = 0037
1524 = 7777

Error Message

5021 0505 4 H10 Empty 5004

History Table

7600 = 5010
7601 = 7777
7602 = 7777
7603 = 7777
7604 = 5004
7605 = 7777
7606 = 7777
7607 = 7777

PARAMETERS

Address	L500 = 0002	L507 = 0001	L517 = 7777
	L501 = 1000	L510 = 7777	L520 = 7777
	L502 = 0505	L512 = 0000	L521 = 7777
		L513 = 0000	L522 = XXXX
		L514 = 0036	L523 = 0037
		L515 = 5777	L524 = 7777
		L516 = 0505	

Error Message

S030 0505 4 H14 Empty S001

History Table

7600	= S002
7601	= 1000
7602	= 0000
7603	= 0050
7604	= S004
7605	= 0010
7606	= 0000
7607	= 0000
7610	= S001
7611	= 1000
7612	= 0000
7613	= 0050

PARAMETERS

Address	L500 = 0002	L507 = 0001	L517 = 7777
	L501 = 1000	L510 = 7777	L520 = 7777
	L502 = 0505	L512 = 0000	L521 = 7777
		L513 = 0000	L522 = XXXX
		L514 = 0036	L523 = 0037
		L515 = 5777	L514 = 7777
		L516 = 0505	

Error Message

S051 0505 6 H20 Data A 7677 E7777 2 0000000

History Table

7600 = 5002
7601 = 0000
7602 = 0000
7603 = 0450
7604 = 5004
7605 = 0002
7606 = 7777
7607 = 7777
7610 = 5001
7611 = 0000
7612 = 0000
7613 = 0050
7614 = 5004
7615 = 0002
7616 = 7777
7617 = 7777

PARAMETERS

Address			
1500 = 0002	1507 = 0001	1517 = 7777
1501 = 1000	1510 = 7777	1520 = 7777
1502 = 0505	1512 = 0000	1521 = 7777
	1513 = 0000	1522 = XXXX
	1514 = 0036	1523 = 0037
	1515 = 7777	1524 = 7777
	1516 = 0505	

Error Message

S061 0505 6 H10 Data A0032 E0012 Y1 Z000123450

History Table

7600 = 5002
7601 = 0032
7602 = 3450
7603 = 0120

7604 = 5001
7605 = 0012
7606 = 3450
7607 = 0120

PARAMETERS

Address	1500 = 0002	1507 = 0000	1517 = 7777
	1501 = 1000	1510 = 0200	1520 = 7777
	1502 = 0505	1512 = 0000	1521 = 7777
		1513 = 0000	1522 = XXXX
		1514 = 0036	1523 = 0037
		1515 = 5777	1524 = 7777
		1516 = 0505	

Error Message

S101 0505 10 H10 Error See I Display

I Display

C2 Data A7777 , E0000 B1 W0000000

History Table

7600 =	5002
7601 =	1000
7602 =	0000
7603 =	0450
7604 =	5004
7605 =	0010
7606 =	7777
7607 =	7777

EQUIPMENT PERFORMANCE STANDARD

NO. DC135/DT174

DATE 2/28/72

Estimated system hours for completion: 1.5 hours for the DC135 plus .5 hours for each additional DT174 installed (assuming no problems are encountered which need corrective action before the EPS can continue).

1.0 REFERENCE DOCUMENTS:

1.1 6000/CYBER SMM Manual

1.2 6642 C.E. Manual

2.0 TEST EQUIPMENT:

2.1 Model 546 oscilloscope or equivalent

2.2 Precision D.C. voltmeter

2.3 Shock test tool, calibrated to 10 lbs. Insertion tool, P/N 12210773; Nylon tip, P/N 12209308

2.4 Delay probe, 33pf, P/N 18483101

3.0 TEST CONDITIONS:

Condition	Voltage D.C. Chassis Voltage
1	0% (+6.0 VDC)
2	+7 1/2%
3	-7 1/2%

4.0 TEST PROCEDURE:

4.1 Preliminary Electrical Inspection:

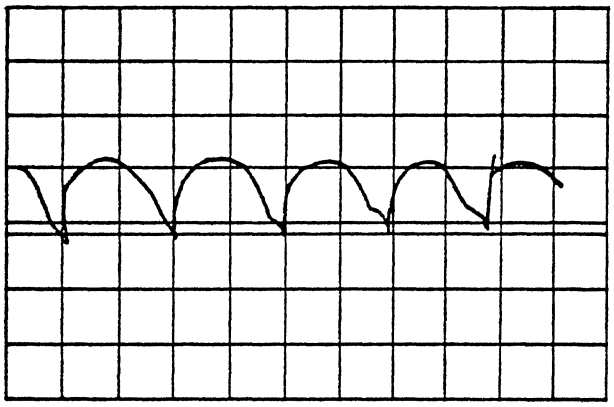
4.1.1 Measure any bus bar with the precision D.C. voltmeter; adjust the power supply to +6 ± .05 VDC. If power supply meter is not on 0%, calibrate meter.

4.1.2 Using the oscilloscope with a X1 probe, measure the ripple voltage on any +6 volt bus bar. The maximum allowable ripple is 100 mv.

4.1.3 Refer to Figure 1 and examine the power supply test points for proper wave forms. Correct any defects.

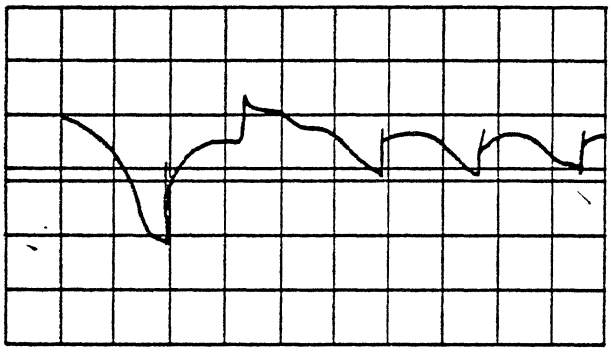
Power Supply Test Point Wave Forms

Good Wave Form:



1 VOLT/cm .1 msec/cm

One or More Open Diodes:



2 VOLTS/cm .1 msec/cm

4.1.4 Clock Checking:

Syncing the oscilloscope externally at I06, TP1 of the DDP, look at I15, TP2 with one probe. This is reference time, time 00. Examine the clocks listed in Table 2. All leading edges should match the time listed ± 2 nanoseconds. All the clock pulses should be 23-27 nanoseconds wide measured at half amplitude.

Table 2

Test Point	Time	Width
I06, TP-1	Sync.	-----
I15, TP-2	00	23-27
I14, TP-4	25	23-27
I15, TP-4	50	23-27
I15, TP-6	75	23-27

4.2 Performance Tests:

4.2.1 Initial Tests:

4.2.1.1 Run Section 5 of diagnostic "DDP" and momentarily ground TP1 of any RW module in the ECS bay. An ECS parity error should be detected by the diagnostic. Repeat for each installed DDP port.

4.2.1.2 Run Section 5 of DDP and put the ECS bay in Maintenance Mode (turn on "Maintenance Unlock" key and "Maintenance" switch). An ECS abort error should be detected by the diagnostic.

Repeat for each installed DDP port.

4.2.1.3 Run Section 1 of DDP and set the "Port Disable" switch for the port being used. An immediate error should occur. Reenable the port. Repeat for each installed port. The port disable switches are located on module I01 in the DDP. The top switch is for port 0 and the bottom switch for port 3.

4.2.2 Shock Tests:

4.2.2.1 Refer to Figure 2 and Table 3 and run indicated test. Use a 10 lb. shock test tool and randomly shock test 25 modules of each port. If more than one intermittent module or loose wire is found, shock test the entire port and control section.

4.2.2.2 Refer to Figure 2 and Table 3 and pat the wire mat while these tests are running to locate possible loose wires.

4.2.3 Delay Probe Margin Tests:

4.2.3.1 Run two complete passes of diagnostic "DDP" with the 33 p.f. delay probe on each of the test points in Table 4. Run Sections 1-3, 5-7 and 13 (1507 = 0167, 1510 = 0001, 1501 = 1000) with all ports running simultaneously.

4.2.4 Voltage Margin Tests:

4.2.4.1 Run Sections 1-3, 5-7, and 13 (1507 = 0167, 1510 = 0001, 1501 = 1000) of diagnostic "DDP" for 10 minutes at each of Conditions 2 and 3 (Table 1). Run all installed ports simultaneously.

4.2.5 Clock Tuning:

4.2.5.1 Refer to the DDP maintenance manual and check the 100 nsec pulse between F16-19 and F12-17. This must be 100 nsec ± 3.

4.2.5.2 Refer to the DDP maintenance manual and check ECS request timing.

FIGURE 2

DDP Chassis Map

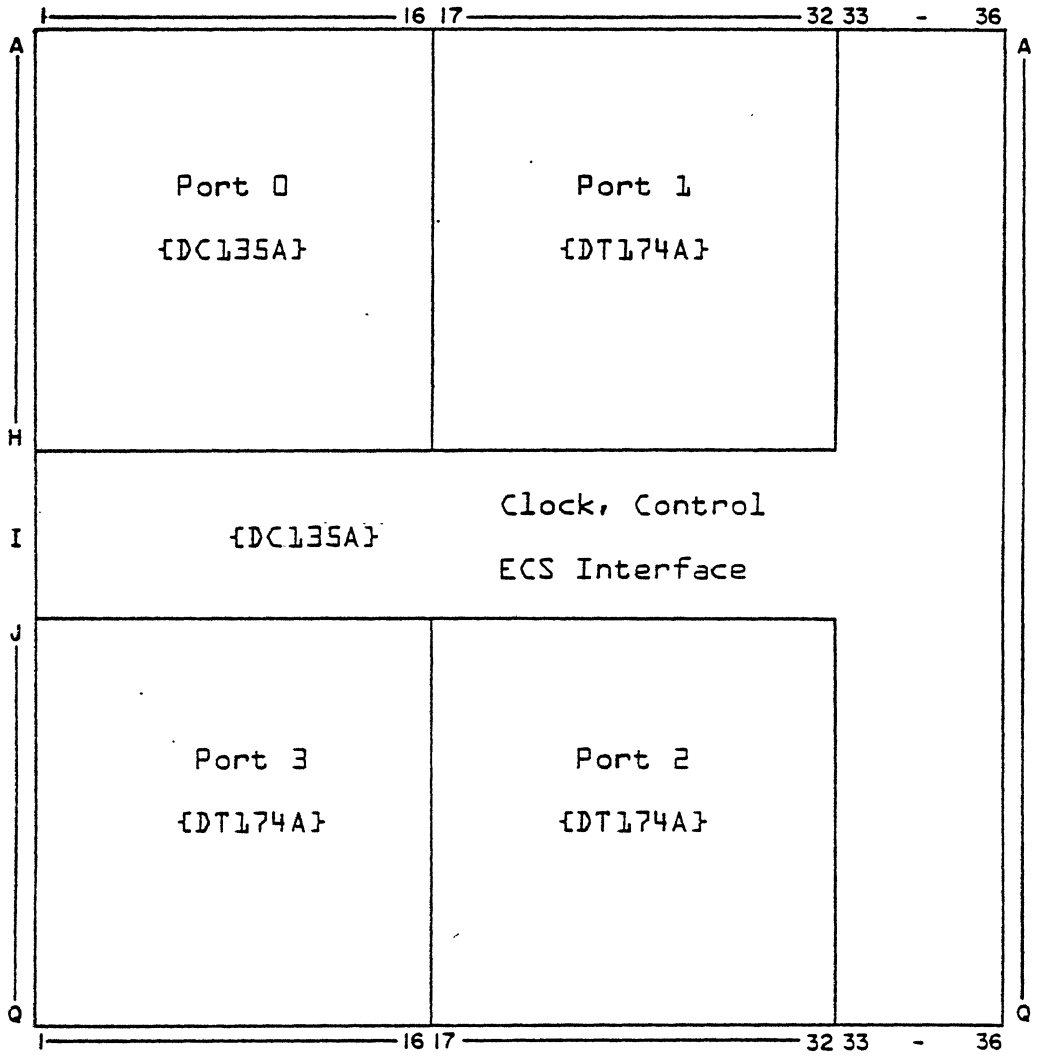


Table 3

Chassis Area	Test Sections	Parameters
Port 0	1507 = 0001 1510 = 0177	Run Port 0 only 1501 = 1002
Port 1	1507 = 0001 1510 = 0177	Run Port 1 only 1501 = 1002
Port 2	1507 = 0001 1510 = 0177	Run Port 2 only 1501 = 1002
Port 3	1507 = 0001 1510 = 0177	Run Port 3 only 1501 = 1002
Clock and Control	1507 = 0001 1510 = 0167	Run all installed ports simultaneously 1500 = 1002

Table 4

Delay Probe Test Points
I15, TP-4 I15, TP-6 I15, TP-2 I14, TP-4

SECTION 20 SENSE LINE-A ERROR STOP

P	S	YL	XL	XG	B	BK	W	BT	RFY	TP	ACTUAL DATA
0	0	0	01	1	0	3	3	00	4L10-5		0001000100010010000

SECTION 18 ERROR STOP

P	S	YL	XL	XG	B	BK	W	BT	RFY	TP	ACTUAL DATA
0	0	2	06	0	0	2	0	**	******		00000000000000023020

SHORT PROGRAM THAT CAN
BE USED UNDER CPC

```
ADDRESS
    10=51000 00100 46000 46000
    11=01200 00100 02000 00005
    12=51000 00200 46000 46000
    13=01100 00100 02000 00006
    14=02000 00010 00000 00000

     P=10
     X0=ECS ADDRESS
     FLECS=1000
```

00000030	0	0	0	00	0	0	3	0	00	4K42-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000031	0	0	0	00	0	0	3	1	00	4M31-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000032	0	0	0	00	0	0	3	2	00	4K21-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000033	0	0	0	00	0	0	3	3	00	4L10-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000070	0	0	0	00	1	0	3	0	00	4K42-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000071	0	0	0	00	1	0	3	1	00	4M31-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000072	0	0	0	00	1	0	3	2	00	4K21-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
173	0	0	0	00	1	0	3	3	00	4L10-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
130	0	0	0	00	2	0	3	0	00	4K42-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
131	0	0	0	00	2	0	3	1	00	4M31-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
132	0	0	0	00	2	0	3	2	00	4K21-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
133	0	0	0	00	2	0	3	3	00	4L10-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
170	0	0	0	00	3	0	3	0	00	4K42-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
171	0	0	0	00	3	0	3	1	00	4M31-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
172	0	0	0	00	3	0	3	2	00	4K21-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000173	0	0	0	00	3	0	3	3	00	4L10-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000430	0	0	0	01	0	0	3	0	00	4K42-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000431	0	0	0	01	0	0	3	1	00	4M31-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000432	0	0	0	01	0	0	3	2	00	4K21-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000433	0	0	0	01	0	0	3	3	00	4L10-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000470	0	0	0	01	1	0	3	0	00	4K42-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000471	0	0	0	01	1	0	3	1	00	4M31-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000472	0	0	0	01	1	0	3	2	00	4K21-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000473	0	0	0	01	1	0	3	3	00	4L10-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000530	0	0	0	01	2	0	3	0	00	4K42-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000531	0	0	0	01	2	0	3	1	00	4M31-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000532	0	0	0	01	2	0	3	2	00	4K21-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000533	0	0	0	01	2	0	3	3	00	4L10-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
570	0	0	0	01	3	0	3	0	00	4K42-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
571	0	0	0	01	3	0	3	1	00	4M31-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
572	0	0	0	01	3	0	3	2	00	4K21-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
573	0	0	0	01	3	0	3	3	00	4L10-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
1430	0	0	0	01	0	0	3	0	00	4K42-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
1431	0	0	0	01	0	0	3	1	00	4M31-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
1432	0	0	0	01	0	0	3	2	00	4K21-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
1433	0	0	0	01	0	0	3	3	00	4L10-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000470	0	0	0	01	1	0	3	0	00	4K42-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000471	0	0	0	01	1	0	3	1	00	4M31-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000472	0	0	0	01	1	0	3	2	00	4K21-4	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20
00000473	0	0	0	01	1	0	3	3	00	4L10-5	0001000100010001000	SHOULD BE	0001000100010001001	0000000000000000001	SECTION 20

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LISTING FROM 524K ECS

```
00007363   0 0 0 16 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00007763   0 0 0 17 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00007763   0 0 0 17 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00011223   0 0 1 02 4 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00011263   0 0 1 02 5 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00012223   0 0 1 04 4 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00012363   0 0 1 04 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00012763   0 0 1 05 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
[illegible]23   0 0 1 06 4 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
[illegible]3   0 0 1 06 5 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
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00015263   0 0 1 12 5 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00015363   0 0 1 12 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00015763   0 0 1 13 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00016263   0 0 1 14 5 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00016363   0 0 1 14 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
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00017323   0 0 1 16 6 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
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00017763   0 0 1 17 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
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0[illegible]3   0 0 1 17 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
0[illegible]3   0 0 2 02 4 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
0[illegible]3   0 0 2 02 5 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
0[illegible]3   0 0 2 02 6 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
0[illegible]3   0 0 2 02 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
0[illegible]3   0 0 2 03 4 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
0[illegible]3   0 0 2 04 4 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
0[illegible]3   0 0 2 04 6 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
0[illegible]3   0 0 2 04 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
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0[illegible]3   0 0 2 06 4 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00023263   0 0 2 06 5 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00023323   0 0 2 06 6 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00023363   0 0 2 06 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
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00024323   0 0 2 10 6 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00024363   0 0 2 10 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00024763   0 0 2 11 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00025223   0 0 2 12 4 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00025363   0 0 2 12 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00025763   0 0 2 13 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00026263   0 0 2 14 5 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00026323   0 0 2 14 6 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00026363   0 0 2 14 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00026763   0 0 2 15 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00027223   0 0 2 16 4 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00027323   0 0 2 16 6 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00027363   0 0 2 16 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00027763   0 0 2 17 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00022363   0 0 2 04 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
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00023263   0 0 2 06 5 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00023323   0 0 2 06 6 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00023363   0 0 2 06 7 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00023723   0 0 2 07 6 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
00024223   0 0 2 10 4 0 2 3 04  3K34-5  00000000000000000000  SHOULD BE 00000000000000000020   00000000000000000020   SECTION 18
```

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LISTING FROM 524K ECS

L7031

HO-115

LISTING FROM 524K ECS

00234023	1	0	3	10	0	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
00234123	1	0	3	10	2	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
00234023	1	0	3	10	0	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
00234123	1	0	3	10	2	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
00254123	1	0	5	10	2	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
00255123	1	0	5	12	2	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
00260023	1	0	6	00	0	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
00260123	1	0	6	00	2	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
3	1	0	6	14	1	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
3	1	0	7	12	2	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
3	1	0	7	14	0	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
3	1	0	7	04	0	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
3	1	0	7	10	0	0	2	3	47	3L41-4	77771777777777777777	SHOULD BE	77775777777777777777	00004000000000000000	SECTION 18
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LISTING FROM 131K ECS

HO-116

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00362007	7	1	1	00	0	0	0	7	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00364000	7	1	2	00	0	0	0	0	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00364001	7	1	2	00	0	0	0	1	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00364002	7	1	2	00	0	0	0	2	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00364003	7	1	2	00	0	0	0	3	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00364 4	7	1	2	00	0	0	0	4	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00364 5	7	1	2	00	0	0	0	5	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00364 6	7	1	2	00	0	0	0	6	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00364 7	7	1	2	00	0	0	0	7	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
END	TEST																
00340 0	7	0	0	00	0	0	0	0	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
0034 1	7	0	0	00	0	0	0	1	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
0034 2	7	0	0	00	0	0	0	2	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
0034 3	7	0	0	00	0	0	0	3	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
0034 4	7	0	0	00	0	0	0	4	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00341 5	7	0	0	00	0	0	0	5	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
0034 6	7	0	0	00	0	0	0	6	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00340007	7	0	0	00	0	0	0	7	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00342000	7	0	1	00	0	0	0	0	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00342001	7	0	1	00	0	0	0	1	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00342002	7	0	1	00	0	0	0	2	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00342003	7	0	1	00	0	0	0	3	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00342004	7	0	1	00	0	0	0	4	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00342005	7	0	1	00	0	0	0	5	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00342006	7	0	1	00	0	0	0	6	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00342007	7	0	1	00	0	0	0	7	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00344000	7	0	2	00	0	0	0	0	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00344001	7	0	2	00	0	0	0	1	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00344002	7	0	2	00	0	0	0	2	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00344003	7	0	2	00	0	0	0	3	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00344004	7	0	2	00	0	0	0	4	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00344005	7	0	2	00	0	0	0	5	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00344006	7	0	2	00	0	0	0	6	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00344007	7	0	2	00	0	0	0	7	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00346000	7	0	3	00	0	0	0	0	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
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00346002	7	0	3	00	0	0	0	2	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
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00346005	7	0	3	00	0	0	0	5	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00346006	7	0	3	00	0	0	0	6	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00346007	7	0	3	00	0	0	0	7	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00350000	7	0	4	00	0	0	0	0	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12
00350001	7	0	4	00	0	0	0	1	**	******	000000000000000000000	SHOULD	BE	777777777777777777777	777777777777777777777	SECTION	12

LISTING FROM 131K ECS

00000000	0	0	0	00	0	0	0	0	12	1K03-4	000000000000000010000	SHOULD BE	000000000000000000000	000000000000010000	SECTION 10
00000001	0	0	0	00	0	0	0	1	12	1K15-5	000000000000000010001	SHOULD BE	000000000000000000001	000000000000010000	SECTION 10
00000002	0	0	0	00	0	0	0	2	12	1L24-4	000000000000000010002	SHOULD BE	000000000000000000002	000000000000010000	SECTION 10
00000003	0	0	0	00	0	0	0	3	12	1L35-5	000000000000000010003	SHOULD BE	000000000000000000003	000000000000010000	SECTION 10
00000004	0	0	0	00	0	0	0	4	12	1K03-3	000000000000000010004	SHOULD BE	000000000000000000004	000000000000010000	SECTION 10
00000005	0	0	0	00	0	0	0	5	12	1K15-6	000000000000000010005	SHOULD BE	000000000000000000005	000000000000010000	SECTION 10
00000006	0	0	0	00	0	0	0	6	12	1L24-3	000000000000000010006	SHOULD BE	000000000000000000006	000000000000010000	SECTION 10
00000007	0	0	0	00	0	0	0	7	12	1L35-6	000000000000000010007	SHOULD BE	000000000000000000007	000000000000010000	SECTION 10
00000010	0	0	0	00	1	0	0	0	12	1K03-4	000000000000000010010	SHOULD BE	000000000000000000010	000000000000010000	SECTION 10
00000011	0	0	0	00	1	0	0	1	12	1K15-5	000000000000000010011	SHOULD BE	000000000000000000011	000000000000010000	SECTION 10
00000012	0	0	0	00	1	0	0	2	12	1L24-4	000000000000000010012	SHOULD BE	000000000000000000012	000000000000010000	SECTION 10
00000013	0	0	0	00	1	0	0	3	12	1L35-5	000000000000000010013	SHOULD BE	000000000000000000013	000000000000010000	SECTION 10
00000014	0	0	0	00	1	0	0	4	12	1K03-3	000000000000000010014	SHOULD BE	000000000000000000014	000000000000010000	SECTION 10
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00000016	0	0	0	00	1	0	0	6	12	1L24-3	000000000000000010016	SHOULD BE	000000000000000000016	000000000000010000	SECTION 10
00000017	0	0	0	00	1	0	0	7	12	1L35-6	000000000000000010017	SHOULD BE	000000000000000000017	000000000000010000	SECTION 10
00000020	0	0	0	00	2	0	0	0	12	1K03-4	000000000000000010020	SHOULD BE	000000000000000000020	000000000000010000	SECTION 10
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00000023	0	0	0	00	2	0	0	3	12	1L35-5	000000000000000010023	SHOULD BE	000000000000000000023	000000000000010000	SECTION 10
00000024	0	0	0	00	2	0	0	4	12	1K03-3	000000000000000010024	SHOULD BE	000000000000000000024	000000000000010000	SECTION 10
00000025	0	0	0	00	2	0	0	5	12	1K15-6	000000000000000010025	SHOULD BE	000000000000000000025	000000000000010000	SECTION 10
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00000031	0	0	0	00	3	0	0	1	12	1K15-5	000000000000000010031	SHOULD BE	000000000000000000031	000000000000010000	SECTION 10
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00000033	0	0	0	00	3	0	0	3	12	1L35-5	000000000000000010033	SHOULD BE	000000000000000000033	000000000000010000	SECTION 10
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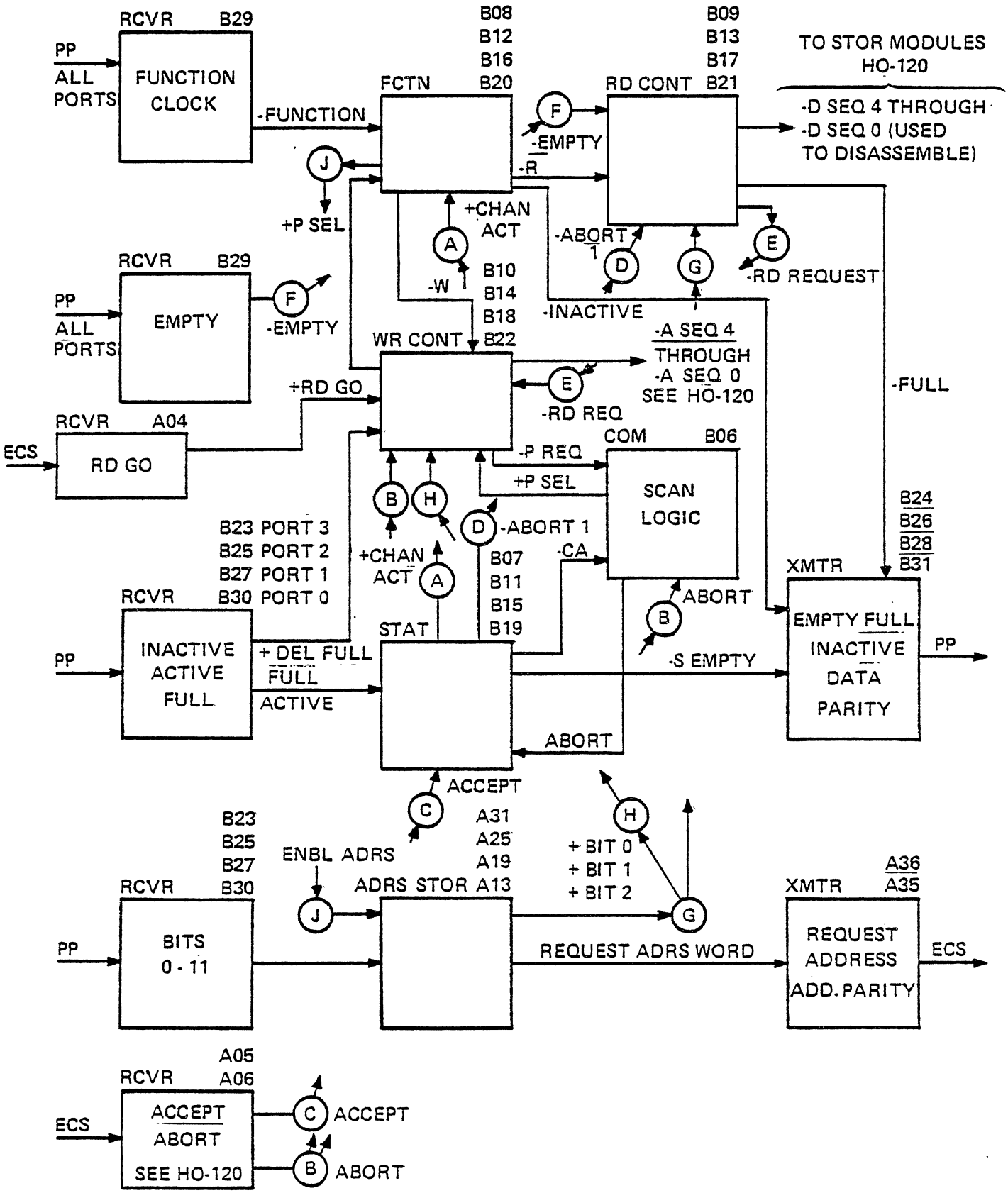
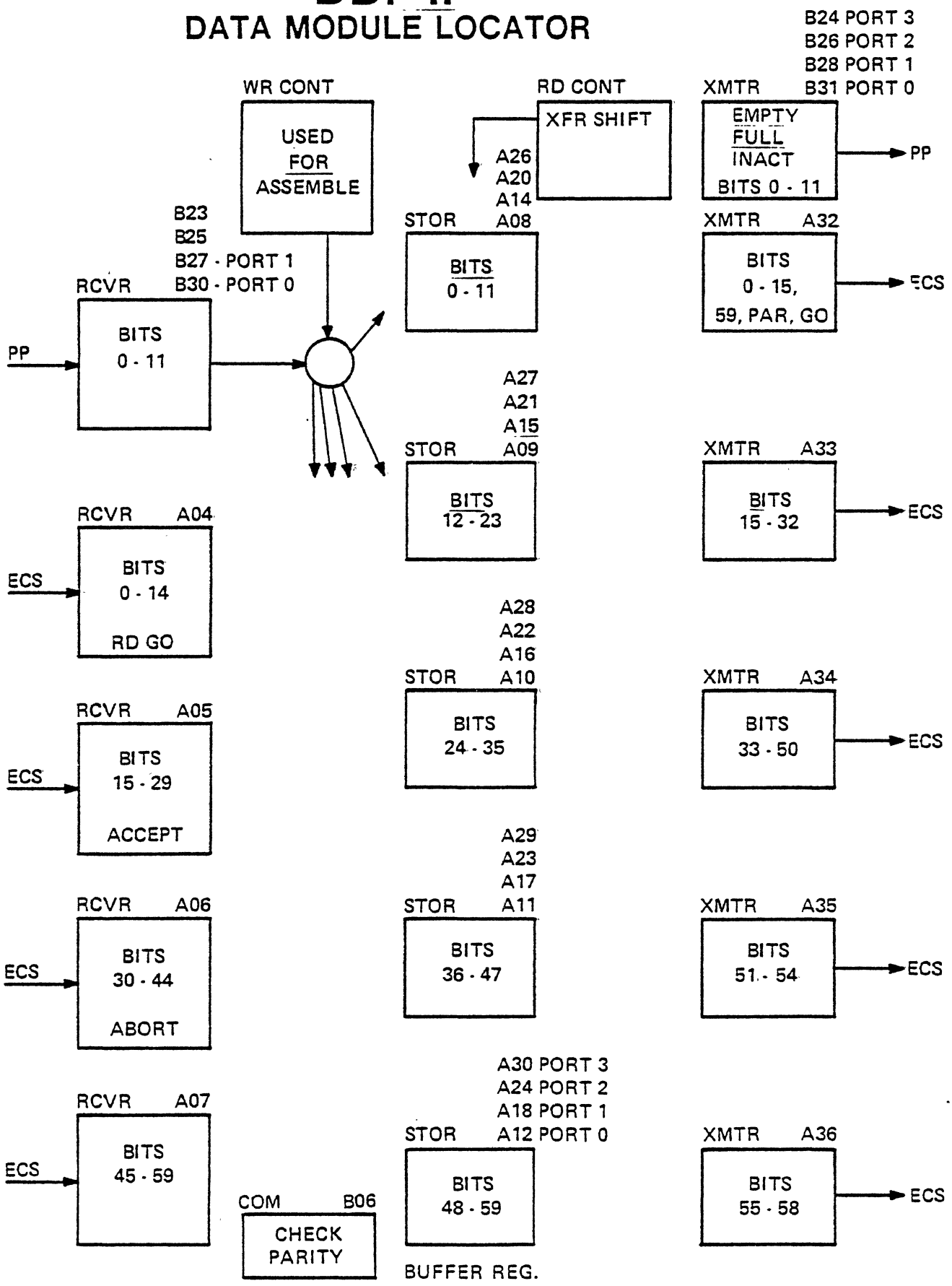
00000047	0	0	0	00	4	0	0	7	12	1L35-6	000000000000000010047	SHOULD BE	000000000000000000047	000000000000010000	SECTION 10
00000050	0	0	0	00	5	0	0	0	12	1K03-4	000000000000000010050	SHOULD BE	000000000000000000050	000000000000010000	SECTION 10
00000051	0	0	0	00	5	0	0	1	12	1K15-5	000000000000000010051	SHOULD BE	000000000000000000051	000000000000010000	SECTION 10
00000052	0	0	0	00	5	0	0	2	12	1L24-4	000000000000000010052	SHOULD BE	000000000000000000052	000000000000010000	SECTION 10
00000053	0	0	0	00	5	0	0	3	12	1L35-5	000000000000000010053	SHOULD BE	000000000000000000053	000000000000010000	SECTION 10
00000054	0	0	0	00	5	0	0	4	12	1K03-3	000000000000000010054	SHOULD BE	000000000000000000054	000000000000010000	SECTION 10
00000055	0	0	0	00	5	0	0	5	12	1K15-6	000000000000000010055	SHOULD BE	000000000000000000055	000000000000010000	SECTION 10
00000056	0	0	0	00	5	0	0	6	12	1L24-3	000000000000000010056	SHOULD BE	000000000000000000056	000000000000010000	SECTION 10
00000057	0	0	0	00	5	0	0	7	12	1L35-6	000000000000000010057	SHOULD BE	000000000000000000057	000000000000010000	SECTION 10
00000060	0	0	0	00	6	0	0	0	12	1K03-4	000000000000000010060	SHOULD BE	000000000000000000060	000000000000010000	SECTION 10
00000061	0	0	0	00	6	0	0	1	12	1K15-5	000000000000000010061	SHOULD BE	000000000000000000061	000000000000010000	SECTION 10
00000062	0	0	0	00	6	0	0	2	12	1L24-4	000000000000000010062	SHOULD BE	000000000000000000062	000000000000010000	SECTION 10
00000063	0	0	0	00	6	0	0	3	12	1L35-5	000000000000000010063	SHOULD BE	000000000000000000063	000000000000010000	SECTION 10
00000064	0	0	0	00	6	0	0	4	12	1K03-3	000000000000000010064	SHOULD BE	000000000000000000064	000000000000010000	SECTION 10
00000065	0	0	0	00	6	0	0	5	12	1K15-6	000000000000000010065	SHOULD BE	000000000000000000065	000000000000010000	SECTION 10
00000066	0	0	0	00	6	0	0	6	12	1L24-3	000000000000000010066	SHOULD BE	000000000000000000066	000000000000010000	SECTION 10
00000067	0	0	0	00	6	0	0	7	12	1L35-6	000000000000000010067	SHOULD BE	000000000000000000067	000000000000010000	SECTION 10
00000070	0	0	0	00	7	0	0	0	12	1K03-4	000000000000000010070	SHOULD BE	000000000000000000070	000000000000010000	SECTION 10
00000071	0	0	0	00	7	0	0	1	12	1K15-5	000000000000000010071	SHOULD BE	000000000000000000071	000000000000010000	SECTION 10
00000072	0	0	0	00	7	0	0	2	12	1L24-4	000000000000000010072	SHOULD BE	000000000000000000072	000000000000010000	SECTION 10
00000073	0	0	0	00	7	0	0	3	12	1L35-5	000000000000000010073	SHOULD BE	000000000000000000073	000000000000010000	SECTION 10
00000074	0	0	0	00	7	0	0	4	12	1K03-3	000000000000000010074	SHOULD BE	000000000000000000074	000000000000010000	SECTION 10
00000075	0	0	0	00	7	0	0	5	12	1K15-6	000000000000000010075	SHOULD BE	000000000000000000075	000000000000010000	SECTION 10
00000076	0	0	0	00	7	0	0	6	12	1L24-3	000000000000000010076	SHOULD BE	000000000000000000076	000000000000010000	SECTION 10

DDP II
CONTROL MODULES



DDP II
DATA MODULE LOCATOR



ECS II BANK

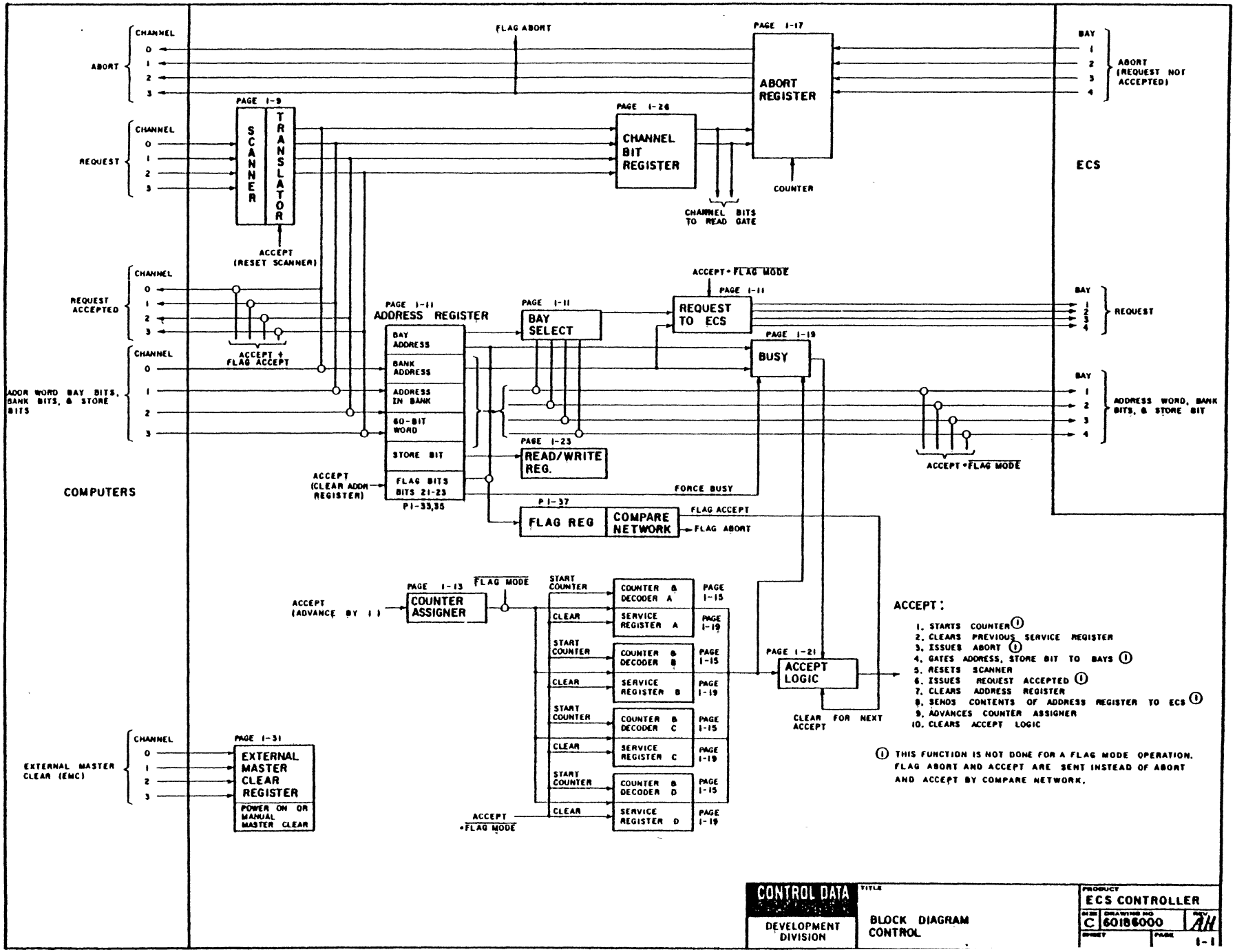
DATA MODULE LOCATOR

BITS 0-29	BITS 30-60
MM1 WORD 7	MM5 WORD 7
MM9 WORD 6	MM13 WORD 6
MM2 WORD 5	MM6 WORD 5
MM10 WORD 4	MM14 WORD 4
MM3 WORD 3	MM7 WORD 3
MM11 WORD 2	MM15 WORD 2
MM4 WORD 1	MM 8 WORD 1
MM12 WORD 0	MM16 WORD 0
BANK CONTROL MODULE	

NOTE:
bit 60 considered
parity bit

L7031

HO-122/TR-48



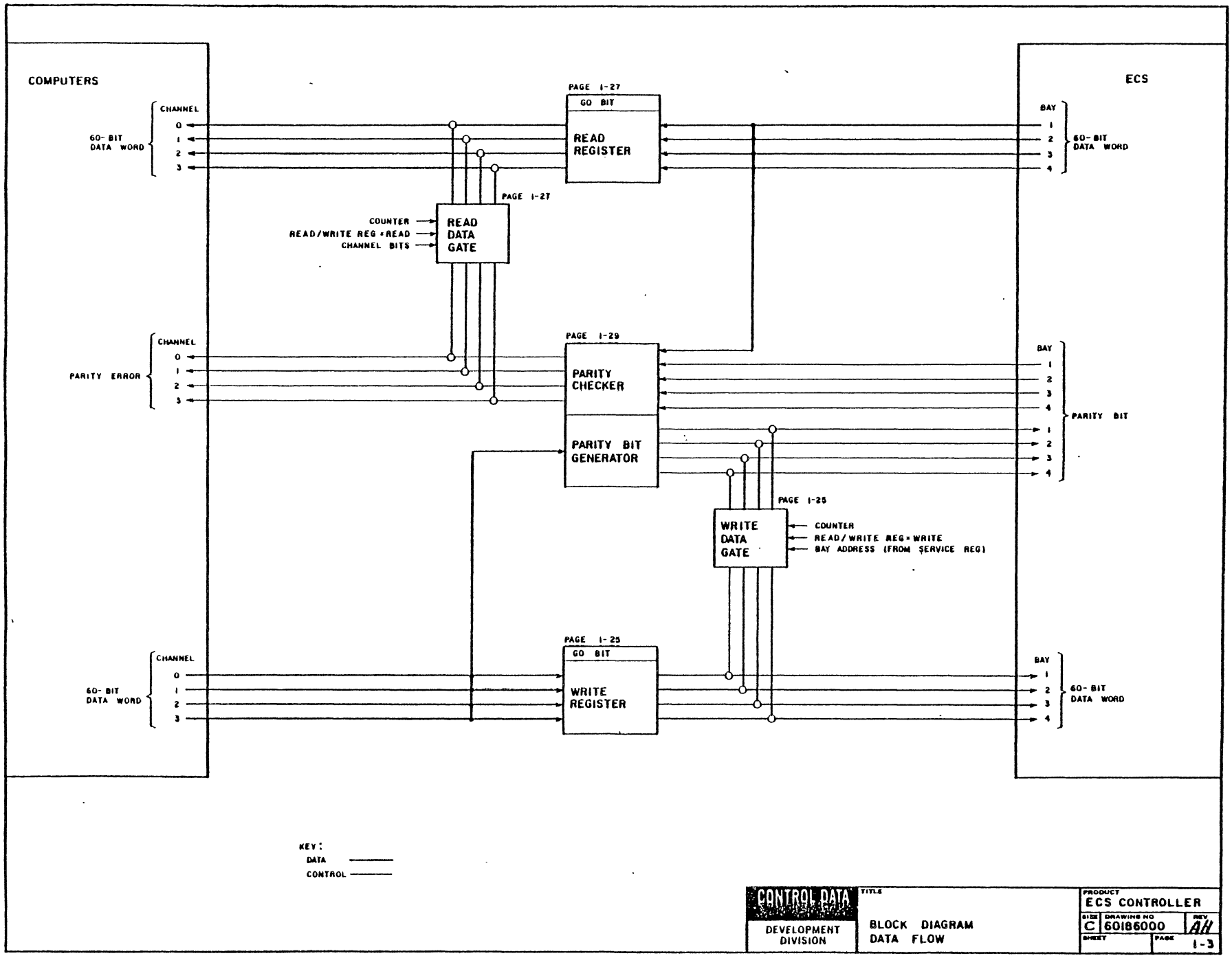
CONTROL DATA
DEVELOPMENT DIVISION

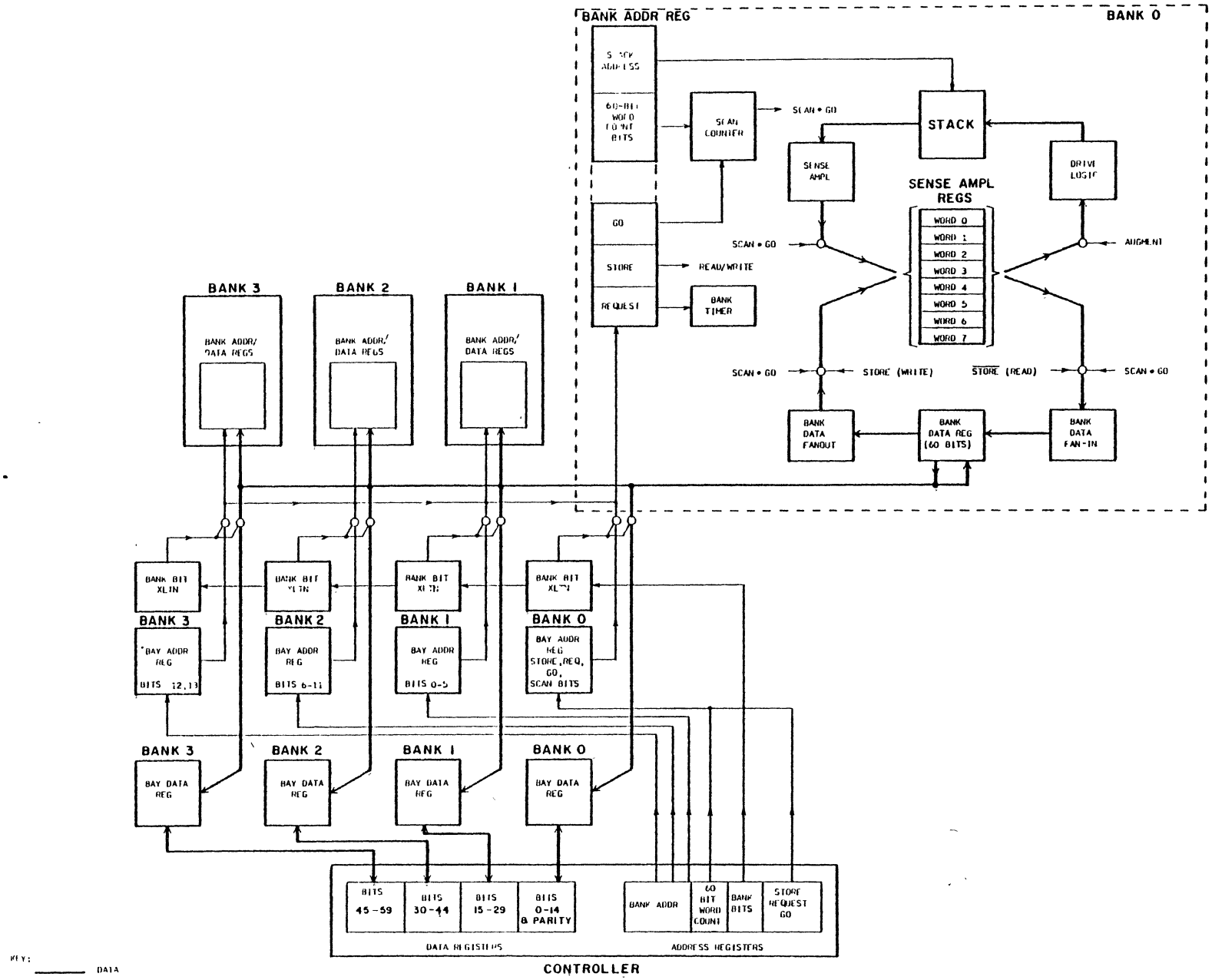
TITLE
BLOCK DIAGRAM CONTROL

PRODUCT
ECS CONTROLLER

SIZE C | DRAWING NO 60186000 | REV AH

SHEET | PAGE 1-1


COMPUTERS
ECS
CHANNEL
0
1
2
3
60-BIT DATA WORD
PAGE 1-27
GO BIT
READ REGISTER
BAY
1
2
3
4
60-BIT DATA WORD
PAGE 1-27
READ DATA GATE
COUNTER
READ/WRITE REG = READ
CHANNEL BITS
PARITY ERROR
PAGE 1-29
PARITY CHECKER
PARITY BIT GENERATOR
PARITY BIT
PAGE 1-25
WRITE DATA GATE
COUNTER
READ/WRITE REG = WRITE
BAY ADDRESS (FROM SERVICE REG)
PAGE 1-25
GO BIT
WRITE REGISTER
KEY:
DATA
CONTROL
CONTROL DATA
DEVELOPMENT DIVISION
TITLE
BLOCK DIAGRAM
DATA FLOW
PRODUCT
ECS CONTROLLER
SIZE C
DRAWING NO 60186000
REV AH
SHEET
PAGE 1-3



CONTROL DATA
THE NATION
DEVELOPMENT DIVISION

TITLE
BLOCK DIAGRAM

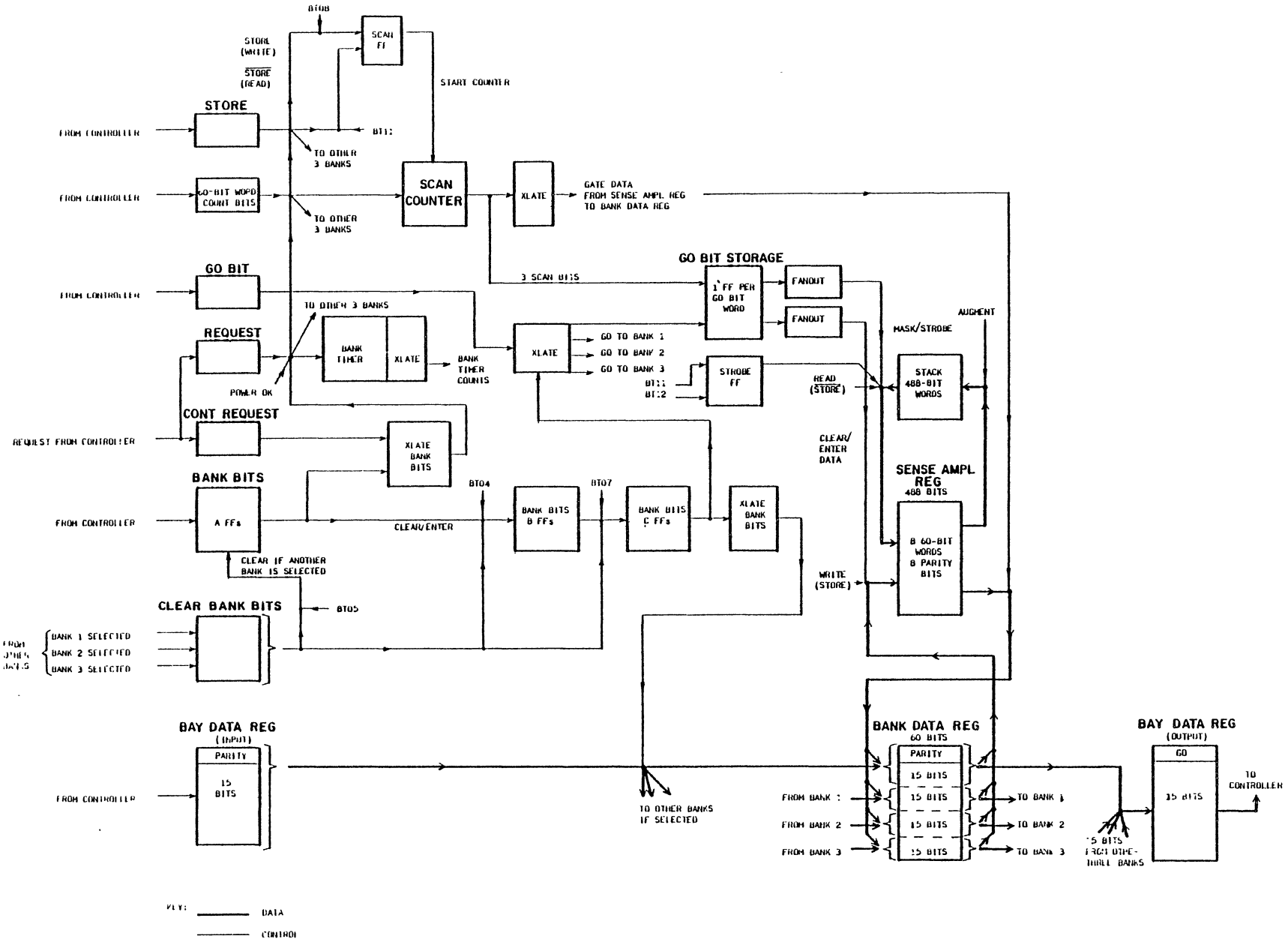
PRODUCT
ECS 524 K

SIZE	DRAWING NO	REV
C	60212200	V

SHEET
PAGE 1-1

L7031

HO-125/TR-51



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE DETAILED BLOCK DIAGRAM OF BANK 0	PRODUCT ECS 524 K	
		SIZE C	DRAWING NO 60212200 REV V
		SHEET	PAGE 1-3

WORKBOOK

INTRODUCTION TO WORKBOOK

The workbook or homework was designed to be an aid for your self evaluation and to improve your knowledge of the material covered in the classroom.

You will find that in most cases the questions or reading assignments will take less than the two hours reserved for study and some days there is no formal homework. This was done so you would have time to study any area you feel you need to. During your study time if you have questions or need some help or review of material, be sure to bring your questions to class, as each day a small amount of time is reserved for review.

On some of the homework you will find references for locating the needed material and on others no references were furnished. The reason for some of the references not being furnished is that it should help you to be able to locate needed material on a real hardware failure. ECS is a system that requires many manuals to document the hardware and you should have some knowledge of these manuals and there use.

WORKBOOK

DAY: 1

TOPIC: Introduction to ECS, Instruction Format,
ECS Address Format, ECS Terminology

OBJECTIVES: E.O. 0.1, E.O. 0.3, E.O. 0.4, E.O. 2.2, E.O. 2.3, E.O. 2.6, E.O. 2.7, E.O. 0.2

1. Review all material covered during class today.
2. Complete objective E.O. 0.2 (page TO-1)
3. Read complete reference manual (publication #60430000)

WORKBOOK

DAY: 2

TOPIC: CYBER 175 ECS coupler, CYBER 172/173/174 coupler

OBJECTIVES: E.O. 2.13, E.O. 2.8

1. Review handouts HO-6 through HO-47 and read backup pages. Note: only CYBER 175 trained people need to review these handouts.
2. P counter is used to tell how many bank initiates for each record, what are the two inputs to P and why?
3. What is K register used for?
4. Y = 0 checks is used for?
5. List pak locations for address bit 3 from the point of receiving bit from CPU to point of transmitting bit to controller.

   Note: CYBER 175 trained people only list paks in 175 coupler

   CYBER 173 trained people only list paks in 173 coupler
6. On a write ECS operation list pak locations for bit 24 of the data for the first 60 bit word from the point of receiving bit from CMC to transmitting bit to controller. See note on item 5.
7. The switch on pak at location 4B34 in the 173 coupler (shown on page 5-2-18 of diagrams) does what?

   Note: Only 173 trained people need to complete this item.
8. The switch on pak at location 4C35 in the 175 coupler (shown on HO-38) does what?

   Note: Only 175 trained people need to complete this item:

DAY: 2 (Cont.)

9. What is the Error Code Generator in the coupler used for?

10. Once End Time Starts why is there a delay in time before the End of Transfer signal back to the CPU?

11. Review 173 Coupler Diagrams and read back up pages.

    Note: Only 173 trained people need to complete item 11.

WORKBOOK

DAY: 3

TOPIC: 6640 A/B Controller

OBJECTIVES: E.O.2.6, E.O.2.23, E.O.2.21, E.O.2.19, E.O.2.22

1. On a 524K ECS System, if the coupler sends a request and Address of 1777777, and the controller was in degrade mode, what would happen?

2. List the modules that Bit 5 of Address uses from point of receiving to point of transmitting to Bay. Assume controller is not in degrade mode and 524K ECS System.

3. On a 524K ECS System, if the coupler sends a request and Address of 37720, and the controller was in degrade mode, what Bank would be used?

4. What is the Channel Bit Register used for?

5. Why are the Data Gate translations for Write ECS Data Inputs for the Bay select taken off the service register rather than the Address Register? (Page 1-25)

6. On an ECS Write Instruction (01100 00002) and

   X0 = 00000 00000 00400 00001

   A0 = 000000

   RAE = 00003000

   RAC = 000100

   FLC = 000010

   FLE = 40000000

   FLAG REGISTER IN CONTROLLER = 000 000

   What would happen when instruction is executed?

7. What are the Bay Bits used for in the Controller?

8. Why are the Bank Bits each transmitted on 4 transmitters to Bay, while Address bit 5 is only transmitted on one transmitter? (Page 1-11)

9. Review 6640 Manual and read write ups on facing pages.

WORKBOOK

DAY: 5

TOPIC: 6635

OBJECTIVES: E.O. 2.7, E.O. 2.30, E.O. 2.31

READ: Back up pages in 6635 manual for logic publication #60212200.

1. What is the scan counter used for? (page 1-21 of 6635 manual)
2. What is the GO bit coming from the controller on as write ECS operations used for? Why is it needed?
3. List all the modules that bit 10 of the data word passes through from receiver module to the RFY module in the BAY on a write ECS when the controller received Address 1600025. Assume 524K ECS bay.
4. List modules that address bit 10 passes through in the 6635 (524K) to get to the correct chassis when the controller received address 1602025.
5. What are the translations off of module 1N34 on page 1-19 of 6635 manual used for?
6. If the wire was removed from pin 26 of BA module at location 1B12 (shown on page 1-11 of 6635 manual) what would the lowest 2 memory locations that would fail? How many locations would fail? Give stack addresses for first question.

WORKBOOK

DAY: 5

TOPIC: 6635

7. If only stack addresses listed below failed to write correct data in locations could the failure be caused by 1B12 module? (shown on page 1-11 of 6635 manual) explain your answer.

Stack addresses that fail

170
370
570
770
1170
1370
1570
1770
2170
2370
2570
2770
3170
3370
3570
3770

Note: all other stack addresses work OK.

WORKBOOK

DAY 7

TOPIC: DDPI

OBJECTIVES: E.O.0.15, E.O.0.16, E.O.2.40, E.O.2.41

READ ASSIGNMENT: Read SMM write up for DDP Diagnostics

1. Write a PP Program to Clear Port, Write one ECS Record to Address 173654, then read that record. Assume the DDP is cabled to channel 5 and start program at address 100.

2. DC Power on and temperature warning light both lite would indicate what condition?

3. What bit positions will the first 12 data bits be loaded into Rank 1?

4. Why does Rank 2 full and byte count = 4 stop the empty signal from being sent to the PP?

5. What conditions is necessary for Request ECS on a READ? Why?

6. What conditions are necessary to start the transfer of Rank 9 to the PP? Why?

WORKBOOK ANSWERS

DAY: 1

TOPIC: ECS Terminology

2. a. ECS Record = 8 - 60 bits words located at any ECS address which has "0s" in bit positions 0, 1 and 2 of address.

   b. Error Exit - Cause by error such as parity errors, power off on bay, bay in maintenance mode or Illegal ECS Address and will cause CPU to exit to parcel 2 for next instruction.

   c. Full Exit - Normal exit (lack of errors on operation) and will cause CPU to exit to P + 1 for next instruction.

   d. Half Exit = Some times used in place of error exit - means same as error exit.

   e. Fake Read - When on a read ECS operation the coupler transfer zero's to central memory without requesting controller more than once. This is caused by an illegal address.

   f. Illegal Address - ECS address too large for size of ECS memory.

   g. Bay - Hardware that contains ECS memory.

   h. Controller Accept - Replay from controller on Request from coupler - on data transfer operation tells coupler bay memory is about to cycle - on flag operation also reply and on flag functions 4 or 6 says positive compare.

   i. Controller Abort - Reply from controller cause by parity errors, illegal address, power off on bay, maintenance mode on bay or negative compare on flag function.

WORKBOOK ANSWERS

DAY: 2

TOPIC: CYBER 175 ECS Coupler, CYBER 172/173/174 Coupler

OBJECTIVES:

2. P counter is used to tell how many Bank Initiates for each record, what are the two inputs to P and why?

   K and Y-1

   K contains the lower three bits of the ECS address and the compliment of K would actual translate number of words in the record minus one for all records put the last record of the transfer. Y contains number of words and on the last record Y-1 would tell number of words in the last record needed for the transfer minus 1. This will take care of cases where the whole last record is not wanted on the transfer.

3. What is K register used for?

   K register is used to hold the lower three bits of the address and checked with Y to determine when to set P up for last record.

4. Y = 0 check is used for?

   Y = 0 check is used to start end time which will start the termination of a data transfer.

5. List pak locations for address bit 3 from the point of receiving bit from CPU to point of transmitting bit to controller.

   Note: CYBER 175 trained people only list paks in 175 coupler

   CYBER 173 trained people only list paks in 173 coupler

DAY: 2 (Cont.)

175 Coupler	4E21, 4E29, 4C27	
173 Coupler	CPU-0 4B19	4D28, 4B26
	CPU-1 4D19	

6. On a write ECS operation list pak locations for bit 24 of the data for the first 60 bit word from the point of receiving bit from CMC to transmitting bit to controller. See note on item 5.

175 Coupler	4C11, 4E08, 4E27
173 Coupler	4D26

7. The switch on pak at location 4B34 in the 173 coupler (shown on page 5-2-18 of diagrams) does what?

   Note: Only 173 trained people need to complete this item.

   - The switch allows the coupler to work with controller that have parity enhancement (6640 D/E) and old type controller (6640 A/B). When switch is on the logical 0 contact input data errors to CMC are not checked.

8. The switch on pak at location 4C35 in the 175 coupler (shown on HO-38) does what?

   Note: only 175 trained people need to complete this item:

   - See answer to question 7.

9. What is the Error Code Generator in the coupler used for?

   To transmit error code to S/C register. Code tells programmer what type of error at termination of ECS operation.

DAY: 2 (Cont.)

10. Once End Time starts why is there a delay in time before the End of Transfer signal back to the CPU?

To allow the last record to complete the data transfer.

WORKBOOK ANSWERS

DAY: 3

TOPIC: 6640 A/B Controller

1. On a 524K ECS System, if the Coupler sends a request and Address of 1777777, and the Controller was in degrade mode what would happen?

   Answer

   The Controller would reply with an Accept followed by an Abort. Accept II would not come up as this would be an illegal address in degrade mode.

2. List the modules that Bit 5 of Address uses from point of receiving to point of transmitting to Bay'. Assume Controller is not in degrade mode and 524K ECS System.

   Answer

Channel	0	F29	
	1	F31	C34
	2	F33	
	3	F35	

3. On a 524K ECS system, if the coupler sends a request and Address of 37720, and the controller was in degrade mode, what Bank would be used?

   Answer

   It would depend on switch for Bit 4 on module at location A04, if Bit 4 was forced set by switch Bank 2, and if Bit 4 was forced clear by switch Bank 0.

4. What is the Channel Bit Register used for?

Answer

The Channel Bit Register is used to Gate Data to the correct channel and is needed because the scanner is released long before data arrives from the controller.

5. Why are the Data Gate translations for Write ECS Data Inputs for the Bay select taken off the service register rather than the Address Register? (Page 1-25)

Answer

The input for Data Gate Translation are from the service register because by the time data arrives from the coupler or CM, the Address Register would have been cleared.

6. On an ECS Write Instruction (01200 00002) and

X0 = 00000 00000 00400 00001

A0 = 000000

RAE = 0000 3000

RAC = 000100

FLC = 000010

FLE = 4000 0000

FLAG REGISTER IN CONTROLLER = 000 000

What would happen when instruction is executed?

Answer

The flag Register would end up with Bit 0 set and the controller would return an Accept to the coupler causing CP to full exit.

7. What are the Bay Bits used for in the Controller?

Answer

The Bay Bits are used to translate so Address will only be transmitted to Correct Bay. BayBits also go to the service with the Bank Bits and are used to check for Busy Banks.

8. Why are the Bank Bits each transmitted on four transmitters to Bay while Address Bit 5 is only transmitted on one transmitter? (Page 1-11)

Answer

The Bank Bits are used in the Bay to direct Address and Data to correct Chassis. All chassis need bank bits.

WORKBOOK ANSWERS

TOPIC: 6635

1. What is the scan counter used for? (page 1-21 of 6635 manual)

ANSWER

The scan counter is used on a write ECS to assemble 60 bit word into an ECS record and on a read ECS is used to disassemble an ECS record into 60 bit words.

2. What is the GO bit coming from the controller on a write ECS operation used for? Why is it needed?

ANSWER

The GO bit is used to tell GO bit storage register that 60 bit word is good data. It is needed in the case of a particle record is to be written into memory. If writing a particle record when GO bits stop coming the CLEAR/ENTER terms for the sense amplifier register are not going to allow data from controller into sense amplifier register. The data from the sense amplifiers will be written for the part of the record that had no GO bit from the controller.

3. List all the modules that bit 10 of the data word passes through from receiver module to the RFY module in the bay on a write ECS when the controller received address 1600025. Assume 524K ECS bay.

ANSWER

Bay data input register	Bank data register	Bank data fan-out
1N35	3Q20	3R25

Sense amplifier register	RFY module
3Q13	3M14

WORKBOOK ANSWERS

DAY: 5
TOPIC: 6635

4. List modules that address bit 10 passes through in the 6635 (524K) to get to the correct chassis when the controller received address 1602025.

ANSWER

Bit 10 is STACK ADDRESS bit 8 on a 524K ECS system.
Received on module 2Ø06 transmitted to 3Ø34

5. What are the translation off of module 1N34 on page 1-19 of 6635 manual used for?

ANSWER

The translations are bank translations are used on a write ECS operation to direct data to the correct chassis.

6. If the wire was removed from pin 26 of BA module at location 1B12 (shown on page 1-11 of 6635 manual) what would the lowest 2 memory locations that would fail? How many locations would fail?

ANSWER

First two locations to fail would be STACK ADDRESS 00170 (octal)
and 00370 (octal)
There would be 128 bad stackaddresses. (128 records)
or
1K of 60 bit words

DAY: 5

7. If only stack addresses listed below failed to write correct data in locations could the failure be caused by 1B12 module? (shown on page 1-11 of 6635 manual) explain your answer:

Stack addresses that fail

170
370
570
770
1170
1370
1570
1770
2170
2370
2570
2770
3170
3370
3570
3770

Note: all other stack addresses work OK

ANSWER

Module 1B12 most likely would not be the problem as it feeds all planes and only one plane is failing. This could be a bad connector on the X jumpers on the stack. (one pin on connector)

DAY 7

TOPIC: DDP

1. Write a PP Program to Clear Port, write one ECS record to Address 173654, then read that record. Assume the DDP is cabled to channel 5 and start program at address 100.

Answer

```
0100 = 6505
0101 = 0103
0102 = 7505
0103 = 7705          Function Clear Port
0104 = 5010
0105 = 7705          Function Write
0106 = 5002
0107 = 7405
0110 = 2000
0111 = 0017
0112 = 7205          Output Upper 12 Bits of Address
0113 = 2000
0114 = 3654          Output Lower 12 Bits of Address
0115 = 7205
0116 = 1450
0117 = 7305          Output
0120 = XXXX
0121 = 6605          *See Program Note
0122 = 0121
0123 = 7505
0124 = 7705          Status
0125 = 5004
0126 = 7405
0127 = 7005          Input Status
0130 = 3460          Save Status
0131 = 1201          Check for Abort
0132 = 0403
0133 = 0100
0134 = XXX           Exit on Abort
0135 = 3060
0136 = 1210          Check Write Late
```

DAY 7 - Page 2

```
0137 = 0567
0140 = 7705
0142 = 5001          Function Read
0143 = 7405
0144 = 2000
0145 = 0017
0146 = 7205
0147 = 2000
0150 = 3654
0151 = 7205
0152 = 1450
0153 = 7105
0154 = XXXX
0155 = 0403
0156 = 0100
0157 = XXXX          Check for Parity Error or Abort
0160 = 6505
0161 = 0165
0162 = 6705
0163 = 0160
0164 = 7505
```

*Program Note: At this point if you were outputting over forty words you would want to check for A=0 in case of abort.

2. DC Power on and temperature warning light both lite would indicate what condition?

   Answer

   Chassis temperature is between 100 and 110 degrees F

3. What bit positions will the first 12 data bits be loaded into Rank 1?

   Answer

   59 through 48

DAY 7 - Page 3

4. Why does Rank 2 full and byte count = 4 stop the empty signal from being sent to the PP?

   Answer

   It signifies the entire buffer is filled.

5. What condition is necessary for Request ECS on a Read? Why?

   Answer

   Rank 8 Empty. It signifies the buffer will hold an entire ECS record.

6. What conditions are necessary to start the transfer of Rank 9 to the PP? Why?

   Answer

   Rank 9 full and address = XXXXXXX0. This signifies that the entire ECS record requested is in the buffer.

CE SAFETY PRACTICES

All customer engineers are expected to follow reasonable and appropriate precautions with respect to electrical, mechanical, and personal safety hazards while working on computer system equipment. You should pay careful attention to all entries in the maintenance documentation labelled "*DANGER*" or "*WARNING*", which identify hazardous areas or procedures encountered in maintaining the system equipment. The following additional procedures should be followed when working on equipment:

PERSONAL

1. You are responsible for insuring that no action on your part causes unsafe conditions that may expose customer personnel to hazards in any device.

2. You should never work alone on equipment having exposed operating mechanical parts or exposed hazardous power components. If you MUST do so notify your EIC or manager. In any case, the following precautions must be observed:

   a. Someone familiar with the power-off controls must be in the immediate area.

   b. Personal jewelry (rings, wristwatches, bracelets, necklaces, etc.) shall be removed. A small box in the CE tool kit will make a good storage place for these items.

   c. If using one hand, keep the other one in your pocket.

   d. Avoid wearing loose articles of clothing that can be snagged and drawn into moving machinery. Wear short-sleeve shirts or roll sleeves above the elbow. Neckties, where required, should be tucked in between the second and third shirt button or fastened about 3 inches from the end with a tietack or tieclasp, preferably nonconductive. Don't use tiechains. Clipon type neckties are preferable to the regular ones; if caught they will pull free without causing injury.

   e. Before starting equipment, make sure that no other CE or customer personnel are in a position where they could get hurt.

   f. While working in equipment put red tape strips across any power controls, or use "DO NOT OPERATE" tags where available.

3. Keep CE tool kits out of walkways; put them on or under a desk or table.

4. Put doors and covers removed from a machine in a safe, out-of-the-way location where nobody will trip over them or cause them to fall on top of someone. ALL machine covers MUST be restored in place before the machine is returned to the customer.

5. All safety covers, guards, shields, groundstraps, panels, etc. shall be properly reinstalled after maintenance is finished.

6. Maintain good housekeeping practices during and following each maintenance activity. Do not permit tools, manuals, wipers, paper trash and the like to accumulate in the work area, and CLEAN UP AFTER YOURSELF.

ELECTRICAL

1. Remove ALL AC and DC power when removing or installing major assemblies, working inside power supplies or power control enclosures, performing detailed mechanical maintenance procedures,or doing wiring and/or module changes in the machine. If possible, turn off and lock or tag the circuit breaker in the service panel on the wall; unplug the main power supply cord.

2. Use only well-insulated pliers, screwdrivers, test leads, etc. when working on or near live circuits.

3. Do not disconnect or otherwise disable safety grounding systems even if the equipment is powered off. These are installed for YOUR protection.

4. Avoid coming in contact with grounds, such as equipment frames, metal floor tile edgings, electrical conduits, and the like. If possible, locally purchase rubber or vinyl mats.

MECHANICAL

1. Do not use chemicals, greases, oils, or solvents that have not been specifically approved by the equipment manufacturer for that device. His recommendations are usually based on extensive experience with his equipment in service.

2. Use the proper tools for the job. Improper use of tools can result in personal injury or equipment damage.

3. Replace worn or broken tools or test equipment as quickly as possible.

4. If the machine is running, DO NOT reach in to the works; remember, they are YOUR fingers and you only get on set per lifetime.

5. If using a strobelight on mechanical devices, DON'T TOUCH ANYTHING; it may be moving.

6. Safety glasses or goggles must be used if you are:

   a. driving pins, riveting, swedging, and similar activities.

   b. using an electric drill, grinder, reamer, etc.

   c. installing or removing springs under tension or compression.

d. using any type of solvent, spray, or chemical for cleaning or touch-up painting.

e. any other activity which may endanger the eyes. They are YOUR eyes, and you need them for this type of work.

7. When lifting, use a method that will not injure the spine or strain back muscles. Be realistic as to what your capacity for lifting really is.

ABOVE ALL, USE GOOD JUDGEMENT AND COMMON SENSE - A MOMENT OF THOUGHT BEFORE YOU ACT CAN SAVE HOURS OF AGONIZING AFTERTHOUGHT.

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