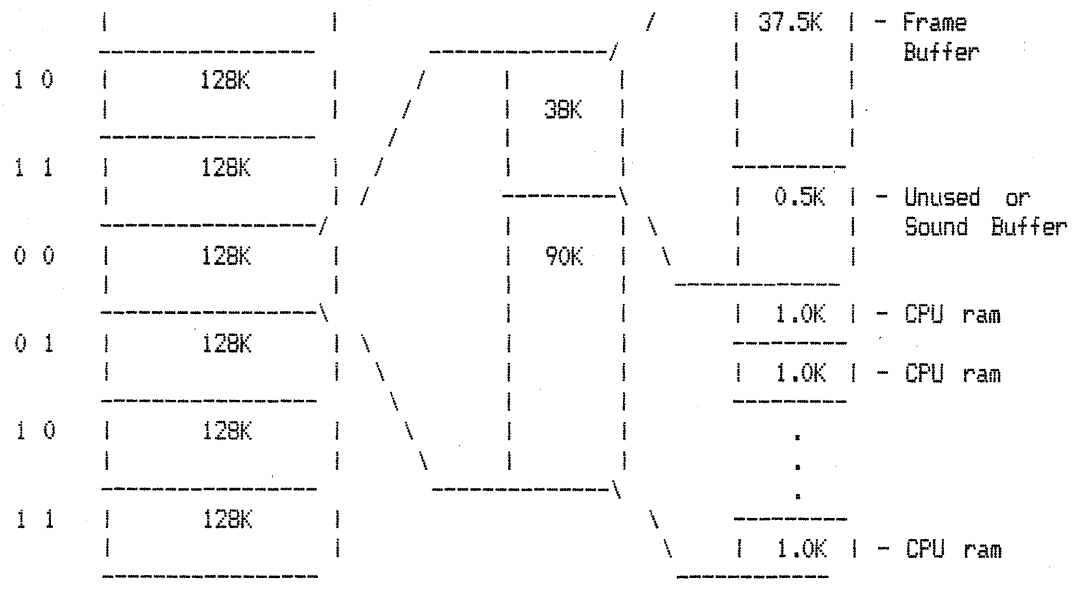
; The YACC is a 1 meg machine with memory management that allows mapping of
; the memory into 1 kilobyte pages. There are 8 video planes which are 640*480
; pixels in size. This is 37.5K of ram per plane; the 1K resolution of the
; pages force an allocation of 38K for each plane. The Video DMA system uses
; physical addresses 19 to 17 for the selection of the 8 planes, thus forcing
; the division of the physical 1 meg of memory into 8 128K partitions. There is
; a 16 bit register that is loaded with a physical address that points to the
; start of the frame buffer in each of the 8 planes.
;
; The Sound subsystem makes all accesses from partition 0, which has addresses
; 17, 18, and 19 = 0. It also has a 16 bit register which points to the start
; of the sound buffer. The system will fetch a 16 bit value at the start of
; video scan line (15.734 KHz horizontal scan rate), of which the low 10 bits
; are used as input to a PWM circuit. The PWM circuit divides the line into 585
; cycles; a value of 585 or higher will turn on the sound for the entire line
; while a value of 0 will turn off the sound for the line. The Sound DMA system
; will continue to fetch successive words of data until a word is read that has
; bit 15 = 1, whereupon the circuit will reset the starting address to the intial
; value in the 16 bit register.
;
; The floppy disk PWM circuit for speed control is two 8 bit registers/counters
; that are written in parallel. When 16 bits are written, the low 8 bits are
; loaded into a PWM_Low register and the high 8 bits are laoded into a PWM_High
; register. The circuit provides Pulse Width Modulation and Pulse Frequency
; Modulation. Each register is fed into a counter that increments at an 8MHz
; rate until it reachs 255, whereupon it halt and reload itself. The other
; register/counter is enabled and it follows an identical process. The number
; of times that both counters increment is proportional to the square-wave
; frequency that is produced. With a sum of counter increments equal to 256,
; a square wave of frequency 31.25Khz is produced (1000/(256*(1000000/8MHz))).
; The value in the PWM_Low register/counter divided by 256 is the proportion
; of the square wave that will be low and the value of PWM_High divided by 256
; is the proportion of time that will square wave will be high.
;
; The memory management hardware consists of 2K x 16 of read/write registers.
; 8 megabytes can be mapped but only 1 megabyte can be mapped at any one time.
; Any 2 accesses that has the low 19 bits the same and the high 3 bits are
; different will cause a memory translation error. To address 1 meg, bits
; 19-10 are provided by the MMU and 9-1 come directly from the address. The
; high 3 bits (22-20) are used by the MMU. To write the MMU, the 16 bits are
; mapped as follows:
;
; Bit 15 - Referenced bit, = 1 if page has been referenced.
; Bit 14 - Modified bit, = 1 if page has been written to.
; Bit 13 - Vaild bit, = 1 if page is mapped to physical address
; Bits 12:03 - Physical address. This is the actual physical address used.
; Bits 02:00 - Tag field. These map the 8 logical meg into 1 physical meg.
;
; There are two maps; 1 is for access in supervisor mode and the 2nd is for
; mapping of user mode accesses.
;
; Below is the actual Physical memory layout of the 1 megabyte of memory,
; along with the chosen mapping of the 128K partitions for the actual locations
; of the Frame Buffer, the Sound Buffer, and CPU ram.
;
; Address
; 19-18-17-16 -- 0
;
; 0 0 0 | 128K |
; | |
; 0 0 1 | 128K |



With memory management, program RAM is mapped from 0 to $B3FFF (8*90*1024). The Video planes are mapped from $B4000 to $FFFFF (8*38*1024). The Sound buffer is mapped from $BD600 to $BD7FF (512), into the unused portion of the first plane of the frame buffer.