

Two circuit boards and a standard software package give iSBC systems a complete Ethernet interface that needs only high level programming

Putting Ethernet onboard the multibus

E thernet has developed rapidly from a concept to a multivendor local area networking system. The system was demonstrated recently at the 1981 National Computer Conference in Chicago, where a yellow Ethernet cable snaking through the Intel, Xerox, and Digital Equipment Corporation booths provided the transmission medium for messages sent around the three locations.

Even before the NCC demonstration, there was great interest in Ethernet local area networks, with several domestic and European companies quietly working on Ethernet based systems. Since that exhibition, interest has grown. That is one reason why Intel has released a single-board Ethernet controller. Another reason is the many systems that are potential sites for Ethernet communications capability. Making Ethernet compatible with the MULTIBUS^R seemed to be the key to broadening the base of local area networking.

Two boards - a processor and a SerDes

The iSBC 550 controller consists of two boards, an 8088 based processor board and a serialization/deserialization board referred to as the "SerDes" board. (See Fig 1.) The processor board contains circuitry for processing, packet buffering, and transferring processed packets to system memory. The SerDes board meets the tricorporate specification for data link control and physical link control. It converts 8-bit parallel data into serial data, frames the messages, computes the cyclic redundancy check polynomial, and determines whether the message received matches the computed value. It also handles the Manchester encoding and decoding of message data, performs destination-address recognition, and takes care of the collision-handling scheme. Like other iSBC boards, the iSBC 550 board pair is built to common dimensions: 12'' (30 cm) wide, 6.75'' (17 cm) high, and 0.5'' (1.3 cm) deep. Board edge connectors are arranged in the standard iSBC layout to make the boards compatible with the MULTIBUS interface.

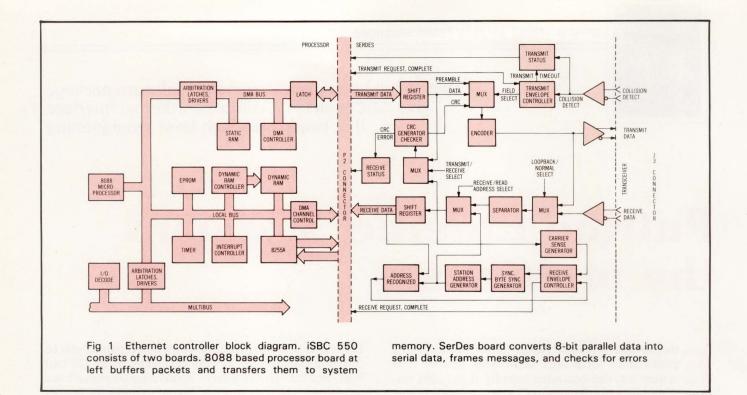
The iSBC 550 processor board contains a 5-MHz version of the 8088 microprocessor, 16k bytes of dynamic random access memory (RAM) dedicated for Ethernet program execution, and 8k bytes of programmable read only memory firmware that supports data link control and the MULTIBUS Interprocessor Protocol (MIP). An additional 8k-byte high speed static RAM is used to buffer transmitted and received data. The processor board provides the necessary commands and control to the SerDes board and receives status and data from it. All data transfers from the Ethernet data link control on the SerDes board are buffered through the 8k bytes of static RAM.

The SerDes board uses small scale integration and medium scale integration logic. It interfaces to the processor board, and through that to the MULTIBUS, but it does not attach directly to the MULTIBUS. The SerDes board accepts transmitted data from the processor board and sends received data to it. In addition, the SerDes board communicates with the processor board using three handshake signals: a "transmit request complete," a "receive request complete," and a "collision detect."

MIP and program interface

The iSBC 550 Ethernet controller contains firmware that supports the MIP interface. The MIP interface defines a pseudo-architecture by which processes executing on different single-board computers can communicate with one another in a reliable, controlled manner. Via MIP, systems consisting of heterogeneous sets of processors running heterogeneous realtime executives and application programs can communicate in a routine fashion.

MIP was created to permit multiple processors residing on the common MULTIBUS to work together



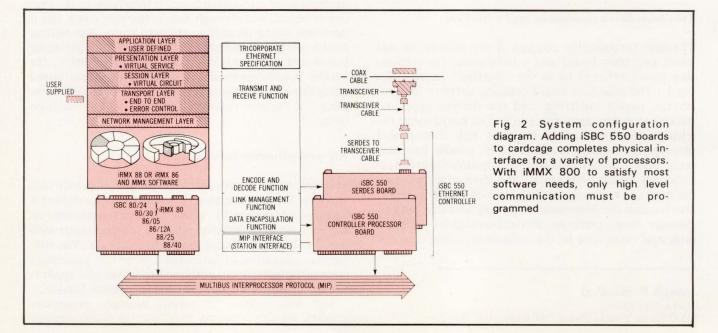
efficiently. A memory based, task-to-task communications protocol, MIP provides loosely-coupled multiprocessing on the MULTIBUS through communications supported by a uniform set of operating system interfaces. MULTIBUS Message Exchange software, iMMX 800, simplifies message transfer across the MULTIBUS. The software supports the addressing, data transfer control, and special memory management services required by such a loosely-coupled multiprocessor arrangement.

System configurations

The iSBC 550 controller and iMMX 800 software package can be used in conjunction with any of the iSBC 80/24,

80/30, 86/05, 86/12A, 88/25, or 88/40 boards to configure systems specialized for 8- or 16-bit processing environments, as well as special numeric processing. (See Fig 2.) Inserting the central processing unit, memory, special options boards, and the iSBC 550 controller into an iSBC cardcage completes the physical interface. Loading an iRMX operating system that includes iMMX 800 software modules satisfies most of the system software requirements. All that remains for the user to develop are four higher levels of communications software, as described in the Ethernet specification.

Ethernet controller firmware consists of commands and data that affect the control of message flow, message type recognition, and multicast addressing. For



Ethernet Local Area Networking

The Ethernet approach to local area networking was described first in the late 1970s, as a culmination of work by Robert Metcalfe and David Boggs at Xerox. A few years later, Intel, Digital Equipment, and Xerox Corp formally agreed to support the concept and jointly issued a set of Ethernet specifications. Published and distributed in September 1980, the Ethernet specification describes specific physical and electrical parameters for the hardware interface of compatible systems. It also describes a layered architecture of functional structures. Only the first two layers, the physical layer and the data link control layer, have been specified in detail. Four remaining, higher layers have not been defined beyond a functional description.

Physically, Ethernet transmits messages serially on 50- Ω coaxial cable. A cable segment can be up to 500 m long and connect up to 100 stations. Each station attaches to the coaxial cable via a transceiver system, through a cable that connects the transceiver to the station and cannot exceed 50 m in length. Messages are formatted into standard frames made up of octets, each 8 bits in length. Framing consists of a destination portion (6 octets), a source portion (6 octets), the message type (2 octets), data (46 to 1500 octets), and a frame check sequence (4 octets). Messages can be addressed to a single station, to all stations (broadcast), or to a number of selected stations (multicast). Signals are transmitted using Manchester encoding, a means of combining separate data and clock signals into a single, selfsynchronizable data stream suitable for transmission on a serial channel.

Message data are transmitted at 10M bits/s. Only one station can transmit at a time. Therefore, Ethernet defines a collision-handling scheme that protects the bus from multiple-station access. Called carrier sense, multiple access with collision detection (CSMA/CD), the scheme ensures detection of multipleaccess situations and aborts multiple-access transmissions. Stations retry at different times to avoid repeated collisions.

Because of the CSMA/CD approach, the bus access method can be strictly first-come, first-served. The advantage of this approach is that each station, through its controller subsystem, shares access to the cable without the need for a separate bus control system. Consequently, the communications network is not vulnerable to catastrophies caused by network control failure. Also, the circuitry is considerably easier to implement. example, two commands control message flow: RECEIVE A MESSAGE and TRANSMIT A MESSAGE. Other commands pertain to network statistic counts, message types to be accepted, and multicast addressing. Firmware recognizes eight message types and up to eight multicast addresses.

Ethernet interface

The Ethernet specification calls out a maximum length for the coaxial cable and transceiver cables. In addition, the specification forces the transceivers to be extremely close (on the order of centimeters) to the coaxial cable to meet the capacitive loading parameters. Physically, the iSBC 550's SerDes board can connect to a supplied 22" (56-cm) cable made up of four twisted pairs of wire. This cable is identical to the Ethernet transceiver cable in its connector, which attaches to the transceiver cable. One twisted pair carries message data to the transceiver, one carries data from the transceiver, one supports the collision detection scheme, and the last pair supplies power to the transceiver.

Messages to be transmitted pass from the iSBC 550 processor board to the SerDes board. After framing and cyclic redundancy check computation, the serialized data are sent via twisted pair to the transceiver. By this time, the data have been Manchester encoded and are converted by the transceiver into electrical signals whose characteristics (rise and fall times, amplitude, etc) are consistent with Ethernet specifications.

Data intended for a particular Ethernet station are received by the transceiver and sent back to the SerDes board for deserialization and transfer to the iSBC 550 processor board. The SerDes board then routes the message to the appropriate process based on the destination address and message-type information sent along with the message.

Conclusion

Putting Ethernet onboard the MULTIBUS was the first step in a cost-effective program that offers the standard Ethernet local area network protocol to original equipment manufacturers and volume end users. Like the iSBC, iRMX, and iMMX products, the iSBC 550 Ethernet controller can serve as a building block that provides a total application solution. Whether that application is prototyped on an Ethernet based Intellec development system or later developed for a component based system, the iSBC 550 offers an easy-to-use cornerstone for Ethernet networking.

About the Author:			
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Harakal holds an MS in computer science from Texas A & M University.	High 734	Average 735	Low 736
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