GAL® Data Book

High Performance E²CMOS® PLDs

1990

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Note: Specifications (t_{PD} and I_{CC}) listed above are for Commercial temperature range devices. See datasheets for Military and Industrial temperature range device specifications.

Introduction to Generic Array Logic

INTRODUCTION

Lattice Semiconductor, located in Hillsboro, Oregon, was founded in 1983 to design, develop and manufacture high-performance semiconductor components. It is a firm belief at Lattice that technological evolution can be accelerated through the continued development of higher-speed and architecturally superior products. This belief led to a decision to enter the programmable logic marketplace by developing the ideal product line: the GAL® (Generic Array Logic) family of devices.

GAL devices are ideal for four important reasons:

1. GAL devices are fabricated using very high-speed Electrically Erasable CMOS (E^2CMOS), which offers the highest degree of testability and quality of any process technology, as well as instant erasability, making GAL devices ideal for prototyping and manufacturing.

2. GAL devices can directly replace PAL devices in nearly every application.

3. GAL devices have the low power consumption of CMOS, one-fourth to one-half that of bipolar devices.

4. GAL devices utilize Output Logic Macrocells (OLMCs), which allow the user to configure outputs as needed.

By melding all these features into a single product line, the GAL family is ideally targeted to replace TTL/74HC random logic, low-density gate arrays, and all other programmable logic. The GAL family offers the benefits of reduced system cost, product size and power requirements, as well as higher reliability and greatly simplified system design.

THE GAL CONCEPT

E^2CMOS — The Ideal Technology

Of the three major technology approaches available E^2CMOS, UVCMOS, and bipolar, the technology of choice is clearly E^2CMOS—for many reasons, including: testability, quality, high speed, low power, and instant erasure for prototyping and error recovery.

Testability

The biggest advantage of E^2CMOS over competing technologies is its inherent testability. Capitalizing on very fast (50ms) erase times, Lattice is able to pattern and erase all devices many times during manufacture, and to directly test all characteristics including AC, DC and functionality. The result is guaranteed 100% programming and functional yields to the customer. Competing technologies suffer serious test constraints, as discussed below.

Low Power

Another advantage of this technology is the low power consumption of CMOS. This provides users the immediate benefit of decreased system power requirements allowing for higher-reliability, cooler-running systems, while maintaining high performance. The low power consumption of CMOS also permits circuit designs of much higher functional density, because of lower junction temperatures and power requirements on chip. The user will benefit because higher functional density means further reduction of chip count and smaller boards in the system.

High Speed

Also advantageous is the very high speed attainable with Lattice's state-of-the-art E^2CMOS process — the speeds available are comparable to bipolar, and faster than other CMOS processes.

Prototyping and Error Recovery

Finally, E^2CMOS gives the user instant erasability, with no additional handling, or special packages necessary. This provides ideal products for prototyping because designs can be altered instantly, with no waste and no waiting. On the manufacturing floor, instant erasability can also be a big advantage for dealing with pattern changes or error recovery. If a GAL device is accidentally programmed to the wrong pattern, the recovery process is simple, again with no waiting or waste. Parts are simply put back into a device programmer and repatterned. No other technology can offer this.

A LOOK AT OTHER TECHNOLOGIES

Here, the technologies that compete with E²CMOS—bipolar and UVCMOS—are compared and contrasted with the E²CMOS approach.

Bipolar

Bipolar fuse-link technology was the first available for programmable logic devices. Although it offers high speed, it is saddled with high power dissipation. This not only significantly increases system power supply and cooling requirements it also limits the ability of high functional density.

Another weakness of this technology is the one-time-programmable fuses. Complete testing is impossible and manufacturers must rely on complex schemes using test rows and columns to simulate and correlate their device's performance, since the fuse array cannot be tested prior to programming. The result is programming failures at the customer location, due to incomplete testing. Also, because these devices can only be programmed once, no reuse in the event of mistakes during prototyping or errors on the production floor are possible and any misprogrammed devices must be discarded.

UVCMOS

UVCMOS addresses many of the weaknesses of the bipolar approach, but introduces many shortcomings of its own. This technology requires much lower power and, while it has the capability to erase, this comes at the expense of slower speeds.

Testability is increased over bipolar since the "fuse" array can be programmed and tested by the manufacturer. The problem here is the long (20 minutes) erase times of this technology, coupled with the requirement of exposing the devices to ultraviolet light for erasing. This becomes a very expensive step in the manufacturing process. Because of the time involved, patterning and erasing is performed only once—a compromised, rather than complete functional test.

Additionally, the devices must be housed in expensive windowed packages to allow users to erase them. Again, this erase is coupled with the time-consuming and cumbersome task of shining ultraviolet light on the parts to erase them. As a cost-cutting measure, UVCMOS PLD manufacturers offer their devices in windowless packages, which cannot be completely tested after packaging, since they cannot be erased. Of course, the user cannot erase them either. These factors significantly detract from the desirability of this technology.

THE GAL ADVANTAGE

GAL devices are ideal programmable logic devices because, as the name implies, they are architecturally generic. Lattice has employed the macrocell approach, which allows users to define the architecture and functionality of each output. The key benefit to the user is the freedom from being tied to any specific architecture. This is advantageous at the manufacturing level, as well as the design level.

Design Advantages

Early programmable logic devices gave the user the ability to specify a function, but limited them to specific, predetermined output architectures. Comparing the GAL device with fixed-architecture programmable logic devices is much like comparing these same fixed PLDs with SSI/MSI devices. The GAL family is the next generation in simplified system design. The user need not bother searching for the architecture that best suits a particular design. Instead, the GAL family's generic architecture lets him configure as he goes.

Manufacturing Advantages

The one-device-does-all approach greatly simplifies manufacturing flow. Inventorying one generic-architecture GAL device type versus having to monitor and maintain many different device types, each with its own architecture, will not only save money but will minimize the paperwork and headaches associated with the latter approach. Manufacturing flow is much smoother, too, because the handling process is greatly simplified. A generic-architecture GAL device also reduces the risk of running out of inventory and halting production, which can be a very expensive nightmare. Reduced chance of obsolete inventory and also easier QA tracking are additional benefits of the generic architecture.

THE IDEAL PACKAGE

Programmable logic devices are ideal for designing today's systems. Lattice Semiconductor believes that the ideal design approach should be supported with the ideal products. It was on this premise that GAL devices were invented. The ideal device—with a generic architecture—fabricated with the ideal process technology, E²CMOS.

Lattice will continue to develop and expand its line of E²CMOS programmable logic devices, bringing higher speeds, more flexibility, and exciting new capabilities such as in-system programmability with our ispGAL® family. This is the Lattice Commitment to programmable logic and to you, our customer.

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DEFINITION OF DATASHEET LEVELS

Datasheet Identification	Product Status	Definition
Advanced	In Design	This datasheet contains advance information and specifications which are subject to change without notice.
Preliminary	Sampling or Pre-Production	This datasheet contains preliminary data and supplementary data will be published at a later date. Lattice reserves the right to make changes at any time without notice.
No Identification	Full Production	This datasheet contains final specifications. Lattice reserves the right to make changes at any time without notice.

Lattice Semiconductor Corporation™

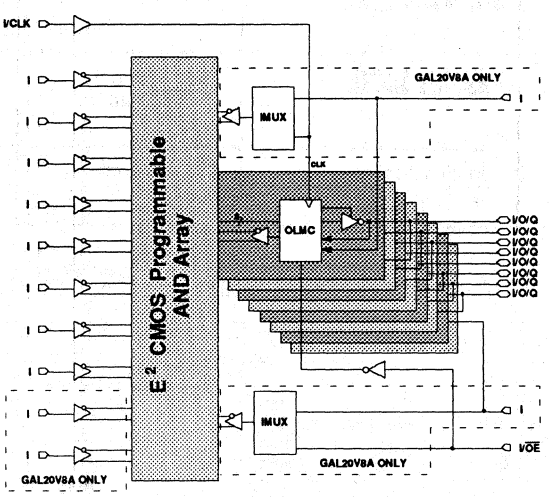
GAL16V8A
GAL20V8A

High Performance E²CMOS® Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS TECHNOLOGY**
  - 10 ns Maximum Propagation Delay
  - Fmax = 62.5 MHz
  - 7 ns Maximum from Clock Input to Data Output
  - TTL Compatible 24 mA Outputs
  - UltraMOS® III Advanced CMOS Technology
- **50% REDUCTION IN POWER**
  - 75mA Typ I_{CC}
- **E² CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/Guaranteed 100% Yields
  - High Speed Electrical Erasure (<50ms)
  - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - GAL16V8A Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
  - GAL20V8A Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

GAL16V8A / GAL20V8A BLOCK DIAGRAM



DESCRIPTION

The GAL16V8A and GAL20V8A, at 10 ns maximum propagation delay time, combine a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest speed performance available in the PLD market. CMOS circuitry allows the GAL16V8A and GAL20V8A to consume just 75mA typical I_{CC} which represents a 50% savings in power when compared to their bipolar counterparts. The E^2 technology offers high speed (50ms) erase times, providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL16V8A and GAL20V8A are capable of emulating standard 20 and 24-pin PAL® devices. The GAL16V8A is capable of emulating standard 20-pin PAL architectures with full function/fuse map/parametric compatibility. The GAL20V8A is capable of emulating standard 24-pin PAL architectures with full function/fuse map/parametric compatibility. On the right is a table listing the PAL architectures that the GAL16V8A and GAL20V8A can replace.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

GAL16V8A / GAL20V8A ARCHITECTURE EMULATION

GAL20V8A PAL Architecture Emulation	GAL16V8A PAL Architecture Emulation
20L8	16L8
20H8	16H8
20R8	16R8
20R6	16R6
20R4	16R4
20P8	16P8
20RP8	16RP8
20RP6	16RP6
20RP4	16RP4
14L8	10L8
16L6	12L6
18L4	14L4
20L2	16L2
14H8	10H8
16H6	12H6
18H4	14H4
20H2	16H2
14P8	10P8
16P6	12P6
18P4	14P4
20P2	16P2

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ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

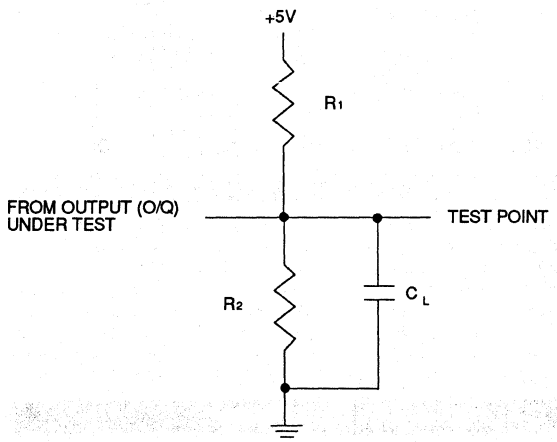
COMMERCIAL		INDUSTRIAL		MILITARY	
R_1	R_2	R_1	R_2	R_1	R_2
200	390	200	390	390	750

AC Test Conditions:

Cond. 1) R_1 per table; C_L = 50pF; R_2 per above table

Cond. 2) Active High R_1 = ∞; Active Low R_1 per table; C_L = 50pF; R_2 per above table

Cond. 3) Active High R_1 = ∞; Active Low R_1 per table; C_L = 5pF; R_2 per above table



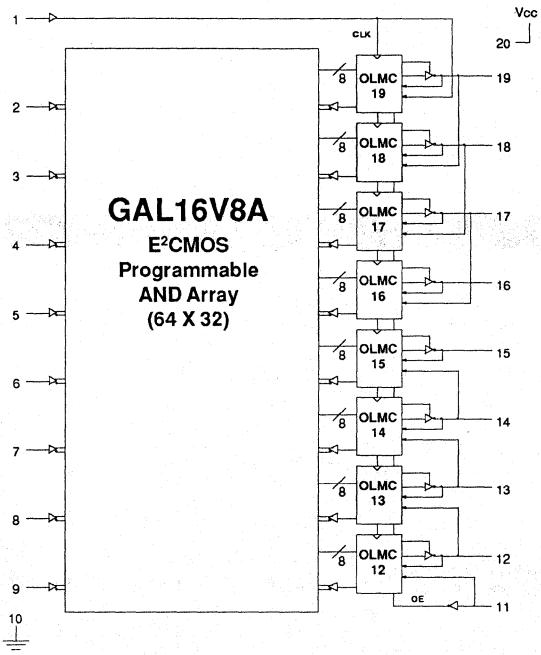
CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

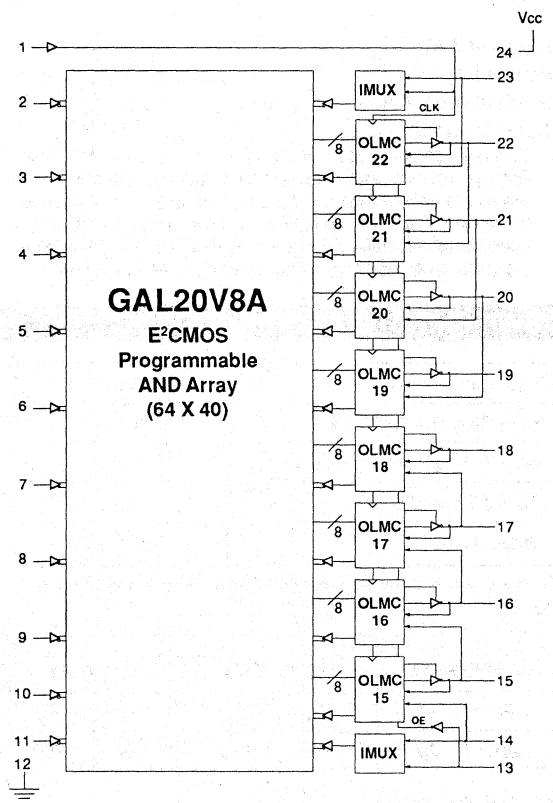
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

GAL16V8A BLOCK DIAGRAM

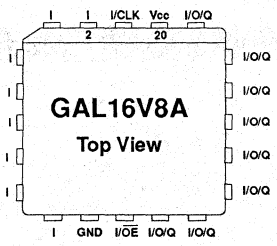


GAL20V8A BLOCK DIAGRAM

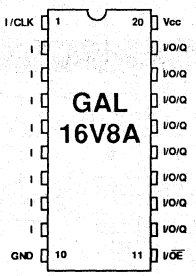


GAL16V8A PIN DIAGRAM

Chip Carrier

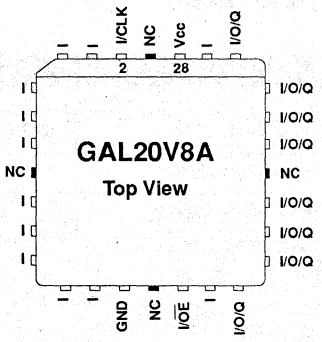


DIP

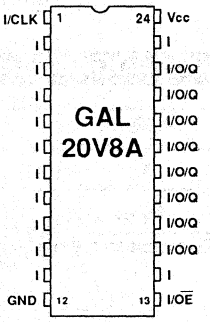


GAL20V8A PIN DIAGRAM

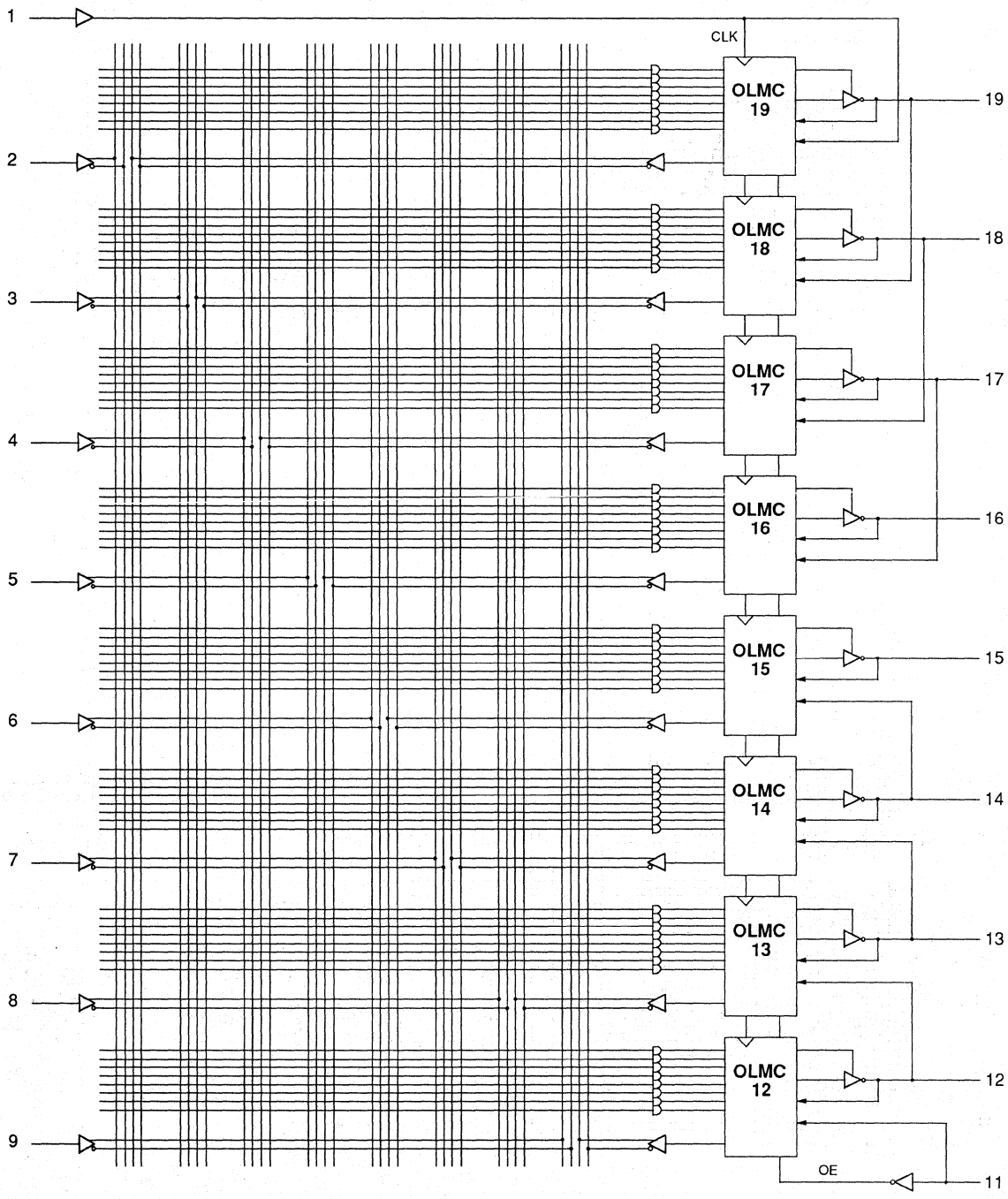
Chip Carrier



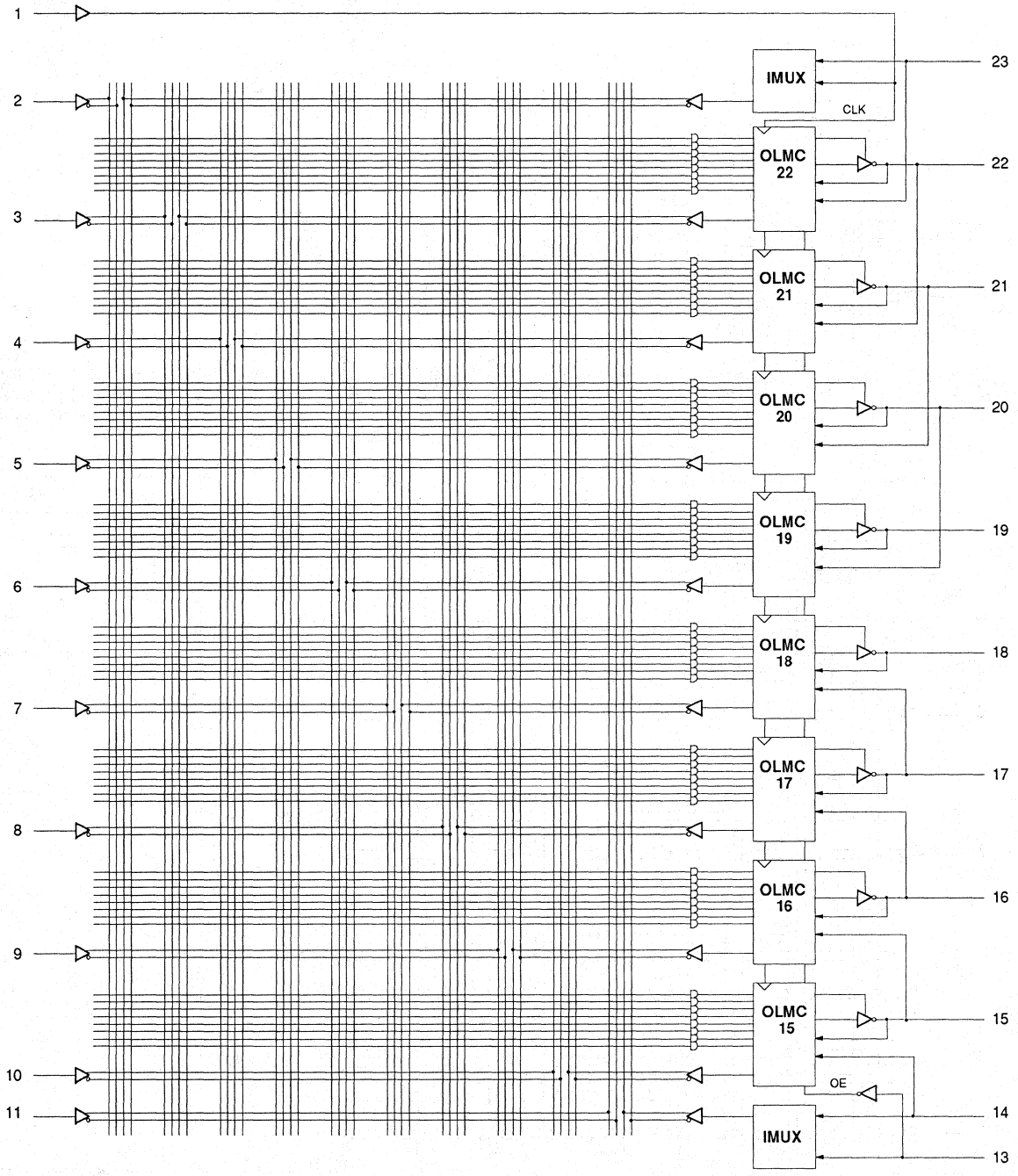
DIP



GAL16V8A LOGIC DIAGRAM



GAL20V8A LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-10L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	115	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-10L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-10L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	10	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	7	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	10	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	10	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	10	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	10	ns

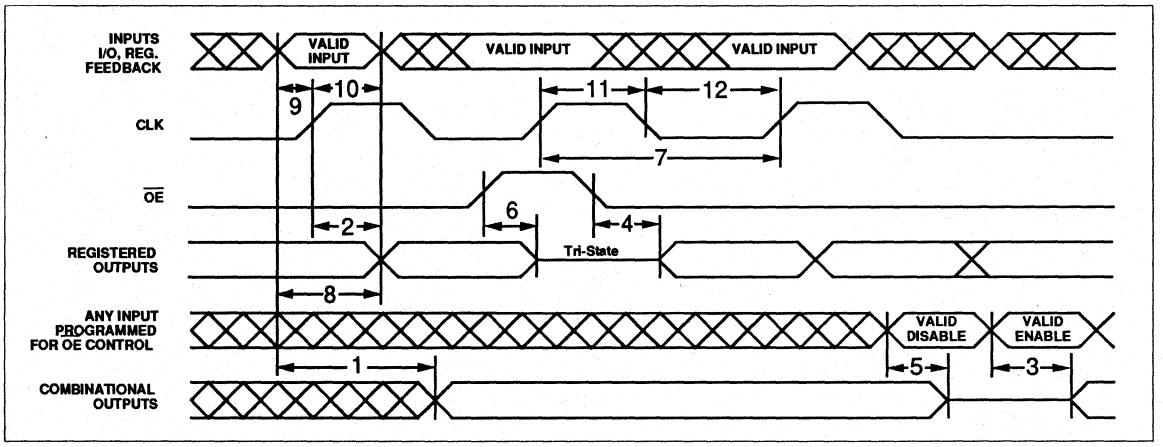
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-10L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	62.5	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	58.8	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	10	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	8	—	ns
	12	Clock Pulse Duration, Low[2]	—	8	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-15L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	115	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-15L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	10	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

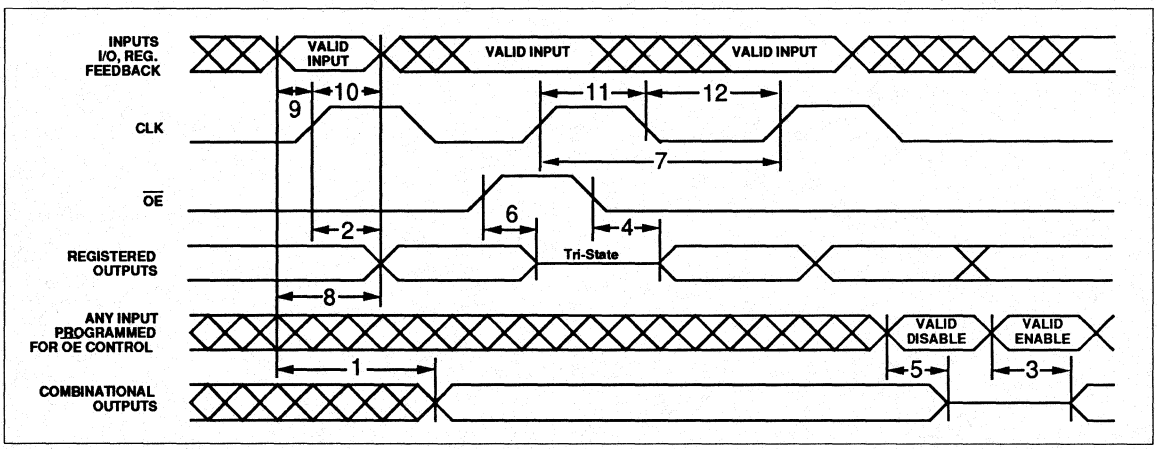
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	62.5	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	45.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	8	—	ns
	12	Clock Pulse Duration, Low[2]	—	8	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-15Q Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	45	55	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15Q Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-15Q Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	10	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

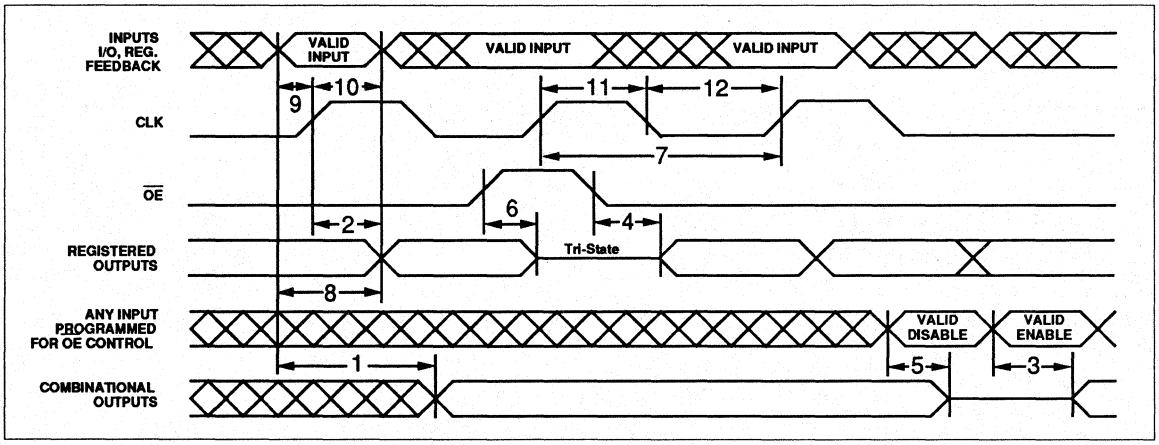
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15Q Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	62.5	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	45.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	8	—	ns
	12	Clock Pulse Duration, Low[2]	—	8	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-25L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	115	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-25L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-25L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	12	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

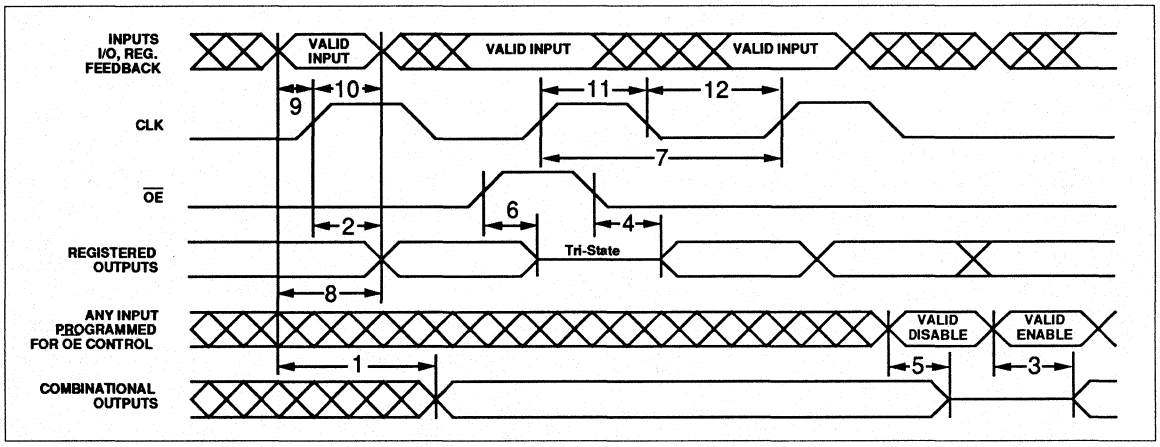
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-25L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	41.7	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	37	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	12	—	ns
	12	Clock Pulse Duration, Low[2]	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-25Q Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	45	55	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-25Q Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-25Q Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	12	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

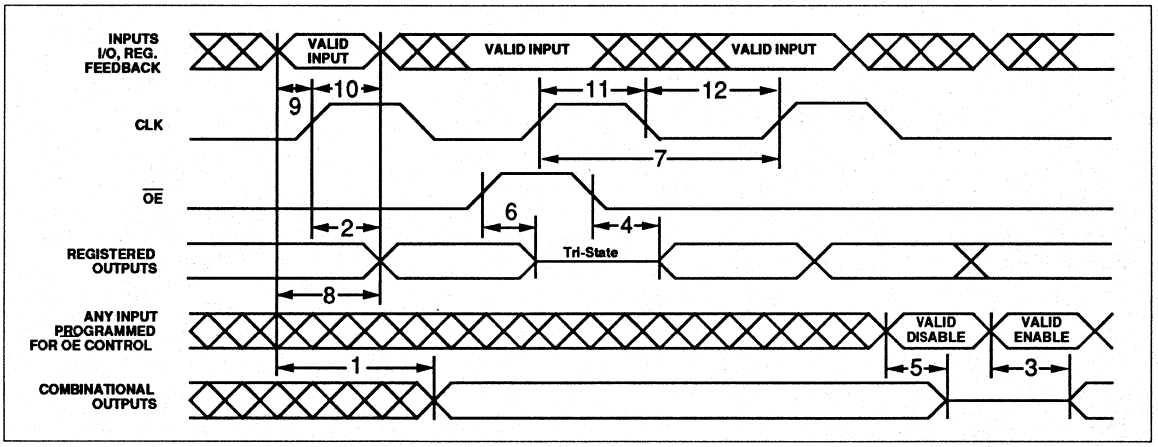
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-25Q Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	41.7	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	37	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	12	—	ns
	12	Clock Pulse Duration, Low[2]	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-15L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	- 40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-15L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	12	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

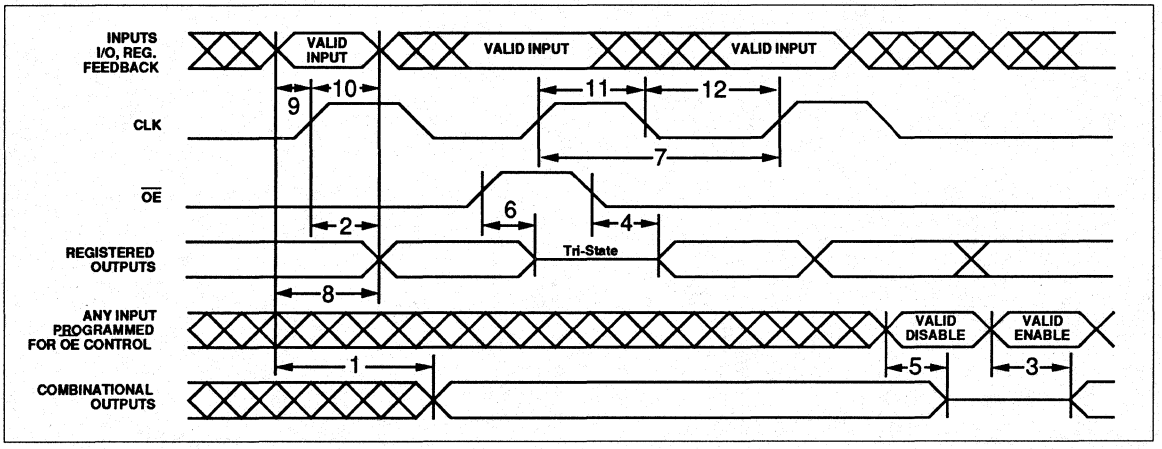
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	50	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	41.6	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	10	—	ns
	12	Clock Pulse Duration, Low[2]	—	10	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-20L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	-30	—	-150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	- 40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	-3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-20L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

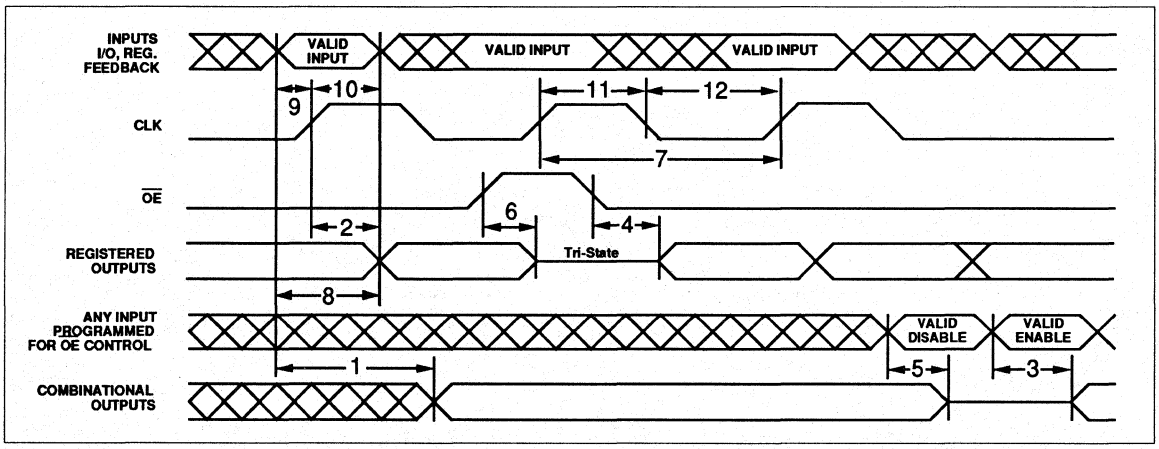
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = 1 / (t_{wh} + t_{wl})	1	0	41.7	MHz
	8	Clock Frequency with Feedback[1] = 1 / (t_{su} + t_{co})	1	0	33.3	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	12	—	ns
	12	Clock Pulse Duration, Low[2]	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-20Q Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	45	65	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20Q Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	- 40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-20Q Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

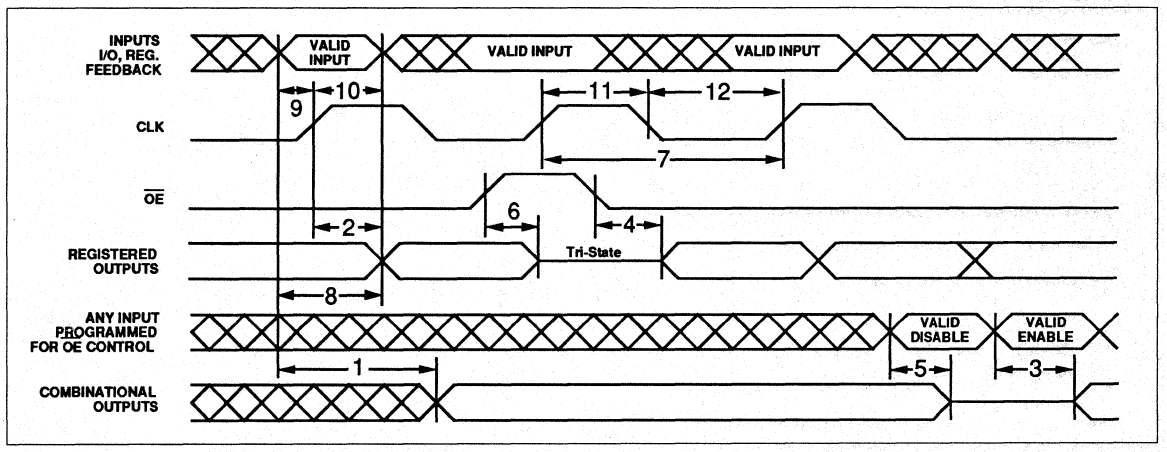
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20Q Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = 1 / (t_{wh} + t_{wl})	1	0	41.7	MHz
	8	Clock Frequency with Feedback[1] = 1 / (t_{su} + t_{co})	1	0	33.3	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	12	—	ns
	12	Clock Pulse Duration, Low[2]	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-25L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-25L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	- 40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-25L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

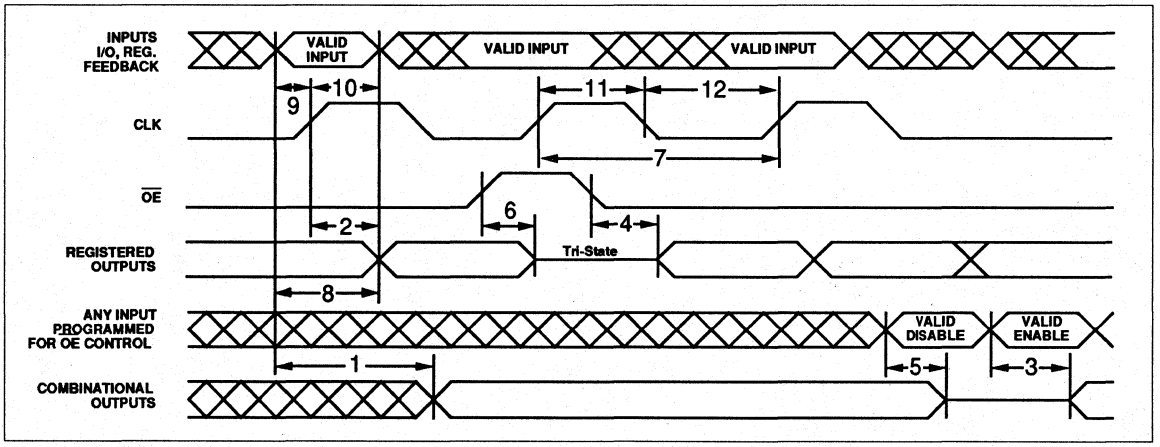
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-25L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	33.3	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	28.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	20	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	15	—	ns
	12	Clock Pulse Duration, Low[2]	—	15	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-15L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	– 55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	12	mA
I_{OH}	High Level Output Current	—	– 2.0	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-15L Military

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	12	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

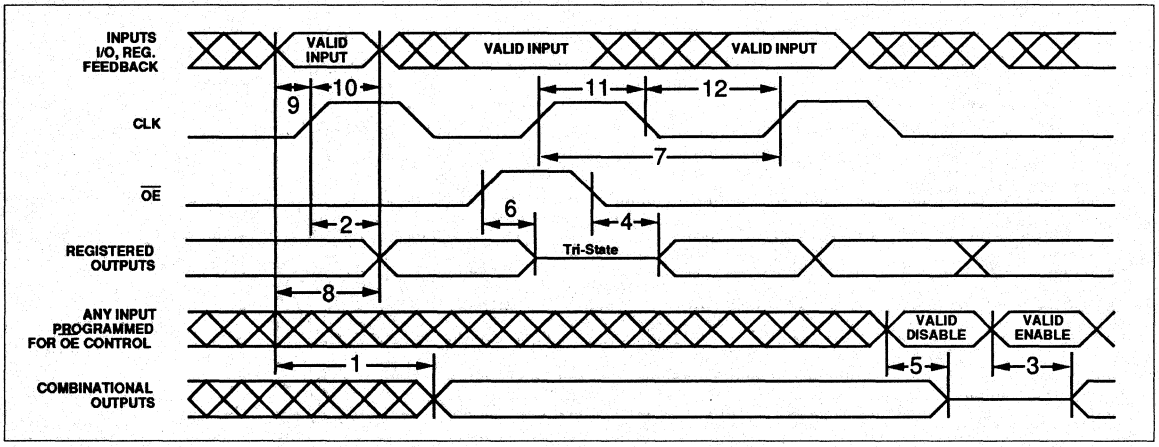
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	50	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	41.6	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	10	—	ns
	12	Clock Pulse Duration, Low[2]	—	10	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-20L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	–55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	12	mA
I_{OH}	High Level Output Current	—	–2.0	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-20L Military

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

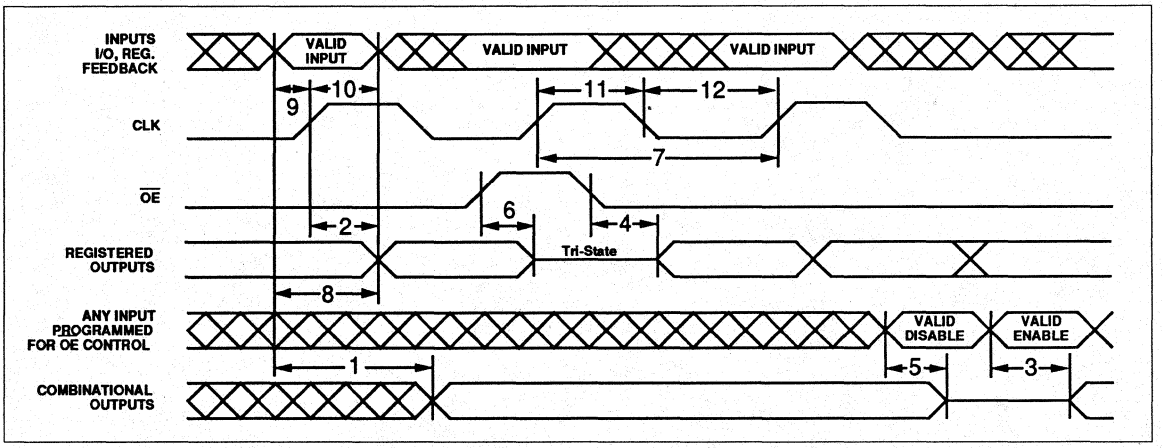
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	41.7	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	33.3	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	12	—	ns
	12	Clock Pulse Duration, Low[2]	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-20Q Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	45	65	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20Q Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	–55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	12	mA
I_{OH}	High Level Output Current	—	–2.0	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-20Q Military

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

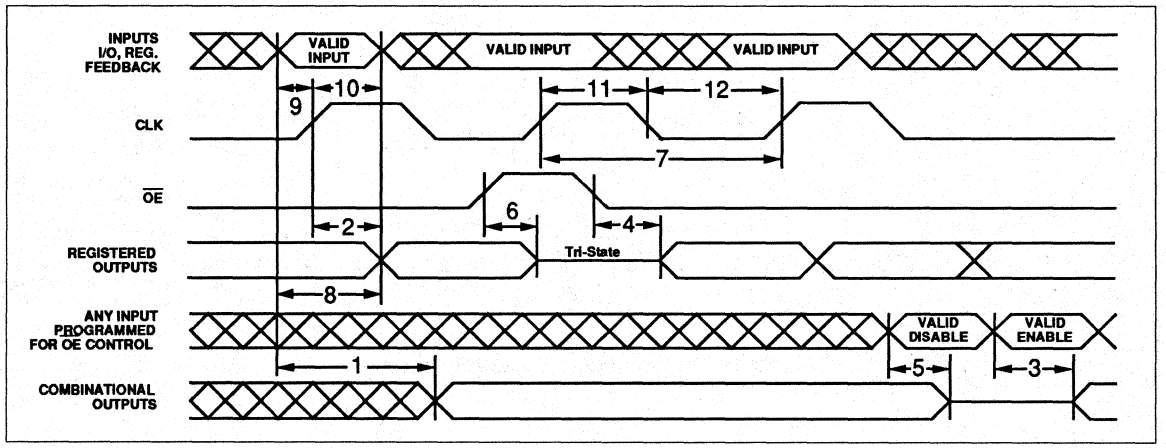
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20Q Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	41.7	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	33.3	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	12	—	ns
	12	Clock Pulse Duration, Low[2]	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



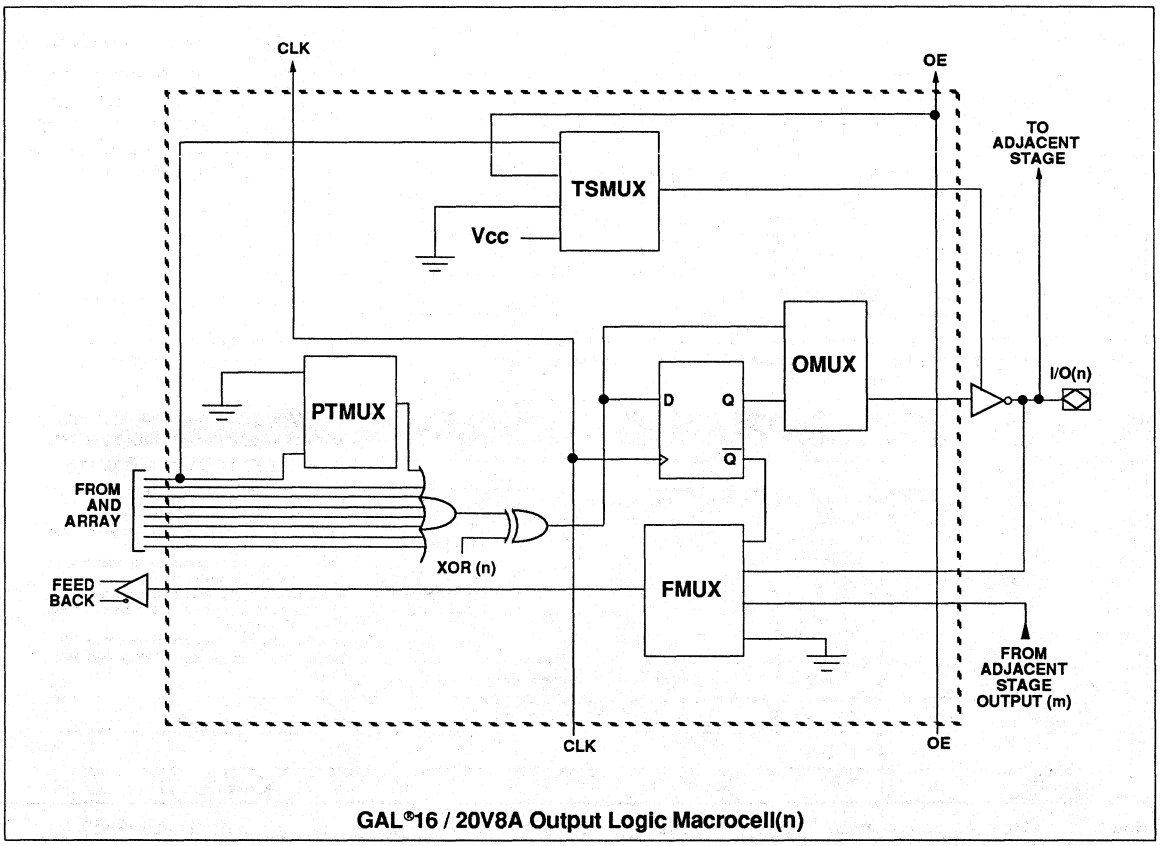
OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three OLMC configuration modes possible: registered, complex, and simple. These are illustrated in the diagrams on the following pages. You cannot mix modes, either all OLMCs are simple, complex, or registered (in registered mode the output can be combinational or registered).

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable is connected to all registered outputs; or a product term can be used to provide individual output enable control for combinational outputs in the registered mode or combinational outputs in the complex mode. There is no output enable control in the small mode. The output logic macrocell provides the designer with maximum output flexibility in matching signal requirements, thus providing more functionality than possible with existing 20 and 24-pin PAL® devices.

The six valid macrocell configurations, two configurations per mode, are shown in each of the macrocell equivalent diagrams. Pin and macrocell functions are detailed in the following diagrams.



GAL®16 / 20V8A Output Logic Macrocell(n)

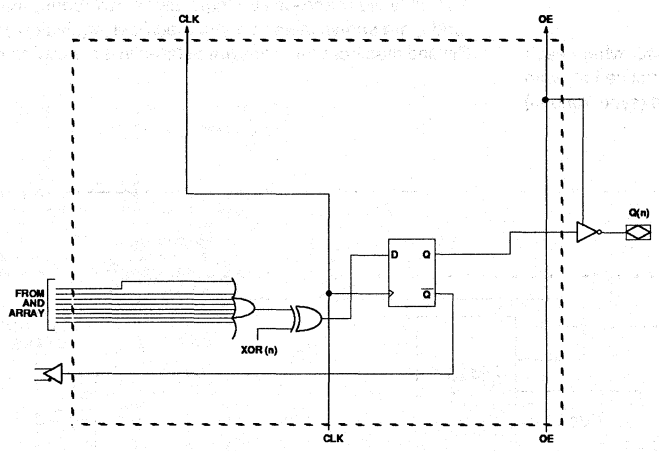
REGISTERED MODE

In the Registered architecture mode macrocells are configured as dedicated, registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8, 20R6 and 16RP4 devices with various permutations of polarity, I/O and register placement.

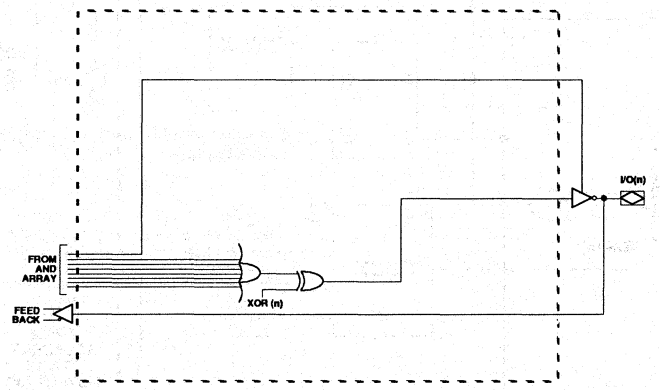
All registered macrocells share common clock and $\overline{OE}$ control pins. Any macrocell can be configured as registered or I/O. Up to 8 registers or up to 8 I/O's are possible in this mode. Dedicated input or output functions can be implemented as sub-sets of the I/O function.

Registered outputs have 8 data product terms per output, I/O's have 7 data product terms per output.



Registered Output with Programmable Polarity

NOTES:
- All macrocells can be individually configured to this function.
- Polarity of the register input is programmable on a macrocell by macrocell basis.
- Feedback into the AND array is from the $\overline{Q}$ signal of the register with active low and active high feedback paths provided.
- Registered macrocells have common clock (pin 1) and common $\overline{OE}$ (16V8 pin 11, 20V8 pin 13)



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- All macrocells can be individually configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- All macrocells have active high and active low feedback of the output buffer and/or device pin data into the AND array.
- When all 8 macrocells are configured into the I/O function the CLK and $\overline{OE}$ pins serve no valid logic function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

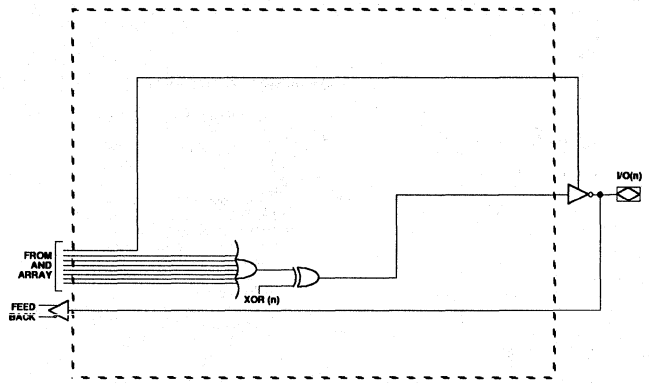
COMPLEX MODE

In the Complex architecture mode macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8, 20L8 and 16P8 devices with programmable polarity in each macrocell.

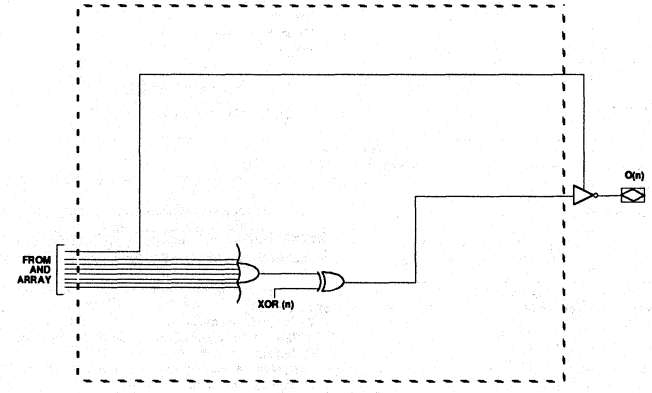
Up to 6 I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as sub-sets of the I/O function. The two "outboard" macrocells do not have input capability. Designs requiring 8 I/O's can be implemented in the Registered mode.

All macrocells have 7 data product terms per output. One product term is used for programmable OE control. Pins 1 and 11 on a GAL16V8A, and pins 1 and 13 on a GAL20V8A, are always available as data inputs into the AND array.



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- The outer most macrocells (16V8 pins 12 & 19, 20V8 pins 15 & 22) cannot perform this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- Each macrocell has active high and active low feedback of the output buffer and/or device pin data into the AND array.



Combinational Output with Programmable OE and Polarity

NOTES:
- The two outer most macrocells (16V8 pins 12 & 19, 20V8 pins 15 & 22) are permanently configured to this function when in the Complex mode.
- The other 6 macrocells can emulate this mode by not using the feedback data as a data input to the array.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

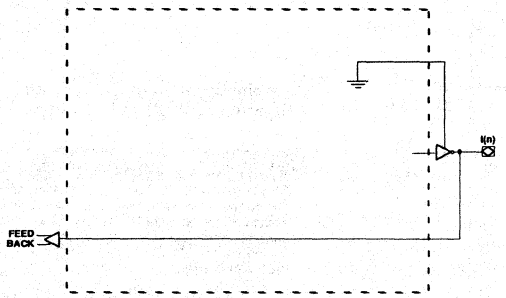
SIMPLE MODE

In the Simple architecture mode pins are configured as dedicated inputs or as dedicated, always active, combinational outputs.

Architecture configurations available in this mode are similar to the common 10L8, 18H4 and 16P6 devices with many permutations of generic polarity output or input choices.

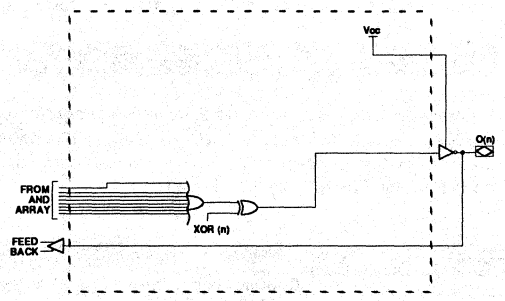
All ouputs are associated with 8 data product terms. In addition, each output has programmable polarity.

Pins 1 and 11 on a GAL16V8A, and pins 1 and 13 on a GAL20V8, are always available as data inputs into the AND array. The "center" two macrocells (GAL16V8A pins 15 &16, GAL20V8A pins 18 & 19) cannot be used in the input configuration.



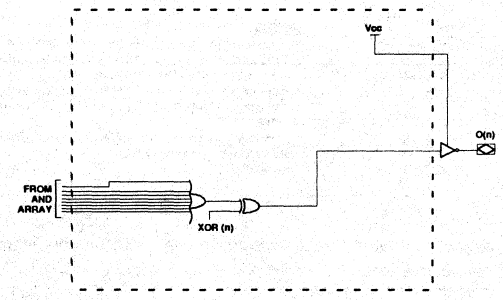
Dedicated Input Mode

NOTES:
- The "center" two macrocells (16V8A pins 15 & 16, 20V8A pins 18 & 19) cannot be configured to this function.



Dedicated Combinational Output with Feedback and Programmable Polarity

NOTES:
- The "center" two macrocells (16V8A pins 15 & 16, 20V8A pins 18 & 19) cannot be configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.



Dedicated Combinational Output with Programmable Polarity

NOTES:
- The "center" two macrocells (16V8A pins 15 & 16, 20V8A pins 18 & 19) are permanently configured to this function when in the Simple mode.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL16V8A and GAL20V8A device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL16V8A and GAL20V8A device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

INPUT BUFFERS

GAL16V8A and GAL20V8A devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL16V8A and GAL20V8A devices do not possess active pullups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

GAL16V8A and GAL20V8A devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

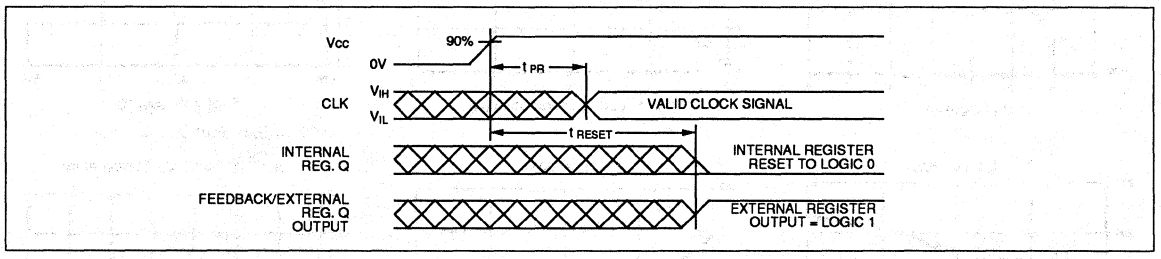
LATCH-UP PROTECTION

GAL16V8A and GAL20V8A devices are designed with an onboard charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-up instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

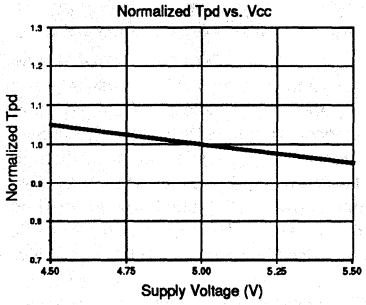
POWER-UP RESET



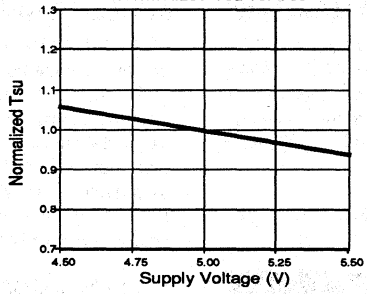
Circuitry within the GAL16V8A and GAL20V8A provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL16V8A and GAL20V8A. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

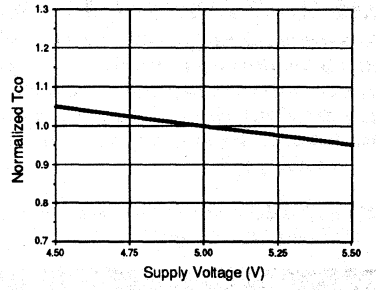
Normalized Tpd vs. Vcc



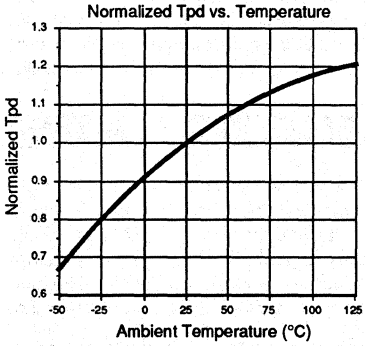
Normalized Tsu vs. Vcc



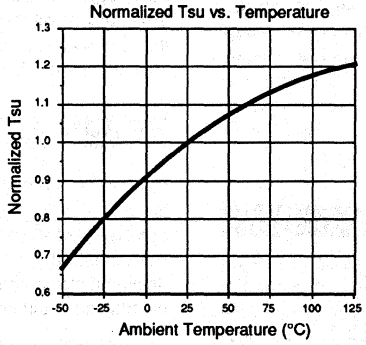
Normalized Tco vs. Vcc



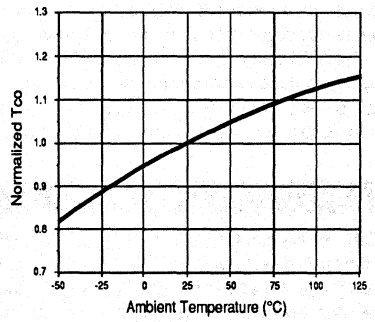
Normalized Tpd vs. Temperature



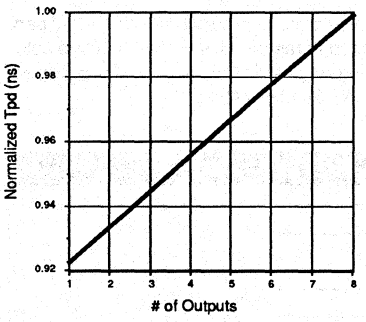
Normalized Tsu vs. Temperature



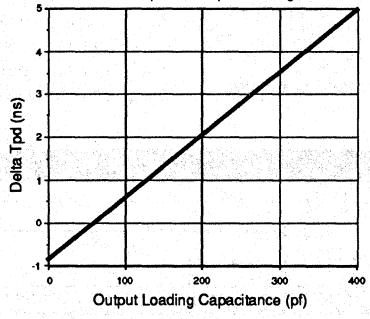
Normalized Tco vs. Temperature



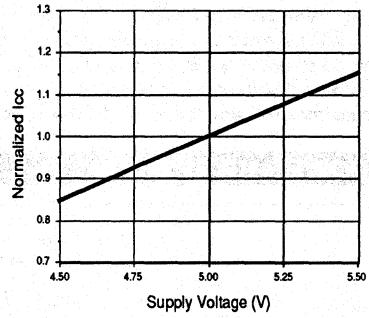
Normalized Tpd vs. # of Outputs Switching



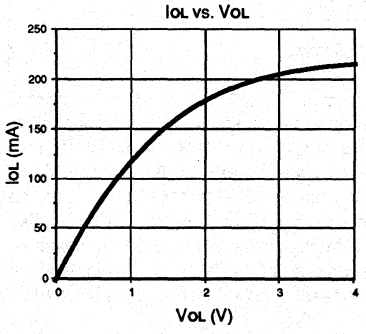
Delta Tpd vs. Output Loading



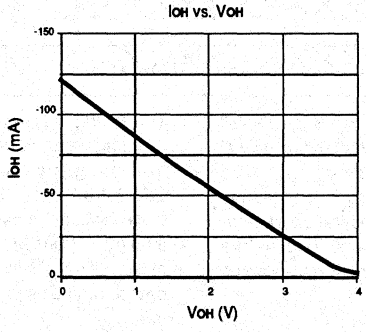
Normalized Icc vs. Vcc



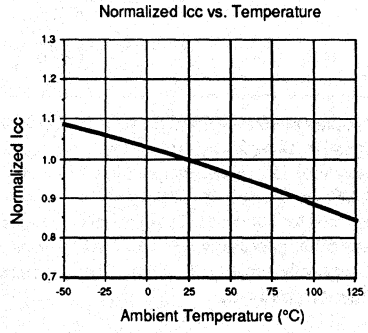
I_{OL} vs. V_{OL}



I_{OH} vs. V_{OH}



Normalized Icc vs. Temperature



GAL22V10 Family

GAL18V10
GAL22V10
GAL26CV12

High-Performance E²CMOS®

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **15 ns Maximum Propagation Delay**
  - **Fmax = 50 MHz**
  - **TTL Compatible 8 - 16 mA Outputs**
  - **UltraMOS® III Advanced CMOS Technology**
  - **Internal Pull-Up Resistor on all Pins**
- **50% REDUCTION IN POWER**
  - **75 - 90mA Typ I_{CC}**
- **E² CELL TECHNOLOGY**
  - **Reconfigurable Logic**
  - **Reprogrammable Cells**
  - **100% Tested/Guaranteed 100% Yields**
  - **High Speed Electrical Erasure (<50ms)**
  - **20 Year Data Retention**
- **OUTPUT LOGIC MACROCELLS**
  - **Maximum Flexibility for Complex Logic Designs**
  - **Uses the Standard 22V10 OLMC Architecture**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **DMA Control**
  - **State Machine Control**
  - **High Speed Graphics Processing**
  - **Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

DESCRIPTION

The GAL22V10 Family of devices are high-speed, E²CMOS® PLDs built using the familiar 22V10 architecture. Three devices are offered in the GAL22V10 Family. They are the GAL18V10 (20-pin), GAL22V10 (24-pin), and the GAL26CV12 (28-pin). Each of these devices uses the industry standard 22V10 universal architecture which provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The devices differ in the number of I/Os, Pins, and Product Terms offered.

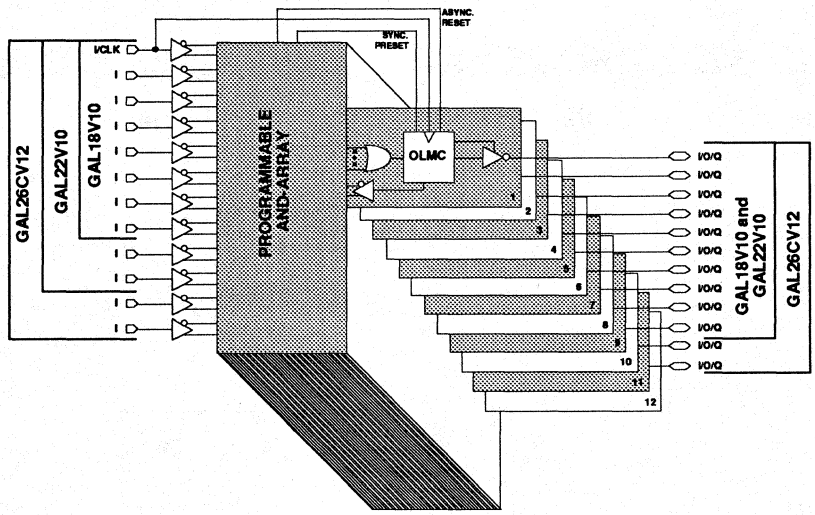
The GAL22V10 is a 24-pin device which contains twelve (12) dedicated input pins and ten (10) input/output pins. The device has a variable number of product terms per OLMC, ranging from eight (8) to sixteen (16) per output.

The GAL18V10 is a 20-pin version of the popular 22V10 device. The GAL18V10 provides design engineers with a smaller footprint and lower cost alternative to the 24-pin 22V10 device. The GAL18V10 contains eight (8) dedicated input pins and ten (10) input/output pins.

The GAL26CV12 is a 28-pin version of the 22V10 device. The GAL26CV12 features more inputs and outputs in order to provide greater functionality and increased I/O. The GAL26CV12 contains fourteen (14) dedicated input pins and twelve (12) input/output pins.

Electrically reprogrammable CMOS technology allows complete AC, DC, and functional testing of every GAL device. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

BLOCK DIAGRAM: GAL18V10, 22V10, and 26CV12



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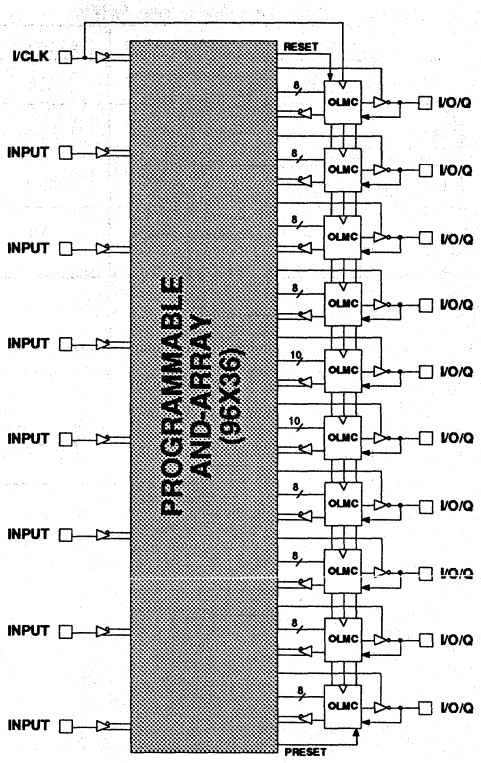
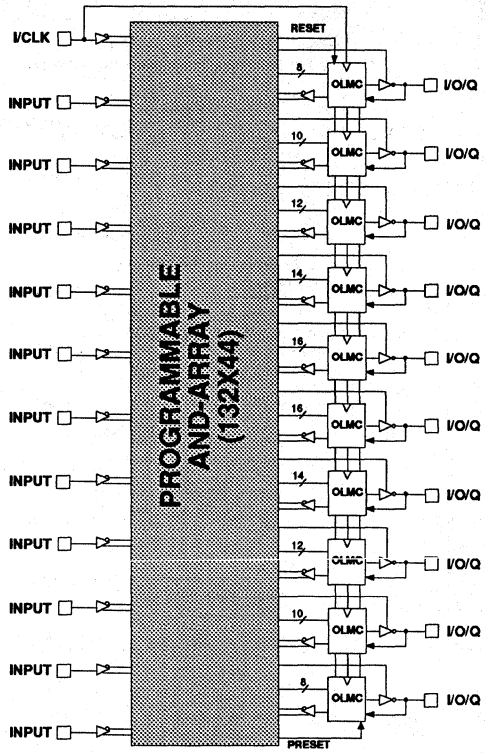
LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124 U.S.A.
Tel. (503) 681-0118 or 1-800-FASTGAL; FAX (503) 681-3037

March 1990

GAL18V10 BLOCK DIAGRAM

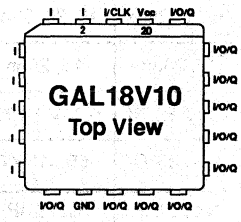


GAL22V10 BLOCK DIAGRAM

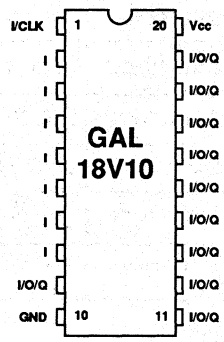


GAL18V10 PIN DIAGRAMS

Chip Carrier

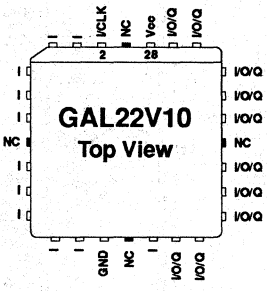


Skinny Dip

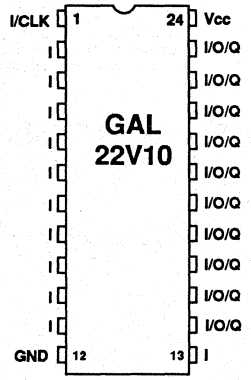


GAL22V10 PIN DIAGRAMS

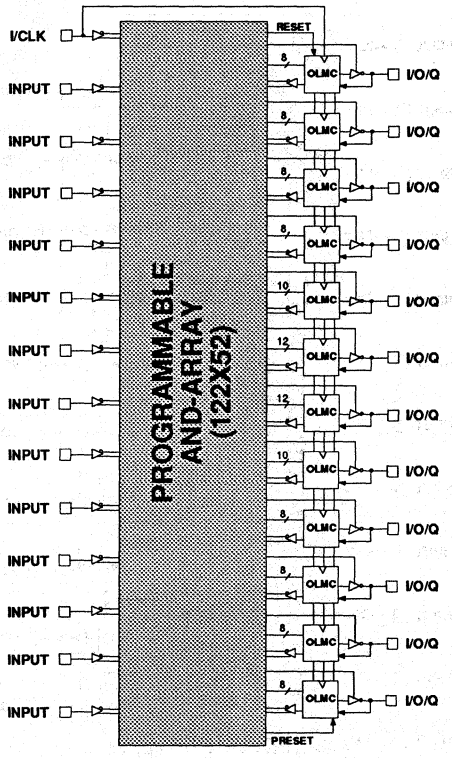
Chip Carrier



Skinny Dip



GAL26CV12 BLOCK DIAGRAM

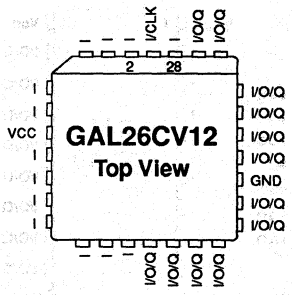


PRODUCT SELECTOR GUIDE

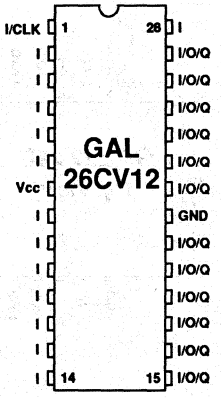
	COMMERCIAL TEMP.		
	GAL18V10	**GAL22V10**	**GAL26CV12**
Pins	20	24	28
Tpd (Max.)	15ns	15ns	15ns
Icc (Typ.)	75mA	90mA	90mA
Dedicated Inputs	8	12	14
Inputs/ Outputs	10	10	12
Product Terms per macrocell	8-12	8-16	8-10
Technology	E²CMOS	E²CMOS	E²CMOS

GAL26CV12 PIN DIAGRAMS

Chip Carrier



Skinny Dip

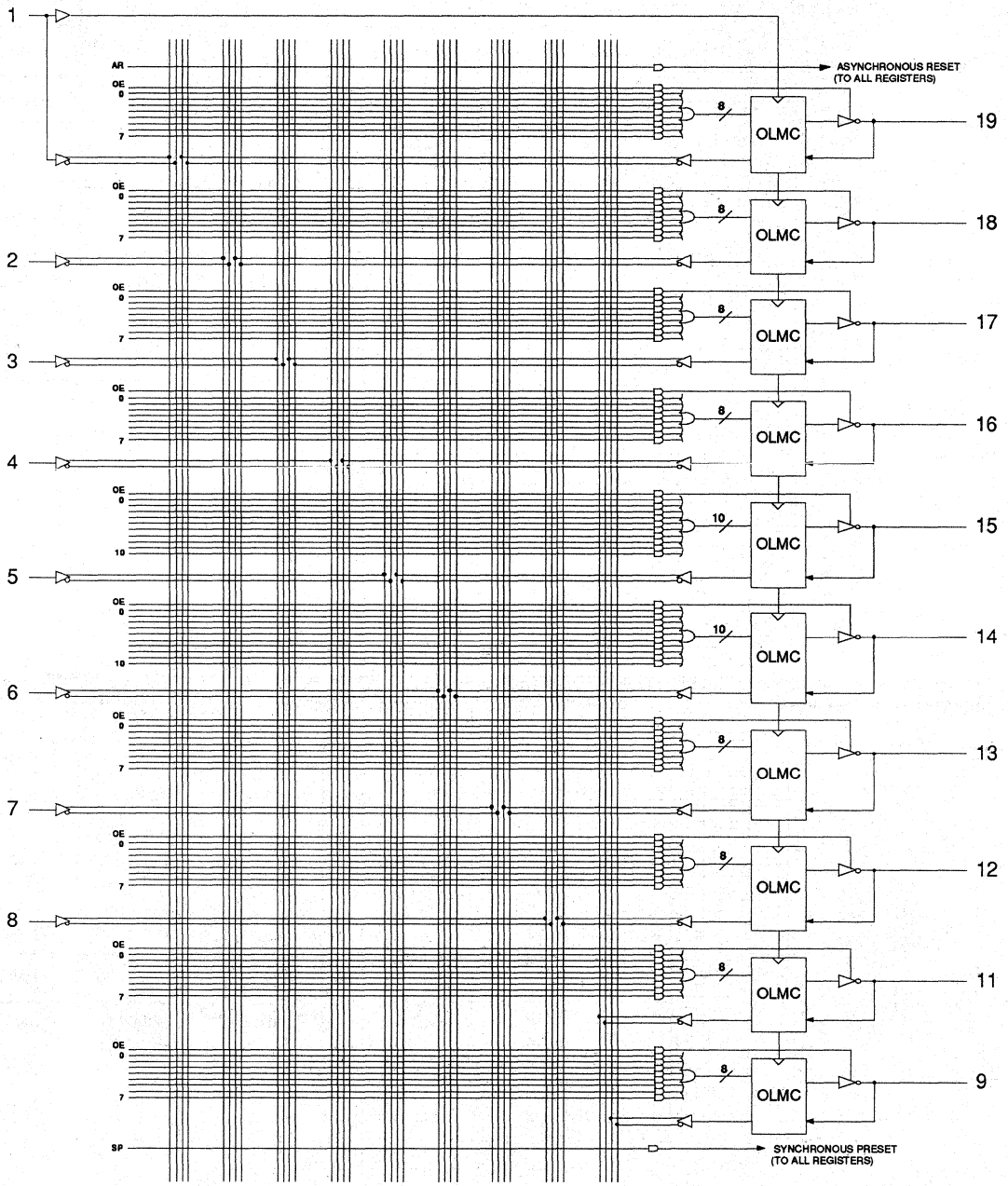


SPEED/GRADE SELECTOR GUIDE

	GRADE		
	Commercial	**Industrial**	**Military**
GAL18V10	15, 20ns	15, 20ns	15, 20ns
GAL22V10	15, 20, 25ns	15, 20, 25ns	15, 20, 30ns
GAL26CV12	15, 20ns	15, 20ns	15, 20ns
Vcc	5.00V ± 5%	5.00V ± 10%	5.00V ± 10%
Temperature	0->75°C	-40->85°C	-55->125°C
Packaging	Plastic DIP PLCC	Plastic DIP PLCC	CERDIP

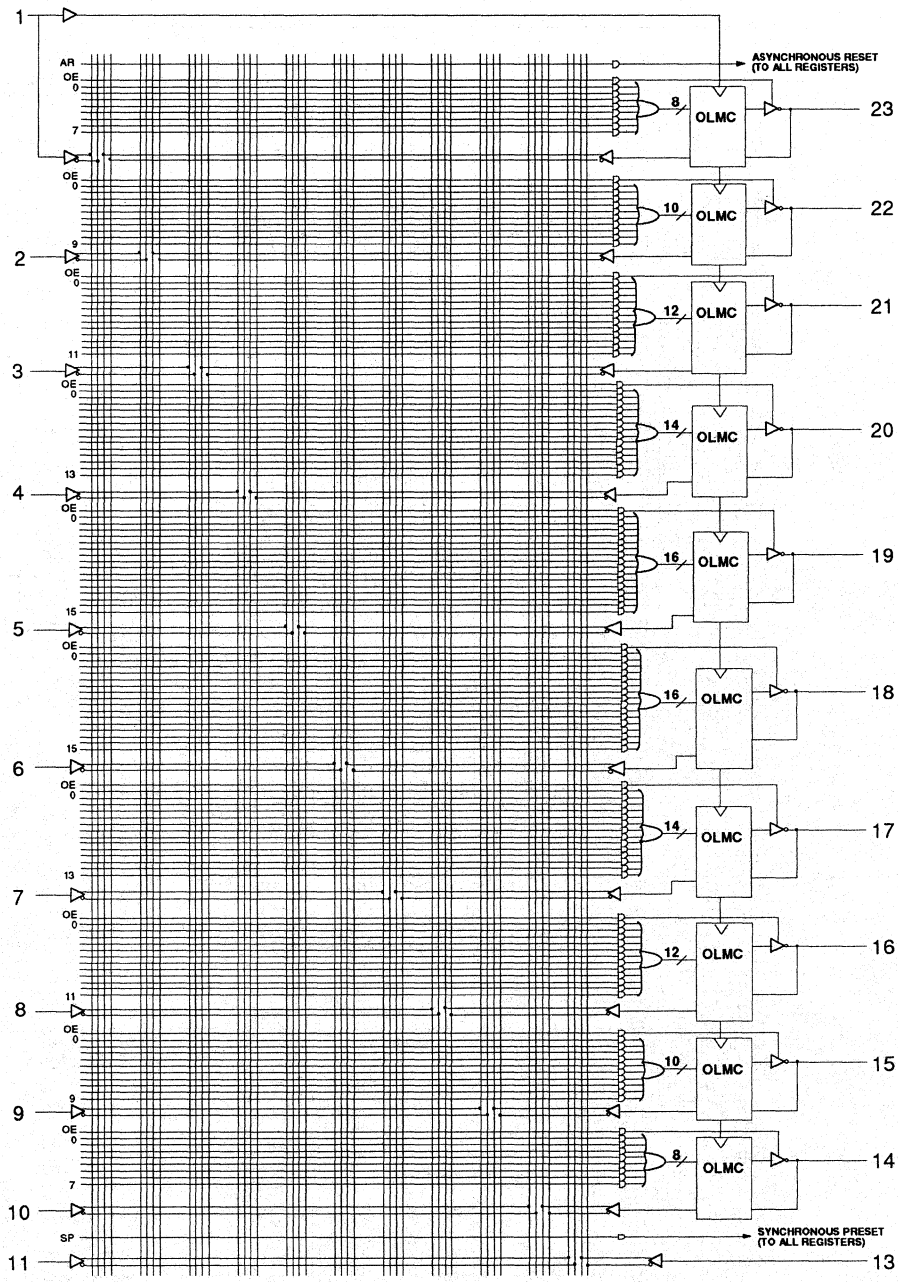
GAL18V10 LOGIC DIAGRAM

GAL18V10



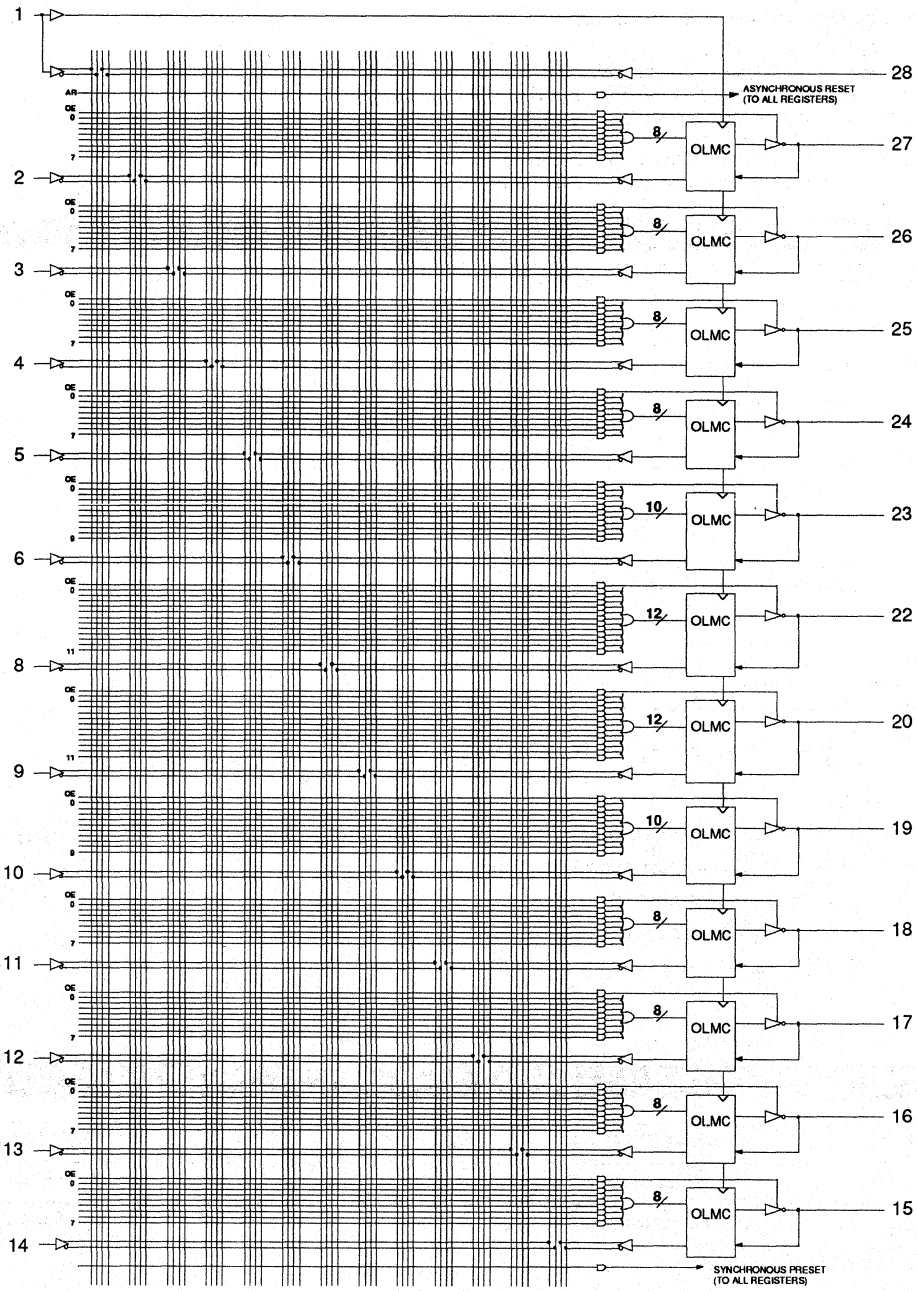
GAL22V10 LOGIC DIAGRAM

GAL22V10



GAL26CV12 LOGIC DIAGRAM

GAL26CV12



ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 125°C

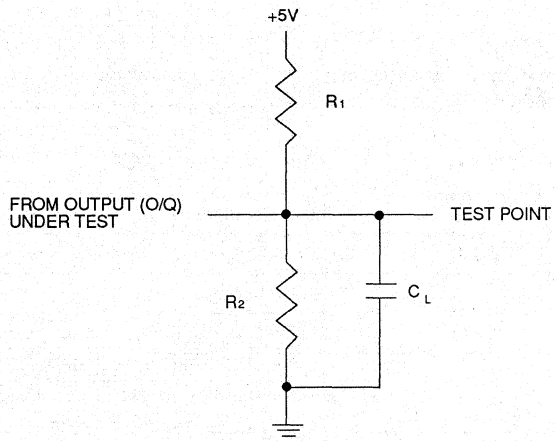
1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

	COMMERCIAL		INDUSTRIAL		MILITARY	
	R_1	R_2	R_1	R_2	R_1	R_2
GAL18V10	300Ω	390Ω	300Ω	390Ω	390Ω	750Ω
GAL22V10	300Ω	390Ω	300Ω	390Ω	390Ω	750Ω
GAL26CV12	470Ω	390Ω	470Ω	390Ω	470Ω	390Ω



CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

AC Test Conditions:

Cond. 1) R_1 per table; C_L = 50pF; R_2 per above table

Cond. 2) Active High R_1 = ∞; Active Low R_1 per table; C_L = 50pF; R_2 per above table

Cond. 3) Active High R_1 = ∞; Active Low R_1 per table; C_L = 5pF; R_2 per above table

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS — 18V10, 22V10, 26CV12-15L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.		2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	GAL26CV12 & 18V10	—	—	-100	µA
			GAL22V10	—	—	-150	µA
I_{IH}, $I_{I/O/QH}$	Leakage Current High	$V_{IH} \geq 3.5V$		—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C		-50	—	-135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V	GAL18V10	—	75	115	mA
		f_{toggle} = 15MHz	GAL22V10 & 26CV12	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-15L Commercial

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
T_A	Ambient Temperature		0	75	°C
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IL}	Input Low Voltage		Vss – 0.5	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc+1	V
I_{OL}	Low Level Output Current	GAL18V10 & 22V10	—	16	mA
		GAL26CV12	—	8	mA
I_{OH}	High Level Output Current		—	-3.2	mA

SWITCHING CHARACTERISTICS — 18V10, 22V10, 26CV12-15L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION		TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output		1	—	15	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	1	—	8	ns
					GAL18V10 & 26CV12	1	—	10	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q		2	—	15	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z		3	—	15	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset		1	—	20	ns

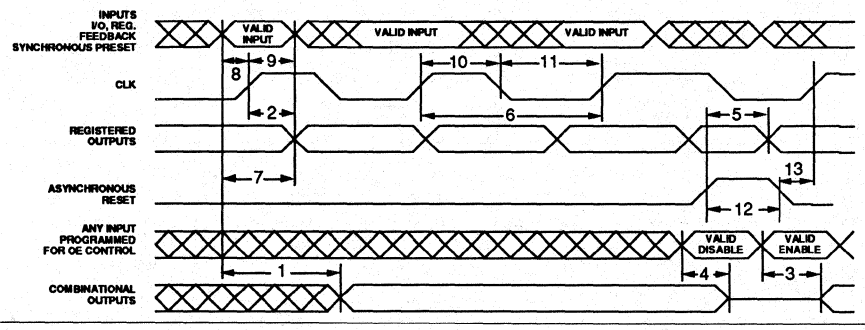
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-15L Commercial

PARAMETER	#	DESCRIPTION		TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$		—	0	62.5	MHz
	7	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$		—	0	50	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	GAL22V10	—	12	—	ns
			GAL18V10 & 26CV12	—	10	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑		—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High[2]		—	8	—	ns
t_{wl}	11	Clock Pulse Duration, Low[2]		—	8	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	GAL22V10	—	15	—	ns
			GAL18V10 & 26CV12	—	10	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time		—	15	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — 18V10, 22V10, 26CV12-20L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

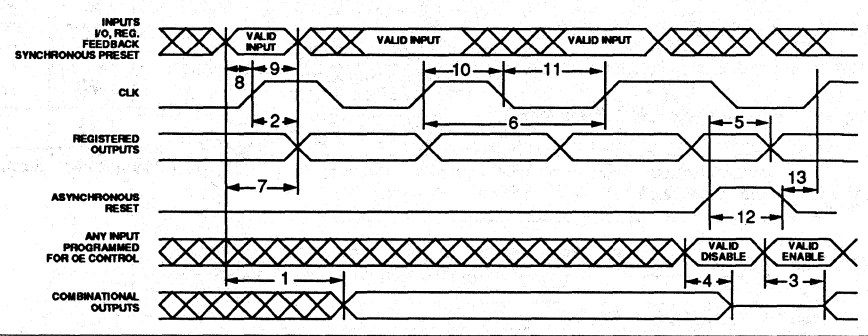
SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.		2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	GAL26CV12 & 18V10	—	—	–100	µA
			GAL22V10	—	—	–150	µA
I_{IH}, $I_{I/O/QH}$	Leakage Current High	$V_{IH} \geq 3.5V$		—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C		–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V	GAL18V10	—	75	115	mA
		f_{toggle} = 15MHz	GAL22V10 & 26CV12	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-20L Commercial

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
T_A	Ambient Temperature		0	75	°C
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IL}	Input Low Voltage		Vss – 0.5	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc+1	V
I_{OL}	Low Level Output Current	GAL18V10	—	16	mA
		GAL22V10 & 26CV12	—	8	mA
I_{OH}	High Level Output Current		—	–3.2	mA

SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS — 18V10, 22V10, 26CV12-20L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION		TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output		1	—	20	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	1	—	10	ns
					GAL18V10 & 26CV12	1	—	12	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q		2	—	20	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z		3	—	20	ns
t_{res}	5	I, I/O	Q	Asynch. Register Reset	GAL22V10	1	—	25	ns
					GAL18V10 & 26CV12	1	—	20	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-20L Commercial

PARAMETER	#	DESCRIPTION		TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clk Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	GAL22V10	—	0	50.0	MHz
			GAL18V10 & 26CV12	—	0	62.5	MHz
	7	Clk Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	GAL22V10	—	0	40.0	MHz
			GAL18V10 & 26CV12	—	0	41.6	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	GAL22V10	—	15	—	ns
			GAL18V10 & 26CV12	—	12	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑		—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High[2]	GAL22V10	—	10	—	ns
			GAL18V10 & 26CV12	—	8	—	ns
t_{wl}	11	Clock Pulse Duration, Low[2]	GAL22V10	—	10	—	ns
			GAL18V10 & 26CV12	—	8	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	GAL22V10	—	20	—	ns
			GAL18V10 & 26CV12	—	15	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	GAL22V10	—	20	—	ns
			GAL18V10 & 26CV12	—	15	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

ELECTRICAL CHARACTERISTICS — GAL22V10-25L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.	2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	—	—	–150	µA
I_{IH}, $I_{I/O/QH}$	Leakage Current High	$V_{IH} \geq 3.5V$	—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL22V10-25L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL22V10-25L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	25	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	1	—	15	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	25	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	25	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	25	ns

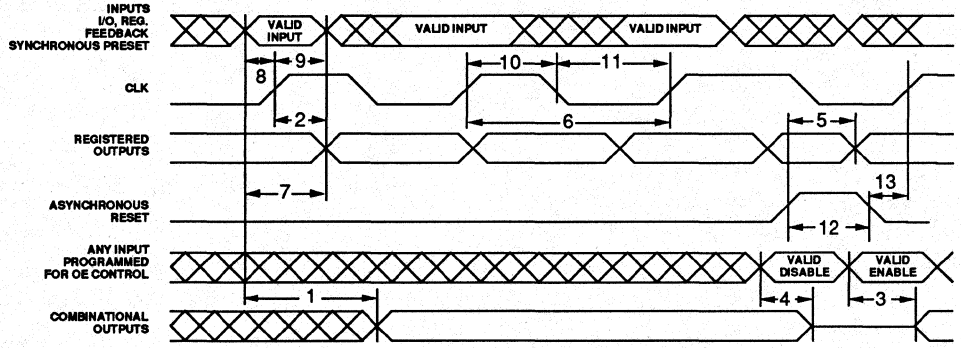
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL22V10-25L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	—	0	33.3	MHz
	7	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	—	0	33.3	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	—	15	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High[2]	—	15	—	ns
t_{wl}	11	Clock Pulse Duration, Low[2]	—	15	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	—	25	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	25	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — 18V10, 22V10, 26CV12-15L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.		2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	GAL26CV12 & 18V10	—	—	–100	µA
			GAL22V10	—	—	–150	µA
I_{IH}, $I_{I/O/QH}$	Leakage Current High	$V_{IH} \geq 3.5V$		—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C		–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	GAL18V10	—	75	125	mA
			GAL22V10 & 26CV12	—	90	150	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-15L Industrial

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
T_A	Ambient Temperature		-40	85	°C
V_{CC}	Supply Voltage		4.5	5.5	V
V_{IL}	Input Low Voltage		Vss – 0.5	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc+1	V
I_{OL}	Low Level Output Current	GAL18V10 & 22V10	—	16	mA
		GAL26CV12	—	8	mA
I_{OH}	High Level Output Current		—	–3.2	mA

PRELIMINARY

SWITCHING CHARACTERISTICS — 18V10, 22V10, 26CV12-15L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION		TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output		1	—	15	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	1	—	8	ns
					GAL18V10 & 26CV12	1	—	10	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q		2	—	15	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z		3	—	15	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset		1	—	20	ns

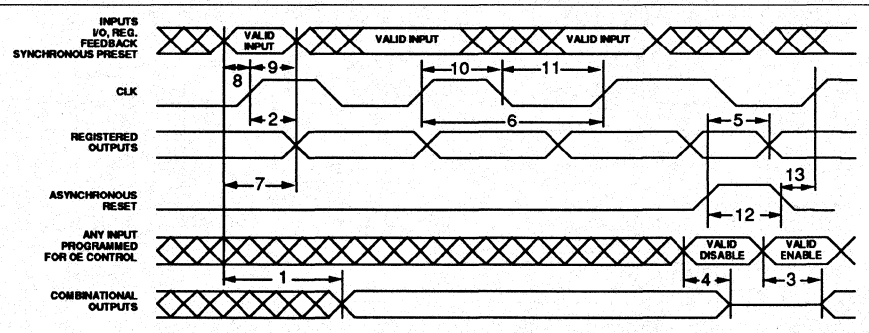
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-15L Industrial

PARAMETER	#	DESCRIPTION		TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$		—	0	62.5	MHz
	7	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$		—	0	50	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	GAL22V10	—	12	—	ns
			GAL18V10 & 26CV12	—	10	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑		—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High[2]		—	8	—	ns
t_{wl}	11	Clock Pulse Duration, Low[2]		—	8	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	GAL22V10	—	15	—	ns
			GAL18V10 & 26CV12	—	10	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time		—	15	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



PRELIMINARY

ELECTRICAL CHARACTERISTICS — 18V10, 22V10, 26CV12-20L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

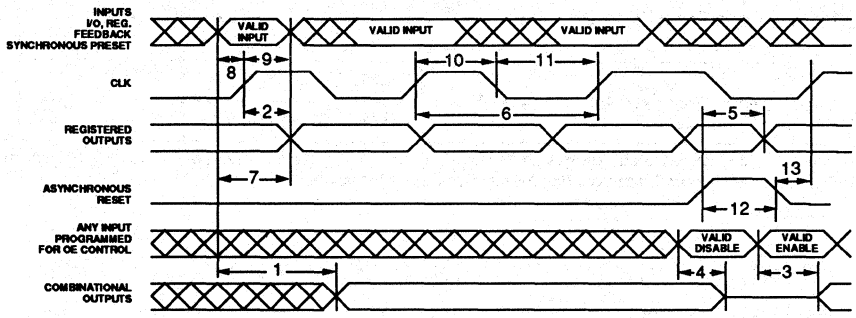
SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.		2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	GAL26CV12 & 18V10	—	—	–100	µA
			GAL22V10	—	—	–150	µA
I_{IH}, $I_{I/O/QH}$	Leakage Current High	$V_{IH} \geq 3.5V$		—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C		–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V	GAL18V10	—	75	125	mA
		f_{toggle} = 15MHz	GAL22V10 & 26CV12	—	90	150	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-20L Industrial

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
T_A	Ambient Temperature		-40	85	°C
V_{CC}	Supply Voltage		4.5	5.5	V
V_{IL}	Input Low Voltage		Vss – 0.5	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc+1	V
I_{OL}	Low Level Output Current	GAL18V10 & 22V10	—	16	mA
		GAL26CV12	—	8	mA
I_{OH}	High Level Output Current		—	–3.2	mA

SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS — 18V10, 22V10, 26CV12-20L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION		TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output		1	—	20	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	1	—	10	ns
					GAL18V10 & 26CV12	1	—	12	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q		2	—	20	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z		3	—	20	ns
t_{res}	5	I, I/O	Q	Asynch. Register Reset		1	—	25	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-20L Industrial

PARAMETER	#	DESCRIPTION		TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clk Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	GAL22V10	—	0	50.0	MHz
			GAL18V10 & 26CV12	—	0	62.5	MHz
	7	Clk Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	GAL22V10	—	0	40.0	MHz
			GAL18V10 & 26CV12	—	0	41.6	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	GAL22V10	—	15	—	ns
			GAL18V10 & 26CV12	—	12	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑		—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High[2]	GAL22V10	—	10	—	ns
			GAL18V10 & 26CV12	—	8	—	ns
t_{wl}	11	Clock Pulse Duration, Low[2]	GAL22V10	—	10	—	ns
			GAL18V10 & 26CV12	—	8	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	GAL22V10	—	20	—	ns
			GAL18V10 & 26CV12	—	15	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	GAL22V10	—	20	—	ns
			GAL18V10 & 26CV12	—	15	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

ELECTRICAL CHARACTERISTICS — 18V10, 22V10, 26CV12-15L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.		2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	GAL26CV12 & 18V10	—	—	–100	µA
			GAL22V10	—	—	–150	µA
I_{IH}, $I_{I/O/QH}$	Leakage Current High	$V_{IH} \geq 3.5V$		—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C		–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	GAL18V10	—	75	135	mA
			GAL22V10 & 26CV12	—	90	150	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-15L Military

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
T_C	Case Temperature		-55	125	°C
V_{CC}	Supply Voltage		4.5	5.5	V
V_{IL}	Input Low Voltage		Vss – 0.5	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc+1	V
I_{OL}	Low Level Output Current	GAL18V10 & 22V10	—	12	mA
		GAL26CV12	—	8	mA
I_{OH}	High Level Output Current		—	–2.0	mA

ADVANCED

SWITCHING CHARACTERISTICS — 18V10, 22V10, 26CV12-15L Military

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION		TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output		1	—	15	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	1	—	8	ns
					GAL18V10 & 26CV12	1	—	10	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q		2	—	15	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z		3	—	15	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset		1	—	20	ns

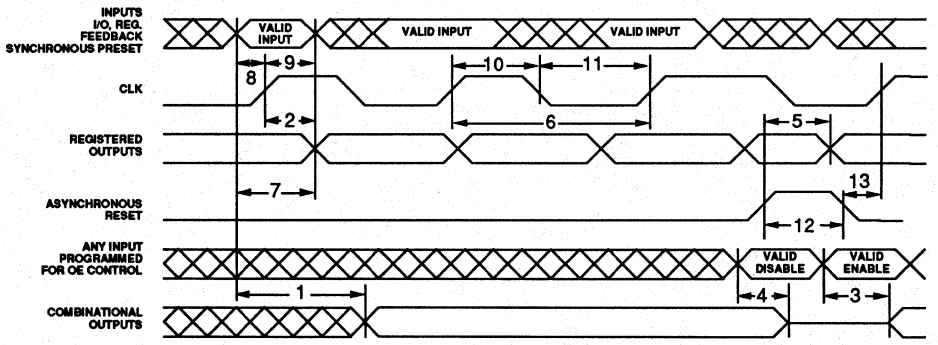
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-15L Military

PARAMETER	#	DESCRIPTION		TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$		—	0	62.5	MHz
	7	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	GAL22V10	—	0	50	MHz
			GAL18V10 & 26CV12	—	0	45.5	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑		—	12	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑		—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High[2]		—	8	—	ns
t_{wl}	11	Clock Pulse Duration, Low[2]		—	8	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration		—	15	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time		—	15	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ADVANCED

ELECTRICAL CHARACTERISTICS — 18V10, 22V10, 26CV12-20L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.		2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	GAL26CV12 & 18V10	—	—	–100	µA
			GAL22V10	—	—	–150	µA
I_{IH}, $I_{I/O/QH}$	Leakage Current High	$V_{IH} \geq 3.5V$		—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C		–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V	GAL18V10	—	75	135	mA
		f_{toggle} = 15MHz	GAL22V10 & 26CV12	—	90	150	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-20L Military

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
T_C	Case Temperature		-55	125	°C
V_{CC}	Supply Voltage		4.5	5.5	V
V_{IL}	Input Low Voltage		Vss – 0.5	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc+1	V
I_{OL}	Low Level Output Current	GAL18V10 & 22V10	—	12	mA
		GAL26CV12	—	8	mA
I_{OH}	High Level Output Current		—	–2.0	mA

SWITCHING CHARACTERISTICS — 18V10, 22V10, 26CV12-20L Military

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION		TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output		1	—	20	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	1	—	15	ns
					GAL18V10 & 26CV12	1	—	15	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q		2	—	20	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z		3	—	20	ns
t_{res}	5	I, I/O	Q	Asynch. Register Reset		1	—	25	ns

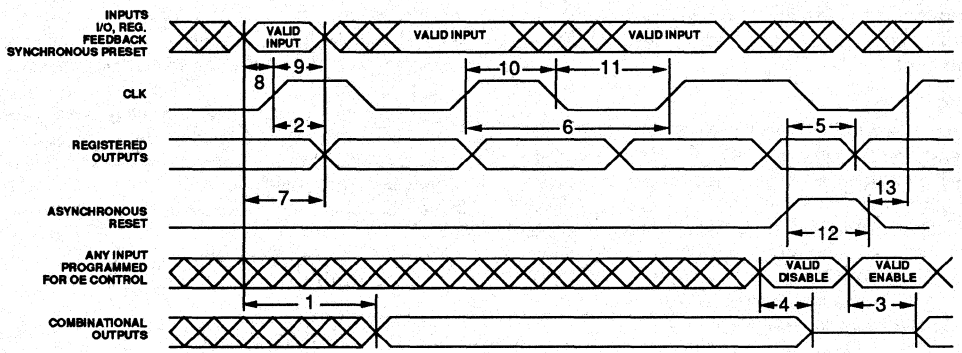
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — 18V10, 22V10, 26CV12-20L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	—	0	33.3	MHz
	7	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	—	0	31.2	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	—	17	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High[2]	—	15	—	ns
t_{wl}	11	Clock Pulse Duration, Low[2]	—	15	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	—	20	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	20	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



OUTPUT LOGIC MACROCELL ARCHITECTURE

The GAL18V10, 22V10, and 26CV12 each have a variable number of product terms per OLMC.

Of the ten OLMCs available in the GAL18V10, eight OLMCs have access to eight product terms and two have ten product terms (refer to GAL18V10 Logic Diagram).

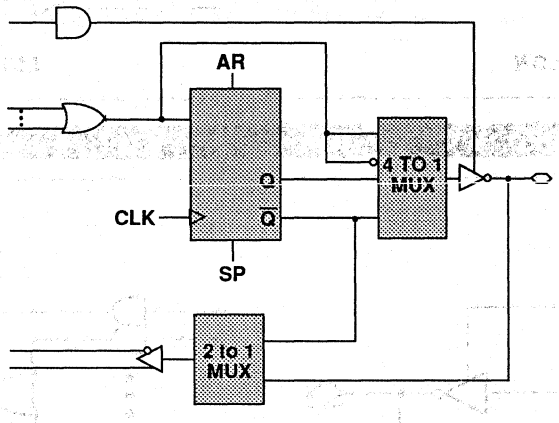
Of the ten OLMCs available in the GAL22V10, two OLMCs have access to eight product terms, two have ten product terms, two have twelve product terms, two have fourteen product terms, and two OLMCs have sixteen product terms (refer to GAL22V10 Logic Diagram).

Of the twelve OLMCs available in the GAL26CV12, eight OLMCs have access to eight product terms, two have ten product terms, and two have twelve product terms (refer to GAL26CV12 Logic Diagram).

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinational or registered mode. This allows the user to reduce the overall number of product terms required in a design and/or to invert the output signal.

GAL22V10 Family devices have a product term for AR (Asynchronous Reset) and a product term for SP (Synchronous Preset). These two product terms are common to all registered OLMCs.

NOTE: Output polarity selection does NOT affect the behavior of the OLMC's integral "D" flip-flop but does affect the value (0 or 1) of the output. The AR and SP product terms will force the flip-flop into the same state regardless of the polarity of the output.



GAL18V10, 22V10, and 26CV12 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

The GAL18V10, 22V10, and 26CV12 have two primary functional modes which may be selected when compiling source equations (registered and combinational / input). Each of these two primary modes are described below.

REGISTERED

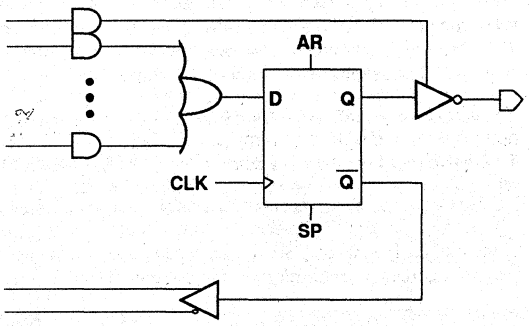
In registered mode the output pin associated with an individual OLMC is driven by the "Q" output of that OLMC's "D" flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or invert (active low). Output tri-state control is available and can be individually selected as either "on", "off", or dynamically "product-term driven. " The "D" flip-flop's "/Q" output is fed back into the "AND" array via the "AND" array buffer. Both polarities (true and invert) of the OLMC are fed back into the "AND" array.

NOTE: In registered mode a tri-stated output pin may NOT be used as an input into the "AND" array.

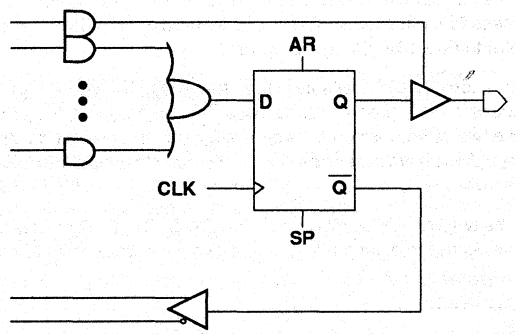
COMBINATIONAL / INPUT

In combinational mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or invert (active low). Output tri-state control is available and may be individually selected as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feed back into the "AND" array is from the device pin, via the "AND" array buffer. Both polarities (true and invert) of the pin are fed back into the "AND" array.

REGISTERED MODE

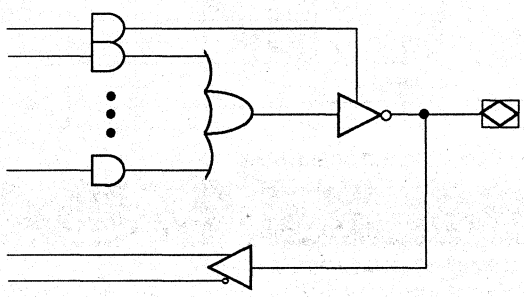


ACTIVE LOW

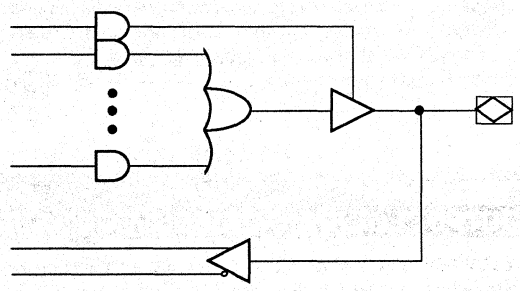


ACTIVE HIGH

COMBINATIONAL MODE



ACTIVE LOW



ACTIVE HIGH

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL18V10, 22V10, and 26CV12 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided with every GAL18V10, 22V10, and 26CV12 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

LATCH-UP PROTECTION

GAL18V10, 22V10, and 26CV12 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullup instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

OUTPUT REGISTER PRELOAD

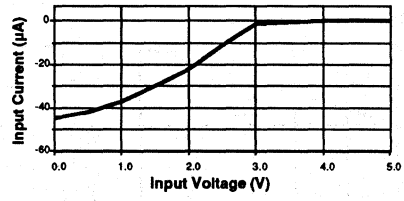
When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

GAL18V10, 22V10, and 26CV12 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

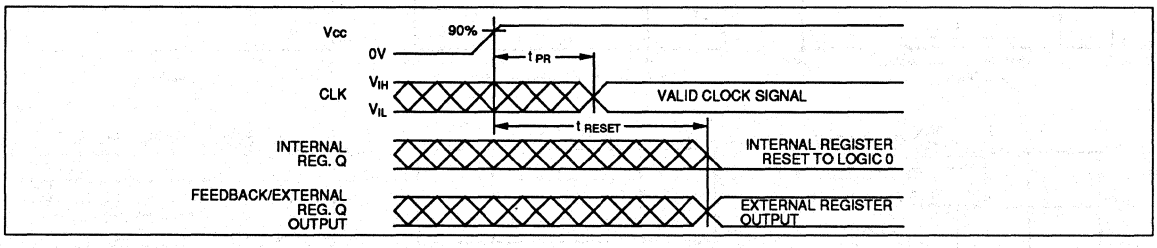
INPUT BUFFERS

GAL22V10 Family devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than bipolar logic.

The buffers also possess active pull-ups within their input structure. Unused inputs and I/O's will float to a TTL "high" (logical "1"), Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.



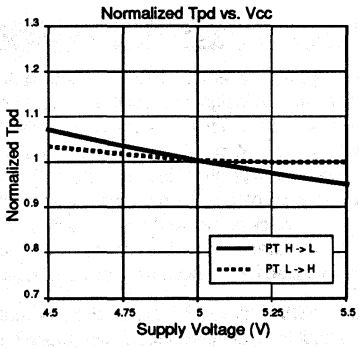
POWER-UP RESET

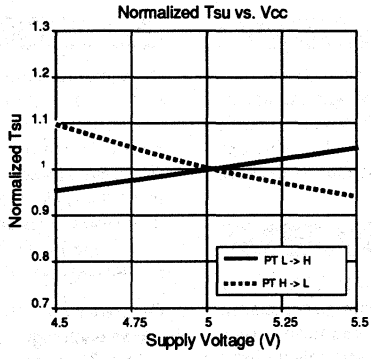


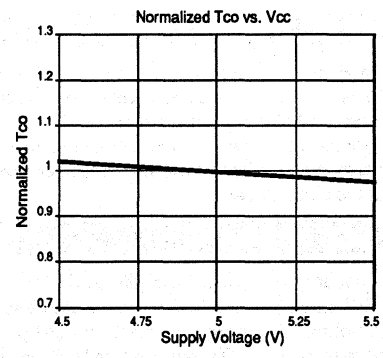
Circuitry within GAL18V10, 22V10, and 26CV12 devices provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). This feature can greatly simplify state machine design by providing a known state on power-up.

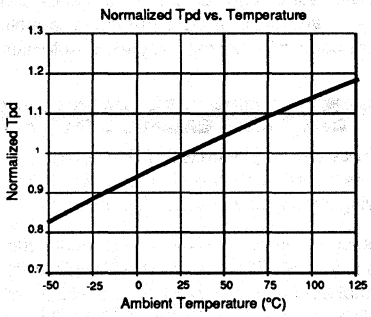
The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

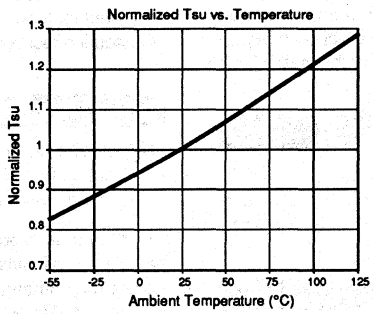
Note that the internal register powers-up to a logic 0. The device pin state is determined by the user-defined polarity control bit on each macrocell (refer to OLMC description).

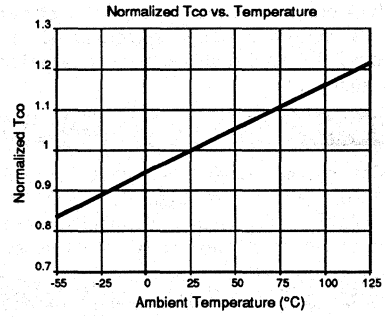

Normalized Tpd vs. Vcc
Normalized Tpd
Supply Voltage (V)
PT H -> L
PT L -> H

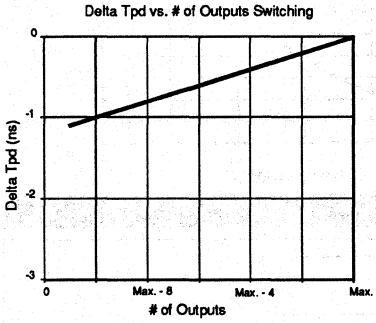

Normalized Tsu vs. Vcc
Normalized Tsu
Supply Voltage (V)
PT L -> H
PT H -> L

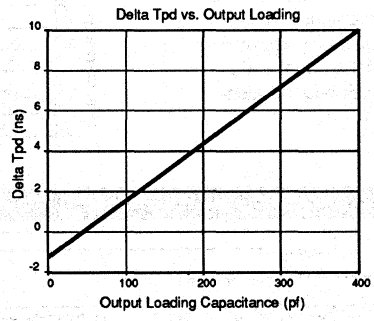

Normalized Tco vs. Vcc
Normalized Tco
Supply Voltage (V)

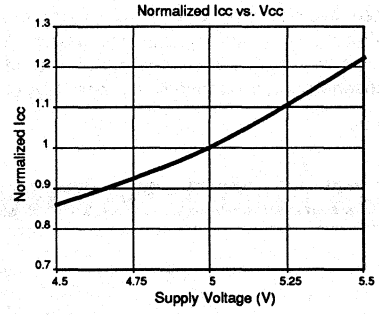

Normalized Tpd vs. Temperature
Normalized Tpd
Ambient Temperature (°C)

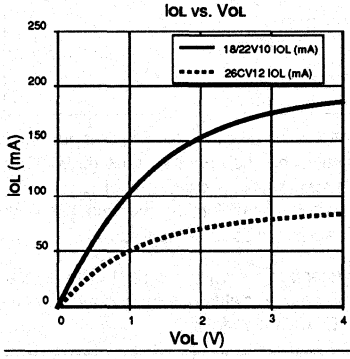

Normalized Tsu vs. Temperature
Normalized Tsu
Ambient Temperature (°C)

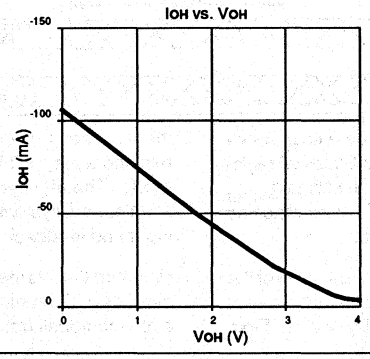

Normalized Tco vs. Temperature
Normalized Tco
Ambient Temperature (°C)

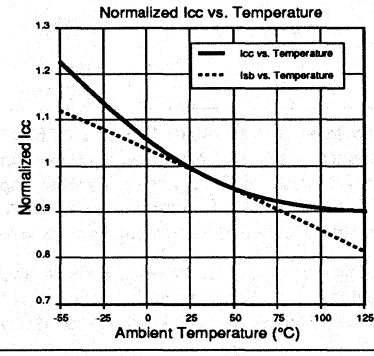

Delta Tpd vs. # of Outputs Switching
Delta Tpd (ns)
# of Outputs
Max. - 8
Max. - 4
Max.


Delta Tpd vs. Output Loading
Delta Tpd (ns)
Output Loading Capacitance (pf)


Normalized Icc vs. Vcc
Normalized Icc
Supply Voltage (V)


IOL vs. VOL
IOL (mA)
VOL (V)
18/22V10 IOL (mA)
26CV12 IOL (mA)


IOH vs. VOH
IOH (mA)
VOH (V)


Normalized Icc vs. Temperature
Normalized Icc
Ambient Temperature (°C)
Icc vs. Temperature
Isb vs. Temperature

GAL 20RA10

High Performance E²CMOS® Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS TECHNOLOGY**
  - **15 ns Maximum Propagation Delay**
  - **Fmax = 50 MHz**
  - **15 ns Maximum from Clock Input to Data Output**
  - **TTL Compatible 8 mA Outputs**
  - **UltraMOS® III Advanced CMOS Technology**
  - **Internal Pull-Up Resistor on all Pins**
- **50% REDUCTION IN POWER**
  - **100 mA MAX I_{cc}**
- **E² CELL TECHNOLOGY**
  - **Reconfigurable Logic**
  - **Reprogrammable Cells**
  - **100% Tested/Guaranteed 100% Yields**
  - **High Speed Electrical Erasure (<50ms)**
  - **20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **Maximum Flexibility for Complex Logic Designs**
    Registered or Combinational with Polarity
  - **Individually Programmable Macrocell Functions:**
    Product Term Clock
    Asynchronous Reset
    Asynchronous Preset
    Output Enable
  - **Common Output Enable & Preload Functions**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **100% Functional Testability**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

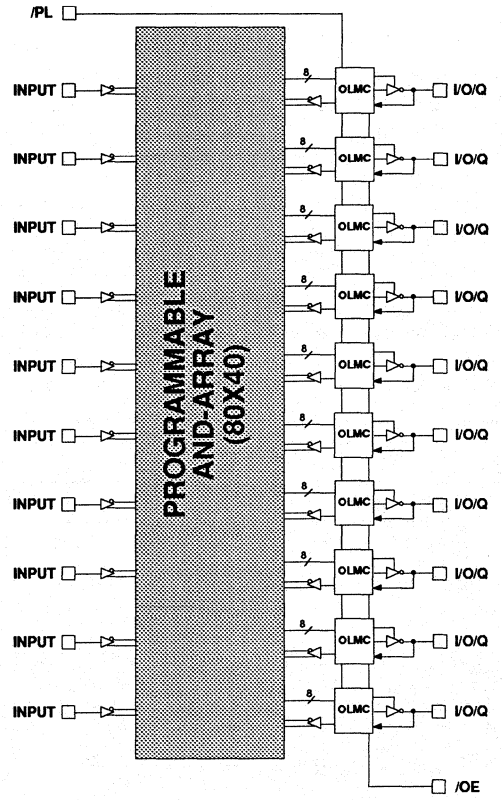
DESCRIPTION

The GAL®20RA10, at 15 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest performance available of any 20RA10 device on the market. CMOS circuitry allows the GAL20RA10 to consume just 100 mA maximum I_{cc} which represents a 50% savings in power when compared to its bipolar counterparts. The E² technology offers high speed (50ms) erase times providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is fully function/fuse map/parametric compatible with bipolar and CMOS 20RA10 devices.

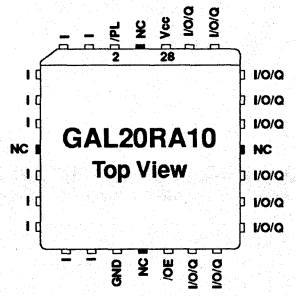
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM

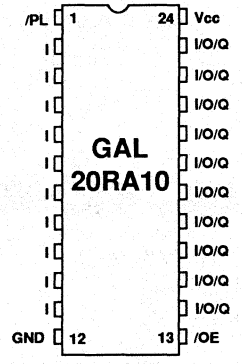


PIN DIAGRAMS

Chip Carrier



DIP



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LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} .....–.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

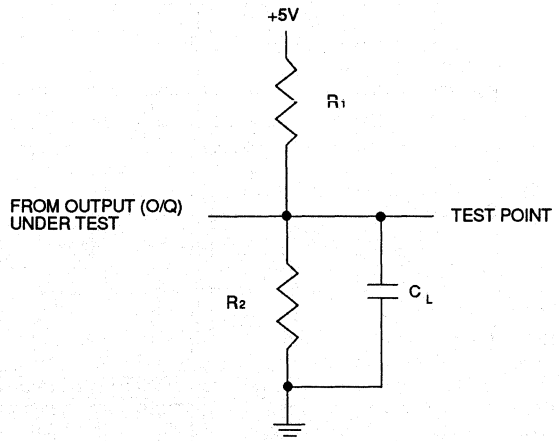
COMMERCIAL		INDUSTRIAL		MILITARY	
R_1	R_2	R_1	R_2	R_1	R_2
470	390	470	390	470	390

AC Test Conditions:

Cond. 1) R_1 per table; C_L = 50pF; R_2 per above table

Cond. 2) Active High $R_1 = \infty$; Active Low R_1 per table; C_L = 50pF; R_2 per above table

Cond. 3) Active High $R_1 = \infty$; Active Low R_1 per table; C_L = 5pF; R_2 per above table



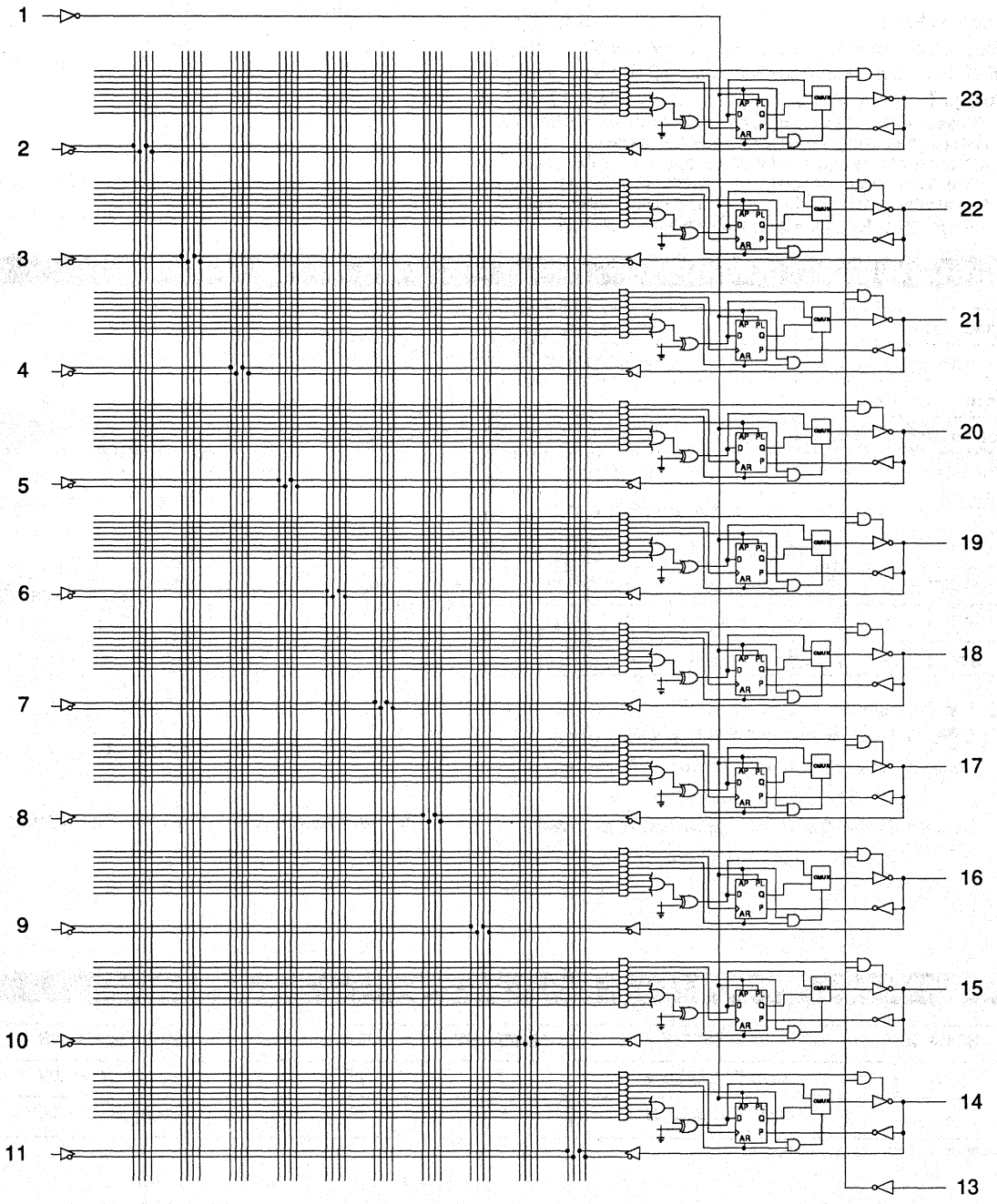
CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

GAL20RA10 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS — GAL20RA10-15L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.	2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	—	—	–100	µA
I_{IH}, $I_{I/O/QH}$[1]	Leakage Current High	$V_{IH} \geq 3.5V$	—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	100	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-15L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	8	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL20RA10-15L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	15	ns
t_{co}	2	I, I/O	Q	Input Clock to Registered Output	1	—	15	ns
$t_{en/dis}$	3	I, I/O	O, Q	Input to Output Enable/Disable	2,3	—	15	ns
$t_{en/dis}$	4	I	O, Q	Pin 13 to Output Enable/Disable	2,3	—	12	ns
$t_{ar/ap}$	5	I, I/O	Q	Asynchronous Register Reset/Preset	1	—	15	ns

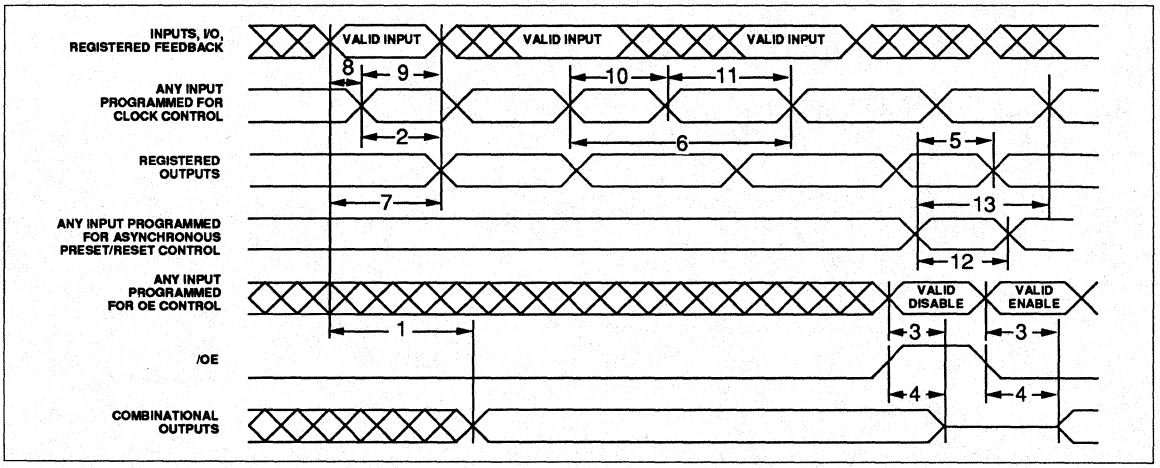
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-15L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1/(t_{wh}+t_{wl})$	—	0	50.0	MHz
	7	Clock Frequency with Feedback[1] = $1/(t_{su}+t_{co})$	—	0	45.0	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	7	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High[2]	—	10	—	ns
	11	Clock Pulse Duration, Low[2]	—	10	—	ns
t_{rpw}	12	Asynchronous Reset/Preset Pulse Duration	—	15	—	ns
t_{rec}	13	Asynchronous Reset/Preset to Clk ↑ Recovery Time	—	10	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL20RA10-20L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.	2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	—	—	–100	µA
I_{IH}, $I_{I/O/QH}$[1]	Leakage Current High	$V_{IH} \geq 3.5V$	—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	100	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	8	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL20RA10-20L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns
t_{co}	2	I, I/O	Q	Input Clock to Registered Output	1	—	20	ns
$t_{en/dis}$	3	I, I/O	O, Q	Input to Output Enable/Disable	2,3	—	20	ns
$t_{en/dis}$	4	I	O, Q	Pin 13 to Output Enable/Disable	2,3	—	15	ns
$t_{ar/ap}$	5	I, I/O	Q	Asynchronous Register Reset/Preset	1	—	20	ns

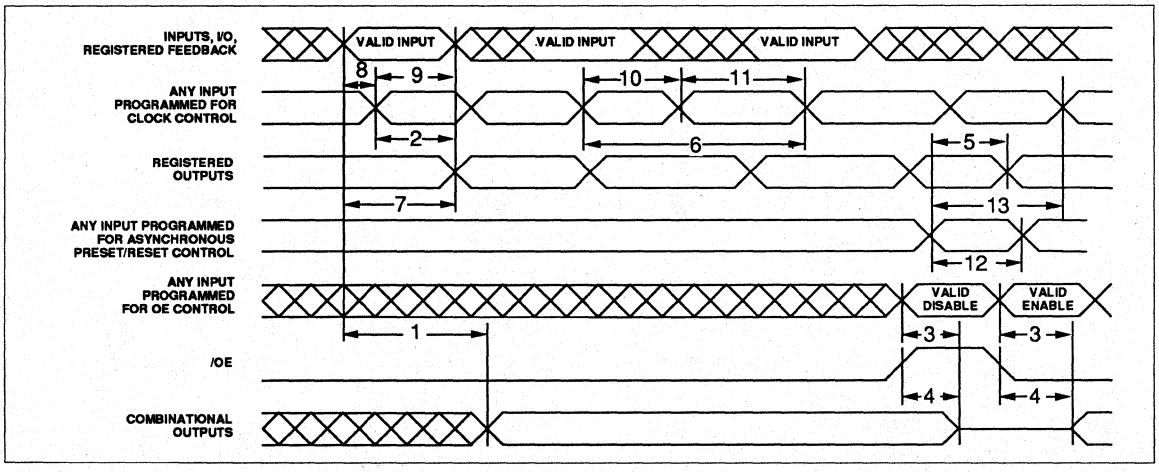
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1/(t_{wh}+t_{wl})$	—	0	41.7	MHz
	7	Clock Frequency with Feedback[1] = $1/(t_{su}+t_{co})$	—	0	33.3	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	10	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High[2]	—	12	—	ns
	11	Clock Pulse Duration, Low[2]	—	12	—	ns
t_{rpw}	12	Asynchronous Reset/Preset Pulse Duration	—	20	—	ns
t_{rec}	13	Asynchronous Reset/Preset to Clk ↑ Recovery Time	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL20RA10-20L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.	2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	—	—	–100	µA
I_{IH}, $I_{I/O/QH}$[1]	Leakage Current High	$V_{IH} \geq 3.5V$	—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	120	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	-40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	8	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL20RA10-20L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns
t_{co}	2	I, I/O	Q	Input Clock to Registered Output	1	—	20	ns
$t_{en/dis}$	3	I, I/O	O, Q	Input to Output Enable/Disable	2,3	—	20	ns
$t_{en/dis}$	4	I	O, Q	Pin 13 to Output Enable/Disable	2,3	—	15	ns
$t_{ar/ap}$	5	I, I/O	Q	Asynchronous Register Reset/Preset	1	—	20	ns

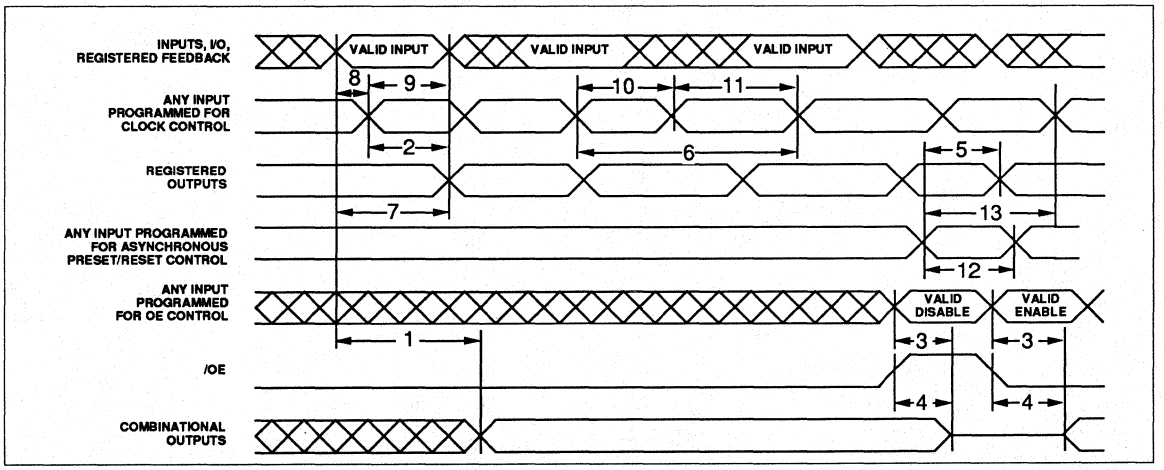
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1/(t_{wh}+t_{wl})$	—	0	41.7	MHz
	7	Clock Frequency with Feedback[1] = $1/(t_{su}+t_{co})$	—	0	33.3	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	10	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High[2]	—	12	—	ns
	11	Clock Pulse Duration, Low[2]	—	12	—	ns
t_{rpw}	12	Asynchronous Reset/Preset Pulse Duration	—	20	—	ns
t_{rec}	13	Asynchronous Reset/Preset to Clk ↑ Recovery Time	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL20RA10-20L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.	2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	—	—	–100	µA
I_{IH}, $I_{I/O/QH}$[1]	Leakage Current High	$V_{IH} \geq 3.5V$	—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	120	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	8	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL20RA10-20L Military

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns
t_{co}	2	I, I/O	Q	Input Clock to Registered Output	1	—	20	ns
$t_{en/dis}$	3	I, I/O	O, Q	Input to Output Enable/Disable	2,3	—	20	ns
$t_{en/dis}$	4	I	O, Q	Pin 13 to Output Enable/Disable	2,3	—	15	ns
$t_{ar/ap}$	5	I, I/O	Q	Asynchronous Register Reset/Preset	1	—	20	ns

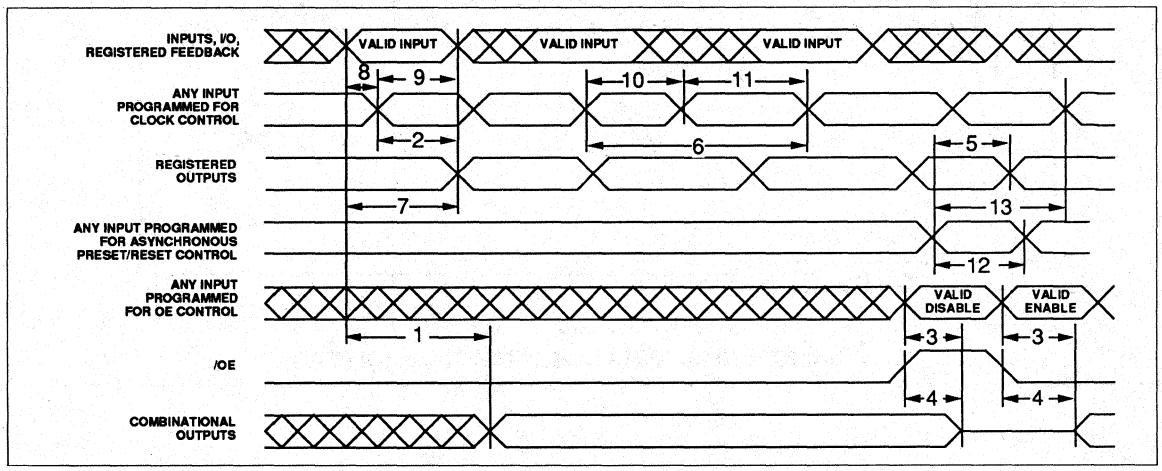
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1/(t_{wh}+t_{wl})$	—	0	41.7	MHz
	7	Clock Frequency with Feedback[1] = $1/(t_{su}+t_{co})$	—	0	33.3	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	10	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High[2]	—	12	—	ns
	11	Clock Pulse Duration, Low[2]	—	12	—	ns
t_{rpw}	12	Asynchronous Reset/Preset Pulse Duration	—	20	—	ns
t_{rec}	13	Asynchronous Reset/Preset to Clk ↑ Recovery Time	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



OUTPUT LOGIC MACROCELL ARCHITECTURE

The GAL20RA10 has eight product terms for each of the ten available OLMCs. Four of the product terms are used for generating the logic function. The remaining four product terms control asynchronous reset, asynchronous preset, clock and output enable individually for every OLMC. Each OLMC can also be individually configured as registered or combinational.

All of the 20 input and I/O pins have a unique array input path assigned to them. This allows input functions of up to 19 inputs (assuming at least one output function is used) using any combination of 10 dedicated and 9 of the 10 programmable I/O pins. All macrocells are controlled by the same configuration of data and control pins allowing the design engineer to exchange pin assignments for I/O functions without restriction.

OUTPUT ENABLE

The output enable function of each macrocell is controlled by a dynamic "AND" function of a product term in each macrocell and a common, active low /OE device pin. If product term control is selected then all macrocells must be product term controlled as the /OE device pin must be tied to a logic "0" for product term control to be effective.

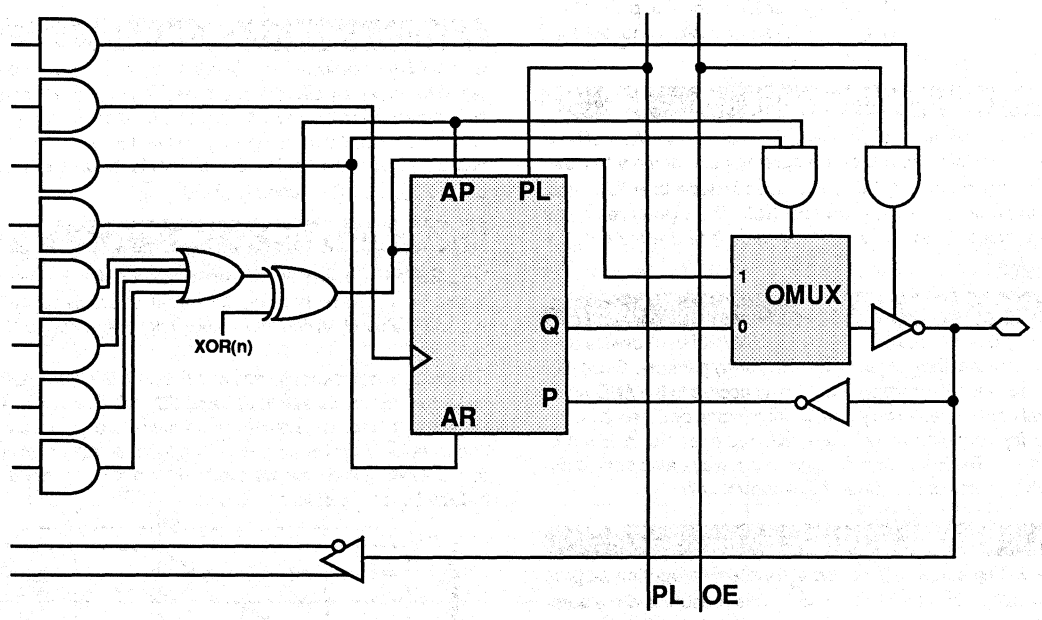
REGISTER / COMBINATIONAL CONTROL

Register control in each macrocell is dynamic through the use of the individual Clock, Reset and Preset product terms. Macrocells with both the Reset and Preset product terms held logic "1" simultaneously will have register-bypass enabled for asynchronous operation. Selection of the registered operating mode is accomplished by not allowing both the Reset & Preset product terms to be logic "1" simultaneously. Preset and Reset affect the register on the rising edge of a logic "1" level of the appropriate product term. Similarly, the data is clocked into the register on the rising edge of the Clock product term. The GAL20RA10 has a common register preload function controlled by the PL pin.

OUTPUT POLARITY

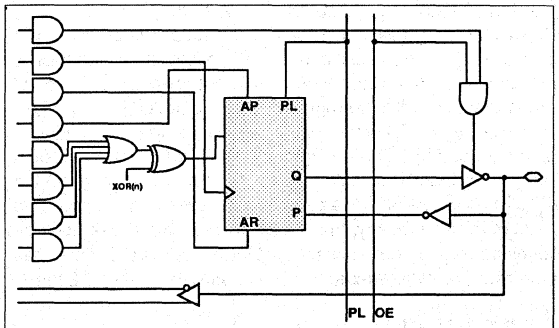
The output polarity can be individually programmed to be true or inverting without any performance degradation, in either combinational or registered mode. This allows the user to reduce the overall number of product terms required in a design and to invert the output signal.

NOTE: Output polarity selection does NOT affect the behavior of the OLMC's integral "D" flip-flop. The AR and AP product terms will force the flip-flop to Reset/Preset regardless of the polarity of the output.

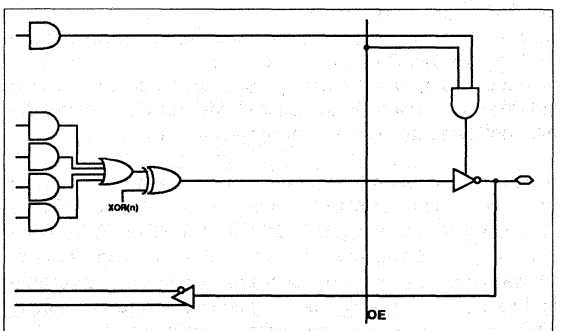


GAL20RA10 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS



REGISTERED WITH POLARITY



COMBINATIONAL WITH POLARITY

RESET/PRESET FUNCTIONALITY

The AR and AP product terms are sensed on the rising edge. In addition, these pins control the selection of registered or combinational operating mode.

RESET	PRESET	FUNCTION
0	0	Registered function of data product terms
↑	0	Reset register to "0" (device pin = "1')
0	↑	Preset register to "1" (device pin = "0')
0	↑	Register-bypass (combinational output)

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL®20RA10 device. It contains 80 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided with every GAL®20RA10 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

ASYNCRHONOUS CLOCK

A separate clock control product term is provided for each GAL20RA10 macrocell. The data is clocked into the register on the rising edge of the clock product term. The use of individual clock control product terms allows up to ten seperate clocks or clock pins for a highly asynchrounous system, or through the use of a common AND function driving several clock product terms groups of registers can be clocked together.

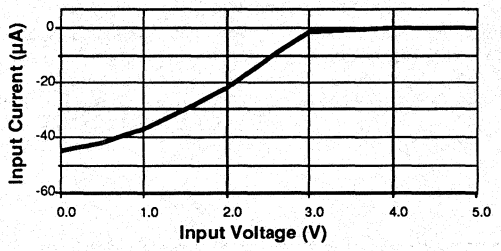
LATCH-UP PROTECTION

GAL®20RA10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullup instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

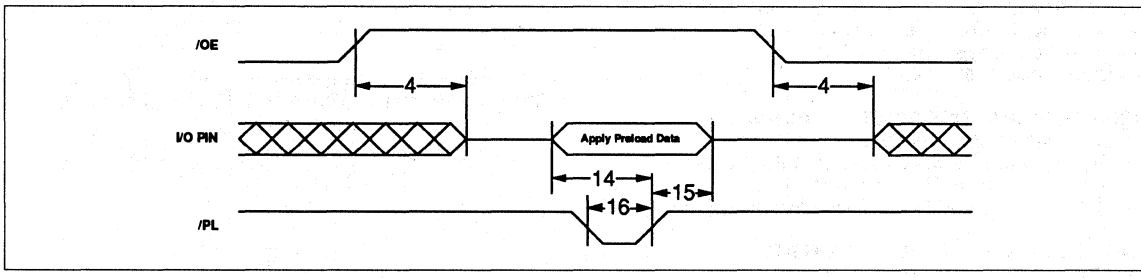
INPUT BUFFERS

GAL®20RA10 devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar logic.

The buffers also possess active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"), however, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.



REGISTER PRELOAD



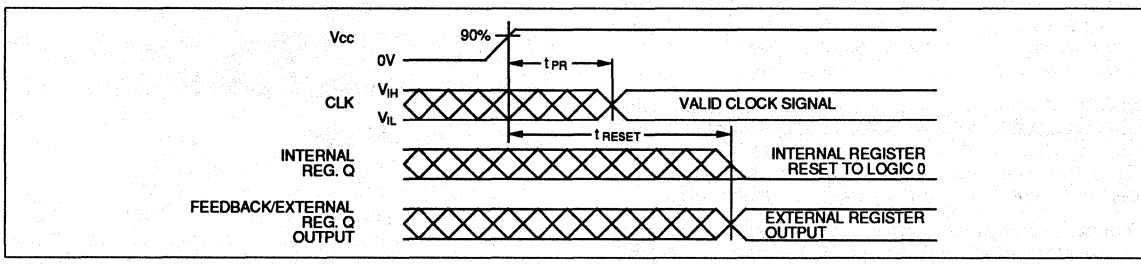
Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	MIN.	MAX.	UNITS
$t_{en/dis}$	4	/OE ↑	O	Pin 13 to Output Enable/Disable	—	*	ns
t_{sup}	14	I/O	/PL ↑	Setup Time, Apply Preload Data before /PL↑	15	—	ns
t_{hp}	15	/PL ↑	no data	Hold Time, after /PL ↑	—	15	ns
t_{wp}	16	/PL ↓	/PL ↑	Preload Pulse Duration	—	15	ns

* Refer to **Switching Characteristics Table**.

The registers of the GAL20RA10 can be preloaded from the I/O pins to facilitate board-level (TTL-level) control for initialization and testing of state machine designs. This capability can be used to force the device into a particular state without lengthy sequencing operations. Non-valid (illegal) states for a given design can also be entered to assure that the state machine recovers properly. This function is used by qualified device programmers to apply test vector sequences during functional testing.

POWER-UP RESET



Circuitry within the GAL20RA10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20RA10. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

GAL6001

High Performance E²CMOS®
Generic Array Logic™

FEATURES

- **ELECTRICALLY ERASABLE CELL TECHNOLOGY**
  - **Instantly Reconfigurable Logic**
  - **Instantly Reprogrammable Cells**
  - **Guaranteed 100% Yields**
- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **Low Power: 90mA Typical**
  - **High Speed: 12ns Max. Clock to Output Delay**
    25ns Max. Setup Time
    30ns Max. Propagation Delay
- **UNPRECENTED FUNCTIONAL DENSITY**
  - **78 x 64 x 36 FPLA Architecture**
  - **10 Output Logic Macrocells**
  - **8 Buried Logic Macrocells**
  - **20 Input and I/O Logic Macrocells**
- **HIGH-LEVEL DESIGN FLEXIBILITY**
  - **Asynchronous or Synchronous Clocking**
  - **Separate State Register and Input Clock Pins**
  - **Functionally Supersets Existing 24-pin PAL® and IFL™ Devices**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **SPACE SAVING 24-PIN, 300-MIL DIP**
- **HIGH SPEED PROGRAMMING ALGORITHM**
- **20-YEAR DATA RETENTION**

DESCRIPTION

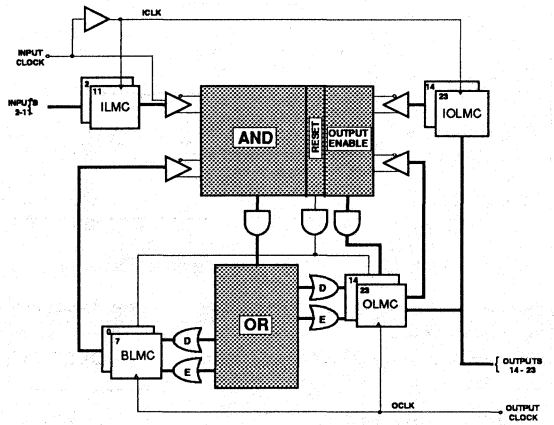
Using a high performance E²CMOS technology, Lattice Semiconductor has produced a next-generation programmable logic device, the GAL6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL6001 offers the highest degree of functional integration, flexibility, and speed currently available in a 24-pin, 300-mil package.

The GAL6001 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL6001 during manufacture. This allows Lattice to guarantee 100% performance to specifications. In addition, data retention of 20 years and a minimum of 100 erase/write cycles are guaranteed.

Programming is accomplished using standard hardware and software tools. In addition, an Electronic Signature is available for storage of user specified data, and a security cell is provided to protect proprietary designs.

FUNCTIONAL BLOCK DIAGRAM



MACROCELL NAMES

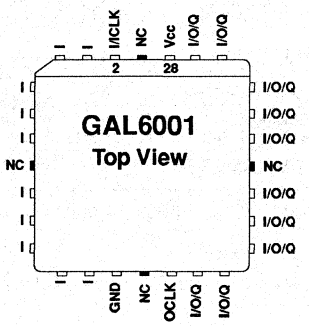
ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

PIN NAMES

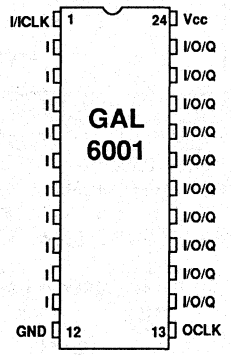
I_0 - I_{10}	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V_{CC}	POWER (+5)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN DIAGRAM

Chip Carrier



DIP



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LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon U.S.A.
Tel. (503) 681-0118 or 1-800-FAST GAL; FAX (503) 681-3037

March 1990

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} .....–.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

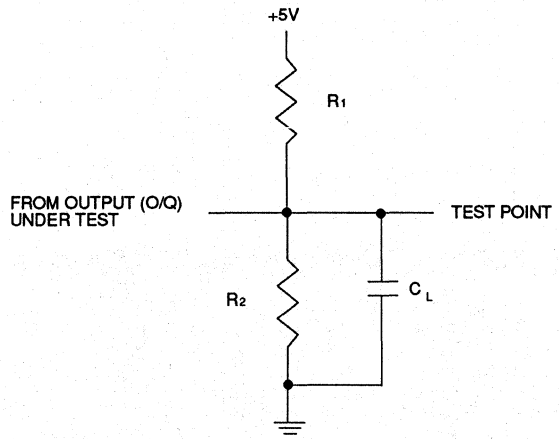
COMMERCIAL		INDUSTRIAL		MILITARY	
R_1	R_2	R_1	R_2	R_1	R_2
300	390	300	390	390	750

AC Test Conditions:

Cond. 1) R_1 per table; C_L = 50pF; R_2 per above table

Cond. 2) Active High $R_1 = \infty$; Active Low R_1 per table; C_L = 50pF; R_2 per above table

Cond. 3) Active High $R_1 = \infty$; Active Low R_1 per table; C_L = 5pF; R_2 per above table



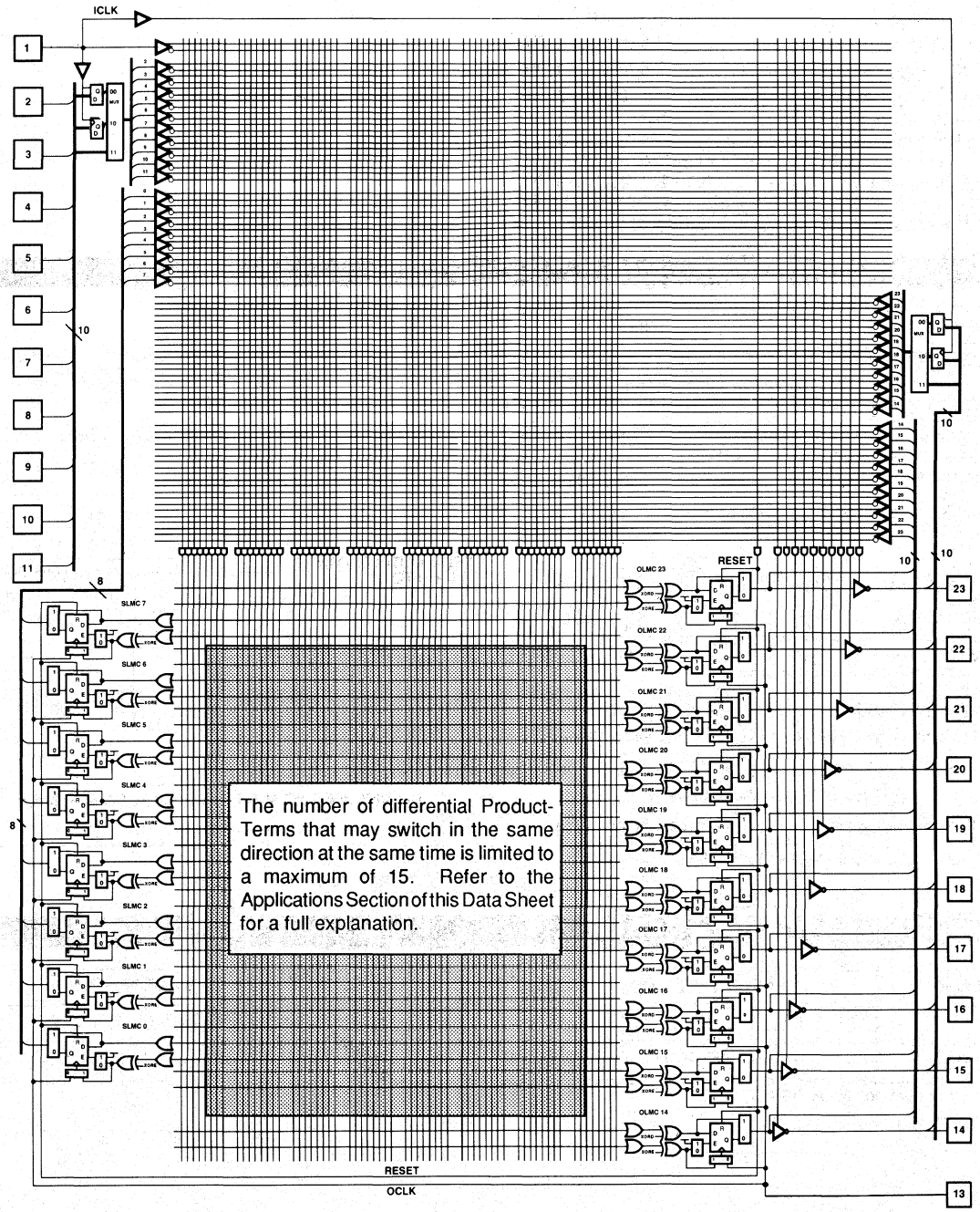
CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

GAL6001 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS — GAL6001-30 Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

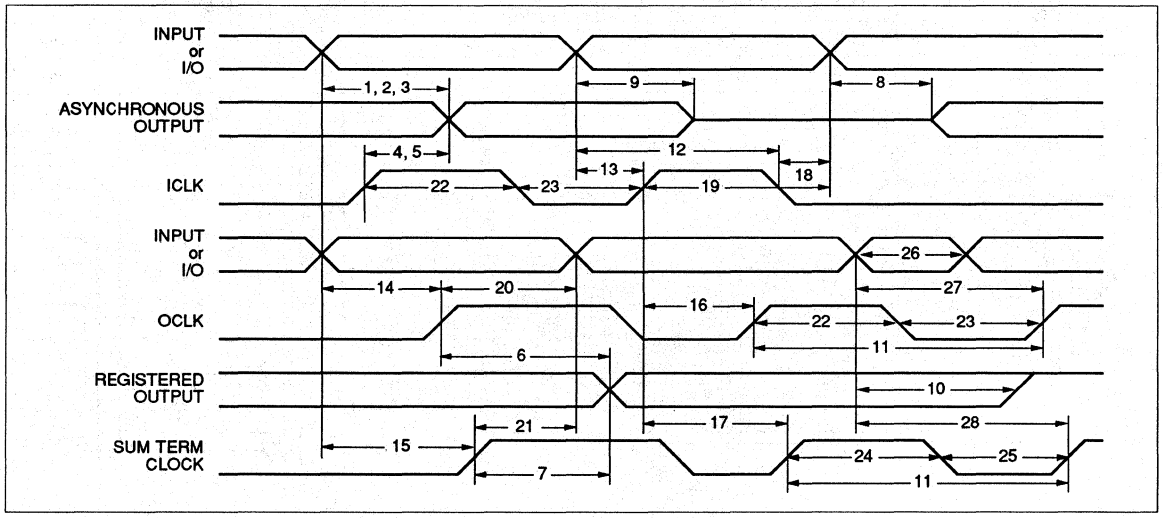
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–130	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	150	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL6001-30 Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS — GAL6001-30 Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I	O	ILMC = Async, OLMC = Combinational	1	—	30	ns
	2	O, Q	O	Feedback → O, OLMC = Combinational	1	—	30	ns
	3	I	O	ILMC = Latch, OLMC = Combinational	1	—	35	ns
t_{co}	4	ICLK ↑	O	ILMC = Reg, OLMC = Combinational	1	—	35	ns
	5	ICLK ↑	O	ILMC = Latch, OLMC = Combinational	1	—	35	ns
	6	OCLK ↑	Q	OLMC = D/E Reg	1	—	12	ns
	7	STCLK ↑	Q	OLMC = DReg STCLK	1	—	35	ns
t_{en}	8	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	25	ns
t_{dis}	9	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	25	ns
t_{res}	10	I, I/O	Q	Register Reset, Q → 1	1	—	35	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL6001-30 Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	11	Clock Frequency, OCLK or STCLK	—	0	27	MHz
t_{su}	12	Input Setup Time before ICLK ↓ , ILMC = Latch	—	2.5	—	ns
	13	Input Setup Time before ICLK ↑ , ILMC = Reg	—	2.5	—	ns
	14	Setup Time, input or feedback, before OCLK ↑ , OLMC = D/E Reg	—	25	—	ns
	15	Setup Time, input or feedback, before STCLK ↑ , OLMC = DReg STCLK	—	7.5	—	ns
	16	Setup Time, ICLK ↑, before OCLK ↑ , OLMC = D/E Reg	—	30	—	ns
	17	Setup Time, ICLK ↑ , before STCLK ↑ , OLMC = DReg STCLK	—	15	—	ns
t_h	18	Hold Time after ICLK ↓ , ILMC = Latch	—	5	—	ns
	19	Hold Time after ICLK ↑, ILMC = Reg	—	5	—	ns
	20	Hold Time after OCLK ↑ , OLMC = D/E Reg	—	-5	—	ns
	21	Hold Time after STCLK ↑, OLMC = DReg STCLK	—	10	—	ns
t_w	22	ICLK or OCLK pulse duration, high	—	10	—	ns
	23	ICLK or OCLK pulse duration, low	—	10	—	ns
	24	STCLK pulse duration, high	—	15	—	ns
	25	STCLK pulse duration, low	—	15	—	ns
	26	Reset pulse duration	—	15	—	ns
t_{rec}	27	Reset to OCLK Recovery Time	—	20	—	ns
	28	Reset to STCLK Recovery Time	—	10	—	ns

ELECTRICAL CHARACTERISTICS — GAL6001-35 Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

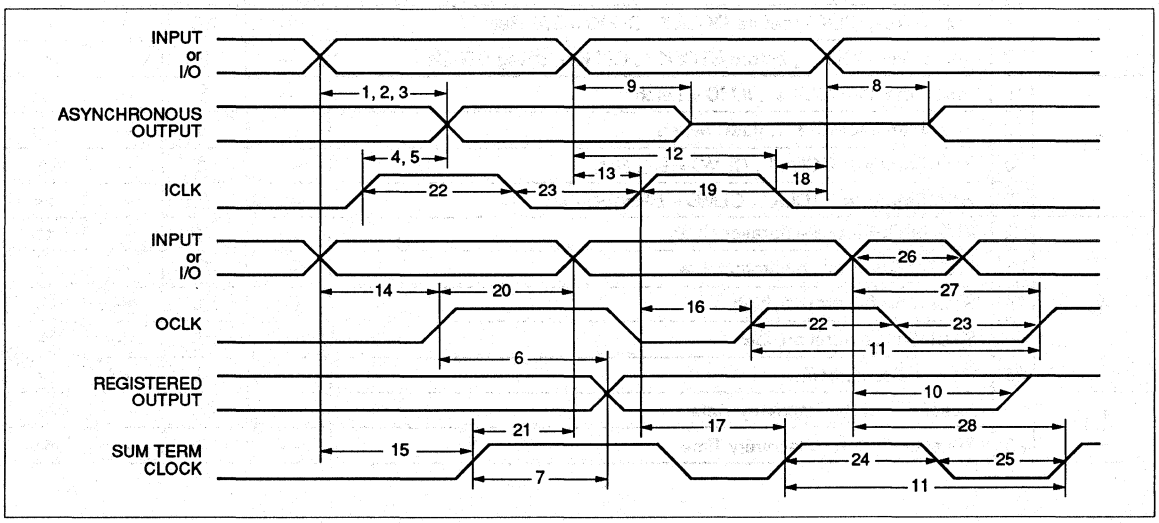
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–130	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	150	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL6001-35 Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS — GAL6001-35 Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I	O	ILMC = Async, OLMC = Combinational	1	—	35	ns
	2	O, Q	O	Feedback → O, OLMC = Combinational	1	—	35	ns
	3	I	O	ILMC = Latch, OLMC = Combinational	1	—	40	ns
t_{co}	4	ICLK ↑	O	ILMC = Reg, OLMC = Combinational	1	—	40	ns
	5	ICLK ↑	O	ILMC = Latch, OLMC = Combinational	1	—	40	ns
	6	OCLK ↑	Q	OLMC = D/E Reg	1	—	13.5	ns
	7	STCLK ↑	Q	OLMC = DReg STCLK	1	—	40	ns
t_{en}	8	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	30	ns
t_{dis}	9	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	30	ns
t_{res}	10	I, I/O	Q	Register Reset, Q → 1	1	—	35	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL6001-35 Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	11	Clock Frequency, OCLK or STCLK	—	0	22.9	MHz
t_{su}	12	Input Setup Time before ICLK ↓, ILMC = Latch	—	3.5	—	ns
	13	Input Setup Time before ICLK ↑, ILMC = Reg	—	3.5	—	ns
	14	Setup Time, input or feedback, before OCLK ↑, OLMC = D/E Reg	—	30	—	ns
	15	Setup Time, input or feedback, before STCLK ↑, OLMC = DReg STCLK	—	10	—	ns
	16	Setup Time, ICLK ↑, before OCLK ↑, OLMC = D/E Reg	—	35	—	ns
	17	Setup Time, ICLK ↑, before STCLK ↑, OLMC = DReg STCLK	—	17	—	ns
t_h	18	Hold Time after ICLK ↓, ILMC = Latch	—	5	—	ns
	19	Hold Time after ICLK ↑, ILMC = Reg	—	5	—	ns
	20	Hold Time after OCLK ↑, OLMC = D/E Reg	—	-5	—	ns
	21	Hold Time after STCLK ↑, OLMC = DReg STCLK	—	12.5	—	ns
t_w	22	ICLK or OCLK pulse duration, high	—	10	—	ns
	23	ICLK or OCLK pulse duration, low	—	10	—	ns
	24	STCLK pulse duration, high	—	15	—	ns
	25	STCLK pulse duration, low	—	15	—	ns
	26	Reset pulse duration	—	15	—	ns
t_{rec}	27	Reset to OCLK Recovery Time	—	20	—	ns
	28	Reset to STCLK Recovery Time	—	10	—	ns

INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL6001 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Configurable input blocks provide systems designers with unparalled design flexibility. With the GAL6001, external registers and latches are not necessary.

Both the ILMC and the IOLMC are block configurable. However, the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinational, "D-type register with sum term (asynchronous) clock", or "D/E-type register." Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the "D" XOR. Polarity selection is available for BLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all "E" sum terms is selected through the "E" XOR.

When the macrocell is configured as a "D/E type registered", the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with state hold functions.

When the macrocell is configured as a "D type register with a sum term clock", the register is always enabled and its "E" sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

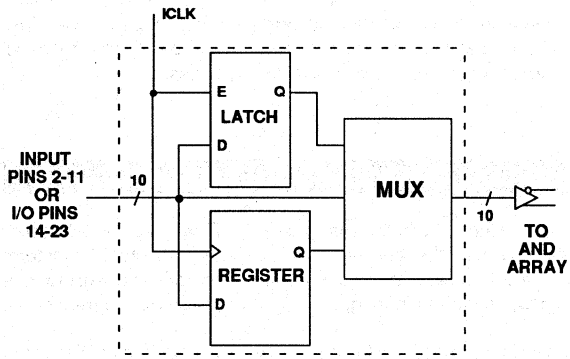
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. Registers are reset to a logic zero. If connected to an ouput pin, a logic one will occur because of the inverting output buffer.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer and always present). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried (the associated OLMC pin is an input), or dynamically buried with the use of the output enable product term.

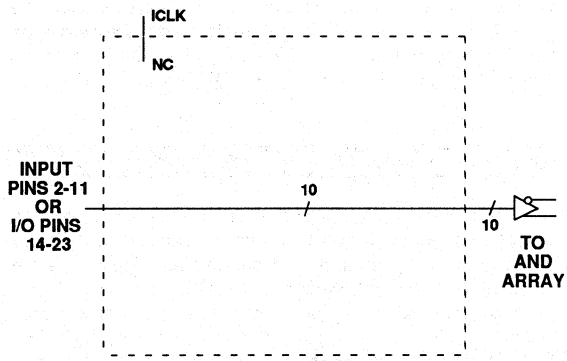
The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK-, or T-register.

The three macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

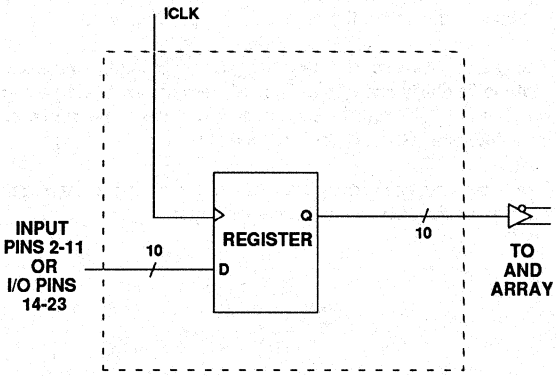
ILMC AND IOLMC CONFIGURATIONS



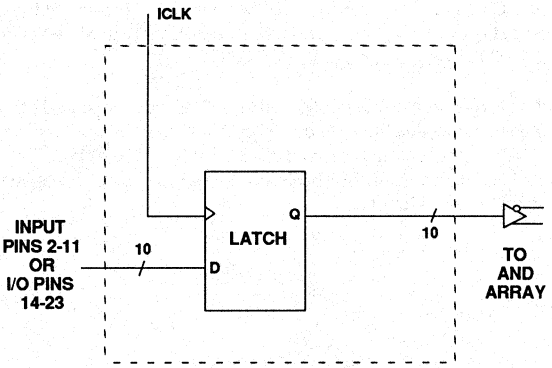
ILMC/IOLMC
Generic Block Diagram



Asynchronous Input

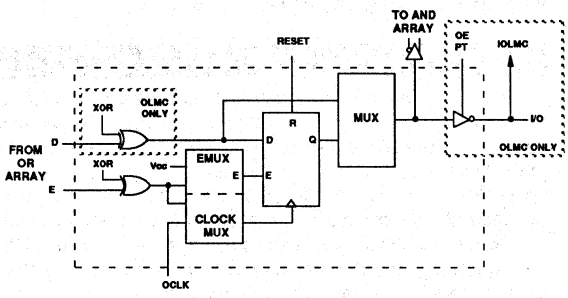


Registered Input

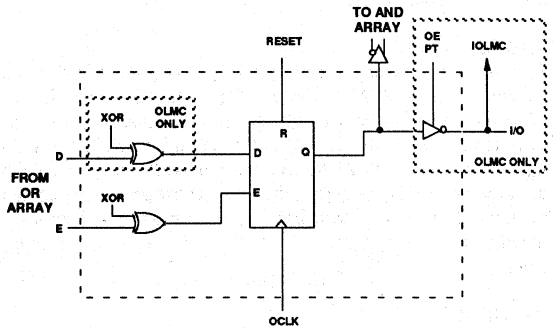


Latched Input

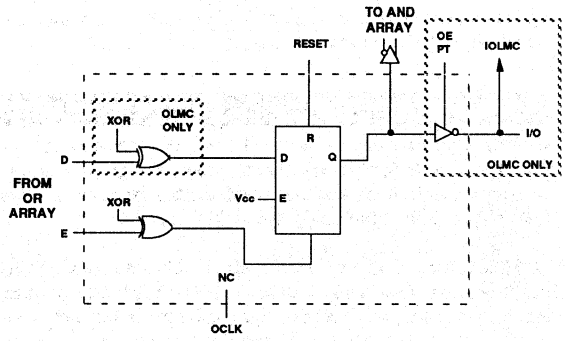
OLMC AND BLMC CONFIGURATIONS



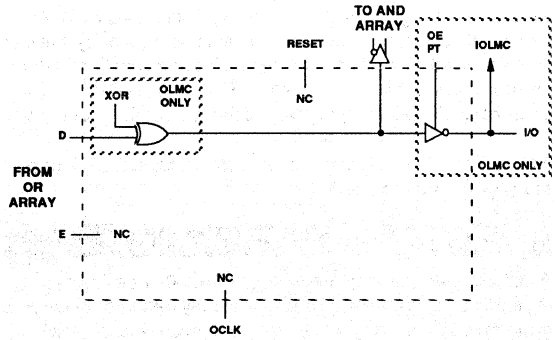
OLMC/BLMC
Generic Block Diagram



D/E Type Registered



D Type Register with Sum Term Asynchronous Clock



Combinational

ARRAY DESCRIPTION

The GAL6001 contains two E^2 reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complemented forms). 64 product terms serve as inputs to the OR array. There is a RESET PT; it generates the RESET signal described in the earlier discussion of Output and Buried Logic Macrocells. There are 10 output enables, thus allowing device pins 14-23 to be bi-directional or tri-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL6001 device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL6001 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND and OR array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6001 can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

LATCH-UP PROTECTION

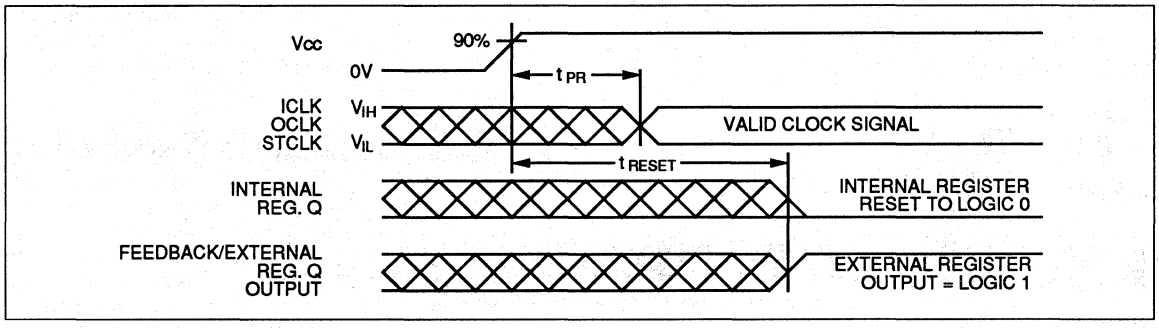
GAL6001 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-up instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL6001 devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

POWER-UP RESET



Circuitry within the GAL6001 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL6001. First, the Vcc rise must be monotonic. Second, the clock inputs must become a proper TTL level within the specified time (t_{PR}, 100µs). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS) APPLICATIONS

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

$$DPTS = \left| (P\text{-}Terms)_{LH} - (P\text{-}Terms)_{HL} \right|$$

DPTS restricts the number of product terms that can be switched simultaneously - there is no limit on the number of product terms that can be used.

A software utility is available from Lattice Applications Engineering that will perform this calculation on any GAL6001 JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice representative or by contacting Lattice Applications Engineering (Tel: 503-681-0118 or 800-FASTGAL; FAX: 681-3037).

Lattice Semiconductor Corporation™

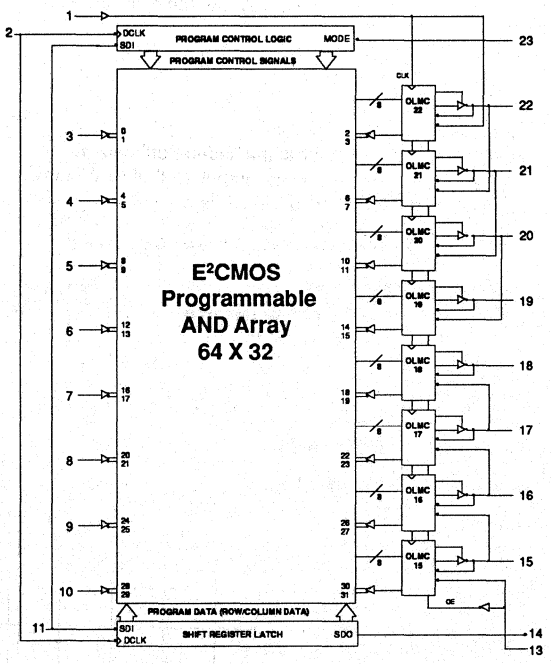
ispGAL16Z8

In-System Programmable Generic Array Logic™

FEATURES

- **IN-SYSTEM-PROGRAMMABLE — 5-VOLT ONLY**
  - **Change Logic "On the Fly" (in milliseconds)**
  - **Nonvolatile E² Technology**
- **DIAGNOSTICS MODE FOR CONTROLLABILITY AND OBSERVABILITY OF SYSTEM LOGIC**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **20 ns Maximum Propagation Delay**
  - **Fmax = 41.6 MHz**
  - **90mA MAX I_{cc}**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **Maximum Flexibility for Complex Logic Designs**
  - **Programmable Output Polarity**
  - **Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **100% Functional Testability**
- **24-PIN 300-MIL DIP, AND 28-LEAD PLCC PACKAGING**
- **MINIMUM 10,000 ERASE/WRITE CYCLES**
- **DATA RETENTION EXCEEDS 10 YEARS**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **APPLICATIONS INCLUDE:**
  - **Reconfigurable Interfaces and Decoders**
  - **Copy Protection and Security Schemes**
  - **"Soft" Hardware (Generic Systems)**
  - **RFT™ (Reconfiguration For Test)**
  - **Proprietary Hardware/Software Interlocks**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

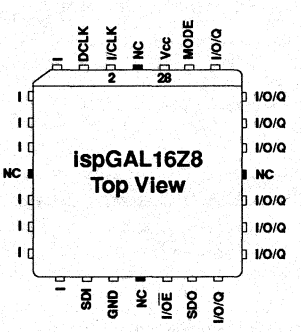
The Lattice ispGAL®16Z8 is a revolutionary programmable logic device featuring 5-volt only in-system programmablitiy and real time, in-system diagnostic capabilities. This is made possible by on-chip circuitry which generates and shapes the necessary high voltage internal programming control signals. Using Lattice's proprietary UltraMOS® technology, this device provides true bipolar performance at significantly reduced power levels.

The 24-pin ispGAL16Z8 is architecturally and parametrically identical to the 20-pin GAL®16V8, but includes 4 extra pins to control in-system programming. These extra pins are: data clock (DCLK), serial data in (SDI), serial data out (SDO), and mode control (MODE). These pins are not associated with normal logic functions and are typically used for programming and for diagnostics. Additionally, this 4-pin interface allows an unlimited number of devices to be cascaded to form a serial programming and diagnostics loop.

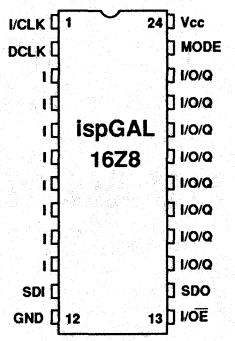
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of the GAL devices . A security circuit is built-in, providing proprietary designs with copy protection.

PIN DIAGRAMS

Chip Carrier



DIP



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LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037

April 1990

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress-only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

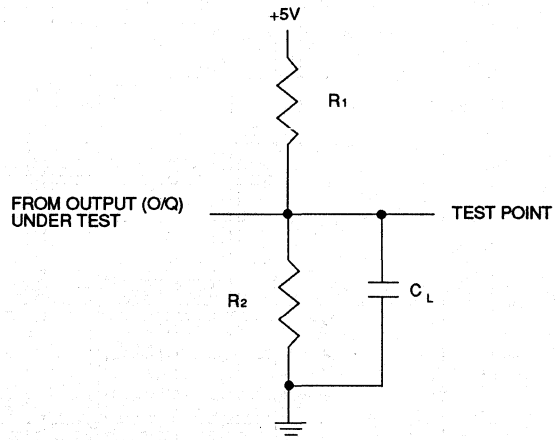
COMMERCIAL		INDUSTRIAL		MILITARY	
R_1	R_2	R_1	R_2	R_1	R_2
200	390	200	390	390	750

AC Test Conditions:

Cond. 1) R_1 per table; C_L = 50pF; R_2 per above table

Cond. 2) Active High R_1 = ∞; Active Low R_1 per table; C_L = 50pF; R_2 per above table

Cond. 3) Active High R_1 = ∞; Active Low R_1 per table; C_L = 5pF; R_2 per above table



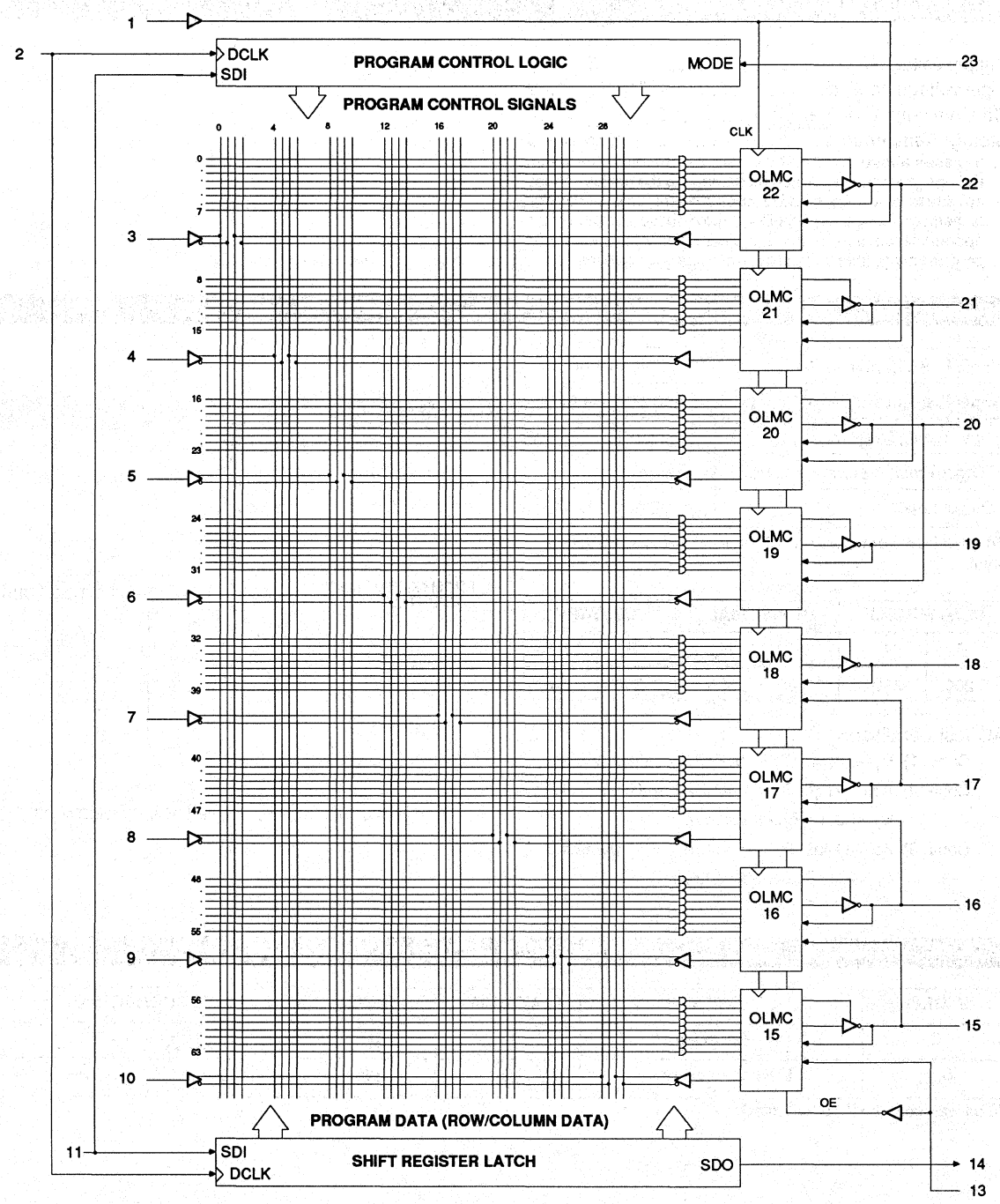
CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

ispGAL16Z8 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS — ispGAL16Z8-20L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	90	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-20L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — ispGAL16Z8-20L Commercial

Over Recommended Operating Conditions

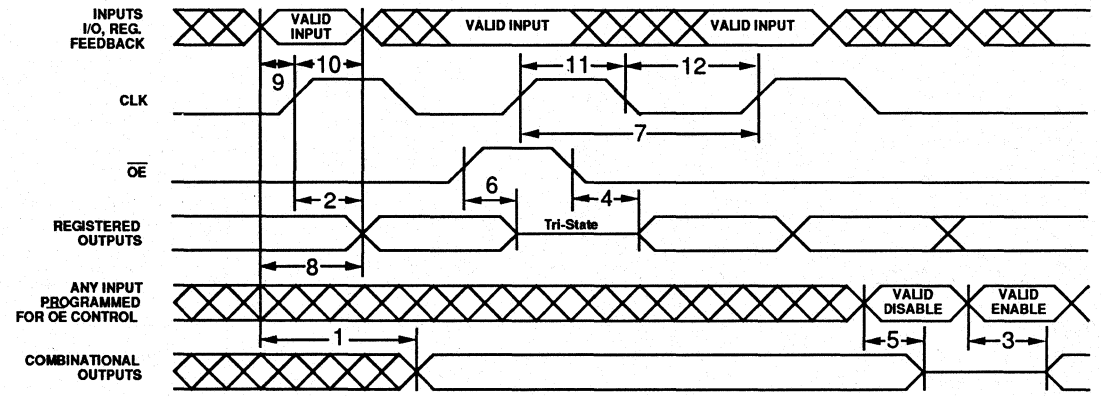
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

AC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-20L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	41.6	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	33.3	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	12	—	ns
	12	Clock Pulse Duration, Low[2]	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — ispGAL16Z8-25L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	90	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-25L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — ispGAL16Z8-25L Commercial

Over Recommended Operating Conditions

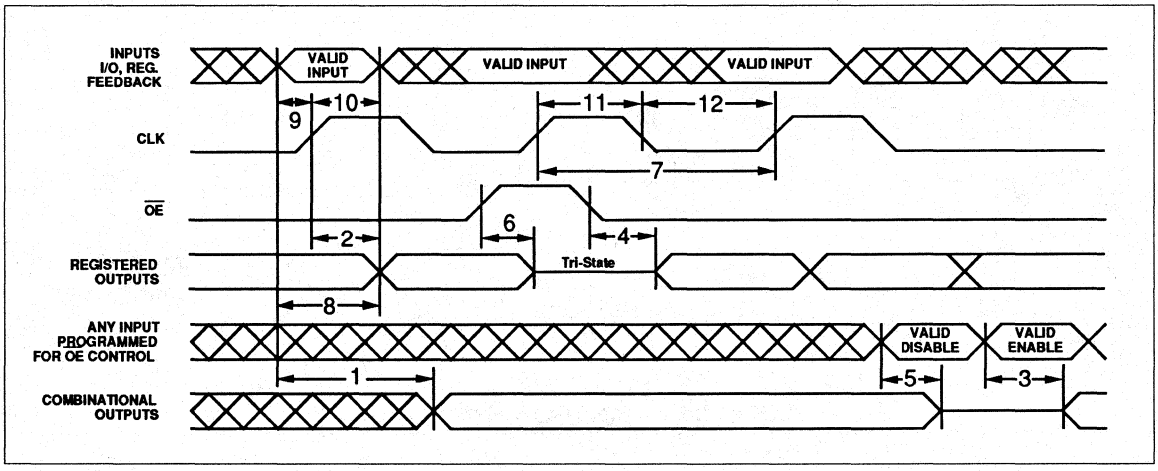
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

AC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-25L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	33.3	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	28.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	20	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	15	—	ns
	12	Clock Pulse Duration, Low[2]	—	15	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



OUTPUT LOGIC MACROCELL (OLMC)

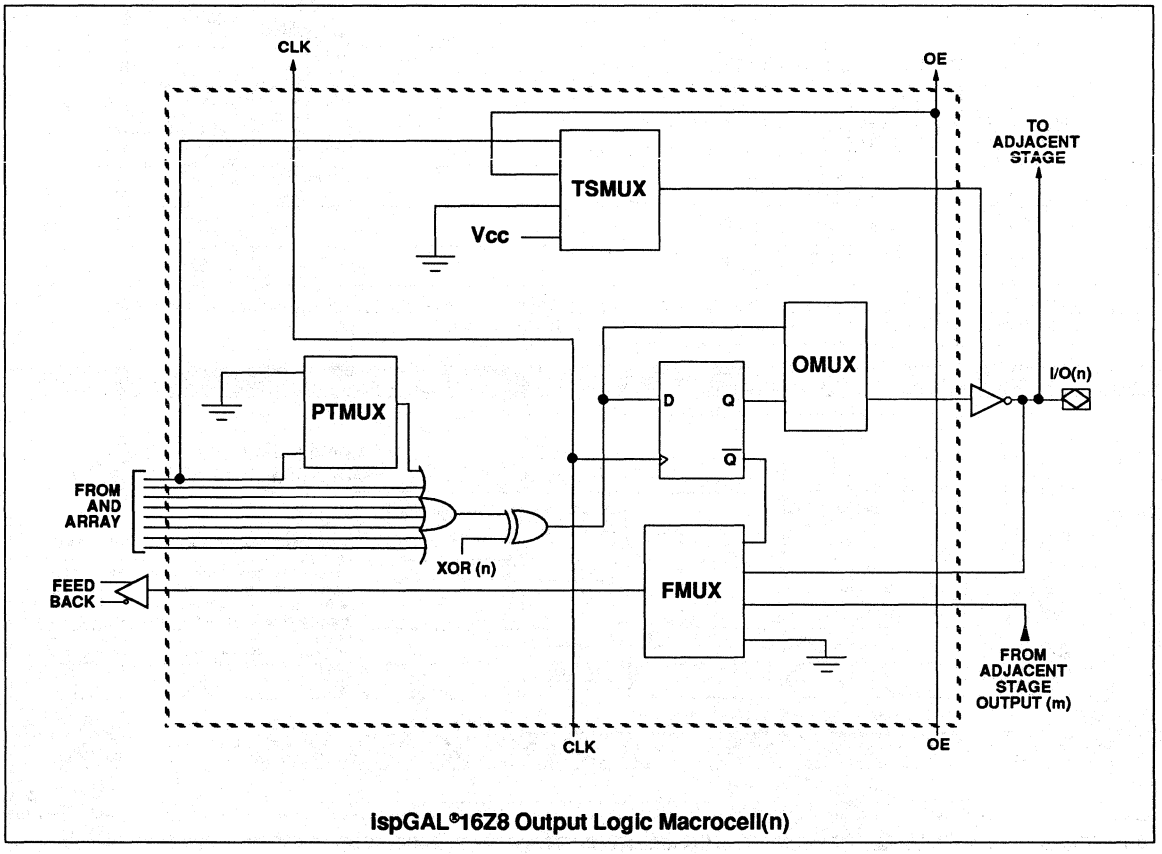
The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

NOTE: See ispGAL16Z8 Programmer's Guide for additional information on in-system OLMC reconfiguration.

There are three OLMC configuration modes possible: registered, complex, and simple. These are illustrated in the diagrams on the following pages. You cannot mix modes, either all OLMCs are simple, complex, or registered (in registered mode the output can be combinational or registered).

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable is connected to all registered outputs; or a product term can be used to provide individual output enable control for combinational outputs in the registered mode or combinational outputs in the complex mode. There is no output enable control in the small mode. The output logic macrocell provides the designer with maximum output flexibility in matching signal requirements, thus providing more functionality than possible with existing 20-pin PAL® devices.

The six valid macrocell configurations, two configurations per mode, are shown in each of the macrocell equivalent diagrams. Pin and macrocell functions are detailed in the following diagrams.



ispGAL®16Z8 Output Logic Macrocell(n)

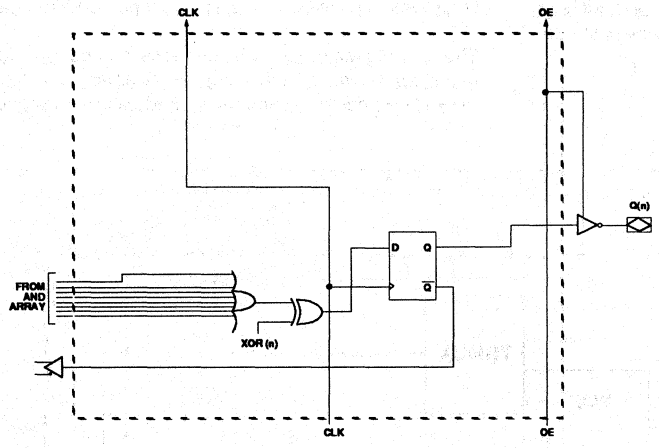
REGISTERED MODE

In the Registered architecture mode macrocells are configured as dedicated, registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

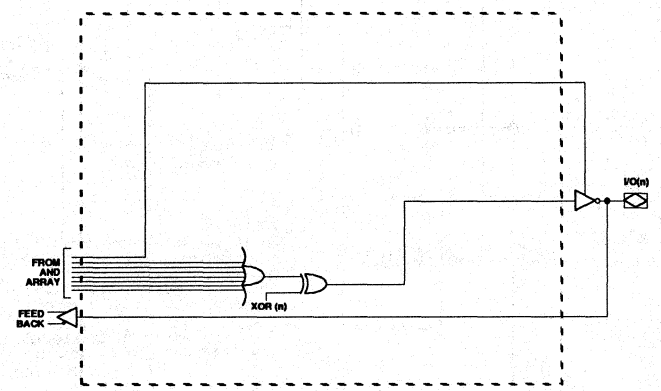
All registered macrocells share common clock and $\overline{OE}$ control pins. Any macrocell can be configured as registered or I/O. Up to 8 registers or up to 8 I/O's are possible in this mode. Dedicated input or output functions can be implemented as sub-sets of the I/O function.

Registered outputs have 8 data product terms per output. I/O's have 7 data product terms per output.



Registered Output with Programmable Polarity

NOTES:
- All macrocells can be individually configured to this function.
- Polarity of the register input is programmable on a macrocell by macrocell basis.
- Feedback into the AND array is from the $\overline{Q}$ signal of the register with active low and active high feedback paths provided.
- Registered macrocells have common clock (pin 1) and common $\overline{OE}$ (pin 13)



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- All macrocells can be individually configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- All macrocells have active high and active low feedback of the output buffer and/or device pin data into the AND array.
- When all 8 macrocells are configured into the I/O function the CLK and $\overline{OE}$ pins serve no valid logic function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

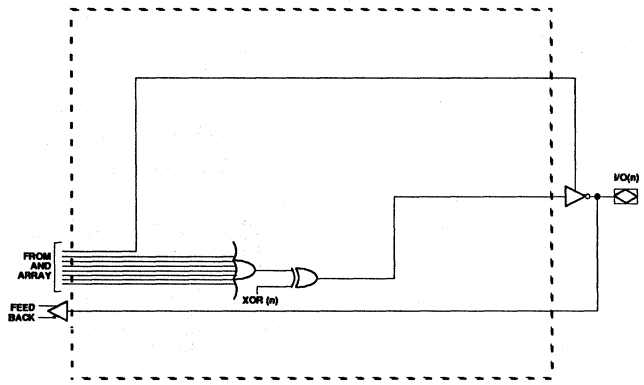
COMPLEX MODE

In the Complex architecture mode macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

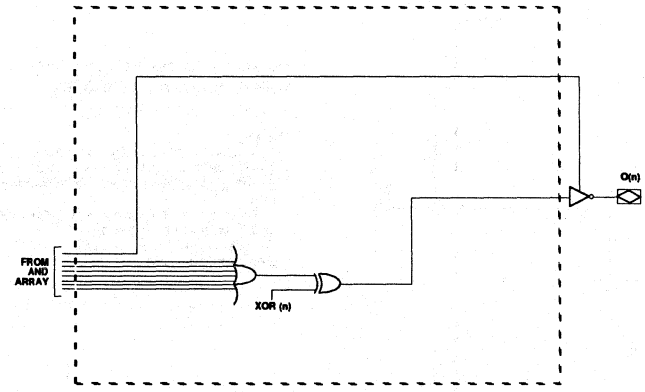
Up to 6 I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as sub-sets of the I/O function. The two "outboard" macrocells do not have input capability. Designs requiring 8 I/O's can be implemented in the Registered mode.

All macrocells have 7 data product terms per output. One product term is used for programmable OE control. Pins 1 and 13 are always available as data inputs into the AND array.



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- The outer most macrocells (pins 15 & 22) cannot perform this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- Each macrocell has active high and active low feedback of the output buffer and/or device pin data into the AND array.



Combinational Output with Programmable OE and Polarity

NOTES:
- The two outer most macrocells (pins 15 & 22) are permanently configured to this function when in the Complex mode.
- The other 6 macrocells can emulate this mode by not using the feedback data as a data input to the array.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

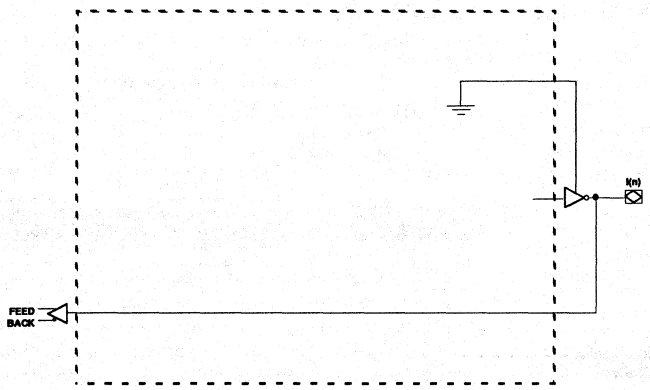
SIMPLE MODE

In the Simple architecture mode pins are configured as dedicated inputs or as dedicated, always active, combinational outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 16P6 devices with many permutations of generic polarity output or input choices.

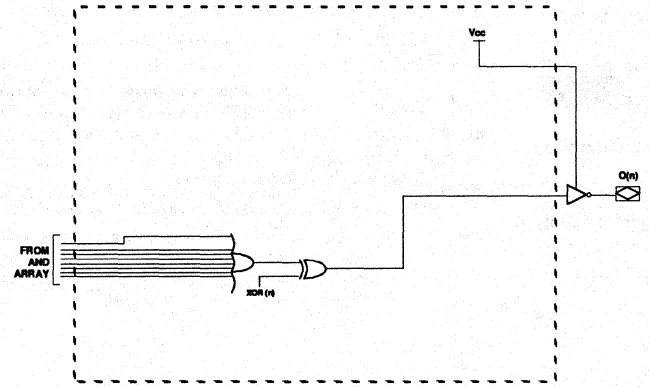
All ouputs are associated with 8 data product terms. In addition, each output has programmable polarity.

Pins 1 and 13 are always available as data inputs into the AND array. The "center" two macrocells (pins 15 &16) cannot be used in the input configuration.



Dedicated Input Mode

NOTES:
- The "center" two macrocells (18 & 19) cannot be configured to this function.



Dedicated Combinational Output with Programmable Polarity

NOTES:
- All Macrocells can be configured to this function. The "center" macrocells (pins 18 & 19) can only be configured to this function when in the Simple mode.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- The outputs can also be permanently programmed tri-stated.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every ispGAL16Z8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

TC CELL

The ispGAL16Z8 is equipped with a TC (Tri-state Control) cell which allows output driver state control during in-system programming and/or diagnostic mode. In the default setting (logic 1), this cell causes the output state (logic 1, logic 0, or tri-state) to be latched upon entering the programming/diagnostic mode. In the tri-state setting (logic 0), this cell causes all outputs to tri-state upon entering the programming/diagnostic mode.

NOTE: Refer to the ispGAL16Z8 Programmers Guide for additional information on TC cell programming and functionality.

SECURITY CELL

A security cell is provided with every ispGAL16Z8 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased.

NOTE: Refer to the ispGAL16Z8 Programmers Guide for additional information on the Bulk Erase procedure.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break any feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next-state conditions.

The ispGAL16Z8 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any desired state condition can be forced for test sequencing.

NOTE: Refer to the ispGAL16Z8 Programmers Guide for additional information on registered oriented diagnostic preload.

LATCH-UP PROTECTION

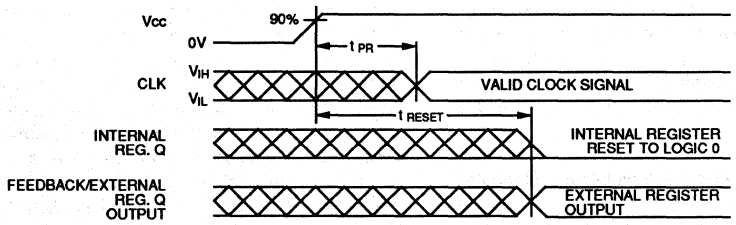
ispGAL16Z8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

ispGAL16Z8 devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, require much less drive current than traditional bipolar devices. This allows for a greater fan out from the driving logic.

ispGAL16Z8 devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

POWER-UP RESET



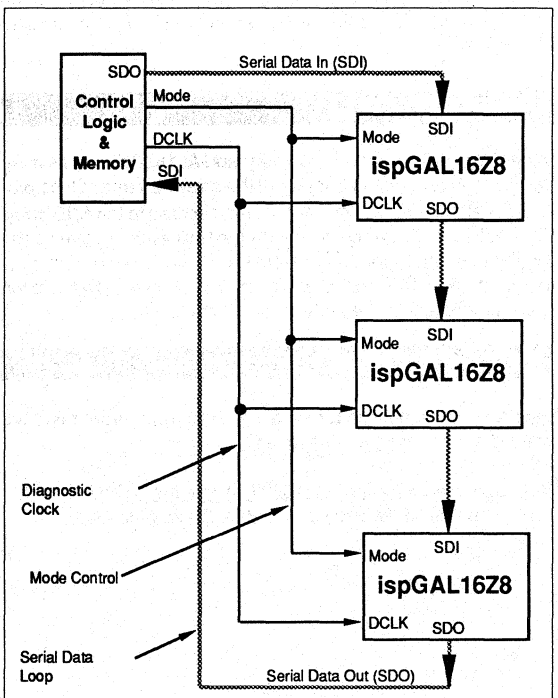
Circuitry within the ispGAL16Z8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the ispGAL16Z8. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

SERIAL PROGRAMMING: LOOP OPERATION

The following figure illustrates a simplified block diagram of a microprocessor system containing three (3) ispGAL16Z8 devices. These devices have been "daisy chained" together to form a serial programming/diagnostic loop. In this configuration, the data bit rate and the DCLK clock frequency are the same. A programming and/or diagnostic bit stream may be shifted through all three (3) devices at the maximum DCLK clock frequency. The ispGAL16Z8 data cells are not dynamic. In other words, there is no minimum DCLK clock frequency.

In this configuration, only four (4) wires are required to access and control an unlimited number of devices. All the functions associated with reprogrammable logic devices are available via this 4-wire interface. An important benefit offered by the ispGAL16Z8 is RFT (Reconfiguration For Test) capability. RFT is a concept pioneered and developed by Lattice Semiconductor. RFT, in brief, is the process of reprogramming Lattice ispGAL devices, in-circuit, to serve as on-board diagnostic test vector drivers and/or receivers. Any pin associated with an OLMC (Output Logic Macrocell) can be configured via the 4-wire serial interface to serve as an output or an input. Elementary test vector sequencing or driver/receiver control can be achieved by patterning portions of the ispGAL16Z8 to serve as a micro-control state-machine.



Typical ispGAL16Z8 Daisy Chain

ispGAL16Z8 PROGRAMMERS GUIDE

The ispGAL16Z8 Programmers Guide contains complete information on the use of the serial programming and diagnostic capability of the ispGAL16Z8 device. The information provided in this datasheet is insufficient to properly design circuitry to control the device. The information is presented here only for reference and conceptual design evaluation. The guide can be requested from the Applications Engineering department at the factory.

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MILITARY PRODUCT INDEX

FAMILY	tpd (ns)	fmax (MHz)	Icc (mA)	MIL-STD-883C QUALIFIED	STANDARD MILITARY DRAWING NUMBER	PACKAGE	PAGE #
GAL16V8A	15	50	130	YES	5962-8983903RA	20-Pin CerDIP	32
	20	41.7	130	YES	5962-8983902RA		34
	20	41.7	65	*	TBA		36
	30	33.3	130	*	5962-8983901RA		*
GAL20V8A	15	50	130	YES	5962-8984003LA	24-Pin CerDIP	32
	20	41.7	130	YES	5962-8984002LA		34
	20	41.7	65	*	TBA		36
	30	33.3	130	*	5962-8984001LA		*
GAL18V10	15	62.5	135	*	*	24-Pin CerDIP	62
	20	33.3	135	*	*		64
GAL22V10	15	62.5	150	YES	5962-8984103LA	24-Pin CerDIP	62
	20	33.3	150	YES	5962-8984102LA		64
	30	25	150	*	5962-8984101LA		*
GAL26CV12	15	62.5	150	*	*	28-Pin CerDIP	62
	20	33.3	150	*	*		64
GAL20RA10	20	41.7	120	*	*	24-Pin CerDIP	80

* Contact Lattice (1-800 FASTGAL) for additional information.

GAL MILITARY PROGRAM

CORPORATE PHILOSOPHY

Lattice Semiconductor is committed to leadership in performance and quality. Our family of military GAL devices is consistant with this philosophy. Lattice manufactures all devices under strict Quality Assurance guidelines. All grades, Commercial thru Military 883C are monitored under a Quality program conformant to MIL-M-38510 Appendix A with inspections conformant to MIL-I-45208A.

Lattice Semiconductor has manufactured millions of GAL devices over the last half decade. The engineering analysis and characterization during this time has been focused into our current design, process and manufacturing test procedures to assure superior product meeting all datasheet and quality goals.

Complete review of the procedures and technical data can be arranged at our facility near Portland, Oregon. Factory audits of our documentation and processes are also welcomed.

QUALITY AND TESTABILITY

Lattice Semiconductor processes its GAL devices to strict conformance with MIL-STD-883C Class B. The inherent testability and quality advantages of E²CMOS® technology used in the design and manufacture of GAL devices allow Lattice to achieve superior levels of screening.

All GAL devices are patterned dozens of times throughout the manufacturing flow to test for device performance under worst case configurations using the same E^2 cell array that will be used for your final patterning of the devices. This "100% actual test" philosophy does away with the correlated and simulated testing that is necessary with bipolar and UV (EPROM) based PLD devices.

Complete details of the methodologies used, the quality gains, and the cost savings obtained with this test philosophy can be found in the GAL Handbook, available from your local Lattice Sales Representative.

RELIABILITY

Lattice Semiconductor performs extensive reliability testing prior to product release. This testing continues in the form of Reliability Monitors that are run on an ongoing basis to assure continued process integrity. A formal, written report of these test results is updated regularly and can be obtained from your local Lattice Sales Representative.

The reliability testing performed includes extensive analysis of fundamental design and process integrity. The reprogrammable nature of GAL devices allows for an inherently more thorough reliability evaluation than other programmable alternatives.

MIL-STD-883C

MIL–STD–883C is a procedure defined by RADC specifying a series of environmental, mechanical and electrical test methods that are aimed at providing uniform manufacturing screening and outgoing test requirements for military microcircuits. Lattice devices are processed to Class B. Table I summarizes the MIL–STD–883C, Class B flow.

MIL-M-38510

MIL–M–38510, when used in conjunction with MIL–STD–883C, defines design, packaging, material, marking, sampling, qualification and Quality System requirements for non-JAN devices. Table II summarizes the conformance testing required by MIL–STD–883C, Method 5005 for quality conformance testing of Lattice military microcircuits.

GROUP DATA

Group A and B data is taken on every inspection lot per the MIL-STD-883C, Class B requirements. This data, along with Generic Group C and D data, can be supplied, upon written request, for each shipment. Your Lattice Sales Representative can advise you of charges and leadtime necessary for this data collection.

STANDARD MILITARY DRAWINGS

Lattice actively supports the Standard Military Drawing (SMD) Program. The SMD Program offers a cost effective alternative to source control drawings. The Program provides a standardization of MIL-STD-883C product specifications. SMDs are available from participating manufacturers.

Standard Military Drawings are available for most of Lattice's MIL-STD-883C qualified GAL devices. Your local Lattice Sales Representative can advise you on the status of these drawings.

MILITARY SCREENING FLOW (TABLE I)

Screen	Method	Requirement
Internal Visual	2010 Cond. B	100%
Temp. Cycling	1010 Cond. C	100%
Constant Acceleration	2001 Cond. E	100%
Hermeticity Fine Gross	1014 Cond. A or B Cond. C	100%
Endurance Test	1033	100%
Retention Test	Unbiased Bake 48 HRS. TA = 150°C	100%
Pre Burn-In Electrical	Applicable Device Specification Tc = 25°C	100%
Dynamic Burn-In	1015 Cond. D	100%
Post Burn-In Electrical	Applicable Device Specification Tc = 25°C PDA = 5%	100%
Final Electrical Test	Applicable Device Specification Tc = 125°C	100%
Final Electrical Test	Applicable Device Specification Tc = - 55°C	100%
External Visual	2009	100%
QCI Sample Selection	MIL-M-38510H Sec. 4.5 and MIL-STD-883C Sec. 1.2	Sample

MILITARY QUALITY CONFORMANCE INSPECTIONS (TABLE II)

Subgroup	Method	Sample
GROUP A: Electrical Tests		
Subgroups 1, 7, 9	Applicable Device Spec.	116(0)
Electrical Test	25°C	
Subgroups 2, 8A, 10	Applicable Device Spec.	116(0)
Electrical Test	Max. Operating Temp.	
Subgroups 3, 8B, 11	Applicable Device Spec.	116(0)
Electrical Test	Min. Operating Temp.	
GROUP B: Mechanical Tests		
Subgroup 2		4(0)
Solvent Resistance	2015	
Subgroup 3		LTPD = 10
Solderability	2003	
Subgroup 5		LTPD = 15
Bond Strength	2011	
GROUP C: Chip Integrity Tests		
Subgroup 1		
Dynamic Life Test	1005, 1,000 HRS. 125°C	LTPD = 5
End Point Electrical	Applicable Device Spec.	
Subgroup 2		
Unbiased Retention	1,000 HRS. 150°C	LTPD = 5
End Point Electrical	Applicable Device Spec.	
GROUP D: Environmental Integrity		
Subgroup 1		LTPD = 15
Physical Dimensions	2016	
Subgroup 2		LTPD = 15
Lead Integrity	2004, Cond. B	
Hermeticity	1014	
Subgroup 3		LTPD = 15
Thermal Shock	1011, Cond. B, 15 Cycles	
Temp. Cycle	1010, Cond. C, 100 Cycles	
Moisture Resistance	1004	
Hermeticity	1014	
Visual Examination	1004, 1010	
Endpoint Electrical	Applicable Device Spec.	
Subgroup 4		LTPD = 15
Mechanical Shock	2002, Cond. B	
Vibration	2007, Cond. A	
Constant Acceleration	2001, Cond. E	
Hermeticity	1014	
Visual Examination	1010, 1011	
Endpoint Electrical	Applicable Device Spec.	
Subgroup 5		LTPD = 15
Salt Atmoshpere	1009, Cond. A	
Hermeticity	1014	
Visual Examination	1009	
Subgroup 6		3(0)
Internal Water Vapor	1018 < 5,000 PPM, 100°C	
Subgroup 7		LTPD = 15
Lead Finish Adhesion	2025	
Subgroup 8		5(0)
Lid Torque	2024	

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GAL QUALITY AND RELIABILITY

INTRODUCTION

There are many considerations to be made when choosing a PLD. Issues such as technology, quality, reliability and yields must be considered in addition to the device architecture and cost. The growing acceptance of the high performance CMOS processes such as the UltraMOS®-III E²CMOS® technology used in GAL® devices show dramatic gains over previous bipolar and UV EPROM devices.

The three sections of this chapter will help build a foundation upon which these decisions can be made. First will be an overview of the testing needs of PLDs and their impact on a technology choice. Second will be a technology and reliability overview to provide some background on Lattice's application of testability to the GAL device family. And finally, a brief look at a concept know as "System Cost" where the actual cost of design and manufacturing implementation for various technologies will be compared.

TESTABILITY

ACTUAL TEST VS. SIMULATED TEST

Why is "actual test" so significant? PLDs, unlike most other semiconductor devices, have a programmable element that determines the final device functionality and AC/DC performance. These programmable elements can be fabricated from metal link fuses, programmable diodes or transistors, volatile static RAM cells, UV EPROM cells or electrically erasable EEPROM cells. Each of these technologies carries a different variability of programming success and a variance in the impact of the programming success on the performance and reliability of the device.

The most common programmable elements are the metal fuse, EPROM cell and EEPROM cell. Of these element types, only the EEPROM cell can be thoroughly tested by the manufacturer prior to shipment to an end user OEM.

EEPROM ALLOWS ACTUAL TEST

Each of the methods identified above can be programmed. In this manner they are all the same. The differences become apparent when the erase times are analyzed. Metal link and One-Time Programmable (OTP) devices cannot be erased. UV E-PROM devices can be erased, however the time required is 20-30 minutes (and an expensive windowed package). EEPROM devices, on the other hand, offer instant erasability on the order of 50 mS (thousandth's of a second). The advantage of this instant erase for manufacturing test is significant. Instant erase allows instant re-patterning for additional testing.

EEPROM technology has been used for PLD manufacturing by Lattice for more than half a decade. Lattice refers to their high performance EEPROM technology as E²CMOS technology. Extensive reliability studies of the technology have been performed with industry-wide acceptance, including the military.

OTHER METHODS ARE IMPRECISE

All PLD devices must be tested to some degree to validate functionality and performance. Technologies that are not erasable or offer lengthy erase times severely constrain the test flexibility. Since the normal "user" programmable elements cannot be programmed during manufacture (all elements must be available for end-user programming) the manufacturers resort to using simulated and correlated performance of test rows, test columns and phantom or dummy-test arrays. At best, this is a statistical measure of the actual device performance. One needs only to look at the "normal" programming yield fallout of 0.5 → 3% or the "acceptable" post-programming test vector & board yield fallout of 0.5 → 2% to know that this correlation is weak. The quality systems of today are measuring defects in the parts per million (PPM). A six sigma program requires less than 3.4 PPM, four orders of magnitude less than that achievable with non-testable PLDs.

ACTUAL MATRIX PATTERNING

The unique capability of E²CMOS devices to be instantly electrically erased allows these devices to be patterned multiple times during Lattice's manufacturing test. Normal array cells in the programmable matrix are patterned, erased & tested again and again. The test rows or columns, phantom arrays, etc., that are used with other technologies are not necessary with E²CMOS devices. Programmability of every cell is checked dozens of times.

Historically the checking of a successful programming operation consisted of no more than a pass/fail verification step. This digital, black/white style check is not adequate to assure that the cell programmed properly with sufficient margin to guarantee long-term reliable performance of the device. E²CMOS devices have an additional cell verification step that consists of an analog measure (to millivolt accuracy) of the actual charge stored on the cell. This data is used for extensive reliability and quality measurements and testing.

WORST CASE AC/DC TESTING

A PLD does not have a defined function until the engineer patterns the device with his custom pattern. The manufacturer, when considering the testing of a PLD, must consider the hundreds of different architecture and functional variations that can be created by the end user. Each configuration of architecture brings on a different set of worst case pattern and stimulus conditions. Quick application of a series of worst case patterns that cover all of the permutations of input combinations, array load & switching, and output configuration is required.

E²CMOS devices offer instant erasability to address this reconfiguration & test problem. Testing each additional worst case configuration takes fractions of a second, allowing dozens of patterns to be checked to assure performance to rated speeds even under the most grueling AC pattern. The final result is a device with defects reduced from PPH (parts per hundred) to PPM (parts per million).

TECHNOLOGY & RELIABILITY

Lattice maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, data is continuously accumulated through monitor programs so as to further drive failure rates down. Each product's qualification plan is generated in conformance to Lattice's Qualification Policy with failure analysis in conformance to Lattice's Failure Analysis Procedures. Both documents are contained in Lattice's Quality Assurance Manual, which can be obtained upon request. Failure rates in this reliability summary are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

PROCESS OVERVIEW

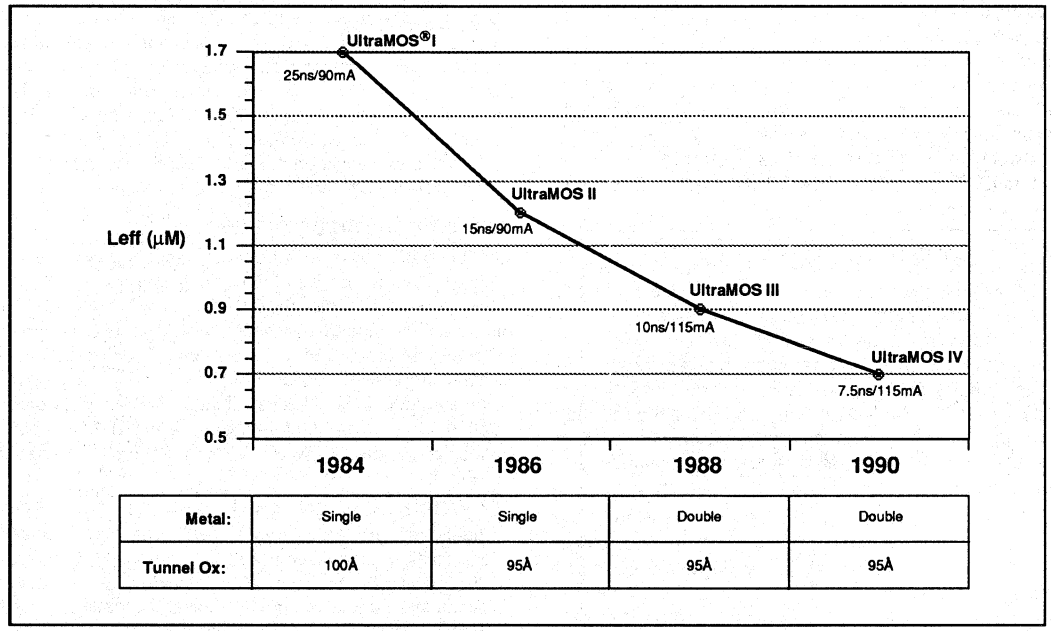
Lattice Semiconductor is using the third generation of its advanced UltraMOS® process for most of its current manufacturing (Figure 1). Our fourth generation process is in development with products expected to be sampling on this process in the near future. The primary difference between UltraMOS III and its predecessor, UltraMOS II, is the addition of a second layer of metalization. The second level of metalization is used to improve signal routing density in the logic circuitry as well as improve speed by strapping the poly word lines in the programmable array.

BASIC THEORY OF OPERATION

An E²CMOS cell is built around a MOS transistor with a floating gate which is externally charged or discharged by a small programming current. If the floating gate is charged up to a positive potential by removing electrons from the floating gate, the cell transistor is turned on, storing a binary zero in the cell. If the floating gate is charged to a negative potential by placing electrons on the floating gate, the transistor is kept in the non-conducting or off state, which writes a binary one into the cell. In addition to the floating gate or sense device, an additional select transistor, or pass gate, is added in series with the cell to isolate it from the array during read and write operations. A schematic representation of this cell is shown in Figure 2.

The small halos in the source/drain regions of the sense device are used to indicate that this device does not have the conventional self aligned source/drain regions of a typical MOS device (see process technology, below). In addition to the conventional bit line and word line, the E²CMOS cell also has an additional line for the control gate, or top gate, which controls the potential of the floating gate.

The cell is programmed by applying a programming pulse to either the control gate or the bit line of a cell which has been selected by an applied high voltage on the word line. Programming takes place when electrons tunnel through the thin tunneling dielectric shown in the schematic by the small notch in the floating gate over the drain of the sense device. Before describing the detailed operation of the E²CMOS cell, the requirements and tradeoffs of the process technology will be reviewed.



Metal:	Single	Single	Double	Double
Tunnel Ox:	100Å	95Å	95Å	95Å

Figure 1

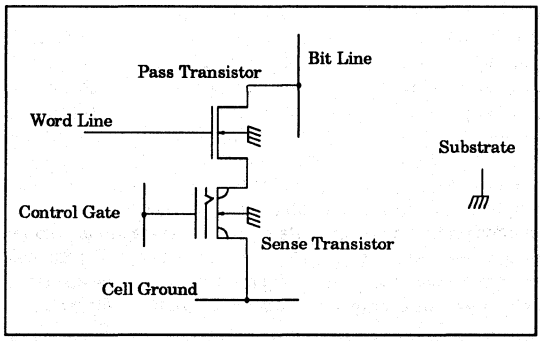


Figure 2

E²CMOS PROCESS TECHNOLOGY

Lattice's E²CMOS technology is based upon a highly successful combination of CMOS and NMOS technologies. The requirements for both on-chip high voltage and high speed devices put severe restrictions on the process technology. By incorporating both pumped substrate techniques and depletion devices from NMOS technology with low power CMOS devices, Lattice's E²CMOS technology maintains high performance while meeting the high voltage requirements of programming.

In addition to combining the techniques of both NMOS and CMOS, Lattice's E²CMOS technology incorporates an additional level of polysilicon to form the floating gate, as well as an ultra-clean, ultra-thin tunneling oxide approximately 100 Angstroms thick. A cross section of a typical E²CMOS cell is shown in Figure 3. Note that the sense transistor channel length is defined by a masking layer and not by the polysilicon gate as in the case of the select, or pass, transistor. This technique minimizes the size of the cell while maintaining a high coupling ratio between the floating gate and the control gate. As in the case of an EPROM cell, the E²CMOS cell requires a very low

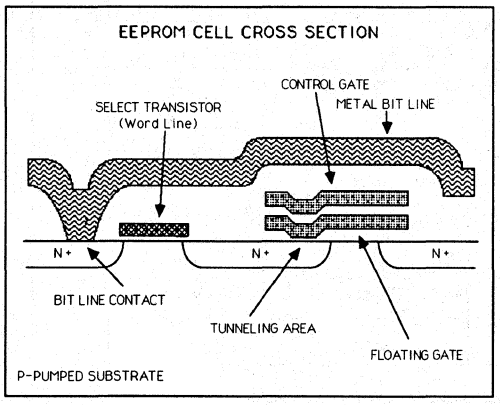


Figure 3

leakage, high quality oxide between the two levels of polysilicon, in order to assure good data retention characteristics. The requirements placed on these oxides will be much more apparent after the programming characteristics of the cell are examined.

SINGLE CELL PROGRAMMING

The E²CMOS cell is programmed by placing a high voltage across the thin tunnel dielectric. The resulting tunneling current will tunnel electrons onto the floating gate turning off the sense transistor or, with a different applied potential, tunnel electrons off of the floating gate, turning on the sense transistor. Once the charge has been placed on the floating gate, the actual floating gate potential can be modulated by the voltage on the control gate through capacitive coupling. It is this capacitive coupling that is used to generate the high voltage across the tunnel dielectric at the beginning of a programming pulse.

During a programming cycle, the cell is first erased into the one, or non-conducting state and then selectively written to a zero, or conducting state by a write cycle. This prevents the sense device from conducting current during the write operation when voltage is applied to the drain of the device. Therefore, the programming characteristics will be explored by first examining the cell during an erase.

ERASE CYCLE PROGRAMMING

During an erase cycle, a high voltage is applied to the control gate of the cell to be programmed, as shown in Figure 4. If all current through the tunnel oxide is neglected, the floating gate will simply track the applied voltage following the relationship of a capacitive divider,

$$V_{fg}^{1} = C_{up} * V_{cg}^{2} + V_{fg}^{3} \quad (0)$$

1 floating gate voltage; 2 Control gate voltage; 3 Initial floating gate voltage

where C_{up} is the coupling ratio of the cell, and is typically between 0.6 and 0.7. At the end of the erase pulse, the floating gate would again couple negatively by the same amount, and end up back at the initial floating gate voltage $V_{fg}(0)$.

However, the high voltage applied across the tunnel dielectric causes tunneling current to flow, which will discharge the floating gate during the erase pulse, as shown in Figure 4. At the end of the erase pulse, the floating gate will end up at a potential that is lower than the initial floating gate voltage by the amount that the floating gate has decayed during the pulse. This negative voltage is sufficient to turn off the sense transistor during a read operation. The magnitude of the control gate voltage which is required to couple this negative floating gate voltage up to the threshold of the sense device and actually turn it on after the erase pulse is defined as the programmed high threshold Vt_{High}.

4

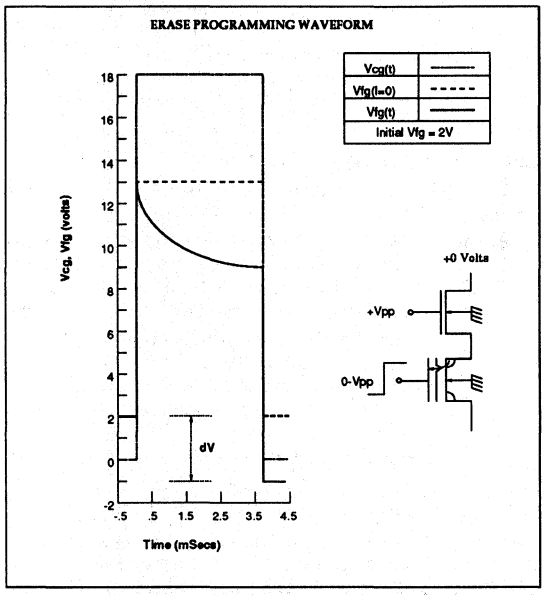


Figure 4

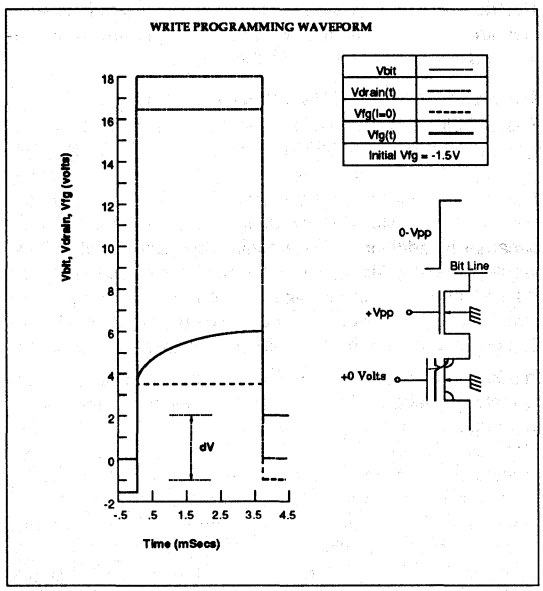


Figure 5

WRITE CYCLE PROGRAMMING

During the write cycle, a high voltage is applied to the bit line of the cell to be programmed as shown in Figure 5. If all current through the tunnel oxide is again neglected, the floating gate will track the applied drain voltage following the relationship of a capacitive divider:

$$V_{fg} = C_d * V_{drain}^{1} + V_{fg}(0) \quad (1)$$

1. Drain voltage applied during a write

C_d is the drain coupling ratio of the cell and is typically much lower than the coupling ratio to the control gate, ranging between 0.2 and 0.3. As in the erase case, the floating gate would again couple negatively by this same amount, and end up back at the initial floating gate voltage $V_{fg}(0)$ at the end of the write pulse. Also note that the pass transistor may have a voltage drop across it, lowering the voltage on the drain below the applied programming voltage V_{pp}.

However, instead of no current flowing through the tunnel oxide, the low coupling ratio keeps the floating gate at a low potential, which forces a high negative voltage to appear across the tunnel oxide. This high voltage causes tunneling current to flow which will charge the floating gate during the write pulse as shown in Figure 5. At the end of the write pulse, the floating gate will end up at a potential that is higher than the initial floating gate voltage by the amount that the floating gate has charged during the pulse. This positive voltage is sufficient to turn on the sense transistor during a read operation. The magnitude of the control gate voltage which is required to couple this positive floating gate voltage down to the threshold of the sense device and actually turn it off is defined as the programmed low threshold Vt_{Low}.

READING THE CELL

After an erase cycle the charge on the floating gate has left the sense transistor in the off, or non-conducting "1" state. If the erase cycle is followed by a write cycle, then the floating gate charge leaves the sense device in the on or conducting "0" state. Therefore, the data in the cell can be read by simply sensing the cell current when biased with the control gate centered between the on and off states. This is shown schematically in Figure 6. The bit line and control gate voltages are selected to minimize the potential across the tunnel dielectric during a read in order to maximize the retention of the floating gate charge. The actual magnitude of the programmed thresholds, and thus the margins of the cell, are controlled by the programming voltage, the physical cell layout, and the tunnel oxide electrical characteristics. The key

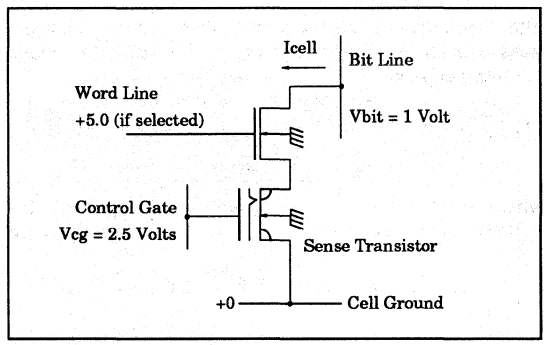


Figure 6

electrical properties of the tunnel oxide will be examined since they are critical in determining both the programming properties and the reliability of the E²CMOS cell.

TUNNEL OXIDE ELECTRICAL CHARACTERISTICS

The E²CMOS cell is programmed by placing a high voltage across the thin tunnel dielectric. The tunnel oxide is sufficiently thin, typically with a thickness between 90 and 120 Angstroms, that electrons will tunnel through the dielectric and program the cell. The exact nature of the tunneling mechanism is important because in addition to determining the amount of voltage required to get sufficient current through the oxide to program the cell, the tunnel characteristic also must be a very strong function of voltage to prevent the charge from leaking off of the floating gate during the low voltage, normal read, operation.

In addition to the electrical current voltage characteristics, thin tunneling dielectrics must also be characterized by the amount of charge that can pass through the oxide without altering its electrical properties. Electron traps located in the oxide will capture some of the electrons passing through the dielectric. As this trapped charge builds up in the oxide, the electrical properties change, and eventually the oxide wears out and ruptures. Thus, in addition to controlling the erase and write characteristics of an E²CMOS cell, the tunnel oxide, and oxide quality, play a major role in the reliability of the technology.

I-V CHARACTERISTICS OF THIN TUNNEL DIELECTRICS

A typical I-V characteristic of a thin tunnel oxide is shown in Figure 7. Since the current must flow through this oxide in both directions, the characteristic of the oxide is shown for both positive and negative polarities. Note that a higher negative voltage is required to get the same current as in the positive voltage case because of an additional voltage drop that occurs across a depletion region formed in the silicon for negative applied voltage. For a tunnel oxide of approximately 100 Angstroms in thickness, the maximum voltage developed during programming is roughly 10 volts, or a field strength of 10 MV/Cm. This very high applied field stress, needed for the tunneling process requires very high quality oxides and very clean processing conditions. Optimizing the thickness of the tunneling dielectric and trading off between the programming characteristics and the oxide reliability is a requirement of the E²CMOS technology.

The I-V characteristic is a very strong function of oxide thickness and follows the relationship of the Fowler-Nordheim tunneling equation,

$$I_{tox}(V) = A * Area * \left(\frac{V^2}{Tox^2}\right) * Exp\left(\frac{-B * Tox}{V}\right)$$

where A and B are the Fowler-Nordheim coefficients. This equation can be rewritten in terms of the field across the oxide as:

$$I_{tox}(E) = A * Area * E^2 * Exp\left(\frac{-B}{E}\right)$$

which is independent of oxide thickness.

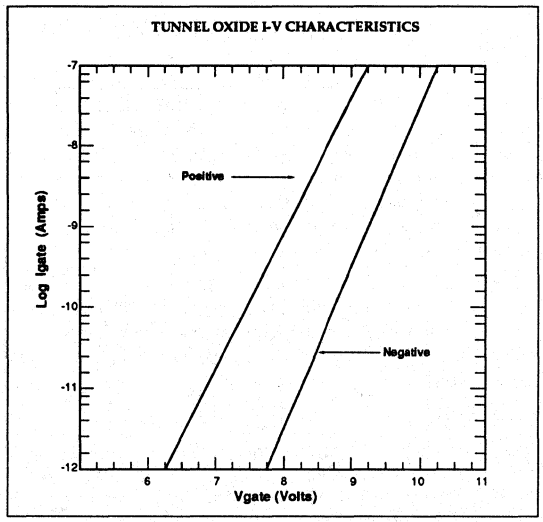


Figure 7

CHARGE-TO-BREAKDOWN OF THIN TUNNEL OXIDES

The I-V characteristic shown in the previous section was measured at sufficiently low current densities such that no charge trapping occurred during the measurements. If, however, a large amount of charge is passed through the oxide, the trapped charge in the oxide will alter the electrical I-V characteristic. The increase in voltage required to get the same tunneling current after a large amount of charge passes through the oxide will reduce the amount of charge transferred into the cell during a programming cycle and therefore reduce the cell programming margins with continued cycling. The magnitude of the charge required to shift the I-V characteristic depends on the quality and the number of traps in the oxide.

In addition to this shift in the electrical properties of the tunnel dielectric, defects in the oxide, whose properties change as the charge passes through the oxide, will actually cause the oxide to rupture after a finite amount of charge has passed through the dielectric. The maximum charge that can be passed through the oxide prior to oxide breakdown, or the oxide fluence expressed in Coulombs/Cm², can be determined by passing current through a tunnel dielectric until it ruptures. This physical limitation on the current that can be passed through the tunnel oxide places a limit on the number of programming cycles that can be performed on any E² device. This cycling limit, or endurance, is dependent on the quality of the tunnel dielectric and its associated defect density as well as the exact programming stress on the oxide. Lattice's technology maximizes the endurance of the devices through careful control of the requirements on the oxide as well as by optimizing the quality of the dielectric.

SYSTEM COST

DEFINITION

System cost differs from the cost (or "price") of components. Component cost is the acquisition cost of the unit. This cost can be readily observed and is quite measurable. Unfortunately, the cost of ownership of a component can be much higher than the unit cost. This is due to the hidden cost adders that relate to handling, quality, throughput and overhead necessary to take a "raw" unit and get it to a functional state in a board.

The system cost of a component is the sum of all of these hidden costs and represents the true cost of ownership for a given component. This cost can be difficult to define due to the multiplicity of potential overhead and cost added departments and locations.

APPLICATION

System cost is a real cost; however, the two groups most likely to influence a device technology decision are the least likely to be in a position to observe this cost. Purchasing and engineering, in most companies, are responsible for the parts list definition and component acquisition. These two departments are usually responsible for reducing the absolute unit cost while achieving the board-level performance criteria.

This situation is unfortunate since corporate and product line profitability are function of the system cost of a device, not its acquisition cost. A formula will be developed in the subsequent paragraphs that will help to define the system cost for using a given PLD type, vendor and technology. Each of the subsequent paragraphs relate to Figure 9 as contributors to total system cost.

PURCHASING OVERHEAD

The cost adders associated with purchasing can add 2% to the actual device cost. The more inventory line items to maintain, the more overhead. This is true in the maintenance of engineering as well as manufacturing environments. The minimization of device inventories without compromising flexibility is easily achieved by using generic architecture devices. Fewer line items reduces the purchasing overhead of maintaining sufficient stock.

INVENTORY MANAGEMENT

Inventory management overhead can add as much as 10% to the actual device cost. The costs of inventory management include shelf space, depreciation, count management, obsolete write-offs and safety stock. Again, the reduction of inventory line items simplifies the management overhead and reduces cost adders.

PROTOTYPE INVENTORY

Engineering labs are stocked with devices to assure proper supplies for prototype build and debug. At many companies, the engineering lab shortages are supplied from manufacturing stock. This results in a shrinkage of manufacturing inventories that contributes to a higher cost of the remaining units. This increase in cost can be as high as 1% --- if engineering inventories are maintained separately.

ACTUAL TEST ELIMINATES INCOMING QA

Extensive correlation has been performed by manufacturers and users of various types of semiconductor devices. Logic, memory, microprocessor and interface devices are seldom processed through an incoming electrical QA step. This is due to the consistent high quality of these devices guaranteed by the manufacturer.

Why then are PLDs subjected to a complete electrical incoming QA process? The lower quality and lack of performance of device to datasheet performance historically associated with these devices resulted in this QA step.

HIGH YIELDS CAN OBSOLETE QA TESTING

The costly step of incoming test can be eliminated with confidence when using E²CMOS PLDs due to the extensive "100% actual test" performed by the manufacturer. The elimination of this step brings several efficiencies to the user.

PROGRAMMING ELEMENT	ERASE TIME	TESTABILITY
Fuse	n/a	simulated
UV (OTP)	n/a	correlated
UV (window)	20+ min.	limited
E²CMOS	50 mS	100%

REUSABLE PLDS EASE QA

Some companies have extensive incoming QA operations that cannot be eliminated. Use of the reusable E²CMOS devices is ideal for these operations as the devices can be returned to manufacturing inventory after QA test where they can be instantly erased and used in production boards. This flexibility also allows QA to be performed at any step in the process.

QA testing, when required, is further simplified by utilizing the devices with generic architectures. Generic devices can be tested using one common test program and then configured in a variety of patterns during the programming operation. Thus, the generation and maintenance of multiple test programs and fixtures (one per architecture) are no longer required.

LESS HANDLING REDUCES DEFECTS

Semiconductor devices are inherently susceptible to mechanical and electrical defects induced during handling. In most cases this damage shows up as a bent pin (a real problem for automated pick & place machinery) or as an ESD failure. Whenever handling can be minimized, such as elimination of electrical incoming test, the quality of the devices will be maximized.

7% PARTS COST SAVINGS

The incoming QA handling and test of devices typically adds 7% to the device cost. This cost adder is based on resources, yield, and equipment utilization. This 7% can be saved by using E²CMOS devices and eliminating the QA operation with no degradation in device quality.

REDUCED DEFECTS FOR JIT/CERTIFIED INVENTORY

Today's manufacturing environments are moving toward minimizing inventories and maximizing throughput. These types of environments allow no room for defects that would cause the shut-down of a production line or component shortages. The use of higher quality devices is mandated in these environments.

BOARD & SYSTEM LEVEL SCREENS ARE EXPENSIVE

It is critical that devices with defects be screened as soon as possible in the manufacturing process. A common guideline used to determine the costs associated with the detection and screening of defective PLDs at various points in the manufacturing process is the "Factor of Ten" rule.

"FACTOR OF TEN" RULE

This rule is summarized in Table 1. The rule basically states that the cost of detecting and repairing a defective PLD grows by 10x at each subsequent manufacturing operation. The reason for this dramatic growth has to do with the fact that the device becomes increasingly "buried" within the system at each subsequent manufacturing step, allowing faulty functionality to be masked by other symptoms.

The "Factor of Ten Rule" implies that the efforts should be made as early as possible in the manufacturing process to keep the cost adder as low as possible. E²CMOS devices, with 100% factory testing, eliminate these defects altogether by detecting any defects prior to shipment to the end user.

Factor of Ten Rule

Cost*	Multiplier	Operation
$5	1x	Raw (incoming) cost of a device
$50	10x	Cost of detecting & repairing a board level failure
$500	100x	Cost of detecting and repairing a system level failure
$5,000+	1,000x	Cost of detecting and repairing a field failure (excludes customer goodwill, etc.)

* Assumed a $5.00 cost

Table 1

FAULTY PLDS INCREASE SYSTEM ERRORS

It should be noted that a very small yield loss can be greatly magnified by the quantity of devices on a board or in a system. It is quite common for enthusiasm to be generated for yield "improvements" from 97% to 99% or 98.5% to 99.5%. Figure 8 shows that even a yield loss as small as 0.5% can result in system failures of 5% with only 5 PLDs per system. This is due to the fact that 0.5% is a defect rate of 0.5 PPH which equates to 5,000 PPM, a very high defect rate.

E²CMOS technology offers a dramatic improvement to this sensitivity by bringing the board and system-level failure rate down to less than 100 PPM.

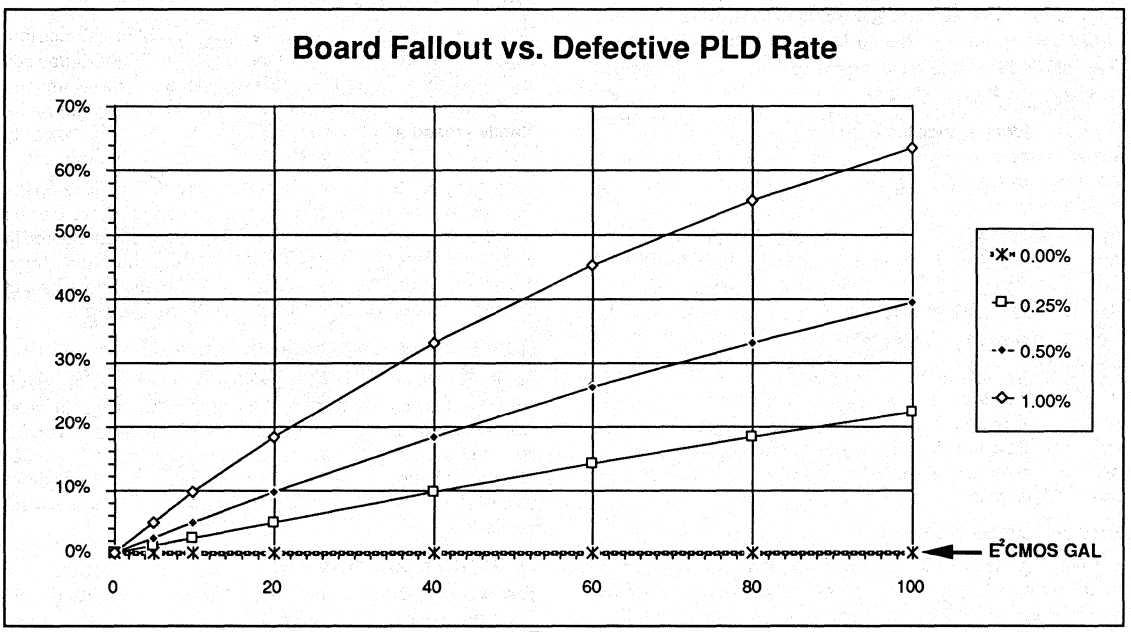


Figure 8

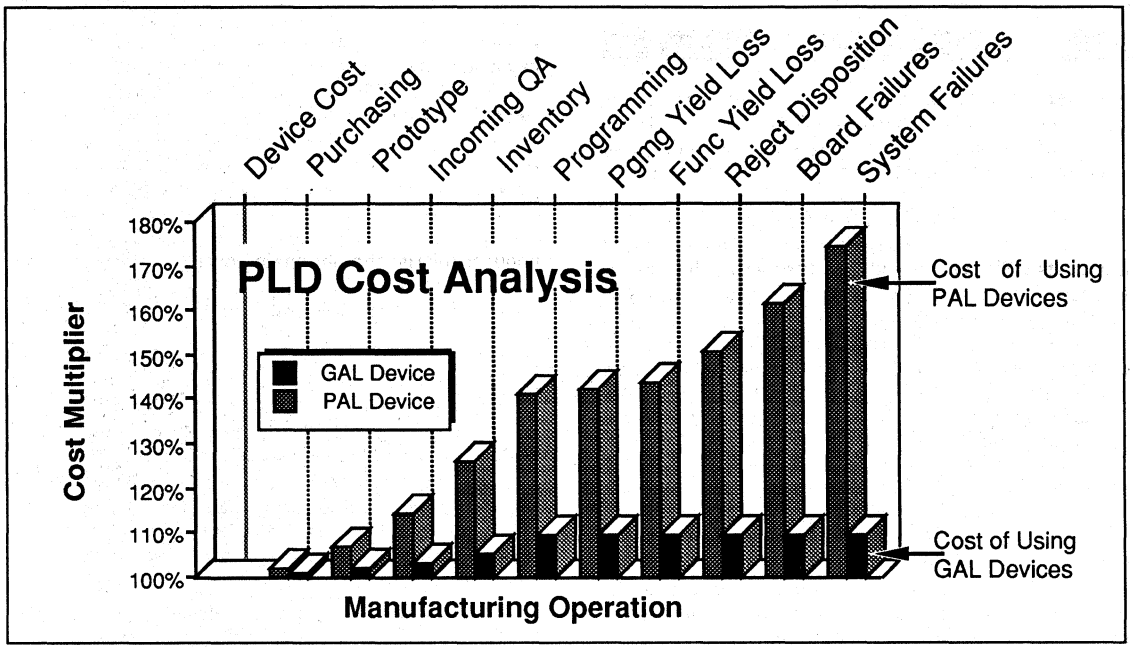


Figure 9

COST REDUCTION FORMULA

The preceding cost adders can be reduced to a formula that allows you to analyze the actual system cost of using a particular PLD. The formula is generic in nature, allowing you to tailor the factors to your specific environment. The formula is based on a very simple approach of assuming a percentage cost adder and yield factor for each operation.

$$Cost_n = Cost_{n-1} + (Cost_{n-1}/Yield_n)$$

The example in Figure 9 is based on actual data taken from a 100,000 piece-per-year user of traditional bipolar PLDs and the resulting savings possible with E²CMOS GAL devices. The technology advantage of E²CMOS shows very clearly in the graph as a savings of 34% over bipolar. The cost adder of the E²CMOS device is 9%, while the bipolar adder is 66% ... more than 7x higher!

CHOOSING AN EE-PROM BASED PLD VENDOR

The semiconductor industry cost & quality curves can be accurately modeled using statistics based on unit shipments. In short, the efficiencies and growth in expertise of a semiconductor manufacturer is a linear function of the doubling of units shipments. This theory concludes that the unit shipment leader in a given product technology will have the quality and efficiency advantage for that device technology.

EE-PROM technology has been used for programmable memory elements for over 10 years. During the last 5 years Lattice Semiconductor has used these elements for the manufacture of its E²CMOS GAL devices. Lattice has gathered hundreds of millions of hours of cell reliability data and shipped tens of millions of units (more than all other CMOS PLD vendors combined). Lattice's experience with manufacturing E²CMOS GAL devices allows the Company to provide customers with the highest quality levels available from any PLD manufacturer. □

GAL METASTABILITY REPORT

INTRODUCTION

The dictionary definition of metastability is "a situation that is characterized by a slight margin of stability." When applied to bi-stable (digital) logic, the term refers to an undesirable marginally stable output state between VIL max and VIH min.

Metastability can occur in bi-stable storage elements (registers, latches, memories, etc.) when setup and/or hold times are violated. Since setup and hold times vary with temperature and operating voltage, among other factors, the times referred to here are not the min/max numbers printed in data sheets, but rather the actual times for the given set of operating conditions. Typical applications where such times are likely to be violated include bus & memory arbiters, interfaces, synchronizers, and other state machines employing asynchronous inputs or asynchronous clocks.

Metastability manifests itself in a number of different ways. Common responses are (shown as they might be captured on a digital oscilloscope in Figure 1): runt pulse (1a), decreased output slew rate (1b), output oscillation (1c), and increased clock-to-output time (1d). By definition, the phenomenon of metastability is statistical in nature. Not only is entry into the state uncertain, but the time spent there is also variable.

Because PLDs are commonplace in today's designs, a thorough understanding of their metastable behavior is crucial. In some applications, output anomalies shorter than one clock cycle may be acceptable, but in applications where the register output is used as a control signal (clock, bus grant, chip select, etc.) for other circuitry, faults such as runt pulses and oscillation cannot be tolerated.

This report will not study the causes or characteristics of metastability in great detail; excellent material has already been prepared on this subject [1-5]. Rather, this report will introduce a mathematical model for the metastable phenomenon, discuss potential test methodologies, present and compare test results from various bipolar and CMOS PLDs, and discuss how to interpret the data. This report will close with suggestions on how to design metastable tolerant systems.

DERIVATION OF CONSTANTS

The basic premise of all metastability models is that a device's output is more likely to have settled to a valid state in time(t) than in time(t-n). In fact, the failure probability distribution follows an exponential curve. Figure 2 shows a typical failure frequency plot.

It is accepted [1] that metastable failures can be accurately modeled by the equation:

$$\log \text{Failure} = \log \text{MAX} - b(\Delta - \Delta o) \quad (1)$$

In this equation, MAX represents the maximum failure rate for a particular environment, Δ is the time delayed before sampling the DUT (Device Under Test) output, and Δo is the time at which the number of failures starts to decrease. On a failure frequency plot (such as the one in Figure 2), Δo represents the knee of the curve. The constant b is rate at which the frequency of failures decreases after the knee is reached.

Recall that:

$$\log X = a \ln (X), \text{ where } a = \log (e)$$

Substituting this into (1):

$$a \cdot \ln \text{Failure} = a \cdot \ln \text{MAX} - b(\Delta - \Delta o) \quad (2)$$

MAX is related to the clock frequency (fCLOCK) and data frequency (fDATA). That is,

$$\text{MAX} = (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) \quad (3)$$

Substituting (3) into (2) and applying some algebra:

$$a \cdot \ln \text{Failure} = a \cdot \ln (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) - b(\Delta - \Delta o)$$

$$\ln \text{Failure} - \ln (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) = -b/a(\Delta - \Delta o)$$

Setting $k2 = b/a$ and rearranging the equation yields:

$$\text{Failure} = (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) e^{-k2} (\Delta - \Delta o) \quad (4)$$

When used with equation (4), the constants k1, k2, and Δo, completely describe a particular device's metastable characteristics; they indicate how quickly a device can resolve the metastable condition. Devices which transition out of the metastable region quickly are characterized by a small Δo and a large k2.

The constant k1 is peculiar to the test apparatus (it can be thought of as a "scaling factor"). The maximum metastable failure rate (MAX) is limited by fCLOCK; a failure cannot occur if the device isn't clocked. Likewise, it is true that a metastable failure cannot occur unless data has changed. So, if fDATA < fCLOCK, then MAX = fDATA. This was the case in the test fixture Lattice used (fCLOCK=10MHZ, fDATA=2.5MHz). Substituting MAX = fDATA back into equation (3) yields: k1 = 1/fCLOCK, so k1 = 100ns for our tests.

TEST FIXTURE

The goal of testing a particular device's metastable characteristics is to generate real numbers for the constants k2 and Δo. To do this, the device must first be forced into the metastable state. This is done by intentionally violating setup and/or hold times. Once metastable, the output can be observed on an oscilloscope or used to increment an event counter.

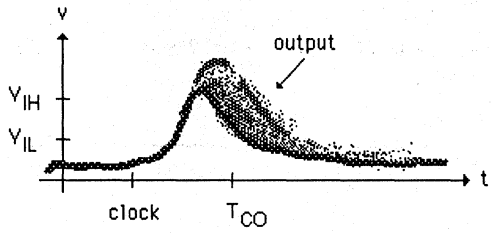
Traditional Approach

One approach to characterizing a device's metastable behavior employs a test fixture similar to that shown in Figure 3a. In such a fixture, data to the device includes a "jitter band" so that the device sees changing data as it is clocked. The DUT output is fed to a window comparator to determine when it is in the metastable region (between VIL max and VIH min). The comparator output can be sampled periodically and used to increment an event counter.

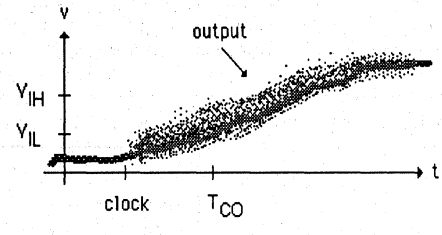
This method of testing, though it directly yields MTBF numbers, has some drawbacks. The first is that it does not distinguish between the different types of metastable behavior (runt pulse, oscillation, slow rise/fall time, delayed transition), and it may have difficulty detecting every type. Also, the registers used in the detector circuit itself may become metastable, which would adversely affect the results.

A New Approach

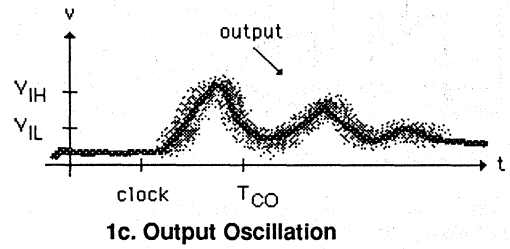
The test method used to gather data for this report used the circuit shown in Figure 3b. The tester employed an "infinite precision" variable delay circuit to control clock placement with respect to data. This arrangement allowed exact worst



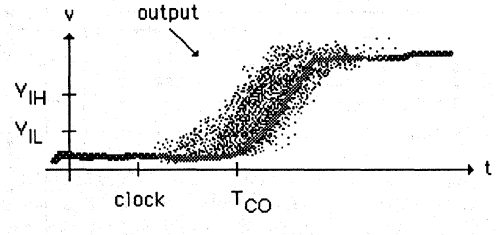
1a. Runt Pulse



1b. Decreased Slew Rate



1c. Output Oscillation



1d. Increased T_{co}

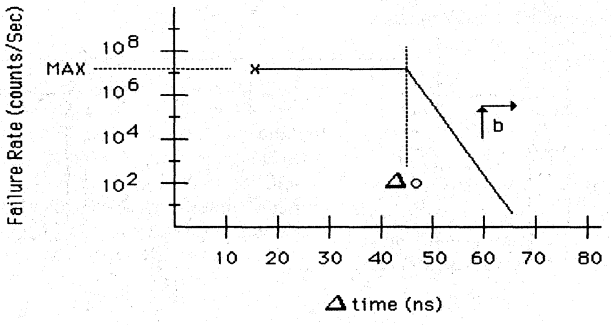


Figure 2. Typical Failure Frequency Plot

case placement of the clock, so as to induce metastability with nearly every clock pulse.

Using a digital oscilloscope (Tektronix 11402) in point accumulate mode, metastable failures were recorded over a lengthy period of time. A hardcopy was then made and the constants empirically obtained (details below).

The oscilloscope approach, being visual in nature, enables the designer to make educated decisions regarding maximum clock and data rates, as well as the suitability of using the output to drive other circuitry. The five minute sample period used in our tests contained approximately 750 million failures. Much longer sample periods were evaluated, but they provided no perceptible gain in usable information.

A slight disadvantage of this approach is that extracting k2 and Δo values from the hardcopies is not straightforward. Because each point on the hardcopy can represent any number of actual samples (between one and 1.5 million), one cannot simply count the points at time(t) for the MTBF at that time (although, in the case of the scattered points, the probability is low that a single isolated point represents more than one sample).

To generate values for k2 and Δo, it was necessary to refer to previous metastability studies [1]. By studying the output plots of devices with known constants, certain relationships were established. For example, it was determined that Δo represents the time from the leading edge of the output until the "dot density" starts to decrease measurably. It should be noted that Δo in previous studies included device propagation delays, whereas in our test it does not.

The time from Δo until the dot density equals zero was defined to be the "time to metastable release" or simply time(r). The relationship between k2 and time(r) is given below in (5), and shown graphically in Figure 4. Recall that MAX=2.5x10^6 and a=log(e).

$$k2 = \log(MAX) / (time(r) \cdot a) = 14.73/time(r) \qquad (5)$$

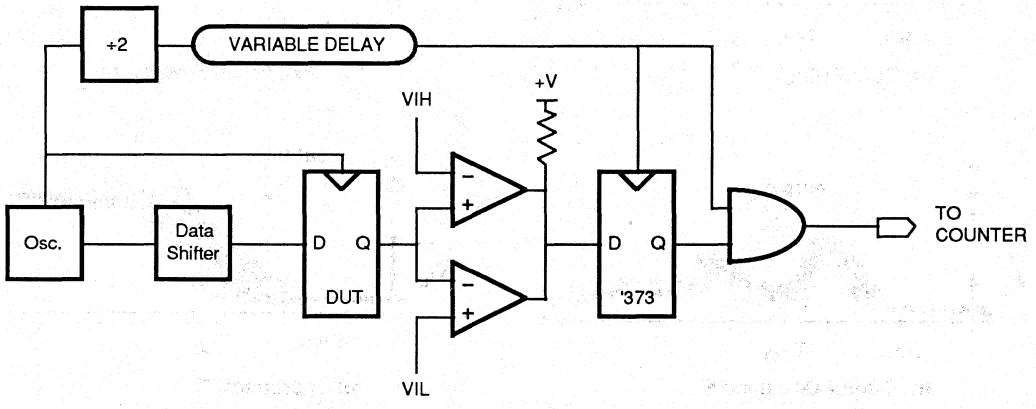


Figure 3a. Traditional Metastability Test Circuit

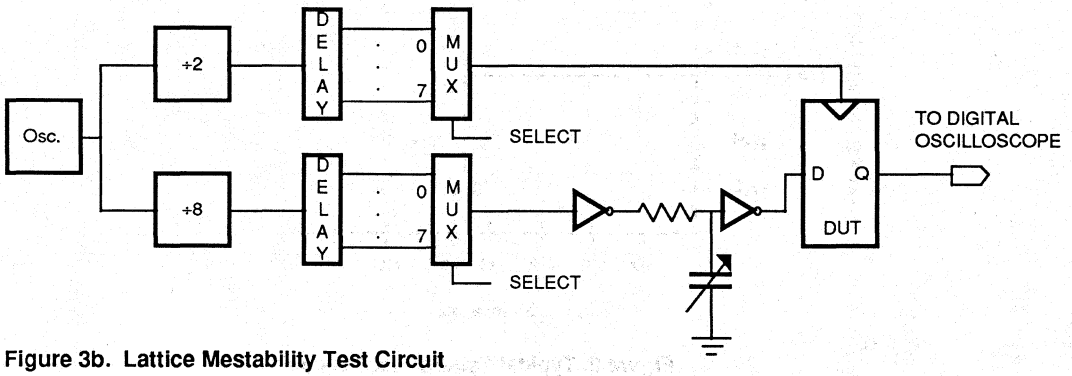


Figure 3b. Lattice Mestability Test Circuit

INTERPRETING THE RESULTS

In addition to examining E²CMOS GAL devices, this study also tested several bipolar PAL devices as well as other CMOS PLDs. To insure that the results of this study would be relevant, all necessary precautions were observed: the devices were of recent vintage and were acquired blindly through distributors; multiple samples of each device were tested and the results combined; all devices had either fixed 16R8 architectures or were configured to emulate the 16R8 architecture; the devices were programmed from the same JEDEC fuse map file (the source equations and the JEDEC fuse map file are presented in Listing 1).

Plots 1 through 4 on the following pages are some of the oscilloscope plots generated for this study. The top waveform in each plot is the clock signal and the middle trace is the data input. The horizontal scale is 10ns per division, so the exact data setup time that caused the metastable condition can be read directly. The vertical scale is 2V per division for the top two traces, and 1V per division for the bottom trace. Only the bottom trace is aligned with the voltage scale on the left margin of the plot.

The bottom waveform in each plot is the device output (the only signal captured in point accumulate mode). In every case, the output signal plot shows two stable levels after the transition. This is a direct result of the "indecision" caused by metastability; on some cycles the output settled to a high level, while on others it settled to a low level.

Plot 1 shows the response of a bipolar PAL16R8B (15ns). Notice the very well defined runt pulse (this correlates with previous data gathered on similar devices by the manufacturer [1]). The absence of a secondary trace along ground indicates that the output always starts to transition to a high level, even when it finally settles to a low level. This characteristic makes the device unsuitable for use in control path applications (when metastability is possible). All of the bipolar parts examined showed similar results.

Plot 2 is from a UV-EPLD. This CMOS device, as did all CMOS PLDs Lattice tested, exhibited characteristics far superior to bipolar parts. This can be attributed, in part, to the higher switching speed of CMOS logic. GAL devices, for example, have output slew rates approaching 5V/ns, compared to about 1V/ns for bipolar devices.

Plot 3 is from a GAL16V8-15 and Plot 4 is from a GAL6001. Aside from the fact that setup time violations may cause tCO to increase by a small (but random) amount, the outputs are very clean and well behaved. The fact that there are no runt pulses or other anomalies is extremely significant, as the GAL6001 not only allows asynchronous clocking, but encourages that activity. Compare Plots 3 & 4 with Plot 2. Just as the characteristics of CMOS PLDs (in general) are superior to those of bipolar PLDs, the metastable response of GAL devices is noticeably better than that of UV-CMOS EPLDs.

For reference purposes, Plots 5 through 7 are included. Plot 6 shows a normal (ie. non-metastable) GAL16V8-15 transition, and Plot 7 a normal PAL16R8B transition. Plot 5 is from a TTL flip-flop (TI 7474). For consistency, only rising edges have been shown. Our tests also covered falling edges which,

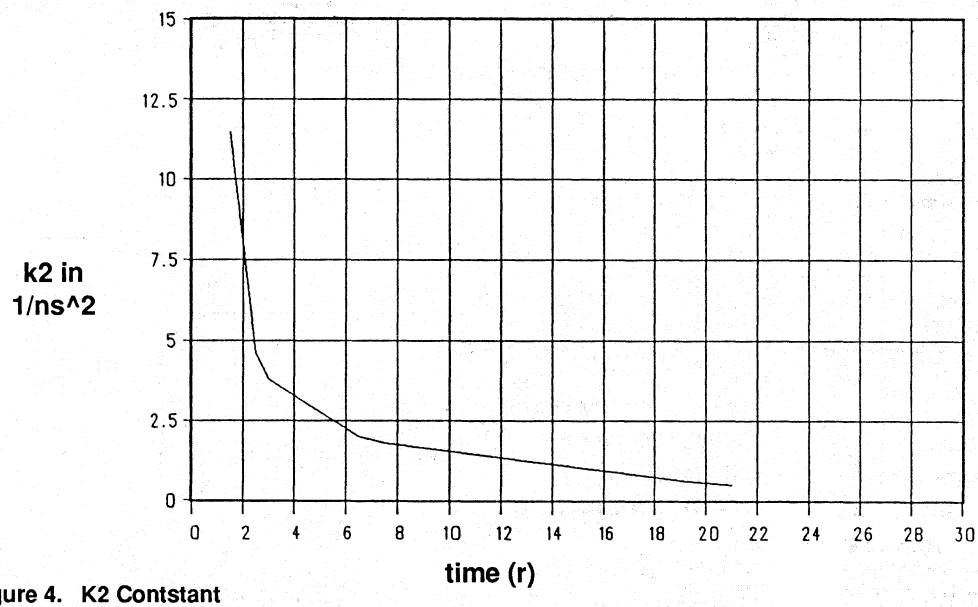


Figure 4. K2 Contstant

in general, were interesting but did not provide any additional information.

For a more quantitative look at the phenomenon of metastability, refer to the table beneath each plot. These tables list the measured values of the constants Δo and k2 for the device whose plot is shown, and for similar devices. Recall that large k2 and small Δo values are desirable. The numbers in the tables correlate closely with the results of earlier tests [1,5], confirming the validity of our test method.

Since all current GAL devices possess very similar register and output buffer circuitry, and all are fabricated using the same basic process, the data shown in Table 1 for the GAL16V8 is considered applicable to all devices and speed grades in the GAL family.

USING THE RESULTS

If a register enters the metastable state in a system, then data was obviously unstable as the register was being clocked. The argument over which data should have been captured (old or new) is academic as the register will randomly pick one or the other. Signals in most asynchronous systems are active for more than one clock cycle, so if they are missed initially, they could be captured on a subsequent clock cycle.

It is the task of the state machine designer to take adequate precautions against metastability causing illegal states to be entered. One way to do this is by using "gray codes" when ordering states. Gray code state equations allow only one state bit to change during a state transition. Thus, the worst metastability could do would be to delay a state transition by one clock cycle. If more than one bit were allowed to change, the outcome would be purely random, and probably illegal. Figure 5 shows examples of both cases.

Other solutions are to externally (or internally) synchronize the asynchronous signals, or to increase cycle times to allow time for metastable outputs to settle. An example of the latter solution is given below.

It is worth noting at this point that state machines (synchronous or asynchronous) can fail for reasons other than metastability. A not insignificant component of a PLD's specified setup time is directly attributable to internal data skewing [2]. Data skewing is the inevitable result of differing signal path lengths, loading conditions, and gate delays. Stated another way, each input to output path has its own set of actual AC specifications. If insufficient setup time has passed, different "versions" of the same data may be present at the inputs of different registers as they are clocked. A good example of this is:

```
Output_Pin19 := Input_Pin2;
Output_Pin15 := !Input_Pin2;
```

If clocked at precisely the right moment after an input transition, one register will capture old data while the other captures new data, resulting in a system failure. This condition, though also the result of a setup time violation, should not be confused with metastability (the "incorrect" data that is captured has normal output characteristics); it is, pure and simply, the result of a violation of specifications. Incidentally, there is less than 1.5ns of skew between the various paths through a 15ns GAL device.

Example

To determine the maximum clock rate (given an acceptable error rate) that a particular device will allow in an asynchronous environment, equation (4) is used. For example, the system shown in Figure 6 utilizes a 9600 baud (bits/sec) asynchronous data stream. The system clock period is tCO+tPD+tSU+Δ. For one failure per year:

$$3.2\text{x}10\text{-}8 = [(1\text{x}10\text{-}7)(1/(\Delta+49))(9600)]e^{-[8(\Delta-2)]}$$

Solving for Δ yields Δ=2.796ns, or about 3ns, for a cycle time of 52ns. Referring back to Plot 2, the additional delay of 3ns intuitively makes sense. Remember, in terms of setup and hold time violations, the oscilloscope plots were made under worst case failure conditions; the scattered dots could represent MTBFs of days, years, or even millenniums in a typical asynchronous environment.

Due to the extremely quick metastable settling times of GAL devices, a relatively small increase in the cycle time will produce a dramatic improvement in reliability.

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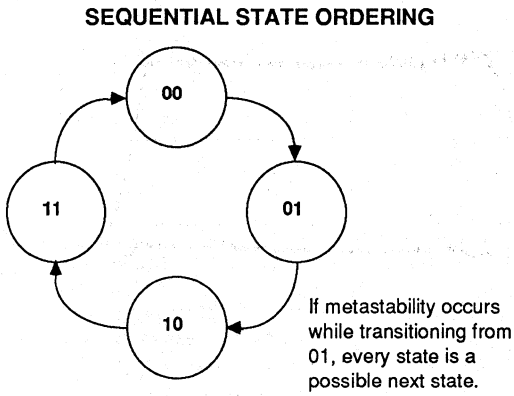


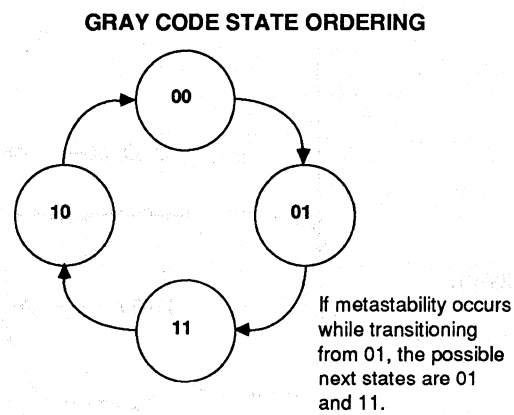


Figure 5.

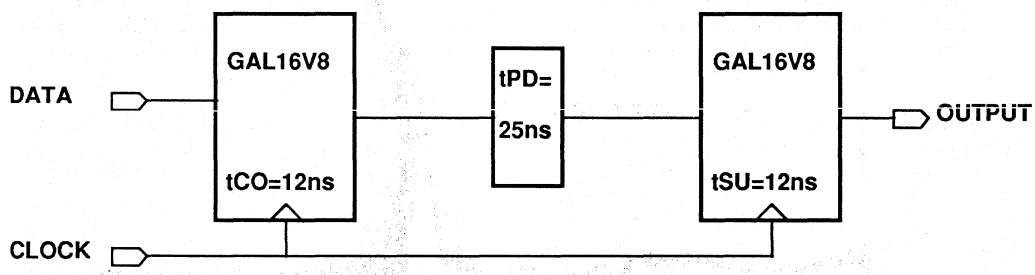


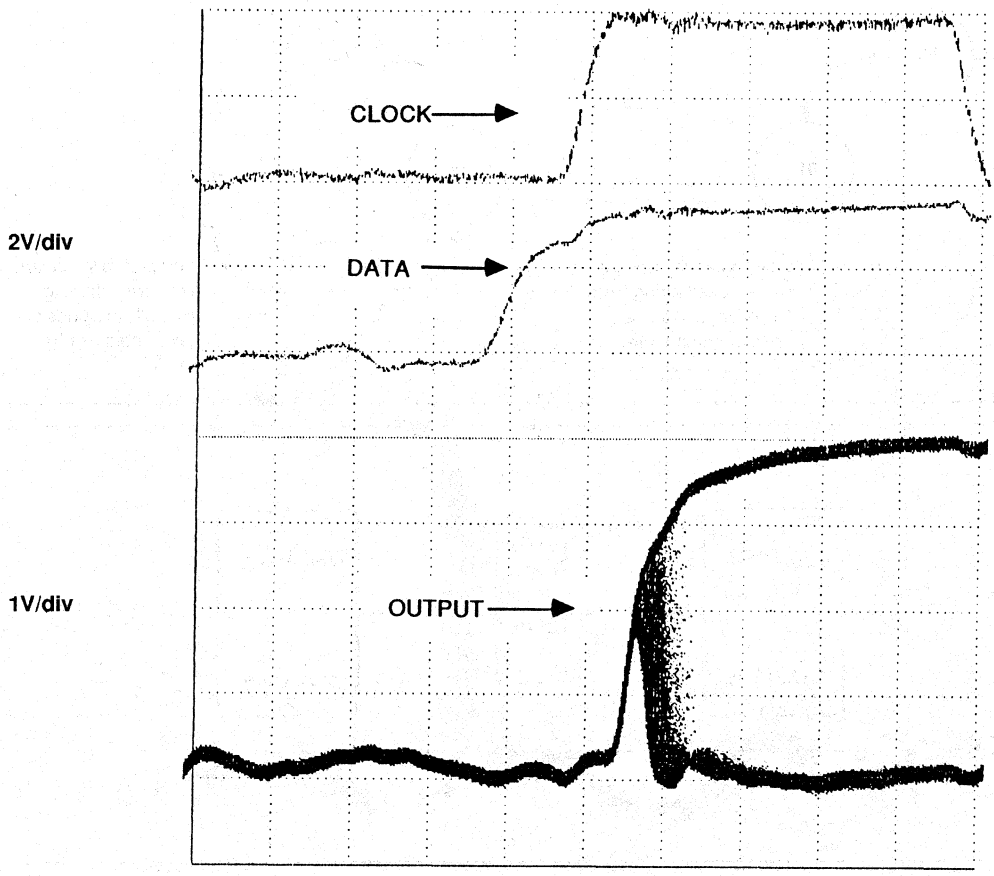
Figure 6.

```
MODULE metastable

TITLE 'Metastable Test
Pattern'

uOO Device 'P16R8';

d       PIN  2;
q1,q2   PIN  12,19;
        EQUATIONS
q1 := d;
q2 := d;
        End metastable
```

Listing 1a. Source equations

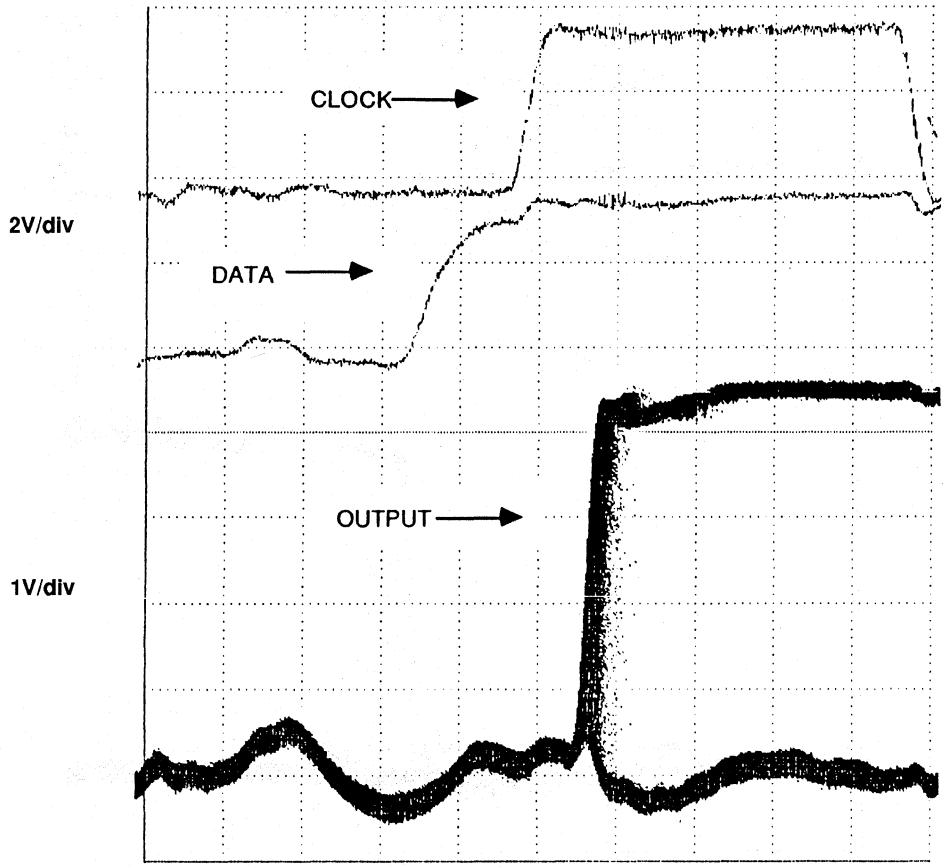
```
JEDEC file for: P16R8
Metastability Test Pattern*
QP20* QF2048* F0*
L0000 10111111111111111111111111111111*
L1792 10111111111111111111111111111111*
C07F4*
```

Listing 1b. JEDEC file



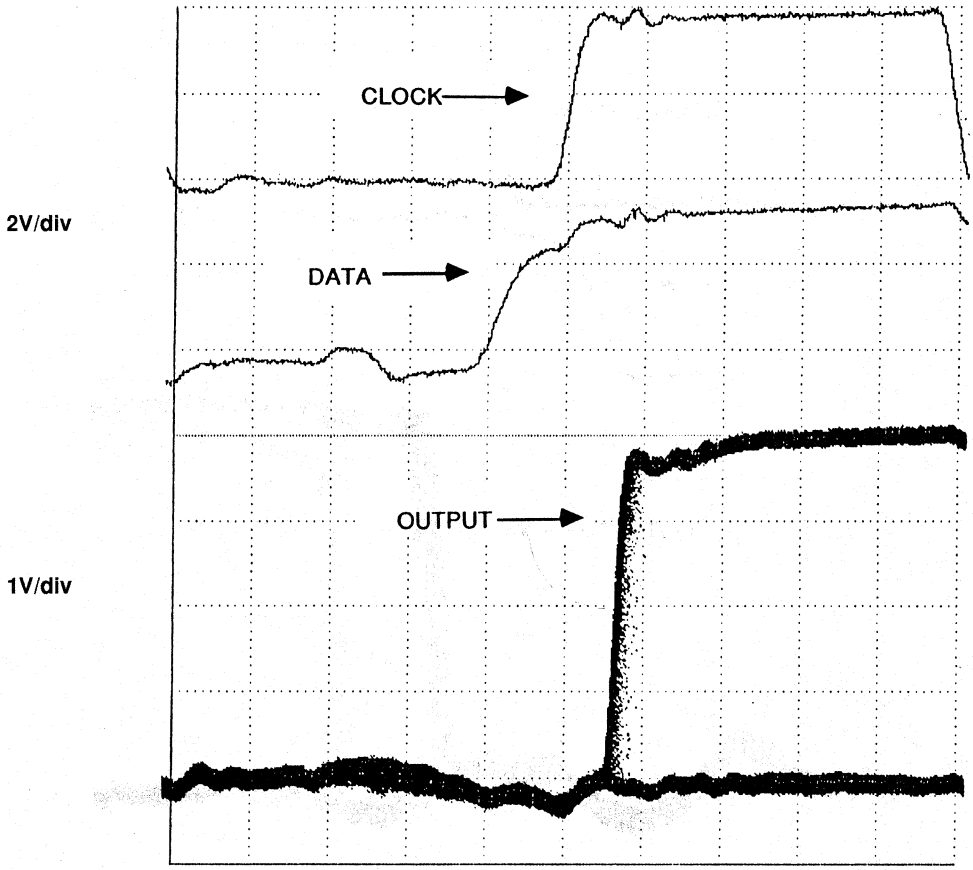
Plot 1. PAL16R8B

Part #	Date Code	∆o (ns)	k2/ns^{-2}
PAL16R8A	8721	11	2.0
PAL16R8B	8722	6	3.0
AmPAL16R8A	8631	8	1.9
TIBPAL16R8-15	8723	5	1.25



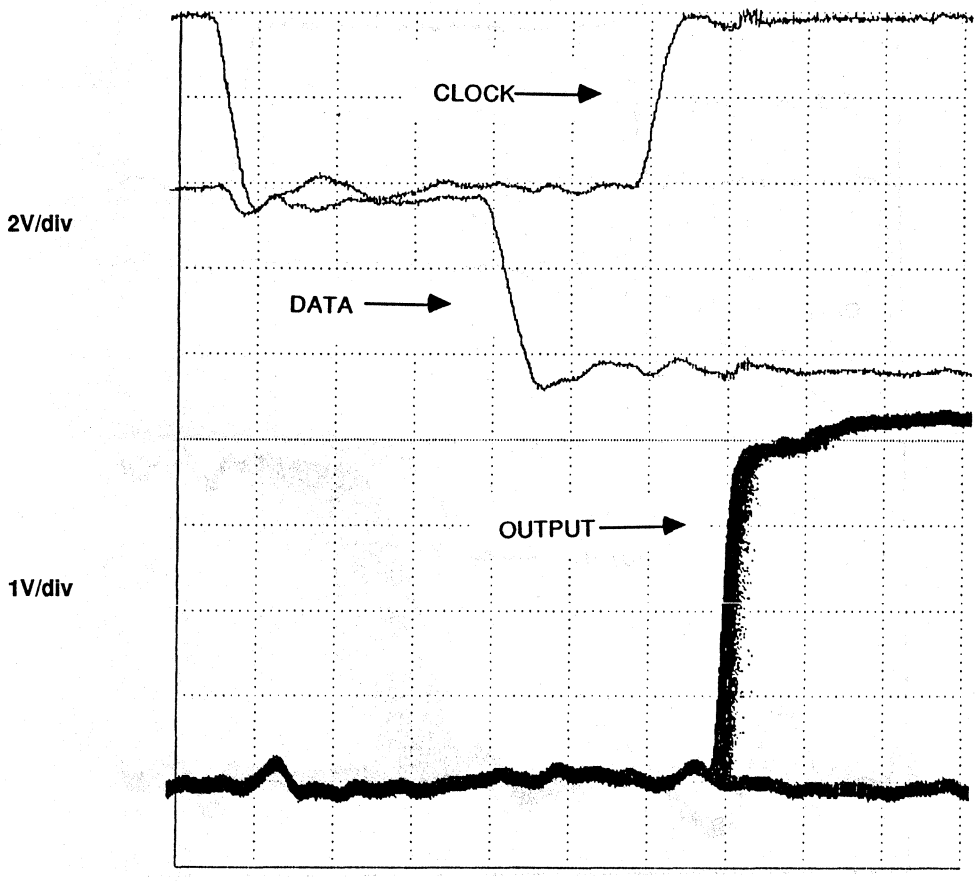
Plot 2. CYPALC16R8-25

Part #	Date Code	△o (ns)	k2/ns^{-2}
CYPALC16R8-25	8622	3	3.75



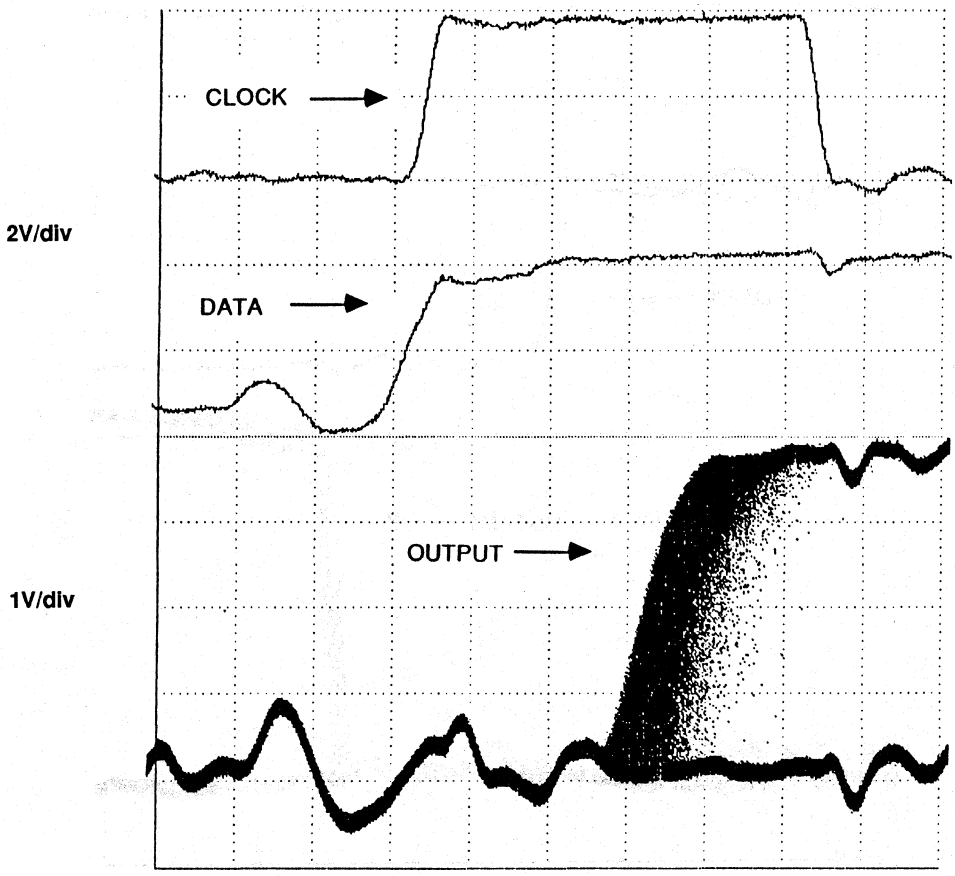
Plot 3. Lattice GAL16V8-15L

Part #	Date Code	△o (ns)	k2/ns^{-2}
GAL16V8-15	8731	2	8
GAL16V8-25	8730	2	8



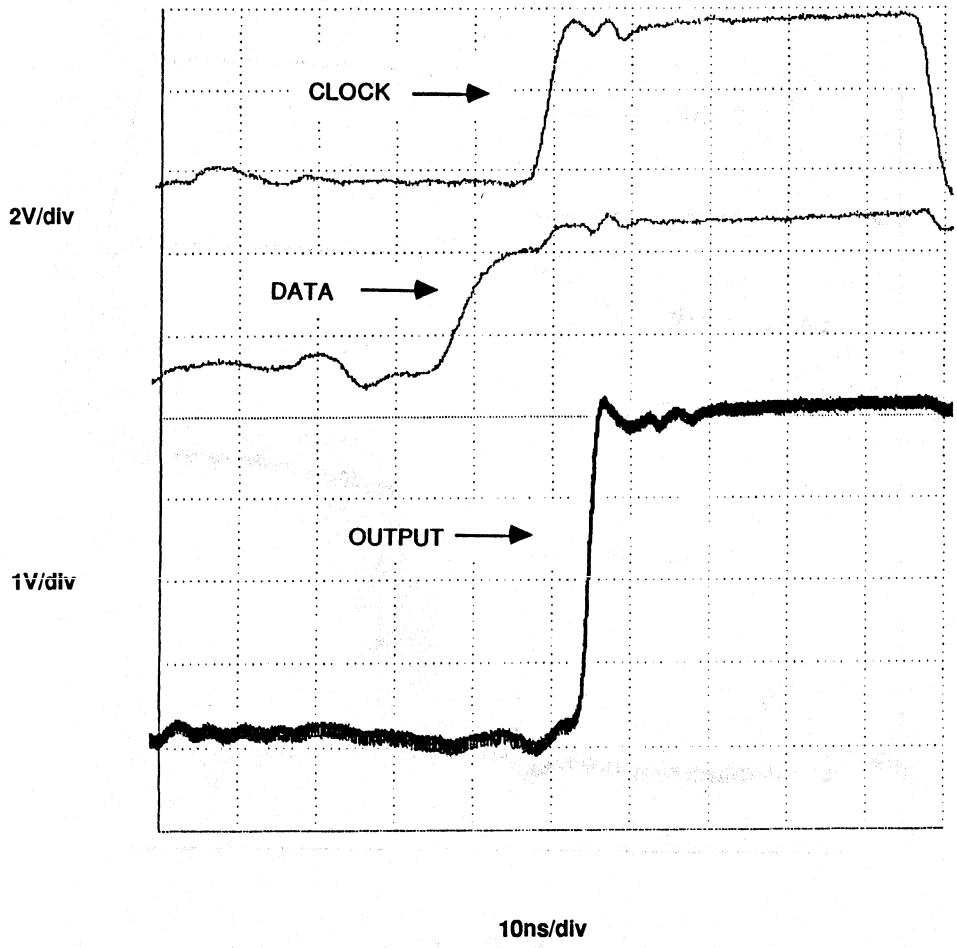
Plot 4. Lattice GAL6001ES

Part #	Date Code	Δo (ns)	k2/ns^{-2}
GAL6001ES	8652	1	6.25

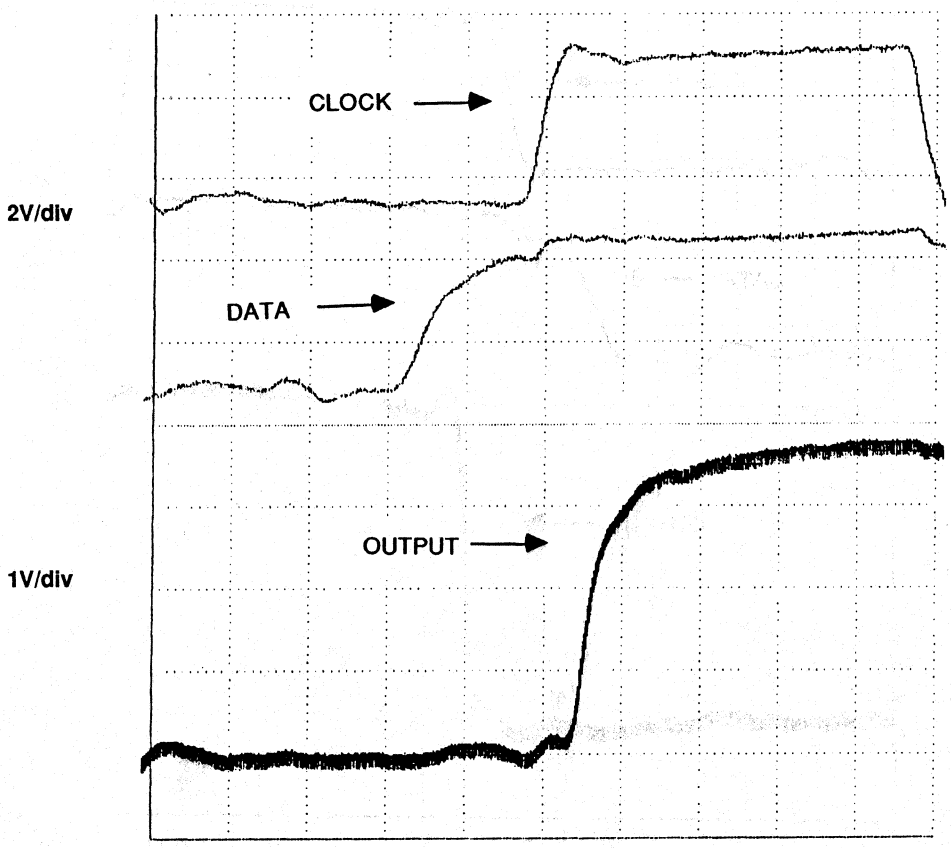


Plot 5. 7474

Part #	Date Code	Δo (ns)	k2/ns^{-2}
SN7474N	7615	6	1.3
9N74/7474	7341	7	1.25



Plot 6. Normal Lattice GAL16V8-15L Transition



Plot 7. Normal PAL16R8B Transition

END

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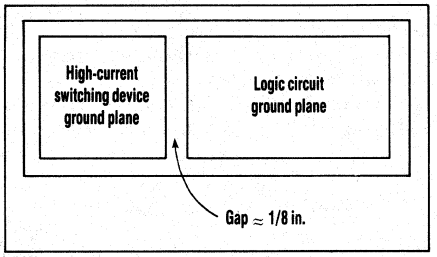
MAKE SURE THAT YOUR TURBO-CHARGED LOGIC SYSTEM WORKS BY PAYING AS MUCH ATTENTION TO PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES AS TO LOGIC DESIGN CONSIDERATIONS.

AVOID THE PITFALLS OF HIGH-SPEED LOGIC DESIGN

Modern high-speed systems demand modern high-speed logic families. Consequently, semiconductor houses have developed such product lines as ACT, FACT, and AS. But these systems also demand that the lay-out of their boards conform with the results of distributed-element theory, otherwise ringing, crosstalk, and other transmission-line phenomena render those systems inoperative. Meeting this second requirement necessitates something more than a new product introduction—it insists on a change in the way logic boards are engineered. The logic-systems designer and the board-layout designer must work hand-in-hand if a viable high-speed board or system is to be produced.

In the past, logic design and board layout were usually regarded as separate parts of the design process. First the system designer configured the logic, then the board engineer laid it out. That approach worked because slew rates were so low (0.3 to 0.5 V/ns) that crosstalk wasn't much of a problem; rise times were so long (4 to 6 ns) that ringing could settle down before a logic element could change state; and in general, the assumptions of lumped-element circuit theory usually worked out pretty well.

For systems designed with today's high-speed logic circuitry, those underlying assumptions no longer hold true. Today's slew rates are on the order of 2 to 3 V/ns, rise times are below 2 ns (frequently, below 1 ns), and transmission-line phenomena, such as ringing, can be a problem for trace



1. TO MINIMIZE NOISE, THE ground plane should be fragmented into separate areas for noisy high-current devices and for sensitive logic circuits. For best results, the number of signal lines that cross the gap between the fragments should be minimized.

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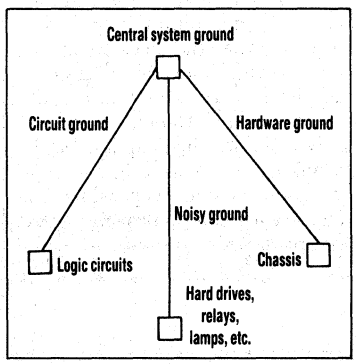
lengths as short as 7 in. As a result, logic designers must take certain steps:

- Use ground and power planes.
- Control conductor spacings to eliminate crosstalk.
- Make extensive use of decoupling capacitors.
- Pay attention to ac loading.
- Terminate lines properly to minimize reflections.

PLANE ADVICE

For high-speed logic, ground planes aren't simply suggested for reliable board performance—they are absolutely necessary. It's essential that one layer of the board be assigned for a ground plane and that it cover as large an area as possible. A solid ground plane lowers the ground-return-path impedance as well as the device-to-device ground pin impedance.

But a common ground plane for all of the circuitry in a system can cause problems by coupling noise from high-current switching devices into sensitive logic inputs. Therefore, the ground plane for such high-current devices as relays, lamps, motors, and hard drives should be separated from the logic ground. This can be accomplished by fragmenting the ground plane into discrete areas *(Fig. 1)*.



2. SEPARATE DEDICATED grounds should be supplied for the logic circuitry, noisy high-current devices, and the chassis. The three should come together at one point, the central system ground, which is usually located near the power supply.

But fragmentation causes problems of its own—it creates discontinuities in the characteristic impedance of any transmission line that crosses the separation between fragments. Therefore, for best results, boards should be laid out so that only two fragments are needed. The gap between those fragments should be kept as narrow as possible (an eighth of an inch works well in most applications), and the number of signal lines that cross the gap should be minimized. Designers should also bear in mind that through-holes and vias subtract from the effective area of the plane, increasing its effective impedance.

As with grounding, an entire layer of the board should be designated as a power plane. Even though it is at a different potential, the power plane should be implemented in accordance with the same concepts as the ground plane. Therefore, it should be fragmented when necessary to isolate noisy components from delicate logic circuits.

A WELL-GROUNDED SYSTEM

In addition to properly designed power and ground planes, high-speed logic systems require the establishment of a good, clean (low-

SIGNAL LINES BECOME TRANSMISSION LINES

For the transmission line model illustrated in the diagram, the rise time (t_R) is less than the line propagation delay (T_D). In other words, a complete TTL level transition will occur before the pulse is received at the receiving end of the line and reflections (ringing) will result. The voltage change at point A on the line is expressed in Eq. 1:

$\Delta V_A = \Delta V_{int} (Z_O / (R_O + Z_O))$

Where: V_{int} = internal voltage on the output of the driver;

R_O = output impedance of the driving gate;

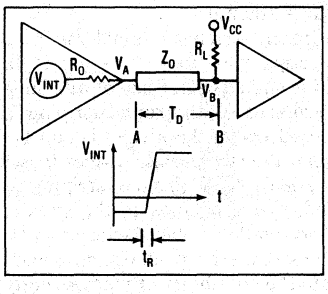
R_L = load impedance;

Z_O = the characteristic line impedance;

and V_A = the source voltage at the sending end of the line.

Because R_O is so small when compared to the line impedance, the change in voltage at point A (ΔV_A) will approximately equal the change in internal voltage (ΔV_{int}). This voltage transition propagates down the line and is seen at point B after the line propagation delay, T_D.

At point B, a portion of the wave will be reflected back towards point A in accordance with the formula (Eq. 2):



Eq. 2

$\rho_L = (R_L - Z_O) / (R_L + Z_O)$

where ρ_L, called the voltage reflection coefficient (rho), is the ratio of the reflected voltage to the incident voltage.

After examining Eq. 2, it should be evident that $-1 \leq \rho \leq +1$. It should also be evident that there will be no reflected wave if $R_L = Z_O$—if the line is terminated in its characteristic impedance. Note that the reflected wave can, in principle, be as large as the incident voltage and of either positive or negative polarity.

This analysis holds true for the sending end of the line, as well as the receiving end. That is,

Eq. 3

$\rho_S = (R_O - Z_O) / (R_O + Z_O)$

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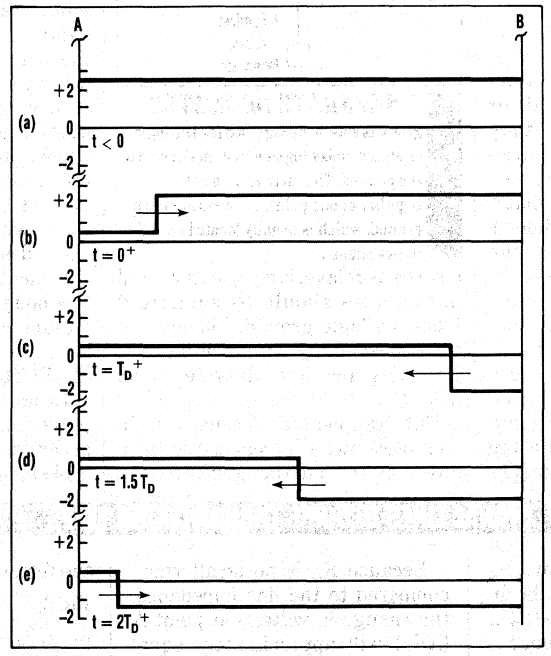
noise) system ground for reliable performance. A clean system ground ensures less noise within the system, and thus ensures good, strong transistor margins. At least 10% of the ground connections on the pc card should be connected to the system ground to reduce card-to-ground impedance.

Like the ground and power planes of the individual boards, the overall grounding scheme should be fragmented with separate conductors provided for the various sections of the system. For example, all relays, lamps, hard drives, and other noise-generating devices should have their own separate ground path. The system's mechanical package (chassis, panels, and cabinet doors) should have a dedicated ground. And, of course, the logic circuitry should have a ground of its own.

Those three grounds should then come together at the central system ground point, which will usually be located near the power supply *(Fig. 2)*. This common-point grounding technique can also be very effective in reducing radiated interference (EMI and RFI).



3. WAVE PROPAGATION along a transmission line occurs as follows: Prior to time zero, there is a steady-state voltage of 2.5 V dc on the line (a). At t = 0, the voltage at point A drops to 0.5 V, sending a negative pulse of -2 V toward point B (b). At t = T_D, that negative pulse is reflected from point B. It adds algebraically to the 0.5 V on the line and sends a -1.5-V pulse back toward point A (c). The reflections then continue as in (d) and (e).

TAMING CROSSTALK

Crosstalk—the undesirable coupling of a signal on one conductor to one on a nearby conductor—becomes an increasingly serious problem as slew rates go up. This signal coupling is made worse if the second trace has a high impedance or if the traces run parallel to one another for more than a few inches and are spaced less than 100 to 150 mils apart.

Crosstalk can be catastrophic to a logic board, sabotaging a conceptually flawless piece of logic design. For example, if a clock line and a data line run parallel to each other for more than several inches, and if the data line cross-couples or superimposes its signal onto the clock line, the device that the clock is driving may detect an illegal level transition.

Methods to reduce crosstalk are straightforward, though not particularly elegant. The coupling can be attenuated by separating the adjacent traces as much as possible. The trouble with this approach is that available board real estate often limits the possible separation to an inadequate amount.

Ground striping, or shielding, is an effective way to reduce crosstalk and it makes better use of available board area. With ground striping, a ground trace (the stripe) is run between the two parallel traces to act as a shield. If ground striping is used, through holes to the ground plane should be placed every 1 to 1.5 inches along the ground strip to eliminate the possibility of inadvertently creating a stub or a high-frequency antenna.

Another step that can be taken to reduce crosstalk is to lower the impedance of those traces into which crosstalk is especially to be avoided. The lower the impedance that a trace presents, the harder it will be to cross-couple a signal into it.

Even with the use of power and ground planes on a pc board, decoupling capacitors must be used on the V_{CC} pins of every high-speed device. Those devices demand a nearly instantaneous change in current whenever they switch states. Because the power plane can't meet that demand, a high-quality decoupling capacitor is required, otherwise the switching will cause noise on the V_{CC} plane.

A 0.1-μF multilayer ceramic (MLC) or other RF quality (low-inductance) capacitor should be placed on every fast-slew-rate device as close to the V_{CC} pin as possible. The commercially available DIP sockets with built-in decoupling capacitors also work well in this application.

Most designers, when they think of loading at all, think in terms of dc loading—traditionally referred to as fan-out and fan-in. But that type of loading rarely presents a problem with today's state-of-the-art logic devices. Much more significant when designing with high-speed logic are input and output ac loading.

INPUT CAPACITANCE

Because the input capacitance of a device impacts the overall performance of the logic circuit, it should be examined before a particular device is selected for a design. To ensure specified performance, the total load capacitance that a device drives—including the distributed ca-

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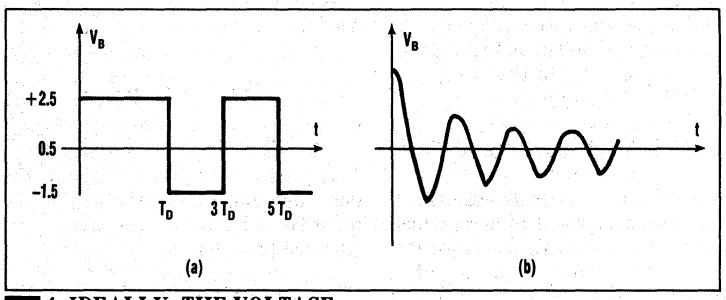

4. IDEALLY, THE VOLTAGE at point B oscillates forever between +2.5 V and -1.5 V (a). In reality, it will be a damped ringing (b).

pacitance of the trace—shouldn't exceed the device's specified capacitive load. Most high-speed logic devices have a maximum loading of 50 pF. As a rule of thumb, the maximum load on any logic element should be no more than four to six devices for best speed/load performance. However, there are some high-slew-rate devices on the market that have higher output drive capabilities.

BEWARE OF AUTOROUTER

The most common reason for not following the board-layout principles mentioned so far is having an autorouter do the layout. Autorouters do what they were designed to do very well: They place traces so as to make the most efficient use of the pc-board real estate. But most autorouters don't have the capability to determine which devices are high-speed and which are not. This is where the logic designer must step in and lay out sections, or islands, of high-speed logic by hand in order to avoid the pitfalls of designing with high-speed logic.

TRANSMISSION LINES

In addition to the common-sense layout considerations discussed so far, designers of high-speed systems must have at least a basic understanding of transmission lines and proper termination techniques *(see "Signal Lines Become Transmission Lines," p. 76)*. The reason: As frequencies go up, wavelengths come down to the point where they are of the same order as circuit-board dimensions. Once that happens, any connection between devices should be considered a transmission line. The lumped-element assumption is simply invalid above that point.

The most common consequence of failing to consider the distributed nature of a high-speed logic board is ringing, which is caused by multiple reflections from the ends of unterminated transmission lines. An unterminated line has no load impedance ($R_L = \infty$) and is therefore an impedance-mismatched line. The behavior of this line when connected to a device with a fast slew rate can be understood from the following example: Prior to time zero, there's a steady-state voltage of 2.5 V dc at all points on the line *(Fig. 3a)*. At t = 0, an initial TTL voltage transition from 2.5 V to 0.5 V occurs at point A *(Fig. 3b)*. Time T_D later, the signal reaches point B and is reflected by the load reflection coefficient, ρ_L.

The input impedance of the device at point B is very high with respect to Z_0; R_L can be approximated by infinity. By plugging into Eq. 2 from the box *(p. 76)*, the reflection coefficient approximately equals +1. In other words, the voltage reflected by the load is equal to the incident voltage *(Fig. 3c)*. The reflected wave passes back along the signal path toward point A *(Fig. 3d)*.

Repeating the calculations for the sending end of the line (point A), where $R_0 \approx 0$, you get a value for the source reflection coefficient, ρ_S, of –1. In other words, there are reflections from the source as well as the load,, but the source reflects the inversion of the wave that is incident upon it *(Fig. 3e)*.

Looking just at the behavior of the signal at point B, the single-step volt-

RULES TO REMEMBER

The following ten rules summarize everything the logic designer needs to know when designing with high-speed CMOS.

1) Keep signal interconnections as short as possible.

2) Use a multilayer PCB.

3) Provide ground and power planes. Discontinuities in the planes should be avoided because reflections can occur from abrupt changes in the characteristic impedance.

4) Fragment the ground and power planes to supply separate sections for high-current switching devices.

5) Use decoupling capacitors on every high-speed logic device (0.1 μF MLC type) located as close to the V_{CC} pin as possible.

6) Provide the maximum possible spacing among all high-speed parallel signal leads.

7) Terminate high-speed signal lines where $t_R < 2T_D$.

8) Beware of ac loading conditions within the design. Exceeding the manufacturer's recommended operating conditions, especially for capacitance, can cause problems.

9) When using parallel termination, put bends in all high-speed signal runs that go to more than one load. Use a termination load at the absolute end of the line.

10) Create islands of high-speed devices on the pc board. This simplifies board layout and ropes-off the high-speed areas.

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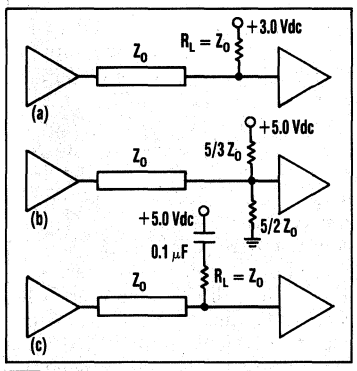


5. THE BASIC PARALLEL termination scheme works well but requires a separate 3-V supply (a). The Thevenin equivalent eliminates the need for a separate supply, but dissipates extra power from the regular 5-V supply (b). The use of a capacitor cuts dc dissipation altogether while supplying ac termination (c).

age transition at t = 0 leads to an endlessly oscillating signal with a total voltage swing of 4.0 V—twice the original level transition. The voltage doubling comes about because the voltage at point B is the sum of the incident and reflected waves at that point *(Fig. 4a)*. Actually, because of the non-ideal nature of a real circuit board (finite input and output impedances, losses in the transmission lines, and so forth), ρ_L will be less than +1, and ρ_S will be greater than −1. As a result, the reflections will become successively smaller, causing the familiar damped ringing condition *(Fig. 4b)*.

If the ringing amplitude is large enough, it can cause the receiving device to see an illegal level transition and possibly result in spurious logic states occupying the logic design. In some cases, the amplitude of the ringing can actually be large enough to damage the input of the receiving device.

TERMINATE YOUR TROUBLES

The way to eliminate ringing on a transmission line is to terminate the line in its characteristic impedance at either the sending or receiving end. The most common way to terminate a line is with a parallel termination at the receiving end *(Fig. 5)*.

In the configuration *(Fig. 5a)*, $R_L = Z_0$ and R_L is pulled up to 3 V dc. In principle, R_L could be tied to ground, but TTL-compatible devices could not then supply the necessary drive.

Solving for ρ_L *(Eq. 2)*, it can be seen that $\rho_L = 0$. Terminating a line in its characteristic impedance results in a reflection coefficient of zero, which means that there will be no reflections or distortions on the line. Other than the time delay, T_D, the line will act as if it were a dc circuit. It's important to note that even though devices or gates may be placed at any location on the line, the terminating resistor should be placed at the end of the line. In no case should the line be split like a Tee to feed several devices in parallel *(Fig. 6a)*. Instead, it should be serpentined to feed them sequentially *(Fig. 6b)*.

The 3-V power source shown *(Fig. 5a)* appears at first to be a major drawback, but R_L and the power supply can be expressed as a Thevenin equivalent running off the system power supply of 5 V dc *(Fig. 5b)*. This variant works well, but the designer should bear in mind that it dissipates additional power.

REDUCING DISSIPATION

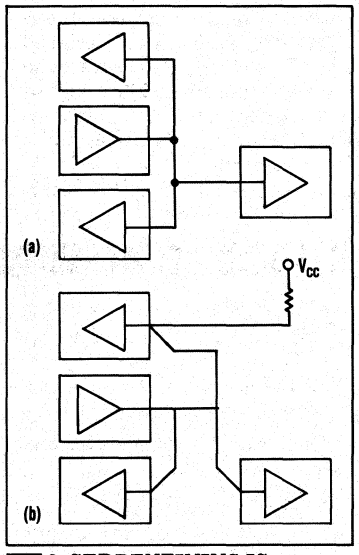
A solution that dissipates less power than either of the others uses a capacitor to cut the dc dissipation to zero *(Fig. 5c)*. The recommended capacitor is a 0.1-μF MLC type. Several manufacturers produce both capacitor-resistor and pull-up/pull-down termination packs. The pull-up/pull-down packs usually come in a single in-line package (SIP) with pins on 0.1-in. centers, while the capacitor-resistor combination comes in a standard 16-pin DIP. The most common SIP pull-up/pull-down resistor values are 220Ω/330Ω, 330Ω/470Ω combinations.

An alternative to a parallel termination at the receiving end is a series termination at the sending end *(Fig. 7)*. The idea behind serial termination is to make $\rho_S = 0$ and $\rho_L = +1$. To do so, R_L is made equal to infinity (left unterminated) and a series resistor is added at the source to make the overall source impedance equal to the characteristic impedance of the line—that is, $R_S + R_O = Z_{OL}$.

Making $R_S + R_O$ equal to Z_{OL}, of course, creates a voltage divider, which puts half of the signal amplitude across the line and half across the series combination of R_S and R_O. Therefore, with the series termination, the amplitude of the transmitted wave is half of what it would be without the termination.

Interestingly enough, the unterminated receiving end of the line precisely compensates for this halving of the amplitude. The reason is as follows: At the receiving end, the half-amplitude wave is received and a half-amplitude wave is reflected. But bear in mind that those are two separate waves whose amplitudes add at the point of reflection. As a result of this addition, the only thing seen at the receiving end of the line is a full-size pulse.

The main disadvantage of a series termination is that the receiving gate or gates must be at the end of the line—no distributed loading is possible. The obvious advantage of a series termination over a parallel one is that a series termination doesn't



6. SERPENTINING IS essential when terminating a line. Never split the line to feed parallel devices (a). Rather, feed them sequentially with a serpentined line (b).

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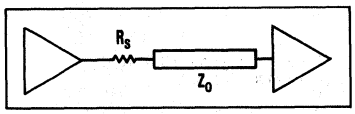
require any connection to a power supply.

Transmission-line effects must be taken into consideration whenever line propagation delays get up to the point where a signal transition can be completed before that signal can travel down a line, be reflected, and travel back to its starting point. In other words, lines must be terminated when,

$2T_D = T_R$.



7. THE SERIES termination needs no pull-up supply. Its main disadvantage is that it can't handle distributed loads.

CALCULATING DELAY

Taking 2 ns as a typical rise time for a state-of-the-art high-speed logic device, how long can a board trace get before its propagation delay gets to be 1-ns long? For a pc board with a continuous ground plane and a signal trace on the adjacent layer, the propagation delay depends on only one variable, the dielectric constant of the board material. That delay time is given by:

$$t_{PD} = 1.017\,(0.475\,e_R + 0.67)^{1/2}\ \text{ns/ft}$$

For a typical board constructed of FR4 material, e_R (the dielectric constant) is 4.7 to 4.9. If an average e_R of 4.8 is used in the equation, then t_{PD} turns out to be 1.75 ns/ft, which works out to 6.86 in./ns. As a rule of thumb, then, any line that is over 7 in. long should be considered a transmission line and approached accordingly.□

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Extending the 22V10 EPLD

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An extendable device family allows gate and I/O counts to be boosted without major changes in board layout

The 22V10 device architecture is now one of the industry standards in programmable logic devices. The 22V10 owes its popularity to a number of architectural features that bring versatility and flexibility to system design. The Output Logic Macro-Cell (OLMC) is perhaps the most revolutionary feature of the 22V10 architecture. OLMCs eliminate such architectural constraints as insufficient product-term access, fixed output polarity, limited three-state control, and poor control of registered outputs. The OLMC at any device I/O pin is functionally identical to any other. Additionally, any I/O can be used as a feedback path into the AND array.

Asynchronous reset is another attractive feature of the 22V10. One reset signal is common to all registered OLMCs and operates independently of the dedicated clock input. This signal is taken from the AND array and may be generated via a product term. Registered OLMCs respond immediately to a reset signal. In addition, one preset signal is common to all registered OLMCs and operates on the arrival of a valid clock input. This signal is taken from the AND array and may be generated by a product term. Registered OLMCs respond only on the arrival of a valid clock input.

Along with a minimum of eight product terms per OLMC in all modes, two outputs have access to 10 product terms per OLMC in all modes, another two have access to 14 product terms, and the center two outputs have access to 16 product terms. Each OLMC's output driver has a unique enable/disable signal that is taken from the AND array and that may be generated via a product term. All OLMCs respond immediately to the arrival of a valid enable signal generated externally or internally.

The three members of Lattice's GAL22V10 series—the GAL18V10, GAL22V10, and GAL26CV12—are high-speed, EECMOS PLDs. Each is based on the standard 22V10 architecture; their differences involve the number of I/Os, pins, and product terms offered. The GAL18V10 is a 20-pin version of the 24-pin GAL22V10. It contains eight dedicated input pins (four less than the 22V10) and 10 I/O (the same as the 22V10). The 28-pin GAL26CV12 has two more dedicated input pins and two more I/O pins than the GAL22V10. The GAL26CV12 in a PLCC package requires no more space than many lower-density PLDs.

The EECMOS GAL18V10 and GAL26CV12 consume just 75 mA and 90 mA typical I_{CC}, respectively—50 percent less power than bipolar alternatives. The programmable AND arrays are proportional to the pin count of each device. The arrays are 96 × 36, 132 × 44, and 122 × 52 for the GAL18V10, GAL22V10, and GAL26CV12, respectively.

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The first job that a designer has in selecting the right 22V10 device for a system is to evaluate the size and complexity of the design as well as system speed and power requirements. PLDs excel in applications that have a number of SSI parts with low gate counts and combinational logic that optimally fit into a single device.

The GAL18V10 features an equivalent gate count of 450 to 550 gates, along with eight to 18 inputs and one to 10 outputs. The GAL22V10's equivalent gate count is 550 to 750 gates; it offers 12 to 22 inputs and one to 10 outputs. The GAL26CV12 has an equivalent gate count of 650 to 850, 14 to 26 inputs, and one to 12 outputs. If a design has a fairly low gate count and relatively small I/O requirements, the GAL18V10 is the best choice. Should additional inputs be required without any additional output requirements, the best place to start is the GAL22V10. If gate count, input, and output requirements are large, the GAL26CV12 is recommended. For designs with larger requirements, some combination of the three devices will meet design needs.

The final stages of the evaluation cycle often reveal problems with a design. Typically, such problems include the omission of a critical input signal or a need for more output signals. Such adjustments are best accomplished by repatterning the fuse map of the PLD. This type of design fix is limited by the number of unused PLD pins available and by the flexibility of the PLD's internal fuse-map array. If the PLD has not been fully used, a new fuse-map pattern can often be implemented without any board-level redesign. If additional I/O is necessary, however, additional parts usually are needed.

The GAL22V10 family is well suited for situations in which greater overall complexity and lower power consumption must be achieved without a corresponding increase in device count or real estate use. With an extendable family, gate and I/O count can be boosted without major changes in board layout.

When designers are under pressure to produce a design quickly, the design cycle is much more chaotic. Many times, a designer will simply grab the closest part and use either single parts or multiple parts to build the circuit. When the final product has been in production for a few months, the manufacturing-engineering group then must come to grips with the challenge of cost reduction. In some cases, these cost-reduction efforts can also result in reliability gains and performance enhancements.

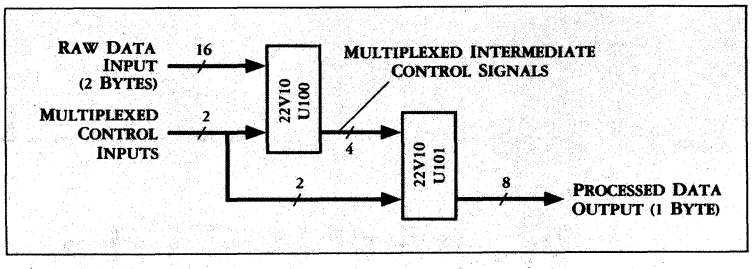

Figure 1. In this example, two 22V10 devices are needed to provide enough inputs and outputs for a state machine.

For example, suppose a designer, in a rush to build a state machine for control in a pipeline application, used two 22V10s to implement the function (Figure 1). The objective of the design is to take 16 data-input bits and two control bits to generate eight data-output bits. In the first device, 16 data inputs and two control inputs were used to generate four encoded outputs. Since the first device was output-bound, only four of the eight required data bits could be generated. The second device was used to take the four encoded outputs from the first device and the two control inputs to generate the required eight data output bits.

The above design can be implemented in a single 26-pin device (Figure 2). The 16 data-input bits and the two control bits are fed directly into the GAL26CV12, and the remaining two pins can be used for the required eight data-output bits. Not only does this approach offer the obvious advantage of reduced board space, it also saves more than 0.5 W of power and removes an entire package delay. Enough power reduction can mean power-supply cost savings and an indirect increase in board reliability. Performance enhancement results in an extension of the life of an already mature system.

■ A 10-Bit Counter Design

A second design example involves a standard 10-bit counter. A 10-bit counter can be used to provide location-by-location access of up to 1,024 addresses or to provide divide-by-two to divide-by-1,024 clock frequency reduction and distribution. A 10-bit counter can also be used to identify up to 1,024 sequential edge-identified events.

These counters generally are implemented in one of two ways—with multiple 20V8 devices or with a single 22V10 device. If a 22V10 is used, enough inherent flexibility remains for the implementation of asynchronous reset and synchronous preset functions. For a 10-bit counter built with a 22V10 that generates an output for every clock phase, which is appropriate for the implementation of a "watchdog" timer function for real-time activities, eight dedicated inputs remain unused. If that same counter were built with a 20-pin GAL18V10, four pins of real estate could be saved and power use cut by 0.5 W.

Suppose that same 10-bit counter is used to signal the "half-full" and "three-quarter full" points of a 1,024-location circular buffer. Two independent event codes will be needed to decode and generate single clock-width pulses at these two points in the buffer.

Such a part requires 12 outputs. Previously, multiple 22V10 devices or the combination of a 22V10 component and another PLD have been used for the task. Now, the part can be built with a single 28-pin GAL26CV12, yielding a power savings of about 1 W and eliminating one package delay. ■

About the Authors

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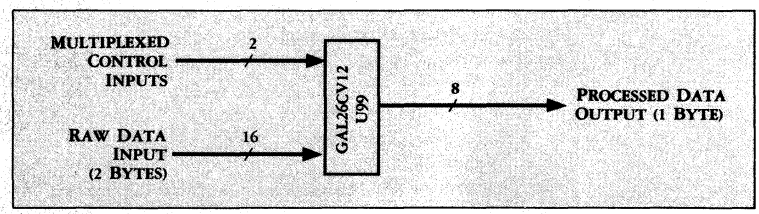


Figure 2. Here, a single 26CV12 replaces two 22V10s and reduces delays and power-supply requirements.

ELECTRONIC DESIGN EXCLUSIVE

In-circuit logic device can be reprogrammed on the fly

Compatible with 5-V systems, an EEPROM-based chip allows designers to update systems in situ, with 100% testing and observability.

Of the multitude of ways available for reconfiguring logic systems on circuit boards, none has ever proved entirely satisfactory. Changing dozens of DIP switches or jumper settings manually can be a nightmare. Electrically erasable or battery-backed memory can do the job at least in part, but the use of memory bits is limited in most cases to controlling signal flow in the parts of a system where speed is not critical.

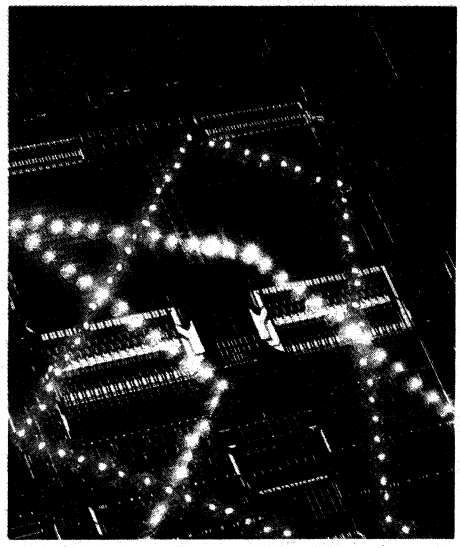
Memory bits do have their place in controlling such tasks as decoding I/O ports, enabling and disabling features, and selecting a memory bank, but those jobs are mutually exclusive: Designers have to decide which one they want to control through the use of memory.

The few logic devices now using UV EPROM cells cannot be reprogrammed without being removed from the system. Nor, if sealed in windowless plastic packages, are such chips 100% testable. Even with windows, they usually have to be removed from the board for erasing and reprogramming, because the 12- to 21-V programming voltage risks damage to other components on the board. Other difficulties can arise too with these techniques, such as mechanical switch failures, wire breaks or shorts, dead batteries, and mishaps that occur when technically unskilled users try their hand at reconfiguring or fixing circuitry.

A new 24-pin chip does away with all those pitfalls. By combining programmable logic circuits with 5-V electrically erasable CMOS memory, it opens up all kinds of options in reconfiguring a system. The ispGAL16Z8 not only is reprogrammable in circuit but also is 100% testable—a big plus. Propagation delays of a mere 25 to 35 ns mean that the reprogrammable device can be used in data paths where speed is critical, so that even the system's basic logic flow can be altered in an instant.

The chip is the first in a planned family of in-system reprogrammable devices, and its flexibility is limited only by the designer's imagination. Logic designers need not be restricted to that last etch on the board, and final testing no longer presents so many problems.

Because the new chip combines CMOS with electrically erasable floating-gate and high-speed logic, it runs at speeds associated with bipolar chips, but consumes significantly less power—450 mW maximum and 350 mW on standby—than do most bipolar chips. The 16Z8 is similar to the company's earlier programmable logic device, the 20-pin GAL16V8. Four additional pins in the 16Z8 control in-system programming and diagnostic testing (Fig. 1). A proprietary state-machine–based interface controller on the chip handles all programming and testing. It also makes possible, through the four pins, the in-system observability and controllability



5

that are such powerful diagnostic aids.

Like the 16V8, the new chip has a core consisting of a standard AND array plane and eight programmable output logic macrocells; it adds 5-V E²CMOS programming circuitry. Each programmable output macrocell gives the designer five configuration options, among them output polarity (active high or active low), feedback, combinatorial logic, registered outputs and input selection. Either all the outputs are connected to one Output Enable signal, or separate product terms provide individual enabling controls.

The new chip also emulates all common 20-pin architectures similar to Monolithic Memories' programmable array logic. Its programming software and hardware support come through the standard PLD development packages. Because its fuse map is compatible with that of the older chip, the new chip accommodates the latter's software. (Data I/O is the first third-party vendor to offer updated programming; other companies are expected to follow suit shortly.)

SERIAL PORT SIMPLIFIES INTERFACE

The new chip can be programmed over a −55°C to −125°C operating range and can undergo at least 10,000 erase-write cycles. Given its 100% reprogrammability, yields of 100% in ac and dc parameters are guaranteed, as is a programming time of less than 1 second. The 5-V programming circuitry generates the necessary higher voltages internally and also shapes waveforms so that the device can be programmed through the four-pin interface without high-cost, high-voltage external hardware.

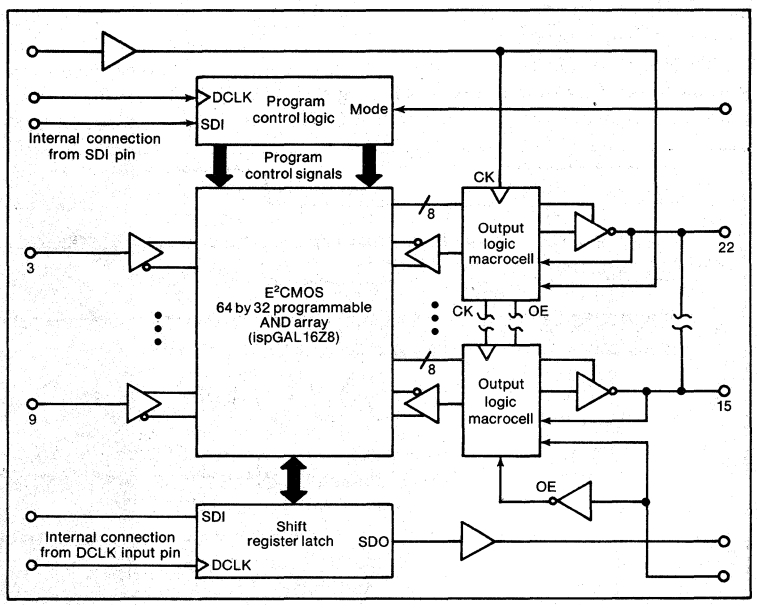
The four-pin interface controlling programming and diagnostics is compatible with Monolithic Memories' JEDEC-standard "diagnostics on chip." By eliminating multiplexed data paths, the interface optimizes data propagation. It has four basic functions: diagnostic preload, program shift, program read, and program write. The chip's state machine controls the sequence with information from three of the four signal pins: Serial Data In (SDI) for programming; Mode for loading; and Diagnostic Clock (DCLK) for diagnostics. The fourth pin, Serial Data Out (SDO), for data shifting, comes into play when the serial scan data has to be expanded into a loop (Fig. 2).

When the chip receives a Power on Reset signal, the state machine resets to the normal state to prevent unwanted writes at power-up. A user-controlled Reset signal makes the state machine move to the normal state from any state when the Mode pin is a logic 1, SDI is a logic 0, and DCLK has a rising edge.

The four interface signals are relatively simple to gen-

Typical write programming sequence

	Enter programming states from the normal state
Step 1	Mode is TTL high; SDI is TTL high; DCLK is clock Diagnostic: Preload state (just passing through)
Step 2	Mode is TTL high; SDI is TTL high; DCLK is clock Program: Shift state
Step 3	Mode is TTL low; SDI is address and data bits; DCLK is clock Program: Shift state (Load shift register latch with 82 data bits and 6 address bits) (Note: SDO data field is "don't care")
Step 4	Mode is TTL high; SDI is TTL high; DCLK is clock Program: Read state (just passing through)
Step 5	Mode is TTL high; SDI is TTL high; DCLK is clock Program: Write state (Write begins immediately upon entering Program: write state) (Time-out write pulse)
Step 6	Mode is TTL low; SDI is TTL high; DCLK is clock Program: Read state (End write)
Step 7	Mode is TTL low; SDI is "don't care"; clock is DCLK Program: Shift state (Read address; execution of verify; shift register latch is loaded)
Step 8	Mode is TTL low; SDI is next 88-bit word; clock is DCLK. Program: Shift state (Shift out 82 data bits and 6 address bits; observe SDO)
Step 9	Repeat steps 4–6 for each row address of verification



1. The 24-pin ispGAL16Z8 starts with an E²CMOS programmable AND array at its core and eight output macrocells. Then it adds a serial diagnostic and programming port and 5-V programming circuitry.

erate, needing only the output ports of a standard single-chip microprocessor and a little support software. A typical serial scan programming-and-diagnostic control loop can take on a system with several devices (Fig. 3). In its normal state, the 16Z8 works like a standard PLD, remembering the last update to the E^2CMOS logic and functioning in the system as programmed. In the diagnostic preload state, the chip latches the macrocells' presen condition and, with DCLK, lets diagnostic test information move from SDI to SDO. SDI is loaded into the least significant output register on DCLK's rising edge. Most significant register data is shifted out through SDO. When the chip returns to normal, its outputs resume their preload state.

SHIFT, READ, AND WRITE

In the program shift state, one row of data in the array is shifted into SDI, with the appropriate array data moving first, followed by the row address field. To configure a device completely, each array location must be filled with the appropriate data. Any data already in the serial shift register is shifted out through SDO for cascading or for verifying a device.

In the program read state, one row of the array is transferred in parallel into the serial shift register, whose contents are transferred out of the selected row in the array. Returning the chip to the program shift state loads the shift register and lets the user verify the device. However, if the chip goes to the program write state, the register's data is programmed to the selected row in the array and its contents remain unchanged.

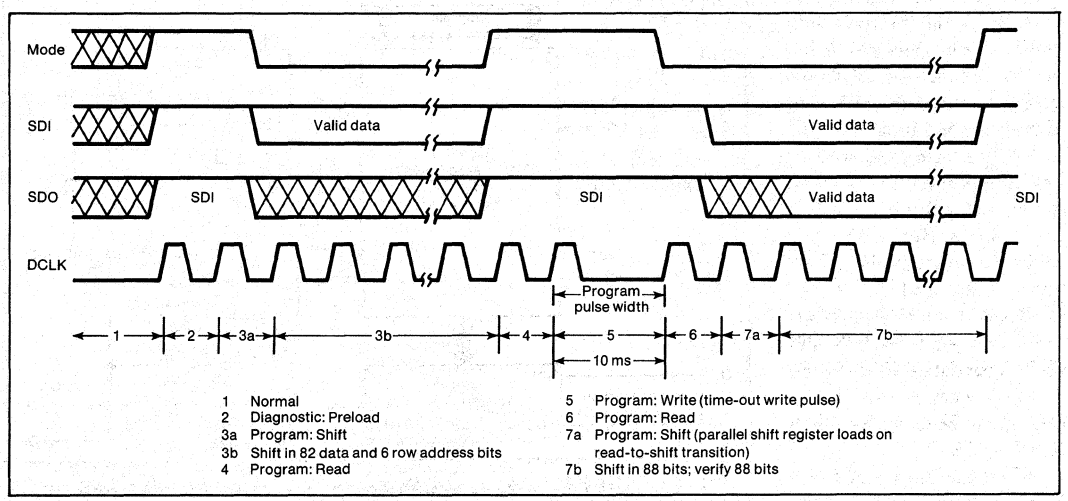
In the program write state, one row of the array is programmed with data from the serial shift register. Programming begins on one leading edge of the DCLK signal and ends on the next; the user must maintain the correct 10-ms programming timing (see the programming sequence, p. 95).

The chip's in-circuit reprogrammability makes possible the design and programming of generic hardware for specific applications. Small-volume system manufacturers can blend several lines of hardware into one, simply by updating the firmware. The fast system upgrades can even be predesigned into a system and enabled later by reprogramming.

ACHIEVING FLEXIBILITY

On-the-spot reprogramming maintains the integrity of a system's hardware, eliminating the need for field service or for returning the chip to the maker for upgrading or replacement. Upgrading can be done in the field by software delivered electronically or by mail, whichever is more convenient. Furthermore, the chip is programmed through the serial scan path, so that system diagnostics are easy to do, either locally or from a remote host system. Repair time and costs can be cut without significant impact on the system's cost or complexity. Since the chip's serial scan path is compatible with the ports in other commercial ICs, a complete system, including logic, can use these powerful and flexible diagnostic techniques.

Two design examples—a programmable two-output, 16-bit input selection decoder and a programmable output port—show off the 16Z8 chip's best points. Normally



2. During chip programming, just four lines transfer all data and perform diagnostics, ensuring that bit patterns are properly loaded.

a decoder's circuitry includes such standard logic as address comparators, DIP switches, and pull-up resistors. The pull-up resistors guarantee noise immunity at the comparator when a switch is off.

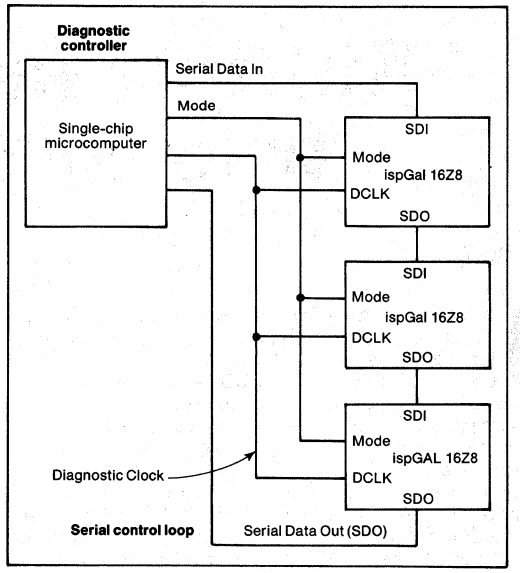
The decoder compares a 16-bit address from a microprocessor with a preset address held in the set of DIP switches. Decoding the two outputs requires four comparators, four octal DIP switches, and four octal resistor packs. In addition, the circuit needs 104 solder connections and 32 switch contacts, all subject to mechanical wear and tear.

A single 16Z8 can implement the same decoder. Switches controlling the address selection functions are internal and, in fact, are the product terms in the AND array. All programming occurs through the four-pin serial interface, and address selection updates are handled through reliable interactive software, rather than through a production-line assembler that uses a factory-standard DIP-switch programming pencil. Moreover, there are only 24 solder connections and no switch contacts, which substantially improves reliability and calls for a much smaller board area.

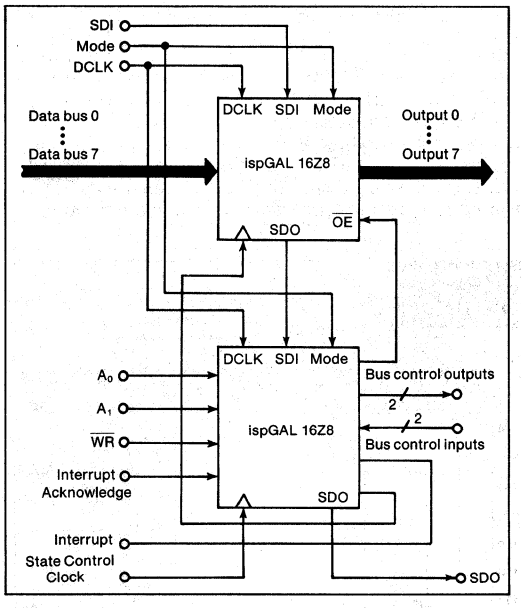
WORKING TOGETHER

The second application, a reconfigurable output port, gives systems wide flexibility and can be put together easily. In this setup, two chips work together, one for the output data path and the other for the microprocessor bus and output-port control paths (Fig. 4). The data path can be configured for registered, combinatorial, or latched outputs, and each output bit can be either active high or active low. Other Boolean logic manipulations are possible with the logic in the chip's AND array.

The control-path device handles the other chip's Clock and Output Enable signals, and its inherent logic can implement virtually any microprocessor or output port interface protocol. Interfaces may be synchronous or asynchronous, and each signal set up individually as a registered or combinatorial output, active high or active low. The interface can be programmed through the serial scan programming interface ICs. Thus a single interface is all that is necessary to tie into many different kinds of peripherals. □



3. Through the four-line serial port, several logic chips can tie into one diagnostic controller for board-level troubleshooting. Preloading the output registers affords rapid testing of programmable devices, since the logic-based circuit can be made to start at any desired state.



4. A programmable output port can be readily formed using two ispGAL16Z8s. The top one sets up the data path, the bottom one handles interface control and external handshaking. The output situation is very flexible; data can be configured in several ways.

Multiple factors define true cost of PLDs

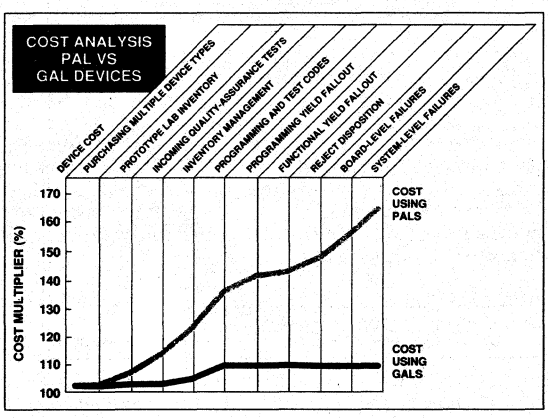
By DEAN SUHR

Designers using PLDs (programmable logic devices) for system design and manufacturing traditionally think of piece price as the key consideration in the PLD selection process. Thanks to recent advances in technology, however, the system cost of using PLDs is influenced by factors such as fabrication technology, device quality, reliability and yield.

System cost is quite different from the sum of the component costs. The price paid for a device or component represents only one part of the system cost of a PLD; the systems team also has to consider the costs hidden in the programming, handling, quality control, throughput and overhead that's necessary to get a "raw" PLD to a functional state on a board.

Because the true system cost of a PLD is the sum of the piece price and all of these hidden costs, and is spread over several functions and departments, it's often difficult to define and measure. In most companies, for example, purchasing and engineering define the parts list and acquire the parts. These departments are often under pressure to reduce absolute unit cost and to purchase the least-expensive part available.

But the profitability of both the product line and the company is based not on device acquisition cost but on total system cost. Buying the least-expensive part may not provide the lowest total system cost.



Programmability can play a significant role in the total cost of PLDs. The example above was taken from a system that used 100,000 bipolar PLDs per year. Moving to E²CMOS GALs can reduce total cost by up to 34 percent.

Hidden cost factors

To calculate the system cost of using a particular PLD type, vendor and technology, managers must also take into consideration the additional costs of purchasing overhead, inventory management, prototype inventory and quality assurance (QA). Purchasing overhead can add 2 percent to the actual device cost. As the number of inventory line items rises, the overhead needed to purchase those items increases. PLDs with generic architectures can minimize the number of different devices a company must purchase, and therefore reduce purchasing costs.

As much as 10 percent of a device's cost can be attributed to inventory management overhead, including shelf space, depreciation, count management, obsolete write-offs, and safety stock. Reducing inventory line items simplifies the management overhead, in turn cutting costs.

BY ELIMINATING YIELD AND HANDLING LOSS, IMPROVING QUALITY, AND SIMPLIFYING INVENTORY MANAGEMENT, DESIGNERS CAN CUT THE TRUE COST OF USING PLDS

PLDs are particularly adaptable to just-in-time (JIT) inventory management systems, which minimize inventory by increasing throughput. Using a JIT system constrains a company's flexibility because the company must carry fewer items. But adding PLDs to the inventory will let the same narrow range of products provide a wide variety of functions.

Macrocell-based PLDs also have increased the flexibility of companies that use them and reduced stocking requirements. In the past, designers using fixed-architecture PLDs had to keep in stock every PLD architecture required for a design. Macrocell-based devices, on the other hand, can be configured to emulate dozens of old architectures and many new configurations.

The macrocell used in E²CMOS generic array logic (GAL) devices goes one step further. These devices also offer 100 percent socket compatibility with older programmable array logic (PAL) architectures, so designers can simply substitute the GAL device for the old PLD architecture. No redesign is necessary. Existing JEDEC files and master devices can be used, reducing system cost.

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No longer a simple calculation, the system cost of using programmable logic devices is affected by their fabrication technology, testability and impact on inventory management.

The cost of the prototype inventory also influences total system cost. Although engineering labs are stocked with devices for building and debugging prototypes, many companies meet engineering lab shortages by borrowing from manufacturing stock. This policy can shrink manufacturing inventories and, by doing so, can increase the system cost of the remaining manufacturing units by as much as 1 percent when units are ordered to restock the shelves.

All PLDs have a programmable element that determines their functionality and ac/dc performance. These programmable elements can be fabricated from metal-link fuses, programmable diodes or transistors, volatile static RAM cells, UV EPROM cells or EEPROM cells. Each of these technologies varies in programmability and has a different impact on device performance and reliability.

Each programmable element also offers a different erase capability. Metal-link and one-time-programmable devices, for instance, can't be erased. UV EPROM devices can be erased, but this process requires an expensive windowed package and takes 20 to 30 minutes. EEPROM devices offer instant erasability in as little as 50 ms. Technologies that aren't erasable or that have lengthy erase times constrain test flexibility and may add to the total system cost.

Finally, PLDs are usually subjected to a complete, electrical QA test upon receipt, which typically adds 7 percent to the device cost. This additional cost is based on test engineering and manufacturing resources, yield and equipment utilization. Manufacturers can avoid this additional expense without degrading device quality, by using E²CMOS devices. These devices are 100 percent pretested by the manufacturer, and require no incoming test. And their instant erasability lets IC manufacturers perform extensive tests at the manufacturing stage, prior to shipment to end-users.

Some companies, however, have extensive incoming QA operations that can't be eliminated. Reusable E²CMOS devices are ideal for these operations because they can be returned to manufacturing inventory after QA testing, instantly reprogrammed, and reused in production boards. This flexibility also lets QA engineers perform their inspection at any step in the process.

QA engineers can also simplify their testing by using generic-architecture, macrocell-based devices. These devices can be tested with one common test program and then configure in many ways during the programming operation. This step eliminates the generation and maintenance of multiple test programs and fixtures, one for each fixed architecture.

Analyzing the system cost

Managers can reduce these overhead costs to a formula based on a simple approach that assumes a percentage cost adder and yield factor for each operation: $Cost_n = Cost_{n-1} + (Cost_{n-1}/Yield_n)$. This formula is generic, so managers can tailor the factors to their specific environment and then analyze the actual system cost of using a particular PLD.

E²CMOS PLDs offer performance, quality, reliability and, most important, cost advantages over alternative solutions. By eliminating yield and handling loss, improving quality, and simplifying inventory management, designers can significantly reduce the true cost of using PLDs.

Dean Suhr is product marketing manager at Lattice Semiconductor, Hillsboro, OR.

The Factor of Ten rule

It's crucial that managers keep in mind the cost of detecting and repairing defective PLDs during manufacturing — and the importance of early detection. A common guideline for determining this cost is the Factor of Ten rule.

This rule states that the cost of detecting and repairing a defective PLD grows by a factor of ten at each subsequent stage in the manufacturing process. This dramatic growth rate is possible because other symptoms mask the PLD's faulty functionality as the device is buried deeper in the system.

The Factor of Ten rule implies that the earlier defective devices are caught, the lower the repair cost. If defects aren't found early, a very small yield loss can be greatly magnified by the quantity of devices on a board or in a system. Even a yield loss as small as 0.5 percent can result in a 5 percent system failure rate with only five PLDs per system. A loss of 0.5 percent translates to a defect rate of 5,000 ppm, a high defect rate.

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COPYING PAL PATTERNS INTO GAL DEVICES

INTRODUCTION

The generic architecture of the GAL family offers the user many different device configurations. For example, the GAL16V8A has the ability to emulate 21 of the most popular 20-pin PAL devices. To put it simply, the GAL16V8A is functionally, parametrically, and fuse map compatible with all common 20-pin PAL devices. Table 1 lists the PAL devices that the GAL16V8A can replace. Table 2 shows the 21 different 24-pin PAL devices that the GAL20V8A can fully replace. This technical brief addresses the procedure of copying a PAL pattern - either a PAL master or a PAL JEDEC file - into a GAL device.

The technique of copying a PAL into a GAL device is straightforward, since existing JEDEC files or PAL masters can be used without modification. Other devices that only emulate PAL architectures may require access to source equations and/or design modifications. The Lattice approach has been to allow customers the ability to "cross program" a PAL pattern without having to change the programming procedure, master device, or JEDEC file.

A Lattice GAL16V8A or GAL20V8A device configured to emulate a PAL architecture is referred to as a RAL device. There is a one-to-one correspondence between PAL architectures and RAL architectures (see figure 1 and 2). GAL22V10 and GAL20RA10 devices are 100% JEDEC map compatible with their UV and bipolar fuse counterparts.

GAL16V8A PAL Architecture Emulation
16L8
16H8
16R8
16R6
16R4
16P8
16RP8
16RP6
16RP4
10L8
12L6
14L4
16L2
10H8
12H6
14H4
16H2
10P8
12P6
14P4
16P2

TABLE 1: PAL Architectures Emulated by the GAL16V8A

GAL20V8A PAL Architecture Emulation
20L8
20H8
20R8
20R6
20R4
20P8
20RP8
20RP6
20RP4
14L8
16L6
18L4
20L2
14H8
16H6
18H4
20H2
14P8
16P6
18P4

TABLE 2: PAL Architectures Emulated by the GAL20V8A

GAL16V8A AND GAL20V8A

COPYING A PAL MASTER INTO A GAL16/20V8A

If a programmed PAL is available, and is one of the devices listed in Table 1 or Table 2, all that is needed to copy a PAL pattern into a GAL device is a qualified GAL programmer .

1) Place the PAL device into the programmer and read the PAL using the normal procedure.

2) Select the appropriate RAL family/pinout code for the PAL being emulated. Note: the RAL code is required for PAL device copying in order to con figure the architecture properly. Do not use the GAL device code for copying PAL devices.

3) Place the GAL device into the programmer and program the GAL device using the appropri ate RAL family/pinout code. The copy procedure is complete and the resulting GAL device is 100% compatible with the PAL device it copied.

COPYING A PAL JEDEC FILE INTO A GAL DEVICE

If a JEDEC file for one of the PAL devices listed in Table 1 or Table 2 is available, again all that is needed is a qualified GAL programmer.

1) Select the appropriate RAL family/pinout code for the PAL JEDEC file that is to be downloaded to the programmer. Note: the RAL code is required for the programmer to configure the architecture properly. Do not use the GAL device code when downloading a PAL JEDEC file.

2) Download the PAL JEDEC file from a computer to the programmer using the normal procedure.

3) Place the GAL device into the programmer and program the GAL device without changing the family/pinout code. The programming procedure is complete and the resulting GAL device is 100% compatible with the PAL device being emulated.

GAL22V10 AND GAL20RA10

The 100% JEDEC map compatibility of the GAL20RA10 and GAL22V10 devices allow existing PAL JEDEC files and master devices to be copied into the GAL device without modification.

1) Place the PAL device into the programmer and read the PAL using the normal procedure.

2) Select the appropriate GAL family/pinout code for the PAL being emulated (see Notes).

3) Place the GAL device into the programmer and program the GAL device using the GAL family/ pinout code. The copy procedure is complete and the resulting GAL device is 100% compatible with the PAL device it copied.

NOTES

•Some programmers use different names for "family/ pinout code." "Select codes," "algorithm" or menu selections are interchangeable.

•Programming PAL patterns into GAL devices is not unlike copying a PAL pattern from PAL vendor A to PAL vendor B. The difference is that you must have a generic GAL device in the socket with a specific RAL architecture code selected.

•JEDEC files compiled with GAL16V8A or GAL20V8A target devices should be programmed with GAL device codes selected.

•The GAL22V10 code emulates PAL22V10 devices directly (no RAL code is required).

•The GAL20RA10 code emulates PAL20RA10 devices directly (no RAL code is required).

•After programming, the GAL device still retains its full erasability feature. The device can be reused with different array patterns and architecture configurations, as selected by the designer.

GAL DEVELOPMENT TOOLS

Introduction

The Tools Engineering Group at Lattice Semiconductor works closely with hardware and software vendors to insure programming support for GAL devices is available in a timely manner.

Lattice works with a variety of programming vendors to satisfy your needs, whether you need a low-cost programmer, an engineering programmer, or a production programmer.

For a current list of Lattice qualified GAL programmers, please contact Lattice's Applications Engineering Department (Tel: 503-681-0118, or FAX: 503-681-3037).

Benefits of Using Lattice Approved Programmers

Lattice provides one of the most extensive review and qualification procedures in the industry. When Lattice approves a programmer, you are insured that it conforms to all programming procedures and specifications. In addition, programmers qualified by Lattice adhere to the latest JEDEC communication standards.

The use of unapproved equipment will void all warranties, including quality, reliability and data retention.

Below are lists of programmer manufacturers and software developers that provide Lattice qualified GAL development tools.

PROGRAMMER MANUFACTURERS

Data I/O Corp.
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
Phone: (206) 881-6444
FAX: (206) 882-1043
In Europe contact:
Data I/O Corp.
Phone: +31 (0) 20-6622866
In Japan contact:
Data I/O Corp.
Phone: (03) 432-6991

Promac Data Systems
516 Imaiminami-Cho,
Nakahara-ku
Kawasaki-City, 211 Japan
Phone: 044-711-0022
In the U.S. contact:
Adams • McDonald Corp.
Phone: 1-800-777-1202
FAX: (408) 373-3622

Kontron
630 Clyde Ave.
Mountain View, CA 94039
Phone: (415) 361-1012
FAX: (415) 965-3505

Logical Devices
1321 N.W. 65th Place.
Fort Lauderdale, FL 33309
Phone: (305) 974-0967
FAX: (305) 974-8531

SMS Micro Systems
1M Morgenthal
D-8994 Hergatz
Scwarzenberg
W. Germany
In the U.S. contact:
Adams • McDonald Corp.
Phone: 1-800-777-1202
FAX: (408) 373-3622

Stag Microsystems
Martinfield
Welwyn Garden City
Hertz. AL7 15T
United Kingdom
Phone: (0707) 332148
FAX: (0707) 371503
In the U.S. contact:
Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
Phone: (408) 988-1118
FAX: (408) 988-1232

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P.O. Box: 53-591
Taipei, Taiwan R.O.C.
Phone: 886-2-7212613
FAX: 886-2-7212615
In the U.S. contact:
System General
510 South Park Victoria Dr.
Milpitas, CA 95035
Phone: (408) 263-6667
FAX: (408) 262-9220

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Accel Technologies
6825 Flanders Dr.
San Diego, CA 92121
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FAX: (619) 554-1019

Capilano Computing
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North Vancouver, BC
V7L 4P6 Canada
Phone: (604) 669-6343

Data I/O / FutureNet
10515 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073
Phone: (206) 881-6444
FAX: (206) 882-1043

ISDATA GmbH
Haid-und-Neu-Straße 7
7500 Karlsruhe 1
West Germany
Phone: 0721-693092
FAX: 0721-174263
In the U.S. contact:
ISDATA Inc.
Phone: (408) 373-7359
FAX: (408) 373-3622

Logical Devices
1321 N.W. 65th Place.
Fort Lauderdale, FL 33309
Phone: (305) 974-0967
FAX: (305) 974-8531

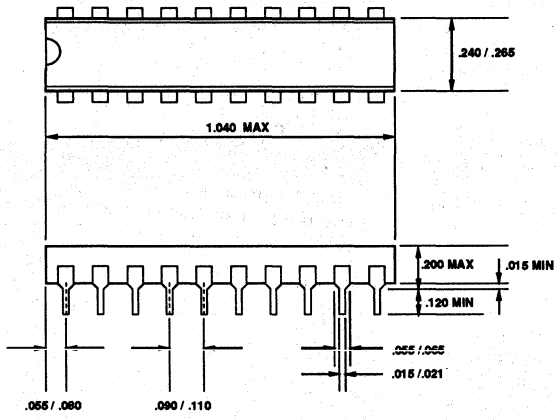
Minc Incorporated
1575 York Rd.
Colorado Springs, CO 80918
Phone: (719) 590-1155
FAX: (719) 594-4708

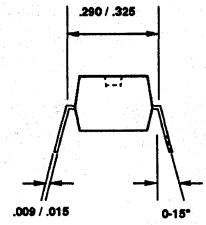
OrCAD Systems Corp.
3175 N.W. Aloclek Dr.
Hillsboro, OR 97124
Phone: (503) 690-9881
FAX: (503) 690-9891

PACKAGE DIAGRAMS

20-Pin Plastic DIP

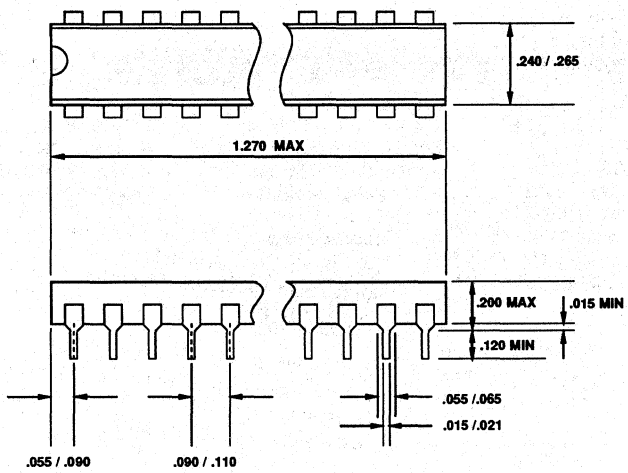
Dimensions in Inches MIN. / MAX.

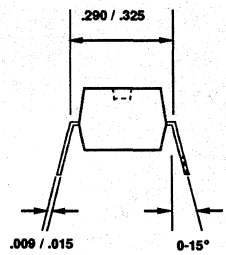




24-Pin Plastic DIP

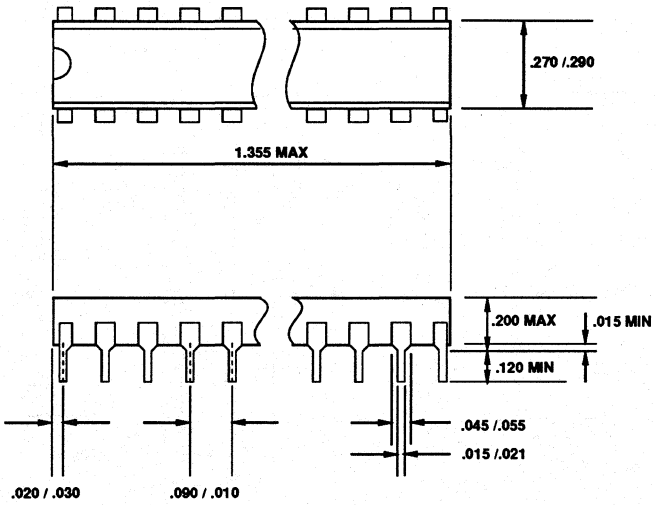
Dimensions in Inches MIN. / MAX.

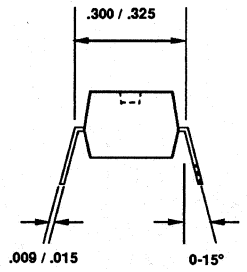




28-Pin Plastic DIP

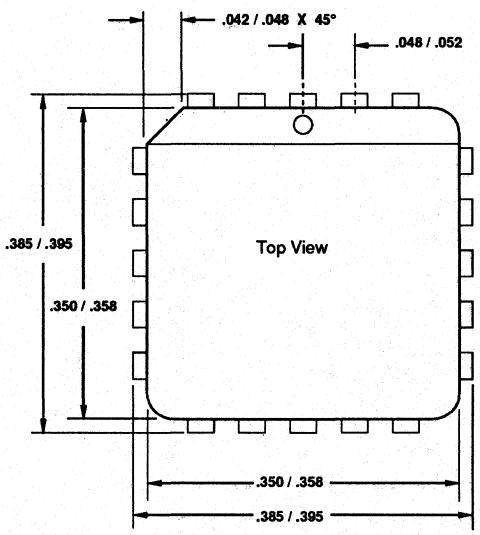
Dimensions in Inches MIN. / MAX.

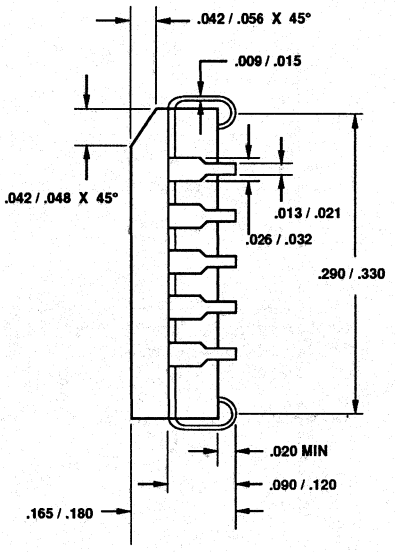




20-Pin PLCC Package

Dimensions in Inches MIN. / MAX.

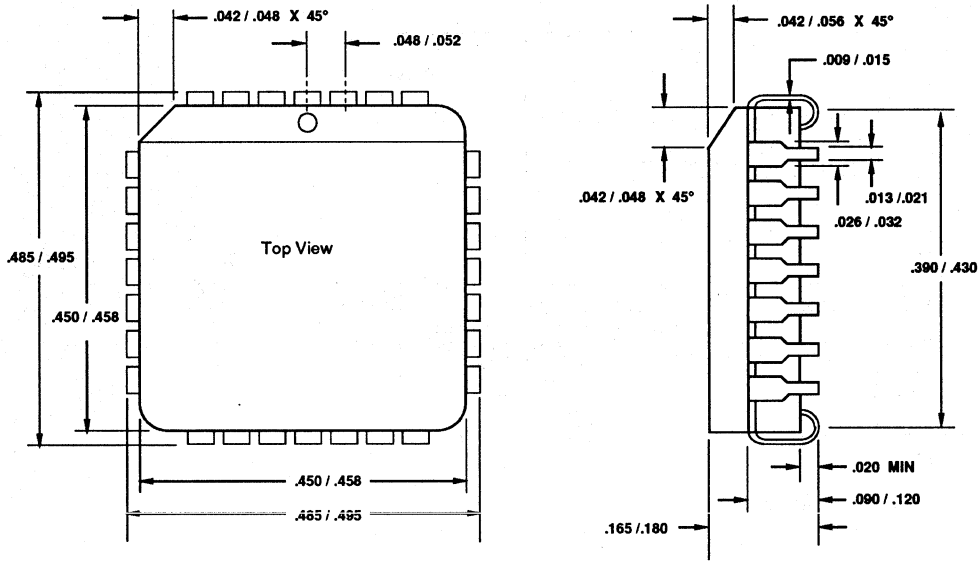




6

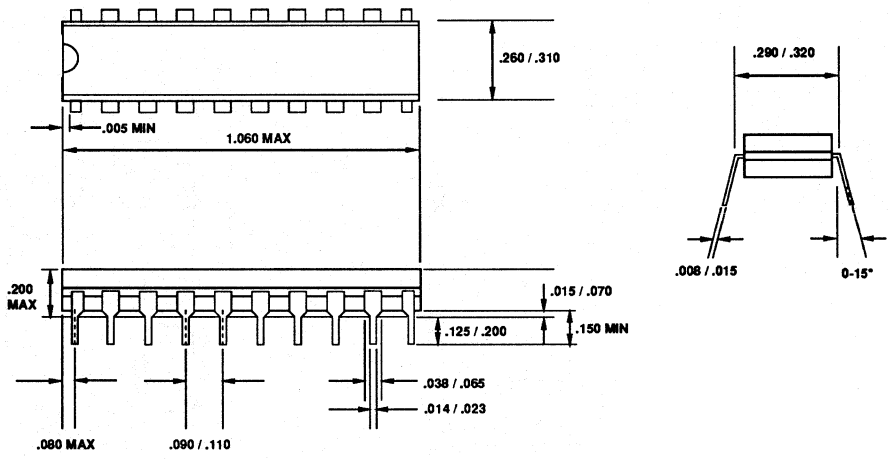
28-Pin PLCC Package

Dimensions in Inches MIN. / MAX.



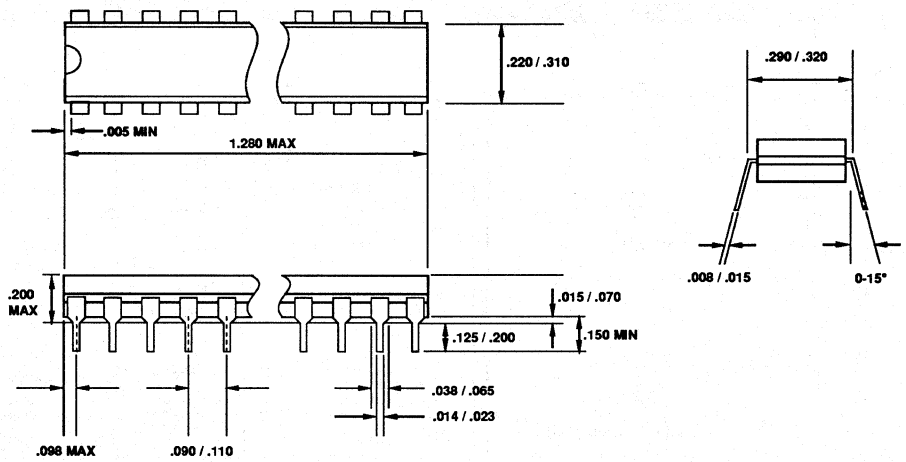
20-Pin (300 MIL) CERDIP

Dimensions in Inches MIN. / MAX.



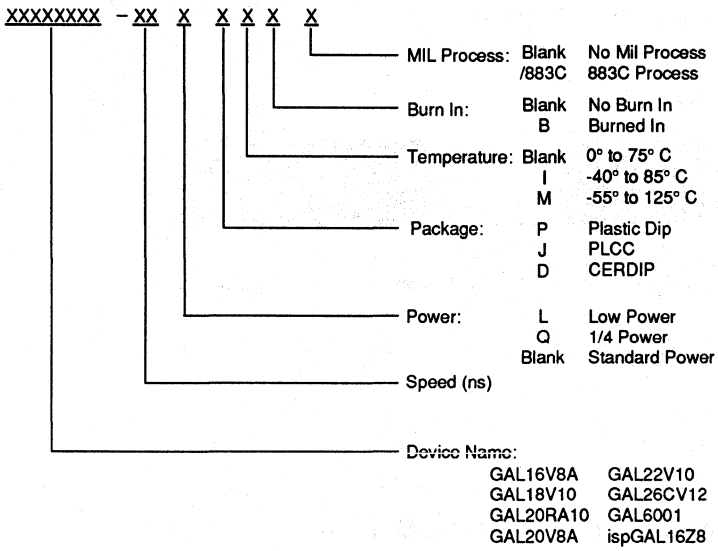
24-Pin (300 MIL) CERDIP

Dimensions in Inches MIN. / MAX.



ORDERING INFORMATION

PART NUMBER DESCRIPTION



Note 1: All fields are adjacent with no imbedded spaces. The Device Revision Level, Mil Process, Burn-In and Temperature fields are optional. All other fields must be indicated.
Note 2: When "883C" is indicated, "M" & "B" are implied and should not be listed.
Note 3: "B" refers to 160 hours of burn-in beyond the standard burn-in requirement for the commercial product reliability requirements currently in affect.

SPEED/GRADE SELECTOR GUIDE

	t_{PD} by GRADE		
	Commercial	**Industrial**	**Military**
GAL16V8A-xxL	10, 15, 25 ns	15, 20, 25 ns	15, 20 ns
GAL16V8A-xxQ	15, 25 ns	20 ns	20 ns
GAL18V10	15, 20 ns	15, 20 ns	15, 20 ns
GAL20RA10	15, 20 ns	20 ns	20 ns
GAL20V8A-xxL	10, 15, 25 ns	15, 20, 25 ns	15, 20 ns
GAL20V8A-xxQ	15, 25 ns	20 ns	20 ns
GAL22V10	15, 20, 25 ns	15, 20 ns	15, 20 ns
GAL26CV12	15, 20 ns	15, 20 ns	15, 20 ns
GAL6001	30, 35 ns	—	—
ispGAL16Z8	20, 25 ns	—	—
Vcc	5.00V ± 5%	5.00V ± 10%	5.00V ± 10%
Temperature	0->75°C	-40->85°C	-55->125°C
Packaging	Plastic DIP PLCC	Plastic DIP PLCC	CERDIP

Products listed in the adjacent table have complete datasheets in this data book and are recommended for new designs. Contact the factory for information on product and packaging options not listed in this table.

Complete guidelines for the ordering of Lattice products can be obtained from Customer Service.

GAL16V8A / 20V8A CROSS REFERENCE

The GAL16V8A and GAL20V8A devices are designed to be pin-for-pin, functional and JEDEC map compatible with standard PAL devices. The following table should be of assistance in determining which GAL16V8A or GAL20V8A device to use when replacing standard PAL devices.

SPEED	POWER	GAL DEVICE	BIPOLAR PAL DEVICE
10ns	115mA	A-10L	--
10ns	180mA	use A-10L	D or -10C
12ns	115mA	use A-10L	--
12ns	200mA	use A-10L	-12C
15ns	55mA	A-15Q	--
15ns	115mA	A-15L	--
15ns	180mA	use A-15L	B or -15C
15ns*	130mA	A-15LM	--
15ns*	220mA	use A-15LM	-15M
20ns	55mA	use -15Q	--
20ns	115mA	A-20L	--
20ns*	130mA	A-20LM	--
20ns*	210mA	use A-20LM	B MIL
25ns	55mA	-25Q	--
25ns	90mA	A-25L	B-2
25ns	180mA	use A-25L	A
30ns*	65mA	use -20QM	--
30ns*	125mA	use -20LM	--
35ns	45mA	use -25Q	B-4
35ns	90mA	use A-25L	A-2
35ns	180mA	use A-25L	STD

4/90

* Military Temperature Range

6

CUSTOM DEVICE PROGRAMMING

The additional service of having GAL devices custom programmed and permanently ink marked with customer specific identification codes is available from Lattice. Many of our distributors also offer programming and mark services.

Due to Lattice's stringent test philosophy and 100% AC/DC testing, the quality of pre-patterned GAL devices will be higher than pre-patterned devices from other technologies. In addition, a pattern change after initial programming can be accommodated as the GAL devices can be instantly reprogrammed to the revised pattern.

TAPE & REEL

Pre-programmed PLCC devices can be supplied in tape & reel for automated assembly environments. Special leadtime and order quantities apply. Contact your local sales representative or factory Customer Service for additional details.

ADDITIONAL BURN-IN

All GAL devices are extensively tested during the normal manufacturing flow, including a specific reliability bake step of every GAL device to assure their reliability. This extensive testing, which is not possible with other technologies, alleviates many of the traditional motivations for purchasing burned-in devices.

Our MIL-STD-883C and Standard Military Drawing devices meet all of the requirements of the military reliability testing and require no additional burn-in.

Customers desiring additional burn-in of commercial devices should contact the factory to review their specific requirements and specifications.

SCD'S, SPECIFICATIONS & AUDITS

Lattice encourages our customers to audit our processes, procedures, and specifications during factory visits. Our specification systems are compliant to the requirements of MIL-38510, where applicable. Specific details of our control procedures will be explained in detail during these audits.

Lattice has a sophisticated specification control system and QA audit procedure that assures compliance to the datasheet requirements. We also offer product manufactured in compliance to Standard Military Drawings. If a customer requirement is for non-standard product specifications or processes then customer Source Control Drawings or Specifications can be reviewed.

DIE SALES POLICY

Lattices recommends the purchase of factory assembled and tested devices wherever possible to assure the highest quality and reliability. Lattice is continually evaluating customer requirements for new and different packages.

Lattice is concerned with the ultimate reliability and quality of devices assembled and tested by our customers. We require a complete review of the systems, procedures and flows that our customers are utilizing for the assembly of GAL devices into packages or hybrids. Die sales must be approved by the Reliability and Quality departments as well as the President of Lattice *prior to* the beginning of the customer design cycle. Contact Customer Service for further details.

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3rd Floor
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Norcross, GAL 30071
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Burlington, MA 01803
(617) 229-5819

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Hillsboro, OR 97124
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(49) 89 329 09960

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Koto-ku, Tokyo
Japan 135
813-642-0621

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Scottsdale, AZ 85260
(602) 998-4850

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Fountain Valley, CA 92708
(714) 957-3367

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6312 Variel Ave.
Suite 204
Woodland Hills, CA 91367
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3350 Scott Blvd.
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(408) 988-6300

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7585 Ronson Rd.
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San Diego, CA 92111
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Waugaman Associates
4800 Van Gordon
Wheat Ridge, CO 80033
(303) 423-1020

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Yatesville, CT 06492
(203) 269-1145

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Deerfield Beach, FL 33442
(305) 426-4601

Sales Engineering Concepts
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Indianapolis, IN 46250
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ILLINOIS
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328 E. Main
Barrington, IL 60008
(708) 381-9087

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35 Corporate Woods
9101 W. 110th St. #222
Overland Park, KS 66210
(913) 345-1248

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Gaithersburg, MD 20882
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Grosse Pointe Park, MI 48230
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Eden Prairie, MN 55344
(612-944-3456

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West Caldwell, NJ 07006
(201) 226-3300

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7704 Ranchwood NW
Albuquerque, NM 87120
(505) 345-5003

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Suite B121
Phoenix, AZ 85044
(602) 496-0290

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(408) 745-6600

Arrow Electronics
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San Jose, CA 95131
(408) 452-3550

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500 Guiseppe Ct. #7
Roseville, CA 95678
(916) 969-3100

Bell Industries
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Sunnyvale, CA 94089
(408) 734-8570

Marshall Industries
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Milpitas, CA 95035
(408) 942-4600

Marshall Industries
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Suite 140
Rancho Cordova, CA 95670
(916) 635-9700

Merit Electronics
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San Jose, CA 95131
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Micro Genesis
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Santa Clara, CA 95054
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Arrow Electronics
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Arrow Electronics
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Tustin, CA 92680
(714) 838-5422

Arrow Electronics
9511 Ridgehaven Ct.
San Diego, CA 92123
(619) 565-4800

Bell Industries
30101 Agoura Ct.
Agoura Hills, CA 91301
(818) 706-2608

Bell Industries
11812 San Vicente
Los Angeles, CA 90049
(213) 826-6778

Bell Industries
11095 Knott Ave.
Suite E
Cypress, CA 90630
(714) 895-7801

Sterling Electronics
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San Diego, CA 92131
(619) 271-6555

Sterling Electronics
1342 Bell Ave.
Tustin, CA 92680
(714) 259-0900

Sterling Electronics
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Suite 103
Chatsworth, CA 91311
(818) 407-8850

Insight Electronics
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Aquora, CA 91301
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Insight Electronics
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San Diego, CA 92121
(619) 587-0471

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Suite 120
Irvine, CA 92718
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Chatsworth, CA 91311
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Marshall Industries
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El Monte, CA 91731
(818) 459-5500

Marshall Industries
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Irvine, CA 92718
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Marshall Industries
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San Diego, CA 92131
(619) 578-9606

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(203) 265-3822

Marshall Industries
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Deerfield Beach, FL 33441
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Suite 1024
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32701
(407) 767-8585

Marshall Industries
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33441
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Chicago, IL 60007
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3433 E. Washington
Fort Wayne, IN 46801
(219) 423-3422

Marshall Industries
6990 Corporate Dr.
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10413 W. 84th Terr.
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Interface Electronic Corp.
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Hauppauge, NY 11788
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1250 Scottsville Rd.
Rochester, NY 14624
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129 Brown St.
Johnson City, NY 13790
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(513) 435-8660

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