PowerPC 405EP

Embedded Processor

With speeds of up to 333MHz and two on-chip Ethernet interfaces, the PowerPC 405EP processor provides a flexible, low cost solution for developers of wireless LAN access points, edge routers, broadband modems and other wired and wireless networking devices. A rich feature set — including an on-chip SDRAM controller and PCI interface — and extremely low power consumption make this processor an ideal choice for high-density designs where connectivity is at a premium.

Benefits

- Delilvers 133 MHz to 333 MHz performance (CPU)
- Two on-chip 10/100 Ethernet MACs
- "Packet Reject" external interface and counters enhance network management
- On-chip SRAM for faster processing in data-intensive applications
- On-chip SDRAM controller supports up to 512 Mbytes of memory
- On-chip PCI bus interface
- Small package and extremely low power consumption for high-density applications

The PowerPC 405 Core

The PowerPC 405 core has been optimized for system on a chip designs requiring solid performance, low cost and low power consumption. Performance is enhanced through the use of separate instruction and data cache units. A 5-stage pipeline further boosts performance by offering single cycle execution of most instructions, including loads and stores.

Dual Bus Architecture

The PowerPC 405EP offers two on-chip buses: a processor local bus (PLB) and an on-chip peripheral bus (OPB). High-speed peripherals, like the PCI bus or memory controller connect directly to the core through the high-bandwidth, 64-bit PLB. Less demanding devices are served by the 32-bit OPB. An external bus controller supports ROM, EPROM, SRAM Flash and slave peripheral devices.

Memory Support

A 4-Kbyte on-chip SRAM stores critical code and data, and provides single-cycle access for faster processing in data-intensive router and switch applications. An on-chip SDRAM controller provides access to up to 512 Mbytes of external memory, and enhances performance with separate read and write buffers.

PCI Support

The PowerPC 405EP offers a 32-bit PCI interface that is PCI V2.2 compatible. An internal PCI arbiter supports three off-chip PCI masters as well as one internal master.

Ethernet Interface

Two 10/100 Ethernet MACs are supported on-chip, making this an ideal processor for 802.11 A/B wireless access points, broadband modems, or other applications requiring dual Ethernet connections. A "Packet Reject" external interface and five counters are also included to enhance network management.

Standard Peripherals

The PowerPC 405EP offers an array of on-chip standard peripherals. Two serial ports are provided as well as an IIC serial EEPROM controller. Up to 32 general-purpose I/Os further enhance functionality.

PowerPC Partners Ecosystem

AMCC's embedded PowerPC processors are supported by an extensive ecosystem of products and services from a wide range of leading suppliers. AMCC's PowerPC Partners program includes industry-standard providers of:

- Embedded operating systems
- Hardware and software development tools
- Embedded software products and services
- Board-level products
- System design services
- Technical training

For full details of the products and services available through the PowerPC Partners program, or to browse support available for a specific processor, visit:

http://www.amcc.com/Embedded/Partners

AMCC also provides an evaluation kit for this PowerPC processor, including an optimized evaluation board as well as sample applications and other software.

PowerPC 405EP

Features

- Speed (frequency): 133 MHz to 333 MHz
- Performance: 1.52 DMIPS/MHz (506 DMIPS @ 333 MHz peak)
- On-chip SDRAM Controller with separate 32-byte read and 128-byte write buffers
- Supports up to 512 Mbytes of memory
- External bus controller supporting ROM, EPROM, SRAM Flash, and slave peripheral I/O devices; 8- or 16-bit addressable bus width support with 16-bit interface
- DMA controller with four independent channels supports transfers between SDRAM, PCI, internal UARTs and devices on the external peripheral bus
- 32-bit PCI V2.2 compatible PCI interface with synchronous operation and internal PCI arbiter supporting three PCI off-chip masters and one internal master; supports external arbitration
- On-chip Ethernet support with two 10/100 MACs; includes dedicated memory access layer controller and "Packet Reject" external interface
- Five general-purpose timers in addition to the built-in 405 core timer facilities
- Two serial ports
- IIC serial EEPROM controller
- Up to 32 general-purpose I/Os
- Interrupt controller including up to 13 external interrupts
- JTAG support in processor core
- RoHS compliant versions available (lead-free)

For more information, please visit **http://www.amcc.com.**

Specifications

Technology

- 0.18 μm (0.13 pm L_{eff})

Performance (estimated)

- 202 Dhrystone 2.1 MIPS @ 133 MHz
- 304 Dhrystone 2.1 MIPS @ 200 MHz
- 404 Dhrystone 2.1 MIPS @ 266 MHz
- 506 Dhrystone 2.1 MIPS @ 333 MHz

Frequency

CPU/SDRAM/PCI/EBC

- 133/133/66/66 MHz
- 200/100/66/50 MHz
- 266/133/66/66 MHz
- 333/111/66/66 MHz
- 133/133/66/66 MHz
- 200/100/66/50 MHz

Typical Power Dissipation

- 0.72 W @ 266 MHz
- 0.76 W @ 333 MHz

Case Temperature Range

-

-40° C to +85° C

Power Supply

- 1.8 V (logic), 3.3 V (I /O), supports 5 V I/Os

Signal I/Os

- 248

Packaging

- 385-Ball, 31 mm x31 mm, E-PBGA
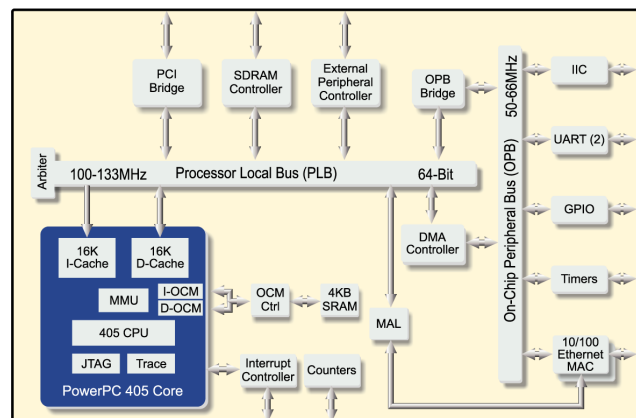
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