YAMAHA® LSI

YMF754 (DS-1E)

Hardware Specification

PCI Audio function only

YAMAHA Corporation
Semiconductor Division

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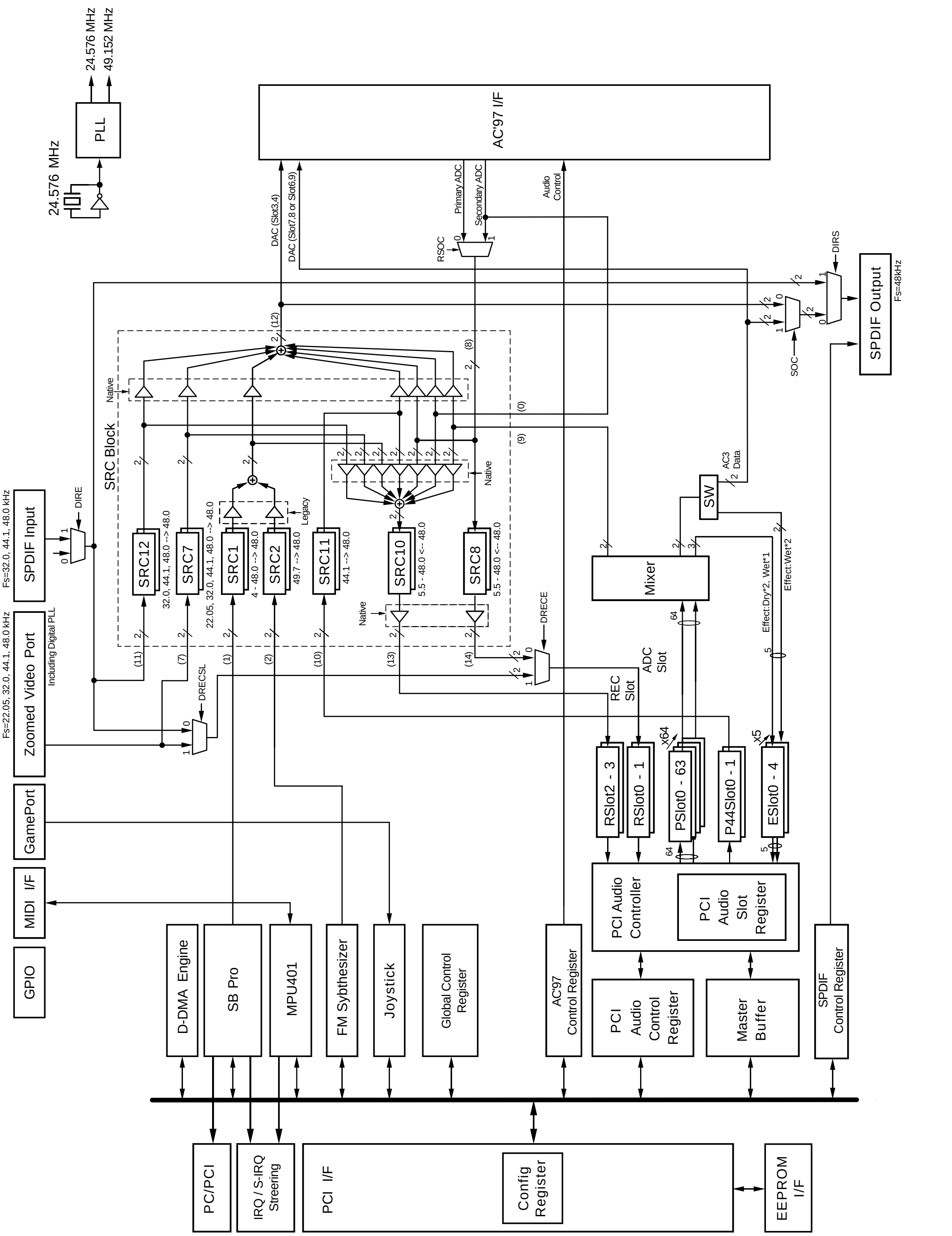
Index

Document Conventions

0Eh: Header Type	indicates the name of register. Two digit address means PCI Configuration register. Four digit address means PCI Audio register.
Latency Timer	indicates the name of bit in each register.
FRAME#	indicates the name of pin

1. Block


24.576 MHz
PLL
24.576 MHz
49.152 MHz
AC'97 I/F
DAC (Slot3,4)
DAC (Slot7,8 or Slot6,9)
Primary ADC
Secondary ADC
Audio Control
RSOC
SRC Block
Native
Legacy
SRC12
SRC7
SRC1
SRC2
SRC11
SRC10
SRC8
32.0, 44.1, 48.0 --> 48.0
22.05, 32.0, 44.1, 48.0 --> 48.0
4 - 48.0 --> 48.0
49.7 --> 48.0
44.1 --> 48.0
5.5 - 48.0 <-- 48.0
DRECE
DRECSL
DIRE
DIRS
SOC
SPDIF Output
Fs=48kHz
AC3 Data
SW
Mixer
Effect:Dry*2, Wet*1
Effect:Wet*2
ADC Slot
REC Slot
RSlot2 - 3
RSlot0 - 1
PSlot0 - 63
P44Slot0 - 1
ESlot0 - 4
PCI Audio Controller
PCI Audio Slot Register
SPDIF Input
Fs=32.0, 44.1, 48.0 kHz
Zoomed Video Port
Including Digital PLL
Fs=22.05, 32.0, 44.1, 48.0 kHz
GamePort
MIDI I/F
GPIO
D-DMA Engine
SB Pro
MPU401
FM Sybthesizer
Joystick
Global Control Register
AC'97 Control Register
PCI Audio Control Register
Master Buffer
SPDIF Control Register
PC/PCI
IRQ / S-IRQ Streering
PCI I/F
Config Register
EEPROM I/F

2. PCI Audio Registers

This chapter explains the capability of control registers of DS-1E PCI Audio and their register mapping. The control registers of DS-1E PCI Audio consists of two groups: One group includes built-in registers of DS-1E and the other group includes register to be mapped in the host memory. The Built-in registers of DS-1E are as follows.

- Timer Control
- SPDIF Input/Output Control
- General Purpose I/O Control
- EEPROM Control
- Zoomed Video Port Control
- Volume Control
- AC'97 Control
- PCI Audio Control

The following sections describe the built-in registers of DS-1E. Please refer to **4. DSP Control Data** of this document for the registers that are memory mapped in the host memory.

To access the built-in registers of DS-1E PCI Audio, PCI memory transfer operation should be used. Burst access is available for any register access.

Address	b[31:24]	b[23:16]	b[15:8]	b[7:0]	Remark
0000h	Reserved		YAMAHA Audio Revision ID		Global Register
0004h	Activity		Interrupt Flag		
0008h	ZV Control		Global Control		
000Ch	Reserved				
0010h	Timer Count		Reserved	Timer CTRL	
0014h	Reserved				
0018h	Reserved			SPDIF Output Control	
001Ch	Reserved		SPDIF Channel Status Control		
0020h - 0028h	Reserved				
002Ch	EEPROM Control				
0030h	Reserved				
0034h	Reserved		SPDIF Input Control		
0038h	SPDIF Input Channel Status				
003Ch – 004Ch	Reserved				Reserved
0050h	GPIO Input Interrupt Enable		GPIO Input Interrupt Flag		GPIO Register
0054h	GPIO Output Control		GPIO Input Status		
0058h	GPIO Input Type Configuration		GPIO Function Enable		
005Ch	Reserved				
0060h	AC'97 Command Address		AC'97 Command Data		AC'97 Interface
0064h	Primary AC'97 Status Address		Primary AC'97 Status Data		
0068h	Secondary AC'97 Status Address		Secondary AC'97 Status Data		
006Ch	Reserved				
0070h	Reserved		Secondary AC'97 Configuration		
0064h - 007Ch	Reserved				
0080h	Legacy Audio Output Volume Rch		Legacy Audio Output Volume Lch		Volume Register
0084h	PCI Audio DAC Output Volume Rch		PCI Audio DAC Output Volume Lch		
0088h	ZV Output Volume Rch		ZV Output Volume Lch		
008Ch	Secondary AC'97 Volume Rch		Secondary AC'97 Volume Lch		
0090h	Primary ADC Output Volume Rch		Primary ADC Output Volume Lch		
0094h	Legacy Audio Loopback Volume Rch		Legacy Audio Loopback Volume Lch		
0098h	PCI Audio DAC Loopback Volume Rch		PCI Audio DAC Loopback Volume Lch		
009Ch	ZV Loopback Volume Rch		ZV Loopback Volume Lch		
00A0h	Secondary ADC Loopback Rch		Secondary ADC Loopback Lch		
00A4h	Primary ADC Loopback Volume Rch		Primary ADC Loopback Volume Lch		
00A8h	PCI Audio ADC Input Volume Rch		PCI Audio ADC Input Volume Lch		
00ACh	PCI Audio REC Input Volume Rch		PCI Audio REC Input Volume Lch		
00B0h	P44Slot Output Volume Rch		P44Slot Output Volume Lch		
P44Slot	P44Slot Loopback Volume Rch		P44Slot Loopback Volume Lch		
00B8h	SPDIF In Output Volume Rch		SPDIF In Output Volume Lch		
00BCh	SPDIF In Loopback Volume Rch		SPDIF In Loopback Volume Lch		
00B0h - 00BCh	Reserved				Reserved
00C0h	Reserved		ADC Slot Sampling Rate		Sampling Rate Register
00C4h	Reserved		REC Slot Sampling Rate		
00C8h	Reserved			ADC Format	
00CCh	Reserved			REC Format	
00D0h - 00FCh	Reserved				
0100h	Status				PCI Audio Register
0104h	ControlSelect				
0108h	Mode				
010Ch	SampleCount				
0110h	NumOfSample				
0114h	Config				
0118h - 0138h	Reserved				
013Ch	TestRegister				
0140h	PlayControlSize				
0144h	RecControlSize				
0148h	EffControlSize				
014Ch	WorkSize				
0150h	MapOfRec				
0154h	MapOfEffects				
0158h	PlayControlBase				
015Ch	RecControlBase				
0160h	EffControlBase				
0164h	WorkBase				
0168h – 3FFCh	Reserved				Reserved
4000h – 6FFCh	Controller Instruction RAM				Controller Instruction
7000h – 7FFCh	Reserved				

2.1. Description of Global Register

These registers indicate the Interrupt flag Control, Zoomed Video Port Control, Hardware Volume Control, the Timer Control and SPDIF Input / Output Control register. The structure of the registers is shown below:

Address	b[31:24]	b[23:16]	b[15:8]	b[7:0]	Remark
0000h	Reserved		YAMAHA Audio Revision ID		
0004h	Activity		Interrupt Flag		
0008h	ZV Control		Global Control		
000Ch	Reserved				
0010h	Timer Count		Reserved	Timer CTRL	
0014h	Reserved				
0018h	Reserved			SPDIF Output Control	
001Ch	Reserved		SPDIF Output Channel Status Control		
0020h	Reserved				
0024h	Reserved				
0028h	Reserved				
002Ch	EEPROM Control				
0030h	Reserved				
0034h	Reserved		SPDIF Input Control		
0038h	SPDIF Input Channel Status				
003Ch	Reserved				

Reserved area is writable but transferred data will be ignored. If you try to read Reserved register, the value is read as "0". The Address is offset from 10 - 13h: DS-1E Audio function Memory Base Address.

0000h: YAMAHA Audio Revision ID

Read Only
Default: 0x0002h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	B7	b6	b5	b4	b3	b2	b1	b0
YAMAHA Audio Revision ID															

b[15:0] .... YAMAHA Audio Revision ID

This register indicates the YAMAHA Audio Revision ID of DS-1E. This is hardwired to "0x0002"

0004h: Interrupt Flag

Read / Write Clear
Default: 0000h or 0100h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	B7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	DOCK	PSCI	OVF3	OVF2	OVF1	OVF0	ZVI	HVI	TI

b0 .... TI: Timer Interrupt Flag

This bit indicates that the internal counter of the DS-1E has reached to"0".
When TEN bit of 0010h: Timer Control is set to "1", the timer starts to downcount operation after the value of the 0012h: Timer Count is loaded to the internal counter. When the internal counter reaches to "0", TI is set to "1". Afterwards, the timer reloads the 0012h: Timer Count value to continue downcount operation.

b1 .... HVI: Hardware Volume Change Interrupt Flag

This bit indicates the master volume of AC'97 has been changed by the Hardware Volume pin: *VOLUP#* and *VOLDW#.*

When AC97 is not connected to DS-1E or AC'97 is in Power Down state, HVI is not set to "1" since the AC'97 Master Volume is never changed.

b2 .... ZVI: Zoomed Video port Hot Insertion / Remove Interrupt Flag

When both valid BIT Clock and valid L/R Clock start to be supplied to the Zoomed Video Port, this bit is set to "1". ZVI is set to "1", when the ZVA flag in 0006h: Activity changes its level from "0" to "1" or "1" to "0".

b3 .... OVF0: Overflow Flag for SRC output mixer Lch

This bit indicates an overflow has occurred at the SRC output mixer for L channel.
In the event of an overflow, the value is rounded in 16-bit form.

b4 .... OVF1: Overflow Flag for SRC output mixer Rch

This bit indicates an overflow has occurred at the SRC output mixer for R channel.

b5 .... OVF2: Overflow Flag for SRC input mixer Lch

This bit indicates an overflow has occurred at the SRC input mixer for L channel.

b6 .... OVF3: Overflow Flag for SRC input mixer Rch

This bit indicates an overflow has occurred at the SRC input mixer for R channel.

b7 .... PSCI: Power State Change Interrupt Flag

This bit indicates PS of 54-55h: Power Management Control / Status is changed to different value. Once this flag is set to "1", the PSCI bit is never changed regardless of the state of the PS bit. This bit is independent of any setting on the ACPI bit of 58-59h: ACPI mode.

b8 .... DOCK:

This bit indicates the state of *DOCKEN#* is changed from "0" to "1", or "1" to"0".

Once each interrupt flag is set to "1", it is held "1" until cleared by writing "1" to the corresponding bit.

0006h: Activity

Read Only
Default: 0000h or 0010h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	DOCKA	MUTE	HWUP	HWDW	ZVA

b0 .... ZVA: Zoomed Video Port Activity

This bit indicates that the valid Bit Clock and L/R Clock are supplied to the Zoome Video Port of DS-1E. For L/R Clock, valid clock means that a frequency is either one of 22.09kHz,32.0kHz,44.1kHz or 48.0kHz. For Bit Clock, valid clock means that logic level transtion take place several times during 1Fs.

"0": No valid BIT and L/R Clock to the ZV port.
"1": Valid BIT and L/R Clock to the ZV port.

b1 .... HWDW: Hardware Volume Down pin status

This bit indicates the state of *VOLDW#*. When the VOLDW# pin is open or high, the HWDW is set to "0". When the VOLDW# pin is low continously more than 4Fs, the HWDW is set to “1”. Once HWDW is set to “1”, it's held "1" until the *VOLDW#* pin becomes open or goes high. This bit will be valid regardless of the state of the HVE in the 0008h: Global Control and the state of the PSACL in the 4E-4Fh: DS-1E Power Control 2.

b2 .... HWUP: Hardware Volume Up pin status

This bit indicates the state of *VOLUP#*. When the VOLUP# pin is open or high, the HWUP is set to "0". When the VOLUP# pin is low continously more than 4Fs, the HWUP is set to “1”. Once HWUP is set to “1”, it's held "1" until the *VOLUP#* pin becomes open or goes high. This bit will be valid regardless of the state of the HVE in the 0008h: Global Control and the state of the PSACL in the 4E-4Fh: DS-1E Power Control 2.

b3 .... MUTE: Hardware Volume Mute

This bit indicates the MUTE state of the Hardware Volume. When the *VOLDW#* and *VOLUP#* pin are low continuously more than 4Fs, the Mute is set to “1”. Once the MUTE is set to “1” it’s held “1” until either one of the VOLDW# or VOLUP# pins becomes open or goes high. With the MUTE set to “1”, the HWUP and HWDW bits are both set to “1”. This bit will be valid regardless of the state of the HVE in the 0008h: Global Control and the state of the PSACL in the 4E-4Fh: DS-1E Power Control 2.

b4 .... DOCKA: Docking Activity

This bit indicates the state of *DOCKEN#* pin. When the *DOCKEN#* is held low level, the DOCKA is set to "0". When *DOCKEN#* is open or set to “1”, DOCKA is set to "1".

0008h: Global Control

Read / Write
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	B10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	DRECSL	DRECE	DOCKIE	MVCD	PSCIE	OVFIE	ZVIE	-	HVIE	HVE

b0 .... HVE: Hardware Volume Control Enable

This bit enables the Hardware Volume Control function.

"0": Disables the Hardware Volume (default)
"1": Enables the Hardware Volume

b1 .... HVIE: Hardware Volume Control Interrupt Enable

This bit enables to assert *INTA#* when the HVI of 0004h: Interrupt Flag is set to "1".

"0": Does not assert the *INTA#* (default)
"1": Asserts the *INTA#*

b3 .... ZVIE: Zoomed Video port Interrupt Enable

This bit enables to assert *INTA#* when the ZVI of 0004h: Interrupt Flag is set to "1".

"0": Does not assert the *INTA#* (default)
"1": Asserts the *INTA#*

b4 .... OVFIE: Overflow Flag Interrupt Enable

This bit enables to assert *INTA#* when one of the OVF[3:0] of 0004h: Interrupt Flag is set to "1".

"0": Does not assert the *INTA#* (default)
"1": Asserts the *INTA#*

b5 .... PSCIE: Power State Change Interrupt Enable

This bit enables to assert *INTA#* when the PSCI of 0004h: Interrupt Flag is set to "1".

"0": Does not assert the *INTA#* (default)
"1": Asserts the *INTA#*

b6 .... MVCD: Master Volume Change Disable

This bit disables to increment (or decrement) the AC'97 Master Volume automatically when *VOLHW#* (or *VOLDW#*) is held low level.

"0": AC'97 Master Volume is incremented (or decremented) automatically. (default)
"1": AC'97 Master Volume is not incremented (or decremented) automatically, setting only HVI of 0004h: Interrupt Flag to "1". The control of AC'97 Master Volume is done by writing AC'97 control register.

b7 .... DOCKIE: Docking Interrrupt Enable

This bit enables to assert *INTA#* when DOCK of 0004h: Interrupt Flag is set to "1".

"0": Does not assert the *INTA#* (default)

"1": Assert the *INTA#*

b8 .... DRECE: Direct Recording Enable

This bit selects the input source at ADC Slot.

"0": selects the output of SRC#8 (default)

"1": selects the input of SPDIF Input / ZV Port, allowing direct recording. The DRECSL selects either one of the inputs.

b8 .... DRECSL: Direct Recording Source Select

This bit select the source of direct recording, when DRECE is set to "1".

"0": SPDIF Input (default)

"1": ZV Port

When either of b7, b5, b4, b3 or b1 is set to "1", the interrupt remain asserted until the corresponding flag of 0004h: Interrupt Flag is cleared.

000Ah: ZV Control

Read Only
Default: 0000h
Access Bus Width: 8-bit, 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	FS			

b0 .... FS: FS Status

These bits indicate the sampling rate of input data supplied to the ZV port.

"0": No valid data (default)

"1": 22.05kHz

"2": 32.0kHz

"4": 44.1kHz

"8": 48.0kHz

0010h: Timer Control

Read / Write
Default: 00h
Access Bus Width: 8-bit, 16-bit, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	TIEN	TEN

b0 .... TEN: Timer Enable

This bit controls start and stop operation of the timer. When TEN is set to "1", the timer starts downcount operation after the value of the 0012h: Timer Count is loaded to the internal counter. When the internal counter comes to "0", TI of the 0004h: Interrupt Flag is set to "1". Then, the counter reloads the value from the 0012h: Timer Count to continue a count down operation. With the TEN bit set to "0", the timer stops its count operation.

"0": Stops Timer counting (default)
"1": Stars Timer counting

b1 .... TIEN: Timer Interrupt Enable

This bit enables to assert *INTA#* when TI of 0004h: Interrupt Flag is set to "1". When TI is cleared, INTA# is deasserted.

"0": Does not assert the *INTA#* (default)
"1": Asserts the *INTA#*

0012h: Timer Count

Read / Write
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Timer Count															

b[15:0] .... Timer Count

This register specifies an interrupt interval of the general purpose of timerl. The resolution is 10.4 µs (1/2Fs @ Fs=48kHz). The interval time is calculated by the following equation. However,"Timer Count" cannot be set to "0000h". Allowable minimum time is 20.8us.

T = [Timer Count + 1] * 10.4 [µs]

0018h: SPDIF Output Control

Read / Write
Default: 00h
Access Bus Width: 8-bit, 16-bit, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	SOC	DITE

b0 .... DITE: Digital interface Transmitter Enable

This bit enables to output digital audio stream (PCM and AC-3 bit stream) from *SPDIFOUT*.

"0": No digital audio data (default)
"1": Output the digital audio stream

With the DITE set to "0", the SPDIFOUT pin is placed in a logic low level.

b1 .... SOC: Source Select

This bit selects the digital audio source to be transmitted from *SPDIFOUT*. In both case, Fs is fixed to 48kHz.

"0": PCM data (default)

The PCM data (same data supplied to te Slot3 and Slot4 on the AC-Link) is transmitted from *SPDIFOUT* .

"1": AC-3 bit stream

The data for EffectSlot-2 and EffectSlot-3 are transmitted from *SPDIFOUT*. When SOC="1", set AC3 0108h: Mode of to "1" as well.

001Ch: SPDIF Output Channel Status Control

Read / Write

Default: 0000h

Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Category Code								-	-	Control					-

bit[5:1].......... Control

These bits specify "Control code" in channel status of SPDIF output.

	PCM data	Dolby Digital
Copyright Protection	00000b	00001b
No Copyright Protection	00010b	00011b

Use Copyright Protection mode for DS-1E.

bit[15:8]........ Category Code

These bits specify "Category code" in channel status of SPDIF output.

Normally set "10011010b" (meaning sampling-rate-converted, pre-recorded software commercially available (the first generation),original) to these bits.

Serial copy management system(SCMS) defines that a single digital copy operation is possible by specifying Copyright Protection mode and pre-recorded software commercially available(the first generation,original).

Channel status other than Control and Category is fixed by the hardware as show below.

Bit	Value	Comment
Bit[0]	0b	for Consumer
Bit[7:6]	00b	mode 2
Bit[19:16]	0000b	Source Number (not specified)
Bit[23:20]	0000b	Channel Number (not specified)
Bit[27:24]	0010b	Sampling Rate (48.0 kHz)
Bit[29:28]	00b	Clock Accuracy (Level-II)
Bit[191:30]		"0"

002Ch: EEPROM Control

Read / Write
Default: 00000000h
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ROM DATA															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
BUSY	-	-	-	-	-	-	-	OP Code		ROM ADDR					

bit[15:0]........ ROM DATA

In case of write access to EEPROM, set data needs to be written into EEPROM. In case of read access, data in EEPROM is read from this register.

bit[21:16]...... ROM ADDR (Write Only)

These bits specify the address to access for write and read operation.

bit[23:22]...... OP Code (Write Only)

These bits specify the access mode for EEPROM

bit31............. BUSY (Read Only)

This bit indicates the access for EEPROM is busy.
In case of writing the data, this bit is set to "1" until transferring data to EEPROM is completed. In case of reading the data, this bit is set to "1" until the data from EEPROM is set to ROM_DATA register.

Before access to EEPROM, set HVE of 0008h: Global Control to "0" and set PSIO of 4E-4Fh: DS-1E Power Control 2 to "0".

For detailed information for EEPROM write operation, refer to the Section 16. EEPROM Interface.

0034h: SPDIF Input Control

Read / Write
Default: 0004h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	B4	B3	b2	b1	b0
-	-	-	-	-	-	-	-	-	U/LIE	U/L	DIRS	-	FS		DIRE

b0 .... DIRE: DIR Enable

This bit enables the digital data received on SPDIFIN pin to be supplied to SRC#12.

"0": The data from *SPDIFIN* is supplied to SRC#12. (default)
"1": The data from *SPDIFIN* is supplied to SRC#12.

b[2:1] .... FS: FS Status (Read Only)

These bits indicate the sampling rate of digital data at SPDIF input.

"0": 44.1kHz
"1": 48kHz
"2": Reserved (Unlock state) (default)
"3": 32kHz

b4 .... DIRS: DIR Input Select

This bit selects which data is supplied to SPDIFOUT pin.

"0": PCM data (default)
"1": Digital data received at SPDIFIN pin directly to SPDIFOUT pin

b5 .... U/L: Unlock / Lock Flag

This bit indicates the state of SPDIF input is changed from the Unlock state to the Lock state, or from the Lock state to the Unlock state. This bit is held "1" until writing "1" to this bit. While U/L is set to "1", DS-1E can not detect the change of any new lock state. While locked, 0038h: SPDIF Input Channel Status does not change.

"0": No change is detected (default)
"1": The change from Unlock to Lock (or from Lock to Unlock) is detected.

b6 .... U/LIE: Unlcok / Lock Interrupt Enable

This bit enables to assert the *INTA#* when U/L is set to "1".

"0": Doed not assert the *INTA#* (default)
"1": Asserts the *INTA#*

0038h: SPDIF Input Channel Status

Read Only
Default: 0000h
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Category Code								Mode		Control					
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	Clock Accuracy		Sampling Rate				Channel Number				Source Number			

The channel status will not be available until at least 192-sample is supplied to afer FS has been locked. Please refer to IEC958: Digital Audio Interface, Part 3: Consumer Applications for more information of Channel status.

b[5:0] .... Control

These bits indicate "Control" in channel status of SPDIF input.

b[7:6] .... Mode

These bits indicate "Mode" in channel status of SPDIF input.

b[15:8] .... Category Code

These bits indicate "Category Code" in channel status of SPDIF input.

b[19:16] .... Source Number

These bits indicate "Source Number" in channel status of SPDIF input.

b[23:20] .... Channel Number

These bits indicate "Channel Number" in channel status of SPDIF input.

b[27:24] .... Sampling Rate

These bits indicate "Sampling Rate" in channel status of SPDIF input.

b[29:28] .... Clock Accuracy

These bits indicate "Clock Accuracy" in channel status of SPDIF input.

2.2. Description of General Purpose I/O Control Register

Address	b[31:24]	b[23:16]	b[15:8]	b[7:0]	Remark
0050h	GPIO Input Interrupt Enable		GPIO Input Interrupt Flag		
0054h	GPIO Output Control		GPIO Input Status		
0058h	GPIO Input Type Configuration		GPIO Function Enable		
005Ch	Reserved				

Reserved area is writable but all the data will be ignored. If you try to read Reserved register, the value is read as "0". The Address is offset from 10 - 13h: DS-1E Audio function Memory Base Address.

0050h: GPIO Input Interrupt Flag

Read / Write Clear
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	GI2	GI1	GI0

b[2:0] .... GI[2:0]: GPIO Input Interrupt flag

When the GPIO is configured as an input pin by the 0058h: GPIO Input/Output Configuration and the edge detection mode is set by 005Ah: GPIO Input Type Configuration, corresponding bit is set to “1” if the edge is detected on respetive GPIO pin.

"0": No edge is detected (default)
"1": Edge is detected

Once these bits are set to "1", they are held "1" until cleared by writing "1" to corresponding bit. With those bits set to “1”, the edge is not detected.

0052h: GPIO Input Interrupt Enable

Read / Write
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	GIE2	GIE1	GIE0

b[2:0] .... GIE[2:0]: GPIO Interrupt Enable

These bits enable to assert *INTA#* when 0050h: GPIO Input Interrupt Flag is set to "1".

"0": Does not assert the *INTA#* (default)
"1": Asserts the *INTA#*

0054h: GPIO Input Status

Read only
Default: 000xh (It depends on the configuration of GPIO pin)
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	GPI2	GPI1	GPI0

b[2:0] .... GPI[2:0]: GPIO Input State

These bits indicate a logic level of GPIO input when GPIO is configured as an input pin. When GPIO is configured as an output pin, the bit shows the output level. Even if the GPE of 0058h: GPIO Function Enable is set to “0”, this bit reflects the logic level of GPIO.

"0": Low level is input
"1": High level is input

0056h: GPIO Output Control

Read / Write
Default: 00FFh
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	GPO2	GPO1	GPO0

b[2:0] .... GPO[2:0]: GPIO Output Control

These bits control the output level of GPIO when GPIO is configured as an output pin.

"0": low-level output
"1": high level output (default)

Though these bits are written when GPIO is configured as an input, the logic level of GPIO does not change.

0058h: GPIO Function Enable

Read / Write
Default: 00FFh
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	GPE2	GPE1	GPE0	-	-	-	-	-	GPC2	GPC1	GPC0

b[2:0] .... GPC[2:0]: GPIO Input/Output Configuration

These bits specify the direction (Input / Output) of GPIO.

"0": Output
"1": Input (default)

b[10:8] ...... GPE[2:0]: GPIO Function Enable

These bits enable the GPIO function.

"0": Disable (default)
"1": Enable

005Ah: GPIO Input Type Configuration

Read / Write
Default: 5555h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	GPT2		GPT1		GPT0	

b[1:0] .... GPT0: GPIO Input Type Confiugration
b[3:2] .... GPT1: GPIO Input Type Confiugration
b[5:4] .... GPT2: GPIO Input Type Confiugration

These bits specify the detection method of level change at input pin when GPIO is configured as input pin.

"0": No detection mode (level only)
"1": Detects rising edge (the change from low to high) (default)
"2": Detects falling edge (the change from high to low)
"3": Detects both edge (the change from low to high , or the change from high to low)

2.3. Description of AC'97 Control Register

The listed below is the register map to write to AC’97 register and to read from AC’97 register via AC-link. The address and data of AC’97 register are transferred to AC’97 at each sample frame (about 20µs). Therefore software needs to wait for the successive read and wrirte access until the previous one is completed.

Offset	b[31..24]	b[23..16]	b[15..8]	b[7..0]	Remark
0060h	AC'97 Command Address		AC'97 Command Data		
0064h	Primary AC'97 Status Address		Primary AC'97 Status Data		
0068h	Secondary AC'97 Status Address		Secondary AC'97 Status Data		
006Ch	Reserved				
0070h	Reserved		Secondary AC'97 Configuration		
0074h : 007Ch	Reserved				

Reserved area is writable but all the data will be ignored. If you try to read Reserved register, the value is read as "0". The Address is offset from 10 - 13h: DS-1E Audio function Memory Base Address.

0060h: AC'97 Command Data

Read / Write
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CMD_DATA															

b[15:0] .... CMD_DATA: Command Data

This register specifies the data to be written to AC’97 registers. When data is written to the COM_DATA, CMD_DATA and CMD_ADRS of 0062h: AC’97 Command Address are transferred to the AC’97 on the next frame. The Tag of Slot1 and Slot2 on the CSD0 pin will become valid on the next frame where data is written to to the CMD_DATA.

0062h: AC'97 Command Address

Read / Write
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
R/W	-	-	-	-	-	ID1	ID0	-	CMD_ADDR						

b[6:0] .... CMD_ADDR: Command Address

This register specifies the address of AC97 to be accessed. Since AC’97 is addressed in 2-byte, b0 must be set to “0”.

b[9:8] .... ID[1:0]: Codec ID

This register specifies the Codec ID of AC’97 to be access. In case of access to the Primary AC’97, "00b" should be set. In case of access to the Secondary AC’97, the value determined by the ID definition pins of AC’97 should be set. When CodecID is not correct, access to the AC’97 register is not possible. CodecID of the Secondary AC’97 may be different depending on the system to be used.

b15 .... R/W: Read/Write

This bit controls read or write operation to AC’97 register.

"0": Writes the data to AC97 register (default)

"1": Reads the data from AC97 register

0064h: Primary AC'97 Status Data

Read Only
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PRI_STAT_DATA															

b[15:0] .... PRI_STAT_DATA: Primary Status Data

This register stores the Primay AC’97 register data.

When R/W is set to "1" in 0062h: AC'97 Command Address, the data read from Primary AC97 will be set on this register. After CMD_ADDR of 0062h: AC'97 Command Address is set, this register is updated in approximately 1-sample time period.

0066h: Primary AC'97 Status Address

Read Only
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PBUSY	-	-	-	-	-	-	-	-	PRI_STAT_ADDR						

b[6:0] .... PRI_STAT_ADDR: Primary Status Address

These bits indicate that the PRI_STAT_DATA of 0064h: Primary AC'97 Status Data belongs to which Primay AC’97 register.

b15 .... PBUSY: Primary AC'97 Busy

This bit indicates whether or not the access to the Primary AC’97 register is possible.

"0": Access to the Primary AC’97 register is possible (default)

"1": Access to the Primay AC’97 register is not possible.

When CRST of 48-49h: DS-1E Control is set to "1", PBUSY is held "0".

0068h: Secondary AC'97 Status Data

Read Only
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	B9	b8	b7	b6	b5	b4	b3	b2	b1	b0
SEC_STAT_DATA															

b[15:0] .... SEC_STAT_DATA: Status Data

This register stores the Secondary AC'97 register data.
When R/W is set to "1" in 0062h: AC'97 Command Address, the data read from Secondary AC97 will be set on this register. After CMD_ADDR of 0062h: AC'97 Command Address is set, this register is updated in approximately 1-sample time period.

006Ah: Secondary AC'97 Status Address

Read Only
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	B9	b8	b7	b6	b5	b4	b3	b2	b1	b0
SBUSY	-	-	-	-	-	-	-	-	SEC_STAT_ADDR						

b[6:0] .... SEC_STAT_ADDR: Status Address

These bits indicate where the SEC_STAT_DATA of 0068h: Secondary AC'97 Status Data belongs to which Secondary AC'97 register.

b15 .... SBUSY

This bit indicates whether or not the access to the Secondary AC'97 register is possible.

"0": Access to the Secondary AC'97 register is possible (default)
"1": Access to the Secondary AC'97 register is not possible.

When CRST of 48-49h: DS-1E Control is set to "1", PBUSY is held "0".

0070h: Secondary AC'97 Configuration

Read / Write
Default: 0002h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	B9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	ID1	ID0	-	-	4CHSL	4CHEN	-	SHWV	PHWV	RSOC

b0 .... RSOC: Recording Source Select

This bit selects the recording source at ADC Slot.

"0": ADC data from Primary AC'97 is supplied to the ADC slot. (default)
"1": ADC data from Secondary AC'97 is supplied to the ADC slot.

b1 .... PHWV: Primary Hardware Volume Control Enable

This bit enables to control the Master Volume of Primary AC'97 by using *VOLDW#* and *VOLUP#*.

"0": Disables to control Master Volume of Primary AC'97 by Hardware Volume control.
"1": Enables to control Master Volume of Primary AC'97 by Hardware Volume control. (default)

b2 ....SHWV: Secondary Hardware Volume Control Enable

This bit enables to control Master Volume of Secondary AC'97 by using *VOLDW#* and *VOLUP#*.

"0": Disables to control Master Volume of Secondary AC'97 by Hardware Volume control.

"1": Enables to control Master Volume of Secondary AC'97 by Hardware Volume control.(default)

b4 ....4CHEN: 4channel output enable

This bit determines whether Effect Slot2/3 data is processe as effect data or it is supplied to the Secondary AC'97 DAC.

"0": Effect Slot2 and Effect Slot3 is processed as an effect data. (default)

"1": Effect Slot2 and Effect Slot3 is used for the Secondary AC'97 DAC.

Effect Slot2 corresponds to L-Channel of the Secondary AC'97 DAC. Effect Slot3 corresponds to R-Channel of the Secondary AC'97 DAC. AC3 of 0108h: Mode is set to "1" as well when 4CHEN is set to "1".

b5 ....4CHSL: 4channel Slot select

This bit selects which slot of AC-link the data of Effect Slot2 and Effect Slot3 is transferred on. This bit is effective only when 4CHEN is set to "1".

"0": The data of Effect Slot2 is transferred on Slot7 of AC-link. The data of Effect Slot3 is transferred on Slot8 of AC-link. (default)

"1": The data of Effect Slot2 is transferred on Slot6 of AC-link. The data of Effect Slot3 is transferred on Slot9 of AC-link.

b[9:8] ....ID[1:0]: Secondary Codec ID

These bits specify the Codec ID of Secondary AC'97.

The b[9:8] and b[5:0] is reset to the initial value when the CRST of is set to "1", and the data cannot be set while the CRST is set "1". After the CRST is changed from "0" to "1", the data to be used must be always set again.

An example of how to access the AC’97 registers is shown below.

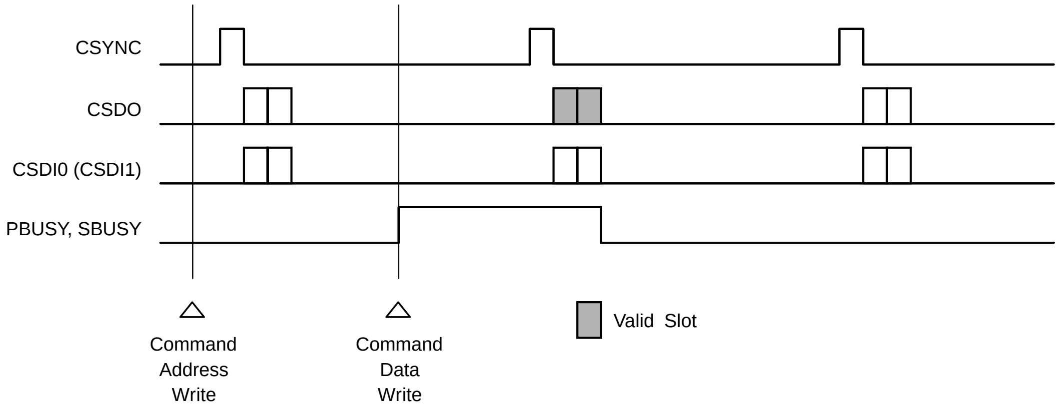
Writing data to AC97

(1) With the R/W of 0062h: AC’97 Command Address set to “1”, set Codec ID of the AC’97 to ID[1:0], and set the address to CMD_ADDR.

(2) Set the data to CMD_DATA register of 0060h: AC’97 Command Data.

(3) To write to the Primay AC’97, poll the PBUSY of 0066h: Primay AC’97 Status Address until the bit becomes "0". To write to the Secondary AC’97, poll the SBUSY of 006Ah: Secondary AC’97 Status Address until the bit becomes "0".

In case of DWORD access, (1) and (2) can be operated simultaneously. To verify the written data, use the sequence of Reading data from AC’97 Described below.

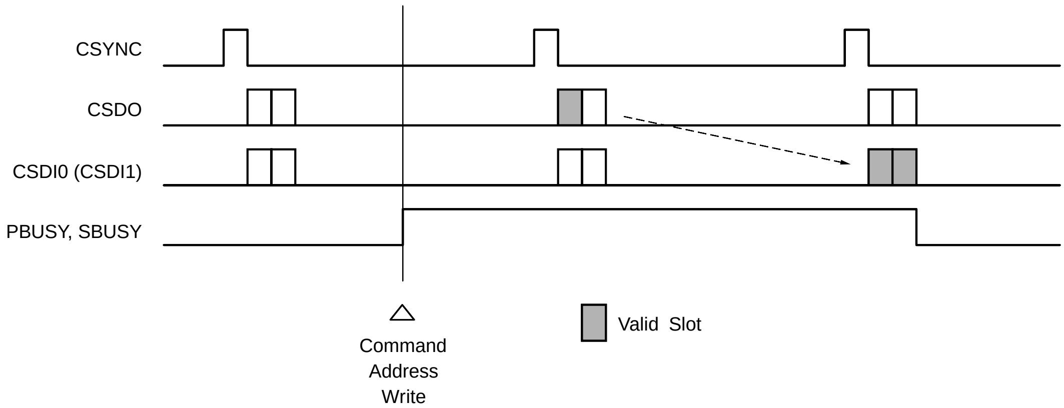


Read the data from AC97

(1) With the R/W of 0062h: AC’97 Command Address set to “1”, set the Codec ID of the AC’97 to ID[1:0], and set the address to CMD_ADDR.
In case of DWORD(32-bit) access, any data set to CMD_DATA is ignored.

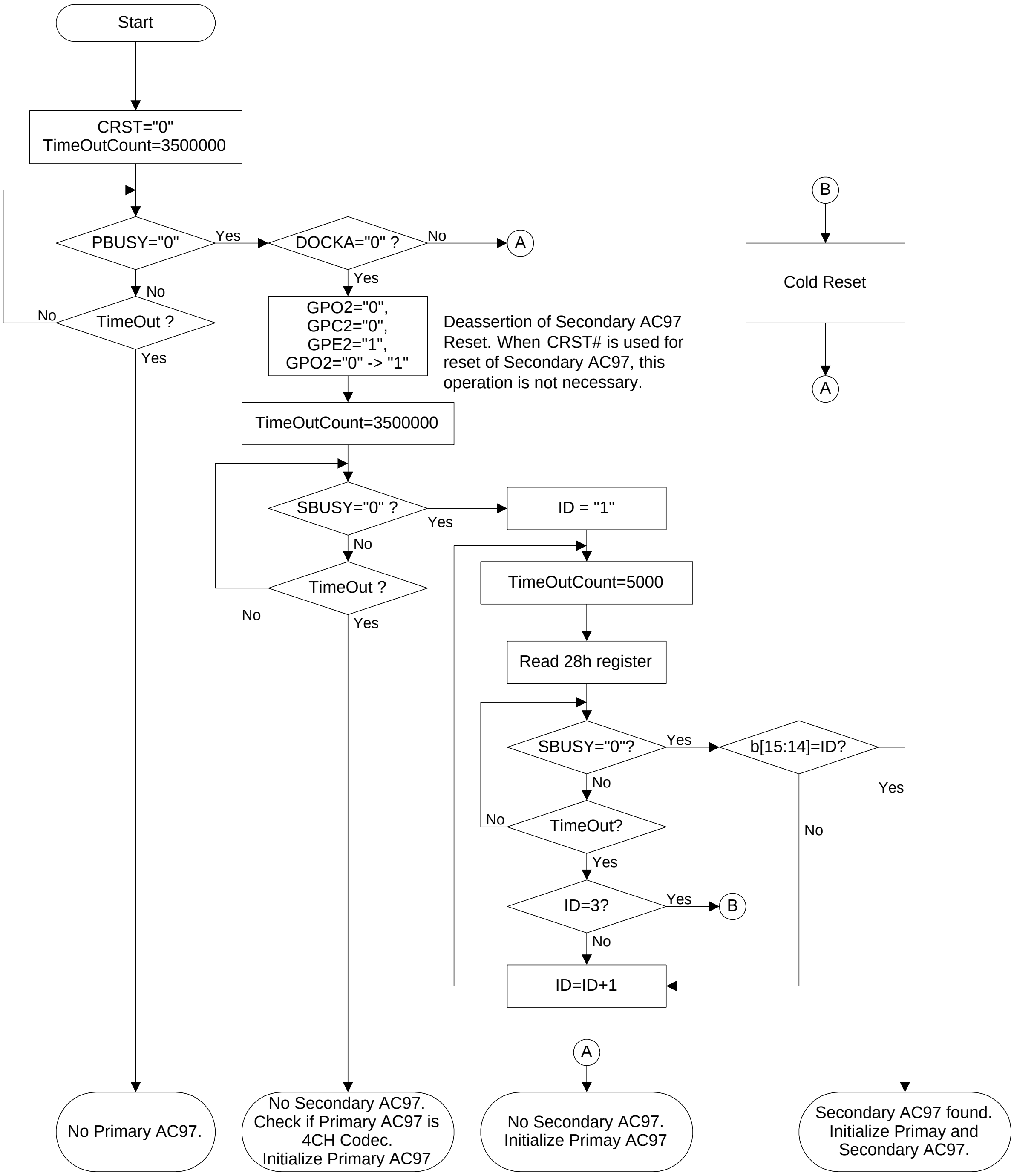
(2) To read from the Primay AC’97, poll the PBUSY of 0066h: Primay AC’97 Status Address until the bit becomes "0". To read from the Secondary AC’97, poll the SBUSY of 006Ah: Secondary AC’97 Status Address until the bit becomes "0".

(3) In case of Primary AC97, the data is read from PRI_STAT_DATA. In case of Secondary AC97, the data is from SEC_STAT_DATA.



Detection of Primary AC'97 and Secondary AC'97

Listed below is the flow chart of how to detect the Primay and Secondary AC’97.



Once the state is placecd in (b), both of PBUSY and SBUSY are held "1" until cleared by Cold Reset for AC97 (setting CRST to "1").

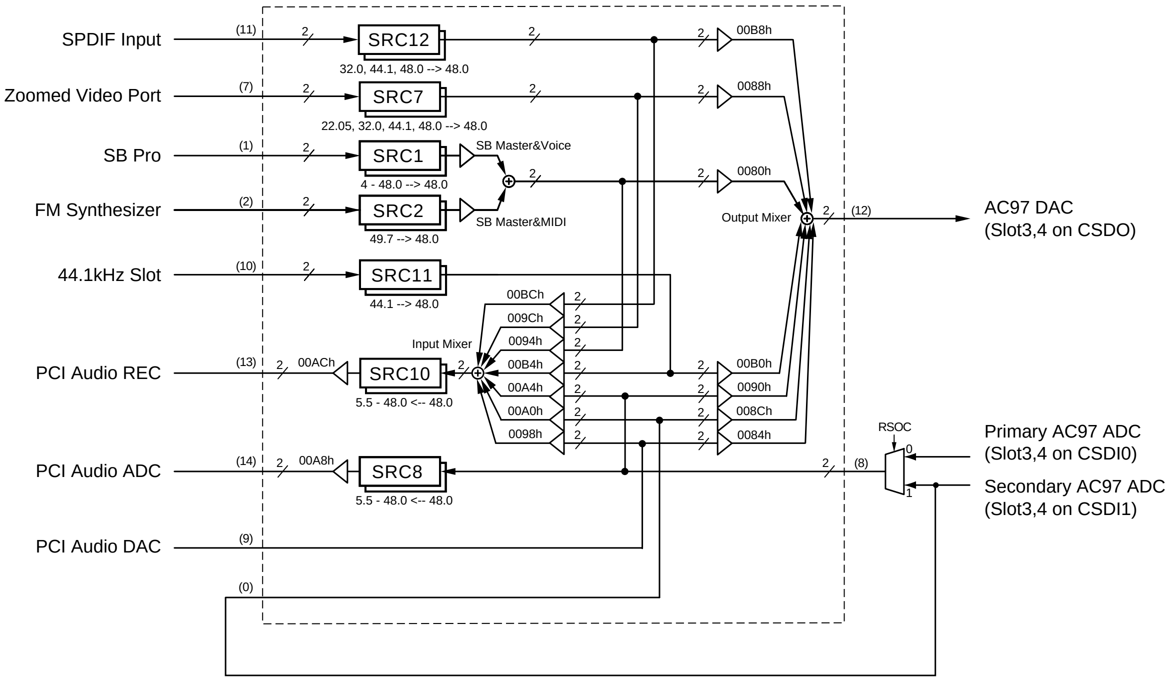
2.4. Description of Volume Control Register

These registers are used to set the attenuation of the volume control in the SRC.

Address	b[31..24]	b[23..16]	b[15..8]	b[7..0]	Remark
0080h	Legacy Audio Output Volume Rch		Legacy Audio Output Volume Lch		
0084h	PCI Audio DAC Output Volume Rch		PCI Audio DAC Output Volume Lch		
0088h	ZV Port Output Volume Rch		ZV Port Output Volume Lch		
008Ch	Secondary AC'97 Output Volume Rch		Secondary AC'97 Output Volume Lch		
0090h	ADC Output Volume Rch		ADC Output Volume Lch		
0094h	Legacy Audio Loopback Volume Rch		Legacy Audio Loopback Volume Lch		
0098h	PCI Audio DAC Loopback Volume Rch		PCI Audio DAC Loopback Volume Lch		
009Ch	ZV Port Loopback Volume Rch		ZV Port Loopback Volume Lch		
00A0h	Secondary AC'97 Loopback Volume Rch		Secondary AC'97 Loopback Volume Lch		
00A4h	ADC Loopback Volume Rch		ADC Loopback Volume Lch		
00A8h	PCI Audio ADC Input Volume Rch		PCI Audio ADC Input Volume Lch		
00ACh	PCI Audio REC Input Volume Rch		PCI Audio REC Input Volume Lch		
00B0h	P44Slot Output Volume Rch		P44Slot Output Volume Lch		
00B4h	P44Slot Loopback Volume Rch		P44Slot Loopback Volume Lch		
00B8h	SPDIF In Output Volume Rch		SPDIF In Output Volume Lch		
00BCh	SPDIF In Loopback Volume Rch		SPDIF In Loopback Volume Lch		

Reserved area is writable but the data will be ignored although the PCI transaction is completed normally. If you try to read Reserved register, the value is read as "0". The Address is offset from 10 - 13h: DS-1E Audio function Memory Base Address.

The structure of the Digital Mixer in the SRC is show below.



When an overflow occurs in the mixer section, the positive value is rounded to +32767, and the negative value is rounded to –32868.

Because the SoundBlaster block hold the last transferred data for playback, this may result in DC offset on the SRC output. To prevent this, mute the volume of the SoundBlaster block when it is not used, or initialize the SoundBlaster using its DSP command.

0080h + (n*4): Output / Loopback / Input Volume Lch

n = 0 - 15
Read / Write
Default: 0000h (0080h=3FFFh)
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	Volume Lch													

b[13:0] .... Volume Lch

This register specifies L-Channel volume (attenuation) of each signal in mixing block. This value is used as DSP coefficient. dB is calculated as follows:

(Volume) = 20 x log(Volume Lch / 16384) [dB]

Any value from 0-16383 can be set to this register. When Volume Lch is set to "0", the volume is muted. Initial values is “0”.

0082h + (n*4): Output / Loopback / Input Volume Rch

n = 0 - 15
Read / Write
Default: 0000h (0082h=3FFFh)
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	Volume Rch													

b[13:0] .... Volume Rch

This register specifies R-Channel volume (attenuation) of each signal in mixing block. This value is used as DSP coefficient. dB is calculated as follows:

(Volume) = 20 x log(Volume Rch / 16384) [dB]

Any value from 0-16383 can be set to this register. When Volume Rch is set to "0", the volume is muted. Initial values is “0”.

2.5. Description of Sampling Rate Register

These registers are used to set the sampling rate of the recording slots.

Address	b[31..24]	b[23..16]	b[15..8]	b[7..0]	Remark
00C0h	Reserved		ADC Slot Sampling Rate		Port#14
00C4h	Reserved		REC Slot Sampling Rate		Port#13
00C8h	Reserved			ADC Format	
00CCh	Reserved			REC Format	
00D0h : 00FCh	Reserved				

Reserved area is writable but all the data will be ignored. If you try to read Reserved register, the value is read as "0". The Address is offset from 10 - 13h: DS-1E Audio function Memory Base Address.

00C0h: ADC Slot Sampling Rate

Read / Write
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	B11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ADC Slot Sampling Rate															

b[15:0] .... ADC Slot Sampling Rate

This register specifies the sampling rate of the ADC Slot.

DS-1E has a low-pass filter that supports sampling rate of 5.51kHz, 8.0kHz, 11.025kHz, 16.0kHz, 22.05kHz, 32.0kHz, 44.1kHz and 48.0kHz. If any other sampling rate is selected, the LPF filter for lower and closest sampling rate is used. The sampling rate is calculated as follows:

Sampling Rate = 48000 * 4096 / SR[Hz] - 1

00C4h: REC Slot Sampling Rate

Read / Write
Default: 0000h
Access Bus Width: 16-bit, 32-bit

b15	b14	b13	b12	b11	B10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
REC Slot Sampling Rate															

b[15:0] .... REC Slot Sampling Rate

This register specifies the sampling rate of the REC Slot.

DS-1E has a low-pass filter that supports sampling rate of 5.51kHz, 8.0kHz, 11.025kHz, 16.0kHz, 22.05kHz, 32.0kHz, 44.1kHz and 48.0kHz. If any other sampling rate is selected, the LPF filter for lower and closest sampling rate is used. The sampling rate is calculated as follows:

Sampling Rate = 48000 * 4096 / SR[Hz] - 1

The table below shows supported sampling rate, register value and actual sampling rate

Target [Hz]	Register Value	Actual Rate [Hz]	Error [%]
5512.5	35665	5512.8	0.005
8000	24575	8000.0	0.000
11025	17832	11025.0	0.000
16000	12287	16000.0	0.000
22050	8915	22051.1	0.005
32000	6143	32000.0	0.000
44100	4457	44102.3	0.005
48000	4095	48000.0	0.000

00C8h: ADC Format

Read / Write
Default: 00h
Access Bus Width: 8-bit, 16-bit, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	CH	BIT

b0 .... BIT

This bit specifies the bit length of PCM data at ADC Slot

"0": 16-bit signed (default)
"1": 8-bit unsigned

b1 .... CH

This bit specifies the number of channel at ADC Slot.

"0": mono (default)
"1": stereo

00CCh: REC Format

Read / Write
Default: 00h
Access Bus Width: 8-bit, 16-bit, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	CH	BIT

b0 .... BIT

This bit specifies the bit length of PCM data at REC Slot

"0": 16-bit signed (default)
"1": 8-bit unsigned

b1 .... CH

This bit specifies the number of channel at ADC Slot.

"0": mono (default)
"1": stereo

2.6. Description of PCI Audio Register

These register controls PCI Audio functions. The structure is shown below:

Address	b[31..24]	b[23..16]	b[15..8]	b[7..0]	Remark
0100h	Status				
0104h	ControlSelect				
0108h	Mode				
010Ch	SampleCount				
0110h	NumOfSample				
0114h	Config				
0118h : 013Ch	Reserved				
0140h	PlayControlSize				
0144h	RecControlSize				
0148h	EffControlSize				
014Ch	WorkSize				
0150h	MapOfRec				
0154h	MapOfEffects				
0158h	PlayControlBase				
015Ch	RecControlBase				
0160h	EffControlBase				
0164h	WorkBase				
0168h : 0FFCh	Reserved				

Reserved area is writable but all the data will be ignored. If you try to read Reserved register, the value is read as "non-0". This value should be ignored since it has no meaning. The Address is offset from 10 - 13h: DS-1E Audio function Memory Base Address.

With the ACTV2 of 0108h: Mode set to “1”, the access to the 140h-17Ch space via PCI bus is inhibited. Prior to the access to this area from the device driver, be sure to veriry that the ACTV is set to “0”.

0100h:Status

Read / Write
Default: 00000000h
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
TINT	-	-	-	-	-	-	-	-	-	-	-	-	-	WKG	ACT
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
INT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b0 ....ACT: Active (Read Only)

This bit indicates the ACTV2 of 0108h: Mode is set to "1" by software during the previous frame.

"0": ACTV2 is not set to "1" during the previous frame (default)

"1": ACTV2 is set to "1" during the previous frame

b1 ....WKG : Working (Read Only)

This bit indicates the DSP and the Controller in PCI Audio block is still active.

"0": The DSP and the Controller is inactive. (default)

"1": The DSP and the Controller is active.

In case of suspend, software needs to store the register values after WKG is set to "0". In case of resume, all stored data should be re-stored to the registers which has been stored for suspend process after power-up. This makes it possible to resume to the exactly same condition before suspend.

b15 .... TINT : TimeInt

This bit indicates DS-1E cannot complete the provided operation in one frame.

"0": Operation is completed in one frame (default)

"1": Operation is not completed in one frame

This bit is set to “1” by the controller and reset to “0” by writing "1" to this bit.

b31 .... INT

This bit is indicates the frame interrupt has occurred.

"0": Interrupt has not occurred (default)

"1": Interrupt has occurred

This bit is set to “1” by the controller and reset to “0” by writing "1" to this bit. When ACTV2 of 0108h: Mode is set to "1" at the beginning of the frame, INT is set to "1". When this bit is set to "1", *INTA#* is asserted. After this bit is cleared, *INTA#* is deasserted.

0104h: Control Select

Read / Write
Default: 00000000h
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CSEL
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b0 .... CSEL: ControlSelect

This bit indicates which Bank of control data is processed by PCI Audio block.

"0": Bank-1 of control data is processed. (default)

"1": Bank-2 of control data is processed

Software can write to the control data that PCI Audio is not processing. Normally, this bit is alternated at every frame.

0108h: Mode

Read / Write
Default: 00000000h
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
TOUT	-	-	-	-	-	-	-	-	-	-	-	-	-	ACTV2	ACTV
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
MUTE	AC3	-	-	-	-	-	-	-	-	-	-	-	-	-	RST

b0 .... ACTV : Active

This bit controls playback and recording operation of PCI Audio block.

"0": PCI Audio stops operation. (default)

"1": PCI Audio enables playback and recording operation.

While ACTV is being set to "1", PCI Audio continues playback and recording operation. When ACTV is set to "0", PCI Audio will not start the process for the new frame after finishing the current frrame processing.
It takes approximately 20 us to start the frame operation after ACTV is set to "1".

b1 .... ACTV2 : Active2

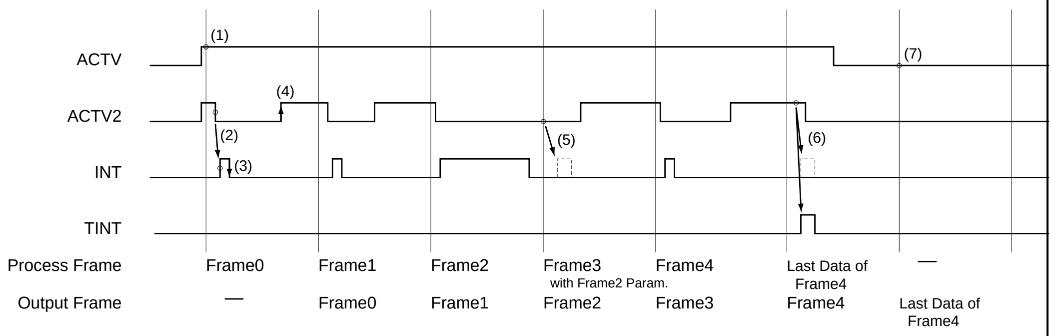
This bit notifies PCI Audio that the software has completed the preparation for the following frame.

"0": Software has not completed yet, or PCI Audio has not started yet. (default)
"1": Software has completed the operation.

After PCI Audio copies ACTV2 value to ACT of 0100h:Status at the frame boundary, ACTV2 is automatically cleared. In order to continue operation, software needs to set ACTV2 to "1" after finishing the necessary process when a frame interrupt has occurred at the frame boundary.

When ACTV2 is set to "1", software should not access the PCI Audio register from 140h to 17Ch.

The operation between software and PCI Audio



(INT is set to "1" when ACT=ACTV2="1" at the beginning of each frame)

(1) The PCI Audio starts the playback and recording operation after ACTV is set to "1".

(2) PCI Audio checks if ACTV2 is set to "1" at the begging of the frame. If ACTV2 is set to "1", the PCI Audio clears ACTV2 and generates the interrupt by setting INT flag to "1".

(3) Software detects the interrupt and clears INT flag.

(4) After software prepares the control data for the following frame, software sets ACTV2 to "1".

The output data is always delayed by one frame. For example, the audio data calculated on Frame0 is generated on the Frame1. the audio data calculated on Frame1 is generated on the Frame2 and so on.

(5) If software cannot set ACTV2 to "1" by the following frame boundary for some reasons, PCI Audio does not set INT flag.

(6) If PCI Audio cannot reset ACTV2 by the frame boundary because it does not complete to generate the audio data of the following frame, PCI Audio sets TINT flag instead of INT flag, and generates the interrupt. The audio data for Frame5 is same as the one held in the last frame:Frame4.

(7) When software sets ACTV to "0", PCI Audio does not process the following frame and stops operation.

b15 .... TOUT : TimeOut

This bit enable to assert *INTA#* when PCI Audio does not complete the operation in one frame.
"0": *INTA#* is not asserted when the operation is not completed in one frame. (default)
"1": *INTA#* is asserted when the operation is not completed in one frame.

b16 .... RST : Reset

This bit resets the PCI Audio block by software.
"0": Reset release (default)
"1": Reset

This bit does not clear the contents in the buffer memory of the PCI Audio block. Please mute 0084h:PCI Audio DAC Output Volume L, R before setting RST to “1”.

b30 .... AC3 : Dolby Digital mode

This bit enables the Effect Slot2 and Effect Slot3 to be used to playback Dolby Digital bit stream or playback the rear channel in 4-channel mode.
"0": Effect Slot2 and Effect Slot3 are used for Effect operation. (default)
"1": Effect Slot2 and Effect Slot3 are used to playback Dolby Digital bit stream or rear channel in 4-channel outpu mode.

In case to playback Dolby Digital bit stream, set SOC of 0018h: SPDIF Output Control to "1". In case to playback rear channel in 4-channel output mode, set 4CHEN of 0070h: Secondary AC'97 Configuration to "1".

b31 .... Mute

This bit controls the muting of the output path from PCI Audio block to SRC block.

"0": un-muted. (default)

"1": muted.

010Ch: SampleCount

Read / Write

Default: 00000000h

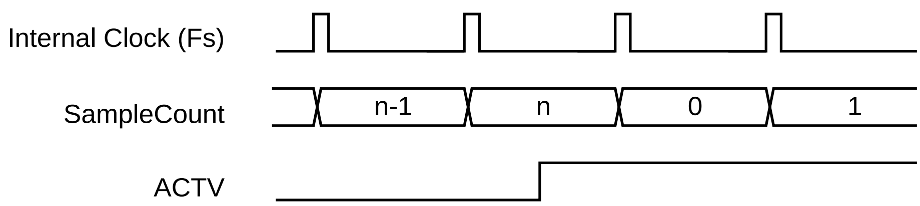
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
SampleCount (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
SampleCount (higher)															

b[31:0] .... SampleCount

This register holds the sample counter value used as an absolute time to calculate the sample position of playback and recording. The sample counter is a 32-bit counter incremented by 1 on every Fs(48kHz). This counter starts operation after the hardwar reset (RST# is deasserted). When the ACTV of 0108h: Mode is set to “1”, the sample couter is reset to “0” synchronized with the internal clock. Initial value is “0”.

Before reading the SampleCount register, the dummy write operation should be performed on the SampleCount register. When the dummy write operation is done, the SampleCount register is updated to the current sample counter value.



0110h: NumOfSample

Read / Write

Default: 00000000h

Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	NumOfSample							
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b[7:0] .... NumOfSample

This register is used to indicate the number of playback / recording sample in a frame. This register is a subset of 010Ch: SampleCount and 8 lower bit of the sample counter can be read. As with the SampleCount, it's reset to "0" automatically at the rising edge of the ACTV.

Before reading the NumSampleCount register, the dummy write operation should be performed on the NumSampleCount register. When the dummy write operation is done, the NumSampleCount register is updated to the current sample counter value.

0114h: Config

Read / Write
Default: 00000000h
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SETUP
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b0 .... SETUP

The PCI Audio block holds the reset state until the SETUP is set to "1" after *RST#* is deasserted. It starts operation after SETUP is set to "1". Software should set "1" to the SETUP after downloading the firmware for the Controller of PCI Audio.

0140h: PlayControlSize

Read Only
Default: 0000001Eh
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PlayControlSize															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b[15:0] .... PlayControlSize

This register indicates the size of one bank of the PlayControlSlotData (DWORD unit).
Software needs to allocate the data area on the system memory for the PlayControlData. PlayControlSize is available after downloading the firmware and setting the SETUP to "1".

0144h: RecControlSize

Read / Write
Default: 00000004h
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	B8	b7	b6	b5	b4	b3	b2	b1	b0
RecControlSize															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b[15:0] .... RecControlSize

This register indicates the size of one bank of the RecControlData (DWORD unit).
Software needs to allocate the data area on the system memory for RecControlData. RecControlSize is available after downloading the firmware and setting the SETUP to "1".

0148h: EffControlSize

Read Only
Default: 00000004h
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
EffControlSize															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b[15:0] .... EffControlSize

This register indicates the size of one bank of the EffectControlData (DWORD unit).

In case of using effect slot, software needs to allocate the data area on the system memory for EffectControlData. EffControlSize is available after downloading the firmware and setting the SETUP to "1".

014Ch: WorkSize

Read Only
Default: 00000000h
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
WorkSize															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b[15:0] .... WorkSize

This register indicates the size of work area (DWORD unit).

In case of using P44Slot for playback, software needs to allocate the data area on the system memory for PCI Audio working area. WorkSize is available after downloading the firmware and setting the SETUP to "1".

0150h: Map of Rec

Read / Write
Default: xxxxxxxxh
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	MapOfRec	
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b[1:0] .... MapOfRec

These bits indicate a flag for valid elements of RecControlData. Each bit indicates whether the slot is valid or invalid.

"0": Invalid
"1": Valid

Each bit corresponds to each slot:

b0: RECSlot
b1: ADCSlot

When all bits are "0", this indicates that there is no recording process, so RecControlData will not be accessed. The specified value will take effect at the beginning of a frame. After the hardware reset, software must initialize these bits by writing “0”.

0154h: Map of Effects

Read / Write
Default: xxxxxxxxh
Access Bus Width: 32-bit

b15	b14	b13	B12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	MapOfEffects				
b31	b30	b29	B28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b[4:0] .... MapOfEffects

These bits indicate a flag for valid elements of EffectControlData. Each bit indicates whether the slot is valid or invalid.

"0": Invalid
"1": Valid

Each bit correspond to each slot:

b0: Dry Lch

b1: Dry Rch

b2: Effect1

b3: Effect2

b4: Effect3

When all bits are "0", this indicates that there is no effect processing, so EffectControlData will not be accessed. The specified value will take effect at the beginning of a frame. After te hardware reset, software must initialize these bits by writing “0”.

0158h: Play Control Base

Read / Write
Default: xxxxxxxxh
Access Bus Width: 32-bit

b15	b14	b13	B12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PlayControlBase (lower)														-	-
b31	b30	b29	B28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PlayControlBase (higher)															

bit[31:2]........ PlayControlBase

This register specifies the physical address of the playback control data referred as PlayControlSlotTable. While this register is set to "0", no playback operation is being processed. After the hardware reset, software must initialize this register by writing “0”.

015Ch: Rec Control Base

Read / Write
Default: xxxxxxxxh
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RecControlBase (lower)														-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
RecControlBase (higher)															

bit[31:2]........ RecControlBase

This register specifies the physical address of the recording control data referred as RecControlData. While this register is set to "0", no recording operation is being processed. After the hardware reset, software must initialize this register by writing “0”

0160h: Effects Control Base

Read / Write
Default: xxxxxxxxh
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
EffControlBase (lower)														-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
EffControlBase (higher)															

bit[31:2]........ EffControlBase

This register specifies the physical address of the effect control data referred as EffectControlData. While this register is set to "0", no effect operation is being processed. After the hardware reset, software must initialize this register by writing “0”.

0164h: Work Base

Read / Write
Default: xxxxxxxxh
Access Bus Width: 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
WorkBase (lower)														-	-
b31	b30	b29	b28	b27	B26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
WorkBase (higher)															

bit[31:2]........ WorkBase

This register specifies the physical address of work area.
When this register is set to "0", PCI Audio can not use work area. So it may leads to noise when using P44slot for playback. After the hardware reset, software must initialize this register by writing “0”.

2.7. Description of Controller Instruction RAM

The Controller instruction RAM is located in this area.

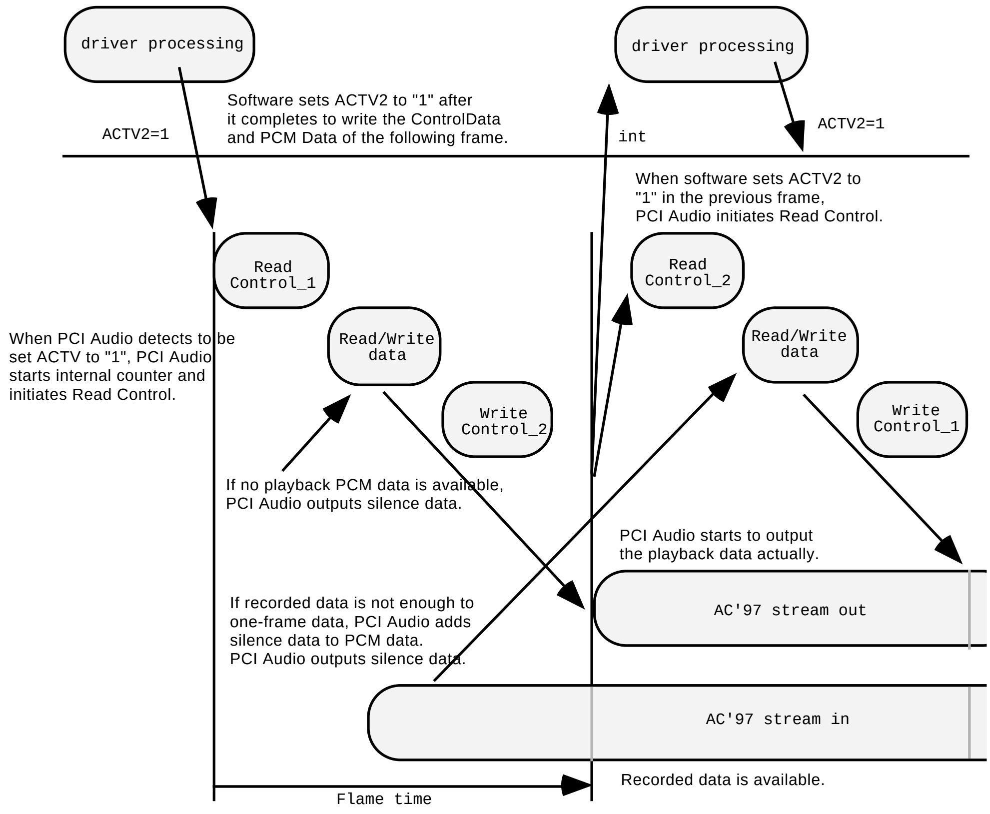
Address	b[31:24]	b[23:16]	b[15:8]	b[7:0]	Remark
4000h : 6FFCh	Controller Instruction RAM				
7000h : 7FFCh	Reserved				

Reserved area is writable but all the data will be ignored. If you try to read Reserved register, the value is read as "non-zero". This value should be ignored since it has no meaning. The Address is offset from 10 - 13h: DS-1E Audio function Memory Base Address.

Software should not access this area when SETUP of 0114h:Config is set to "1".

3. PCI Audio Operation

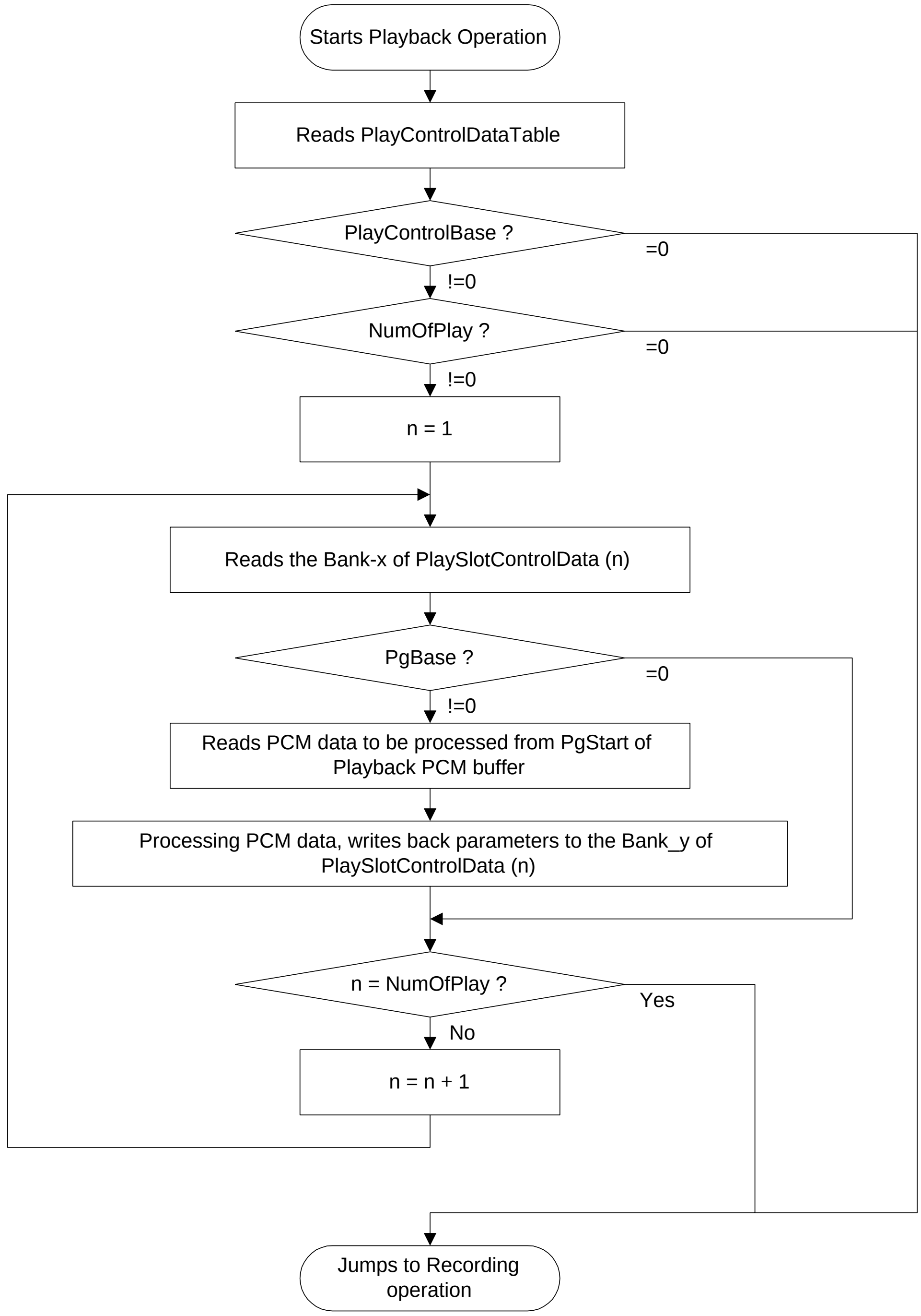
The below indicates the PCI Native Audio operation flow:



Flow of data processing (normal case)

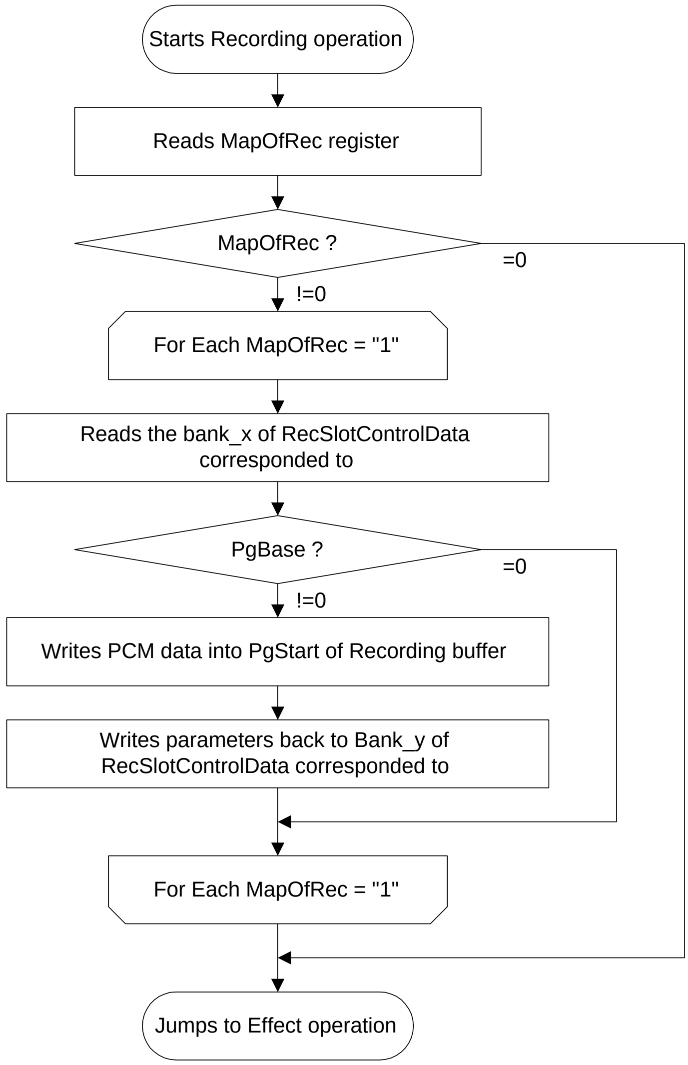
The PCI Audio block handles 256-samples (@Fs=48kHz) as 1-frame.
When ACTV of 0108h: Mode is set to "1", PCI Audio processes the playback operation, recording operation and effect operation one by one from the start of the frame. In each operation, PCI Audio read ControlData, process PCM data and write back ControlData to the system memory.
PCI Audio starts to process each operation on the beginning of the frame. Upon completion of one process, PCI Audio stops its operation until it detects the next frame start timing. If PCI did not complete the process within the frame, it skips the process for the following frames. In this case, PCM output holds the data of the last sample.
PCI Audio still continues the process until ACTV is set to "0".
Outline of each process is described in the following sections.

3.1. Play Slot Operation



When Bank_x is Bank-1, Bank_y is the other Bank meaning Bank-2. In each frame boundary, Bank_x is alternated between Bank-1 and Bank-2, such as Bank-1 -> Bank-2 -> Bank-1 - > Bank-2....
When CSEL of <u>0104h: Control Select</u> is set to "1" at Frame start, PCI Audio reads ControlData from Bank-2. When CSEL="0", PCI Audio reads them from Bank-1.

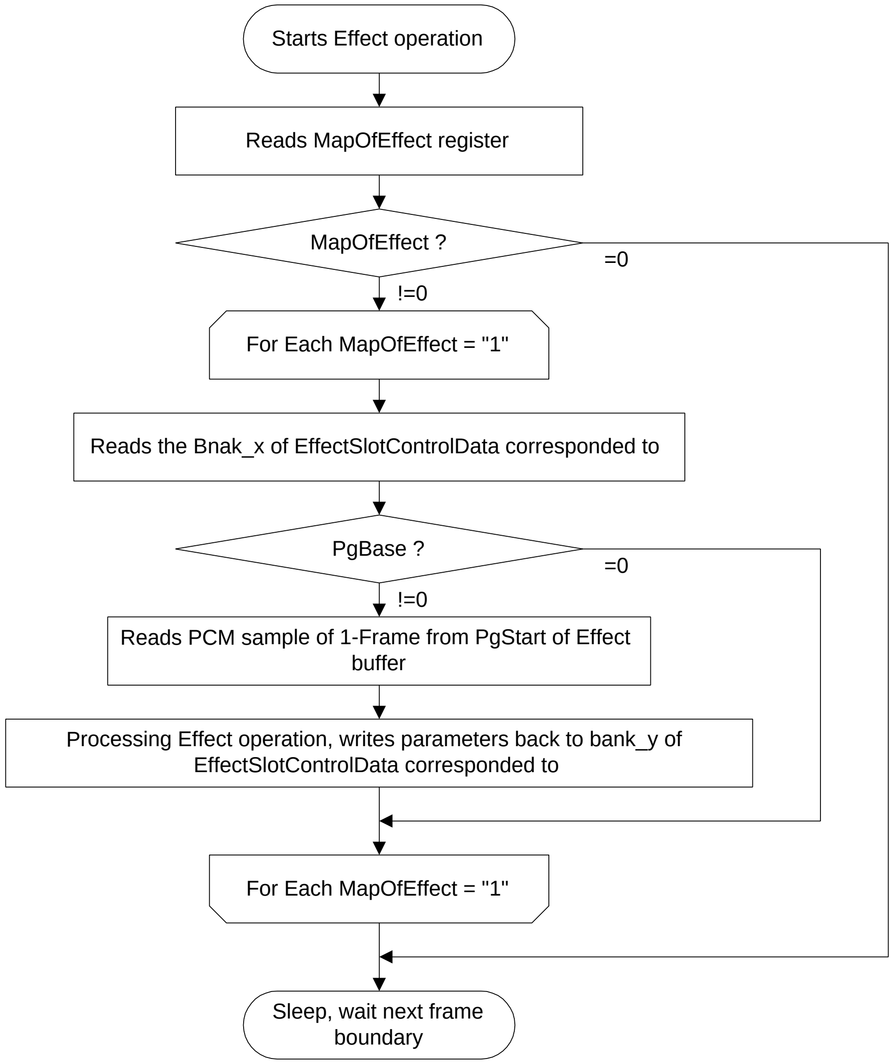
3.2. Recording Slot Operation



When Bank_x is Bank-1, Bank_y is the other Bank meaning Bank-2. In each frame boundary, Bank_x is alternated between Bank-1 and Bank-2, such as Bank-1 -> Bank-2 -> Bank-1 - > Bank-2....

When CSEL of <u>0104h: Control Select</u> is set to "1" at Frame start, PCI Audio reads ControlData from Bank-2. When CSEL="0", PCI Audio reads them from Bank-1.

3.3. Effect Slot Operation



When Bank_x is Bank-1, Bank_y is the other Bank meaning Bank-2. In each frame boundary, Bank_x is alternated between Bank-1 and Bank-2, such as Bank-1 -> Bank-2 -> Bank-1 - > Bank-2....
When CSEL of 0104h: Control Select is set to "1" at Frame start, PCI Audio reads ControlData from Bank-2. When CSEL="0", PCI Audio reads them from Bank-1.

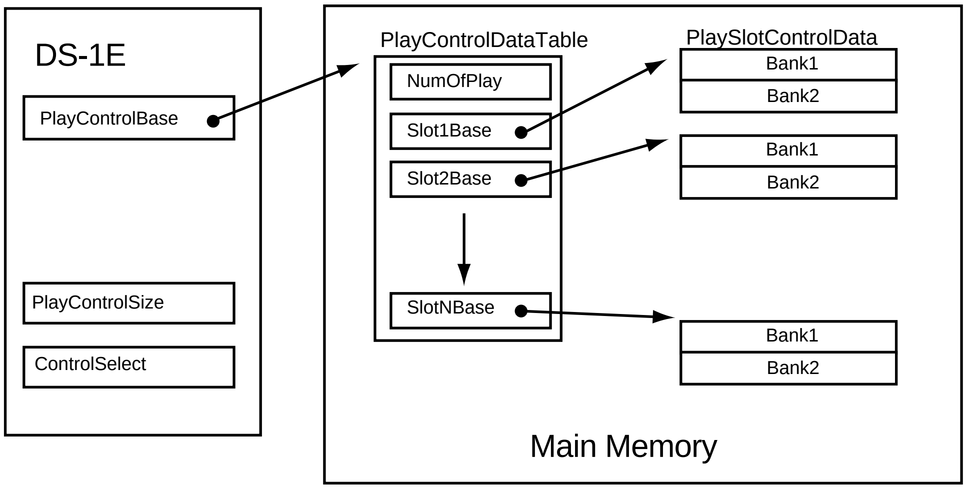
4. DSP Control Data

This Chapter explains the PCI Audio ControlData that is allocated in the host memory. There are three types of control data: PlayControlData, RecordingControlData and EffectControlData. The structure of each control data is shown below.

4.1. Structure of PCI Audio Control Data

4.1.1. PlayControlData

The PlayControlData consists of the PlayControlDataTable and PlaySlotControlData.



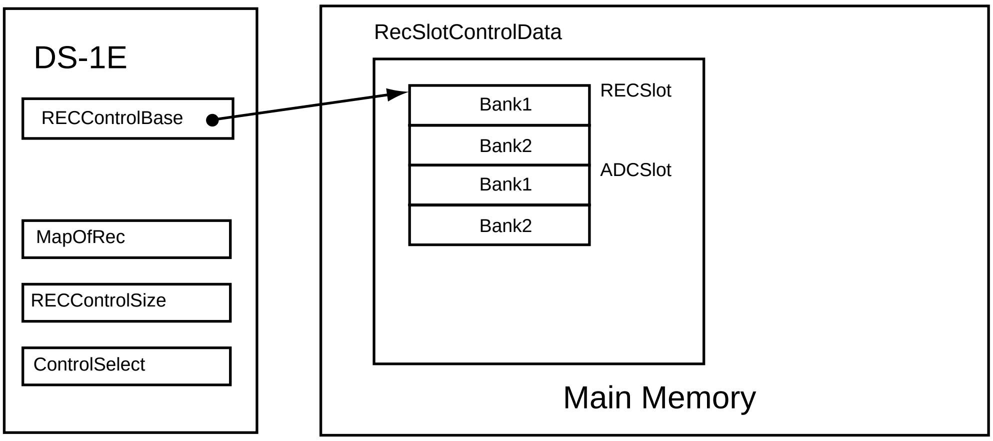
0158h: Play Control Base specifies the Base Address of PlayControlDataTable as physical memory address.

The PlayControlDataTable includes the number of PlaySlotControlData to be processed in this frame, and the Base Address of each PlaySlotControlData as physical memory address. The number of playback slots can be changed at each frame. The PlayControlDataTable must be allocated in the physically continuous memory space.

The PlaySlotControlData includes two Banks of Slot Data. The size of one Bank of Slot Data can be read from 0140h: PlayControlSize. The PlaySlotControlData must be allocated in the physically continuous memory space.

4.1.2. RecordingControlData

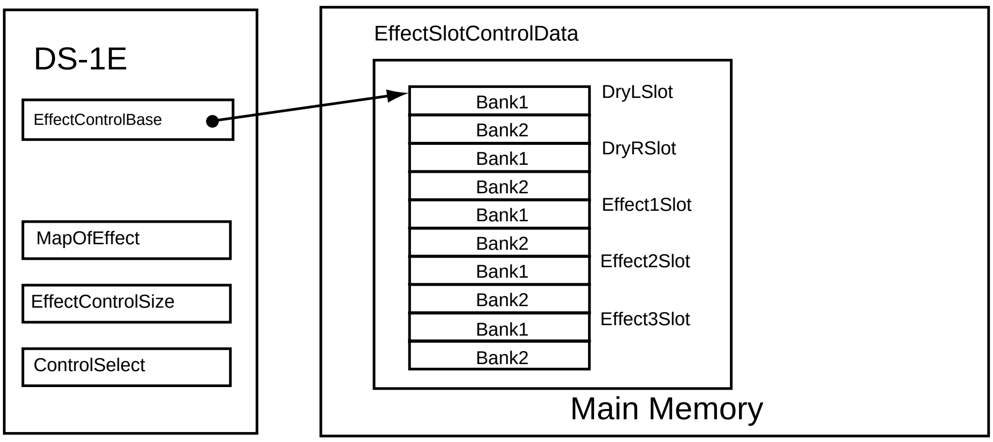
The RecSlotControlData consists of the ControlData for RECSlot and the ControlData for ADCSlot. The both ControlData includes two Banks of Slot Data.



015Ch: Rec Control Base specifies the base address of RecSlotControlData as physical memory address. The RecSlotControlData must be allocated in the physically continuous memory space.

4.1.3. EffectControlData

The EffectSlotControlData consists of the ControlData for Effect Slot3, Effect Slot2, Effect Slot1, DryL Slot and DryR Slot. The each ControlData includes two Banks of Slot Data.



0160h: Effects Control Base specifies the base address of EffectSlotControlData as physical memory address. The EffectSlotControlData must be allocated in the physically continuous memory space.

4.2. Description of Play Control Data

This section describes the format of the PlayControlData.

4.2.1. Play Control Data Table

The structure of the PlayControlDataTable is shown below:

Offset	b[31..24]	B[23..16]	b[15..8]	b[7..0]
0000h	NumOfPlay			
0004h	Slot1Base			
0008h	Slot2Base			
:	:			
4 * n	SlotnBase			
:	:			
4 * N	SlotNBase			

The parameters are addressed in DWORD units.

000h: NumOfPlay

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
NumOfPlay (lower)															
b31	b30	b29	b28	b27	b26	B25	b24	b23	b22	b21	b20	b19	b18	b17	b16
NumOfPlay (higher)															

b[31:0] .... NumOfPlay

This specifies the number of PlaySlotControlData to be processed in this frame. When NumOfPlay is set to "0", no playback processing will occur. When NumOfPlay is set to any value more than "41h", DS-1E will process up-to 64 PlayControlSlotData.

004h + (x – 1) * 4: SlotxBase

x: Slot Number (1 - NumOfPlay)

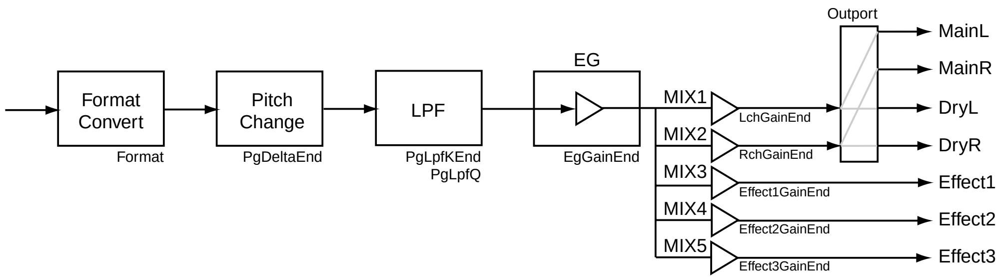
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
SlotxBase (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
SlotxBase (higher)															

b[31:0] .... SlotxBase

This specifies the base address of each PlaySlotControlData as physical memory address. When SlotxBase (0 <= x <= N) is set to "0", the process of corresponding Playback Slot is skipped.

4.2.2. Play Slot Control Data

The playback slot of the DS-1E consists of the following blocks. (In case of P44Slot, the following block is bypassed and PCM data is transferred directly to SRC block.) The DS-1E can process 64 slots at maximum in one frame time. Each playback slot can playback only monaural data. To playback stereo data, use two playback slots.



The structure of the PlaySlotControlData is shown below. All parameters are addressed in DWORD units. Before starting playback, allocate both Bank of ControlData.

Offset	Pointer	b[31..24]	b[23..16]	b[15..8]	b[7..0]
0000h	0	Format			
0004h	1	LoopDefault			
0008h	2	PgBase			
000Ch	3	PgLoop			
0010h	4	PgLoopEnd			
0014h	5	PgLoopFrac			
0018h	6	PgDeltaEnd			
001Ch	7	LpfKEnd			
0020h	8	EgGainEnd			
0024h	9	LchGainEnd			
0028h	10	RchGainEnd			
002Ch	11	Effect1GainEnd			
0030h	12	Effect2GainEnd			
0034h	13	Effect3GainEnd			
0038h	14	LpfQ			
003Ch	15	Status			
0040h	16	NumOfFrames			
0044h	17	LoopCount			
0048h	18	PgStart			
004Ch	19	PgStartFrac			
0050h	20	PgDelta			
0054h	21	LpfK			
0058h	22	EgGain			
005Ch	23	LchGain			
0060h	24	RchGain			
0064h	25	Effect1Gain			
0068h	26	Effect2Gain			
006Ch	27	Effect3Gain			
0070h	28	LpfD1			
0074h	29	LpfD2			

SlotxBase + 000h : Format

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	OutPt	-	-	-	-	-	-	-	ChOff
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Fmt	-	-	SRC441	-	-	-	StpRq	-	-	-	-	-	-	-	NofCh

bit0............... ChOff:Channel Offset

This bit selects the playback channel for this slot.

"0": Lch

"1": Rch

b8 .... OutPt:Out Port

This bit selects the output port for this slot.

"0": MainL, R

"1": DryL, R

b16 .... NofCh:Number of Channel

This bit specifies the number of channels for this slot.

"0": Mono

"1": Stereo

When stereo is selected, this slot and the next slot will be used to play stereo PCM data. The stereo channel is assigned by the ChOff bit and the the volume is controlled by the XxGainEnd(PgGainEnd, LchGainEnd, RchGainEnd, Effect1GainEnd, Effect2GainEnd, Effect3GainEnd) and XxGain(PgGain, LchGain, RchGain, Effect1Gain, Effect2Gain, Effect3Gain). The Other parameters should be set to the same value in both slots.

b24 .... StpRq:Stop Request

This bit selects playback mode.

"0": Loops the number specified in SlotxBase + 004h: LoopDefault

"1": Stops playback automatically when SlotxBase + 048h: PgStart reaches to SlotxBase + 010h: PgLoopEnd.

b28 .... SRC441:SRC for 44.1kHz Play Slot

This bit specifies the output port for this slot.

"0": Pslot

"1": P44slot

P44Slot is used for high-quality sampling rate conversion at 44.1kHz playback. If you need high-quality sampling rate conversion at 44.1kHz, please use P44Slot rather than normal PSlot. P44Slot can be used by only one-PlaySlotControlData among all PlaySlotControlData. The slot assigned to P44Slot can play stereo PCM data by own slot and the format is fixed to 16-bit signed.

When P44Slot is used, the following parameters are effective: StopReq, LoopDefault, PgBase, PgLoop, PgLoopEnd, Status, NumOfFrames, LoopCount and PgStart. Please set "0" to the other parameters.

The volume for P44Slot is controlled by 00B0h: P44Slot Loopback Volume.

b31 .... Fmt:Format

This bit specifies the data format for the slot.

"0": 16-bit signed

"1": 8-bit unsigned

b[30:29], b[27:25], b[23:17], b[15:9], b[7:1]

These bits must be "0".

SlotxBase + 004h: LoopDefault

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
LoopDefault (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
LoopDefault (higher)															

b[31:0] .... LoopDefault

This parameter specifies the number of data loops between SlotxBase + 00Ch: PgLoop and SlotxBase + 010h: PgLoopEnd. When "0" is set, it continues to loop until playback stops. When "1" is set, it becomes one-shot sound.

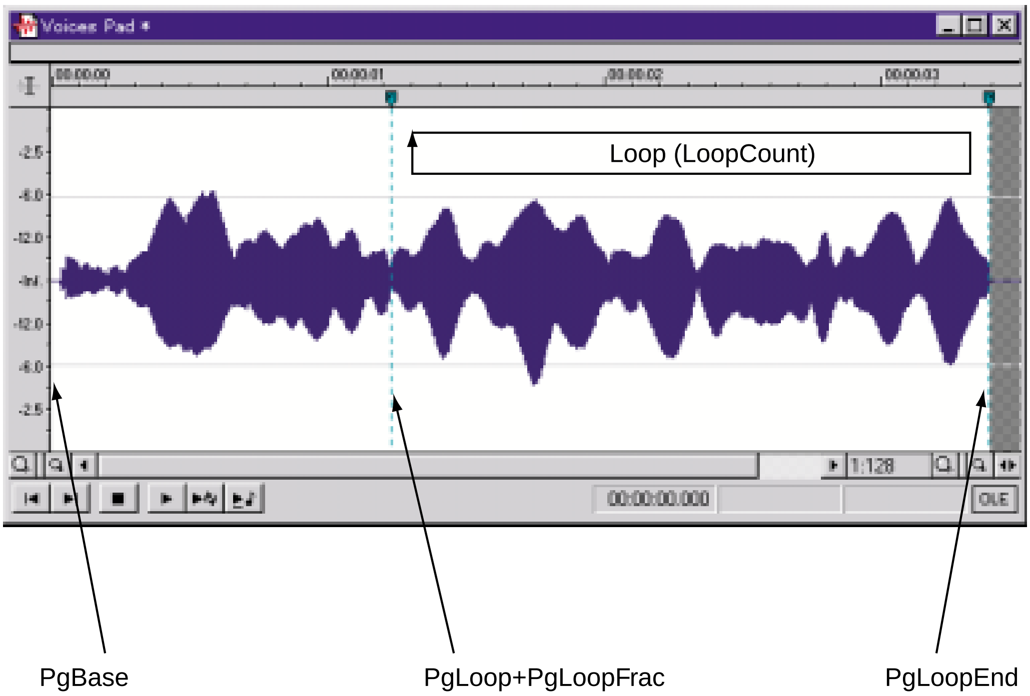
SlotxBase + 008h: PgBase

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	B2	b1	b0
PgBase (lower)														-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgBase (higher)															

b[31:2] .... PgBase

This parameter specifies the base address of PCM Data Buffer as physical address. PCM Data buffer must be allocated in the physically continuous memory space and DWORD boundary. (lower two bits must be "0"). The Sound Data Parameter is shown below. PCM Data format is compliant to Microsoft WAVE (PCM) format.



b[1:0]

These bits must be "0".

SlotxBase + 00Ch: PgLoop

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PgLoop (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgLoop (higher)															

b[31:0] .... PgLoop

This parameter specifies the Loop Start Address that is the sample number offset from PgBase. The same process is done as one shot sound where PgLoop = SlotxBase + 010h: PgLoopEnd.

SlotxBase + 010h: PgLoopEnd

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PgLoopEnd (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgLoopEnd (higher)															

b[31:0] .... PgLoopEnd

This parameter specifies the Loop End Address that is the sample sumber offset from PgBase. Set the number added by one to the actual End Address to the PgLoopEnd Register.

SlotxBase + 014h: PgLoopFrac

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PgLoopFrac (lower)				-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	B18	b17	b16
PgLoopFrac (higher)															

b[31:12] .... PgLoopFrac

This parameter specifies the decimal fraction of Loop Start Address.

Loop Start Point = PgLoop + (PgLoopFrac / 2^{20})

b[11:0]

These bits must be "0".

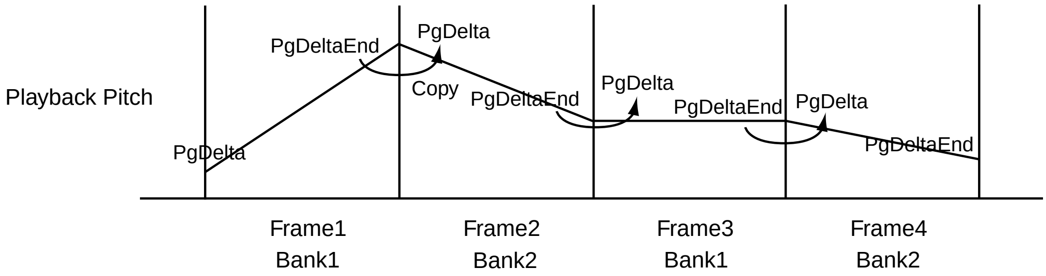
SlotxBase + 018h: PgDeltaEnd

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PgDeltaEnd (lower)								-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	B18	b17	b16
-	PgDeltaEnd (higher)														

b[30:8] .... PgDeltaEnd

This parameter specifies the pitch at the end of the current frame. The DS-1E playback pitch is determined by two parameters: One is SlotxBase + 050h: PgDelta (beginning of the frame). The other one is PgDeltaEnd (end of fthe frame).



PgDeltaEnd is copied automatically to PgDelta of the next bank by the controller. During the playback, pitch is controlled by PgDeltaEnd so do not change the PgDelta. PgDelta can be set at the beginning of playback. Bit[30:28] indicates an integer part, and bit[27:8] indicates a decimal fraction part. Pith is calculated as shown below:

(Playback Pitch) = PgDeltaEnd / 2^{28}

Playback pitch supports up-to 4.0(192kHZ) with mono data and supports up-to 2.0(96Hz) with stereo data. If PCM data is playbacked with the specified sample rate, set the value to PgDeltaEnd which is calculated by the equation below:

PgDeltaEnd = ((Specified Sampling Rate) / 48000 * 2^{28}) & 0x7FFFFF00

b31, b[7:0]

These bits must be "0".

SlotxBase + 01Ch: LpfKEnd

x: Slot Number (1 - NumOfPlay)

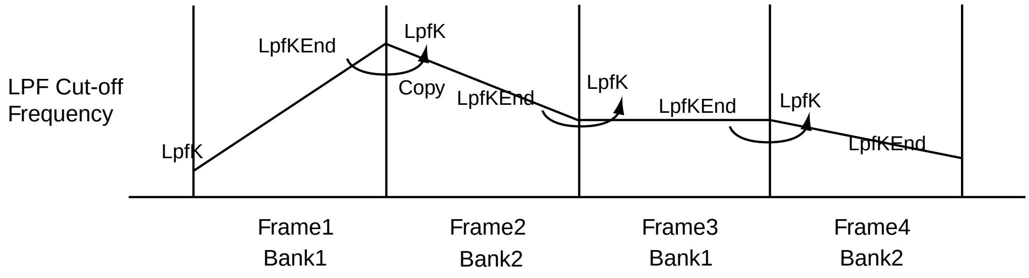
b15	B14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	B30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
LpfKEnd													-	-	-

b[31:19] .... LpfKEnd

This parameter specifies the cut-off frequency of LPF at the end of the current frame. The value set to LpfK and LpfKEnd is sown below:

Sampling Rate [Hz]	LpfK, LpfKEnd [DWORD]
8.0k	0x18B00000
11.025k	0x20900000
16.0k	0x2B980000
22.05k	0x35A00000
32.0k	0x40000000
44.1k	0x40000000
48.0k	0x40000000

The LPF cut-off frequency for DS-1E is determined by two parameters: One is the cutoff (SlotxBase + 054h: LpfK) at the beginning of the frame. The other is the cutoff (LpfKEnd) is at the end of the frame.



The value of LpfKEnd is copied automatically to LpfK of the next bank data by the controller. During the playback, LPF cutoff is controlled by LpfKEnd so do not change the LpfK. LpfK can be set at the beginning of playback.

b[18:0]

These bits must be "0".

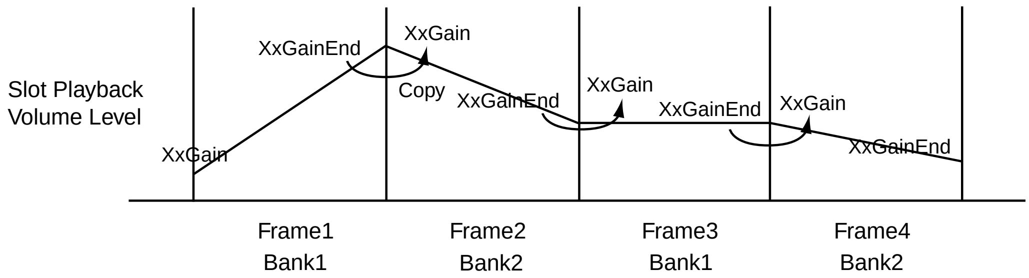
SlotxBase + 020h: EgGainEnd

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	B7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
EgGainEnd (higher)															

b[31:15] .... EgGainEnd

This parameter specifies the Gain of EG (Envelope Generator) at the end of current frame. The DS-1E volume level is determined by two parameters: One is the XxGain at the beginning of the frame. The other is the XxGainEnd at the end of frame.



XxGain: PgGain, LchGain, RchGain, Effect1Gain, Effect2Gain, Effect3Gain
XXGainEnd: PgGainEnd, LchGainEnd, RchGainEnd, Effect1GainEnd, Effect2GainEnd, Effect3GainEnd

The value of XxGainEnd is copied automatically to XxGain of the next bank data by the controller. During the playback, the volume is controlled by XxGainEnd so do not change the XxGain. XxGain can be set at the beginning of playback.

Bit31 indicates a sign bit. Bit30 indicates an integer part, and bit[29:15] indicates a decimal fraction part.
The sign bit for positive number is "0", and "1" for negative number.

-1.0 (0xC0000000) - +1.0 (0x40000000)

b[14:0]

These bits must be "0".

SlotxBase + 024h: LchGainEnd

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
LchGainEnd (higher)															

b[31:15] .... LchGainEnd

This parameter specifies the volume of MIX1 (MainL/DryL Output) at the end of this frame. Please refer to description of SlotxBase + 020h: EgGainEnd.

b[14:0]

These bit must be "0".

SlotxBase + 028h: RchGainEnd

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
RchGainEnd (higher)															

b[31:15] .... RchGainEnd

This parameter specifies the volume of MIX2 (MainR/DryR Output) at the end of this frame. Please refer to description of SlotxBase + 020h: EgGainEnd.

b[14:0]

These bit must be "0".

SlotxBase + 02Ch: Effect1GainEnd

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
EffectGain1End (higher)															

b[31:15] Effect1GainEnd

This parameter specifies the volume of MIX3 (Effect1 Output) at the end of this frame. Please refer to description of SlotxBase + 020h: EgGainEnd.

b[14:0]

These bits must be "0".

SlotxBase + 030h: Effect2GainEnd

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Effect2GainEnd (higher)															

b[31:15] Effect2GainEnd

This parameter specifies the volume of MIX4 (Effect2 Output) at the end of this frame. Please refer to description of SlotxBase + 020h: EgGainEnd.

b[14:0]

These bits must be "0".

SlotxBase + 034h: Effect3GainEnd

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Effect3GainEnd (higher)															

b[31:15] Effect3GainEnd

This parameter specifies the volume of MIX5 (Effect3 Output) at the end of this frame. Please refer to description of SlotxBase + 020h: EgGainEnd.

b[14:0]

These bits must be "0".

SlotxBase + 038h: LpfQ

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
LpfQ													-	-	-

b[31:19] .... LpfQ

This parameter specifies the LPF resonance. The value set to LpfQ is shown below:

Sampling Rate [Hz]	LpfQ [DWORD]
8.0k	0x32020000
11.025k	0x31780000
16.0k	0x31380000
22.05k	0x31C80000
32.0k	0x33D00000
44.1k	0x40000000
48.0k	0x40000000

b[18:0]

These bits must be "0".

SlotxBase + 03Ch: Status

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DEND
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b0 .... DEND: Data End

This parameter indicates the playback is done at this slot. Once DEND bit is set to "1", playback cannot be operated unless software sets "0" to this bit.

"0": Playback

"1": Playback is done

b[31:1]

These bits must be "0".

SlotxBase + 040h: NumOfFrames

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
NumOfFrames (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
NumOfFrames (higher)															

b[31:8] .... NumOfFrames

This parameter indicates the number of frames that has already been playbacked. It's incremented by one every time interrupt occurs. This parameter is automatically copied to that of the next bank. This parameter must be initialized before playback.

When software needs to read this parameter, use the Bank that DS-1E does not operate.

SlotxBase + 044h: LoopCount

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
LoopCount (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
LoopCount (higher)															

b[31:0] .... LoopCount

This parameter indicates the number of loops that has already occurred. When SlotxBase + 048h: PgStart returns to SlotxBase + 00Ch: PgLoop, the controller increment the LoopCount. This parameter must be initialized before playback.

When software needs to read this parameter, use the Bank that DS-1E does not operate.

SlotxBase + 048h: PgStart

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	B9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PgStart (lower)															
b31	b30	b29	b28	b27	b26	B25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgStart (higher)															

b[31:0] .... PgStart

This parameter indicates the integer part of the processed number of the samples offset from SlotxBase + 008h: PgBase at the beginning of the current frame. This parameter must be initialized before playback. The controller

starts to playback from the offset address specified PgStart.
When software needs to read this parameter, use the Bank that DS-1E does not operate.

SlotxBase + 04Ch: PgStartFrac

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PgStartFrac (lower)					-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgStartFrac (higher)															

b[31:11] .... PgStartFrac

This parameter indicates the decimal fraction part of the processed number of the samples offset from SlotxBase + 008h: PgBase.

b[10:0]

These bits must be "0".

SlotxBase + 050h: PgDelta

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PgDelta (lower)								-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	PgDelta (higher)														

b[30:8] .... PgDelta

This parameter specifies the playback Pitch at the beginning of the frame. Please refer to the description of SlotxBase + 018h: PgDeltaEnd. This parameter must be initialized before playback.

b31, b[7:0]

These bits must be "0".

SlotxBase + 054h: LpfK

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
LpfK													-	-	-

b[31:19] .... LpfK

This parameter specifies the LPF cutoff frequency at the beginning of the frame. Please refer to the description of SlotxBase + 01Ch: LpfKEnd. This parameter must be initialized before playback.

b[18:0]

These bits must be "0".

SlotxBase + 058h: EgGain

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
EgGain (higher)															

b[31:15] .... EgGain

This parameter specifies the playback volume level at the beginning of the frame. Please refer to the description of SlotxBase + 020h: EgGainEnd. This parameter must be initialized before playback.

b[14:0]

These bits must be "0".

SlotxBase + 05Ch: LchGain

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
LchGain (higher)															

b[31:15] .... LchGain

This parameter specifies the volume of MIX1 (MainL/DryL Output) at the beginning of the frame. Please refer to the description of SlotxBase + 020h: EgGainEnd. This parameter must be initialized before playback.

b[14:0]

These bits must be "0".

SlotxBase + 060h: RchGain

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
RchGain (higher)															

b[31:15] .... RchGain

This parameter specifies the volume of MIX2 (MainR/DryR Output) at the beginning of the frame. Please refer to the description of SlotxBase + 020h: EgGainEnd. This parameter must be initialized before playback.

b[14:0]

These bits must be "0".

SlotxBase + 064h: Effect1Gain

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Effect1Gain (higher)															

b[31:15] Effect1Gain

This parameter specifies the volume of MIX3 (Effect1 Output) at the beginning of the frame. Please refer to the description of SlotxBase + 020h: EgGainEnd. This parameter must be initialized before playback.

b[14:0]

These bits must be "0".

SlotxBase + 068h: Effect2Gain

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Effect2Gain (higher)															

b[31:15] Effect2Gain

This parameter indicates the volume of MIX4 (Effect2 Output) at the beginning of the frame. Please refer to the description of SlotxBase + 020h: EgGainEnd. This parameter must be initialized before playback.

b[14:0]

These bits must be "0".

SlotxBase + 06Ch: Effect3Gain

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(lower)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Effect3Gain (higher)															

b[31:15] Effect3Gain

This parameter indicates the volume of MIX5 (Effect3 Output) at the beginning of the frame. Please refer to the description of SlotxBase + 020h: EgGainEnd. This parameter must be initialized before playback.

b[14:0]

These bits must be "0".

SlotxBase + 070h: LpfD1

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	B6	b5	b4	b3	b2	b1	b0
LpfD1 (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
LpfD1 (higher)															

b[31:0] LpfD1

This parameter is used by the controller for the playback operation.

SlotxBase + 074h: LpfD2

x: Slot Number (1 - NumOfPlay)

b15	b14	b13	b12	b11	b10	b9	b8	b7	B6	b5	b4	b3	b2	b1	b0
LpfD2 (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
LpfD2 (higher)															

b[31:0] LpfD2

This parameter is used by the controller for the playback operation.

4.2.3. Recording Slot Control Data

DS-1E Recording Slot is not similar to playback slot and input source is determined by the slot number.

Slot1: ADC L/Rch

Slot2: REC L/Rch

Recording data is transferred after it is re-sampled by the specified sampling rate in the SRC block. One Recording Slot can handle both mono and stereo PCM data.

The register to specify sampling rate and audio format is allocated in PCI Audio registers. The parameters to control Recording Slot are shown below:

Offset	b[31..24]	b[23..16]	b[15..8]	b[7..0]
0000h	PgBase			
0004h	PgLoopEndAdr			
0008h	PgStartAdr			
000Ch	NumOfLoops			

Before start recording, both Slot data of Bank-1 and Bank-2 must be prepared.

000h: PgBase

b15	b14	b13	b12	b11	b10	b9	b8	b7	B6	b5	b4	b3	b2	b1	b0
PgBase (lower)														-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgBase (higher)															

bit[31:2]........ PgBase

This parameter specifies the physical memory address to store the recorded PCM data. The recording buffer should be allocated in the physically continuous memory space and DWORD boundary (lower two bits are must be "0").

bit[1:0]

These bits must be "0".

004h: PgLoopEndAdr

b15	b14	b13	b12	b11	b10	b9	b8	b7	B6	b5	b4	b3	b2	b1	b0
PgLoopEndAdr (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgLoopEndAdr (higher)															

bit[31:0]........ PgLoopEndAdr

This parameter specifies the size of recording buffer (BYTE units) as an offset from 000h: PgBase. This value has to be the next address of the last sample. The number multiplied by 4 always has to be set. When PgStart reaches to PgLoopEnd, the PgSatrt is automatically reset to "0".

008h: PgStartAdr

b15	b14	b13	b12	b11	b10	b9	b8	b7	B6	b5	b4	b3	b2	b1	b0
PgStartAdr (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgStartAdr (higher)															

bit[31:0]........ PgStartAdr

This parameter indicates the number of the processed sample as offset from 000h: PgBase at the beginning of the current frame. The number multiplied by 4 always has to be set. By reading PgStartAdr, software is abe to know the processed address at the beginning of the frame. This parameter must be initialized before recording. During recording, read from the Bank that controller does not process.

00Ch: NumOfLoops

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
NumOfLoops (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
NumOfLoops (higher)															

bit[31:0]........ NumOfLoops

This parameter indicates the number of loops to be done for writing data to recording buffer. When PgStartAdr is returned to "0", this parameter is incremented. This parameter must be initialized prior to start of recording. During recording, read from the Bank that controller does not process.

4.2.4. Effect Slot Control Data

For DS-1E Effect Slot, input sources are fixed by the slot number.

Slot1: Dry Lch
Slot2: Dry Rch
Slot3: Effect1 (Reverb)
Slot4: Effect2
Slot5: Effect3

For Effect Slot, mono 16-bit signed PCM data can be used. The sampling rate is fixed to 48kHz. The parameters to control Effect Slot are shown below:

Offset	b[31..24]	b[23..16]	b[15..8]	b[7..0]
0000h	PgBase			
0004h	PgLoopEnd			
0008h	PgStart			
000Ch	Temp			

Before using Effect Slot, both slot data of Bank-1 and Bank-2 must be prepared.

000h: PgBase

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PgBase (lower)														-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgBase (higher)															

bit[31:2]........ PgBase

This parameter specifies the base address of Effect buffer to store PCM data with effect as physical address. The Effect buffer should be allocated in the physically continuous memory and DWORD boundary (lower two bits are must be "0").

bit[1:0]

These bits must be "0".

004h: PgLoopEnd

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PgLoopEnd (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgLoopEnd (higher)															

bit[31:0]........ PgLoopEnd

This parameter specifies the size of effect buffer (WORD unit) as offset from 000h: PgBase. This value has to be the next address of the last sample. The value must be even number.

008h: PgStart

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PgStart (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
PgStart (higher)															

bit[31:0]........ PgStart

This parameter indicates the number of the processed sample as offset from 000h: PgBase at beginning of the current frame. Before using Effect Slot, this parameter must be initialized.

During using Effect Slot, read PgStart form the Bank that controller does not operate.

000Ch: Temp

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Temp (lower)															
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Temp (higher)															

b[31:0] .... Temp

This parameter is used by the controller for the operation.