YAMAHA LSI

YMF754 (DS-1E)

Hardware Specification

YAMAHA Corporation
Semiconductor Division

Revision 1.01
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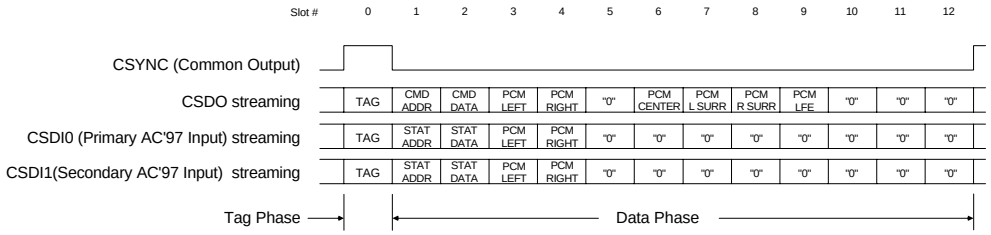
Index

1. AC-link Connection

This chapter describes the format of AC-Link and the connection with AC'97 codec.
DS-1E can support up tp two AC'97 codecs simultaneously that is compliant with AC'97 rev.1.03/2.1.
One AC'97 is supported as Primary AC'97 Audio Codec, and the other AC'97 is supported as Secondary AC'97 Audio Codec. AC-link consists of several signals: *CSYNC*, *CBCLK*, *CSDO*, *CSDI0* (Primary AC'97 Audio Codec), *CSDI1* (Secondary AC'97 Audio Codec), *CRST#.* AC-link can transfer register data and several PCM data simultaneously with 1 sampling rate(1/48000 second) divided into 13 slots.
Below is the format of AC-link.



AC-link Standard Bi-directional Audio Frame

Bit assignment for each slot is described below.

1.1. CSDO: Serial Data Output Stream (DS-1E -> AC'97)

- Slot0: TAG Slot

bit15	Valid Frame. It indicates if CSDO of this frame is valid or not. Always "1" while AC-link is working.
bit14	This bit is "1" when specifying the INDEX address of Primary AC'97.
bit13	This bit is "1" when specifying the DATA of Primary AC'97.
bit12	This bit indicates DAC data of L channel slot is valid. Always "1" after hardware reset. This bit is "0" while AC-link or SRC of DS-1E is under Power down state.
bit11	This bit indicates DAC data of R channel slot is valid. Always "1" after hardware reset. This bit is "0" while AC-link or SRC of DS-1E is under Power down state.
bit10	This bit is always stuck to "0".
bit9	This bit indicates DAC data of Center Channel slot is valid. This bit is "0" after hardware reset. This bit becomes "1" in case of 4CHEN="1", 4CHSL="1" of 0070h: Secondary AC'97 Configuration. Note, it becomes "0" while AC-link or PCI Audio of DS-1E is under Power down state.
bit8	This bit indicates DAC data of L channel Surround slot is valid. This bit is "0" after hardware reset. This bit becomes "1" in case of 4CHEN="1", 4CHSL="0" of 0070h: Secondary AC'97 Configuration. Note, it becomes "0" while AC-link or PCI Audio of DS-1E is under Power down state.
bit7	This bit indicates DAC data of R channel Surround slot is valid. This bit is "0" after hardware reset. This bit becomees "1" in case of 4CHEN="1", 4CHSL="0" of 0070h: Secondary AC'97 Configuration. Note, it becomes "0" while AC-link or PCI Audio of DS-1E is under Power down.
bit6	This bit indicates DAC data of LFE slot is valid. This bit is "0" after hardware reset. This bit becomes "1" in case of 4CHEN="1", 4CHSL="0" of 0070h: Secondary AC'97 Configuration. Note, it becomes "0" while AC-link or PCI Audio of DS-1E is under Power down.
bit[5:2]	This bit is always stuck to "0".
bit[1:0]	These bit indicates Secondary Codec ID only in accessing Secondary AC'97 codec.

The relationship between bit14,13 of TAG Slot and ID bit

R/W Slot1:bit19	Address Slot0:bit14	Data Slot0:bit13	ID Slot0:bit[1:0]	Function
0	1	1	0	Write to Primary AC'97
1	1	0	0	Read from Primary AC'97
0	0	0	1 - 3(*1)	Write to Secondary AC'97
1	0	0	1 - 3(*1)	Read from Secondary AC'97
0/1	1	0/1	1 - 3	N/A
0/1	0	1	1 - 3	No Codecs respond

*1: This number is determined in accordance with Secondary AC'97 ID.

- Slot1: Command Index Address Slot

  bit19 This bit specifies Read / Write. "0" : Write, "1" : Read.

  bit[18:12] Index of Control Register

  bit[11:0] This bit is always stuck to "0".

- Slot2: Command Data Slot

  bit[19:4] Data[15:0] of Control Register

  bit[3:0] This bit is always stuck to "0".

- Slot3: Audio Left Channel Slot

  bit[19:4] Audio data of the Left channel for Master/Docking.

  bit[3:0] This bit is always stuck to "0".

- Slot4: Audio Right Channel Slot

  bit[19:4] Audio data of the Left channel for Master/Docking

  bit[3:0] This bit is always stuck to "0".

- Slot5: Modem Slot

  bit[19:0] This bit is always stuck to "0".

- Slot6: Audio Center Channel Slot

  bit[19:4] Audio data of the Center channel.

  bit[3:0] This bit is always stuck to "0".

- Slot7: Audio Left Surround Channel Slot

  bit[19:4] Audio data of the Left surround channel data.

  bit[3:0] This bit is always stuck to "0".

- Slot8: Audio Right Surround Slot

  bit[19:4] Audio data of the Right Surround channel data.

  bit[3:0] This bit is always stuck to "0".

- Slot9: Audio LFE Channel Slot

  bit[19:4] Audio data of the LFE channel data.

  bit[3:0] This bit is always stuck to "0".

- Slot10-11: Reserved Slot

  bit[19:0] This bit is always stuck to "0".

- Slot12: IO Control Slot

bit[19:0] This bit is always stuck to "0".

1.2. CSDI0:Serial Data Input Stream 0 (Primary AC'97 -> DS-1E)

- Slot0: TAG Slot

bit15 CODEC Ready bit. In case that this bit is "1", DS-1E recognizes the frame data as valid. In case that this bit is "0", DS-1E ignores every input data from Primary AC'97.

bit14 This bit indicates STAT_ADDR of the Primary AC'97 is valid. In case that this bit is "1", DS-1E stores the value of Slot1 bit[18:12] to PRI_STAT_ADDR of 0066h: Primary AC'97 Status Address.

bit13 This bit indicates STAT_DATA of the Primary AC'97 is valid. In case that this bit is "1", DS-1E stores the value of Slot2 bit[19:4] to PRI_STAT_DATA of 0064h: Primary AC'97 Status Data.

bit12 This bit indicates Primary AC'97 ADC data of the L channel is valid. In case that this bit is "1", DS-1E stores the value of slot3 bit[19:4]on CSDI0 as ADC data.

bit11 This bit indicates Primary AC'97 ADC data of the R channel is valid. In case that this bit is "1", DS-1E stores the value of slot4 bit[19:4]on CSDI0 as ADC data.

bit[10:0] DS-1E always ignores these bits.

- Slot1: Status Address Slot

bit19 DS-1E always ignores this bit.

bit[18:12] In case that slot0 bit[14] on CSDI0 is "1", DS-1E stores the value as PRI_STAT_ADDR of the Primary AC'97. In case that slot0 bit[14] on CSDI0 is "0", DS-1E ignores the value.

bit[11:0] DS-1E always ignores these bit.

- Slot2: Status Data Slot

bit[19:4] In case that slot0 bit[13] on CSDI0 is "1", DS-1E stores the value as PRI_STAT_DATA of the Primary AC'97. In case that slot0 bit[13] on CSDI0 is "0", DS-1E ignores the value.

bit[3:0] DS-1E always ignores these bit.

- Slot3: Audio Left Channel Slot

bit[19:4] In case that slot0 bit[12] on CSDI0 is "1", DS-1E stores the value as the Left channel ADC data of the Primary AC'97. In case that slot0 bit[12] on CSDI0 is "0", DS-1E ignores the value.

bit[3:0] DS-1E always ignores these bit.

- Slot4: Audio Right Channel Slot

bit[19:4] In case that slot0 bit[11] on CSDI0 is "1", DS-1E stores the value as the Right channel ADC data of the Primary AC'97. In case that slot0 bit[11] on CSDI0 is "0", DS-1E ignores the value.

bit[3:0] DS-1E always ignores these bit.

- Slot5 - 12: Reserved Slot

bit[19:0] DS-1E always ignores these bit.

1.3. CSDI1:Serial Data Input Stream 1 (Secondary AC'97 -> DS-1E)

- Slot0: TAG Slot

bit15	CODEC Ready bit. In case that this bit is "1", DS-1E recognizes the frame data as valid. In case that this bit is "0", DS-1E ignores every input data from Secondary AC'97.
bit14	This bit indicates STAT_ADDR of the Secondary AC'97 is valid. In case that this bit is "1", DS-1E stores the value of Slot1 bit[18:12] to SEC_STAT_ADDR of 006Ah: Secondary AC'97 Status Address.
bit13	This bit indicates STAT_DATA of the Secondary AC'97 is valid. In case that this bit is "1", DS-1E stores the value of Slot2 bit[19:4] to SEC_STAT_DATA of 0068h: Secondary AC'97 Status Data.
bit12	This bit indicates Secondary AC'97 ADC data of the L channel is valid. In case that this bit is "1", DS-1E stores the value of slot3 bit[19:4]on CSDI1 as ADC data.
bit11	This bit indicates Secondary AC'97 ADC data of the R channel is valid. In case that this bit is "1", DS-1E stores the value of slot4 bit[19:4]on CSDI1 as ADC data.
bit[10:0]	DS-1E always ignores these bit.

- Slot1: Status Address Slot

bit19	DS-1E always ignores this bit.
bit[18:12]	In case that slot0 bit[14] on CSDI1 is "1", DS-1E stores the value as PRI_STAT_ADDR of the Secondary AC'97. In case that slot0 bit[14] on CSDI0 is "0", DS-1E ignores the value.
bit[11:0]	DS-1E always ignores these bit.

- Slot2: Status Data Slot

bit[19:4]	In case that slot0 bit[13] on CSDI1 is "1", DS-1E stores the value as PRI_STAT_DATA of the Secondary AC'97. In case that slot0 bit[13] on CSDI1 is "0", DS-1E ignores the value.
bit[3:0]	DS-1E always ignores these bit.

- Slot3: Audio Left Channel Slot

bit[19:4]	In case that slot0 bit[12] on CSDI1 is "1", DS-1E stores the value as the Left channel ADC data of the Secondary AC'97. In case that slot0 bit[12] on CSDI1 is "0", DS-1E ignores the value.
bit[3:0]	DS-1E always ignores these bit.

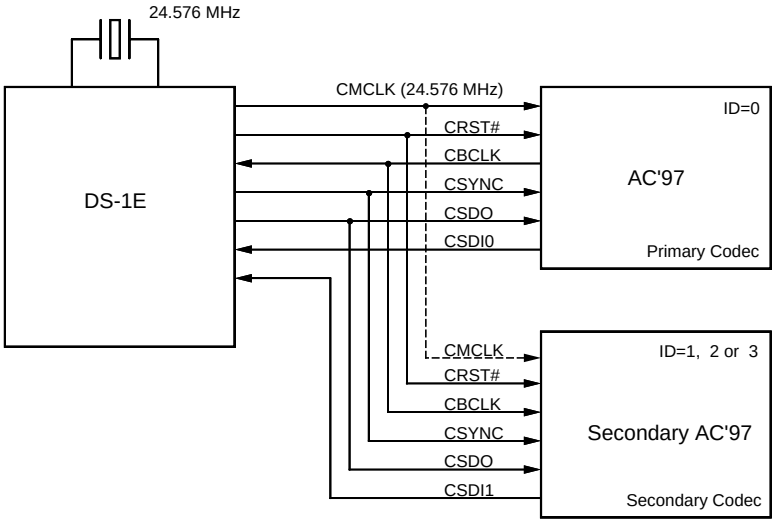
- Slot4: Audio Right Channel Slot

bit[19:4]	In case that slot0 bit[11] on CSDI1 is "1", DS-1E stores the value as the Right channel ADC data of the Secondary AC'97. In case that slot0 bit[11] on CSDI1 is "0", DS-1E ignores the value.
bit[3:0]	DS-1E always ignores these bit.

- Slot5 - 12: Reserved Slot

bit[19:0]	DS-1E always ignores these bit.

1.4. Connection of DS-1E, AC-97 and Crystal



In case that the Secondary AC'97 is working synchronously to CBCLK, CMCLK does not have to be connected to the Secondary AC'97

In case of using the Secondary AC'97 as the Codec at Docking Station, CRST# of Secondary AC97 should be connected to GPIO2 of DS-1E.

2. Power Management

This chapter describes Power Management of DS-1E.
Generally, PCI device can support D0-D3 Power State defined by PCI Bus Power Management.
Audio device is required to support D0, D2, D3 Power State in accordance with Device Class Power Management.
DS-1E supports D0, D2, D3 Power State.
The transition of Power state of PCI Bus Power Management is controlled by OS, however DS-1E does not transit to Power down mode by only changing Power state. So in oder to reduce the power consumption, it is required for the driver of DS-1E to set the corresponding Low power consumption mode to DS-1E when OS notifies the message to transit the Power state.
DS-1E prepares the registers in 4A-4Bh, 4E-4Fh, 5Ah of PCI Configuration registers to control the power consumption of DS-1E.
The table shown in the next page describes the relationship between Power state and Power down Control bit of DS-1E.

The relationship between Power State and Power down bit

	PSFM	PSSB	PSMPU	PSJOY	PSPCA	PSSRC	PSZV	PSDIT	PSDIR	PSACL	PSHWV	CMCD	PSIO	DPLL	DMC	PR5	PR4	PR3	PR2	PR1	PR0
D0	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"
D0_1	"1"	"1"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"
D0_2	"1"	"1"	"1"	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"
D2	"1"	"1"	"1"	"0"	"1"	"1"	"1"	"1"	"1"	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"	"1"
D3hot	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"
D3cold	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

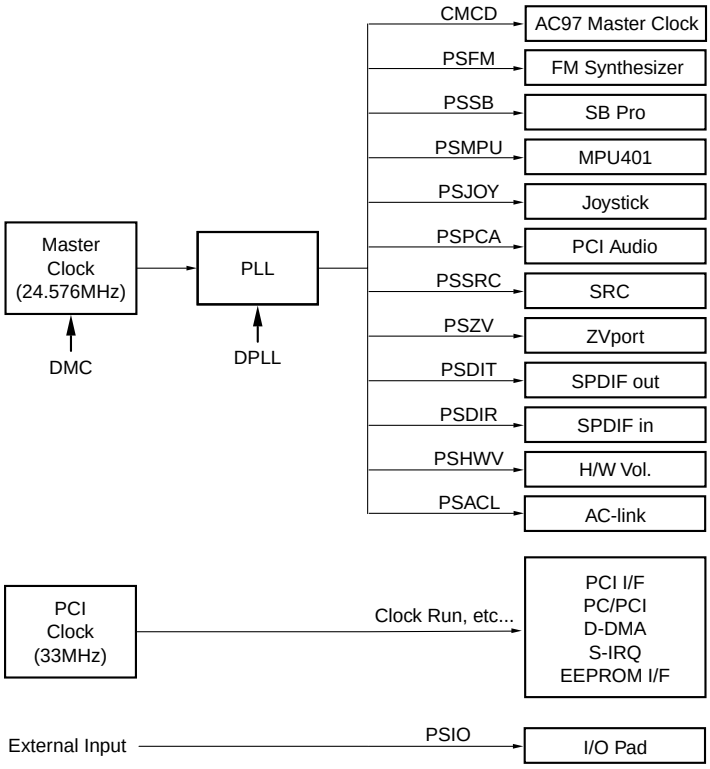
D0 : Full On
D0_1 : Power Down Legacy Audio block only.
Windows98 or WindowsNT or DosBox is closed in Windows95.
D0_2 : No sound from Audio Device. However, input from external Audio is effective.
The device Driver is closed (Wave, Midi, DirectSound, recording Wave, etc is not active) in Windows95/98/NT.
D2 : Audio function is disabled. Only clock oscillating block and analog mixer block are active.
D3hot: All blocks are Power down.

D0_1, D0_2 is uniquely defined by Yamaha.

2.1. Power managed block

DS-1E allows Power management control in block units.

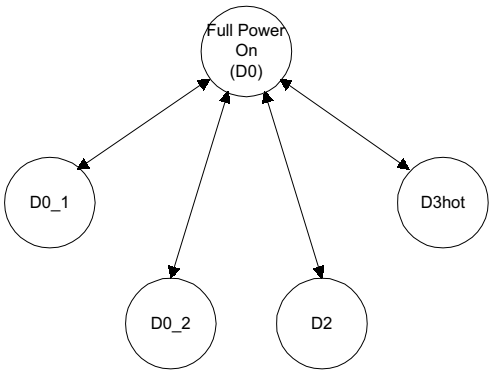
How to control the PCI Clock depends on the System Chipset. To reduce the power consumption exceedingly in Power down mode, it is recommended to stop PCI clock also.



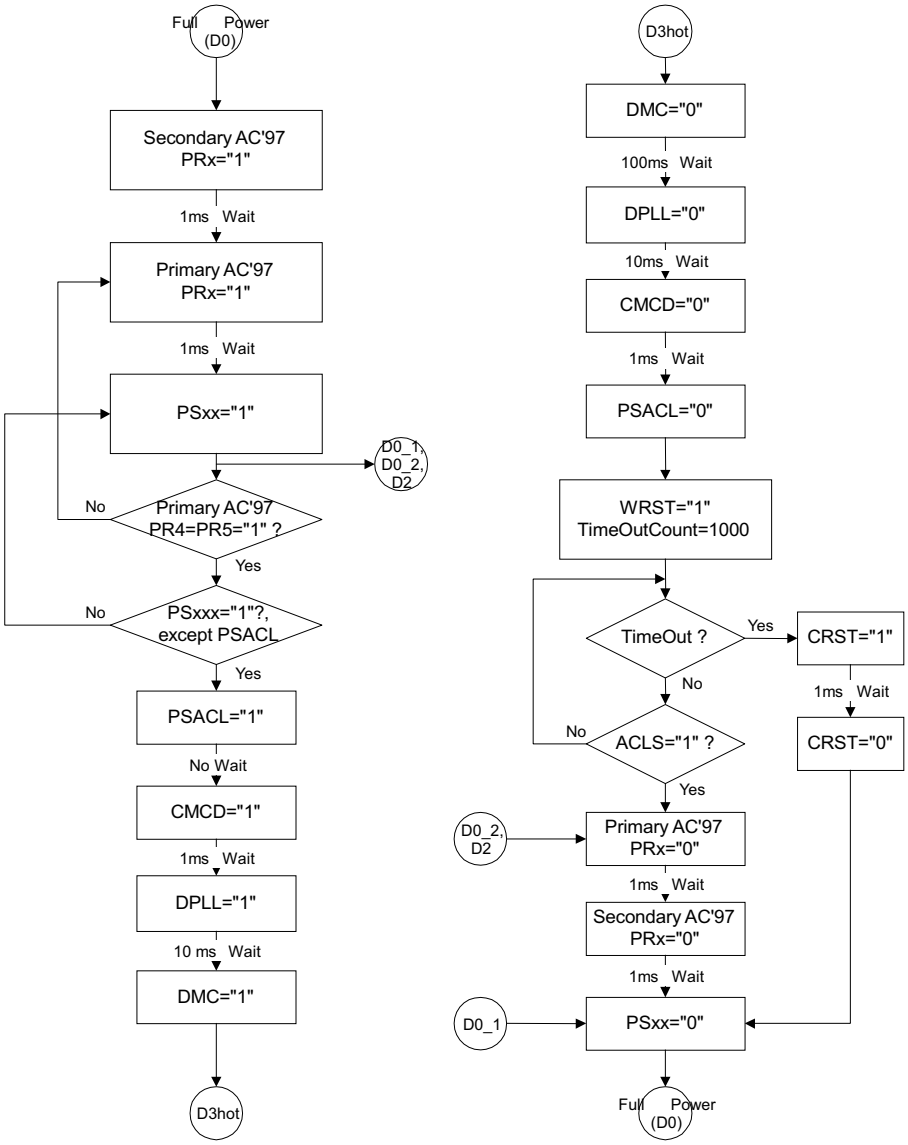
In case that DMC="1", Timer stops.

2.2. How to transit to each state

In transiting to every state by the device drivers, it is recommended to transit to every state via Full Power On state to make process simple.



Follow the flow chart below to transit the state.



Below is the blocks that are needed to be handle carefully.

- Legacy Block

When transition to power saving mode is made for the Legacy blocks, it is required to disable I/O decode.
Write "0" to FMEN, SBEN, MEN, GPEN of 40 - 41h: Legacy Audio Control corresponding to each blocks, before writing "1" to PSFM, PSSB, PSMPU, PSJOY of 4E-4Fh: DS-1E Power Control 2.
Wait time is not necessary for setting Power Save bit, after I/O decode is disabled.
When transition to Power saving mode is mode for the FM Synthesizer block, all of the notes of FM Synthesizer must be off before transition.
When transition to Power saving mode is made for the SB Pro block, it is required to mute SB Voice by SB Mixer and mask interrupt by setting SBEN=IMOD="0" before transition. Note, if transit to Power save mode is made with interrupt asserted, it will keep the state as Interrupt is occurring. In case of using ISA-IRQ, S-IRQ, setting SBEN="0" will mask Interrupt, however in case that INTA# is used, setting SBEN=IMOD="0" is required to mask Interrupt.
When transition to Power saving mode is made for the MPU401 block, it is required to wait more than 10ms to empty the FIFO and set MPU401 to default mode or MEN=MIEN="0" , to mask Interrupt before transition. Note, if transition to Power save mode is made with Interrupt asserted, it will keep the state as interrupt is occurring.
To resume from Power saving mode, after writing "0" to PSFM, PSSB, SBMPU, SBJOY, write "1" FMEN, SBEN, MEN, GPEN to enable I/O decode.
As for Joystick, write "1" then "0" to 4A-4Bh: DS-1E Power Control 1 after resume.
In case to Suspend/Resume DS-1E with SB Pro block active, it is required to save and restore the state machine of internal SB Pro block registers. Refer to 8.2.4. SB Suspend / Resume to save/restore the internal state machine in Suspend/Resume.

- AC-link

When Secondary AC'97 is connected to DS-1E, it is required to place the Secondary AC'97 in Power save mode first.
ID[1:0] of 0070h: Secondary AC'97 Configuration must be set as CodecID of Secondary AC'97 in order to control Power save mode of Secondary AC'97 through 5Ah: DS-1E Secondary AC'97 Power Control.
Since the definition of PR4, PR5 of Secondary AC'97 is different depending on AC'97 Codec manufacturer, be sure to confirm the specification of AC'97 codec manufacture.
If PR4, PR5 of Primary AC'97 is set to "1", the PRx bits of Primary AC'97 and Secondary AC'97 are no longer controlled. Note, it is possible to write PCI Configuration registers of DS-1E, however the transaction will not be made on the registers of AC'97 Codec.
Prior to setting PR4, PR5 of Primary AC'97, it is required to control the PRx bits of Secondary AC'97.
If PSACL of 4E-4Fh: DS-1E Power Control 2 is set to "1", AC-Link is inactive. Controlling PRx bits must be completed before writing PSACL to "1".
When returning from Power save mode of AC-Link, if PR4, PR5 of Primary AC'97 is not set to "1", write "0" to the corresponding bits. In case that PR4, PR5 is set to "1", use Warm Reset of AC'97. To assert Warm Reset, write "1" to WRST of 48-49h: DS-1E Control. Note, WRST will be automatically cleared to "0" by DS-1E.
PR4, PR5 of Primary AC'97 is cleared to "0" after the Warm Reset, however PR4, PR5 of Secondary AC'97 inside DS-1E is still "1" so that the device driver must write "0" after the Warm Reset is done.

- Harware Volume Control

If PR4 (or PR5) of Primary AC'97 is set to "1", AC-link becomes inactive. In this case, low level input to *VOLDW#*, *VOLUP#* PIN will be ignored and the volume of AC'97 will not be able to change, even though the Master Volume of AC'97 is set to change automatically. However, to prevent unexpected change of the Master Volume, disable the Hardware Volume function by setting HYE=0 of 0008h: Global Control, before setting PR4 (or PR5) of Primary AC'97 to "1".
In case of controlling Master Volume through drivers without using automatic change, Power save of AC'97 does not cause any unecpected change of the Master Volume.

Wait time is not necessary till setting PR4(or PR5) to "1" after setting HVE="0".
When returning from Power save mode, set PSHWV="0" of 4E-4Fh: DS-1E Power Control 2 first,then set HVE="1".

- SPDIF Input

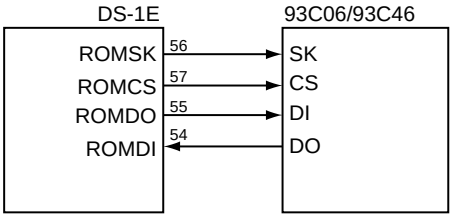
To transit to Power save mode, set DIRE="0", DIRS="0" of SPDIF Input Control before setting PSDIR="1" of 4E-4Fh: DS-1E Power Control 2.
Wait time is not necessary till setting PSDIR to "1" after setting DIRE="0".
When returning from Power save mode, after setting PSDIR="0", restore the value of DIRE, DIRS to the one before entering the Power saving mode.

2.3. Power management mode

DS-1E has two Power management mode. One is PCI Bus Power Management mode and the other is ASL Code Implementation mode. To change the mode, select ACPI bit of 58-59h: ACPI mode.
The difference between two modes is how to notify the Power state capability of DS-1E to OS. In case of PCI Bus Power Management mode, OS reads 52-53h: Power Management Capabilities in PCI Configuration Registers and checks which Power state of PCI is able to use.
In case of ASL Code Implementation mode, OS collects those information from ACPI . However PC'98 specification or later requires PCI Bus Power Management, it will be less likely to use this mode.

3. EEPROM Interface

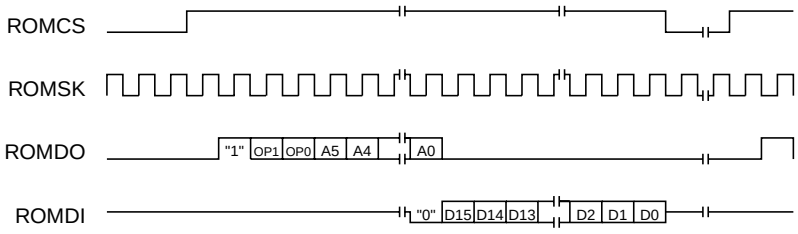
This chapter describes the interface between DS-1E and the external EEPROM.
By connecting EEPROM to DS-1E, it becomes possible to change Subsystem ID, Subsystem Vendor ID of DS-1E without configuring through BIOS or Software. Below is the connection between DS-1R and EEPROM.



(Pin Number is that of YMF754-V)

The EEPROM that DS-1E can support is 93C06 or 93C46, and data width must be 16bit.
DS-1E will read the data from EEPROM through *ROMSK/VOLUP#*, *ROMCS*, *ROMDO/VOLDW#*, *ROMDI* Pins, after the Hardware reset. If EEPROM is connected, DS-1E will read Subsystem ID, Subsystem Vendor ID that user wrote into EEPROM, and transferred to Subsystem ID, Subsystem Vendor ID in PCI Configuration Registers. Once the data is loaded from EEPROM, it is not possible to change Subsystem ID, Subsystem Vendor ID using Subsystem ID Write, Subsystem Vendor ID Write of PCI Configuration Registers. Also after DS-1E loaded the data from EEPROM, *ROMSK*, *ROMDO* Pins for EEPROM Interface change their function to the Hardware Volume Pins.
In case that EEPROM is not connected to DS-1E, the Yamaha Vendor ID will be set to Subsystem Vendor ID, also the device ID of DS-1E will be set to Subsystem ID. In this case, it is possible to change Subsystem ID, Subsystem Vendor ID through Subsystem ID Write, Subsystem Vendor ID Write in PCI Configuration Registers.

3.1. EEPROM Signal Format



The frequency of ROMSK is 32 times of PCI Clock. If PCI Clock is 33MHz, ROMSK is 1.03MHz.
The recovery time of ROMCS in read mode is 2 clocks of ROMSK. It is required to use EEPROM that meets these format.

Below is the table that show the OP Code of 002Ch: EEPROM Control and address, that is changed according to the access mode to EEPROM.

Access mode	OP Code	Address	Data	Comments
READ	10	A[5:0]	-	Normal Read
WEN	00	11xxxx	-	Write mode enable
ERASE	11	A[5:0]	-	Erase
WRITE	01	A[5:0]	D[15:0]	Write
ERAL	00	10xxxx	-	Erase all data
WRALL	00	01xxxx	D[15:0]	Write all data
WDS	00	00xxxx		Write mode disable

The default of access mode after the hardware reset is the read mode.

3.2. EEPROM Data Format

The data in EEPROM is defined as below.

It is recommended to fill the Reserved area with "0" for future extension.

The size of EEPROM is 32 byte in case of 93C06, 128 byte in case of 93C46.

Address (Word unit)	Data
0x00	Subsystem Vendor ID (SSVID)
0x01	Subsystem ID (SSID)
0x03 - 0x0F (0x3F)	Reserved

3.3. EEPROM Data Download

Downloading to EEPROM is controlled by the 002Ch: EEPROM Control. The procedure is described below. Note, when downloading data to EEPROM, set HVE of 0008h: Global Control to "0".

(1) Wait until BUSY of 002Ch: EEPROM Control becomes "0".
(2) Write 0x00300000 to 002Ch. (Enable Write mode)
(3) Wait until BUSY becomes "0". The Wait period is about 40us.
(4) Write 0x00100000 to 002Ch. (Initialize all data to "0")
(5) Wait until BUSY becomes "0". The Wait period is depending on which EEPROM is used, however it is approximately 10ms.
(6) Write (0x00400000+SSVID(Subsystem Vendor ID)) to 002Ch. SSVID should be the Vendor ID that the IHV has registered to PCI-SIG.
(7) Wait until BUSY becomes "0". The Wait period is depending on which EEPROM is used, however it is approximately 10ms.
(8) Write (0x00410000+SSID(Subsystem ID)) to 002Ch. The IHV may define SSID uniquely.
(9) Wait until BUSY becomes"0".
(10) Write 0x00000000 to 002Ch.
(11) Wait until BUSY becomes"0". The Wait period is about 40us.

To verify the data inside the EEPROM, read the EEPROM with the procedure below.

(1) Wait until BUSY of 002Ch: EEPROM Control becomes "0".
(2) Write 0x00800000 to 002Ch.
(3) Wait until BUSY becomes "0". The Wait period is about 40us.
(4) Lower 16-bit of 002Ch becomes SSVID.
(5) Write 0x00810000 to 002Ch.
(6) Wait until BUSY becomes "0". The Wait period is about 40us.
(7) Lower 16-bit of 002Ch becomes SSID.

4. Clock Run Protocol

This chapter describes how to support ClockRun protocol of DS-1E.
ClockRun is the protocol that is defined by Intel Mobile Design Guide. While PCI Bus is Idle (Bus Parking state), it controls supply and stop of PCICLK dynamically, which is equivalent to reducing the clock rate. As the result, the power consumption is reduced.
There is no Pin to Enable/Disable ClockRun function in DS-1E. ClockRun function is always enabled.
In case of using ClockRun function, connect *CLKRUN#* Pin of DS-1E to CLKRUN# line of the system.
In case of not using ClockRun function, connect *CLKRUN#* Pin of DS-1E to GND.

When *CLKRUN#* Pin of DS-1E is connected to CLKRUN# line of the system, DS-1E will drive *CLKRUN#* Pin while transferring or when it starts transferring protocol listed below. The protocol is, if PCICLK stopps, DS-1E requests the Host to supply PCICLK, or if PCICLK is supplied, it controls *CLKRUN#* Pin until the transferring ends.

- PCI Bus Master Write / Read Transfer (PCI Audio, SB D-DMA engine)
- PC/PCI Transfer
- S-IRQ (Quiet mode)

In case that PC/PCI is used for Sound Blaster DMA emulation, it may happens that DS-1E always keep requesting to supply PCICLK to the system after closing the application, which may cause the system not to stop PCICLK. The device driver must reset Sound Blaster block by using DSP Reset command of Sound Blaster, after closing the application that uses Sound Blaster. DS-1E can stop PCICLK responding the request to stop PCICLK after the DSP Reset command of SoundBalster.

5. General Purpose Input / Output

This chapter describes how to control *GPIO* Pins of DS-1E.

5.1. How to control GPIO

DS-1E has 3 *GPIO* Pins. *GPIO[2:0]* can be configured as Input or Output.
When configured as as Input pin, it can be used as Interrupt signal to detect edge sense.
Basically, *GPIO* Pins of DS-1E are configured as below.

GPIO0 output

Can be used to control the mute circuit of the external amplifier in Power Down or AC'97 Reset.

GPIO1 output

Can be used to control the Power down of the external amplifier.

GPIO2 output

Can be used as Reset Pin for Secondary AC'97, in case of using Secondary AC'97 as Docking Codec. (Pull down register is required.)

Input

Can be used to detect the power status of the external Analog circuit.

GPIO Pins becomes Hi-Z when disabled and is Input Pins by default when enabled. So that it is required to put pull up register or pull down register to set the default level for the Pins.
Since *GPIO* Pins are pulled up with several hundred K Ohm inside the chip,10k Ohm resistor is appropriate when Pull up or Pull down is necessry.

Below is the brief explanation of the procedure to control *GPIO* Pins

5.2. Output Pin

1. Write "0" to GPC bit corresponding to the *GPIO* Pin to be used as Output Pin, with the GPE bit of 0058h: GPIO Function Enable register set to "0"(Upper Byte = "00h"). Write "1" to the unused Pins.
2. Set the Level to GPO bit of 0056h: GPIO Output Control register for output pin.
3. Write "1" to GPE bit corresponding to the *GPIO* Pin to be used as Output Pin. Note, do not change lower byte already set to 0058h: GPIO Function Enable register.
4. Later on, set the level to corresponding GPO bit to change the level of the *GPIO* Pin.

5.3. Input Pin (Level Sense Mode)

1. Write "1" to GPC corresponding to the *GPIO* Pin to be used as Input Pin, with the GPE bit of 0058h: GPIO Function Enable register set to "0"(Upper Byte = "00h"). Write "1" to the unused Pins.
2. Set corresponding GPT bit of 005Ah: GPIO Input Type Configuration register to the Level Sense mode.
3. Write "1" to GPE bit corresponding to the *GPIO* Pin to be used as Input Pin. Note, do not change lower byte already set to 0058h: GPIO Function Enable register.
4. Read the level of the Pin from corresponding GPI bit of 0054h: GPIO Input Status register.

5.4. Input Mode (Edge Sense Mode)

1. Write "1" to GPC bit corresponding to the *GPIO* Pin to be used as Input Pin, with the GPE bit of 0058h: GPIO Function Enable register set to "0"(Upper Byte = "00h"). Write "1" to the nused Pins.
2. Set corresponding GPT bit of 005Ah: GPIO Input Type Configuration register to the Edge Sense mode.
3. Write "1" to GPE bit corresponding to the *GPIO* Pin to be used as Input Pin. Note, do not change lower byte already set to 0058h: GPIO Function Enable register.
4. Check GI bit of 0050h: GPIO Input Interrupt Flag register. In case that "1" is read, it indicates the corresponding *GPIO* Pin has been edge-triggered. To reset GI bit to "0", write "1" to the corresponding bit.
5. To use the edge sense detection as Interrupt, write "1" to the corresponding GIE bit of 0052h: GPIO Input Interrupt Enable .
6. If Interrupt has occurred, check GI bit of 0050h: GPIO Input Interrupt Flag register. The bit set to "1" indicates the corresponding *GPIO* Pin has been edge-triggered.
7. To reset GI bit of 0050h: GPIO Input Interrupt Flag to "0", write "1" to the corresponding bit.
   (In case of setting Interrupt mode, Interrupt will be de-asserted if all GI bit are cleared to "0".)
8. The level of each *GPIO* Pin when Interrupt is occurred, can be read from GPI bit of 0054h: GPIO Input Status register.